Development of methods for control of a massively parallel 3D USCT system

Zur Erlangung des akademischen Grades eines

DOKTORS DER INGENIEURWISSENSCHAFTEN (Dr.-Ing.)

von der KIT-Fakultät für Elektrotechnik und Informationstechnik des Karlsruher Instituts für Technologie (KIT)

genehmigte

DISSERTATION

von

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geb. in China

Tag der mündlichen Prüfung: 13.05.2024 Hauptreferent: Prof. Dr. Marc Weber Korreferent: Prof. Dr.-ing. Jürgen Becker

Kurzfassung

In dieser Arbeit wird die Entwicklung und Implementierung des 3D-USCT-III-Systems vorgestellt. Das System ist ein Prototyp einer neuen medizinischen Bildgebungstechnologie für die Erkennung von Brustkrebs im Frühstadium. Einzigartig an diesem System ist seine Fähigkeit zur gleichzeitigen Transmissionsund Reflexionsbildgebung in 3D, von der eine hohe Spezifität bei der Erkennung von Krebsgewebe erwartet wird.

Frühere Systemvarianten zeigten in kleinen Studien vielversprechende Ergebnisse. Das hier entwickelte System soll nun in internationalen multizentrischen Studien eingesetzt werden, um den klinischen Nutzen der Methode statistisch signifikant zu belegen.

Zu den wichtigsten Fortschritten des entwickelten 3D-USCT-III-Systems gehört daher ein fortschrittliches Hardware-Design, um die Anforderungen an die benötige große Bandbreite zu erfüllen, Empfangs- und Sendemultiplexing zu ermöglichen und die mehr als 2000 Ultraschallwandler effizient zu steuern. Dieses Design stellt eine erhebliche Verbesserung gegenüber früheren Iterationen dar und umfasst eine verbesserte analoge Signalübertragung, digitale Steuersysteme und Energieverwaltung. Das System hat nur 13 % mehr Schallköpfe, kann aber sechsmal mehr A-Scans an einer Messposition empfangen, was zu einer 2,3-fachen Beschleunigung der Datenerfassung im Vergleich zum vorherigen Prototyp führt. Die Architektur der Systemkommunikation wurde erheblich verbessert, wodurch Probleme wie Signalreflexionen und Oszillationen gelöst wurden, was zu einer sehr stabilen Kommunikation führt. Darüber hinaus erhöht die Implementierung von programmierbaren globalen Triggern und NOR-Gate-Acknowledge für die Pseudo-Echtzeitsteuerung die Zuverlässigkeit des Systems.

Die ersten Tests des 3D-USCT-III-Systems sind sehr vielversprechend. Tests an Phantomen und Probanden zeigten eine höhere Bildqualität und kürzere Messzeiten im Vergleich zu früheren Systemen. Eine erste klinische Studie ist gerade angelaufen. Das 3D-USCT-III-System ist nun bereit für umfassende internationale klinische Studien und hat das Potenzial, die neue nicht-invasive, kosteneffiziente Methode für die Brustkrebsvorsorge zu werden.

Abstract

This thesis presents the development and implementation of the 3D USCT III system, a novel prototype in medical imaging technology designed for the detection of breast cancer. Unique to this system is its capability for simultaneous transmission and reflection imaging in 3D, which is expected to provide high specificity in the detection of cancerous tissue.

Earlier prototypes showed promising results in small studies. The system developed here is to be used in international multi-center studies in order to provide statistically significant evidence of the clinical benefits of the method.

Key advances in the developed 3D USCT III system therefore include an advanced hardware design to meet the wide bandwidth requirements, enable receive and transmit multiplexing, and efficiently control the more than 2000 ultrasound transducers. This design represents a significant improvement over previous iterations and incorporates improved analog signal transmission, digital control systems, and power management. The system has only 13 % more transducers but can receive six times more A-scans at one measurement position, which results in a 2.3-fold speed up of data acquisition compared to the previous prototype. The architecture of the system communication has been significantly improved, solving problems such as signal reflections and oscillations, resulting in a very stable communication. Additionally, the implementation of programmable global triggers and NOR-gate acknowledge for pseudo real-time control increases the system's reliability.

The initial application and prospects for the 3D USCT III system are very promising. Tests on phantoms and volunteers show higher image quality and shorter measurement times compared to previous systems. A first clinical study has just started. The 3D USCT III system is now ready for extensive international clinical studies and has the potential for becoming the new non-invasive, cost-effective method for breast cancer screening.

Acknowledgment

I would like to take this opportunity to thank all those who have accompanied and supported me during my thesis.

First of all, I would like to thank my supervisor Prof. Dr. Weber, who made it possible for me to carry out this thesis at the Institute for Data Processing and Electronics. His constructive comments, professional guidance as well as the insightful discussion regarding my topic made a decisive contribution to the success of this work.

I am grateful to USCT group leader Dr. Nicole Ruiter. Thanks to her profound knowledge and outstanding support in supervising this work. Thanks also go to the whole USCT group members for the consistently excellent working atmosphere, fruitful discussions, and for their support during the project.

I would like to thank my family and all my friends, especially my parents Mr. Bin Lu and Mrs. Ying Wang. Although they are thousands of kilometers away, their love and encouragement are the keys for me to be able to complete this challenge in a foreign country.

I would like to express my heartfelt thanks to my wife Mrs. Sijia Liu. It is her accompany and motivating words help me go through many difficulties. Thanks to her forbearance, understanding, and support during the past few years. Finally, my deepest gratitude goes to all those who have supported and guided me throughout my academic career.

Contents

1 Introduction

Breast cancer remains the most common malignancy in women worldwide and the leading cause of cancer-related deaths [\[1,](#page-156-1) [2,](#page-156-2) [3\]](#page-156-3). According to statistics shown in Figure [1.1,](#page-12-1) approximately 2.3 million new cases of breast cancer were diagnosed in 2020, ranking as the most frequent of all cancers [\[3\]](#page-156-3). 685,000 people died of breast cancer in 2020. The cases are expected to reach 4.4 million in 2070 [\[2\]](#page-156-2).

Despite the high prevalence of breast cancer, 95 % of patients with early detection are curable [\[1,](#page-156-1) [4\]](#page-156-4). In industrialized countries, with the improvement of medical technology and the popularization of breast cancer screening, the mortality rate

Figure 1.1: Global distribution of new cancers in 2020. [\[2\]](#page-156-2)

Figure 1.2: Traditional Breast Cancer Detection Devices.

of breast cancer has decreased steadily. In contrast, incidence rates are increasing in less affluent societies due to the cost of breast cancer screening [\[5\]](#page-156-6). Therefore, developing safe and affordable breast cancer detection devices has become a hot topic.

Presently, the typically used methods to detect breast cancer (as shown in Figure [1.2\)](#page-13-0) are Mammography (a), Magnetic Resonance Imaging (MRI) (b), and Sonography (c). In mammography, X-ray projections of the compressed breast are created. The limitation of this monitoring method is the high false positive rate of breast cancer due to the poor contrast between the fibroglandular tissue and a potential tumor[\[6\]](#page-156-7). Besides, the patients are exposed to radiation. MRI has a high soft-tissue resolution. However, due to the long imaging time and expensive equipment, MRI is not suited as an early breast cancer monitoring method. Conventional ultrasound devices such as sonography can be used to detect breast cancer without radiation. However, sonography is operator-dependent and has low soft-tissue contrast[\[6\]](#page-156-7). It is not recommended as a stand-alone detection method.

[Ultrasound Computer Tomography \(USCT\)](#page-144-0) is a medical imaging technique that uses ultrasound to generate high-resolution, 3-dimensional images of biological tissues. It works by sending ultrasound waves through the tissue and detecting the echoes, which are reflected and scattered from different parts of the tissue. These echoes are then processed by a computer to create a detailed image of the tissue being imaged. Additionally, transmitted ultrasound is used to calculate images of the speed of sound and attenuation.

[USCT](#page-144-0) has the advantage of being non-invasive, safe, and relatively inexpensive compared to other medical imaging techniques such as X-ray, CT, or MRI.

1.1 Motivation and challenges

Preliminary clinical studies with USCT showed that the method is promising for the early diagnosis of breast cancer and is an important innovation in the field of medical imaging. However, the transition from small-scale clinical studies to large-scale multi-center studies requires the development of a new generation of [USCT](#page-144-0) systems (3D USCT III). The main challenges to achieve this goal are listed in the following.

The 3D USCT III system needs fast measurements, a reliable control system, and the inclusion and management of more transducers. To meet these requirements, the architecture of the 3D USCT III system has to incorporate new component layouts, stable digital communications, and analog signal conditioning. In addition, the architecture should be scalable, allowing flexibility in integrating additional transducers for future development.

In the 3D USCT III system, a large number of hardware components have to be designed for recording very weak ultrasound signals, dispatching many control signals, and overseeing power management. The development of the hardware needs to include theoretical simulations, circuit design implementation, and functional verification. In addition, these various components have to be integrated into the overall 3D USCT III system.

In previous research, a dedicated analog front-end ASIC was designed and fabricated for the system. The challenge here is to integrate the ASIC into the 3D USCT III system design and to fully utilize the performance of the ASIC.

Before integration, characterizing the ASIC is a critical step. Characterization of the ASIC requires rigorous testing under a variety of conditions to fully capture the electrical and temporal properties, which is critical to improving the USCT III

system's ability to perform complex ultrasound computed tomography procedures in a clinical setup.

Developing a 3D USCT III prototype for worldwide clinical studies is not just the final goal of this work, also could be the catalyst for transitioning USCT technology from theoretical concepts to practical clinical application, thereby pushing the boundaries of medical imaging a step forward. 3D USCT III might be the next generation in breast cancer diagnostics, providing a rapid, safe and cost-effective method that could be widely accessible.

1.2 Research questions

This work focuses on the development and integration of the 3D USCT III system for early breast cancer diagnosis, and enabling global large-scale multi-center studies. The research questions are as follows:

- How to design and implement a fast, safe, and reliable 3D USCT III prototype to perform ultrasound computed tomography on a large-scale clinical setting?
- How to get more unduplicated A-scans for a given number of USCT transducers?
- How to design and implement the analog signal chain of the 3D USCT III? What is its bandwidth and amplification performance?
- How to integrate the front-end ASIC into the USCT III system? How to characterize it?

1.3 Structure of the thesis

The research process for the 3D [USCT](#page-144-0) III system can be represented by a Vmodel [\[10\]](#page-157-2) as shown in Figure [1.3.](#page-16-1) The structure of this paper roughly follows the research sequence of the V-model. The chapters corresponding to the segments of the V-model are indicated by different colors in Figure [1.3.](#page-16-1)

Chapter [2](#page-18-0) introduces concepts related to diagnostic ultrasound. It includes an overview of medical ultrasound, ultrasound transducers, ultrasound signal processing, and an introduction to conventional ultrasound techniques.

Chapter [3](#page-36-0) describes the history and principles of USCT and gives a clear definition of USCT. This chapter compares the current USCT systems. In addition, it provides a brief overview of the predecessors USCT II.

Chapter [4](#page-46-0) focuses on the hardware development of the USCT III, describing the steps from system design to actual implementation. This chapter introduces the architectural considerations, component selection, and system integration that enable the USCT III design to achieve its goals.

Chapter [5](#page-96-0) focuses on the validation of the single components as well as the entire system. This chapter discusses the methods, which are used to implement these

Figure 1.3: V-model based development process of USCT III. The colors indicate where the different chapters are located in the V-model.

tests and the results. In addition, the results of current clinical studies are presented and compared to the results of the previous USCT II system.

Chapter [6](#page-138-0) summarizes the entire work and points out some aspects of the future of USCT.

2 Background

This chapter provides the foundation for understanding the basic technology and environment of [USCT](#page-144-0) devices. This chapter is divided into four parts. The first part focuses on the three basic features of ultrasound for medical diagnosis. The second part introduces three types of ultrasonic transducers and their principles. The third section introduces the [Analog Front-end \(AFE\).](#page-142-0) In addition, the last section introduces conventional echo-based ultrasound devices.

2.1 Fundamentals of medical ultrasound

According to the acoustic frequency spectrum, sound waves can be classified as infrasound $(< 20$ Hz), (audible) sound (20 Hz to 20 kHz), ultrasound (20 kHz to 1 GHz), and hypersound (above 1 GHz) [\[11\]](#page-157-3). Medical ultrasound typically operates in the frequency range of 500 kHz to 15 MHz (Figure [2.1\)](#page-19-1). Lowfrequency ultrasound $(< 2 MHz)$ is often used as a medical treatment [\[12\]](#page-157-4). Medical studies proved that high-energy, low-frequency ultrasound can be used to open the blood-brain barrier [\[13\]](#page-157-5). Ultrasound in the high-frequency range $(> 20 \text{ MHz})$ is able to obtain higher resolution due to its shorter wavelength [\[14\]](#page-157-6). Therefore, high-frequency ultrasound is mostly applied for medical diagnostics, such as sonography.

When ultrasound is used for diagnostic purposes, it propagates through body tissues. The propagation characteristics of ultrasound can be used as criteria to differentiate body tissues. These propagation characteristics include sound velocity, attenuation and acoustic impedance. Table [2.1](#page-19-2) shows the propagation

Figure 2.1: Acoustic spectrum [\[15\]](#page-157-7)

Material		Speed of sound Acoustic impedance	Attenuation	Source
	(m s)	$(10^6 \text{ kg/s}^2 m)$	(dB/cm/MHz)	
Water	1480	1.48	0.0025	(Dong et al., 1999)
Fat	1478	1.4	0.48	(Mast. 2000)
Breast	1510	1.54	0.75	(ICRU, 1998)
Cardiac muscle	1576	1.67	0.52	(Mast, 2000)

Table 2.1: Propagation characteristics of ultrasound in different soft tissues

characteristics of ultrasound in several human soft tissues and water. Human soft tissues are similar to water in terms of sound velocity as well as acoustic impedance, but water has a significantly smaller attenuation coefficient.

2.1.1 Speed of sound

Sound waves propagate in a medium. Assuming that ultrasound propagates in an adiabatic process, the speed c of ultrasound propagation is [\[15\]](#page-157-7):

$$
c = \sqrt{\frac{B}{\rho}}\tag{2.1}
$$

where B is the isothermal bulk modulus, which is a measure of the bulk resistance of a material to compression. ρ is the density of the fluid. Thus, sound waves can travel faster in less compressible and less dense media.

Most human soft tissues are composed of cells, and the vast majority of cell is water. The density and bulk modulus of human soft tissues are similar to those of water. Therefore, on a macroscopic scale, the propagation speed of sound waves in human soft tissues is close to that of water.

Figure 2.2: Reflection and transmission of the ultrasound

2.1.2 Acoustic impedance

The acoustic impedance Z of a medium is the product of the density ρ of the medium and the velocity c of the ultrasonic waves in the medium [\[16\]](#page-157-8). According to equation 2.1 of sound velocity, the acoustic impedance is also equal to the product of the square root density as well as the bulk modulus.

$$
Z = c \cdot \rho = \sqrt{B \cdot \rho} \tag{2.2}
$$

Acoustic impedance is an important parameter for the transfer of acoustic energy between two media. Similar to the reflection of light waves at the interface of two media with different optical properties (i.e., refractive index, dielectric constant, or conductivity), sound waves are reflected at the interface of two media with different acoustic impedances [\[16\]](#page-157-8). As shown in Figure [2.2,](#page-20-1) when the acoustic wave reaches the boundary between medium one and medium two, part of the acoustic energy is reflected and the remaining part enters medium two.

The amount of reflected or transmitted energy can be expressed in terms of acoustic impedance. In the special case of waves perpendicular to the boundary plane, the ratio between reflected and incident power α_R is given by:

$$
\alpha_R = \left(\frac{Z_2 - Z_1}{Z_2 + Z_1}\right)^2 \tag{2.3}
$$

The fraction of the incident energy that is transmitted across an interface is described by α_T , where:

$$
\alpha_T = \frac{4Z_2 Z_1}{(Z_2 + Z_1)^2} \tag{2.4}
$$

Ultrasonic reflection and transmission satisfy the law of conservation of energy, where:

$$
P_{total} = \alpha_T * P_{total} + \alpha_R * P_{total} = P_{transmit} + P_{reflect}
$$
 (2.5)

In equation [2.4,](#page-21-0) Z_1 is the acoustic impedance of the medium in which the wave is incident, and Z_2 is the acoustic impedance of the medium behind the boundary plane. Obviously, if the acoustic impedance of the two medium are equal, there will be no reflection (and therefore complete transmission). Conversely, when the impedance shows a strong difference, the power transmission is small. For example, at the water-fat interface, 99.9% of the energy can penetrate the boundary, while less than 0.1% of the energy will form an ultrasonic reflection. At the water-air interface, 99% of the energy is reflected.

In medical imaging physics [\[16\]](#page-157-8), α_R and α_T are defined as the reflection and transmission coefficients, respectively. However, in acoustics and electromagnetism, the reflection and transmission coefficients are usually defined in terms of amplitude, where:

$$
\Gamma_R = \sqrt{\alpha_R} = \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{2.6}
$$

$$
\Gamma_T = \sqrt{\alpha_T} = \frac{2Z_2Z_1}{Z_2 + Z_1} \tag{2.7}
$$

To avoid ambiguity, α_R and α_T are defined here as the power reflection coefficient and power transmission coefficient. Γ_R (reflection coefficient) and Γ_T (transmission coefficient) are following the definition in acoustics.

2.1.3 Attenuation

An acoustic wave is attenuated by molecular absorption of sound energy and by scattering: the wave gradually loses energy when propagating [\[17\]](#page-157-9). For a plane wave, Beer's law applies:

$$
P_0 = P_i e^{-\alpha \triangle x} \tag{2.8}
$$

 P_i is the acoustic power at a certain place, P_0 is the power at a place $\triangle x$ farther in the direction of propagation. The attenuation coefficient α comprises two effects: absorption loss and scattering loss [\[17\]](#page-157-9). In soft tissue, the absorption coefficient accounts for 60% to 90% of the attenuation, and scatter accounts for the remainder [\[16\]](#page-157-8).

$$
\alpha = \alpha_1 f^n \tag{2.9}
$$

Experiments have shown that the attenuation coefficient α is usually proportional to the exponent n of the ultrasound frequency. In Equation [2.9,](#page-22-1) α_1 is the attenuation coefficient of the material at 1 MHz, and f represents the frequency of the acoustic wave. n denotes the attenuation exponent for different materials. Usually, n ranges from 0 to 4. Most soft tissues have an index n between 1 and 2 [\[16\]](#page-157-8).

Figure 2.3: Schematics of ultrasound transducers [\[18,](#page-157-10) [19\]](#page-158-0)

2.2 Ultrasound transducers

The tasks of ultrasound transducers are to transmit and receive ultrasound waves. Figure [2.3](#page-23-1) shows three different transducers. According to the driving principle, the transducer (a) and transducer (b) are based on the piezoelectric principle. The transducer (c) is based on the electrostatic principle.

The theoretical basis of the piezoelectric effect is the electric dipole [\[20\]](#page-158-1). The structure of piezoelectric materials is usually an ion-bonded crystal. At rest, due to the symmetry of the crystal structure, the dipoles formed by the positive and negative ions cancel each other out and the crystal is electrically neutral [\[20\]](#page-158-1). When subjected to pressure, the crystal deforms, the symmetry disappears, and a net dipole moment is created. This dipole moment produces an electric field on the crystal as shown in Figure [2.4](#page-24-1) (a). Conversely, when an electric field is applied to a piezoelectric material, the crystal deforms. This is known as the inverse piezoelectric effect, as shown in Figure [2.4](#page-24-1) (b).

The transducer (a) is a traditional ceramic transducer, which achieves acoustic impedance matching through the matching layer in the front and buffers the signal through the damping layer. transducer (b) is [Piezoelectric Micromachined](#page-143-0) [Ultrasonic Transducer \(PMUT\).](#page-143-0) The [PMUT](#page-143-0) is based on semiconductor processes so that it can achieve high transducer density.

Transducer (c) is a [Capacitive Micromachined Ultrasonic Transducer \(CMUT\).](#page-142-1) Its working principle is to drive the silicon membrane through the electrostatic

Figure 2.4: Piezoelectric effect and inverse piezoelectric effect [\[21\]](#page-158-2)

force to generate ultrasonic waves [\[20\]](#page-158-1). Benefiting from modern semiconductor infrastructure, [CMUT](#page-142-1) and [PMUT](#page-143-0) are capable of submicron-sized transducers and are compatible with application-specific integrated circuits, enabling high-density ultrasonic transducers. However, [PMUT](#page-143-0) and [CMUT](#page-142-1) have not been widely commercialized, and the device performance may vary with wafer substrates, leading to potential challenges in fabricating large arrays with hundreds to thousands of device chips[\[18\]](#page-157-10).

In summary, the ultrasound transducer typically has a huge contrast in the amplitude of the received and transmitted signals. When receiving, it needs to receive electrical signals as low as µV level. During transmission, the ultrasound transducer can operate under several hundred volts in order to maximize the transmission energy.

2.3 Ultrasound analog front-end

The ultrasound [AFE](#page-142-0) focuses on conditioning the signals from ultrasound transducers. The ultrasound [AFE](#page-142-0) is a critical component of an [USCT](#page-144-0) system, and its performance can significantly affect the quality and reliability of the ultrasound images generated. In addition, different types of [AFE](#page-142-0) have different control methods.

Figure 2.5: Simplified ultrasound front-end

Figure [2.5](#page-25-1) shows a simplified [AFE,](#page-142-0) which contains [Transmit \(TX\)](#page-144-1) amplifier, [Transmit/Receive \(T/R\)](#page-144-2) switch, and the [Receive \(RX\)](#page-143-1) amplifier. The excitation signal from [Digital Analog Converter \(DAC\)](#page-142-2) is amplified by [TX](#page-144-1) amplifier, and the amplified excitation signal drives the piezoelectric materials and sends ultrasound via the [T/R](#page-144-2) switch. During the receiving process, ultrasound is converted into weak electric signals by the transducer. Through a low noise amplifier, the analog signal can be acquired by the [Analog Digital Converter \(ADC\).](#page-142-3)

The purpose of the [T/R](#page-144-2) switch is to enable [Time-division multiplexing \(TDM\)](#page-144-3) of the transducer between the receiver and the transmitter. In addition, the [T/R](#page-144-2) switch protects sensitive low-voltage electronics from the high-voltage signals used to drive the ultrasonic transducer. This section describes the different implementations of [TX](#page-144-1) driver, [RX](#page-143-1) amplifier, and [T/R](#page-144-2) switches.

2.3.1 Ultrasound transducer driver

The drive voltage of a piezoelectric transducer usually ranges from a few volts to several hundred volts. The ultrasound transducer driver is responsible for amplifying the signal into the range required by the transducer.

(a) Ultrsound driver (pulser) based on half bridge structure (b) Ultrasound linear amplifier (class-A)

Figure 2.6: Two structures of ultrasound transducer drivers

Figure [2.6](#page-26-1) shows two general schemes of ultrasonic drivers. Figure [2.6](#page-26-1) (a) is a pulse generator (pulser) based on a half-bridge structure. Since transistors Q1 and Q2 work as switches, this pulse generator can effectively amplify pulsed or square wave signals by the alternating conduction of Q1 and Q2. Figure [2.6](#page-26-1) (b) shows a common-emitter Class-A linear amplifier. The [Bipolar Junction Transistor \(BJT\)](#page-142-4) Q operates in the linear range with the base current proportional to the collector current. The collector current through resistor R3 is eventually converted into a voltage signal through Ohm's law to drive the transducer. The static point of the bipolar transistor is configured by two resistors R1 and R2.

Pulsers are highly efficient, simple in structure, and have high power density. However, pulsers can only be driven by pulsed or square waves. In addition, pulsers have high harmonic noise when driving transducers. The analog amplifierbased driver is highly linear and can amplify arbitrary waveforms in the frequency range. However, it is not as efficient as a pulser and it requires a suitable operating point to keep the transistor operating in the linear region.

2.3.2 Amplifier of ultrasound sensor

The ultrasound transducer converts the ultrasound signal into a weak electrical signal. Amplifiers of ultrasound sensor is able to increase the dynamic range of the signal before digitising these electrical signals.

Figure 2.7: Equivalent circuit of a piezoelectric sensor

The equivalent model of a piezoelectric sensor can be formed by combining a current source with linear components such as inductors, capacitors and resistors. A generic equivalent model of a piezoelectric sensor is shown in Figure [2.7.](#page-27-0) The element C_s represents the dominant capacitance of the piezoelectric element; the elements L_m , R_m and C_m are related to the equivalent mass m, the damping factor c and the spring constant k of the piezoelectric element [\[22\]](#page-158-3), respectively. The element R_p represents the internal charge leakage due to energy dissipation.

According to Norton's theorem [\[23\]](#page-158-4), the linear single-port network model of a piezoelectric sensor can be further reduced to a current source and a parallel connected component Z_s . The impedance Z_s of the simplified model can be denoted as:

$$
Z_s = R_p ||(R_s + C_s)||(R_m + C_m + L_m)
$$
\n(2.10)

A voltage or charge amplifier can amplify the weak electrical signal converted by a piezoelectric sensor.

Figure [2.8\(](#page-28-0)a) shows an inverting voltage amplifier. For the operational amplifier, the voltage difference between the non-inverting and inverting inputs is negligible, and the current of the non-inverting input can be considered as 0. (i.e., $U_{+} = U_{-}$ and $I_{AMP} = 0$). Furthermore, according to [Kirchhoff's Current Law \(KCL\)](#page-143-2) and [Kirchhoff's Voltage Law \(KVL\)](#page-143-3) [\[23\]](#page-158-4), the gain of the voltage amplifier is:

Figure 2.8: Voltage and charge amplifiers for ultrasound sensor

$$
G_v = -\frac{U_{OUT}}{U_S} = -\frac{R_{FB}}{R_{IN}}
$$
\n
$$
(2.11)
$$

Here, I_s is the current generated by the charge movement of the piezoelectric material, C_s is the parasitic capacitance of the sensor, and R_{fb} is the feedback capacitance.

In voltage amplifiers, the amplification is dependent not only on the feedback network but also on the impedance Z_S of the piezoelectric sensor itself.

The charge amplifier is essentially an integrator composed of operational ampli-fiers. As shown in Figure [2.8\(](#page-28-0)b), the feedback capacitor C_{FB} replaces R_{FB} . Similarly, the amplification of the charge amplifier can be derived as shown in equation [2.12.](#page-28-1)

$$
G_q = -\frac{dU_{OUT}}{dg} = -\frac{1}{C_{FB}}\tag{2.12}
$$

In a charge amplifier, since the potentials at both ends of the sensor are equal, the current does not pass through the capacitor C_S . Therefore, the gain of the charge amplifier is determined by the feedback capacitance C_{FB} .

Figure 2.9: Simplified schematic of [T/R](#page-144-2) switch based on transmission gate [\[24\]](#page-158-5)

2.3.3 Transmit/Receive switch

Depending on the control method, [T/R](#page-144-2) switches can be divided into manual [T/R](#page-144-2) switches and self-control [T/R](#page-144-2) switches. Manual [T/R](#page-144-2) switches are controlled by external signals. Figure [2.9](#page-29-1) shows a transmission-gate-based [T/R](#page-144-2) switch. It consists of two [Metal Oxide Semiconductor Field Effect Transistors \(MOSFETs\)](#page-143-4) with opposite channel polarities [\(P-channel Metal Oxide Semiconductor \(PMOS\)](#page-143-5) and [N-channel Metal Oxide Semiconductor \(NMOS\)\)](#page-143-6). The gate control voltages (C and \overline{C}) are DC voltages of opposite polarity [\[24\]](#page-158-5). When the gate of the [NMOS](#page-143-6) transistor is high, and the gate of the [PMOS](#page-143-5) transistor is low, the transmission gate is closed [\[24\]](#page-158-5). Therefore, the [PMOS](#page-143-5) is the dominant current pathway for positive voltages. Conversely, the [NMOS](#page-143-6) is the dominant current pathway for negative voltages.

Figure [2.10](#page-30-0) shows a self-controlled [T/R](#page-144-2) switch based on a forward voltage-biased rectifier. It receives and transmits through four diodes D1-4 with forward bias, depending on the input voltage. Diodes D5 and D6 are two clamping diodes to protect the receive amplifier from damage by high voltages.

The self-controlled [T/R](#page-144-2) switches automatically open or close the signal path from the input to the output depending on the level of the input signal. When the amplitude of the input signal is between $V_{ss} + V_f$ and $V_{ss} - V_f$ (receive mode),

Diodes D1-D4 operate in forward bias mode. According to [KCL,](#page-143-2) the following equations [2.13](#page-30-1) valid. By simplification, the input current I_{IN} is equal to the reverse output current I_{OUT} .

$$
\begin{cases}\nI_{dd} = I_1 + I_2 \\
I_3 = I_1 + I_{IN} \\
I_2 = I_{OUT} + I_4 \\
I_{ss} = I_3 + I_4\n\end{cases}
$$
\n(2.13)

In transmit mode, the input voltage is out of the range from V_{DD} to V_{SS} , resulting in either diode D1 or diode D2 being in reverse cut-off mode. When the input voltage is higher than V_{DD} , diode D1 is turned off. When the I_{IN} is less than I_{ss} , the formula [2.13](#page-30-1) is still valid. When the I_{IN} exceeds I_{ss} , due to the limitation of the current source I_{ss} , I_{OUT} is limited to I_{dd} . Conversely, when the input voltage is lower than $V_S S$, I_{OUT} cannot exceed the current source I_{dd} .

Figure 2.10: Self-controlled [T/R](#page-144-2) switch based on forward bias rectifier

$$
I_{OUT} = \begin{cases} I_{IN}, & if \quad I_{IN} \in [-I_{SS}, I_{DD}] \\ I_{DD}, & if \quad I_{IN} < -I_{SS} \\ I_{SS}, & if \quad I_{IN} > I_{DD} \end{cases}
$$
(2.14)

The expression [2.14](#page-31-1) summarizes the relationship between the output current I_{OUT} and the input current I_{IN} in a self-controlled [T/R](#page-144-2) switch. The maximum output current depends on the current source so that the self-controlled [T/R](#page-144-2) switch prevents excessive current from damaging the sensitive receiver amplifier. However, the self-controlled [T/R](#page-144-2) switch cannot completely open the input and output path when the input current I_{IN} is not greater than the current source. As a result, a self-controlled [T/R](#page-144-2) switch has greater crossover distortion in transmit mode than a manually controlled [T/R](#page-144-2) switch.

2.4 System architecture of ultrasound device

Transducers, [AFE,](#page-142-0) [ADC,](#page-142-3) and other elements form the ultrasound system. Two different architectures for digitizing ultrasound signals in the medical field are shown in Figure [2.11.](#page-32-0)

The first architecture utilizes a passive transducer design. The sensor probe integrates multiple piezo elements, and the analog signal from the sensor is transmitted to the Data Acquisition (DAQ) system through cable assembly. The DAQ system is responsible for analog signal digitization and storage.

The second architecture involves digitizing the signal within the probe itself, reducing the distance of the analog signal link. Inside the probe, the data can be accessed by the user interface through a digital data link, such as Ethernet, enabling data readout.

The first approach is commonly employed in many ultrasound devices, such as sonography ultrasound systems in Figure [1.2](#page-13-0) (c). It offers the advantage

Figure 2.11: Two architectures to digitize ultrasound signals in the medical field

of integrating more piezoelectric transducers within a relatively small probe. Different probes can be interchangeably used via a universal adapter to adapt to various tissue measurements. Since the passive probe and electronics are physically separated, the heat generated by the electronic components has a limited impact on the transducers. However, this architecture results in higher system complexity and a larger overall volume. Additionally, addressing the loss of the analog signal during transmission through cables presents a challenge.

The second architecture, as exemplified by the LightProbe project [\[25\]](#page-158-6) in Figure [2.12,](#page-33-0) incorporates digitization within the probe. This device digitizes the signals from 64-channel transducers using electronics housed in a compact space. The digitized data is then transmitted to the computer via an optic data link. This approach minimizes the length of the analog signal chain, reducing analog signal loss. By utilizing highly customized chips such as [PMUT,](#page-143-0) [CMUT,](#page-142-1) and [Appli](#page-142-5)[cation Specific Integrated Circuit \(ASIC\),](#page-142-5) high sensor densities can be achieved. However, heat dissipation within such systems can limit data processing performance and potentially affect the transducers. For the LightProbe, it operates with

Figure 2.12: Digital probe with optical interface [\[25\]](#page-158-6)

a maximum power consumption of 10 W and an average power per channel of about 156 mW [\[25\]](#page-158-6).

The number of transducers in 3D USCT systems far exceeds traditional ultrasound devices, such as sonography devices, by at least an order of magnitude. This significant increase in transducer count presents challenges in terms of signal transmission. The utilization of analog cables to connect the numerous transducers to digitized devices results in inevitable analog signal loss, which is a drawback that USCT systems aim to avoid. Unlike traditional ultrasound devices, USCT systems prioritize minimizing analog signal loss as it can degrade the overall image quality and diagnostic accuracy.

Another concern associated with analog front-end digitization in ultrasound devices is the generation of heat. The conversion process from analog to digital signals produces heat, which can have detrimental effects on temperature-sensitive USCT systems. Hence, it becomes crucial to address the heat dissipation and thermal management requirements during the design of USCT systems.

Due to these factors, designing the USCT system architecture presents a considerable challenge. The choice of architecture ultimately depends on striking the right balance among the number of transducers, signal quality, system size, cost, and specific application requirements to ensure optimal performance and usability of the ultrasound system. Various design considerations, such as signal chain, communication, and power management strategies, need to be carefully analyzed and implemented to achieve the desired functionality and performance in USCT systems.

Figure 2.13: Two scan modes in reflection image

2.5 Conventional ultrasound imaging

Conventional ultrasound instruments, such as ultrasound imaging systems, detect objects by echos. It is based on the principle shown in the figure [2.13](#page-34-1) (a). The transducer emits a signal and the reflection phenomenon occurs when the ultrasound waves encounter the interface of different tissues. The transducer receives the reflected signal. By calculating [Time Of Flight \(TOF\)](#page-144-4) and obtaining the intensity of the received signal, a one-dimensional amplitude signal can be presented. It is known as amplitude scan (A-scan). By combining several A-scans in the two-dimensional X-Y plane, a two-dimensional section of the tissue under test can be reconstructed (see figure [2.13](#page-34-1) (b)). This mode is known as brightness scanning (B-scan).

Starting with the introduction of gray-scale signal processing in 1974, B-mode ultrasound became a widely accepted method [\[26\]](#page-158-7). Advances in transducer shaping led to better spatial resolution and imaging of very small structures (0.5- 1 cm) in the abdomen. The development of real-time systems even led to the possibility of continuous visualization or ultrasound fluoroscopy [\[27\]](#page-158-8). From the clinical aspect, ultrasound was invaluable due to its non-invasiveness, good visualization properties, and relative ease of administration [\[27\]](#page-158-8).

According to the reflection theory in Section 2.1, conventional ultrasound has a relatively strict acoustic impedance limitation for the object under test. When there is a strong acoustic impedance interface, the strong reflection will mask the tissue behind it. For example, it is difficult for ultrasound to penetrate the bonemuscle interface because the reflection coefficient of the bone-muscle interface is close to 1. When the difference in acoustic impedance of the object under test is similar, the reflected ultrasound energy is insufficient for a clear display. This is because most of the energy penetrates the tissue, and conventional ultrasound equipment cannot measure the transmitted ultrasound.
3 State of the art

This chapter offers an in-depth look into the evolution of the [USCT](#page-144-0) system. While the [USCT](#page-144-0) system shares some foundational aspects with traditional ultrasound equipment in its hardware, it differentiates itself significantly through its enhanced complexity and advanced features. The first part of this chapter covers the basic principles, definitions, and historical milestones of the [USCT](#page-144-0) system. The subsequent section highlights the [USCT](#page-144-0) model crafted through the research and efforts of [Karlsruhe Institute of Technology \(KIT\).](#page-143-0)

3.1 Definition of USCT systems

[USCT](#page-144-0) uses ultrasound to produce high-resolution, three-dimensional images of biological tissues. These images can provide detailed information about the structure, composition, and function of the tissue being imaged [\[28\]](#page-158-0). During the measurement, the object being imaged is surrounded by a fixed structured ultrasound transducer array and exposed to sound so that reflected and transmitted images of reflection, speed of sound, and attenuation distributions can be reconstructed. Unlike standard sonography, this method captures both reflection and transmission data, enabling detailed reconstructions of sound speed and tissue attenuation.

While traditional ultrasonography qualitatively illustrates the gradient of acoustic impedance in the human body through reflectivity tomography, it presents challenges in resolution. The B-scan from an ultrasound displays an anisotropic and spatially inconsistent resolution. [\(USCT\)](#page-144-0) offers a solution to these challenges.

Figure 3.1: Sonography (left) and [USCT](#page-144-0) (right) acquisition modes. A phased array focuses on one point in the imaged object for sonography. The focused beam is steered to acquire a slice image. For [USCT,](#page-144-0) unfocused waves are emitted by each transducer sequentially. The acquired signals are then focused during the reconstruction. [\[28\]](#page-158-0)

By optimizing transducer placement and utilizing unfocused methods for both transmission and reception, [USCT](#page-144-0) improves the resolution and consistency of imaging. The distinct modes of acquisition for both methods can be visualized in Figure [3.1.](#page-37-0)

Ultrasound imaging is characterized by a distinct granular background pattern known as speckle, resulting from interference effects. While this prominent speckle noise can serve as a diagnostic tool, offering indirect insights into the tissue being examined, it can also obscure essential features in the image. One effective method to mitigate this noise is through spatial compositing. This technique involves adding B-scan images acquired from multiple angles. Due to their encompassing aperture, [USCT](#page-144-0) systems inherently use compositing.

3D ultrasound systems provide the capability to capture images of a 3D volume. However, at any given imaging position, this volume only represents a tiny portion of the entire object being observed. To represent the entire object or body region of interest, numerous partial volumes need to be captured across the entire area. These individual volumes are then assembled together for a complete representation. An innovative application in this realm is the Automated Whole-Breast

Ultrasound (AWBU, SonoCine) [\[29\]](#page-158-1). This technique is designed to capture reflectivity volumes throughout the entire breast, providing a more objective and systematically documented image than traditional ultrasound scans. Nevertheless, these systems typically employ conventional US scanners to image from a single side. This approach can introduce challenges, including anisotropic and inconsistent resolution and a decline in the signal-to-noise ratio as the penetration depth increases.

3.2 History of USCT systems

The first ultrasound imaging system was developed in the late 1940s and early 1950s by the Austrian psychiatrist and neurologist Dr. Karl Dussik [\[30,](#page-159-0) [31,](#page-159-1) [32\]](#page-159-2). He constructed the ultrasound apparatus shown in Figure [3.2\(](#page-38-0)a) to image the brain and detect tumors. His technique, known as A-mode ultrasound, used two opposing separate transducers to transmit and receive ultrasound waves. The resulting ultrasound waves were recorded on a graph, which could be used to visualize the internal structure of the brain.

Shortly after Dr. Dussik, Dr. George Ludwig of Pennsylvania and his colleagues designed experiments to detect the presence in animal tissue [\[33\]](#page-159-3). In their setup,

(a) Ultrasound apparatus by Dr. Karl Dussik (b) Echo-based ultrasound devices by Dr. George Ludwig

Figure 3.2: The early ultrasound devices

see Figure [3.2\(](#page-38-0)b), a combined transmitter/receiver transducer was used with a very short ultrasound pulse. The echo signal from the reflected ultrasound waves is recorded on an oscilloscope screen. Using this device, Dr. Ludwig was able to successfully image gallstones for the first time [\[34\]](#page-159-4).

The idea of using ultrasound to generate 3D images was first proposed in the 1950s, but it was not until the development of advanced computing technology in the 1970s that the concept became technically feasible. Combined systems that provided both transmission and reflection data from the breast were described by Müller in 1979 [\[35\]](#page-159-5) and by Carson and colleagues in 1981 [\[36\]](#page-159-6). Carson used two directional opposed ultrasound transducers with a center frequency of 3.5 MHz and a bandwidth of 40 %. These transducers were rotated around the patient's breast and lifted while the patient was prone to produce a slice image of the front of the breast [\[36,](#page-159-6) [28\]](#page-158-0).

In 1997, Andrè and colleagues presented a [USCT](#page-144-0) consisting of two circular transducer arrays [\[37\]](#page-159-7). One array had 512 elements with 0.5 MHz centre frequency, the other array had 1024 elements with 1.0 MHz. The resulting images were calculated through diffraction tomography. Waag and Fedewa [\[38\]](#page-159-8) described in 2006 a ring aperture with 2048 transducers with 2.5 MHz (67 % -6 dB bandwidth) for reflection tomography.

Figure [3.3](#page-39-0) shows the most common [USCT](#page-144-0) systems acquire both reflectivity and transmission data and focus on breast cancer diagnosis. These systems can be divided into three types according to their aperture: 2D ring apertures, 2.5D apertures, or 3D apertures [\[28\]](#page-158-0). These systems work within 0.35 to 8 MHz,

Figure 3.3: Structural sketches of a variety of different [USCT](#page-144-0) aperture

System	Modality	Aperture	Freq. range	No.	Motion	In vivo or	
			(Bandwidth)	elements		clinical test	
ANA \overline{S} [50]	Transmission	Semicircle	$3.0 \,\mathrm{MHz}$ (75%)	1024	Rotation	no	
	Reflection				Translation		
OT Scanner 2000 [51]	Transmission	Planar arrays	0.9 MHz (100%)	8x256	Rotation	[44, 45]	
	Reflection	Circular segments	$3.6 \,\mathrm{MHz}$ (70%)	Translation 3x192			
MUT [52, 53]	Transmission	Planar Arrays	8 MHz (50%)	128	Rotation	[48]	
					Translation		
SoftVue [40, 43]	Transmission	Ring	2.75 MHz (100%)	2048	Translation	[47, 46]	
	Reflection						
Prototype us CT [54]	Transmission	Ring	$3 MHz$ (unk.)	2048	Translation	[54]	
	Reflection						
BUTIS [55]	Transmission	Ring	2.25 MHz (unk.)	2048	Translation	[55]	
	Reflection						

Table 3.1: Compare the properties of the current USCT systems

sending unfocused 2D or 3D ultrasound pulses. The more sophisticated systems have acquisition times in the range of minutes [\[28\]](#page-158-0). The total time is dominated by the duration of the movements of the apertures; the travel times of the pulses are almost negligible with current systems [\[28\]](#page-158-0). Table [3.2](#page-40-0) shows an overview of current [USCT](#page-144-0) systems and their properties.

Image reconstruction is computed offline in minutes to hours, often using massive parallelization in clinical studies, e.g. [\[39,](#page-160-4) [40,](#page-160-2) [41,](#page-160-5) [42,](#page-160-6) [43\]](#page-160-3). Since most groups did not provide detailed information on acquisition time, it is estimated that recordings with patients would take 2 to 10 minutes per breast from the available system parameters [\[28\]](#page-158-0). Clinical studies have been described for systems from QT Imaging, Inc. (formerly QT Ultrasound and TechniScan) [\[44,](#page-160-0) [45\]](#page-160-1), Delphinus Medical Systems [\[46,](#page-161-5) [47\]](#page-161-4), MastoScopia [\[48\]](#page-161-3), and KIT [\[49\]](#page-161-6).

3.3 3D USCT device at KIT

A prototype 2D [USCT](#page-144-0) for reflection and transmission tomography was developed at KIT in 2000 [\[56,](#page-162-3) [57\]](#page-162-4). The device has two face-to-face transducer arrays. Each array consists of 16 elements with a center frequency of 2.5 MHz [\[57\]](#page-162-4). The transducer arrays can be moved independently on a ring trajectory and record data for all combinations of a complete ring of 1600 elements with a diameter of 12 cm [\[56\]](#page-162-3). This 2D [USCT](#page-144-0) device was used for the initial evaluation of the reconstruction algorithm.

Subsequently, the prototype of the first fully three-dimensional ultrasound computerized tomography (3D [USCT](#page-144-0) I) was introduced in 2005. The 3D [USCT](#page-144-0) I prototype had 1920 individual transducers arranged in a cylindrical aperture [\[58\]](#page-162-5), as shown in Figure [3.4\(](#page-41-0)a). By rotating, the 3D [USCT](#page-144-0) I could achieve a higher transducer coverage. However, the utilization of vertically arranged sensor arrays depends on the height of the object being measured.

The 3D [USCT](#page-144-0) II shown in Figure [3.4\(](#page-41-0)b), is the second generation successor to the innovative full-array hemispherical aperture. 2041 actors and sensors are grouped in an array of 157 transducers [\[59,](#page-162-6) [60\]](#page-162-7). In addition, the [USCT](#page-144-0) II is capable of

(a) Apature of [USCT](#page-144-0) I device with 1920 transducers (b) Apature of [USCT](#page-144-0) II device with 2041 [\[58\]](#page-162-5)

transducers [\[59\]](#page-162-6)

Figure 3.4: Aperture of [USCT](#page-144-0) I and [USCT](#page-144-0) II devices

(a) TAS electronics in USCT II.

(b) Transducer arrays. Transmit elements in red and receive elements in blue.

(c) TAS II with metal housing.

Figure 3.5: Second generation TAS (TAS II) [\[49,](#page-161-6) [61\]](#page-163-0)

two degrees of freedom of movement, rotating and lifting. The different position measurements improve the transducer coverage.

Figure [3.5](#page-42-0) shows the second generation of Transducer Array System (TAS II) in the [USCT](#page-144-0) II device. Nine sensors are marked in blue, and four actuators are marked in red, as shown in Figure [3.5](#page-42-0) (b). A 28 mm diameter steel housing protects the transducer array, front-end electronics, and control circuitry [\[62,](#page-163-1) [63,](#page-163-2) [59\]](#page-162-6). The transducer array is connected to the front-end electronics via a flexible printed circuit board in Figure [3.5](#page-42-0) (a). The right part of the PCB is a 3-stage amplifier for receiving signals. The first stage is a fixed gain (23.1 dB) low noise amplifier (LNA) designed to amplify the signal with as little noise as possible. The second stage is a variable gain amplifier, which has 4 stages of gain, from 15 to 28

Figure 3.6: Simplified system architecture of data acquisition system in USCT II [\[61\]](#page-163-0)

dB. The third stage unity gain amplifier drives the analog cable via impedance transformation. The left part of the PCB consists of a 1:6 transformer, which enables a linear excitation signal of about 196 V_{nn} . In addition, a [Micro Controller](#page-143-1) [Unit \(MCU\)](#page-143-1) is used to control all electronic components on the front-end [Printed](#page-143-2) [Circuit Board \(PCB\)](#page-143-2) and to communicate with the central board.

The connection between the 157 TAS II and the central control board is established via the stand-mode I^2C bus [\[64,](#page-163-3) [65\]](#page-163-4). This bus serves as a communication interface, allowing the central control board to control the channel selection and gain of each individual TAS II.

Using the I^2C bus in the USCT II system presents several challenges. First, the number of TAS in the USCT II system exceeds the 7-bit address defined by the standard mode I^2C protocol [\[64\]](#page-163-3). Therefore, an I^2C bus expander is required to communicate with all 157 TAS. Second, the $I²C$ bus has a 400 pF load limit [\[65\]](#page-163-4). To overcome this load limitation and increase the stability of the communication system, the I^2C bus drivers were used extensively in the USCT II system. Even though the address and bus load limitations have been solved in hardware, communication errors may still occur. The lack of fault tolerance of the $I²C$ bus means that the USCT II system can lose connection with multiple TAS during the measurement.

The amplified analog signals from the [Front-end Board \(FEB\)](#page-142-0) are digitalized by a customized [Data Acquisition \(DAQ\)](#page-142-1) system. In the [USCT](#page-144-0) II configurations, the [DAQ](#page-142-1) system is composed of 21 expansion boards, which includes one secondlevel card (SLC) and 20 first-level cards (FLC) [\[60\]](#page-162-7). The device characteristics of the Field Programmable Gate Arrays (FPGAs) are provided in Figure [3.6,](#page-43-0) offering an overview of their properties.

By allocating 24 channels to each primary card (FLC), the DAQ system can acquire a maximum of 480 receiver signals simultaneously[\[60,](#page-162-7) [63\]](#page-163-2). The SLC controls the entire measurement process and communicates with the reconstruction PC via ethernet and with the FLCs via the backplane bus [\[60\]](#page-162-7). This high channel capacity allows for a receiver multiplexing factor of three, enabling the acquisition of all possible transmitter-receiver combinations in the 3D [USCT](#page-144-0) II device.

The measurement time of the [USCT](#page-144-0) II system can be determined based on the propagation time of the ultrasound, the number of measurement positions, and the average number of DAQs. The equation for calculating the measurement time is as follows:

$$
T(k, m, t) = k \times [2.3s + 3 \times m(157 \times 4) \times t] + (k - 1) \times 15s \tag{3.1}
$$

In the equation, k represents the number of measurement positions, m represents the averaging factor, and t represents the propagation time of the ultrasound.

The [USCT](#page-144-0) II system hardware is designed to perform measurements rapidly, and it can complete a measurement in just a few seconds when there is no averaging and no movement involved. However, increasing the number of measurement positions and averaging factor are generally necessary to obtain high-quality imaging. In practical scenarios, using 12 motor positions and 8 averages as measurement parameters can improve the overall image quality by reducing noise and enhancing the signal-to-noise ratio. Achieving such a measurement takes around 270 s.

4 Developing hardware for third generation USCT

As previously discussed, the [USCT](#page-144-0) II device has demonstrated its effectiveness and advantages in early breast cancer detection. Building on the success of its predecessor, [USCT](#page-144-0) III aims to further amplify the capabilities of ultrasound computed tomography and to be a prototype for worldwide large-scale clinical studies.

To realize these objectives, the [USCT](#page-144-0) hardware system incorporates several significant advancements and enhancements. This involves the application of cuttingedge technologies such as high-speed data acquisition systems, new [Transducer](#page-144-1) [Array System \(TAS\)](#page-144-1) based on customized [ASIC,](#page-142-2) and efficient system architecture. By optimizing the process of the system's data acquisition, [USCT](#page-144-0) III is anticipated to considerably decrease the time for data acquisition, thus expediting and enhancing the efficiency of diagnostic procedures.

Consequently, the objective of this chapter is to show the [USCT](#page-144-0) III system from a hardware perspective. This includes an analysis of the [USCT](#page-144-0) III system architecture, multiple simulations, and implementation for the essential components, and a thorough exploration of the measurement process.

4.1 System design

The design of the [USCT](#page-144-0) III system focuses on addressing three primary challenges: reducing measurement time, digitizing signals from a larger number of transducers, and establishing a secure and stable system architecture.

In the evolution of ultrasound computed tomography systems, the [USCT](#page-144-0) III represents a significant step forward, especially when it comes to the capacity of its [TAS.](#page-144-1)

As illustrated in Figure [4.1,](#page-47-0) the transducer number of the [TAS](#page-144-1) in the [USCT](#page-144-0) III system has been increased from 13 in the [USCT](#page-144-0) II to 18 in the latest iteration. In the previous [USCT](#page-144-0) II, each transducer was multifunctional: it could both emit and detect ultrasound. However, the [AFE](#page-142-3) constrainted the use. Consequently, the 13 transducers were allocated distinct roles: four functioned as transmitters, while the remaining nine were dedicated receivers.

While designing the [USCT](#page-144-0) III system, certain constraints pertaining to the aperture dimensions necessitated design modifications. As a consequence, the quantity of [TAS](#page-144-1) in the [USCT](#page-144-0) III system was trimmed from the original 157 (as in the [USCT](#page-144-0) II) down to 128. However, a noteworthy observation is that despite this

Figure 4.1: Transducer array of [USCT](#page-144-0) II to Transducer array of [USCT](#page-144-0) III

Figure 4.2: A-Scans per aperture position (A-Scans/AP) for [USCT](#page-144-0) II an[d USCT I](#page-144-0)II over the number of transducers. The red dashed-dotted line indicates 10 million A-Scans, which are acquired for one image.

reduction in the [TAS](#page-144-1) count, the total number of transducers in the [USCT](#page-144-0) III system experienced a growth of approximately 13 %.

To harness the potential offered by the augmented number of transducers in the [USCT](#page-144-0) III system, time division multiplexing has been integrated. This methodological shift ensures the simultaneous multiplexing of both transmit and receive functionalities, facilitating an increase in the quantity of A-scans for each aperture position. As illustrated in Figure [4.2,](#page-48-0) an elevation in data acquisition efficiency can be observed. Specifically, for each aperture position in the [USCT](#page-144-0) III system, the number of A-scans surges from the previous 0.89 million in the [USCT](#page-144-0) II system to 5.3 million. This jump signifies 598 % enhancement.

To put this into perspective, the amount of data gathered for each aperture position in the [USCT](#page-144-0) III system is the same amount of data collated across six distinct aperture positions in its predecessor, the [USCT](#page-144-0) II system. The details of how the

Figure 4.3: Architecture of the USCT III device

transducer multiplexing functions, along with the strategic control mechanisms, are given in the subsequent chapters.

Studies [\[49,](#page-161-6) [63,](#page-163-2) [28\]](#page-158-0) show that the overall amount of 10 million A-scans for one high-quality [USCT](#page-144-0) image is necessary, it can be inferred that achieving a movement-free 3D [USCT](#page-144-0) device becomes plausible when the count of multiplexed transducers in a [USCT](#page-144-0) system ascends to 3,263. Based on Equation [3.1,](#page-44-0) it is clear that each aperture position requires 15 seconds of movement. Without movement, the [USCT](#page-144-0) system can notably shorten the overhead associated with measurement time. This forward-thinking approach to scalability was considered during the design of the [USCT](#page-144-0) III system, laying a foundation for future upgrades involving additional transducers for the implementation of a movement-free [USCT](#page-144-0) system.

The choice of system architecture plays a key role in achieving optimal performance for the [USCT](#page-144-0) III system. As illustrated in Figure [4.3,](#page-49-0) the [USCT](#page-144-0) III integrates the dual architectures described in section [2.4,](#page-31-0) in a distributed front-end architecture. This architecture is designed to facilitate tight and direct integration of the transducers and [AFE](#page-142-3) components. By reducing the gap between the transducers and the [AFE,](#page-142-3) the system avoids the employment of long cables, which are often responsible for signal degradation and attenuation.

The distributed front-end has a control unit to receive control commands from the [DAQ](#page-142-1) system. At the same time, analog and digital signals from amplifiers as well as drivers are connected to the [DAQ](#page-142-1) via analog and digital cables. This allows communication between the [DAQ](#page-142-1) system and the [AFE.](#page-142-3)

Figure 4.4: USCT III system diagram

Analog signals, conditioned by the [AFE,](#page-142-3) are digitized at the back end by a general purpose [DAQ](#page-142-1) system. This centralised digitisation process has several advantages. By separating the [DAQ](#page-142-1) from the [AFE,](#page-142-3) the heat generated by the digitization process can be directed away from the sensitive sensor components, thus reducing the potential negative impact of temperature rise on [AFE.](#page-142-3)

Based on these considerations, a system architecture diagram based on a distributed front-end (see Figure [4.4\)](#page-50-0) was introduced. The [TAS](#page-144-1) is the smallest unit in the system, each integrating 18 transducers and a [FEB.](#page-142-0) The FEB includes customised [ASIC](#page-142-2) and [MCU.](#page-143-1) They perform functions such as signal amplification, channel multiplexing, and temperature measurement. Detailed information about the [TAS](#page-144-1) is provided in Section [4.4.](#page-69-0)

One distribution board connects 32 [TASs](#page-144-1) to form a cluster of 32 x 18 piezoelectric transducers each. The distribution board is responsible for bridging and isolating the digital and analog signals between the [DAQ](#page-142-1) system and the [TASs.](#page-144-1) In addition, the power control unit and channel control mechanisms on the distribution board ensure patient safety by limiting the maximum ultrasound power. The distribution board is described in detail in chapter [4.3.](#page-60-0)

The [USCT](#page-144-0) system utilizes a two-dimensional matrix system architecture that simplifies communication and control between [TASs.](#page-144-1) This design facilitates the simultaneous transmission of analog signals, digital control signals, and power to each [TAS.](#page-144-1) The matrix structure enables parallel operation and synchronization of multiple [AFE,](#page-142-3) which helps to improve the overall functionality and performance of the [USCT](#page-144-0) III system.

In the [USCT](#page-144-0) system architecture, the analog signal chain is represented in the x-direction. The process begins with the transducer capturing the ultrasound. The [AFE](#page-142-3) amplifies the signal, which is then transmitted over coaxial cable. To maintain signal integrity and prevent signal loss, the analog signals are isolated through distribution boards. Finally, the analog signals are digitised by the [DAQ](#page-142-1) (Data Acquisition) system.

The control signal chain is represented in the Y direction. The control signal chain can be divided into synchronous and asynchronous links. Synchronous link is ring shaped and is used to control components that need to be synchronised for the distribution boards and the [FEB.](#page-142-0) asynchronous communication link is used to control components that do not have high time requirements. Examples include motors and temperature sensors. The control signal links are detailed in Chapter [4.2.](#page-52-0)

The [USCT](#page-144-0) III system consists of four sensor groups supporting a total of 2304 sensors. Each sensor group is connected to a two-dimensional matrix. When the [DAQ](#page-142-1) system has enough analog channels, up to 32 sensor groups can be configured to support up to 18,432 transducers.

4.2 Digital communication

The communication system in [USCT](#page-144-0) III needs to communicate efficiently with a variety of devices. These devices are classified into two categories: time-critical devices and non-time-critical devices, depending on their impact on measurement time. For time-critical devices, such as [FEBs](#page-142-0) and distribution boards, the main objectives are achieving the shortest communication time and precise synchronization. These devices require a dedicated bus optimized for fast data transfer and coordination among time-critical components, ensuring accurate and synchronized measurements.

On the other hand, non-time-critical devices like temperature sensors, aperture position sensors, and motors can be controlled using a regular field bus, providing basic communication and control functionalities without significantly affecting measurement time. By employing separate buses for each category, the [USCT](#page-144-0) III system efficiently manages its devices, prioritizing measurement accuracy for time-critical components while maintaining smooth operation for non-timecritical peripherals, ultimately enhancing system stability and reliability.

4.2.1 Global trigger

Synchronisation of multiple time-critical devices within a [USCT](#page-144-0) system is important for accurate imaging and data acquisition. However, the typical communication bus broadcast approach cannot ensure reliable confirmation that all devices have successfully received the trigger signal in real time.

Therefore, [USCT](#page-144-0) III employs a sequential trigger-response mechanism known as STEP/ACK. The trigger broadcast (STEP) is followed by an acknowledgement signal (ACK) from each component (see Figure [4.5\)](#page-53-0). This approach confirms the synchronisation of all devices. In addition, the ACK signal monitors the operating status of each device and provides a prompt response to any errors that occur.

As shown in Figure [4.5,](#page-53-0) the system is divided into four layers: the mainframe [\(DAQ\)](#page-142-1), the isolation board, the distribution board, and the [FEB.](#page-142-0) The STEP signals are generated by the [DAQ,](#page-142-1) pass through the isolation board, and the distribution board ultimately reaches the FEB. The $STEP_I$, $STEP_D$, and $STEP_T$ are all single-master signals. This layered approach optimizes signal distribution, but there is a time trade-off due to the cascade design.

However, this structure has its limitations. Simultaneous responses such as ACK_T and ACK_D from multiple slave devices can lead to communication conflicts. The solution for the [USCT](#page-144-0) III system is a not-or (NOR) logic mechanism. This mechanism essentially waits for the least responsive device to respond before proceeding, thus ensuring collective readiness before making any subsequent measurements.

Figure [4.6](#page-54-0) shows the simplified schematic of the ACK_T signals, i.e. the response signal from [TAS](#page-144-1) to distribution board. The ACK_T signals (DI_A to DI_H) are

Figure 4.5: Simplified timing diagram of STEP/ACK for USCT III, where blue represents trigger signal and red represents acknowledgement signal. The x-axis represents each time node. t_{AB}, t_{CD}, t_{IJ} , and t_{KL} : The hardware latency from the isolation board. t_{BE} :Configuration time of the distribution board. t_{FG} : Configuration time of the [TAS.](#page-144-1) t_{HI} Configurable time variable, t_{IJ} C Configurable timeout.

gathered via an open-drain structure. This structure is equivalent to an eight-input NOR gate. When the [TASs](#page-144-1) do not respond, i.e., the DI_A to DI_H levels are low, the pull-up resistor will hold the signal $DOut$ level high. At this time, the ACK_T signal is in the Idle state. When at least one [TAS](#page-144-1) sends the ACK_T signal, the corresponding transducers pull the ACK_T signal down and the $DOut$ signal is low. DOut resumes the Idle state until all [TASs](#page-144-1) release the ACK_T signal. The distribution board uses the Dout signal to determine whether this group, totaling eight [TASs,](#page-144-1) has completed configuration.

Among the isolation board and the distribution board, the ACK_D signal is designed with the same concept. Due to the long distance between the distribution boards and the isolation board, ACK_D is implemented as a differential signal pair based on RS485 specification [\[64\]](#page-163-3) as shown in Figure [4.7.](#page-55-0)

 ACK_D signals of distribution boards $(ACK_{D1}$ to ACK_{DN}) control the enable terminal of the RS485 transmitters. When the RS485 transmitters are disabled, the three-resistor divider ensures that $V_A - V_B$ is greater than the RS485 positive threshold voltage (typically 200 mV), and thus the ACK_{OUT} output level is high. This process is equivalent to the idle status of the ACK_T signal. When at least

Figure 4.6: Simplified diagram for processing ACK signals (DI_A to DI_H) from [TASs](#page-144-1) to distibution board. Each ACK signal is connected to an open-drain structure consisting of a pull-up resistor and a transistor. The digital logic of this structure is the equivalent of a NOR gate with 8 inputs.

one distribution board enables the RS485 transmitter via ACK_D , the transmitter drives $V_A - V_B$ below the negative threshold voltage. This process is equivalent to the block status of the ACK_D signal. Similarly, when all distribution boards complete their tasks, i.e., disable the transmitter, ACK_D reverts to idle status.

All the slave devices can pull the bus low to acknowledge the receipt of a signal and release the bus when the task is complete. Importantly, if any device fails during operation, the system initiates a time-out feature that allows the [DAQ](#page-142-1) to continue operation bypassing the failed components, thus increasing the system's robustness.

However, this complex setup does introduce ambiguity; when signals are merged through NOR operation, the [DAQ](#page-142-1) cannot tell which particular [TAS](#page-144-1) or distribution board responded. The solution here is the Enhanced Step Acknowledgement System. By assigning specific execution times to events and utilising the [DAQ'](#page-142-1)s precise timer, the system can distinguish these unique timings from acknowledgement signals.

Figure 4.7: Simplified diagram of the processing of ACK signals $(ACK_{D1}$ to ACK_{DN}) from the distribution boards to the isolation board. The ACK signals from the distribution boards control the RS485 transmitters. When the RS485 transmitter is enabled, the bus is pulled down $(V_A - V_B < -200mV)$. When the RS485 transmitter is disabled, the transmitter is in high impedance state. The idle state of the bus $(V_A - V_B > 200mV)$ is achieved by a voltage divider consisting of three resistors $(R_P, R_T, \text{and } R_D)$. This circuit is equivalent to a NOR operation on the differential ACK signals.

In summary, the [USCT](#page-144-0) III system's approach to synchronisation ensures harmony between components, which is critical for applications such as ultrasonic testing. By ensuring that every signal, step and acknowledgement is carefully timed and synchronised, the system produces reliable and accurate results.

4.2.2 Bus communication

The global triggering mechanism effectively reduces the bandwidth requirements for communication broadcast triggering by uniformly synchronising individual devices. Before starting a measurement, the system can be pre-configured at a lower baud rate over the communications bus as needed to set the correct parameters and state for all subsystems.

A major advantage of this approach is that pre-configuration can be performed in advance without affecting the execution of the measurement. As long as the preconfiguration is done during the disinfection and cleaning process of the [USCT](#page-144-0) III device (e.g. 15 minutes), the measurements will not be affected. For example, in the previous generation of [USCT](#page-144-0) system, even Inter Integrated Circuit (I^2C) communication speeds of only 400 Kbit/s were sufficient to complete all preconfiguration tasks in 15 minutes. Therefore, ensuring the stability and reliability of the system's communication may be more important than speed, and [USCT](#page-144-0) III follows this design philosophy by placing more emphasis on communication stability than high-speed communication.

The communication architecture of the [USCT](#page-144-0) III system can be simplified into a three-layer [Open Systems Interconnection \(OSI\)](#page-143-3) model [\[66\]](#page-163-5) (Figure [4.8\)](#page-57-0). This model encompasses the transmission medium, physical layer, data link layer, and application layer. Primarily, the physical layer is tasked with the transformation of bit-wised data through diverse media such as twisted pair cables and optical fibers. The data link layer then packages this bit-wised data into data frames, which include protocol control bits and the actual data. Furthermore, the data link layer supervises data flow control, collision prevention, and error detection mechanisms. The application layer, being the only layer that directly interacts

Figure 4.8: Simplified OSI model of [USCT](#page-144-0) III device

	Bus System						
Features	$\overline{I^2C}$	CAN 2.0	RS485 Modbus	$10BASE-T1S$			
Nodes	127	>100	254				
Speed	< 0.4 Mbps	≤ 1 Mbps	$<$ 50 Mbps	< 10 Mbps			
Topology	Tree/Bus	Bus/Tree	Bus/Ring/Tree	P ₂ P/Bus			
Distance	Short	Long	Long	Middle			
Power	Low	Middle	Middle	High			
Cost	Low	Middle	Middle	High			
Implementation	Low	Middle	Middle	High			

Table 4.1: [C](#page-0-0)omparison of CAN, RS485, Ethernet, and I^2C

with user data, verifies the data via software and conveys the validated data to the end consumers.

The physical layer directly affects communication speed, drive capability, and interference immunity. The characteristics of the physical layer are mostly determined by the physical layer protocols and topology. Table [4.1](#page-57-1) represents the protocols that are centrally applicable to the multi-point configuration, where I^2C I^2C is the synchronous bus used in USCT II, RS485 is the field bus protocol used in industry, and CAN is the well-known bus protocol for the automotive industry. 10 BASE-T is one of the newest ethernet protocols focused on the field bus.

Figure 4.9: Topologies of digital communication.

Among the four protocols, only the I^2C I^2C uses single-ended wires to transmit data and clock. As the length of the wires increases, the interference on the clock and data wires, as well as as the asymmetry of the wire lengths, increases the error rate of the $I²C$ $I²C$ bus. This phenomenon has also been observed in the [USCT](#page-144-0) II system.

In the physical layer, topologies represent different ways of connecting devices. As shown in the Figure [4.9](#page-58-0), the most common topologies are: daisy-chain, bus and star. Daisy-chain is the most recommended topology. The reason is that the devices are connected only by the backbone. It has better impedance continuity and reduce communication errors caused by signal reflections. The distribution boards of the USCT III are connected in this way.

In a bus topology, devices are connected to the backbone via short cables. Such short cables are called "stubs". Due to the presence of stubs, the impedance continuity of the backbone network is affected. This can cause signals to reflect during communication.

The TAS of the USCT III is connected to the distribution board via a star topology. Impedance discontinuities in the star topology can lead to signal reflections and oscillations. To address this issue, simulations and solutions are given in the chapter [4.5.](#page-81-0)

The data link layer in the OSI model is responsible for encapsulating bits into frames, facilitating frame-based data transmission. Additionally, this layer can implement data validation, conflict detection, and other functions as defined in various standard communication protocols.

For example, in a CAN bus, the data link layer is specified and conflict-free detection is achieved through the Carrier Sense Multiple Access/Collision Avoidance (CSMA/CA) [\[67\]](#page-163-6). This feature enables multiple sensors to transmit information concurrently, making the CAN bus more suitable for networks that necessitate simultaneous data transmission. The inbuilt arbitration mechanism ensures effective and systematic communication among multiple nodes in the network.

In contrast, RS485 only defines signals at the physical layer, and leaves the data frame format and arbitration to be implemented in the software or microcontroller firmware. This grants RS485 greater flexibility in terms of communication patterns between master and slave nodes. In the context of USCT III systems, data frames with long payloads minimize communication overheads; for instance, in CAN 2.0 mode, the maximum payload length is 64, but the RS485 protocol can be customized [\[67\]](#page-163-6).

10BASE-T1S is a newly introduced single-pair communication protocol based on the network protocol. The advantage of 10BASE-T1S is that it enables the implementation of a single communication protocol throughout the system, simplifying the network architecture and reducing complexity [\[68\]](#page-163-7). However, 10BASE-T1S supports less number of nodes than RS485 and CAN, requiring the integration of routers to facilitate communication across a larger network. As a result, in multinode scenarios, 10BASE-T1S does not offer benefits in terms of power efficiency, hardware cost, or ease of implementation.

The communication design of the [USCT](#page-144-0) III system reflects the high priority given to stability. The single-ended signal line of the $I²C$ $I²C$ bus may result in signals that are susceptible to interference and noise, and therefore it is excluded from the

(a) Front side of the distribution board

(b) Back side of the distribution board

Figure 4.10: Distribution board V3.0

[USCT](#page-144-0) III system. Despite the significant advantages of 10BASE-T1S in terms of speed, arbitration mechanism and flexibility, its size and power consumption limit its use in [USCT](#page-144-0) III systems. Eventually, both CAN and RS485 were implemented in the existing [USCT](#page-144-0) III system. Both of them support long distance communication and have good resistance to electrical noise. RS485 was chosen as the main communication interface for [USCT](#page-144-0) III due to its higher flexibility.

4.3 Distribution board

The distribution board (see Figure [4.10\)](#page-60-1) in the [USCT](#page-144-0) III system is the central hub, which connects all the [TAS,](#page-144-1) ensuring digital communication and analog data transfer. There are 32 Hirose Electric 30-pin connectors on the back of the distribution board. These connectors facilitate the connection of 32 TAS that can receive signals from multiple transducers simultaneously.

The front of the distribution board has 96 single-ended to differential buffers. These buffers are based on isolation transformers and play a vital role in converting and protecting the three analog signals collected by each [TAS.](#page-144-1) By converting the single-ended signals to differential signals, they help reduce noise and interference and ensure signal integrity.

To send the processed signals to the [DAQ](#page-142-1) system, the distribution board utilises 24 RJ-45 connectors. These connectors are located on both sides of the board and can carry a total of 96 differential signal pairs, ensuring efficient and clear data transmission.

In addition to these connectors, there are three RJ-45 connectors on the distribution board with specific functions. One of them is dedicated to the input of an excitation signal. The distribution board can multiplex the external signal to selected [TAS.](#page-144-1) The other two RJ-45 connectors are dedicated to communication. They are used to handle the STEP/ACK trigger signals and are also hosts for the RS485 communication bus.

4.3.1 Power management

The distribution board in the [USCT](#page-144-0) III system manages power distribution to the 32 [TASs](#page-144-1) and on-board amplifiers. With each [TAS](#page-144-1) designed to draw a current of 100 mA, the collective power demand from the [TAS](#page-144-1) units alone amounts to approximately 3.2 A. Beyond this, the integrated amplifiers on the board contribute an additional consumption of 400 mA.

This scenario becomes particularly challenging given the presence of numerous capacitive loads in parallel configurations, prominently from the FEBs and the decoupling capacitors. These components can induce significant inrush current during the system power-up phase. To circumvent potential hazards and system instabilities a power control unit was designed. This unit ensures a safe and smooth system power-up.

In order to gain insight into the behaviour of the distribution board under these conditions, a simplified load equivalent circuit for a single [FEB](#page-142-0) (see Figure [4.11\)](#page-62-0) was investigated. The circuit includes several key elements, including a cable

resistance (R_C) of 400 m Ω for the 800 mm micro-coaxial cable, a [FEB](#page-142-0) static load resistance (R_L) of 100 Ω based on a 5 V power supply and 100 mA quiescent current, a decoupling capacitor (C) totalling 30 μ F, and a series equivalent resistance (R_{ser}) for C of approximately 800 m Ω .

As results, Figure [4.12](#page-63-0) shows the simulated inrush current of a single TAS over the rise time of the supply voltage. For instance, the inrush current of a single [TAS](#page-144-1) corresponds to 4.2 A, 3.7 A, 2.8 A, 1.5 A, and 230 mA when the power supply rise time is 1 µs, 10 µs, 50 µs, 100 µs, and 1 ms, respectively. By reducing the rise time of the supply voltage, the inrush current can be effectively mitigated. However, this also leads to a longer power-up time.

Limiting the rise time of the supply voltage proved effective in reducing the inrush current. During FEB power-up, the combined inrush current of all 32 [FEBs](#page-142-0) on one distribution board is still as high as 7.36 A for a rise time of 1 ms. Therefore, sequential power-up strategy is necessary to further reduce the inrush current.

Figure [4.13](#page-64-0) shows a sequential power-up simulation of four groups of [FEBs](#page-142-0) at 3 ms intervals. Each group of eight [FEBs](#page-142-0) is controlled by a load switch (TPS22918 from Texas Instruments) with a configured 1 ms rise time. The simulation results show that the inrush current can be further reduced from 7.36 A to 3.91 A by the group sequential power-up method. In addition, the power-up time is extended to around 10 ms.

Figure 4.11: Load equivalent circuit for a single FEB

Figure 4.12: Simulated inrush current of a single FEB over different rise time of the supply voltage. The simulation based on the load equivalent circuit which described in Figure [4.11](#page-62-0)

The adoption of rise time control of the supply voltage and sequential power-up methods in distribution boards provides a sensible approach to reducing inrush currents and facilitates coordinated and stable power distribution to [TASs](#page-144-1) and onboard amplifiers. In addition, by preventing excessive current spikes, it protects the [USCT](#page-144-0) III system from potential disturbances and ensures consistent performance and longevity of components.

4.3.2 Analog signal chain

The distribution board is also the key node in the analog signal chain, bridging the analog signal between the [DAQ](#page-142-1) system and the [TAS.](#page-144-1) Its primary functions include bridging, converting, distributing, and isolating signals to ensure efficient and reliable signal transfer between these two entities.

Figure [4.14](#page-65-0) illustrates one of the 96 receive signal chains responsible for transferring analog signals from the [TAS](#page-144-1) to the [DAQ](#page-142-1) system. It contains a differential amplifier and an isolation transformer. This arrangement facilitates the conversion of the single-ended signal from the [FEBs](#page-142-0) into a differential signal suitable

Figure 4.13: Simulation of sequential start-up of 32 [FEBs.](#page-142-0) 32 [FEBs](#page-142-0) are divided into 4 groups. Each group has eight [FEBs.](#page-142-0) A load switch model (TPS22918) from Texas Instruments is used to simulate the rise time (1 ms) of the power supply.

for the [DAQ](#page-142-1) system. At the same time, the isolation transformer serves the dual purpose of being both an impedance transformer and an isolator, ensuring signal integrity and preventing ground potential differences problems.

As illustrated in Figure [4.15,](#page-66-0) the amplifier circuit's analog frequency response depicts its performance over a spectrum of frequencies. Utilizing an AD4940 amplifier, the circuit components are chosen to balance both gain and bandwidth. The resistances, namely R_m , R_{FB} , R_G , and R_L , are 50 Ω , 2.2 k Ω , 1 k Ω , and 50 Ω , respectively.

A theoretical perspective offers insight into the amplification capability of the circuit. The gain, as determined by the circuit's resistor values, is given by the ratio R_{FB}/R_G , equating to 2.2. Considering the matching resistance of 50 Ω , the actual input signal will be attenuated by 50 % . Consequently, while the circuit's

Figure 4.14: Receive signal chain of the distribution board

design amplification stands at 1.1, simulations indicate a realized gain of 1.05. This figure represents approximately 95 % of the theoretical expectation.

A significant performance metric for amplifiers is their bandwidth. The simulation results shown in Figure [4.15](#page-66-0) indicate a -3 dB bandwidth of 170 MHz based on the small-signal model of the ADA4940. In practice, the output of the receive signal chain of the distribution board can be as high as $4 V_{pp}$. Therefore, it is necessary to consider the slew rate of the ADA4940 and the effect of the output voltage on the bandwidth. According to the ADA4940 data sheet, the slew rate is 90 V/μ s [\[69\]](#page-164-0). The bandwidth of the receiving system is estimated to be approximately 11 MHz for the worst case, i.e., 4 V_{pp} output signal.

As shown in Figure [4.16,](#page-67-0) the [USCT](#page-144-0) has a three-stage amplifier for the excitation signal chain.

The first stage is a differential to single-ended amplifier consisting of an inverting operational amplifier and a summing amplifier. Its principle is to use the inverter to convert the differential signal pair into two co-directional signals. Following this transformation, the summing amplifier steps in to add two co-directional signals as a single-ended output.

The second stage essentially consists of non-inverting amplifiers. The enable signal of the second stage has a 2-to-4 line decoder, which serves to divide the 32

Figure 4.15: Simulated frequency response of the receive signal chain on the distribution board

[TAS](#page-144-1) into four groups, ensuring that only one group of transducer array system, i.e. 8 [TAS,](#page-144-1) can be selected simultaneously. This mechanism not only ensures efficient channelization but also minimizes potential interference and cross-talk between different [TAS](#page-144-1) groups.

The third stage has the same non-inverting amplifiers as the second stage. With an array of 32 amplifiers integrated into this stage, each serves a dedicated coaxial cable. The amplification of the third stages is 2, in order to compensate the 50 % degradation of gain due to 50 Ω impedance matching.

In the simulation results presented in Figure [4.17,](#page-68-0) the performance of the stimulation signal chain is examined. Analyzing the first stage, the theoretical gain is determined by the ratio of R_{FB1}/R_{G1} . According to the provided parameters, both R_{FB1} and R_{G1} are equal to 1 kΩ. Thus, the theoretical gain for this initial

Figure 4.17: Simulated frequency response of the transmit signal chain on the distribution board

stage is unity. Factoring in the impedance matching, the resultant theoretical gain diminishes to 0.5.

The second and third stages employ identical non-inverting amplifier configurations. Given this setup, their combined design gain (after accounting for matching resistors) stands at 1. Due to the feedback configuration in these two stage, i.e. $R_{FB2}, C_{FB2}, R_{FB3}, C_{FB3}$, the stage two and three behave as low-pass filter. The -3 dB corner frequency of these stage is theoretically limited at 14.5 MHz. However, the simulation diverges slightly from this theoretical prediction, rendering a -3 dB corner frequency of 26 MHz. This discrepancy can be attributed to the input capacitance specific to the amplifier model employed in the simulation.

Consolidating the performance across the stages, the cumulative gain of the entire excitation signal chain manifests as -6 dB. Within the operative frequency range of the [USCT](#page-144-0) system, spanning from 0.5 MHz to 5 MHz, the gain exhibits commendable stability, with a flatness deviation of merely 0.4 dB. Furthermore, the total -3 dB bandwidth of stimulation signal chain is 22.9 MHz.

4.4 Smart transducer array systems

As illustrated in Figure [4.18,](#page-69-1) the third generation transducer array system [\(TAS](#page-144-1) III) follows a modular architecture consisting of three distinct functional components. The first component is the transducer array, which receives and transmits the ultrasound signals. It is directly connected to the analog front end using doublerow 1.27-mm pitch connectors, ensuring efficient and reliable signal transfer.

The analog front end serves as the interface between the transducer array and the subsequent stages of signal acquisition. This section of [TAS](#page-144-1) III is responsible for amplifying the received analog signals. The integration of [ASICs](#page-142-2) in the analog front end allows for a higher level of integration, leading to improved performance and expanded capabilities of the overall [USCT](#page-144-0) system.

In order to protect the electronics and maintain structural integrity, [TAS](#page-144-1) III is encased in a plastic enclosure that surrounds the electronic components. Additionally, a back cap is employed to provide additional shielding and facilitate

Figure 4.18: Exploded view of TAS III

easy serviceability. The [TAS](#page-144-1) III device is designed with a semi-open structure, where the transducer array end is waterproof to ensure resistance against environmental factors. Meanwhile, the back cap end can be conveniently removed when maintenance or repairs are required.

The increasing complexity and demands of the [USCT](#page-144-0) III device necessitated a departure from the conventional [TAS](#page-144-1) design relying on discrete components. The integration of [T/R](#page-144-2) switches and a higher number of transducers posed significant challenges that the generic discrete component-based [TAS](#page-144-1) design could no longer adequately address. Consequently, the introduction of [ASICs](#page-142-2) in [TAS](#page-144-1) III marked a significant advancement, enabling improved channel density, dynamic range, and the implementation of time-division multiplexing for the transducers in the analog front-end.

4.4.1 Front-end of TAS III

Figure [4.19](#page-71-0) shows the front-end [PCB](#page-143-2) of the [TAS](#page-144-1) III. The PCB has an area of 29 x 45 mm² . Utilizing the Chip on Board (COB) technology, [TAS](#page-144-1) III incorporates two transceiver [ASICs](#page-142-2) that are wedge bonded to the [PCB](#page-143-2) using aluminum wires.

To achieve communication, power management, and temperature monitoring within [TAS](#page-144-1) III, an ultra-low power [MCU](#page-143-1) from Texas Instruments has been employed. This [MCU](#page-143-1) serves as a central control unit, orchestrating the operation of the [ASICs,](#page-142-2) handling control data transmission, regulating power distribution, and monitoring the water temperature. Its ultra-low power consumption characteristics contribute to the overall energy efficiency of the [USCT](#page-144-0) system.

The transmission of both analog and digital data and power is facilitated through a 30-pin connector with a 0.5 mm pitch. This compact and high-density connector serves as the interface between [TAS](#page-144-1) III and the rest of the [USCT](#page-144-0) system, ensuring the transfer of signals and power between different components.

The simplified architecture of [TAS](#page-144-1) III, as shown in Figure [4.20,](#page-72-0) illustrates the signal flow and key components involved in efficient processing and reliable

Figure 4.19: FEB of TAS III

operation. The diagram distinguishes between the analog signal flow (indicated by red arrows) and the digital signal flow (represented by blue arrows).

The key components responsible for signal conditioning within the [TAS](#page-144-1) III are the [ASICs.](#page-142-2) These specialized integrated circuits handle various essential functions, including the control of the receive and transmit switches, amplification of received signals, and generation of high-voltage transmit excitation signals. By integrating these functions into the [ASICs,](#page-142-2) [TAS](#page-144-1) III achieves a high level of integration and signal acquisition capability, optimizing the performance of the transducer array.

In addition, the [MCU](#page-143-1) plays a crucial role in the overall functionality of [TAS](#page-144-1) III. For example, the temperature of the transducer array and the FEB can be recorded by the Delta-Sigma analog-to-digital (∆Σ-ADC) converter inside the [MCU.](#page-143-1) The [TAS](#page-144-1) III has a recording depth of one thousand points and can be operated while the USCT system is measuring. During the image reconstruction phase, the FEB provides temperature recordings that can be used to compensate for ultrasound velocities due to temperature changes.

The integration of the [ASICs](#page-142-2) and the [MCU](#page-143-1) enables efficient analog signal conditioning and comprehensive control of the ultrasound measurement process. This

Figure 4.20: Schematic diagram of the [TAS](#page-144-0) III front-end board

integrated approach ensures the reliability, accuracy, and stability of the [USCT](#page-144-1) III system, enhancing its overall performance.

4.4.2 Transceiver ASIC

The front-end [ASIC](#page-142-0) of the [TAS](#page-144-0) III has nine multiplexed receive/transmit channels utilising time-division techniques, as depicted in Figure [4.21](#page-73-0) [\[70\]](#page-164-0). Each channel consists of a transmit/receive switch and a high-voltage transmit amplifier. At the same time, the three receive channels share a three-stage receive amplifier through the multiplexer. The bias module in the [ASIC](#page-142-0) generates multiplexed voltages. These voltages are used to adjust the operating point of the amplifier. In addition, these voltages adjust the gain and bandwidth of the amplifier. The digital module can control amplifier channel selection, bias blocks, and feedback resistors and capacitors. The details are discussed in the following subsections.

Figure 4.21: [ASIC](#page-142-0) layout. [\[71,](#page-164-1) [70\]](#page-164-0)

Figure 4.22: Equivalent schematic of three-stage receiving amplifiers in ASIC

4.4.2.1 Analog part of the ASIC

Figure [4.22](#page-73-1) illustrates the equivalent schematic of the three-stage receive amplifier in the [ASIC.](#page-142-0) The design of the receive amplifier comprises three inverting amplifier stages, each tailored with distinct feedback configurations to enable adjustable receiver gain and bandwidth.

The initial phase of the [ASIC](#page-142-0) comprises a low-noise inverting amplifier. Its theoretical gain is determined by the ratio of the capacitance values C_{IN1}/C_{FB1} .

Figure 4.23: Simulated frequency response of the first stage amplifier in the [ASIC](#page-142-0) for different values of [GBW](#page-143-0)

The first stage is constructed as a fixed-gain (40 dB) system, with specific capacitance values of $C_{IN1} = 10$ pF and $C_{FB1} = 0.1$ pF [\[70\]](#page-164-0). Additionally, the bandwidth of this first stage amplifier is primarily restricted by the product of its gain and the [gain-bandwidth product \(GBW\)](#page-143-0) of the amplifier, expressed as: $GBW = Gain \times Bandwidth$.

Figure [4.23](#page-74-0) illustrates that with [GBW](#page-143-0) values at 100 MHz, 500 MHz, and 1 GHz, the corresponding -3 dB bandwidth of the first stage amplifier are 1 MHz, 5 MHz, and 10 MHz, respectively. In order to achieve the 5 MHz bandwidth required by the [USCT](#page-144-1) III system, the first stage amplifier needs a [GBW](#page-143-0) of at least 500 MHz at a gain of 40 dB.

The second stage is an amplifier with RC-CR shaper as shown in Figure [4.22.](#page-73-1) The gain of the amplifier can be expressed as:

$$
G = \frac{Vout2}{Vout1} = -\frac{R_{FB2} \cdot X_{CFB2}}{(R_{FB2} + X_{CFB2})(R_{IN2} + X_{CIN2})}
$$
(4.1)

To calculate the Laplace transfer function of the second stage, we need to replace the variables X_{CIN2} and X_{CFB2} with their corresponding expressions in terms of the complex frequency variable s. In the Laplace domain, $j\omega$ is represented as s.

Here,
$$
X_{CIN2} = \frac{1}{j\omega C_{IN2}} = \frac{1}{sC_{IN2}}
$$
, $X_{CFB2} = \frac{1}{j\omega C_{FB2}} = \frac{1}{sC_{FB2}}$

Substituting X_{CIN2} and X_{CFB2} :

$$
G(\omega) = -\frac{R_{FB2} \cdot \frac{1}{j\omega C_{FB2}}}{(R_{FB2} + \frac{1}{j\omega C_{FB2}})(R_{IN2} + \frac{1}{j\omega C_{IN2}})}
$$
(4.2)

$$
\mathcal{L}{G}(s) = -\frac{s \frac{R_{FB2}}{C_{FB2}}}{(sR_{FB2} + \frac{1}{C_{FB2}})(sR_{IN2} + \frac{1}{C_{IN2}})}
$$
(4.3)

From the transfer function, the second stage amplifier has one zero and two poles. 1. Zero: The zero is the s value for which the numerator is zero. That is, $s = 0$. 2. Poles: The poles are the s values for which the denominator is zero. i.e. $s = -\frac{1}{R_{FB2}C_{FB2}}$ and $s = -\frac{1}{R_{IN2}C_{IN2}}$

The frequency response of the second stage amplifier can be estimated by analysing its zero and poles. As shown in Figure [4.24,](#page-76-0) the zero at the origin indicates the starting point at 0 Hz on the Bode magnitude plot, leading to an initial increase in magnitude of 20 dB/decade. The introduction of two poles results in a magnitude decrease of 20 dB/decade. Since the second stage amplifier has a magnitude greater than 1, the product of R_{FB2} and C_{FB2} is greater than the product of C_{IN2} and R_{IN2} . So the first pole has a corner frequency at $\frac{1}{2\pi R_{FB2}C_{FB2}}$ Hz and the second pole has a corner frequency at $\frac{1}{2\pi R_{IN2}C_{IN2}}$ Hz. Its bandwidth is determined by two poles.

Figure 4.24: Bode magnitude plot of the second stage amplifier

The second stage amplifier is designed as a band-pass amplifier, with the low cut-off frequency determined by the values of R_{FB2} and C_{FB2} . In the current [ASIC](#page-142-0) implementation, R_{FB2} can be configured as 32 kΩ, 64 kΩ, 160 kΩ, and 192 kΩ, while C_{FB2} remains unchanged at 2 pF. Therefore, depending on the

Figure 4.25: Bode diagram for different values of R_{FB2}

Figure 4.26: Bode diagram for different values of R_{IN2}

specific setting of R_{FB2} , the low-cutoff frequencies of the [ASIC](#page-142-0) are 2.48 MHz, 1.24 MHz, 497 kHz, and 414 kHz, respectively (see Figure [4.25\)](#page-76-1).

The high cut-off frequency of the second stage amplifier relies on the values of R_{IN2} and C_{IN2} . C_{IN2} is adjustable within the range of 2 pF to 32 pF in 2 pF increments. Moreover, C_{IN2} significantly impacts the system's gain, represented as C_{IN2} divided by C_{FB2} , and varies approximately from 1 to 16. To achieve a high gain configuration while ensuring the second stage's bandwidth, R_{IN2} should be set to 1 Ω when C_{IN2} is greater than or equal to 20 pF, resulting in a high cut-off frequency beyond 5 MHz.

Conversely, in situations where the high gain is not required, setting R_{IN2} to 1.6 kΩ would be appropriate. By adjusting the values of C_{IN2} and R_{IN2} , the [ASIC](#page-142-0) can effectively regulate the gain and bandwidth of the second stage amplifier, allowing for fine-tuning and optimization of its performance based on specific operational requirements.

The third stage amplifier is similar in construction to the second stage amplifier. At present, the amplifier is not in use due to stability problems. Instead, an external amplifier with a gain of 6 is used.

The [ASIC](#page-142-0) has nine independent transmit channels. The transmit amplifier consists of two main parts. The first part is a transconductance amplifier that converts the input voltage signal to differential current. The second part is the Class AB amplifier. Its purpose is to transmit the output current generated by the Class AB amplifier through a high-voltage CMOS power stage converter. The advantage of this design of transmitter amplifier is the separation of the high-voltage domain from the low voltage domain.

4.4.2.2 Digital interface of [ASIC](#page-142-0)

As shown in Figure [4.27,](#page-79-0) the front-end [ASIC](#page-142-0) integrated into [TAS](#page-144-0) III incorporates a [serial peripheral interface \(SPI\)](#page-144-2) to streamline the configuration process of its internal parameters, such as bias voltage, channel selection, feedback resistors, and capacitors. Notably, the [SPI](#page-144-2) architecture enables direct access to channel selection via dedicated [SPI](#page-144-2) registers. In addition, a dual-clocked serial bus is cascaded across the [SPI](#page-144-2) bus for control over bias voltage and feedback parameters.

The [ASIC](#page-142-0) implementation of the [SPI](#page-144-2) has four data lines, i.e., clock, chip select, MOSI (Master Output Slave Input), and MISO (Master Input Slave Output). The [SPI](#page-144-2) interface requires four bytes to implement the writing of the channel information to the registers (see Figure [4.28\)](#page-80-0). Five bytes are required for reading (see Figure [4.29\)](#page-80-1).

The first byte serves multiple purposes within the [SPI](#page-144-2) communication. It combines the address of the register, burst mode, and read/write control flag. The register address specifies the destination register in the [ASIC](#page-142-0) where the subsequent data will be written or read. The Burst mode, if applicable, indicates that multiple

registers will be accessed in sequence. Lastly, the read control flag distinguishes between data being written to the [ASIC](#page-142-0) (0) or data being read from it (1).

Data consists of two bytes. When writing parameters to the [ASIC,](#page-142-0) the data bytes are the second and third bytes of the data frame. When reading parameters from the [ASIC,](#page-142-0) the data bytes are the third and fourth bytes of the data frame.

The dummy byte curries no information, but it will provide additional clock cycles for the [ASIC'](#page-142-0)s SPI communication. When writing, at least one additional dummy byte is needed to ensure that the data is written to the [ASIC.](#page-142-0) For reads, the [ASIC](#page-142-0) needs four dummy bytes to generate enough clock cycles to read the data.

When the [SPI](#page-144-2) clock is 1 MHz, the [ASIC](#page-142-0) needs 32 clock cycles to write a register and 40 clock cycles to read it. When configuring the [ASIC'](#page-142-0)s nine channels, a total of three registers need to be configured, so the ASIC requires 93.75 µs to configure all [ASIC](#page-142-0) channels and 120 µs to read at a clock frequency of 1 MHz.

Integrating a cascade architecture for the dual clock shift register interface has several advantages. One of the main advantages is the simplification of the electrical connection between the [MCU](#page-143-1) and the [ASIC.](#page-142-0) In addition, the dual clock shift register architecture simplifies the design of the digital part of the [ASIC.](#page-142-0) Dual-clock shift registers reduce the area footprint and thus have the potential to reduce manufacturing costs.

Figure 4.27: Simplified diagram of [ASIC](#page-142-0) digital interface

Figure 4.28: Write data from MCU to [ASIC](#page-142-0)

Figure 4.29: Read data from [ASIC](#page-142-0) to MCU

The timing diagram for the dual-clock shift register is shown in Figure [4.30.](#page-81-0) The interface consists of Clock 1, Clock 2, data line, reset, and the load signal. Clock 1 and Clock 2 are a pair of clock signals with a phase difference of 180 degrees. The data signal needs to be established on the rising edge of Clock 1 and to be maintained until the falling edge of Clock 2. Once all the data is shifted into the [ASIC,](#page-142-0) the load signal is used to transfer the data from the shift register to the [ASIC.](#page-142-0)

However, the trade-offs associated with dual-clock shift registers must be considered. The cascaded structure, while easier to implement, imposes a limitation on the speed of the dual-clocked serial bus. In the current [ASIC,](#page-142-0) writing one bit data to a dual-clocked shift register requires sending five [SPI](#page-144-2) data frames, or 160 bits of data, at a transfer rate of 1/160. This means that with a 1 MHz [SPI](#page-144-2) clock, it takes 17.92 ms to configure a 112 bits long bias register and 16.36 ms to configure a 96 bits feedback register. This means that it will take at least 8 min to configure the feedback register as well as the bias register during the measurement. Therefore, the configuration of these two registers needs to be done before the measurement.

Figure 4.30: Timing diagram of dual-clock shift register

4.5 Cables

Mixed signals including digital, analog and power are carried between the distribution board and the [TASs](#page-144-0) via a cable assembly. This cable assembly consists of 30 coaxial cables. The cable assembly is terminated with DF-80 connectors and is enclosed in a protective metal shield. The parameters of the cable assembly are outlined in the table [4.2.](#page-82-0) As the diameter of the cable is less than mm, it is also called a "micro-coaxial cable".

Coaxial cables are designed to shield analog signals from external interference. The three-layer construction of the cable (centre conductor, insulator and outer conductor), allows a constant characteristic impedance to be maintained. In the [USCT](#page-144-1) III system, the coaxial cables with a characteristic impedance of 50 Ω are used alongside wire drivers at the [TASs](#page-144-0) and distribution boards to minimise signal reflections.

Considering these parameters and the cable length of 0.8 meter in the [USCT](#page-144-1) III, the parasitic capacitance per cable is 90 pF, with a signal delay of about 3.84 ns. In addition, the serial resistance was measured to be 4 Ω . The signal attenuation of the cable is around $0.4 \, \text{dB}$.

Figure 4.31: Cable connection between TAS and distribution board. (star topology)

When the coaxial cable is used as a power line, it can be equivalently represented by a 4 Ω series resistance. The capacitance of the coaxial cable (90 pF) is about five orders of magnitude smaller than the decoupling capacitance (a few tens of µF) with the [FEB,](#page-142-1) so that the capacitance of the coaxial cable can be ignored, when the coaxial cable is considered as power line.

The [FEB](#page-142-1) is primarily powered by a 5 V power supply and is designed for a maximum current of 100 mA. Due to the 4 Ω series resistance of the coaxial

Figure 4.32: Simulation of star topology with coaxial cables under CAN bus. The simulation is based on Figure [4.31](#page-82-1) and $R_M = 0 \Omega$. The colors represent the positive (CAN-High in blue) and negative (CAN-Low in orange) signals of the differential signal pair.

cables, the input voltage on the FEB side drops to 4.6 V in the worst case. The minimum operational voltage of the FEB is approximately 3.6 V. Therefore, when powered through a coaxial cable, the FEB still maintains a voltage margin of 1 V.

Furthermore, the coaxial cable in the [USCT](#page-144-1) III system is responsible for carrying digital signals. Figure [4.31](#page-82-1) shows the connection between the [TAS](#page-144-0) and the distribution board in the [USCT](#page-144-1) III device. Because the total length of the stub cables is substantially larger than the backbone's length, the topology between [TAS](#page-144-0) and the distribution board can be considered as a star topology. Consequently, a simulation becomes necessary to determine the compatibility and efficacy of the star topology arrangement with the coaxial cable.

Figure [4.32](#page-83-0) presents the simulation results for the star topology under CAN bus. The top section of the figure illustrates signals from the distribution board transceiver, while the bottom section displays signals from the [TAS](#page-144-0) transceiver. The dominant bits have a 10 ns rising and following edges and a length of 1 us. In the first 10 µs of the simulation, the distribution board (top) sends two dominant

bits to the TAS (bottom). In the second 10 µs, the TAS (bottom) sends back two dominant bits, which are received by the distribution board (top). In both cases, the received signals oscillate.

The results in Figure [4.32](#page-83-0) indicate that the micro-coaxial cable does not effectively transmit the signals when a star topology is employed. This inefficiency is attributed to a substantial impedance difference between the transceivers and the cable, resulting in significant signal reflection and oscillation.

In a star topology, the bus does not have a farthest end or the nearest end, which makes it impractical to match each transceiver to a cable directly. Consequently, the [USCT](#page-144-1) system incorporates resistors (R_M) in series between the transmission line and the transceiver. These resistors attenuate the reflections caused by the impedance mismatch. Figure [4.33](#page-84-0) illustrates the transceiver signals from the distribution board and the TAS after the introduction of 10 to 25 Ω attenuating resistors.

The simulation results demonstrate a significant reduction in the system's reflection and oscillation with the attenuating resistors. When the distribution board

Figure 4.33: Simulation of star topology with different values of attenuating resistors (R_M) .

Figure 4.34: The [DAQ](#page-142-2) subsystem consists of an [RTM,](#page-143-2) an [AMC,](#page-142-3) and a [FMC.](#page-142-4)

is transmitting, and the TAS is receiving, resistors in the range of 10 to 25 Ω effectively mitigate the signal reflection. In addition, higher resistance values tend to flatten the rising and falling edges of the signal. When the TAS is transmitting, the distribution board still observes a relatively large signal overshoot at 10 Ω . However, this overshoot dissipates as the resistance is increased to 15 Ω .

In conclusion, incorporating a resistor of 15 to 20 Ω in series with the bus appears to be an effective solution for addressing the signal reflections and oscillations encountered when micro-coaxial cables are used in star topology.

4.6 Data acquisition system

The USCT system uses a flexible [DAQ](#page-142-2) system to digitise signals from multiple [TASs.](#page-144-0) As shown in Figure [4.34,](#page-85-0) the [DAQ](#page-142-2) subsystem consists of an [Rear Transition](#page-143-2) [Module \(RTM\),](#page-143-2) an [Advanced Mezzanine Card \(AMC\),](#page-142-3) and a [\(FPGA Mezzanine](#page-142-4) [Card \(FMC\).](#page-142-4) Each [DAQ](#page-142-2) subsystem can digitise 32 analog signals.

Each [RTM](#page-143-2) includes 32 channels of analog signal processing, consisting of analog [Anti-Aliasing Filters s \(AAFs\)](#page-142-5) and [Variable Gain Amplifiers \(VGAs\).](#page-144-3) This unit is equipped with four octal 12-bit 40 Msps [ADCs](#page-142-6) (AD967) for the acquisition of 32 analog signals. After the acquisition, these signals are serialized and transferred to the [AMC.](#page-142-3)

Additionally, the [RTM](#page-143-2) is designed with four eight-channel [DACs](#page-142-7) that provide gain adjustment capabilities for the [VGA.](#page-144-3) The [VGAs](#page-144-3) (AD8338) themselves offer a broad bandwidth of 18 MHz and a substantial gain adjustment range of 80 dB.

The [FMC](#page-142-4) has a 12-bit [DAC](#page-142-7) as well as a digital bus communication interface. The [DAC](#page-142-7) is controlled by the [AMC](#page-142-3) for analog excitation signal production. In addition, a transceiver on the [FMC](#page-142-4) board enables the conversion of digital bus signals. Thus, the [AMC](#page-142-3) can control the distribution board and the TAS via the digital bus interface of the [FMC.](#page-142-4)

The principal task of the [AMC](#page-142-3) board is to establish connections with the [RTM](#page-143-2) and [FMC](#page-142-4) boards. The [AMC](#page-142-3) collates the serialized signals from the [RTM](#page-143-2) and stores the refined signal in the DDR3 memory following processing via the digital processing module. The [AMC](#page-142-3) also manages the [FMC](#page-142-4) sub-board, transmitting pre-programmed excitation signals to the [FMC](#page-142-4) and commanding it to output these signals through the [DAC.](#page-142-7) Additionally, a control bus linked to the [FMC](#page-142-4) board facilitates communication with all the switchboards as well as the FEB.

Data is stored in the [AMC](#page-142-3) board's memory during measurement. Once the measurement is finished, the [AMC](#page-142-3) can transfer the stored data either via the [Peripheral Component Interconnect Express \(PCIe\)](#page-143-3) bus or the [Small Form-factor](#page-143-4) [Pluggable Transceiver \(SFP\)](#page-143-4) interface. In the context of the USCT III, there are 12 boards in total, collectively providing 384 independent differential analog channels. Out of these 12, one serves as the system master, while the memory of the remaining 11 systems is transferred to the master board via [PCIe](#page-143-3) and subsequently uploaded to the server via Ethernet.

4.7 Firmware

The USCT III system has over 100 [MCUs.](#page-143-1) They are located in the [TAS](#page-144-0) and distribution boards. Firmware is as important to the overall stability of the system as the hardware. In addition, the differences in hardware devices often require the development of several different firmware. Therefore, the USCT III system

requires a reasonable structural layout of the firmware, which is conducive to modularity, scalability, and ease of maintenance.

Figure [4.35](#page-87-0) illustrates the structure of the firmware, which can be categorized into four layers. The first layer is the hardware abstraction layer (HAL), which serves as the bridge between the hardware and the higher-level software components. It abstracts the specifics of the hardware, and provides functions for accessing device peripherals, interfaces like SPI, UART, GPIO, and other device-specific functionalities.

The second layer is the functional module layer (FML). Here, the firmware targets specific functions such as communication, control of the [ASIC,](#page-142-0) and temperature measurement. This layer is responsible for implementing the necessary algorithms and protocols to enable these functionalities effectively.

The third layer is the bootloader layer (BL). Its primary purpose is to provide firmware upgrade capabilities. The BL enables the MCU to receive and install updated versions of the firmware, ensuring the system remains up-to-date and adaptable to evolving requirements.

The fourth layer is the application layer (AL). This layer primarily implements a command-based finite state machine (FSM). It encompasses the main application

Figure 4.35: Structure of the firmware

logic, handling commands and managing the system's behavior based on its current state.

Overall, these four layers in the firmware structure of the USCT system work together to ensure proper control, communication, and functionality of the TAS and distribution boards.

The firmware architecture in the USCT system can be shared between different devices such as [TAS](#page-144-0) and the distribution boards. Because the [TAS](#page-144-0) and the distribution board use the same [MCU,](#page-143-1) they can utilize the first three layers (i.e. HAL, FML and BL) of the firmware architecture in a shared manner. They only need to implement different AL to accommodate their specific functionalities.

Moreover, the firmware architecture also considers future hardware upgrades. The HAL can be configured to support portability, allowing the existing firmware to be easily transferred and adapted to a new embedded platform. This flexibility enables seamless migration to new hardware while minimizing the need for extensive code modifications.

4.7.1 Bootloader

The bootloader plays a critical role in enabling online upgrades of the distribution board and the [TAS,](#page-144-0) significantly reducing the time required for upgrades from days to less than 30 minutes.

Figure [4.36](#page-89-0) illustrates the flowchart of the bootloader, which is developed for [TAS](#page-144-0) and distribution board. After the [MCU](#page-143-1) completes its communication initialization, the firmware first enters the bootloader and checks if the 128-byte upgrade key matches. If the upgrade key matches, the bootloader is executed. Otherwise, the MCU bypasses the bootloader and proceeds directly to the application program.

During the bootloader process, the new firmware can be written to the flash memory using the communication protocol at the function module level. However,

Figure 4.36: Flowchart of the bootloader

unlike the application mode, the bootloader does not provide a readback function. This ensures the security of the application code, preventing unauthorized access or retrieval.

Once the new firmware is successfully loaded, the bootloader offers two modes: debug and release. In debug mode, the MCU immediately jumps to the application mode. Subsequent boots will still occur from the bootloader mode, which is useful for debugging firmware and troubleshooting potential issues. Debug mode can be reverted back to bootloader mode by re-powering the firmware in case of problems. On the other hand, in release mode, the bootloader clears the upgrade key. The next power-up of the system will bypass the bootloader and directly boot into the application mode, which is the normal operating mode.

By incorporating the bootloader functionality, the USCT system facilitates efficient and secure online upgrades of the distribution board and the TAS. This significant reduction in upgrade time enhances the system's flexibility and adaptability to future improvements and advancements.

(a) Interrupt process (b) Compare interrupt (top) and DMA (bottom) methods during communication

Figure 4.37: (a). The process of a single interrupt response. (b). Compare interrupt and [DMA](#page-142-8) methods during communication. DMA reduces the number of interrupts and the load on the MCU when passing large amounts of data.

4.7.2 Multi-task scheduling

Implementing fast-response multitask scheduling on a low-power, low-frequency [MCU](#page-143-1) renders traditional polling or interrupt methods insufficient. To overcome this limitation, we propose utilizing a [Direct Memory Access \(DMA\)](#page-142-8) controller to enhance the efficiency of system scheduling for multitasking.

Figure [4.37a](#page-90-0) illustrates the conventional interrupt process, consisting of three main steps. Firstly, the MCU jumps into the interrupt, requiring it to save the existing pointer and data to ensure the ability to resume execution of the original program once the interrupt concludes. Secondly, the interrupt program itself is executed. Finally, the interrupt return phase involves jumping out of the interrupt program and returning to the pre-interrupt position. All three processes necessitate coordination by the MCU, resulting in a high MCU load.

By introducing a [DMA](#page-142-8) controller, we can optimize the multitask scheduling process and reduce the time overhead associated with interrupts. The [DMA](#page-142-8) controller operates independently of the CPU and can efficiently transfer data between memory and peripheral devices without CPU intervention. This offloading of data transfer tasks from the CPU to the [DMA](#page-142-8) controller significantly reduces the time overhead for interrupt processing.

Figure [4.37](#page-90-0) compares interrupt mode to [DMA](#page-142-8) mode for receiving a 100-byte data frame, using the MSP430FG6626 [MCU](#page-143-1) from [TAS](#page-144-0) as an example. This [MCU](#page-143-1) is a 16-bit, single-cycle instruction device operating at a main frequency of 20 MHz.

In interrupt mode, the [MCU](#page-143-1) generates an interrupt for each byte received, requiring at least 100 cycles for each interrupt handler, including 11 cycles for handling the interrupt's initiation and completion. Consequently, the communication function consumes more than 50 % of the [MCU'](#page-143-1)s resources.

Conversely, in [DMA](#page-142-8) mode, the [DMA](#page-142-8) controller takes over data reception, bypassing the [MCU](#page-143-1) to store data directly into memory. The [MCU](#page-143-1) is only interrupted once the entire data frame is received, significantly reducing its workload. For a 100-byte data frame, the [MCU'](#page-143-1)s resource usage in [DMA](#page-142-8) mode drops to just 1 % compared to that in interrupt mode.

4.8 Control method

The measurement process of the [USCT](#page-144-1) III system needs a comprehensive traversal of all transducers to gather ultrasound data. This process is executed in a systematic manner, employing a step-wise approach wherein each step comprises two distinct phases. This two phase measurement process is shown in Figure [4.38.](#page-91-0)

Measurement Step

Figure 4.38: Two phase measurement step

During the initial phase, i.e. the transmit-receive processing, the [DAQ](#page-142-2) transmits the ultrasound signal through a designated transducer while the remaining transducers receive both the reflected and transmitted ultrasound signals. Throughout this phase, the TAS and the analog segment of the distribution board collaborate to amplify and relay the received signals.

The second phase, referred to as the configuration phase, involves the temporary suspension of the acquisition process by the [DAQ,](#page-142-2) which subsequently re-configures the analog section of the [FEB](#page-142-1) and the distribution board. This re-configuration prepares the system for the next measurement step. The initiation of reconfiguration can be triggered by the transmission of a STEP signal or through communication with the pertinent components.

To complete a full scan in the [USCT](#page-144-1) III system, a total of 13,824 steps are necessary. Each step consists of the transmit-receive and configuration phases.

USCT III has two control modes: single-step mode and automatic mode. In the single-step mode, each TAS receives configuration commands from the [DAQ](#page-142-2) through bus communication. For each step, the [TAS](#page-144-0) selects the transmit and receive channels. The gain of each [TAS](#page-144-0) can be adjusted if necessary. This mode offers high flexibility as any transducers can be assigned to transmit or receive ultrasound signals in each step. However, the single-step mode relies on sequential communication, which takes around an hour to complete a full measurement. This mode is unacceptable for clinical applications where time efficiency is critical.

To minimize system time overhead and expedite the measurement process, the [USCT](#page-144-1) III system also supports an automatic control mode based on a command table. In this mode, the channel selection for each [TAS](#page-144-0) and distribution board is pre-determined and uploaded prior to the measurement. During the measurement, the [TAS](#page-144-0) progressively selects the configured profiles based on trigger signals from the [DAQ.](#page-142-2) This approach significantly reduces the measurement time, allowing for the completion of the measurement in the shortest possible duration. Conversely, in the automatic control mode, the switching time of the [FEB'](#page-142-1)s channels may be shorter than the time it takes for the analog signal chain to set up. As a result, it

Figure 4.39: Receive priority switching mode

becomes necessary to investigate the optimal switching sequence in the automatic mode.

In the automatic control mode of the [USCT](#page-144-1) III system, there are two scanning approaches: the receive priority switching mode (illustrated in Figure [4.39\)](#page-93-0) and the transmit priority switching mode (shown in Figure [4.40\)](#page-94-0). Both methods initiate scanning from the first [TAS.](#page-144-0)

In the receive priority mode, the system prioritises cycling through receive channels, grouping every six channels as one receive cycle. After finishing with one cycle, it moves to the next transmit channel, cycling through all 2304 transducers.

Conversely, the transmit priority mode focuses on the transmit channels first, treating the 2304 transmit channels as a single transmit cycle. Upon completing the transmit cycle, it then shifts focus to the next receive channel, continuing this process until all receive channels have been covered. The measurement concludes once every receive channel has been traversed.

Both of these modes ensure the comprehensive traversal of all transducers during the measurement process, facilitating extensive data collection. The table below summarises the control modes of the USCT system as well as the scanning modes.

In the transmit priority mode, the system minimizes the number of receive toggles, resulting in a total number of steps for a complete scan equal to $(2304 - 1) \times$ $6TX + 5RX$. On the other hand, in the receive priority mode, the system

	TX1	TX ₂	TX3	\cdots	TX2304
RX_mux1					
RX mux2					
RX mux3					
RX mux4					
RX_mux5					
RX mux6					

Figure 4.40: Transmit priority switching mode

minimizes the number of transmit steps, leading to a total number of steps for a complete scan equal to $(6 \times 2304 - 1)$ RX + 2304 TX.

The receive priority mode entails 2304 more channel switching than the transmit priority mode, highlighting a significant difference in operational efficiency. Additionally, measurements in the chapter [5.1.6](#page-115-0) indicate that the transmit channel switching time is 100 times faster than that of the receive channel switching. Considering the total number of switching, along with the difference in switching speeds between transmit and receive channels, the transmit priority switching mode is chosen because it significantly reduces the overall measurement time, making it the more efficient option for rapid scanning.

5 Results

This chapter is dedicated to a comprehensive evaluation of the [USCT](#page-144-1) III system through a series of designed experiments, categorized into components tests and system integration tests.

The primary focus of component testing is on the analog signal paths, including the analog front-end of the distribution board and the transmit and receive signal chains. These tests are further subdivided into static characterization tests and dynamic characterization tests. Static characterization tests include attributes such as the power consumption of the analog front-end and the distribution board. Dynamic characterization is used to evaluate parameters such as channel switching speed and analog channel bandwidth.

For system integration tests, the various systems of [USCT](#page-144-1) III are interconnected using a bus system, with the primary objectives being: System communication: The initial phase of the integration test assesses the system's communication capabilities. Measurement time analysis: Here, a comparative study is conducted on the measurement durations of the system under different control strategies. 3D Reconstruction Performance: Through water bath steel ball experiments, the system's capability to perform accurate 3D reconstructions is evaluated.

In system integration testing, the components of the III system are interconnected via a bus system whose primary objective is that III is interconnected. Integration testing is used to test the overall performance of the system and consists of three main areas: the communication system, measurement time, and the ability to reconstruct in three dimensions.

The findings from these experiments will provide insights into the performance, strengths, and potential areas of improvement of the new [USCT](#page-144-1) III system.

5.1 Front-end characterisation

The [FEB](#page-142-1) stands as an important component in the [TAS.](#page-144-0) It encompasses interconnected subsystems, including a power filter module, a [MCU,](#page-143-1) and two [ASICs.](#page-142-0) In this subsection, the test equipment used to test the front-end board and the connection schematic are first described. The test results are presented in the subsequent sections.

5.1.1 FEB test platform

As outlined in Chapter 4, the [FEB](#page-142-1) employs a 1.27 mm pitch board-to-board connector on the transducers' interface side. Simultaneously, for interfacing with the distribution board, the [FEB](#page-142-1) uses board-to-micro coaxial cable connectors. These connectors on the one hand enable the connection of individual components in a limited space, but pose a challenge when integrating with conventional laboratory equipment.

To address the integration challenge, a set of special-designed interface boards was designed and fabricated. As depicted in Figure [5.1,](#page-98-0) these interface boards were designed to allow in deeper testing and validation. The inclusion of 4 mm high-voltage and low-voltage power connectors ensures a robust and reliable power connection to the board. The LEMO coaxial connectors seamlessly interface with laboratory instruments, such as oscilloscopes and signal generators. This ensures that the signals being generated or monitored with minimal interference or loss.

Furthermore, for debugging and firmware programming tasks, the board incorporates a [Joint Test Action Group \(JTAG\)](#page-143-5) debug interface. This is essential for in-depth analysis or troubleshooting that might be required during the testing phase. The RS485 communication interface allows the board to communicate

Figure 5.1: Mixed-signal interface board for testing the [FEB](#page-142-1)

with external devices or systems, ensuring that the [FEB](#page-142-1) can be configured or queried remotely. In addition, the board features test points for every voltage level. This feature ensures that there is no need for intrusive probes or connections that might otherwise interfere with the system's operation.

Considering the wear and tear associated with repeated connections, a thoughtful design feature has been the integration of replaceable DF80 connection daughter boards. Given that the DF80 connectors, when interfaced with the [FEB,](#page-142-1) have a limited plug life of 30 cycles, it was imperative to consider a cost-effective and sustainable solution. By making the DF80 adapter daughter board replaceable, we have ensured that, upon wear or damage, only this component needs replacement, rather than the entire (and presumably more expensive) interface board. This not only reduces maintenance costs but also ensures minimal downtime during testing and validation phases.

The [FEB'](#page-142-1)s transducer interface board, depicted in Figure [5.2,](#page-99-0) efficiently routes all 18 transducer channels and adapts them to LEMO connectors. This arrangement facilitates the straightforward connection of oscilloscopes and signal generators

Figure 5.2: Transducer interface board for the [FEB](#page-142-1) tests

to the [FEB.](#page-142-1) Furthermore, it is compatible with a channel selector, allowing for seamless automated testing.

In Figure [5.3,](#page-100-0) the comprehensive connection layout of the [FEB](#page-142-1) test platform is delineated. The platform, centrally managed by a computer, integrates with standard measurement devices such as oscilloscope, wave generator and laboratory power supply through the [Virtual instrument software architecture \(VISA\)](#page-144-4) protocol [\[72\]](#page-164-2). This facilitates automated tasks like waveform generation, current measurement, and waveform visualization and archiving.

The MCU's emulator and the USB to RS485 converter bridge with the PC via USB, enabling both [FEB](#page-142-1) communication and debugging capabilities. Acting as intermediaries between the [FEB](#page-142-1) and the measuring instruments are the mixedsignal interface board and the transducer interface board. In the diagram, two distinct signal paths observed during testing are demarcated by color coding:

The red signal path depicts a signal inputting from the [FEB'](#page-142-1)s transducer connector and then outputting from the [FEB.](#page-142-1) As the primary aim here is to assess the [FEB'](#page-142-1)s capability in receiving small signals from the transducer, this pathway is designated as the "receive signal chain."

Figure 5.3: [FEB](#page-142-1) test platform

Contrasting with the red signal path, the green signal path illustrates the signal from the mixed-signal interface board to the transducer connector. The primary assessment focus here is the [FEB'](#page-142-1)s signal-driving capability, hence the nomenclature "transmit signal chain."

The [FEB'](#page-142-1)s unit platform is provisioned in two distinct configurations to validate both the receive and transmit link performances. The receive link assessment involves utilizing an Arbitrary Waveform Generator (AWG) to produce a signal that emulates the sensor's operational conditions during reception. The primary objective here is to test the dynamic performance of the receive link. In this scenario, the AWG interfaces with the transducer, while the oscilloscope is coupled to the [FEB'](#page-142-1)s analog signal output interface. The transmit link assessment is configured antithetically. The AWG delivers the excitation signal to the [FEB,](#page-142-1) and the oscilloscope monitoring the [FEB'](#page-142-1)s capacity to amplify and transmit the signal.

A [graphical user interface \(GUI\)](#page-143-6) based on MATLAB is developed to configure the [TAS](#page-144-0) III front-end. As shown in Figure [5.4,](#page-101-0) the [GUI](#page-143-6) can set all the configuration

Functions	Descriptions		
Channel selection	Select the 18 transducers		
	for transmitter or receiver		
Front-end reference voltage	Generate four extenal reference		
	voltage for ASICs		
	Configure the amplification		
ASIC feedback configuration	of the input and output channels		
	(36 registers)		
ASIC bias voltage configuration	Configure the internal bias voltages		
	of ASIC (16 registers)		
Front-end power and output control	Control the power switch of the ASIC's		
	the analog output of the FEB		

Table 5.1: Function of [USCT](#page-144-1) [FEB](#page-142-1) III

registers of the [FEB.](#page-142-1) The GUI implements the functions, which are listed in table [5.1.](#page-102-0)

In summary, the [FEB](#page-142-1) test platform can evaluate the [FEB'](#page-142-1)s functionality either manually or semi-automatically. This encompasses assessing static attributes like operating voltage and current, alongside dynamic performances of the receive signal link and the analog signal link, which includes metrics like bandwidth and gain.

5.1.2 Power supply characteristics

To assess the power characteristics of the [FEB,](#page-142-1) the configuration delineated in Figure [5.3.](#page-100-0) The laboratory power supply provides the power and measures the current. The [FEB](#page-142-1) can be configured to operate in different states through a GUI and an RS485 communication interface.

The [FEB](#page-142-1) requires two pairs of bipolar power supplies for its functionality. These are denoted as $(V_{CC+}, V_{CC-}, HV_+, HV_-)$. Here, V_{CC+} primarily supplies the MCU, the ASIC's receiver amplifier, and the 6:3 multiplexer. In contrast, V_{CC-} caters to the external multiplexer. The high voltage amplifier of the ASIC derives its power from both HV_+ and HV_- . The precise operating voltages and associated currents are cataloged in Table [5.2.](#page-103-0)

Parameter	Test conditions	Specifications				
Name	Function	MIN	NOM	MAX	Unit	
HV_+	Positive power supply for ASIC	$\overline{}$	40	50		
HV_{-}	Negative power supply for ASIC	-50	-40	-5		
V_{CC+}	Positive power supply for FEB	3.6	5	5.5		
V_{CC}	Negative power supply for FEB	-5.5	-5	-3.6		
I_{HV_+}	Standby	0	0			
	RX/LV: 1ASIC+1CH enabled	0	Ω		mA	
	TX/HV: 1xASIC+1xCH enabled	0	3	5		
I_{HV}	Standby	0	0			
	RX/LV: 1ASIC+1CH enabled	0	Ω		mA	
	TX/HV: 1xASIC+1xCH enabled	0	3	5		
$I_{V_{CC+}}$	Standby	27	30	32		
	RX/LV: 1ASIC+1CH enabled	49	42	45	mA	
	TX/HV: 1ASIC+1CH enabled	34	38	41		
$1_{V_{CC-}}$	Standby	Ω		3		
	RX/LV: 1ASIC+1CH enabled	0	3	4	mA	
	TX/HV: 1ASIC+1CH enabled	Ω		4		

Table 5.2: Power supply characteristics of [FEB](#page-142-1)

The [FEB'](#page-142-1)s power consumption in standby mode, with the ASIC's transmit and receive functions disabled, is around 0.16 W. When the system is in transmit mode, it consumes about 0.44 W, and in receive mode, it requires approximately 0.23 W. The maximum power draw is 0.67 W, which occurs when both the transmit and receive amplifiers are operational simultaneously.

When [FEB](#page-142-1) is powered up, an inrush current is generated due to the decoupling capacitors, as shown in Figure [5.5.](#page-104-0) It is important to note that this observation excludes the effects of the high-voltage power supply since it remains deactivated by default during system startup.

During the startup of V_{CC+} at t = 0 s, the [FEB](#page-142-1) has an inrush current of approximately 260 mA. After 500 ms, the [FEB'](#page-142-1)s power management enables the rest of the circuits, which further induces a second inrush current. This second peak is attributed to the delayed activation of the MCU's ASIC power supply. Employing this staggered startup approach, the [FEB'](#page-142-1)s power management effectively prevents both surges from coinciding, thereby mitigating the maximum inrush current experienced.

Figure 5.5: [FEB](#page-142-1) current of V_{CC+} . The X-axis represents time, and the Y-axis shows current.

5.1.3 Thermal characteristics

The USCT ASIC, as an amplifier, generates heat when the FEB is in operation. Measuring the thermal characteristics of the FEB ensures that the USCT ASIC is operating in the proper temperature range. In addition, this section uses an approximation to determine the junction to ambient temperature resistance (θ_{JA}) of the ASIC.

 θ_{JA} is defined as the ratio of power to junction temperature and ambient temperature difference.

$$
\theta_{JA} = \frac{T_J - T_A}{P_D} \tag{5.1}
$$

Here, T_J is the junction temperature of the [ASIC,](#page-142-0) P_D is the power dissipation of the ASIC, and T_A is the ambient temperature. It is also related to factors such as the package and PCB layout of the ASIC [\[73\]](#page-164-3).

 T_I can be measured by the thermal camera when the case of the ASIC is open [\[74,](#page-164-4) [73\]](#page-164-3). However, the ASIC on the FEB is applied thin transparent silicone (Sylgard 184) as glob top (see Figure [4.19\)](#page-71-0) with less than 1 mm thickness. The thermal conductivity of silicone (Sylgard 184) is 0.27 W/($\rm{m K}$) [\[75\]](#page-164-5). Assuming that the glop top is uniformly distributed on the surface of the ASIC, the difference between the temperature at the die surface of the chip and the temperature at the surface of the glop top can be calculated by Fourier's law of thermal conduction [\[76,](#page-164-6) [77\]](#page-164-7):

$$
Q = \frac{k \cdot A \cdot \Delta T}{L} \tag{5.2}
$$

Here, O is the heat transfer rate in W, k is the thermal conductivity of the glob top $(0.27 \text{ W}/(\text{m K}))$. A is the cross-sectional area (ASIC area) to the heat path. ASIC area is 13.53 mm². ΔT is the temperature difference across the glob top in °C, and L is the thickness of the glob top.

Figure 5.6: Thermogram of FEB in USCT III. Five transmit channels in one ASIC were enabled, and the ASIC worked at 1152 mW. The maximal junction temperature is 96.3 $^{\circ}$ C

Assume that 1 W heat is transferred from the ASIC surface to the glob top surface, the temperature difference ΔT between the glob top surface to the die surface is around $0.27 \degree C$. The actual temperature difference might be smaller than the estimated difference (0.27 $^{\circ}$ C). The reason is that most of the heat generated by the ASIC is transferred via the copper pads on the PCB at the bottom. Since the thermal conductivity of the copper (398 $W/(m K)$) [\[78\]](#page-164-8) is much higher than that of the glob top. Due to the small temperature difference ΔT , the temperature of the glob top will be considered as T_I .

The lab power supply can determine the power dissipation P_D of the [ASIC.](#page-142-0) T_J can be measured by the thermal camera. For example, Figure [5.6](#page-105-0) shows that the junction temperature of the ASIC is 96.3 °C. However, determining T_A is challenging. The conventional method is to achieve a specific ambient temperature by a forced water cooling heat exchanger [\[74\]](#page-164-4).

In the approximate calculation, T_A is assumed to be constant. Thus, the θ_{JA} can be calculated as:

$$
\theta_{JA} = \frac{T_{J1} - T_{J2}}{P_{J1} - P_{J2}}\tag{5.3}
$$

Here, T_{J1} and T_{J2} are two junction temperatures of [ASIC](#page-142-0) with corresponding input power P_{11} and P_{12} .

During the measurement, the FEB operates in transmit mode, and by controlling the transmit voltage and enabling different numbers of transmit channels, the ASIC can operate at different power levels. At the same time, the FEB board is observed using a thermal camera. When the temperature of the FEB is stable, the thermal camera records the junction temperature of the [ASIC.](#page-142-0)

Figure [5.7](#page-107-0) shows the measurement results. The junction temperature of [ASIC](#page-142-0) was measured at four different power dissipation. After linear regression, it can be concluded that θ_{JA} equals 58.4 °C/W with a standard deviation of 2.6 and the ambient temperature is 29.8 \degree C with a standard deviation of 1.9. As can be seen in the previous section, the maximum power consumption scenario for the ASIC in the USCT III is approximately 0.5 W. This means that the junction temperature of the USCT ASIC exceeds a maximum of 29.2 °C above the ambient

Figure 5.7: Junction temperature of [ASIC](#page-142-0) over input power

temperature. Based on the maximum workable junction temperature of the current experiments, the maximum ambient temperature at which the USCT ASIC can operate is approximately 67 °C.

5.1.4 Transmit characterisation

The [FEB](#page-142-1) III was characterized with respect to gain and bandwidth. For transmit characterization, an up-chirp signal with a peak-to-peak voltage of 0.7 V_{pp} was applied to the high-voltage amplifier of the front-end. The length of the excitation signal was 10 ms and the frequency range was between 0.5 MHz and 9.5 MHz.

As shown in [5.8,](#page-108-0) the excitation signal is amplified by the FEB to reach a maximum voltage of 50 V_{nn} . The total gain of the [FEB](#page-142-1) III is about 37 dB. notably, the amplified signal is not completely symmetrical when the frequency of the signal

Figure 5.8: Figure top-left shows the up-chirp signal as an excitation signal. The frequency of this up-chirp signal over time is shown in the bottom-left figure. Figure top-right shows the amplified signal via the ASIC. The frequency of the amplified signal over time is shown in the bottom-right figure.

is greater than 4.5 MHz. It is speculated that the bias voltage of the transistor of the ASIC's Class AB amplifier changes when amplifying the signal.

In addition, it can be seen from the power spectrum that the power of the excitation signal hardly attenuates within the set frequency range. However, for amplified signals, the power starts to decay from about 5 MHz due to the effect of bandwidth.

However, the asymmetry of the output signal and the attenuation of the power have almost no impact on USCT III. The reason is that the USCT transducers operate between 0.5 MHz and 4.5 MHz. In this frequency interval, the high-voltage amplifier has almost no asymmetry and no attenuation of the power.

Next, the ASIC parameter (HVNAMP) was experimentally investigated to understand its effect on the bandwidth. HVNAMP controls the slew rate of the transmit amplifier. Increasing the HVNAMP improves the bandwidth and accordingly increases the power consumption of the transmit amplifier.

The results of the tests are shown in Figure [5.9.](#page-109-0) The tests were performed using chirp signals from 0.5 MHz to 9.5 MHz as input. The FEB test platform recorded the input and output signal of the transmit amplifier. In the measurement, HVNAMP is set from 1 to 22 in steps of 5.

Figure 5.9: The gain of the transmit amplifier over frequency for different HVNAMP settings. The red dash line indicates the -3 dB attenuation.

Overall, the -3 dB cut-off frequency of the transmit amplifier of [ASIC](#page-142-0) becomes larger as the HVNAMP increases. The -3 dB cut-off frequency of the transmit amplifier reaches 2 MHz at a value of HVNAMP of 6. The cut-off frequency significantly increases when HVNAMP is in the range of 1 to 6. At HVNAMP values between 11 and 22, the transmit amplifier reaches a corresponding cut-off frequency in the range of 4 to 5 MHz. However, the effect of HVNAMP on bandwidth is less pronounced in this interval. Typically, HVNAMP is configured to 15 as a standard parameter due to the trade-off between power consumption and bandwidth.

In order to quantitatively evaluate the gain and bandwidth of the [FEB'](#page-142-1)s transmit signal chain, data was collected from 100 transmit channels. In these experiments, the standard HVNAMP value, i.e.15, was used. Based on these data, the spectral representation of the transmit amplifier, shown in [5.10,](#page-110-0) indicates that the maximum gain of the transmit amplifier is 36.9 dB, which incorporates the gain

Figure 5.10: Spectrum diagram of 100 TX amplifiers of [ASIC.](#page-142-0) The black line represents the average characterization of the gain over frequency. The TX amplifiers have a -3 dB bandwidth in the range of 73.4 kHz to 4.9 MHz.

of 30.9 dB provided by the [ASIC](#page-142-0) and 6 dB of gain provided by the analog circuits of the FEB. The total -3 dB bandwidth of the front-end board is 4.8 MHz. In addition, the amplifier has a -6 dB bandwidth of 6.5 MHz with a deviation of 0.65 MHz.

5.1.5 Receive characterisation

According to Chapter [5.1.5,](#page-110-1) the receive signal chain of [FEB](#page-142-1) is used to amplify tiny ultrasound signals and adjust the gain and bandwidth of the receive amplifier. This section verifies the influence of these parameters on the signal through the control variable method.

Figure 5.11: Normalized gain vs C_{IN2}

The second amplifier stage of the [FEB](#page-142-1) is a variable gain amplifier. The relationship between $Gain$ and C_{IN2} can be written as:

$$
Gain \approx \frac{C_{IN2}}{C_{FB2}} \tag{5.4}
$$

 C_{FB2} is a capacitor with a constant value of 2 pF. Therefore, the gain of this stage is proportional to C_{IN2} .

In the characterisation test, C_{IN2} was changed incrementally from 1 to 15, while other parameters remained constant. To figure out the influence of C_{IN2} and isolate its influence from other factors, the gain in Figure [5.11](#page-111-0) was normalized. This normalization cancels out the contributions of the other two amplifier stages, ensuring that the observed changes are due to changes in C_{IN2} .

The experimental results are shown in Figure [5.11.](#page-111-0) Black circles represent the measurement data. The red line represents the theoretical reference. The blue line represents the linear fit to empirical measurements. The black dashed line depicts the 95 % confidence interval, highlighting the region where most empirical measurements correlate with a linear fit. The high linear variable gain amplifier can be used to adjust the dynamic range of the USCT receive chain. In addition, it can also be used to calibrate individual gain differences between different ASICs.

The capacitors C_{FB2} and R_{FB2} together form a high-pass filter in the receive amplifier. While C_{FB2} remains constant, the cut-off frequency of the high-pass filter can be varied by altering R_{FB2} .

Comparing the measured results with the simulated results in [5.12](#page-112-0) shows that they are similar at frequencies below 2.5 MHz. Above 2.5 MHz, the actual measurement results of the ASIC are also affected by the characteristics of the amplifier itself. However, for this high-pass amplifier, the maximum cut-off frequency is only 2.48 MHz, so the characteristics of the high-pass amplifier here are mainly in the range of 0.5 MHz to 2.5 MHz.

Due to the difference in gain between the simulated and measured results, the characteristics of the high-pass filter are compared here by the slope (gain over frequency). For example, with R_{FB2} is equal to 32 kΩ, the gain increases by

(a) Simulated gain over frequency for different R_{FB2} (b) Measured gain over frequency for different R_{FB2}

Figure 5.12: Gain over frequency for different R_{FB2} . Comparison between simulation and measurement results.

approximately 5.5 dB from 0.5 MHz to 1 MHz. This growth rate is the same as the simulation results. For 64 kΩ, 160 kΩ and 192 kΩ, the gains in the measurement increase by 4 dB, 2 dB and 1 dB respectively, which is also consistent with the simulation results.

The measurement results can prove that R_{FB2} is related to the high-pass characteristics of the amplifier. However, in actual situations, amplifiers are also affected by other factors.

The combined effects of the input resistor R_{IN2} and input capacitor C_{IN2} on the second-stage amplifier constitute the low-pass filter for the amplifier, dictating how the amplifier responds to various input frequencies. Figure [5.13](#page-113-0) compares the simulated results and the measured results of the second stage amplifier when the input resistances are 1.6 k Ω and 1 Ω .

When R_{IN2} is equal to 1.6 k Ω , the simulated and measured results show similar trends. However, it is worth noting that the measured results show a slope (gain/frequency) that is twice that of the simulated results. Therefore, it can be learnt that the actual ASIC has another pole that provides an additional doubling of the slope attenuation. The reason for this may be that there is also stray capacitance in the ASIC implementation that is not reflected in the simulated case.

(a) Simulated gain over frequency for different R_{IN2} (b) Measured gain over frequency for different R_{IN2}

Figure 5.13: Gain over frequency for different R_{IN2} . Comparison between simulation and measurement results.

Figure 5.14: Spectrum diagram of RX amplifier

When the input resistance of R_{IN2} is set to 1 Ω , the low-pass filter in the simulation actually disables. This occurs because the corner frequency is considerably higher than the test frequency range and therefore has a negligible effect on the amplifier response. This presents the simulated case of $R_{IN2} = 1 \Omega$, where the gain change in this test frequency is less than 2 dB. However, in the actual measurement $(R_{IN2} = 1 \Omega)$, the gain of the signal shows a decrease in gain from 1.5 MHz to 4.5 MHz. This also demonstrates the existence of another pole present in the ASIC, providing additional low-pass filtering characteristics.

In the test comparison for R_{IN2} , we observed not only the effect of R_{IN2} on the ASIC bandwidth (low-pass characteristics), but also the existence of the other pole in the actual ASIC. This pole causes a gain change in an additional 4 dB. This gain change can be compensated in post signal processing.

As shown in Figure [5.14,](#page-114-0) a chirp signal with an amplitude of 2 mV_{pp} and a frequency range of 0.5 MHz to 7 MHz is introduced into a 3-stage RX amplifier during the receiver characterisation. The coloured dots represent the distribution of the measurement results for 100 receiver channels. The black realisation represents the average frequency response of the receiver channels, which shows an average bandwidth of 4.6 MHz and an average amplification of 54 dB. In addition, the actual measurements (coloured dots) show that the gain can vary up to 12 dB between channels.

5.1.6 Channel switching time

One of the primary objectives of [TAS](#page-144-0) III is the multiplexing of both the [TX](#page-144-1) and [RX](#page-143-0) channels. By leveraging external triggers, such as an external step signal or digital directives, the [MCU](#page-143-1) has the capability to configure the [ASIC](#page-142-0) through the SPI interface, subsequently selecting the appropriate channel. In this particular experiment, our goal was to determine the time taken by the amplifiers to switch from one channel to another after the appropriate configuration of the ASIC.

The experiment was conducted using the [FEB](#page-142-1) test platform. In this setup, the Arbitrary Waveform Generator (AWG) produced a consistent 1 MHz sine waveform, which acted as the input. The oscilloscope was employed to observe this input and measure the outputs.

5.1.6.1 Transmit channel switching time

Figure [5.15](#page-116-0) shows the time consumed by the switching of the [ASIC](#page-142-0) transmit source channel to any transmit target channel. When the time is positive, it indicates a delay in the switching process. When the time is negative, it indicates an overlap between switching processes.

The transmit switching time consists of two main components: the channel configuration time and the setup time of the transmit amplifiers. The [ASIC'](#page-142-0)s transmit channel is controlled by three sequential registers. Register A controls channel 1, channel 2, and channel 3. Register B controls channel 4, channel 5, and channel 6. Register C controls the remaining channels. When channel switching occurs in a single register (e.g., channel 4 switches to channel 5 in register B), the switching

Figure 5.15: Transmit channel switching time. The channel was switched from the source channel (X-axis) to the target channel (Y-axis). The color map represents the switching time. The negative time indicates the time when the source and target channels are turned on in overlap.

time can be determined by the setup time of the ASIC's transmit amplifier. This time is approximately 0.8 µs.

Configuration time must be considered when a register-to-register switching occurs. The neighboring register-to-register switch time is 60 us (A to B, B to C). Cross-register switches can be thought of as multiple register-to-register switches. For example, a register A to register C switch is equivalent to two adjacent register switches, A to B and B to C, with a switch time of 120 us. In addition, registers are always configured in the order of A to B to C. The configuration time for a register switch is 60 us (A to B, B to C). In addition, the registers are always configured in A to B to C order. Therefore, when the registers are switched back to front, the corresponding two channels are turned on during the switching period (overlap). For example, if transmit channel 8 (register C) is switched to channel 2 (register 2), the switching time is -120 µs.

Figure 5.16: Receive channel switching time. The channel was switched from the source channel (X-axis) to the target channel (Y-axis). The color map represents the switching time.

In real measurement scenarios, the USCT III always switches transmit channels sequentially and in the forward direction. This avoids channel overlap and crossregister switching. Thus, the transmit switching time does not exceed 65 µs.

5.1.6.2 Receive channel switching time

The [FEB'](#page-142-1)s receive channel switching time is approximately three orders of magnitude larger than the FEB transmit switching speed, i.e. tens to hundreds of ms. Figure [5.16](#page-117-0) shows the time it takes for the [ASIC](#page-142-0) to switch from one channel to another.

The receiving switching process is similar to the transmitting switching process and consists of the channel configuration time and the setup time of the transmit amplifiers. The receive channel is also controlled through three consecutive registers. Each register still controls three receive channels. The configuration time of the receiving channel is the same as that of the transmitting channel, which

is about 60 µs. However, since the setup time of the receiving amplifier is much higher than the configuration time, there is a delay in the switching process. This means that the switching time is always positive.

The receiving channel switching time can be divided into two situations: inregister switching and register-to-register switching. Switching within the register, the difference in switching time is small, with a standard deviation of approximately 2 ms. When switching between registers and registers, the reception switching time is relatively random, and the standard deviation reaches 25 ms. It is speculated that the longer switching time of the receiving channel may be related to the longer establishment time of the high gain of the receiving amplifier.

Based on the two modes described in Chapter [4.8,](#page-91-0) it is clear that the transmit priority mode minimizes the number of receive channel switching (only 5 times). In transmit priority mode, the USCT III system completes the entire measurement, spending only 738 ms on channel switching. In the receive priority mode, channel switching theoretically takes 1558 s, which is a factor 2000 slower than in the transmit priority mode. As a result, the transmit priority mode is the default scan mode for USCT III.

5.2 Distribution board characterisation

The distribution board serves as the central hub for power management and analog signal bridging within 32 [FEBs.](#page-142-1) To assess the functionality and performance of the distribution board, it was subjected to tests using a modified [FEB](#page-142-1) platform. The RJ45 port was employed with a 100 Ω matched connector for the introduction of the excitation signals. For the analog signal path, the DF80 port was connected through a coaxial cable to the analog signal interface board, previously utilized in [FEB](#page-142-1) testing, and then linked to either an oscilloscope or signal generator through the LEMO connector. It is noteworthy to mention that this testing also encompassed the characterization of the micro-coaxial cable.

Figure 5.17: Test setup of distribution board

5.2.1 Power characterisation

The power management of the distribution board provides sequential power-up as well as slew rate control for powering the 32 [TASs.](#page-144-0) In this chapter, the power supply module of the distribution board was measured.

Figure [5.18](#page-120-0) shows the power-up timing diagram for the USCT III distribution board with 32 [TASs.](#page-144-0) 32 [TASs](#page-144-0) are divided into four groups. Each group is limited to a voltage slew rate of 5 V/ms with 3 ms between groups. The inrush current for each group is about 1.4 A, and the stabilized current is about 650 mA. Due to the sequential power-up, the highest current occurs when the fourth group starts up, at about 3 A. The fifth and sixth current spikes are due to the power-up of the amplifiers for the on-board analog signal chain.

It should be noted that when the input supply voltage to the distribution board is 5 V, the actual output voltage of each voltage group is only 4.5 V. This is due to the voltage drop caused by the internal resistance of the cables and the transistors of load switches in the presence of high currents. This does not affect the normal operation of the [TASs](#page-144-0) as they can be operated over a voltage range of approximately 3.8 V to 5.5 V. Since the [TASs](#page-144-0) use low-dropout regulators

Figure 5.18: The power-up timing diagram for the USCT III distribution board with 32 FEBs. The X-axis represents time, the Y-axis on the left represents voltage, and the Y-axis on the right (green) represents current.

internally to generate the required voltages, a lower supply voltage reduces the power dissipated by the low-dropout regulators.

5.2.2 Transmit signal chain characterization

The transmit signal chain was shown and simulated in chapter [4.3.2.](#page-63-0) The transmit signal chain can be divided into three stages. The first stage is a differential to single-ended amplifier, the second stage is a multiplexer, and the third stage is a line driver. The measurements focused on the bandwidth as well as the switching time of the transmit signal chain.

The first stage gain is shown in Figure [5.19a.](#page-121-0) The observed gain of the stage from the measurement is about -7 dB. This is about a 10 $\%$ deviation from the expected design value of -6 dB. An essential observation is the -3 dB bandwidth of the stage, which ranges from 0.3 MHz to 9.5 MHz. Pertinently, within the [USCT'](#page-144-2)s specified bandwidth region of interest, which is between 0.5 MHz to 4.5 MHz, the flatness of the gain is about 1.5 dB.

The results of the second-and third-stage amplifiers are depicted in Figure [5.19b](#page-121-0) and [5.19c.](#page-121-0) Both stages utilize the same non-inverting amplifier design. The measured data shows that the mean gain for the second stage stands at roughly -0.6 dB, while the third stage's mean gain is approximately -0.2 dB. Intriguingly, the second stage's gain demonstrates a decline as the signal frequency increases, in contrast to the third stage, where the gain exhibits an uptick with the surge in signal frequency.

A crucial distinction influencing these contrasting behaviors is the disparate loads each amplifier manages. Specifically, the second-stage amplifier shoulders the responsibility of driving eight tertiary amplifiers concurrently. In contrast, the third-stage amplifier is typically designated for direct point-to-point signaling. This load difference directly influences their respective frequency responses.

In Figure [5.20,](#page-122-0) the frequency response for the complete transmit signal chain of the distribution board is presented. With an integrated design gain of -6 dB, the transmit chain of the distribution boards shows a -3 dB bandwidth over 9 MHz.

Figure 5.19: Spectrum diagram of each stage amplifiers on distribution board

Figure 5.20: Spectrum diagram of complete transmit signal chain

Notably, the gain of the distribution remains relatively constant over the frequency range of 0.5 MHz to 4.5 MHz, with a flatness deviation of less than 2 dB.

To summarise, the measurement results prove that the transmit signal chain is able to meet the bandwidth requirements (0.5 MHz to 5 MHz) of the [USCT](#page-144-2) system. However, comparing the actual measured signal chain with the simulated results, it can be seen that the actual measured bandwidth (9 MHz) is smaller than the simulated bandwidth results 22.9 (MHz). The main reason for this is that the bandwidth is affected by other characteristics of the amplifier, such as the gain-bandwidth product and the output slew rate, when compared to actual measurements.

The second stage of the transmit signal chain also serves as a signal multiplexer. The four second-stage amplifiers divide the input signal equally into four groups. A signal generator is used to produce a continuous sinusoidal signal at 100 kHz when measuring the switching times of the analog channels. An oscilloscope is used to simultaneously measure the outputs of the two second-stage amplifiers, i.e. CH1 and CH2. CH2 is initially switched on. The distribution board switches the

Figure 5.21: Transmit channel switching

second stage amplifier from CH2 to CH1 by the control command. By analysing the time domain signal and looking at Figure [5.21,](#page-123-0) the channel switching time is determined to be approximately 1.6 µs.

It is important to note that during channel switching, the channel being switched receives a step signal and generates a pulse signal. To avoid the pulse, channels should be switched when both channels are in standby whenever possible.

5.2.3 Receive signal chain characterisation

The receive signal chain of the distribution board is described in chapter [4.3.2.](#page-63-0) It consists mainly of a line driver as well as an isolation transformer to realize the isolation of the received signals. This experiment is used to determine the gain as well as the bandwidth of the receive signal chain. It is important to highlight that this test procedure includes the 800 mm micro-coaxial cable, which connects the [FEB](#page-142-1) to the distribution board.

Figure [5.22](#page-124-0) presents the frequency response for the receive signal chain. The average gain of the receive amplifier is close to -0.5 dB. The gain flatness is consistently 1.5 dB over the test frequency range of 0.3 MHz to 9.5 MHz. The

Figure 5.22: Spectrum diagram of RX amplifier on distribution board

actual gain of the receive signal chain is reduced by 0.9 dB compared to the simulated gain of 0.4 dB. This difference may be due to the 800 mm coaxial cable as well as the isolation transformer.

5.3 Water tank test

The purpose of the water tank test is to verify the [TAS,](#page-144-0) which includes [FEB](#page-142-1) and the transducers. As shown in Figure [5.23,](#page-125-0) the test is performed by mounting two opposing [TASs](#page-144-0) into a tank of size 19 x 15 cm. One [TAS](#page-144-0) is responsible for sending ultrasound signals, and the other is responsible for receiving ultrasound signals. The distance between the two [TASs](#page-144-0) is around 13 cm. In the test, the tank was filled with water as the medium.

The water tank test can provide an A-scan result as shown in Figure [5.24.](#page-126-0) The excitation signal is an up-chirped signal from 0.5 MHz to 4.5 MHz with a length of about 100 µs. The transmit signal is received after about 90 µs. The maximum

Figure 5.23: Water tank used in the test. The distance between TAS to TAS is about 13 cm.

amplitude of the received signal is about 4 Vpp. The transducer receives triple reflection signals. The time interval between the reflected signals is about 180 µs. Based on a distance of 13 cm between the two transducers, the speed of sound can be estimated to be about 1450 m/s . The third reflected signal detected by [TAS](#page-144-0) traveled more than 0.9 m.

Figure [5.24\(](#page-126-0)b) shows the normalized spectrum of the A-scan. It is clear that the transmitted signal uniformly covers the frequency range from 0.5 MHz to 4.5 MHz. However, the main frequency band of the received signal is between 2.2 and 2.8 MHz. There are still signal components from 0.5 to 2 MHz and above 3 MHz, but they are significantly smaller than those in the main frequency band range. Especially at frequencies above 3 MHz, the signal strength differs by a factor of about 10 compared to the main frequency band.

The frequency distribution of the received signal is, in one respect, dependent on the transducer bandwidth. Based on the results of the tank experiment described in previous studies [\[79,](#page-164-0) [80\]](#page-165-0) and the bandwidth of the USCT III sensor and its spectrum, it can be seen that the tank experiment follows the same trend.

(a) Excitation signal (A). Transmission signal (B). First reflection signal (C). Second reflection signal (D). Third reflection signal (E). The X-axis represents time, and the Y-axis represents signal amplitude.

(b) Normalized spectrum of received signal and excitation signal. The X-axis represents frequency, and the Y-axis represents normalized amplitude.

Figure 5.25: Simulated impedance of transducer and ASIC over frequency.

On the other hand, the impedance of the transducer and the input impedance of the [ASIC](#page-142-0) also have an effect. Figure [5.25\(](#page-126-1)a) shows the transducer equivalent impedance and the FEB input impedance. The input impedance of the [ASIC](#page-142-0) in orange is dominated by a 10 pF capacitor. Its impedance decreases with increasing frequency. The impedance of the transducer in blue is simulated according to the RLC model [Ref.].

Figure [5.25\(](#page-126-1)b) shows the factor of the input impedance of the [ASIC](#page-142-0) over the total impedance $(\delta(f) = Z_{AFE}/(Z_{AFE} + Z_{Transducer}))$, which can also be considered as the voltage gain coefficient from the transducer to the [ASIC.](#page-142-0) Figure [5.25\(](#page-126-1)b) shows that the factor δ is equal to 0.5 at 2 MHz. It means that the impedance of the transducer is equal to the input impedance of the [ASIC](#page-142-0) at 2 MHz. Half of the voltage generated by the transducer can be measured from the [ASIC.](#page-142-0) In addition, the [ASIC](#page-142-0) and transducer achieve maximum power matching at 2 MHz.

For low-frequency signals $(< 2$ MHz), the voltage gain coefficients are roughly in the range of 0.35 to 0.45, and for high-frequency signals $(> 3 \text{ MHz})$, they are in the range of approximately 0.15 to 0.25. This pattern is basically reflected in the frequency domain of the test results as shown in Figure [5.24\(](#page-126-0)b). The signal attenuation is most pronounced above 3 MHz due to the low voltage gain coefficients.

Assuming that the electrical signal from the transducer propagates at 0.7 times the speed of light. The bandwidth of the transducers is in the range of 0.5 MHz to 5 MHz. The electrical signal wavelength is approximately in the range of 42 m to 420 m. Since the USCT transducers are tightly coupled to the [ASIC](#page-142-0) (PCB trace < 10 cm), the signal reflection due to impedance mismatch is almost negligible. Therefore, it may be possible to reduce the signal attenuation at high frequencies (> 3 MHz) by increasing the input impedance of the [ASIC](#page-142-0) or decreasing the output impedance of the transducer.

5.4 System communication integration test

The system communication test examines the reliability of the digital communication of the system and the feasibility of the synchronisation triggering mechanism, i.e., STEP/ACK. During the integration test, the complete [USCT](#page-144-2) III system will be involved in the test.

Figure 5.26: Analysis of communication errors

5.4.1 Long-term communication monitoring

In each experiment, the [USCT](#page-144-2) III system requires configurations of the [TAS](#page-144-0) and distribution boards. These configurations consist of a series of settings, including parameters for each [TASs,](#page-144-0) STEP/ACK configurations, and the configurations of temperature measurement. After the measurement is complete, the USCT III system typically performs a self-calibration measurement as a reference. This measurement is also executed via digital communications.

To increase the robustness and diagnostic capability of the system, communication error recognition was integrated into the [USCT](#page-144-2) III system. As a result, the system is able to automatically detect communication errors such as [Cyclic Redundancy](#page-142-2) [Check \(CRC\)](#page-142-2) errors, timeout errors and so on. These errors are appropriately logged and categorized in the system log. Using this system logging mechanism, error rates associated with system communications can be analyzed and quantified retrospectively.

Figure [5.26](#page-128-0) shows that from September 2021 to July 2023, a total of 748 experiments were conducted by [USCT](#page-144-2) III, with 26.7 experiments per month in averaging. The [USCT](#page-144-2) III system sends an average of 17,879 commands per experiment.

During these experiments, the [USCT](#page-144-2) III system recorded 863 communication errors in 748 experiments. The average number of errors per experiment was 1.2. There were 21 [CRC](#page-142-2) errors, 256 timeouts and 586 access overruns. These accounted for 2.4%, 29.7% and 67.9% of the total errors, respectively.

Before April 2022, the [USCT](#page-144-2) III system had about five communication errors per experiment, with a communication error probability of about 2.8 ‰, after which the [USCT](#page-144-2) III communication error rate continued to decrease. The error rate is slightly less than 1 error per experiment, implying a communication probability of about 0.6 ‰. In February 2023, there was a rebound in communication errors for the [USCT](#page-144-2) system. This was due to the hardware damage from water leakage.

It should be noted that errors detected by the USCT III system can be corrected in most cases. When the first error is detected, the USCT III system tries to send the instruction again through the [Automatic Repeat Request \(ARQ\).](#page-142-3) The probability of an error occurring in both sending instructions is less than 0.3 millionths.

5.4.2 Programmable time delay in trigger system

Preliminary tests in chapter [5.1.6](#page-115-0) show the discrepancy: the receive channel switching time (in) of [FEB](#page-142-1) greatly exceeded the switching duration (in microseconds) of the transmit channel. Given this apparent timing inconsistency, the design and functionality of the programmable trigger mechanism of [USCT](#page-144-2) is of particular importance. The switching time can be programmed for different operations, thus allowing the USCT III system to both ensure adequate channel switching time and minimize the complete measurement time.

Figure [5.27](#page-130-0) shows each STEP/ACK process time, which is measured in one complete measurement. The measurement was configured in transmit priority mode (this mode is described in chapter [4.8\)](#page-91-0). In the experiment, the receive channel switching time was set to 100 ms by the programmable trigger in the FEB. The transmit switching time was set to 200 µs.

(a) Ack signals measured in transmit priority mode. The X-axis represents the number of steps, and the Y-axis represents the execution time under each step. The five 0.1 s spikes represent the system performing receive channel switching.

(b) Enlarged view of A. The X-axis represents the number of steps, and the Y-axis represents the execution time under each step. The five 0.1 s spikes represent the system performing receive channel switching. The spikes represent the switching time (between TAS to TAS) of 0.5 ms.

Figure 5.27: ACK signals in one complete measurement, which was recorded by the DAQ system

Five switching of the receive channel can be clearly observed in Figure [5.27\(](#page-130-0)a). The duration of this activity recorded by the DAQ is about 105 ms. This duration includes not only the receive channel switching time but also the time consumed by the DAQ measurements. The interval between the five channel switches is 2304 steps. This is because in transmit priority mode, all 2304 transducers are traversed to transmit the ultrasound signal after switching the receive channel. It should be emphasized that among the five receive channel switching events, the switching event of the transmitter channel is ambiguous. Since the DAQ only records the longest STEP/ACK process, the relatively short transmit channel switching duration is still masked by the long receive channel switching duration.

An expanded view of region A is illustrated in Figure [5.27\(](#page-130-0)b). Since transmit channel switching occurs during each STEP/ACK, transmit channel switching can not be explicitly observed. Therefore, in the experiment, a TAS to TAS switching time was configured to 500 µs. This is the repetitive signal with a period of 18 steps as shown in Figure [5.27\(](#page-130-0)b). This frequency represents that after 18 transducers of a TAS have been traversed, the next TAS starts to work.

5.5 USCT III comprehensive performance

Comprehensive testing focused on system-level imaging testing of the USCT III system and comparison to the USCT II system. Comprehensive testing includes transmission tomography, reflection tomography, and clinical study.

5.5.1 Transmission tomography

To evaluate the image quality of transmission tomography, a custom phantom was made as shown in [5.28](#page-131-0) [\[81,](#page-154-0) [82\]](#page-165-1). It consisted of a gelatine body $(15 \text{ g of}$ gelatine per 100 ml of water) and four spherical inclusions made of [polyvinyl chloride](#page-143-2) [\(PVC\)](#page-143-2) and dioctyl terephthalate (softener) [\[82\]](#page-165-1). The diameter of the inclusions is between 0.8 cm and 2.2 cm. The acoustic properties of the gelatine and the inclusions are similar to the properties of human breast tissue.

The ground truth for sound speed and attenuation was measured with a dedicated setup consisting of two opposing ultrasound transducers in a water bath [\[83\]](#page-165-2). The

Figure 5.28: Custom phantom made of gelatine main body (yellow) and PVC inclusions (greyish purple) [\[81,](#page-154-0) [82\]](#page-165-1)

(a) Sound speed reconstruction. The views from left to right are a front view, a side view, and a top view. The color map shows the different speeds of sound.

(b) Attenuation reconstructions. The views from left to right are a front view, a side view, and a top view. Color map shows the different attenuation of ultrasound.

Figure 5.29: Reconstruction of the gelatine phantom with PVC inclusions[\[82\]](#page-165-1)

speed of sound and attenuation was measured as $1530 \text{ m/s } (\pm 10 \text{ m/s at } 20 \text{ °C})$ and 0.4 dB/cm ($\pm 0.1 \text{ cm}$) in gelatin. The speed of the sound and attenuation of the PVC inclusions was $1430 \text{ m/s } (\pm 2 \text{ m/s})$ and $5.9 \text{ dB/cm } (\pm 0.5 \text{ cm})$ [\[82\]](#page-165-1).

The reconstructions were carried out using ray-based tomography [\[81\]](#page-154-0). The worst-case limitation for the resolution was configured to 1.5 cm [\[81\]](#page-154-0). As shown in Figure [5.29,](#page-132-0) all inclusions were clearly visible in both speed of sound and attenuation reconstructions.

The averaging speed of sound of the main body was reconstructed at 1531.3 m/s . closely aligning with the 1530 m/s ground truth. The mean attenuation averaged over frequency was 0.62 cm, slightly higher than the ground truth of the 0.42 cm. The largest inclusion had a speed of sound of 1436.1 m/s (ground truth 1430) m/s) and an attenuation of 6.1 cm (ground truth 5.9 cm). Smaller inclusions showed greater deviation, with values up to 1452.5 m/s for speed of sound and 3.0 cm for attenuation.

In summary, the imaging results with phantom data show deviations below 5 m/s and 0.2 dB/cm for the phantom body, and below 15 m/s and 0.2 dB/cm for the

(a) Steel balls with a diameter of 50 mm (b) 200 µm aluminium wire

Figure 5.30: Objects used for reflection tomography

largest inclusion [\[82\]](#page-165-1). Given the ground truth's standard deviation, these results are considered to be in good agreement.

5.5.2 Reflection tomography

The reflection experiments were carried out on metallic objects, i.e., the steel ball and the wire tests. Figure [5.30\(](#page-133-0)a) shows the 50 mm diameter steel ball, slightly off-center, held into the USCT III device. Figure [5.30\(](#page-133-0)b) shows a 200 μ m aluminum wire draped through the holder in water.

Figure [5.31](#page-134-0) shows the 3D results of the USCT III steel ball experiments. The data of one aperture position was acquired (approx. 5 million A-scans).The voxel resolution was 0.5 mm [\[81\]](#page-154-0). The greyscale represents the intensity of the reflection. The brighter the greyscale, the higher the reflection intensity.

In the 3D reconstruction, the steel ball and the steel rod connecting the ball were clearly visible in Figure [5.31.](#page-134-0) The bottom part of the steel ball was imaged more clearly. This is because the hemispherical aperture covers the entire lower hemisphere and captures more reflected signals. In addition, the water-air interface can be observed in the 3D reconstruction. The interface showed a circular shape,

Figure 5.31: 3D reflectivity reconstruction of the 50 mm steel ball

struction with 3D USCT II [\[49\]](#page-161-0)

struction with 3D USCT III [\[81\]](#page-154-0)

Figure 5.32: A comparison of the maximum cross-sections of the USCT II and USCT III steel ball experiments

which may be due to the fact that more signal from the ROI section was reflected by the object (i.e. the steel ball).

Figure [5.32](#page-134-1) shows a comparison of the maximum cross-sections of the USCT II and USCT III steel ball experiments. From the results, it can be seen that both USCT II and USCT III are able to reconstruct the steel spheres by reflection very well. Quantitatively, the ratio of the maximum greyvalue in the background to the

Figure 5.33: The maximum intensity projection of the aluminum wire imaged with reflection tomography. The figure shows the xz-plane. The sub-volumes (vol 1 to vol 7) were reconstructed with a resolution of approximately 0.1 μ m.

maximum greyvalue of the sphere is 30.3 % for USCT II and 15.4 % for USCT III [\[49,](#page-161-0) [81\]](#page-154-0).

Figure [5.33](#page-135-0) shows a maximum intensity projection of the aluminum wire imaged by reflection tomography [\[82\]](#page-165-1). The overall resolution of this image was reduced to approximately 1.5 mm. Smaller sub-volumes (vol 1 to vol 7) were reconstructed at a finer resolution of about 0.1 mm at specific locations. These sub-volume average measurements are 0.24 mm ± 0.05 mm for the x-axis, 0.27 mm ± 0.08 mm for the y-axis, and 0.27 mm ± 0.08 mm for the z-axis [\[82\]](#page-165-1). This demonstrates the higher resolution that USCT III can achieve in maximum intensity protection.

In summary, the lower ratio of the maximum greyvalue in the background to the maximum greyvalue of the sphere of USCT III indicates that USCT III has a better contrast than USCT II. In addition, the aluminum wire experiment indicates that USCT III has sub-cm imaging capability. These results are considered to be in good agreement.

(a) 3D reflectivity reconstruction by USCT II. Front view (left). Side view (middle). Top view (right)

(b) 3D reflectivity reconstruction by USCT III. Front view (left). Side view (middle). Top view (right).

Figure 5.34: The reflectivity reconstruction of the same healthy volunteer using USCT II (top) and USCT III (bottom)

5.5.3 Clinical study

Figure [5.34](#page-136-0) compares reflectivity reconstruction using USCT II (top) and USCT III (bottom) of the same healthy volunteer [\[81\]](#page-154-0). In terms of internal structure, the USCT III results showed significantly higher breast tissue contrast and suppression of lobar artifacts on the breast surface. Contrasting the external shape, the external contour imaged by USCT III is much shaper. Especially in the nipple area, USCT III does not show the mosaicization of USCT II. This reflects the higher spatial resolution of USCT III. In addition, the USCT III has a larger aperture, so optimal illumination and contrast can be obtained for more tissue in the ROI. For transmission tomography, this also means that more breast tissue can be imaged because, according to beam assumptions, only the tissue within the area covered by the transducer can be reconstructed [\[81\]](#page-154-0).

6 Discussion

The central goal of this work was to develop a next-generation USCT prototype (3D USCT III) for large-scale clinical studies. As a novel medical imaging method, USCT III allows full 3D ultrasound reconstruction for early cancer detection. In addition, 3D USCT is capable of simultaneous transmission and reflection imaging which is expected to have high specificity in detecting cancerous tissues [\[84\]](#page-165-3).

The central questions for this research were as follows:

- How to design and implement a fast, safe and reliable 3D USCT III prototype to perform ultrasound computed tomography on a large-scale clinical setting?
- How to get more unduplicated A-scans for a given number of USCT transducers?
- How to design and implement the analog signal chain of the 3D USCT III? What is its bandwidth and amplification performance?
- How to characterise the front-end ASIC? How to integrate it into the USCT III system? What advantages and limitations does the ASIC bring to the system?

These questions were all addressed successfully, and the following results were achieved.

Worldwide multi-center clinical studies

Phantom and volunteer imaging experiments have been conducted on two USCT III systems. Analyses show that the USCT III provides higher quality imaging with fewer artifacts than the previous generation system. Quantitatively, the ratio of the maximum greyvalue in the background to the maximum greyvalue of the sphere is 30.3 % for USCT II and 15.4 % for USCT III.

Measurement acceleration

With an average number of 4, the USCT III acquires 10 million A-scans (a complete measurement) in 97 seconds. Compared to the previous generation USCT II, the USCT III is 2.3 times faster. These improvements are directly related to the new system architecture, the optimized scanning strategy and the synergy of the various components (e.g., TAS, distribution board and DAQ).

Fast and stable digital communications

The communication architecture of the USCT III was designed to enable fast and stable communications in the complex system. Signal reflections and oscillations faced by USCT III's communication system when using non-standard wires (coaxial instead of twisted pair) and star topology were identified and resolved by simulation. In long-term tracking tests, the USCT III's communication error rate was approximately 0.6 ‰. Combined with automatic repeat requests at the software level, the USCT III is virtually free of communication problems.

Programmable global triggers and NOR gate acknowledge enable pseudo realtime control of the 3D USCT III system. In contrast to the USCT II system, each device in the USCT III trigger system, e.g. TAS and distribution boards, can set its own minimum wait time, maximum timeout, etc. As the STEP and ACK signals cascade through the system, a small number of device errors will not affect the reliable operation of the USCT III system. In addition, the DAQ system is able to monitor the time of each step, so as to analyse the current operation of the system.

Effective power management

Effective power management keeps the 3D USCT III system running reliably. Sequential power-up and slew rate control effectively reduce the inrush current from 8 A to less than 4 A for each sensor cluster. The power tests not only determine the power characteristics of the individual modules, but also test the power-up and power-down behaviour of the system.

Multiplexing of transmit-receive channels for USCT transducers

On the system level, the 3D USCT III prototype enables the multiplexing of transmit-receive channels for the first time. With only a 12.9 % increase in number of transducers, the number of A-scans was increased by a factor of six. This enables the 3D USCT III system to obtain ten million A-scans with only two measurement positions. In addition, the system scalability of 3D USCT III prepares the system for a movement-free, and thus even faster USCT system.

Characterisation of the analog signal chains

The overall characteristics of analog signal chains of the USCT III system, i.e. the transmit signal chain characteristics as well as the receive signal chain characteristics, were simulated and measured. The complete transmit signal chain has a fixed gain of 29.9 dB. Arbitrary waveforms up to 90 Vpp can be transmitted. The receive signal chain has an average gain of 55.5 dB with a deviation of 12 dB. The receive signal chain has a -6 dB bandwidth of approximately 4.5 MHz. In addition, the receive signal chain has a variable gain of at least 16 dB.

ASIC modelling and characterisation

The ASIC receive equivalent model was presented. It was shown experimentally that the model can predict the filter characteristics and the gain of the receive amplifiers of the ASIC. In addition, the channel switching time of the USCT ASIC is also measured experimentally. The transmit channel switching of the USCT ASIC is only affected by the communication time, which is usually no more than 120 us. The receive channel switching time is about 100 ms, indicating that the receive amplifiers of the USCT ASIC require a long setup time.

Outlook

The USCT III implements a single-frequency power matching of the transducer and the receive amplifier around 2 MHz, which results in a significant reduction of the voltage gain factor at other frequencies as a trade-off. Based on current theories, it may be more effective to increase the analog bandwidth by increasing the voltage gain factor where signal reflections do not affect the tightly coupled TAS III. Therefore, by exploring impedance matching, the voltage gain coefficient may be able to improve further the bandwidth as well as the SNR of the USCT system.

In the long run, the USCT III system also has great potential for expansion. Utilizing the scalability of the USCT III, it is possible for the USCT III system to support additional transducers, resulting in a movement-free USCT III system. In addition, if the USCT III system can be miniaturized, it may also be used for wearable device applications.

The USCT III system is currently being prepared for a large number of clinical studies with more than 1000 patients in different countries. If the USCT III system proves to be effective, it could become a new, harmless and cost-effective means of breast cancer screening.

Abbreviations

- **AAF** Anti-Aliasing Filters
- **ADC** Analog Digital Converter
- **AFE** Analog Front-end
- **AMC** Advanced Mezzanine Card
- **ARQ** Automatic Repeat Request

ASIC Application Specific Integrated Circuit

- **BJT** Bipolar Junction Transistor
- **CMUT** Capacitive Micromachined Ultrasonic Transducer
- **CRC** Cyclic Redundancy Check
- **DAC** Digital Analog Converter
- **DAQ** Data Acquisition
- **DMA** Direct Memory Access
- **FEB** Front-end Board
- **FMC** (FPGA Mezzanine Card

GBW gain-bandwidth product

GUI graphical user interface

JTAG Joint Test Action Group

KCL Kirchhoff's Current Law

KIT Karlsruhe Institute of Technology

KVL Kirchhoff's Voltage Law

MCU Micro Controller Unit

MOSFET Metal Oxide Semiconductor Field Effect Transistor

NMOS N-channel Metal Oxide Semiconductor

OSI Open Systems Interconnection

PCB Printed Circuit Board

PCIe Peripheral Component Interconnect Express

PMOS P-channel Metal Oxide Semiconductor

PMUT Piezoelectric Micromachined Ultrasonic Transducer

PVC polyvinyl chloride

RTM Rear Transition Module

RX Receive

SFP Small Form-factor Pluggable Transceiver
- **SPI** serial peripheral interface
- **T/R** Transmit/Receive
- **TAS** Transducer Array System
- **TDM** Time-division multiplexing
- **TOF** Time Of Flight
- **TX** Transmit
- **USCT** Ultrasound Computer Tomography
- **VGA** Variable Gain Amplifier
- **VISA** Virtual instrument software architecture

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