Silicon Transceiver Design for D-Band Communication and Radar Applications

Zur Erlangung des akademischen Grades eines

DOKTORS DER INGENIEURWISSENSCHAFTEN
(Dr.-Ing.)

von der KIT-Fakultät für
Elektrotechnik und Informationstechnik
des Karlsruher Instituts für Technologie (KIT)

genehmigte

DISSERTATION

von

M.Sc. İbrahim Kağan Aksoyak
geb. in Konya-Türkei

Tag der mündlichen Prüfung:	28.05.2024
Hauptreferent:	Prof. Dr.-Ing. Ahmet Çağrı Ulusoy
Korreferent:	Prof. Dr.-Ing. Hermann Schumacher

Zusammenfassung

Auf der Suche nach Kommunikationssystemen, die Datenraten von über 100 Gbit/s erreichen können, ein Ziel, das oft für 6G und darüber hinaus vorgestellt wird, werden bisher drahtgebundene oder optische Verbindungen bevorzugt. Jedoch hat die Verwendung des Millimeterwellen Frequenzbereichs auch für drahtlose Kommunikationssysteme den Weg, vergleichbare Datenraten zu erreichen, geebnet. Der *D*-Band Frequenzbereich (110 – 170 GHz) zeichnet sich als vielversprechender Kandidat für 6G-Verbindungen ab und bietet ausreichend Bandbreite für leistungsfähigere Übertragungssysteme. Darüber hinaus eröffnet die umfangreiche Bandbreite bei *D*-Band Frequenzen Möglichkeiten für hochpräzise Sensoranwendungen, insbesondere in der Radartechnologie. Diese Dissertation untersucht Silizium Transceiver Technologien, die bei *D*-Band Frequenzen arbeiten, und zielt sowohl auf Kommunikations- als auch Radaranwendungen ab. Die vorgelegte Forschung ist hauptsächlich auf zwei Schlüsselaspekte konzentriert: Hochleistungsverstärkung und rauscharmer Empfang. Durch eine umfassende Untersuchung adressiert diese Arbeit die Einschränkungen bestehender Silizium-basierter Technologien und bietet gleichzeitig systematische Design- und Optimierungsmethoden für Millimeterwellen RF Frontends.

Ein Schwerpunkt liegt auf dem Design und der Optimierung von *D*-Band Leistungsverstärkern. Es wird eine systematische Designmethodik für Millimeterwellen Leistungsverstärker präsentiert, die hauptsächlich darauf abzielt, sowohl die Ausgangsleistung als auch die Effizienz zu verbessern. Ein zweistufiger Kaskoden Leistungsverstärker wird unter Verwendung einer 130 nm Silizium-Germanium Bipolar-CMOS Technologie als Referenzdesign implementiert, wobei eine gemessene gesättigte Ausgangsleistung von 15 dBm und eine maximale Leistungsverstärkungseffizienz von 7.8 % bei 140 GHz erreicht werden, ohne dabei auf Leistungskombination zurückzugreifen. Anschließend wird eine modifizierte Kaskodenschaltung verwendet, um den Leistungsverstärker weiter zu optimieren. Dieses Design integriert außerdem eine Vier-Wege Leis-

tungskombination, um die Ausgangsleistung zu steigern, wobei eine gemessene gesättigte Ausgangsleistung von 19.6 dBm und eine maximale Leistungsverstärkungseffizienz von 9.5 % bei 130 GHz erreicht werden. Unter Verwendung einer fortschrittlichen Silizium-Germanium Bipolar-CMOS Technologie mit schnelleren Bauelementen und einer Kupfermetallisierung zur Reduzierung von Verlusten, wird ein weiterer Vier-Wege Leistungsverstärker vorgeschlagen. Dieses Design erreicht eine gesättigte Ausgangsleistung von 23.7 dBm und eine maximale Leistungsverstärkungseffizienz von 16.6 % bei 136 GHz und belegt eine kompakte Gesamt-integrierte Schaltung-Fläche von 1.4 mm^2. Eine umfassende Liste von Leistungsverstärkern, die über 100 GHz arbeiten, wird präsentiert. Die vorgeschlagenen Leistungsverstärker zeigen Performanz auf dem neuesten Stand der Technik im Vergleich zu anderen auf Silizium basierenden Gegenstücken in der vorhandenen Literatur.

Ein weiterer Schwerpunkt liegt auf dem Design und der Entwicklung von *D*-Band rauscharmen Verstärkern mit einer systematischen Designmethodik. Es werden zwei unterschiedliche rauscharme Verstärker präsentiert. Der erste rauscharme Verstärker verwendet eine zweistufige differentielle Kaskoden-Topologie mit Verstärkungsanhebungstechnik und Rauschunterdrückungstechniken. Dieses Design erreicht eine gemessene Verstärkung von 20 dB, einen eingangsbezogenen 1 dB Kompressionspunkt von −19.7 dBm bei 140 GHz und verbraucht eine Gleichstromleistung von 31.8 mW. Das Design zeigt auch eine simulierte Rauschzahl von 5.9 dB. Der zweite rauscharme Verstärker nutzt eine fortgeschrittenere Silizium-Germanium Bipolar-CMOS Technologie und erreicht eine Rauschzahl von 4.6 dB bei 140 GHz. Darüber hinaus weist dieses Design eine Verstärkung von 24 dB mit einem eingangsbezogenen 1 dB Kompressionspunkt von −21.5 dBm bei einem Verbrauch von nur 13 mW auf. Ein umfassender Vergleich zu vorhandenen rauscharmen Verstärkern, die über 100 GHz arbeiten, wird präsentiert.

Unter Verwendung einer 130 nm Silizium-Germanium Bipolar-CMOS Technologie, wird ein vollständig differentieller *D*-Band I/Q Transceiver für Kommunikations– und Radaranwendungen entwickelt. Traditionelle Transceiver Architekturen, die einen rauscharmen Verstärker als erste Komponente des Empfängers verwenden, stehen vor Herausforderungen aufgrund von Übersprechens des Sendepfads in den Empfangspfad während des Sendevorgangs. Um dies zu adressieren, verwendet der vorgeschlagene Transceiver eine Mixer-First-Architektur im Empfangspfad, eliminiert den rauscharmen

Verstärker und verwendet zum Heruntermischen rauscharme Mischer. Dieser Ansatz bietet im Vergleich zur Nutzung eines rauscharmen Verstärkers ein verbessertes Kompressionsverhalten und verhindert, dass das Übersprechen aus dem Sendepfad den Empfangspfad stört, ohne zusätzliche Kompensationstechniken zu erfordern. Der Mixer-First-Empfangspfad zeigt eine gemessene Doppel-Seitenband-Rauschzahl von 8.2 dB und einen eingangsbezogenen 1 dB Kompressionspunkt von −3.5 dBm. Der Transceiver integriert auch einen Frequenzverdoppler und einen LO-Treiber-Verstärker zur LO-Erzeugung, wobei der Schwerpunkt auf einem breitbandigen Betrieb und einer optimierten LO-Leistungsverteilung liegt. Der Sendekanal verwendet einen differentiellen Leistungsteiler, der LO-Leistung an aufwärtsmischende Mischer liefert, gefolgt von einem Hybridkoppler und einem Leistungsverstärker. Der Sendekanal erreicht eine maximale Ausgangsleistung von 5.8 dBm und einen ausgangsbezogenen 1 dB Kompressionspunkt von 1.6 dBm bei einer RF-Frequenz von 135 GHz und einer IF-Frequenz von 1 GHz. Der Transceiver-Chip belegt eine Fläche von 1.58 mm^2 und verbraucht 189 mW, wenn der Sendekanal mit maximaler Ausgangsleistung betrieben wird.

Abstract

In pursuit of communication systems capable of exceeding data rates of 100 Gbit/s, a target often envisioned for 6G and beyond, traditional approaches have favored wire-line or optical links. However, the use of millimeter-wave (mm-wave) frequencies has paved the way for wireless communication systems to achieve comparable data rates. The *D*-band frequency range (110 – 170 GHz) stands out as a promising candidate for 6G links, offering ample bandwidth for enhanced performance. Additionally, the extensive bandwidth available at *D*-band frequencies creates opportunities for high-precision sensing applications, particularly in radar technology. This dissertation explores silicon (Si) transceiver technologies operating at *D*-band frequencies, targeting both communication and radar applications. The research primarily focuses on two key aspects: high-power amplification and low-noise reception. Through a comprehensive investigation, this work addresses the limitations of existing Si-based technologies, while offering systematic design and optimization methodologies for mm-wave RF front ends.

One area of focus is the design and optimization of *D*-band power amplifiers (PAs). A systematic design methodology for mm-wave PAs, with the primary aim of enhancing both output power and efficiency is presented. A two-stage cascode PA is implemented using a 130 nm silicon-germanium (SiGe) bipolar complementary metal-oxide-semiconductor (BiCMOS) technology as a benchmark design, achieving a measured saturated output power of 15 dBm and a maximum power-added-efficiency (PAE) of 7.8 % at 140 GHz, all without employing any power combining techniques. Subsequently, a modified-cascode approach is adopted to further optimize the cascode PA. This design incorporates a four-way power combiner to boost the output power, achieving a measured saturated output power of 19.6 dBm and a maximum PAE of 9.5 % at 130 GHz. Leveraging an advanced SiGe BiCMOS technology with faster devices and a copper (Cu) back-end-of-line (BEOL) for reduced losses, another four-way power combined cascode PA is proposed. This design achieves a sat-

urated output power of 23.7 dBm and a maximum PAE of 16.6 % at 136 GHz, occupying a compact total integrated circuit (IC) area of 1.4 mm^2. A comprehensive list of PAs operating above 100 GHz is presented. The proposed PAs demonstrate state-of-the-art (SoA) performances when compared to other Si-based counterparts in existing literature.

Another focus area is the design and development of *D*-band low-noise amplifiers (LNAs) with a systematic design methodology. Two distinct LNA designs are presented. The first LNA utilizes a two-stage differential cascode topology with gain boosting and noise reduction techniques. This design achieves a measured gain of 20 dB, input-referred 1 dB compression-point (IP_{1dB}) of −19.7 dBm at 140 GHz, while consuming a DC power of 31.8 mW. The design also demonstrates a simulated noise-figure (NF) of 5.9 dB. The second LNA leverages a successor SiGe BiCMOS technology, leading to a NF of 4.6 dB at 140 GHz. Additionally, this LNA exhibits a gain of 24 dB with an IP_{1dB} of −21.5 dBm while consuming only 13 mW. A comprehensive comparison to existing LNAs operating above 100 GHz is provided.

A fully differential *D*-band quadrature (I/Q) transceiver (TRX) is designed for communication and radar applications, using a 130 nm SiGe BiCMOS technology. Traditional TRX architectures using an LNA as the first receiver (RX) component face challenges due to transmitter (TX)-to-RX spillover during high-power transmission. To address this, the proposed TRX employs a mixer-first architecture in the RX path, eliminating the LNA and using low-noise downconverting mixers. This approach, thanks to an improved compression behavior compared to an LNA-based RX, prevents the TX-to-RX spillover from disrupting the RX performance without requiring additional leakage cancellation techniques. The mixer-first RX demonstrates a measured double-sideband (DSB) NF of 8.2 dB and an IP_{1dB} of −3.5 dBm at an RF frequency of 140 GHz and an IF frequency of 1 GHz. The TRX also includes a frequency doubler and a LO driver amplifier for LO generation, prioritizing wideband operation and optimized LO power distribution. The TX channel utilizes a differential power divider feeding LO power to upconverting mixers, followed by a hybrid coupler and a PA. The TX achieves a maximum output power of 5.8 dBm and an output-referred 1 dB compression-point (OP_{1dB}) of 1.6 dBm at an RF frequency of 135 GHz and an IF frequency of 1 GHz. The TRX chip occupies an area of 1.58 mm^2 and consumes 189 mW when the TX operates at maximum output power.

To my beloved parents, Hatice and Şeref,
for their unconditional love, support,
and sacrifices in raising me and my brother, Berk.

Acknowledgement

First of all, I would like to express my sincere gratitude to my advisor, Prof. Dr.-Ing. Ahmet Çağrı Ulusoy, for his valuable guidance, mentoring and encouragement. Throughout my graduate studies, he has consistently and patiently supported me with utmost interest and I deeply appreciate his belief in me. Under his supervision, I not only learned the fundamentals of RFIC design, but also developed the confidence to pursue my own research path with passion.

I would also like to thank the members of my committee: Prof. Dr.-Ing. Hermann Schumacher, Prof. Dr. rer. nat. Ulrich Lemmer, Prof. Dr.-Ing. Marc Hiller and Prof. Dr. Marc Weber for their contributions to this dissertation and sparing time.

During my graduate studies, I had the chance to meet exceptionally intelligent and good people. During my time in the U.S, I learned a lot from Asad Ali Nawaz and Si-Wook Yoo about circuit design and I am thankful for all the advice, insights and friendship that they shared with me. Additionally, I extend my gratitude to my other former lab mates: Shih-Chang Hung, Xenofon Konstantinou, and Jubaid Abdul Qayyum. I remember our times together with a big smile on my face.

Next, I would like to thank all the members of the circuit design team at IHE for their friendship and support. I have considered them not only as colleagues but also as cherished friends. The past four and a half years of sharing an office with Alexander Haag and Selina Eckel have been very nice. We have made countless memories together, with mutual respect, shared goals and cooperative working atmosphere. Our office has really been a great place to work! Big thanks to Matthias Möck and Kaan Balaban: the memories we have made, from cheerful celebrations to tough times, are priceless. I have continuously felt your full support and sincere friendships. Special thanks to Matthias, for mental and intellectual support during the measurements. I have enjoyed the company of Tsung-Ching Tsai and Tai-Yu Kuo. Along with all the

technical discussions we have had, we have also shared a lot of laughter. I am also thankful for the friendships and technical discussions with Eşref Türkmen, Christian Bohn, Kateryna Smirnova, Xinyu Kong, and Anıl Aslan.

I also appreciate the friendly atmosphere at IHE and would like to thank all the colleagues. Special thanks to the technical staff, Andreas Lipp and Thorsten Fux, for their assistance and support in PCB manufacturing and assemblies. Furthermore, I am thankful to Angela Ziemba, Marion Jentzsch, and Simone Gorré for managing the daily operations and bureaucratic matters for all of us.

I am truly happy for the close friendship that I still maintain with my high school buddies, Talha Akyıldız, Davut Yücedağ, Mustafa Bölük, Ali Aktaş, and Mustafa Sayıcı. The countless hours we have spent chatting over video calls and the reunions we have been able to make back at home are invaluable. I would also like to thank Kerem Gülcan for his friendship. I feel simply lucky that we have managed to stay so close despite the distance.

I owe a deep gratitude to my family. My parents, Hatice and Şeref, have raised me and my brother with unconditional love, care, and continuous support, making countless sacrifices for our well-being. Their encouragement has helped me to achieve my goals, and their belief in me has motivated me and shaped me into the person I am today. My brother, Berk, has always brought immense joy in my life. From our childhood days of playing football in the living room to the countless adventures we have shared over the years, his presence has been comforting, fun and an important source of encouragement.

Anneciğim, babacığım ve canım kardeşim, sizleri çok seviyorum!

Last but not least, I would like to thank my fiancée, Alexandra, who has been a constant source of inspiration, true love, and strength. She has been very patient, understanding, and supportive in my pursuit of achieving my goals.

28 July 2024
Freising, Germany

İbrahim Kağan Aksoyak

Contents

Acronyms and symbols

Acronyms

Al	aluminum
balun	balanced-unbalanced unit
BEOL	back-end-of-line
BER	bit error rate
BJT	homojunction bipolar transistor
BiCMOS	bipolar complementary metal-oxide-semiconductor
CB	common base
CC	common collector
CE	common emiter
CG	conversion gain
CL	coupled line
CMOS	complementary metal-oxide semiconductor
Cu	copper
DA	driver amplifier
DC	downconversion
DSB	double-sideband
DUT	device-under-test

DoAC	doubler-amplifier chain
EIRP	equivalent isotropic radiated power
EM	electromagnetic
EVM	error vector magnitude
F	noise-factor
FMCW	frequency modulated continuous-wave
FRR	fundamental rejection ratio
FSPL	free-space path loss
FoM	figure-of-merit
GND	ground
GaN	gallium nitride
Ge	germanium
HBT	heterojunction bipolar transistor
HEMT	high electron mobility transistor
I/O	input/output
I/Q	quadrature
IC	integrated circuit
IHE	Institute of Radio Frequency Engineering and Electronics
IHP	Leibniz Institute for High Performance Microelectronics
IL	insertion loss
IMN	input matching network
IRR	image rejection-ratio
I-V	current-voltage

KIT	Karlsruhe Institute of Technology
LNA	low-noise amplifier
MAG	maximum available gain
mm-wave	millimeter-wave
MOM	metal-oxide-metal
MOSFET	metal-oxide-semiconductor field-effect transistor
MS	microstrip
MX	mixer
NF	noise-figure
PA	power amplifier
PAE	power-added-efficiency
PAPR	peak-to-average power ratio
PCB	printed circuit board
PMCW	phase modulated continuous-wave
PPFD	push-push frequency doubler
PSD	power spectral density
Q	quality factor
QAM	quadrature amplitude modulation
RCS	radar cross section
RL	return loss
RX	receiver
Si	silicon
SiGe	silicon-germanium

SNR	signal-to-noise-ratio
SoA	state-of-the-art
SSB	single-sideband
TL	transmission line
TRX	transceiver
TX	transmitter
VCO	voltage-controlled-oscillator
UC	upconversion
x2	frequency doubler

Frequently used symbols

α	Conduction angle
A_{R}	Effective area of the receiving antenna
B	Bandwidth
$B_{3\mathrm{dB}}$	3-dB bandwidth
$\mathrm{B}V_{\mathrm{CBO}}$	Open-emitter collector-base breakdown voltage
$\mathrm{B}V_{\mathrm{CEO}}$	Open-base collector-emitter breakdown voltage
C	Capacitor
η	Collector efficiency
f_{MAX}	Maximum frequency of oscillation
f_{T}	Unity current gain cut-off frequency
F_N	Noise factor of stage N
$G_{\mathrm{a},N}$	Available power gain of stage N

$G_{\text{ant,RX}}$	Receiver antenna gain
$G_{\text{ant,TX}}$	Transmitter antenna gain
G_{T}	Antenna gain
I_{B}	Base current
I_{cc}	Collector current
I_{DC}	Bias current
I_{P}	Peak signal current
I_{sink}	Sink current
$\text{I}P_{\text{1dB}}$	Input-referred 1 dB compression-point
J_{c}	Collector current density
L	Inductor
λ	Wavelength
n_{f}	Number of emitter fingers
N_{ch}	Channel noise power
NF_{min}	Minimum noise-figure
NF_{RX}	Receiver noise-figure
$\text{O}P_{\text{1dB}}$	Output-referred 1 dB compression-point
$P_{\text{ant,RX}}$	Received power at the antenna interface
$P_{\text{ava,LO}}$	Available LO power
P_{dc}	DC power consumption
P_{in}	Input power
P_N	Input-referred 1 dB compression-point of stage N
P_{out}	Output power
$P_{\text{out,DoAC}}$	Output power of the doubler-amplifier chain

$P_{\text{out,max}}$	Maximum output power
$P_{\text{out,TX}}$	Transmitter output power
P_{r}, P_{R}	Received power
P_{RT}	Power of the reflected signal at target
$P_{\text{r,min}}$	Minimum detectable received power
P_{sat}	Saturated output power
P_{T}	Peak transmitter power
P_{sat}	Saturated output power
R	Object distance
R_{eq}	Parallel equivalent resistance
R_{load}	Load resistance
$R_{\text{opt,load}}$	Optimum load resistance
s	Spacing
σ	Radar cross section
S_{opt}	Optimum noise impedance
S_{t}	Power density
SNR_{i}	Input signal-to-noise-ratio
SNR_{o}	Output signal-to-noise-ratio
SNR_{req}	Required signal-to-noise-ratio
T	Temperature
V_{be}, V_{BE}	Base-emitter voltage
V_{cc}	Supply voltage
V_{ce}, V_{CE}	Collector-emitter voltage
V_{DC}	DC voltage

V_{knee}	Knee voltage
V_{max}	Maximum voltage
w	Line width
w_{total}	Total width
Z_{in}	Input impedance
Z_L	Load impedance
Z_{Line}	Line impedance
$Z_{opt,load}$	Optimum load impedance
$Z_{opt,source}$	Optimum source impedance
Z_{out}	Output impedance
Z_S	Source impedance

Constants

k_B	Boltzmann's constant: 1.38×10^{-23} J/K

1 Introduction

1.1 Millimeter Wave Systems

1.1.1 Millimeter Wave Systems in Communication Applications

In communication systems aiming for data rates exceeding 100 Gbit/s, a common target envisioned for 6G and beyond [DBM+20, Hey21], wire-line or optical links are the conventional approaches. However, the utilization of mm-wave frequencies enables wireless communication systems to achieve such high data rates as well. As emphasized by Shannon's theory, boosting the data rate requires broadening the bandwidth and improving the signal-to-noise-ratio (SNR). The adoption of high-order modulation schemes like N-quadrature amplitude modulation (QAM) proves efficient in utilizing the bandwidth, leading to additional data rate enhancement. However, the output power limitations of the transmitter and the NF performance of receivers impose constraints on the implementation of very high-order modulation schemes. Consequently, establishing high data rate links necessitates a transition to higher frequencies to exploit the vast available bandwidths. The D-band frequency range (110 – 170 GHz) is one of the potential candidates for 6G links [CEP18].

Fig. 1.1 depicts an exemplary communication link between a TRX pair across a distance, denoted as d. The achievable data rate in this system is influenced by multiple factors. One of the factors is the employed modulation scheme, which determines the required SNR and bandwidth, thereby impacting the channel noise. Additionally, the antenna gains of both the transmitting and receiving ends, the distance, path loss at the frequency of operation over the medium, transmitter output power and receiver NF all impact the system performance. The relationship among these variables is often quantified through link budget

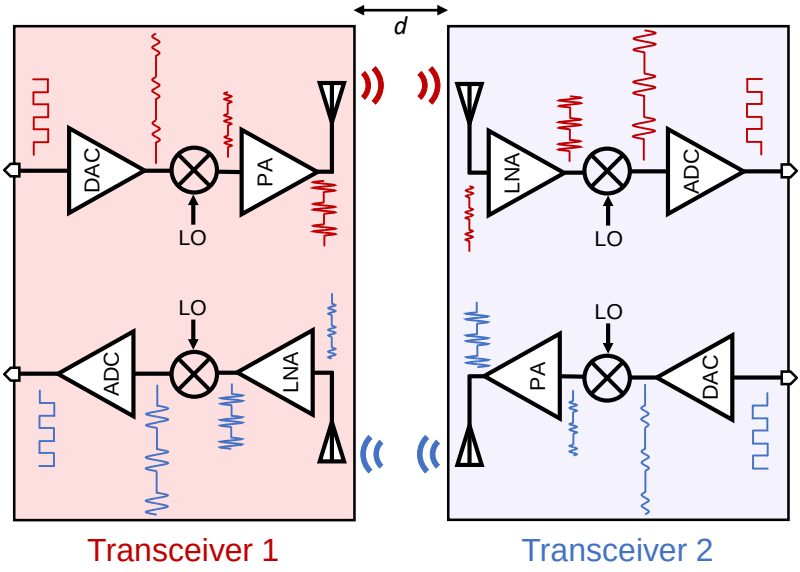


Figure 1.1: Block diagram of a typical communication system with two transceivers communicating over a certain distance.

calculations, providing a comprehensive understanding of the communication link's overall effectiveness.

First of all, the equivalent isotropic radiated power (EIRP) is a function of transmitter output power ($P_{\text{out,TX}}$) and transmitter antenna gain ($G_{\text{ant,TX}}$), as expressed in (1.1), within the logarithmic domain. The amount of attenuation that the transmitted signal experiences over the free space, referred to as free-space path loss (FSPL), depends on the frequency of the signal as well as the separation between the antennas. The FSPL can be expressed in logarithmic domain, as in (1.2) where λ is the wavelength of the transmitted signal in m, and d is the distance in m. Additionally, this expression can also be written in terms of d and frequency (f_c), where d is expressed again in m and f_c is measured in Hz. Note that FSPL formula holds true only under the far-field conditions.

$$\text{EIRP} = P_{\text{out,TX}} + G_{\text{ant,TX}} \tag{1.1}$$

$$\begin{aligned} \text{FSPL} &= 20\log\left(\frac{4\pi d}{\lambda}\right) \\ &= -147.55 + 20\log(d) + 20\log(f_{\text{c}}) \end{aligned} \tag{1.2}$$

Once the FSPL is determined, the received power at the RX antenna interface ($P_{\text{ant,RX}}$) can be expressed as shown in (1.3). Subsequently, upon accounting for the receiver antenna gain ($G_{\text{ant,RX}}$), the received power (P_{r}) takes the form illustrated in (1.4). Note that (1.3) and (1.4) are both expressed in logarithmic domain.

Fundamentally, for successful receiving, P_{r} must exceed the minimum detectable received power ($P_{\text{r,min}}$). This minimum power is determined by the channel noise power (N_{ch}), the required SNR (SNR_{req}) corresponding to a given modulation scheme and bandwidth, and the receiver's noise figure (NF_{RX}), as expressed in (1.5) in logarithmic domain. Ultimately, the link margin is obtained by subtracting $P_{\text{r,min}}$ from P_{r}, as defined in (1.6) in logarithmic domain.

$$P_{\text{ant,RX}} = P_{\text{out,TX}} + G_{\text{ant,TX}} - \text{FSPL} \tag{1.3}$$

$$P_{\text{r}} = P_{\text{out,TX}} + G_{\text{ant,TX}} - \text{FSPL} + G_{\text{ant,RX}} \tag{1.4}$$

$$P_{\text{r,min}} = N_{\text{ch}} + \text{SNR}_{\text{req}} + \text{NF}_{\text{RX}} \tag{1.5}$$

$$\begin{aligned} \text{Link Margin} &= P_{\text{r}} - P_{\text{r,min}} \\ &= (P_{\text{out,TX}} + G_{\text{ant,TX}} - \text{FSPL} + G_{\text{ant,RX}}) - (N_{\text{ch}} + \text{SNR}_{\text{req}} + \text{NF}_{\text{RX}}) \end{aligned} \tag{1.6}$$

According to (1.6), enhancements in data rate or communication range can be achieved through various ways, from the hardware point of view, as listed below.

- Higher transmitter output power.
- Higher transmitter and receiver antenna gain.
- Lower receiver noise figure.

Table 1.1 details the parameters in the communication system scenario, illustrated in Fig. 1.1, where the objective is to achieve a data rate of 100 Gbit/s with a bit error rate (BER) $< 1 \times 10^{-15}$ using a 16 QAM modulation scheme. The specified data rate of 100 Gbit/s corresponds to a symbol rate of 25 GS/s for 16 QAM. For the sake of simplicity and a conservative approach, a frequency bandwidth of 25 GHz is assumed to accommodate the symbol rate. One can also find the change in parameters if another modulation scheme, such as 8 QAM or 32 QAM is used.

Further, a $P_{\text{out,TX}}$ of 20 dBm and a NF_{RX} of 10 dB can be assumed together with $G_{\text{ant,TX}} = G_{\text{ant,RX}} = 3$ dBi. Next, the channel noise power associated with the bandwidth of 25 GHz can be calculated as shown in (1.7), where k_{B} is the Boltzmann's constant, T is temperature and B is the bandwidth. Assuming a temperature of 290 K and substituting the k_{B} and bandwidth values, N_{ch} is found to be approximately −70 dBm. Lastly, employing a 16 QAM modulation scheme and targeting a BER of $< 1 \times 10^{-15}$, requires an SNR of better than 19 dB, according to Fig. 1.2. The link margin can now be calculated based on the aforementioned assumed parameters, as also listed in Table 1.1, to be 5.6 dB.

$$N_{\text{ch}} = k_{\text{B}} T B \tag{1.7}$$

The demonstrated exemplary communication link and the relative link budget calculations prove the ability to establish a communication link with such high data rates at D-band. However, achieving the required output power at the TX and the NF at the RX are still quite challenging. The impacts of $P_{\text{out,TX}}$ and NF_{RX} on the communication range and the achievable data rate are further illustrated in Fig. 1.3.

Table 1.1: The list of parameters in the communication system scenario shown in Fig. 1.1.

Modulation Type	8 QAM	16 QAM	32 QAM
f_c (GHz)	140	140	140
Data Rate (Gbps)	100	100	100
Bandwidth (GHz)	33.3	25	20
Distance (d) (m)	0.2	0.2	0.2
$P_{\text{out,TX}}$ (dBm)	20	20	20
$G_{\text{ant,TX}}$ (dBi)	3	3	3
FSPL @ $d = 20$ cm (dB)	61.4	61.4	61.4
$G_{\text{ant,RX}}$ (dBi)	3	3	3
N_{ch} (dBm)	−68.8	−70	−71
NF_{RX} (dB)	10	10	10
$\text{SNR}_{\text{req.}}$ @ BER $= 1 \times 10^{-15}$ (dB)	18	19	22
Link Margin (dB)	5.4	5.6	3.6

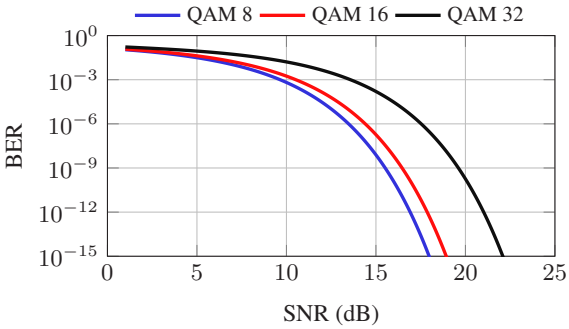


Figure 1.2: SNR vs. BER for various QAM schemes.

Fig. 1.3(a) illustrates the influence of $P_{\text{out,TX}}$ on the communication range, d, for a fixed data rate of 100 Gbit/s. The communication range is limited to sub-meter values, primarily due to the increased FSPL at the D-band frequencies. The required $P_{\text{out,TX}}$ for a target range of 20 cm is around 20 dBm and is indicated on the plot. As depicted, achieving a greater communication range with the same data rate imposes more stringent requirements on $P_{\text{out,TX}}$, assuming all other parameters remain constant. A similar trend is observed in Fig. 1.3(b), where the relationship between the data rate and $P_{\text{out,TX}}$ is illustrated at a fixed range of 20 cm.

On the RX side, Fig. 1.3(c) and Fig. 1.3(d) show the effect of NF_{RX} on the communication range and data rate. The targeted range of 20 cm and the data rate of 100 Gbit/s can be achieved with a NF_{RX} of approximately 10.6 dB. Achieving a greater communication range or a faster data rate necessitates smaller NF_{RX} values. Note that Fig. 1.3(a)–1.3(d) also take a link margin of 5 dB into account.

In order to increase the range of communication, multiple adjustments can be made to the communication scenario illustrated in Fig. 1.1. First of all, the EIRP can be improved by employing an array of transmitters. For example, implementing a transmitter array of n elements would improve the $P_{\text{out,TX}}$ by $10\log(n)$. On top of that, transmitter antenna gain, $G_{\text{ant,TX}}$, also scales by $10\log(n)$ due to the fact that the total antenna area expands by a factor of n when implemented as an array. Consequently, the overall increase in EIRP amounts to $20\log(n)$. Fig. 1.4 illustrates a communication system where each transceiver integrates an 8×8 transmitter array. Based on this configuration, EIRP is enhanced by $20\log(64) = 36$ dB compared to the EIRP exhibited at the transmitter in Fig. 1.1.

Furthermore, to extend the communication range, a more moderate data rate of 50 Gbit/s can be targeted. Assuming the same receiver performance, Table 1.1 can be updated into Table 1.2. Table 1.2 indicates that employing a modulation scheme of 16 QAM permits achieving a data rate of 50 Gbit/s within a bandwidth of 12.5 GHz. Factoring in the provided transmitter and receiver performance data, a communication span of 20 m can be attained with a link margin of 4.6 dB.

It is worth noting that high-order QAM modulations require high peak-to-average power ratio (PAPR) values in PAs, posing additional challenges in

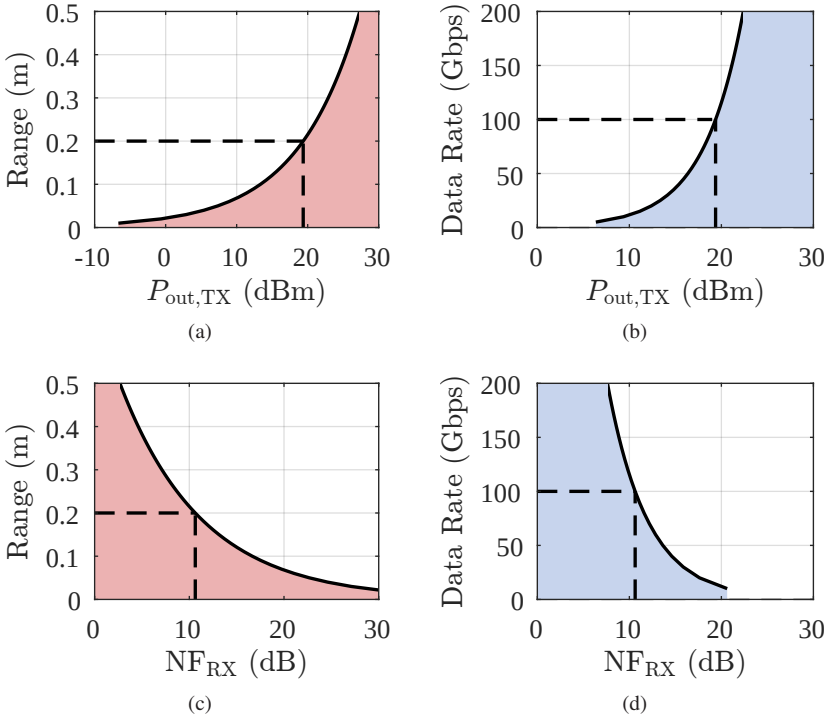


Figure 1.3: Link budget analysis for a 140 GHz with 16 QAM modulation with the targeted data rate of 100 Gbit/s over a distance of 20 cm. Assuming a link margin of 5 dB, $G_{\text{ant,TX}}$ and $G_{\text{ant,RX}}$ of 3 dBi each, and a BER of 1×10^{-15}.

terms of linearity and efficiency. Essentially, the PA has to be operated at a certain power back-off to maintain a linear operation. Therefore, the PA design in communication applications require additional linearization as well as back-off efficiency enhancement techniques [CTZ+20, DDT+19, SPD+16, WW20, WWW20].

This dissertation focuses extensively on the mm-wave PA and LNA designs, which are crucial components in communication systems, as evident from the link budget calculations. While the conventional methods for achieving the specified front-end performances often involve the utilization of III-V

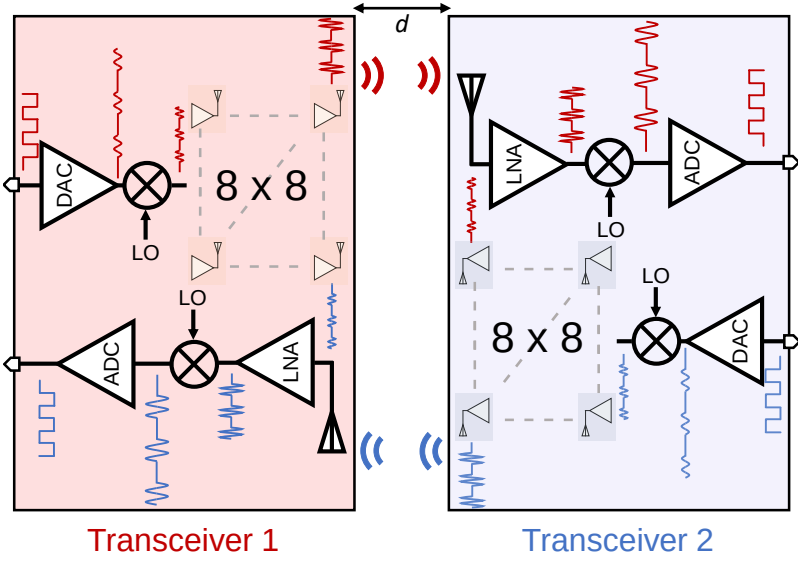


Figure 1.4: Block diagram of a communication system with two transceivers consisting of 8×8 transmitter arrays communicating over a certain distance.

technologies, this research demonstrates the viability of Si-based solutions. The Si-based solutions yield higher integration levels and more cost-effective designs when mass produced, while still meeting the necessary performance metrics. This approach aligns with the findings in the literature, where wireless transceivers operating at *D*-band frequencies and beyond have been demonstrated for communication applications [DST+23, FSCE17, HFA+18, KAS+11].

1.1.2 Millimeter Wave Systems in Radar Applications

The application of radar technology has garnered significant attention for meeting the growing need for precise sensing, involving measurements of range, velocity, and angular direction. In comparison to alternative sensing methods like infrared, ultrasonic, or camera-based approaches, radar systems offer

Table 1.2: The list of parameters in the communication system scenario shown in Fig. 1.4.

Modulation Type	8 QAM	16 QAM	32 QAM
f_c (GHz)	140	140	140
Data Rate (Gbps)	50	50	50
Bandwidth (GHz)	16.6	12.5	10
Distance (d) (m)	20	20	20
$P_{\text{out,TX}}$ (dBm)	38	38	38
$G_{\text{ant,TX}}$ (dBi)	21	21	21
FSPL @ $d = 20$ m (dB)	101.4	101.4	101.4
$G_{\text{ant,RX}}$ (dBi)	3	3	3
N_{ch} (dBm)	−68.8	−70	−71
NF_{RX} (dB)	10	10	10
$\text{SNR}_{\text{req.}}$ @ BER = 1×10^{-15} (dB)	18	19	22
Link Margin (dB)	4.4	4.6	2.6

distinct advantages. Notably, they exhibit resilience to adverse weather conditions and varying lighting, ensuring reliable operation and accuracy even in challenging environments. Furthermore, radar systems possess the ability to penetrate materials, enabling robust 3D sensing. These attributes position radar as a versatile and promising technology for applications that demand precision sensing.

One interesting application is material characterization [MMW+19, BZR18, BJPM15, TAD+23], wherein radar's fine range resolution allows identification of structures with exceptional thickness precision, even down to millimeter levels. Another well-established application that extensively employs radar systems is high-resolution imaging [HBB+22, GBRC+15, SYV+15, DSH+19, MCA17]. Additional applications leveraging radar involve tank-level measurement, motion detection, and healthcare vital sign monitoring [NSL+19, THL16, RKF+17]. Achieving such precise range resolution and facilitating high-resolution imaging in the aforementioned applications requires the development of radar systems with broad bandwidths exceeding 30 GHz to arrive at mm level resolutions.

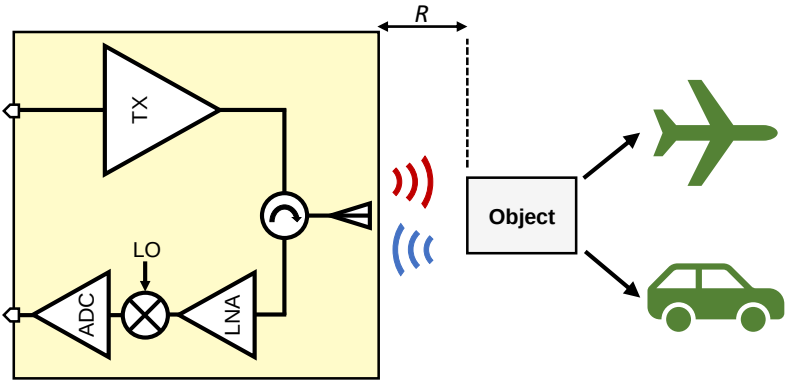


Figure 1.5: Block diagram of a typical radar system with a transceiver and an object to be detected.

As resonance-based amplifiers typically exhibit a relative bandwidth limitation of around 25 %, an operation frequency below 100 GHz promises a bandwidth of no more than 25 GHz, posing a direct limitation on the range resolution. Different methods can be employed to enhance operational bandwidth. One approach involves implementing stagger-tuning techniques, utilizing multi-stage designs, each peaking at different frequencies to achieve a flatter frequency profile. While effective in widening bandwidth, this technique reduces the design flexibility and does not address bandwidth challenges in signal generation circuits such as voltage-controlled-oscillators (VCOs) with continuous tuning capability. Alternatively, bandwidth expansion can be achieved by incorporating wideband matching networks. However, this often leads to increased losses in the matching networks, resulting in lower output powers and higher noise figures in amplifiers. Therefore, a frequency of operation centered well above 100 GHz is essential to overcome these limitations [AKE+21, EHH+20, SRK+22, HBB+22, KANK21, ZBD+21, AIW20].

Considering an exemplary radar system depicted in Fig. 1.5, the radar range equation can be formulated as follows. Assuming a peak transmitter power of P_T, the gain of the directive antenna in the desired direction, G_T, and an object distance of R, the power density, S_t, can be calculated using (1.8).

$$S_t = \frac{P_T G_T}{4\pi R^2} \tag{1.8}$$

The radar target intercepts and reflects a portion of the transmitted energy back towards the radar. The quantification of the energy emitted by the target back to the radar is assessed through the radar cross section (RCS), denoted as σ, and is contingent on various factors, including the shape, size, material, and orientation of the target objects. The power of the reflected signal at target, P_{RT} is equal to the product of power density, S_t, and the RCS, as expressed in (1.9).

$$P_{RT} = S_t \times \sigma = \left(\frac{P_T G_T}{4\pi R^2}\right) \times \sigma \tag{1.9}$$

Subsequently, to determine the power density of the reflected signal, S_r, at the radar, the power of the reflected signal at the target, P_{RT}, is divided by the surface area of the sphere with a radius of R, as formulated in (1.10).

$$S_r = \frac{P_{RT}}{4\pi R^2} = \left(\frac{P_T G_T}{4\pi R^2}\right) \times \sigma \times \left(\frac{1}{4\pi R^2}\right) \tag{1.10}$$

Multiplying the power density of the reflected signal, S_r, by the effective area of the receiving antenna, A_R, results in the received power, P_R, as illustrated in (1.11), where A_R can be expressed as in (1.12).

$$P_R = S_r A_R = \frac{P_T G_T \sigma A_R}{\left(4\pi R^2\right)^2} \tag{1.11}$$

$$A_R = \frac{G_R \lambda^2}{4\pi} \tag{1.12}$$

Substituting the expression for A_R in (1.11), the following expression can be obtained:

$$P_{\mathrm{R}} = P_{\mathrm{T}} \frac{G_{\mathrm{T}} G_{\mathrm{R}} \lambda^2}{(4\pi)^3 R^4} \sigma \tag{1.13}$$

Finally, for a given radar type, defining the $P_{\mathrm{r,min}}$ as the minimum detectable received power for a given SNR, an expression can be derived for R, as in (1.14).

$$R_{\mathrm{max.}} = \sqrt[4]{P_{\mathrm{T}} \frac{G_{\mathrm{T}} G_{\mathrm{R}} \lambda^2}{(4\pi)^3 P_{\mathrm{r,min}}} \sigma} \tag{1.14}$$

As indicated by (1.14), improvements in the maximum achievable range of the radar can be realized through the following hardware-related approaches, as listed below.

- Increased transmitter output power.
- Increased transmitter and receiver antenna gain.
- Reduced receiver noise figure.

Note the similarities to the conclusions drawn based on (1.6), reaffirming the importance of mm-wave PA and LNA designs.

It is worth noting that since it is not possible to measure the range of the targets with the unmodulated continuous-wave signals, the radar systems commonly employ specific modulation types such as frequency modulated continuous-wave (FMCW) or phase modulated continuous-wave (PMCW). While there are further considerations influencing the final performance of these radar systems, this dissertation remains focused to examining the front-end performances of such systems.

1.2 Silicon Technologies for Millimeter Wave Systems

The modern age of continuous technology advancements is particularly driven by the semiconductor industry. The transistor stands out as a crucial player, paving the way for further inventions. Si has emerged as the predominant element in semiconductor manufacturing, because of the reasons, as listed in [CN02]:

- Si is abundantly available, non-toxic and can be purified to achieve low background impurity concentrations, less than 1 part in 10^{12} (0.000001 ppm), making it one of the purest materials on Earth.
- Si crystals can be grown in large, nearly defect-free single crystals, with current worldwide production utilizing 300 mm diameter wafers. The substantial size of the resulting silicon wafer directly correlates with an increased number of ICs per wafer, ultimately reducing the cost per IC.
- An exceptionally high-quality dielectric can be grown on Si by exposing the wafer surface to flowing oxygen at a high enough temperature. This dielectric, silicon dioxide, stands out as one of nature's most flawless insulators. It serves versatile purposes, including electrical isolation, surface passivation, a planarization layer, an etch stop, or as an active layer (e.g., gate oxide) in the device.

In the context of mm-wave wireless systems, producing faster devices, with higher unity current gain cut-off frequency (f_T) and maximum frequency of oscillation (f_{MAX}) values is driven by the growing demand for increased data rates in communication and the need for more precise sensing in radar technologies. Despite the distinct advantages outlined in this section, Si is still far from being an ideal semiconductor. Si has a lossy substrate and in contrast to III-V technologies, it exhibits smaller carrier mobility for both electrons and holes. Since the speed of a device is proportional to how fast the carriers can traverse the device, Si is often considered a somewhat "slow" semiconductor. Meanwhile, although having faster carrier mobilities, III-V technologies suffer from lower levels of integration and lower yield, leading to higher cost solutions for mass production. Therefore, for larger volumes of production,

Si-based technologies persist as the mainstream, and will continue to dominate IC design.

SiGe heterojunction bipolar transistors (HBTs) present a compromise, as SiGe exhibits improved RF performances compared to pure Si while offering higher level of integration, higher yield and lower cost compared to III-V. Especially with the birth of SiGe BiCMOS, the superior RF performance of the SiGe over complementary metal-oxide semiconductor (CMOS) can be integrated with the strength of Si CMOS regarding the low-power logic and memory density, forming a single cost-effective process that can do "more". Although not being up-to-date, [CN02] includes the historic evolution of SiGe HBTs over time until early 2000s, demonstrating the improvement in f_T & f_{MAX} and providing an understanding of the historical background.

The superiority of SiGe HBTs compared to Si homojunction bipolar transistors (BJTs) stem from device physics. Primarily, the key parameters affecting the RF performance of the BJT are the base transit time, determining intrinsic transistor speed, base resistance impacting f_{MAX}, and current gain. Improving RF performance requires attention to certain design parameters during the base design phase. For instance, a transistor with high f_T & f_{MAX} necessitates a thin, highly doped base layer. However, increasing base doping concentration may reduce current gain if the emitter doping concentration is not proportionally adjusted. Additionally, increased doping concentration in the base leads to band gap narrowing in the emitter limiting the emitter doping. This decrease in the emitter's band gap elevates intrinsic carrier concentration, subsequently reducing current gain. Consequently, significantly increasing base doping while maintaining high current gain proves challenging. Hence, thin-base microwave bipolar transistors encounter issues with relatively high base resistances. A viable solution involves fabricating the emitter from a material possessing a larger band gap than the base layer. Ultimately, HBTs feature higher base doping concentrations, providing several advantages:

- Base thickness can be substantially decreased while maintaining acceptable base resistances.
- With constant base thickness, base resistance can be significantly reduced, resulting in higher f_{MAX} and minimal microwave noise.

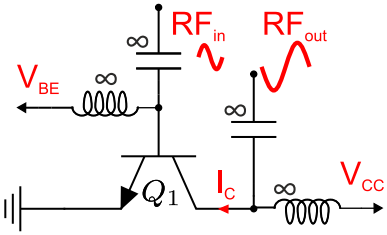


Figure 1.6: A common emitter amplifier with DC block capacitances and RF choke inductances.

The further details on device physics behind SiGe HBTs can be found in [CN02, Yan88, Sch08].

This section presents a brief comparison of two 0.13 µm SiGe BiCMOS technologies adopted in the ICs demonstrated in this dissertation, namely SG13G2 and SG13G3 processes from Leibniz Institute for High Performance Microelectronics (IHP). Fig. 1.6 shows the single HBT device in the common emiter (CE) configuration, while Fig. 1.7 depicts the simulated f_T, f_{MAX}, and maximum available gain (MAG) under varying bias conditions for this configuration.

Fig. 1.7(a) and Fig. 1.7(b) show how f_T & f_{MAX} change with respect to collector current density, J_c, in both technologies, highlighting an optimum current density that maximizes f_T & f_{MAX}. Moreover, Fig. 1.7(c) and Fig. 1.7(d) illustrate the impact of V_{CE} on f_T & f_{MAX} when the collector current density is set to 3 mA per finger. Lastly, MAG is plotted against collector current density at 140 GHz, as shown in Fig. 1.7(e) and Fig. 1.7(f). With the CE topology, the SG13G3 technology offers an MAG improvement of 1.5 dB at 140 GHz compared to SG13G2.

This analysis helps in understanding the capability of the adopted technologies and provide a numerical background for the improvements observed when switching from SG13G2 to SG13G3. The further analysis on noise comparison of the processes is illustrated in Section 3.3.1.

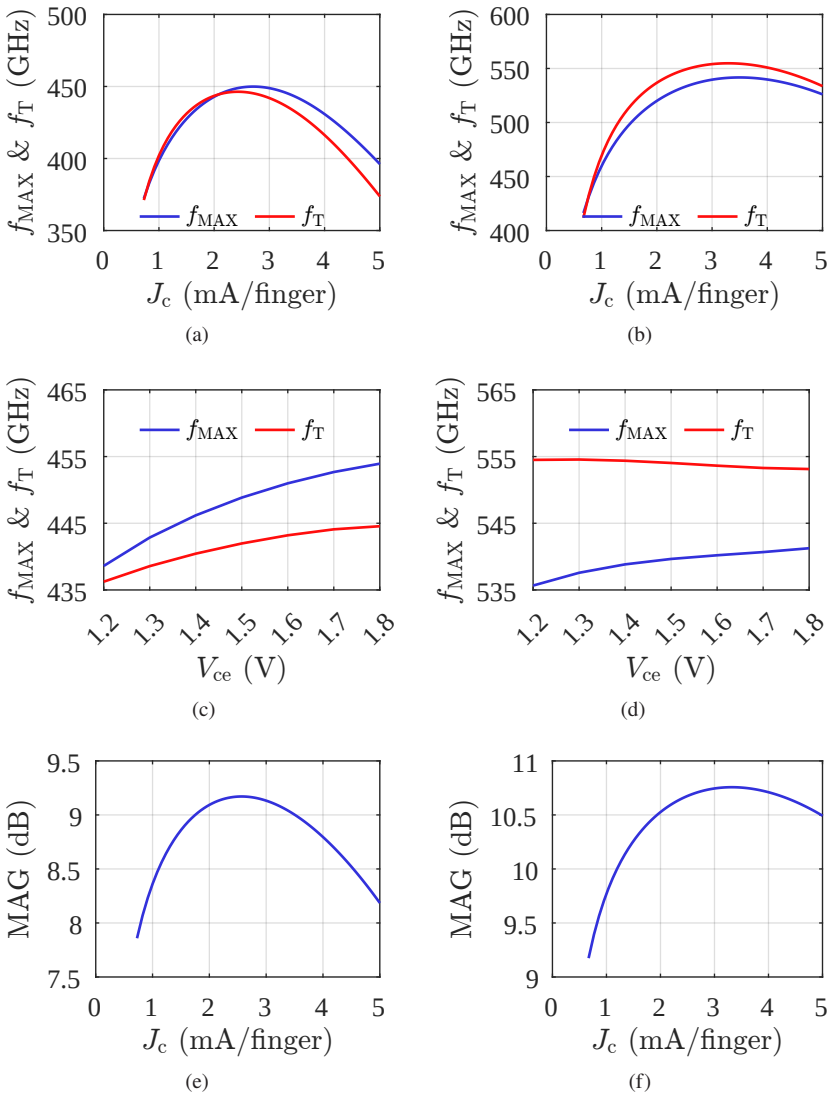


Figure 1.7: Simulated HBT performance in CE configuration (a) f_T and f_{MAX} vs. J_c at V_{ce} = 1.5 V in SG13G2. (b) f_T and f_{MAX} vs. J_c at V_{ce} = 1.5 V in SG13G3. (c) f_T and f_{MAX} vs. V_{ce} at J_c = 3 mA per finger in SG13G2. (d) f_T and f_{MAX} vs. V_{ce} at J_c = 3 mA per finger in SG13G3. (e) MAG vs. J_c in SG13G2 at 140 GHz. (f) MAG vs. J_c in SG13G3 at 140 GHz.

1.3 Thesis Organization and Goals

This thesis presents and discusses the design and analysis of high-power amplifiers, low-noise amplifiers, and an integrated transceiver comprising various sub-blocks, all operating in the *D*-band frequency range.

Chapter 2 explores the design of *D*-band PAs using SiGe BiCMOS technologies. It investigates the constraints on achievable output power imposed by technology-related limitations and presents power combining techniques to boost the output power. A systematic design strategy is introduced, along with three unit PAs and two power-combined PA designs that achieve SoA performances. At the end of the chapter, a comprehensive list of PAs operating above 100 GHz is provided, and performance comparisons are made to the developed PAs.

Chapter 3 briefly examines the main noise sources in high-frequency HBTs and investigates two different LNAs implemented in SiGe BiCMOS technologies. A noise reduction technique is demonstrated to minimize the noise contribution of common base (CB) devices in cascode amplifiers. Moreover, a gain boosting technique is implemented to enhance the limited gain attainable at *D*-band frequencies. The impact of the change in the technology (SG13G2 to SG13G3) on the LNA performance is illustrated. A comprehensive comparison to SoA is given at the end of the chapter.

Chapter 4 details the development of a highly integrated, fully differential *D*-band I/Q transceiver. The design employs a mixer-first architecture to mitigate the TX to RX spillover issue commonly observed in monostatic transceivers by eliminating the LNA. The chapter provides comprehensive descriptions of each sub-block, including the hybrid coupler, power divider, upconversion and downconversion mixers, driver amplifier, power amplifier, and frequency doubler. Detailed characterization results are also presented.

The final chapter, Chapter 5, summarizes the key findings and conclusions of this thesis.

2 High-Power SiGe Amplifiers at D-Band

2.1 Introduction

The transmitter performance in aforementioned communication and radar systems is quite critical. This significance is particularly pronounced at *D*-band frequencies, where increased FSPL demands the generation of high-power levels, imposing rigorous criteria on PA design. Beyond that, additional challenges inherent in PA design are as follows. Ensuring both efficient and linear PA operation is crucial, especially considering that PA power consumption often dominates overall power usage in many systems. At a given linearity constraint, a PA with less efficiency would necessitate a larger DC power consumption, potentially resulting in increased heat generation within the IC and subsequent thermal issues. These challenges assume even more relevance within the context of the *D*-band due to the proximity of the operating frequency to the limits of the adopted technologies.

The choice of technology plays a pivotal role in mm-wave PA design. In this regard, the ascendancy of III-V compound technologies becomes evident due to their superior power density (mW / mm^2) characteristics. Among these, gallium nitride (GaN) high electron mobility transistors (HEMTs) stand out as exemplars, exhibiting larger breakdown voltages, thus higher power densities [MKM+14, CSBE18, GUR19, CQP+20]. Nevertheless, it is crucial to recognize the associated limitations of these compound technologies, which involve challenges related to integration levels and cost implications.

In contrast, emerging advanced Si-based technologies with higher f_T and f_{MAX} facilitate the realization of designs that operate at higher frequencies, enabling superior integration levels. This approach offers a cost-effective solution, particularly suitable for mass production. However, it is important to address

the inherent constraint posed by reduced breakdown voltages, a factor that restricts achievable output power. The trade-off between f_T and breakdown voltage is known as the Johnson's limit [Joh65], stating that there is an inverse proportionality between the f_T performance and breakdown voltage of active devices. Therefore, continuous increase in f_T and f_{MAX} does not necessarily translate into higher output power levels in mm-wave PAs. Another drawback is the reduced MAG due to operating frequencies at D-band being closer to f_T and f_{MAX} of even the most advanced Si-based technologies.

The most obvious strategy to increase the output power of the PAs implemented in technologies with limited breakdown voltages is to increase the current flowing through the output stage devices. Assuming a fixed collector current density, this requires output stage transistors with larger dimensions. Enlarging the device size gives rise to intricate RF routing of device terminals, introducing higher interconnect parasitics, and eventually resulting in reduced power gain, efficiency and a consequent reduction in the returns derived from enlarging the device dimensions.

A straightforward approach to enhance the output power of the PAs realized in technologies with limited breakdown voltages is to increase the current flowing through the output stage transistors. However, for a constant collector current density, this necessitates the implementation of larger output stage devices. Enlarging the device sizes concurrently introduces challenges associated with more complicated RF routing and these challenges manifest as increased parasitic elements at the interconnects, ultimately leading to a degradation in power gain and efficiency. Furthermore, as the device sizes increase, the optimum load impedance ($Z_{opt,load}$) that must be presented to the output transistors reduces, requiring matching networks with larger impedance transformation ratios. However, these matching networks are associated with increased losses, leading to a decline in overall efficiency.

There exist numerous Si-based PAs presented in the literature at D-band [LCL+22a, LCL+22b, LCW+22, KEKM21b, LR21, PRM21, RC21, TNM+21b, PR20, AYG+20, CQP+20, SCE20, ZCY+20, KNK19, VVT+19, DB18, SR18, SLK+18, FAHS17, KBW+17, AFAS16, SJK+16, DB15] which report output powers up to 22 dBm with a PAE of 12.5 %. A substantial portion of the existing literature relies on the utilization of multi-stage cascaded PAs to address the issue of reduced MAG in the D-band. This results in raised power consumption, and a subsequent decrease in efficiency.

Furthermore, as a response to the limitations posed by the constrained output power at *D*-band, a diverse range of on-chip power combining methodologies has been implemented to boost the generated power [DB18, AYG+20, KNK19, LR14, LCL+22a, LCL+22b]. It is worth noting that power combining techniques introduce additional network losses and typically demand a significant amount of IC area. However, as the frequency of operation increases, the area of these power combiners decreases. This trend becomes particularly pronounced at *D*-band frequencies, enabling the design of compact power combiners that, through further techniques as will be explained in Section 2.3.1 and Section 2.4.1, can attain minimal losses.

2.1.1 Amplifier Topologies

A major focus in designing mm-wave PAs involves analysis of saturated output power (P_{sat}), PAE, and gain. There are two mainly employed topologies for SiGe PAs: one is the CE configuration, while the other employs an alternative approach known as the cascode topology.

Given that the output voltage headroom in the CE topology, as shown in Fig. 2.1(a), is constrained by open-base collector-emitter breakdown voltage (BV_{CEO}), achieving higher power levels predominantly relies on increased current flow by enlarging the size of the output transistors.

For the CE amplifier topology depicted in Fig. 2.1(a), the limited output voltage headroom imposed by the open-base collector-emitter breakdown voltage (BV_{CEO}) necessitates larger current to achieve higher power levels, which requires larger output transistors for a fixed current density. However, as the transistor dimensions expand, the $Z_{\text{opt,load}}$ reduces notably, necessitating a larger impedance transformation and a correspondingly intricate matching network. Consequently, the increased complexity of the output matching network introduces losses that counterbalance the performance gains derived from the larger device size, ultimately leading to a pronounced decline in overall performance, specifically PAE.

In contrast, the cascode topology, as illustrated in Fig. 2.1(b), circumvents these limitations by offering an elevated voltage headroom, surpassing the constraints imposed by BV_{CEO}. This is achieved through the utilization of a low impedance (AC ground) positioned at the base of the CB device, effectively

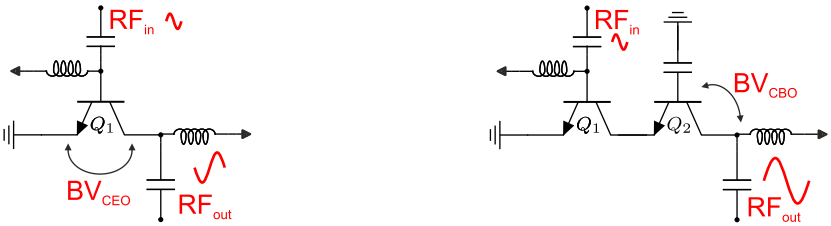


Figure 2.1: Schematic drawings of a (a) CE amplifier. (b) Cascode amplifier.

averting voltage build-up. When the base of the HBT device is shorted, the breakdown mechanism is limited by the collector-base breakdown voltage (BV_{CBO}), 4.8 V, of the CB device which is much higher than BV_{CEO}, 1.6 V, i.e. in IHP's SG13G2 technology. This distinctive attribute empowers SiGe HBT cascode PAs to manage more extensive collector voltage swings without triggering concerns related to reliability [ORW+15].

Additionally, the cascode topology offers higher MAG compared to the CE topology. This is due to the fact that the real part of the output impedance of the cascode amplifier is enhanced by a factor of $g_m r_o$ compared to the real part of the output impedance of CE topology, where g_m is the transconductance and r_o is the real part of the output impedance. The comparison of MAG vs. frequency in CE and cascode topologies at D-band is illustrated in Fig. 2.2. As can be seen, a difference of around 10 dB is observed between CE and cascode topologies at the center frequency of 140 GHz. Apart from the advantages in elevated breakdown voltages as well as the higher MAG, the cascode topology is also more favorable in terms of the bandwidth due to the reduced Miller effect as the CE device in the cascode amplifier has a voltage gain of 1, limiting the enhancement in C_{bc}. Cascode topology also has an improved input-output isolation, proving to be beneficial at D-band frequencies due to the stability concerns. Further analysis and advantages associated with the cascode architecture can be found in [SS04].

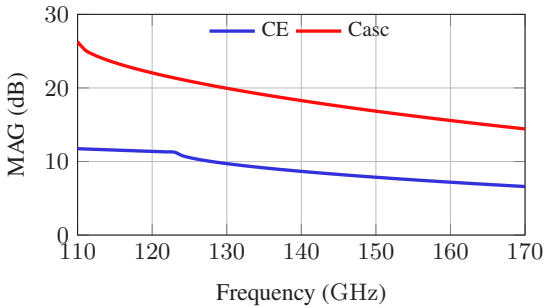


Figure 2.2: Comparison of peak MAG between CE and cascode topologies vs. frequency.

2.1.2 Classes of Operation

Beyond amplifier configuration, another crucial parameter in PA design is the class of operation. There are two main classifications:

1. Operating Point-Based Classes:
    - Class A: Transistor conducts throughout the entire cycle with the conduction angle (α) of 360°. High linearity and low efficiency.
    - Class AB: Partial conduction ($180° \leq \alpha < 360°$). Balanced linearity and efficiency.
    - Class B: Conduction for half the cycle ($\alpha = 180°$). High efficiency and significant distortion.
    - Class C: Conduction for less than half the cycle ($\alpha < 180°$). Very high efficiency, unsuitable for linear amplification.
2. Harmonic Termination-Based Classes:
    - Class E: Utilizes specific harmonic termination to minimize current and voltage waveforms to achieve high efficiency.
    - Class F: Similar to Class E but with optimized harmonic termination for even higher efficiency.

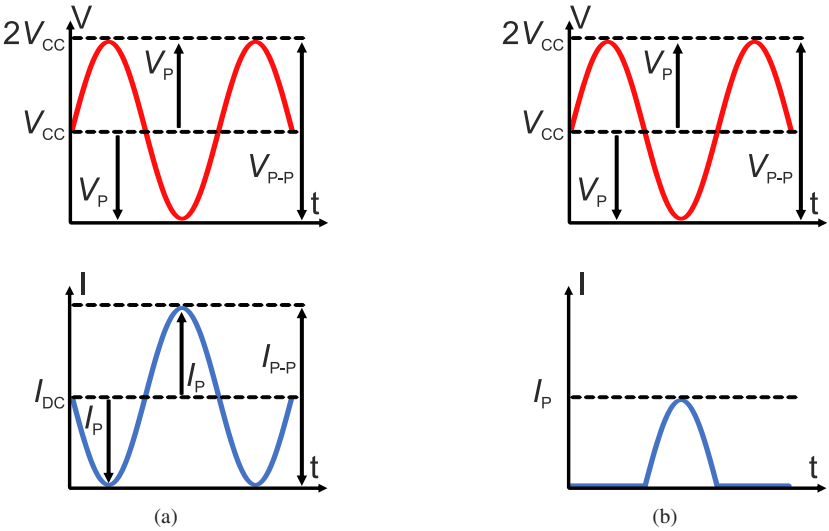


Figure 2.3: Current and voltage waveforms in (a) Class A operation. (b) Class B operation.

In class A operation, the transistor conducts through the entire signal cycle. Fig. 2.3(a) illustrates the voltage and current swings for class A operation. As can be seen, the bias current (I_{DC}) is equal to the peak signal current (I_P). When $I_{DC} > I_P$ is ensured, the device does not turn off at any point during the operation, leading to a conduction angle of 360° ($\alpha = 360°$). Referring to the waveforms depicted in Fig. 2.3(a), the output power is expressed by (2.1), where R_{load} stands for load resistance. Then, the corresponding DC power consumption (P_{dc}) can be calculated using (2.2). Finally, the theoretical collector efficiency (η) is described by (2.3). Note that the peak efficiency is obtained when the output swing reaches all the way from 0 V to $2 \times V_{DC}$.

The current and voltage waveforms in class B operation are shown in Fig. 2.3(b). The conduction angle is limited to $\alpha = 180°$, meaning that the transistor conducts only at the half signal cycle. This can be ensured by choosing an I_{DC} close to 0 A. Repeating the calculations for class A operation, it can be found that class B operation ensures a peak theoretical efficiency of 79% [Raz11].

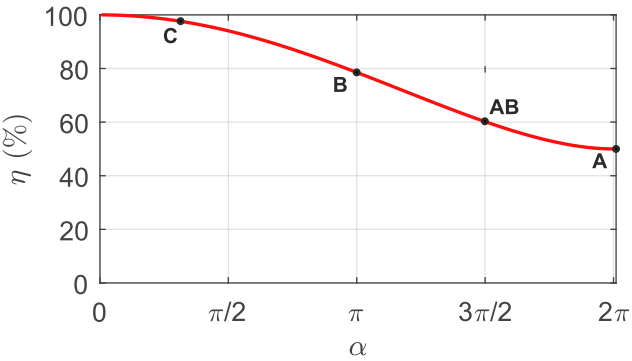


Figure 2.4: Theoretical collector efficiency vs. conduction angle.

$$P_{\text{out}} = \frac{1}{2\pi R_{\text{load}}} \int_{-\pi}^{\pi} V_{\text{P}}^2 \cos^2(\theta) d\theta \tag{2.1}$$

$$P_{\text{dc}} = \frac{V_{\text{P}}^2}{R_{\text{load}}} \tag{2.2}$$

$$\eta = \frac{P_{\text{out}}}{P_{\text{dc}}} = 50\% \tag{2.3}$$

Class AB operation assumes a conduction angle of $180° \leq \alpha < 360°$ while the class C operation has a conduction angle of less than 180°. A general expression governing the theoretical collector efficiency based on the conduction angle can be expressed as in (2.4), as derived in [Raz11]. Fig. 2.4 illustrates the change in theoretical collector efficiency with respect to the conduction angle with the marked points corresponding to the operating point-based classes of operations.

$$\eta = \frac{\alpha - \sin(\alpha)}{4\left(\sin(\frac{\alpha}{2}) - \frac{\alpha}{2}\cos(\frac{\alpha}{2})\right)} \tag{2.4}$$

Fig. 2.5(a) illustrates the relationship between collector current and base-emitter voltage in an HBT CE amplifier, as shown in Fig. 1.6. This characteristic curve plays a crucial role in determining the class of operation for the amplifier. In other words, by adjusting the base-emitter voltage, which controls the base current, the operational class of the HBT amplifier can be set.

The DC current-voltage (I-V) characteristics curve and load lines are depicted in Fig. 2.5(b) for the circuit shown in Fig. 1.6. While choosing the output termination for PAs, performing a small-signal conjugate matching at the amplifier output ensures a maximum power transfer at the small-signal region, represented by the black load line in the figure. However, this approach limits the current swings, ultimately reducing the achievable output power.

To maximize the generated output power, a load line that allows for larger voltage and current swings can be selected. This concept is illustrated by the blue load line in Fig. 2.5(b). By pushing the voltage swing to its limits (between the knee voltage (V_{knee}) and breakdown voltage (V_{max})), and maximizing the current swing, the maximum possible output power, denoted as $P_{\text{out,max}}$, can be achieved. This optimum load resistance (R_{opt}), represented by the blue curve, can be calculated using (2.5).

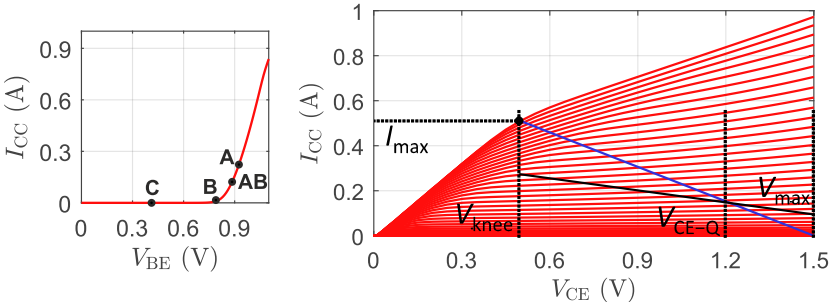
$$R_{\text{opt}} = \frac{V_{\text{max}} - V_{\text{knee}}}{I_{\text{max}}} \tag{2.5}$$

Furthermore, the expression for $P_{\text{out,max}}$ is given in (2.6).

$$P_{\text{out,max}} = (V_{\text{max}} - V_{\text{knee}}) \times I_{\text{max}} \tag{2.6}$$

Although the load-line method provides insights into the fundamentals of PA design in terms of the voltage and current waveforms, it still does not fully reveal the dynamic behavior due to the RF swings that are dependent on the RF input power. Therefore, load-pull simulations are required to more accurately determine the optimum load impedance (including both real and imaginary impedances, on the contrary to load-line method that only considers the load resistance) to maximize the output power.

Class A, B, and C operations primarily address the operating points of the transistor without considering the harmonic content, whereas class E and F



(a) (b)

Figure 2.5: Representations of (a) V_{BE} vs. I_{CC} curve. (b) DC I-V curve and load lines.

operations focus on harmonic terminations, treating transistors as switches. In class E operation, the device is treated as a non-ideal switch and the load condition is optimized to maximize efficiency by minimizing the overlap of current and voltage waveforms [SS75]. Class F operation employs stringent terminations for the harmonics of the device, such as an open circuit for even harmonics and a short circuit for odd harmonics [Raz11].

The typical design flow for mm-wave PAs is depicted in Fig. 2.6. The process begins with transistor sizing based on the desired output power. Next, the class of operation for the active devices is chosen based on requirements for linearity and efficiency. Following this, load pull and source pull simulations are conducted to determine $Z_{opt,load}$ and $Z_{opt,source}$. These load and source pull optimizations can aim for maximum P_{out}, maximum PAE, or a balance between the two. Subsequently, presenting $Z_{opt,load}$ and $Z_{opt,source}$ ideally on the schematic level provides insight into achievable P_{out}, PAE, and linearity metrics. If the results align with targeted values, the design proceeds to the layout of the PA core; otherwise, transistor sizing and bias conditions are adjusted. During PA core layout, minimizing metal and via losses is paramount to preserve output power, gain, and PAE. To address this, wider metal tracks and larger via arrays may be employed, while accounting for shunt parasitic capacitances to the substrate. Additionally, increasing the distance between input and output connections reduces coupling, enhancing stability

and bandwidth. Finally, electromagnetic (EM) simulations are conducted to assess PA core performance.

Once a PA core with the desired performance is attained, the design progresses to the creation of matching networks with the objective of minimizing losses within them. Following EM simulations of the matching networks and assessment of losses, the design may proceed with comprehensive EM modeling, involving both the PA core and the matching networks. If losses are significant, possibly due to extensive impedance transformations within the matching network, resizing of the transistors may be considered to reduce the impedance transformation ratio and thereby achieve matching networks with lower losses. Ultimately, the design is finalized after evaluating the complete EM modeling of the PA core and matching networks, as well as DC routings.

This chapter covers the design, implementation and characterization of three unit PAs and two power-combined PAs operating at *D*-band frequencies. The following sections, Section 2.2 and Section 2.3, include PAs implemented in 0.13 µm SiGe BiCMOS technology that features f_T/f_{MAX} of 300/500 GHz. Section 2.4 discusses PAs implemented in a new generation 0.13 µm SiGe BiCMOS technology with f_T/f_{MAX} of 470/650 GHz. Section 2.5 summarizes the chapter and includes a comprehensive comparison to the SoA PAs operating above 100 GHz.

2.2 A D-Band Power Amplifier with 15 dBm Saturated Output Power

This section includes content and material previously published in [10].

This section describes a *D*-band unit PA, without any power combining, implemented in a 0.13 µm SiGe BiCMOS technology that features f_T/f_{MAX} of 300/500 GHz. The aim of this design is to discover the capabilities of the adopted technology in the context of mm-wave PA design. Furthermore, it also serves as a guideline and reference point for future designs.

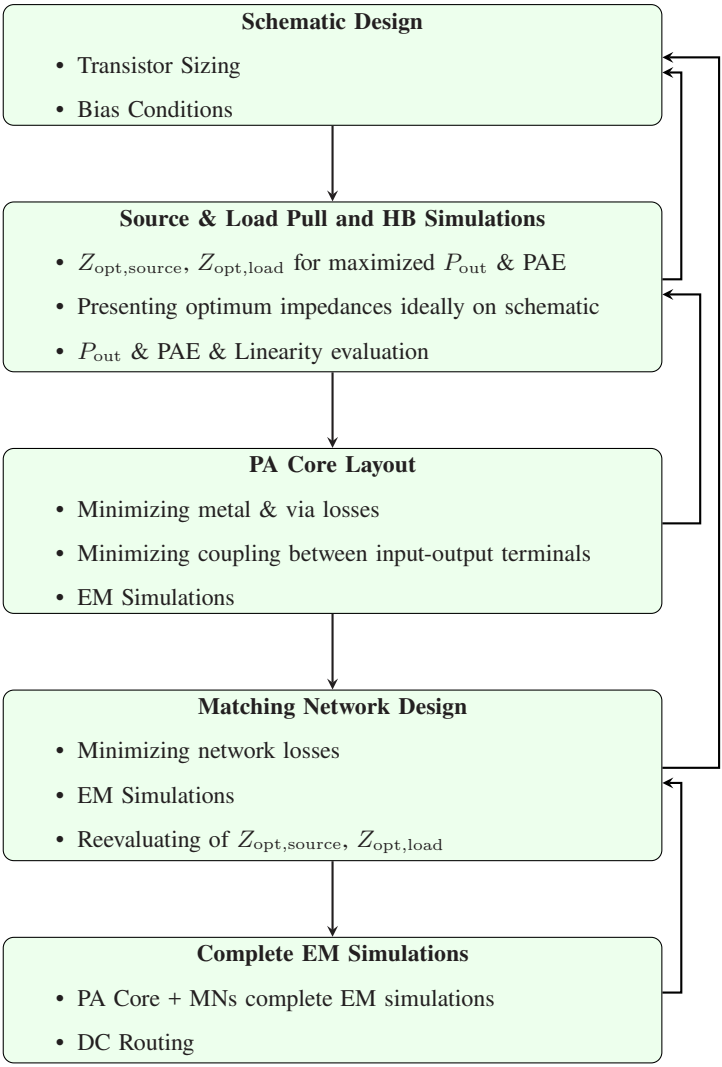


Figure 2.6: Design flow in mm-wave PA design.

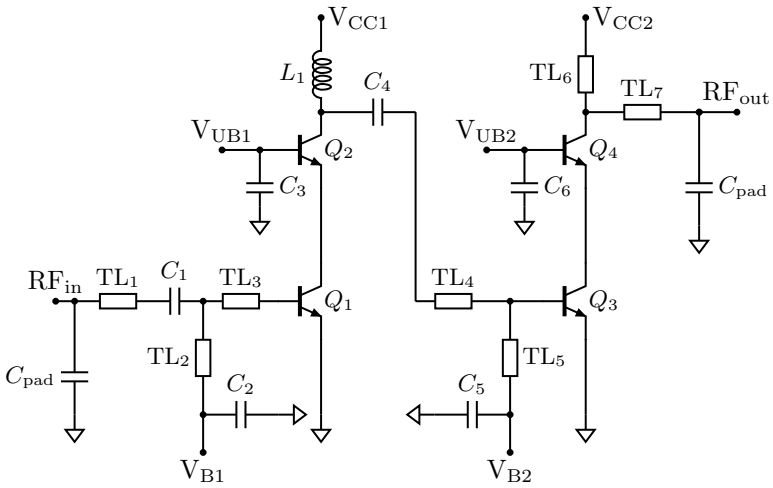


Figure 2.7: Simplified circuit schematic of the two-stage PA. [10] © IEEE

2.2.1 Design and Analysis

The proposed PA adopts the cascode topology, mainly due to the advantages mentioned in the previous section. The simplified circuit diagram of the PA is shown in Fig. 2.7 and the component values are given in Table 2.1.

An investigation on varying device sizes reveals that progressively enlarging the size of the transistors yields diminishing returns in terms of P_{sat} enhancement and leads to a decline in PAE. Fig. 2.8 illustrates the changes in P_{sat} and PAE based on different device sizes. Ideal schematic simulations indicate that doubling the device size results in an additional 3 dB of P_{sat} while maintaining a comparable PAE. However, the benefits of doubling the device size diminish upon core layout, where the active devices are laid out from the device terminals up to the metal layers to be connected to the matching networks, and subsequent EM simulations due to interconnect-related losses. Note that, as a convention throughout this dissertation, P_{sat} is defined as the output power when the gain is compressed by 4 dB.

Table 2.1: Values of the schematic components [10] © IEEE.

TL_1	72 µm, 50 Ω	TL_6	35 µm, 50 Ω	C_2	9 pF	V_{CC1}	3.5 V
TL_2	44 µm, 50 Ω	TL_7	70 µm, 50 Ω	C_3	9.4 pF	I_{CC1}	16.8 mA
TL_3	40 µm, 50 Ω	L_1	250 pH	C_4	350 fF	V_{CC2}	4.2 V
TL_4	40 µm, 50 Ω	C_{pad}	17 fF	C_5	9 pF	I_{CC1}	35.6 mA
TL_5	60 µm, 50 Ω	C_1	120 fF	C_6	9.4 pF	$Q_{1,2,3,4}$	× 20

While schematic-level comparisons offer valuable insights into the power generation capabilities of PA cores with different device sizes, it is equally imperative to perform layout-level comparisons to account for the layout-associated parasitics stemming from interconnects to device terminals. In the current design, a target P_{sat} of 15 dBm is set, necessitating the PA core to generate an output power above 15 dBm to compensate for the losses later incurred by the output matching network. A device size of $20 \times 0.07 \times 0.9\,\mu m^2$ (comprising the number of emitter fingers, effective emitter length, and width) is selected since further increasing the device size would result in significantly reduced PAE, as shown in Fig. 2.8. The output stage devices are biased in the class A regime at a current density of 1.78 mA per finger to improve the gain of the output stage, crucial for achieving higher output power levels. Additionally, the supply voltage of the output stage (V_{CC2} in Fig. 2.7) is increased to 4.2 V, providing nearly 3 V for the V_{CE} of the cascode amplifier's CB device. This expanded voltage headroom, combined with the enhanced gain from class A operation, enables a larger output voltage swing, thus contributing to increased output power.

The design of the PA core includes the device layouts and the network of connections extending from the lower metal layer device terminals to higher metal layers for interfacing with the matching network components. Accurate EM modeling of the core assumes vital significance in the context of mm-wave PAs, as it factors in considerations such as device dimensions, optimal load and source impedances, layout intricacy, and stability.

The technology stack-up of the adopted process is shown in Fig. 2.9(a). The BEOL includes seven aluminum (Al)-based metal layers where the two topmost ones are thicker and provide lower losses. The general strategy is to use

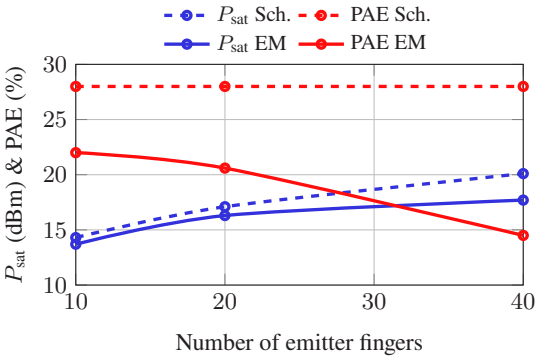
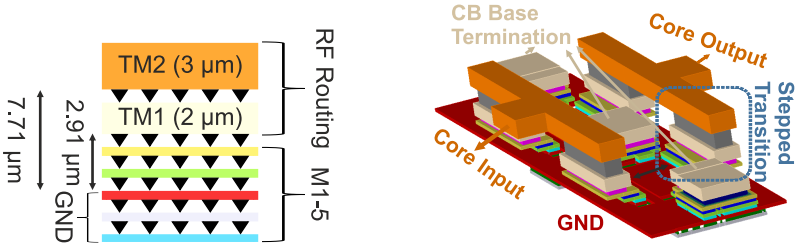


Figure 2.8: Simulated P_{sat} and PAE vs. device size for the schematic level and EM modelled PA core. [10] © IEEE

the two top-most metals for RF routing, and the metals M_1, M_2, and M_3 are stacked together and employed as the ground (GND) plane for reduced GND resistance.

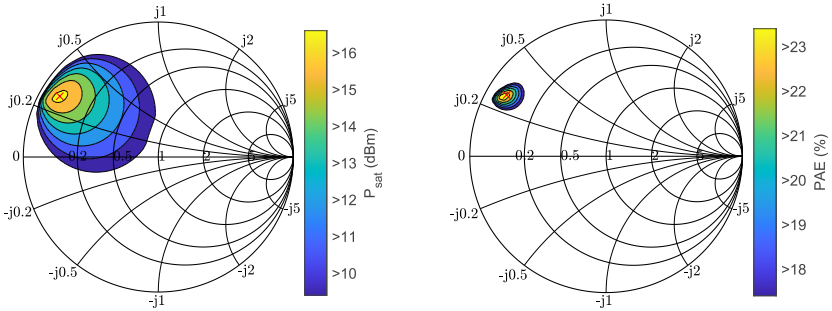
The 3D view of the PA core is presented in Fig. 2.9(b). From a layout perspective, the primary objective centers on minimizing contact losses within the metals and vias while concurrently mitigating parasitic coupling between device terminals, particularly between each input and output. Clear interfaces have been created at the top-most metal layer to connect to the matching networks. To address parasitic coupling concerns, a stairway-based layout approach is adopted, aiming to minimize parasitic coupling between the input/output (I/O) terminals of each device and to reduce parasitic capacitances. In the context of the cascode topology, particular attention is devoted to the base node of the cascode transistors (Q_2 & Q_4), which is a known source of instability at mm-wave frequencies. A careful analysis of capacitive base termination for the CB device is conducted, and this termination is accomplished through substantial AC ground capacitors positioned in the closest proximity to the base terminal to prevent instability.

Subsequent load-pull simulations are executed on the EM-simulated core to obtain the $Z_{opt,load}$ and the attainable P_{sat}. The load-pull contours for P_{sat} and PAE are shown in Fig. 2.10(a) and Fig. 2.10(b). The simulations yield an observed P_{sat} of approximately 16.3 dBm and a PAE of 23 % when a load



(a) (b)

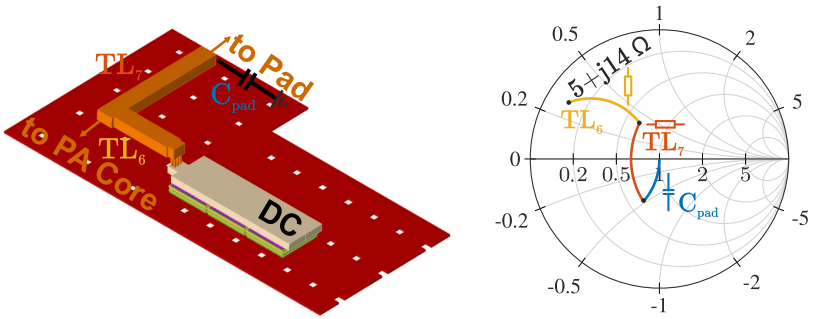
Figure 2.9: (a) SG13G2 technology stack-up. (b) 3D view of the PA core. [10] © IEEE



(a) (b)

Figure 2.10: Simulated load-pull contours for the EM modelled PA core at 140 GHz (a) P_{sat}. (b) PAE.

impedance of 5 + j14 Ω is presented to the PA core's output. This impedance value translates to a parallel equivalent resistance (R_{eq}) of roughly 45 Ω, necessitating a minimal impedance transformation and thereby minimized matching network losses. While a straightforward single-element matching network, realized through a shunt line, could suffice for matching purposes, the influence of pad capacitance (around 17 fF) is considered and integrated into the matching network alongside a series line as shown in Fig. 2.11(a). The impedance transformation through this network is displayed on Smith Chart in Fig. 2.11(b).



(a) (b)

Figure 2.11: Illustration of (a) 3D view of the output matching network. (b) Corresponding impedance transformation through the output matching network. [10] © IEEE

2.2.2 EM Modeling

During the EM modeling of the PA, two primary approaches have been pursued. The first approach involves dividing the PA into sub-blocks, including the input matching network, input stage PA core, inter-stage matching network, output stage PA core, and the output matching network. This EM configuration is depicted in Fig. 2.12(a). The red lines represent the signal paths, while the black lines represent the ground propagation. Additionally, none of the GND lines are assigned with an ideal GND symbol. This approach facilitates the definition of each signal track with a corresponding GND terminal to represent the microstrip transmission mode. Furthermore, the absence of a universal GND definition ensures that shorting between different GND terminals across the entire chip layout is mitigated. The second approach aims to EM model the entire layout, without dividing it into the sub-blocks. This approach helps circumvent potential inaccuracies that may arise during the modeling of individual blocks and their subsequent integration. Both DC and RF connections continue to be modeled using both signal and GND lines, ensuring that each signal maintains its own distinct reference. This approach is depicted in Fig. 2.12(b). The piece-by-piece and complete layout EM modelings lead to similar results as long as there are clear interfaces between the sub-blocks when the piece-by-piece EM modeling is pursued.

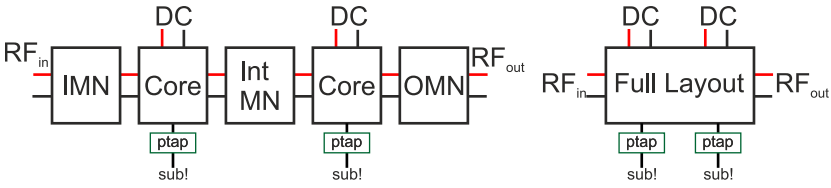


Figure 2.12: Block diagram representations for the (a) Piece-by-piece EM modeling setup. (b) Complete layout EM modeling setup.

In the adopted technology, the connections to the substrate are modeled through a parameterized component (ptap) where the resistance between GND and the substrate can be specified. At this stage of the PA design, the ptap instances, as depicted in Fig. 2.12, connect to the universal node, sub!, which unintentionally shorts the separate GND connections throughout the layout. This inaccuracy was not detected at the time but will be addressed later in Section 2.3.3.

2.2.3 Characterization

The chip micrograph of the fabricated PA is shown in Fig. 2.13. The PA measures 0.83 mm × 0.52 mm, including the pads and the PA core has dimensions of 0.37 mm × 0.3 mm, occupying 0.11 mm^2.

For the small-signal S-parameter measurements, OML's *D*-band frequency extension modules are attached to a PNA-X network analyzer at the RF ports as shown in Fig. 2.14(a). The measured and simulated S-parameters exhibit favorable agreement and are presented in Fig. 2.14(b). The small-signal gain (S_{21}) peaks at 18.2 dB around 135 GHz and has a 3-dB bandwidth (B_{3dB}) of 21 GHz ($\approx$ 16 %).

For the large-signal measurements, WR6.5SGX-M signal generator frequency extension source module is used as the input source where its output power can be controlled through DC voltage. To expand the range of power to be delivered to the device-under-test (DUT) input, a variable attenuator is attached to the source module. In the preliminary phase, the power levels of the input source

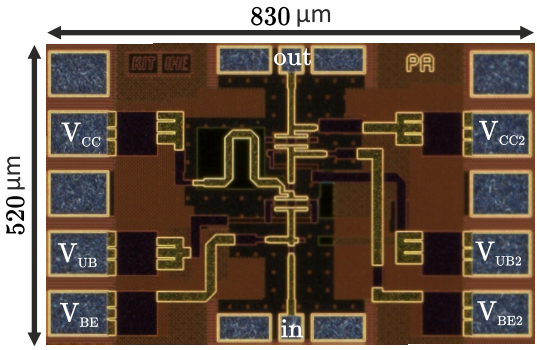


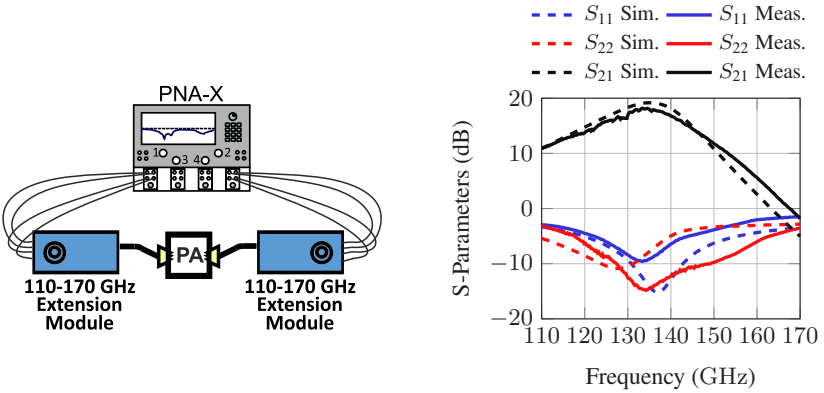
Figure 2.13: Chip micrograph of the fabricated PA. [10] © IEEE

module corresponding to each attenuation levels and DC voltages are recorded through Erickson PM4 power-meter and subsequently used as reference levels as shown in Fig. 2.15(a). Next, the insertion loss (IL) of the probes and the S-bend wave-guides are extracted through a thru measurement, as illustrated in Fig. 2.15(b). Last, a scalar loss calibration has been performed and the measured data are corrected accordingly. Fig. 2.15(c) displays the large-signal measurement setup for the DUT.

Fig. 2.16(a) and Fig. 2.16(b) show the measured and simulated results for P_{sat}, PAE, and gain at 130 GHz and 140 GHz, respectively. At 130 GHz, the measured P_{sat} is 15.5 dBm with a peak PAE of 8.6 %. The amplifier exhibits an output-referred 1 dB compression-point ($OP_{1\text{dB}}$) of 12.2 dBm. On the other hand, at 140 GHz, the measured P_{sat} is 15 dBm with a peak PAE of 7.8 % and $OP_{1\text{dB}}$ of 11 dBm.

2.2.4 Conclusion

A summary of the realized PA's performance is given in Table 2.5, and a comparison to SoA *D*-band PAs are provided in Fig. 2.50, Table 2.5 and Table 2.6. Upon comparing, it is evident that there is room for further improvement, as the proposed PA falls short in performance compared to the SoA. This PA serves as a reference point for future designs, with a focus on optimizing the PA core design as the primary improvement area for future iterations.



(a) (b)

Figure 2.14: (a) Measurement setup for small-signal S-parameters. (b) Measured and simulated small-signal S-parameters. [10] © IEEE

2.3 A SiGe D-Band Power Amplifier with Four-Way Combining

This section includes content and material previously published in [3].

This section introduces a unit and four-way power-combined modified-cascode PAs, as illustrated in Fig. 2.17. The design of the unit PA incorporates a circuit-level solution aimed at enhancing PAE while maintaining high output power for *D*-band PAs. In contrast to conventional design methodologies, the cascode amplifier is conceptualized as a two-stage amplifier, consisting of CE and CB amplifiers. This approach is motivated by the potential for additional optimization at the input terminal of the CB device. The PAs are implemented in a 0.13 µm SiGe BiCMOS technology that features f_T/f_{MAX} of 300/500 GHz.

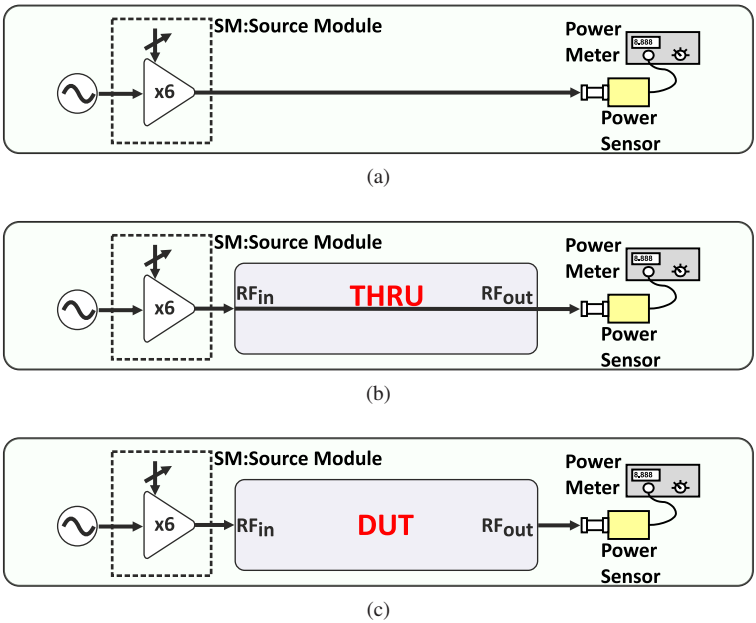


Figure 2.15: Measurement setup for (a) Source module and variable attenuator characterization. (b) D-band probe and waveguide extension characterization. (c) DUT characterization.

2.3.1 Design and Analysis

At mm-wave frequencies, the interconnects between devices introduce significant parasitic effects, requiring the execution of source- and load-pull analyses subsequent to the EM modeling of the PA cores. This step optimizes device sizes and bias points. Notably, as also mentioned in Section 2.2, it is observed that pushing the device size beyond the one chosen in this design leads to diminishing returns in terms of boosting P_{sat}, resulting in decreased PAE due to the increased layout complexity and interconnect losses. To illustrate this pattern clearly for conventional-cascode topology, three different PA cores with increasing number of emitter fingers from 20 to 40 ($\times$20 - $\times$40) are laid out, as shown in Fig. 2.18. Afterwards, EM simulations are performed on these

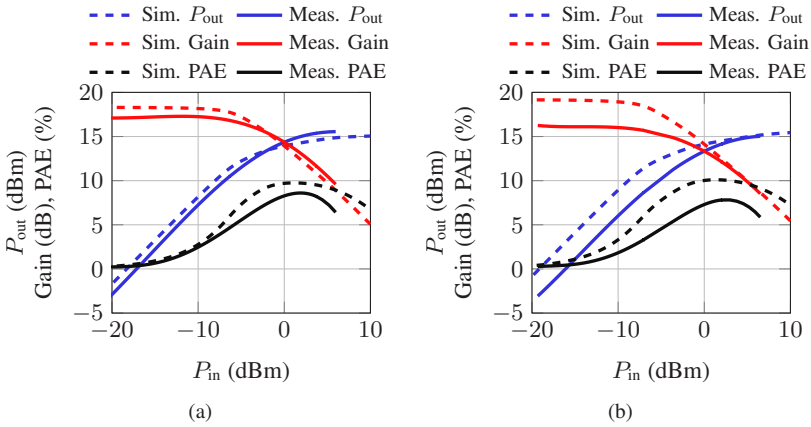


Figure 2.16: Measured and simulated P_{out}, Gain, PAE vs. P_{in} at (a) 130 GHz. (b) 140 GHz. [10] © IEEE

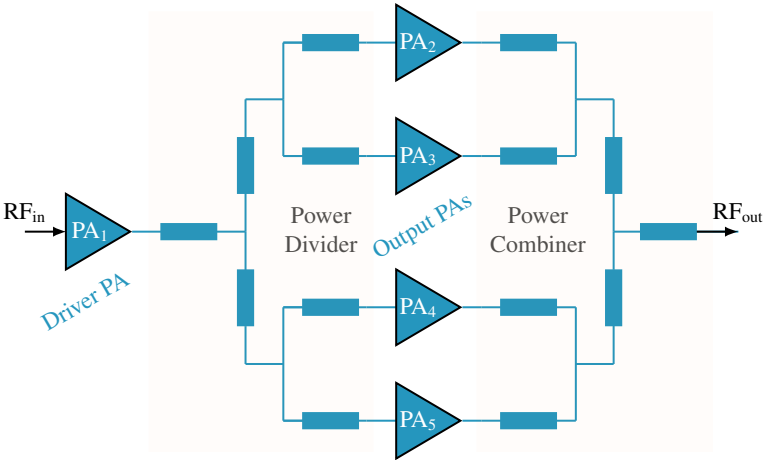
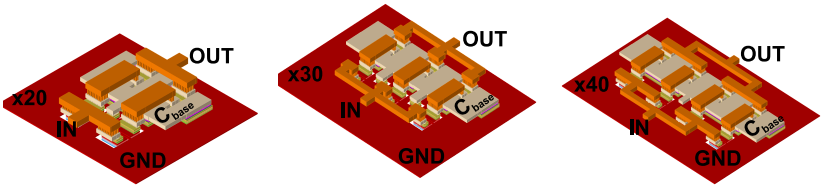


Figure 2.17: Block diagram of the four-way power-combined PA.



(a) (b) (c)

Figure 2.18: 3D representations of PA cores with number of emitter fingers (a) 20. (b) 30. (c) 40.

cores, and optimum source- and load-pull impedances are presented ideally on schematic level to evaluate the large-signal performances.

The large-signal performance evaluation is given in Fig. 2.19(a). At the schematic level, doubling the device size yields a 3 dB increase in P_{sat}, while holding PAE relatively constant. However, at the layout level, where the PA core is EM modeled with interconnects spanning from transistor terminals to the top-most metal layer, enlarging the device size from $\times 20$ to $\times 40$ emitter fingers leads to a mere 1.7 dB P_{sat} enhancement with a notable drop in PAE. Furthermore, the reason why $\times 30$ emitter fingers device performs the worst can be explained as follows. In Fig. 2.18, it can be seen that there is an inherent asymmetry in the layout of $\times 30$ emitter fingers PA core since it contains 3 parallelly placed devices, each formed by $\times 10$ fingers. The input feeding as well as the output lines experience unequal distances between each $\times 10$ emitter fingers device core and matching network interface, leading to a significant drop in P_{sat} and PAE. Furthermore, an indefinite increase in device size results in a considerable decline in the optimum load impedance, resulting in higher losses via more complicated matching networks due to higher impedance transformation ratios, as illustrated in Fig. 2.19(b). In this work, a device size of 20 emitter fingers ($20 \times 0.07 \times 0.9\,\mu\text{m}^2$) is adopted.

Upon selecting a PA core with a device size of $\times 20$, various layout techniques were employed and subsequently compared. Fig. 2.20 displays three distinct PA cores, each incorporating $\times 20$. The leftmost core, Fig. 2.20(a), integrates 4 parallel devices with 5 emitter fingers each, while the middle and rightmost cores, Fig. 2.20(b) and Fig. 2.20(c), consist of 2 parallel devices, each with 10 emitter fingers. The difference between these two cores is that the core in Fig.

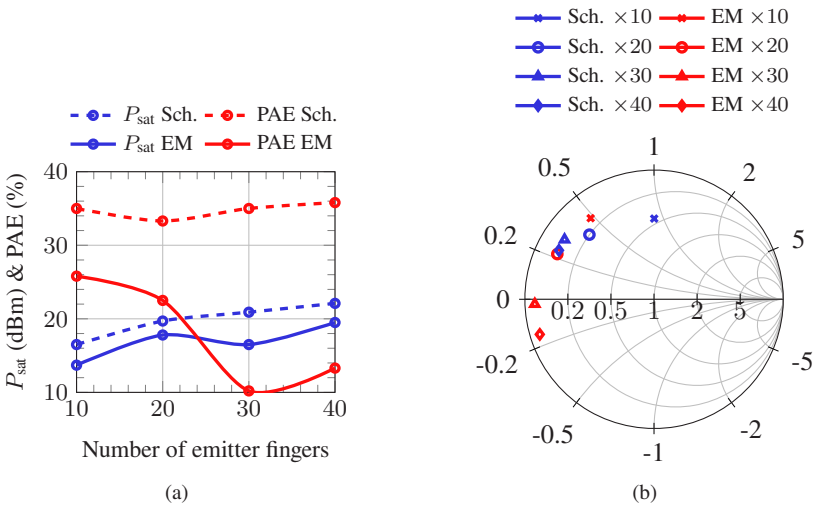


Figure 2.19: Simulated schematic level and EM modeled PA core (a) P_{sat}, PAE vs. device size. (b) $Z_{opt,load}$ vs. device size. [3] © IEEE

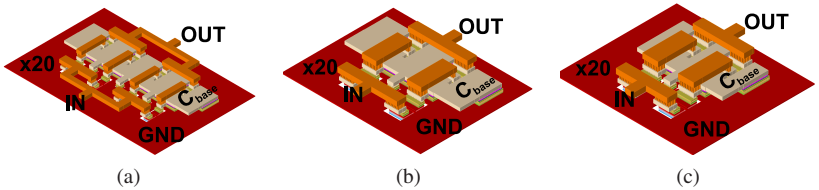


Figure 2.20: Various layout implementation of PA cores with 20 emitter fingers.

2.20(c) maintains a smaller separation between the parallel devices compared to the one in Fig. 2.20(b).

After conducting EM simulations on the PA cores and assessing their large signal performance, a comparative analysis is presented in Table 2.2. This analysis reveals that the core in Fig. 2.20(c) configuration outperforms the other two alternatives due to its minimized interconnect length and reduced parasitic effects.

Table 2.2: Large-signal performance comparison of the PA cores in Fig. 2.20.

	P_{sat} (dBm)	PAE (%)
PA Core in Fig. 2.20(a)	17.8	22.5
PA Core in Fig. 2.20(b)	17.3	17.6
PA Core in Fig. 2.20(c)	17.6	24.5

Table 2.3: Values of the schematic components [3] © IEEE.

$Q_{1,2}$	$20 \times 70\,\text{nm} \times 900\,\text{nm}$	C_1	75 fF	L_1	130 pH
$Q_{3,4,6}$	$1 \times 70\,\text{nm} \times 900\,\text{nm}$	C_2	4 pF	L_2	30 pH
Q_5	$4 \times 70\,\text{nm} \times 900\,\text{nm}$	C_3	70 fF	L_3	450 pH
TL_1	44 µm, 50 Ω	C_4	500 fF	R_1	100 Ω
TL_2	25 µm, 50 Ω	C_{pad}	17 fF	R_2	2 kΩ

The proposed cascode interstage matching design and bias circuits are illustrated in Fig. 2.21 and the component values are given in Table 2.3. By performing a source-pull simulation and optimizing the source impedance for the input terminal of the CB device, along with separating the supply voltages of CE and CB amplifiers, a considerable enhancement in PAE is achieved. Schematic simulations provide a conceptual understanding of this improvement, isolating the design from layout-level effects. As evident from Fig. 2.22(a), the proposed approach achieves a 4 % increase in PAE while maintaining a similar P_{sat}. Notably, this includes the losses introduced by the interstage matching network (L_1, C_3, TL_2) in the proposed approach, which is not part of the conventional-cascode design.

The conventional-cascode approach employs a supply voltage of 4 V, whereas the proposed design distributes the same voltage amount between CE (1.2 V) and CB (2.8 V) amplifiers. Fig. 2.22(b) highlights that at lower P_{in} levels, collector currents (I_{cc}) remain similar, indicating equivalent power consumption for both cases. As P_{in} increases, the I_{cc} rise in the conventional-cascode and CB stage I_{cc} in the modified cascode PA exhibit similar levels of jump, while the rise in CE stage I_{cc} is notably smaller. This disparity can be explained as follows: In the conventional-cascode design, the CE device provides a volt-

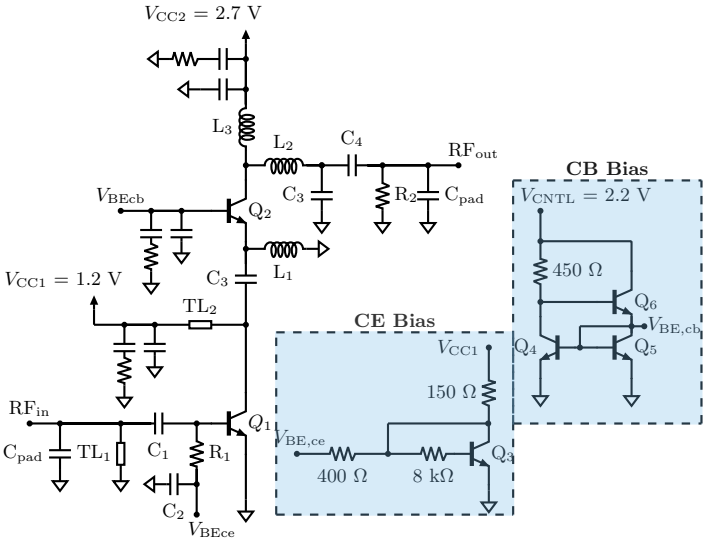


Figure 2.21: Simplified circuit schematic of the modified-cascode PA. [3] © IEEE

age gain of 1, consuming the same current as the CB device. Conversely, in the proposed approach, the same voltage gain can be achieved with a smaller current, thanks to the enhanced impedance at the collector of the CE device.

After EM modeling of the CE and CB stages of the PA core, source and load-pull analyses are conducted, and optimum load 5 + j11 Ω and source 5 - j13 Ω impedances for the CB device are found out. This ensures full utilization of the CB device both at its input and output terminals, whereas the CE device serves primarily as a driver stage due to its favorable input impedance and efficient input matching. Both CE and CB devices are operated at class A regime for improved gain.

The CB devices incorporate bias circuits [VHv+05] capable of sinking avalanche current by presenting a very low impedance ($\approx 1\,\Omega$). This allows the CB devices to be biased beyond BV_{CEO}, ensuring reliable operation while maintaining stability against temperature variations. The simulation results in Fig. 2.23(a) demonstrate that the bias circuit maintains the $V_{BE,cb}$ of the CB device almost constant across changing temperatures, preventing thermal runaways. Conse-

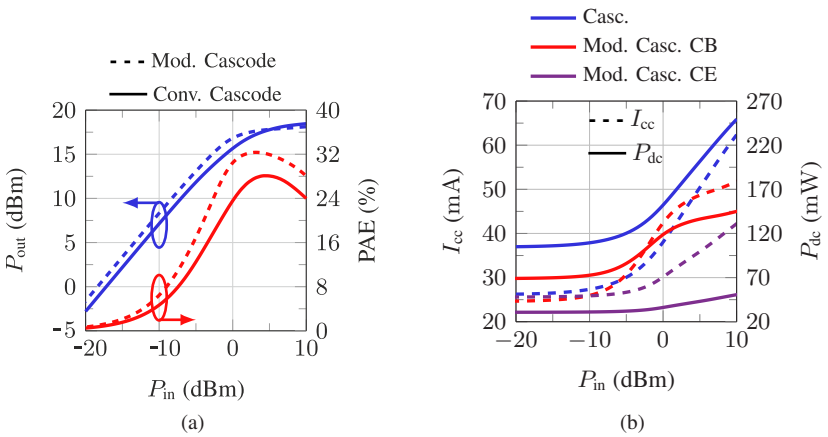


Figure 2.22: Schematic level simulated comparison of conventional-cascode and modified-cascode approaches in (a) P_{out} & PAE. (b) I_{cc} & P_{dc}. [3] © IEEE

quently, the variation in PAE remains below 0.5 % across the entire temperature range, a significant improvement compared to a drop of nearly 5 % without the bias circuitry, as shown in Fig. 2.23(b). The changes in P_{sat}, I_{cc} and I_{sink} over temperature are also given. The CE device bias circuit employs 8 kΩ and 400 Ω resistors, whose ratio equals to the mirroring ratio.

To mitigate instability at mm-wave frequencies, bypass capacitors are placed near the base terminal of CB amplifiers. Large bypass capacitors, both with and without de-Q resistors, are implemented in the supply lines to suppress low-frequency oscillations. Figure 2.24 shows the layout image of the four-way *D*-band power combiner/divider, exhibiting a good matching better than −10 dB at all ports, with a simulated IL of approximately 1.3 dB.

2.3.2 Characterization

The fabricated chip micrographs of the unit and power-combined PAs are shown in Fig. 2.25(a) and Fig. 2.25(b).

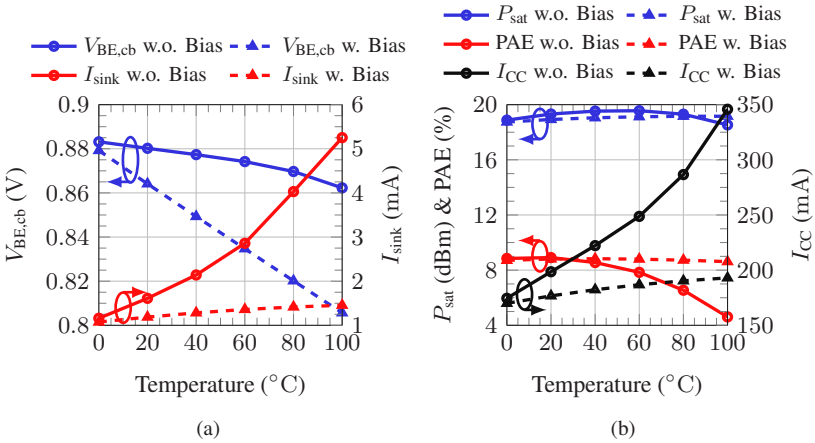


Figure 2.23: Effect of temperature with bias circuitry (dashed) and without bias circuitry (solid) on (a) $V_{BE,cb}$ (blue) and I_{sink} (red). (b) P_{sat} (blue), PAE (red) and I_{cc} (black). [3] © IEEE

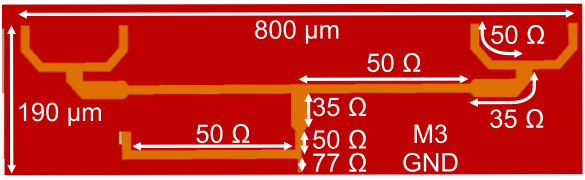


Figure 2.24: A 3D image of the four-way power combiner. [3] © IEEE

The individual PA unit occupies dimensions of 0.43 mm × 0.6 mm, including both pads. The core of the PA measures 0.21 mm × 0.48 mm, utilizing a compact area of 0.1 mm^2. Meanwhile, the power-combined PA's dimensions are 1.43 mm × 1.3 mm, resulting in a combined footprint of 1.86 mm^2.

The measurement setup for the small signal characterization is as illustrated in Fig. 2.14(a). For the power-combined PA, the maximum small-signal gain is measured to be 16 dB at 130 GHz with a B_{3dB} of 18 GHz (≈ 14 %).

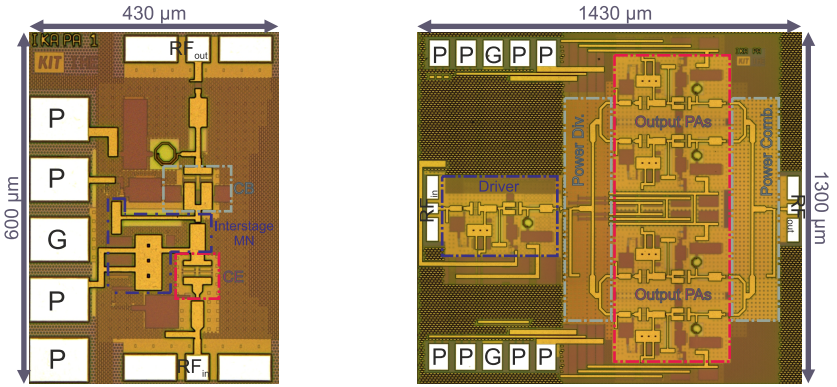


Figure 2.25: Chip micrographs of the fabricated (a) Unit PA. (b) Power-combined PA. [3] © IEEE

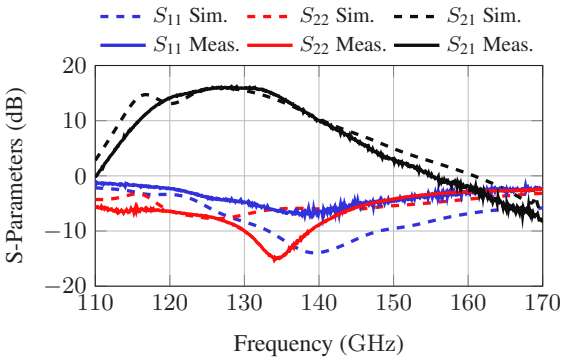


Figure 2.26: Measured and simulated S-parameters of the four-way power-combined PA. [3] © IEEE

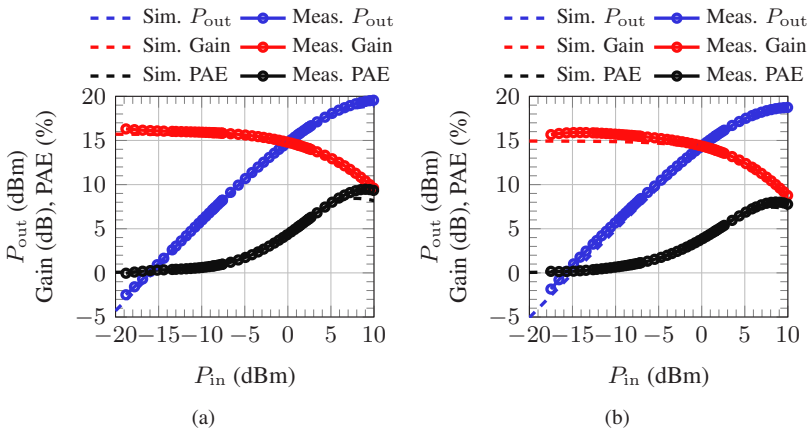


Figure 2.27: Measured and simulated P_{out}, Gain and PAE vs. P_{in} at (a) 130 GHz. (b) 132 GHz. [3] © IEEE

The measurement setup used in large signal characterization is shown in Fig. 2.15. Fig. 2.27 illustrates the measured and simulated large-signal parameters at 130 GHz and 132 GHz. At 132 GHz, a P_{sat} of 19.6 dBm is attained alongside an OP_{1dB} of 14 dBm, and maximum achieved PAE of 9.5 %. Furthermore, Fig. 2.28(a) shows the large signal parameters across the frequency band of 125 to 135 GHz, demonstrating a P_{sat} exceeding 18.75 dBm and a $PAE_{max.}$ above 8 % maintained between 125 to 133 GHz.

The PA is also subjected to large-signal conditions over a specific duration. With a fixed input power of 4 dBm, the P_{out} is recorded every 20 s during a 2 h period. As depicted in Fig. 2.28(b), the variation in P_{out} remains within the range of ±0.2 dB. The collector current of the CB device is also measured and found to remain stable. Despite the increasing temperature caused by dissipated and generated power over time, the PA continues to operate effectively, underscoring the proper functioning of the bias circuits.

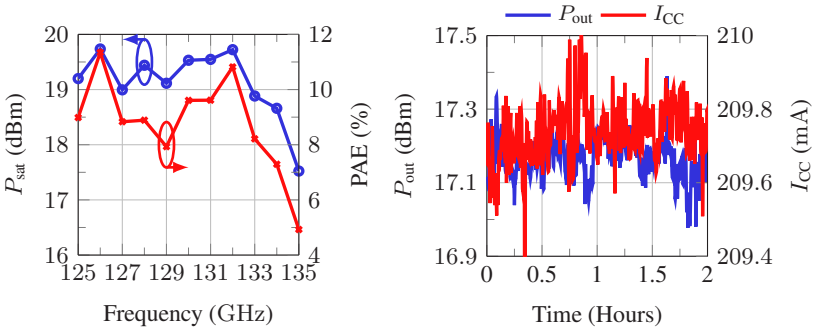


Figure 2.28: Measured (a) P_{sat} and $PAE_{max.}$ vs. frequency. (b) P_{out} and I_{cc} of CB over time. [3] © IEEE

2.3.3 Conclusion

One important observation has to be stated. Prior to achieving agreement between the simulated and measured results, as depicted in Fig. 2.27(a), it is crucial to address the initial disparities encountered in the results. Initially, the planned V_{cc} for the CB device was set at 3.3 V. However, during the measurements, an increase in V_{cc} resulted in breakdown issues, leading to a sudden rise in I_{cc} of the CB. Consequently, V_{cc} was kept at 2.7 V. The resulting drop in simulated performance due to the reduction in V_{cc} from 3.3 V to 2.7 V is shown in Fig. 2.29(a). A crucial finding from the measurements revealed that the current sinking transistor (Q_5) in the bias circuit of the CB device, as depicted in Fig. 2.21, was insufficiently sized to handle the avalanche current resulting from the increased V_{cc}. Scaling up the dimensions of Q_5 would allow for a higher V_{cc} to be applied to the CB device, consequently enhancing the output power.

Subsequently, in the adopted technology, the connections to the substrate are modeled through a parameterized component where the resistance between GND and the substrate can be specified. However, a challenge arises when different devices at various locations in the layout share the same global substrate

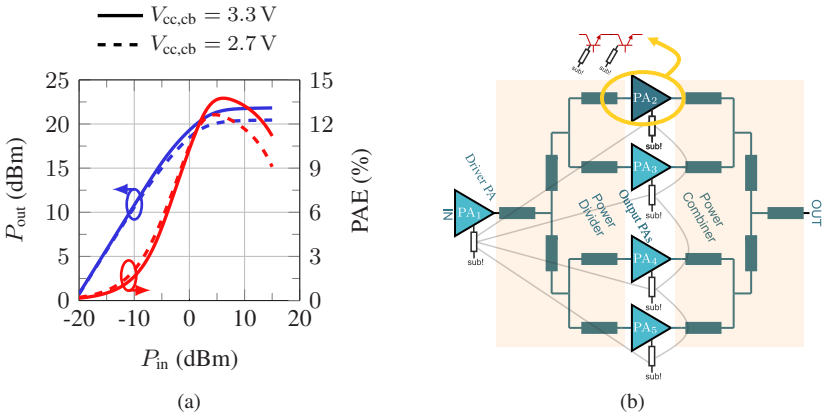


Figure 2.29: (a) Impact of V_{cc} on P_{out} and PAE. (b) Block diagram illustrating the inaccurate connections to the substrate during initial simulations.

(default option in the process), leading to a shorting of the GNDs of different devices together. This modeling mistake is illustrated in Fig. 2.29(b).

Following the individual modeling of the substrate connection for each active device — where the substrate node of the active device in the schematic is tied to the local GND surrounding the device in the layout during EM modeling — a noticeable observation emerges. The output power experiences a reduction of approximately 1.5 dB, as shown in Fig. 2.30(a), attributed to the more precise modeling of the parasitic capacitance to the substrate, consequently resulting in a deviation from the $Z_{opt,load}$. At the end, the measured and simulated results are displayed again in Fig. 2.30(b).

A summary of the realized PA's performance is given in Table 2.5, and a comparison to SoA *D*-band PAs are provided in Table 2.5 and Table 2.6. The proposed PA achieves one of the highest P_{sat} values among the Si based PAs while maintaining a respectable PAE, presenting a competitive performance compared to other SoA Si *D*-band PAs.

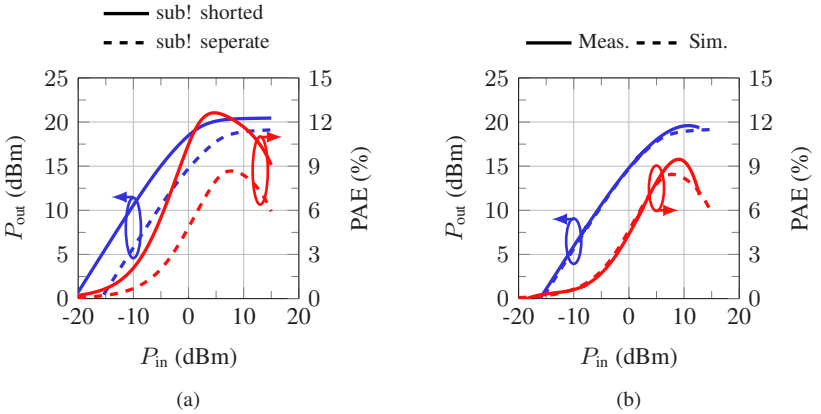
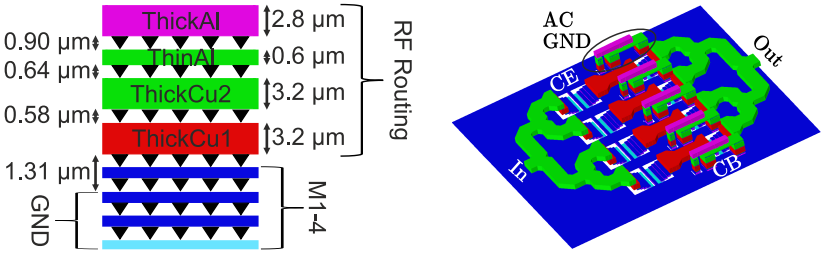


Figure 2.30: (a) Impact of substrate connections on P_{out} and PAE. (b) Measured and simulated curves after reducing the V_{cc} and correcting the substrate connections.

2.4 A D-Band Power Amplifier with Coupled Line Based Four-Way Power Combining in an Advanced SiGe

This section includes the design, analysis and simulated results of a *D*-band PA implemented in a latest generation 130 nm SiGe BiCMOS technology with f_T/f_{MAX} of 470/650 GHz. The limiting factor in generated output power of *D*-band PAs is often the diminished available gain with increased operating frequency at the output stage devices. Opting for a technology with higher f_T and f_{MAX}, thereby ensuring higher available gain, is anticipated to enhance the output power of the PA. Additionally, in contrast to the technology adopted for the PAs in the previous sections, the chosen technology in this work incorporates a Cu BEOL with two thick Cu- and one thick Al metals, promising lower losses incurred in the matching networks as well as in the PA core. The comparison of MAG between the technologies is given in Fig. 1.7(e) and Fig. 1.7(f). The stack-up of the BEOL and an exemplary PA core are displayed in Fig. 2.31.



(a) (b)

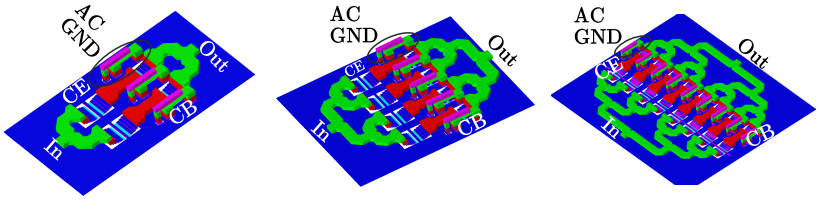
Figure 2.31: (a) SG13G3 technology stack-up. (b) 3D view of a PA core.

2.4.1 Design and Analysis

The advantage of employing Cu BEOL becomes evident in the final performance of the PA core. In comparison to Al BEOL, the sheet resistance of thinner metal layers (M_{1-4}) is reduced by approximately 40 %, while the reduction is more significant for thicker layers, ranging from 50 % to 60 %. Cu BEOL also exhibits a substantially improved via resistivity, reaching as low as one-tenth of that experienced in Al BEOL.

Conducting a similar study on the device sizing of EM-modeled cascode PA cores, as previously illustrated in Section 2.2 and Section 2.3, reveals that the utilization of a better conductivity BEOL allows for the implementation of larger device sizes, owing to the less detrimental characteristics of the interconnects. For instance, as depicted in Fig. 2.8 and Fig. 2.19, utilizing a PA core with a total of 20 emitter fingers (2×10) was the limit with Al BEOL, as further increases resulted in significantly diminished returns. However, with Cu BEOL, this limit now extends to a device size of 32 emitter fingers (4×8), supporting the notion that the adverse impact of RF routing from the transistor terminals to the upper metal layers on the transistor's overall performance, as analyzed in [SUZC15], can be mitigated with the adoption of a superior BEOL.

Three distinct PA cores with a total of 16, 32, and 64 emitter fingers, as shown in Fig. 2.32, are EM modeled and analyzed individually. The performance parameters comparison is presented in Table 2.4. Among them, a total device size of 32 emitter fingers ($4 \times 8 \times 0.07 \times 0.9\,\mu m^2$) is chosen, since it leads to



(a) (b) (c)

Figure 2.32: 3D representations of PA cores with number of emitter fingers (a) 2×8. (b) 4×8. (c) 8×8.

Table 2.4: Large-signal performance comparison of the PA cores with different emitter fingers.

PA Core	Gain (dB)	P_{1dB} (dBm)	P_{sat} (dBm)	PAE (%) @ OP_{1dB}	PAE (%) @ P_{sat}	$Z_{opt,load}$ (Ω)	$Z_{opt,source}$ (Ω)
×16 Fig. 2.32(a)	18.9	16.9	17.6	27.8	30.1	6+j10	3.7-j1.7
×32 Fig. 2.32(b)	17.2	19.3	20.3	24	27.4	3+j1	2-j5
×64 Fig. 2.32(c)	13.7	20.8	22.4	16.5	18.4	2.5-j7	1.9-j10.8

the best output power and PAE combination. The PAs are biased at class A regime, with a collector current density of 2.5 mA, which results in close to the peak f_T & f_{MAX} performance, as shown in Fig. 1.7(b). A V_{cc} of 3.3 V is selected to keep the cascode amplifier under non-aggressive supply conditions.

For a PA core with 32 emitter fingers, the impact of load impedance on P_{sat} and PAE is illustrated in Fig. 2.33 and Fig. 2.34 through contour plots on a Smith chart and a rectangular plot, respectively. The resulting optimum load and source impedances are also displayed in Table 2.4. Presenting the device with 32 emitter fingers with a load impedance of as low as 3 + j1 Ω and a source impedance of 2 - j5 Ω leads to a P_{sat} of 20.3 dBm with a PAE of 27.4 %.

The simulated large-signal performance of the PA core, featuring 32 emitter fingers, with respect to changing P_{in} is presented in Fig. 2.35 after the PA core

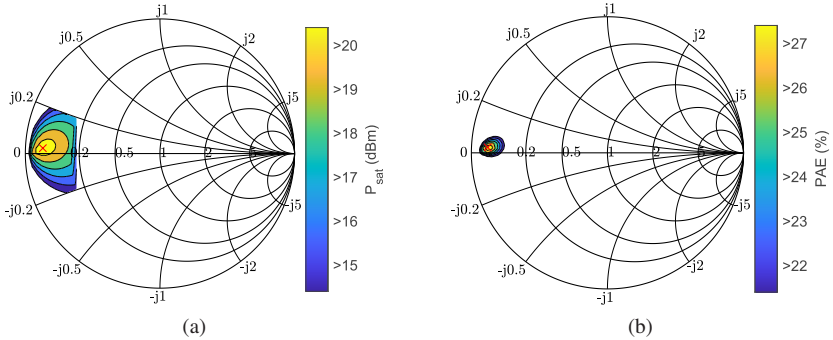


Figure 2.33: Simulated load-pull contours for the EM modelled PA core with 32 emitter fingers simulated at 140 GHz (a) P_{sat}. (b) PAE.

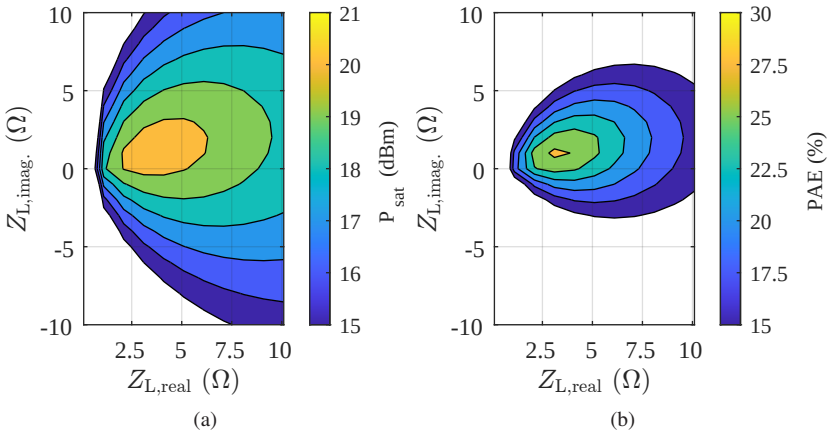


Figure 2.34: The PA core with 32 emitter fingers simulated at 140 GHz (a) P_{sat} vs. $Z_{\mathrm{L,real}}$ & $Z_{\mathrm{L,imag.}}$. (b) PAE vs. $Z_{\mathrm{L,real}}$ & $Z_{\mathrm{L,imag.}}$.

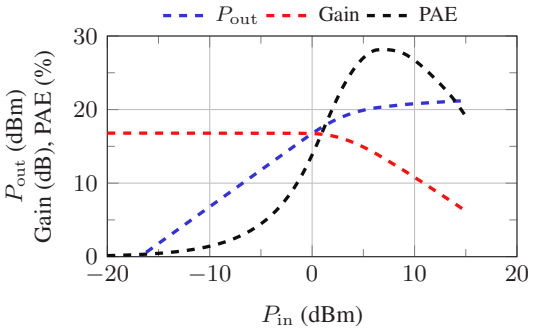


Figure 2.35: The simulated P_{out}, Gain, and PAE vs. P_{in} at 140 GHz for the PA core with 32 emitter fingers.

is ideally presented with $Z_{\mathrm{opt,load}}$ and $Z_{\mathrm{opt,source}}$. It is important to note that, at this point in the design, this simulation does not account for the losses that will be incurred through the matching networks.

After identifying $Z_{\mathrm{opt,load}}$ and $Z_{\mathrm{opt,source}}$ through load and source pull optimizations, the matching networks are designed using lumped elements, and the corresponding circuit schematic is provided in Fig. 2.36. Additionally, Fig. 2.37 illustrates the matching networks with their component parameters. The overall output matching network is optimized in terms of the loss performance, and the final EM-modeled network is simulated to have a loss of 1.4 dB at 140 GHz. The chip micrograph of the realized unit PA is demonstrated in Fig. 2.38(a).

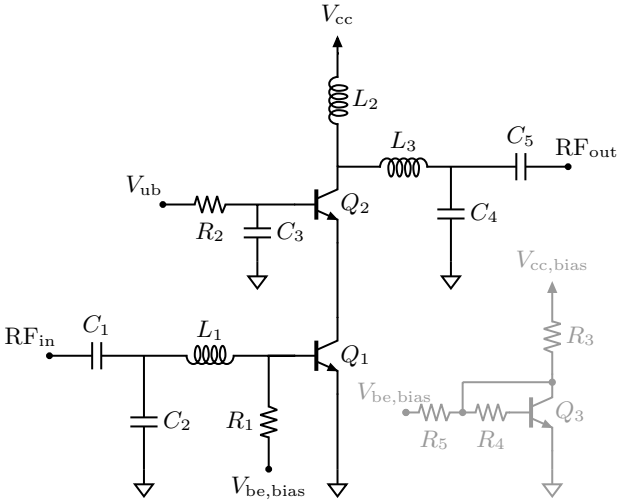


Figure 2.36: Simplified circuit schematic of the unit cell cascode PA (bypass networks not shown), matching network component values are given in Fig. 2.37.

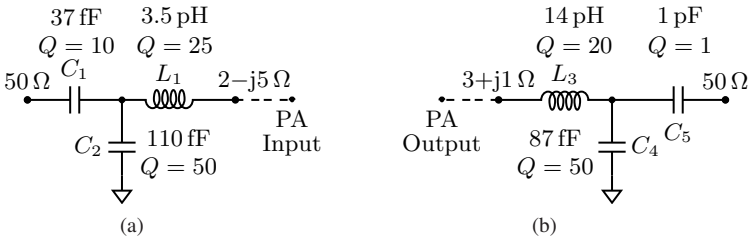
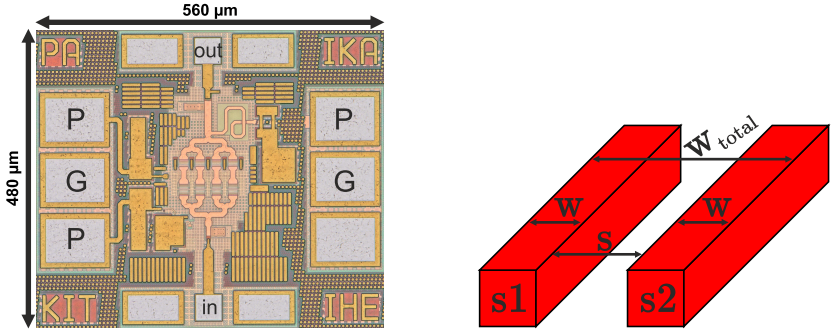


Figure 2.37: Matching networks for the PA core with 32 emitter fingers (a) Input matching network with simulated matching network loss of 0.9 dB. (b) Output matching with simulated matching network loss of 1.4 dB.



(a) (b)

Figure 2.38: (a) Top view of the unit-PA layout. (b) Representation of the coupled lines with the relevant dimensions.

Power Combiner Design

The design of the power combiner starts with an analysis of the microstrip (MS) transmission lines (TLs), focusing on the line impedance (Z_{Line}) and loss per unit length (dB / mm). A 4-1 power combiner requires a 50 Ω to 200 Ω impedance conversion (referring to Fig. 2.42, consider the impedance transformation from X_1 to X_5). Therefore, it is crucial to implement a TL with a line impedance of 100 Ω, according to (2.7) where N is the degree of power combining. Fig. 2.39(a) illustrates that a line impedance of 100 Ω can be achieved only with a line width smaller than 5 µm, which results in increased loss, as depicted in Fig. 2.39(b).

$$\begin{aligned} Z_{\text{L}} &= \sqrt{N \cdot Z_{\text{in}} \cdot Z_{\text{out}}} \\ &= \sqrt{4 \cdot 50\,\Omega \cdot 50\,\Omega} = 100\,\Omega \end{aligned} \tag{2.7}$$

To attain the desired line impedance with larger line widths, a coupled line (CL) approach is employed. Additionally, the spacing between the coupled lines serves as an additional design parameter to control the line impedance. Fig. 2.40(a) illustrates the even-mode line impedance, based on metal width and spacing, for different metal layers. Furthermore, the impact of metal width

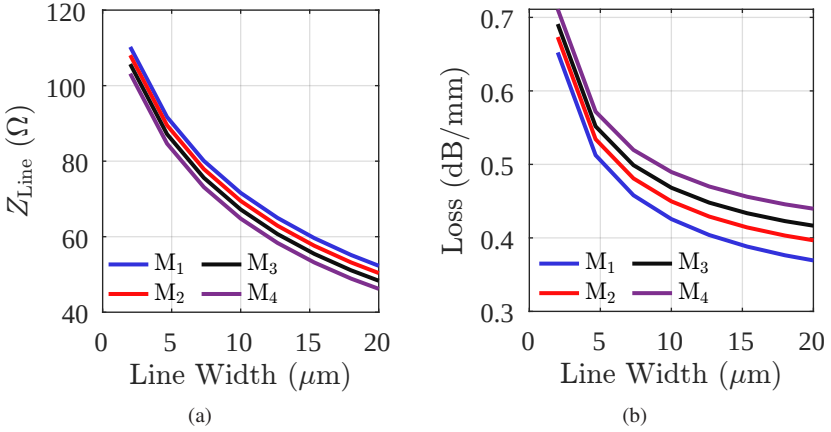


Figure 2.39: Analysis of MS TL in terms of Z_{Line} and loss per unit length based on line width for different GND metal layers (Metal_1-Metal_4).

and spacing on loss performance has been investigated for both ThickAl and ThickCu2 metal layers, with results presented in Fig. 2.40(b). As can be seen, ThickAl demonstrates a better loss performance compared to ThickCu2 (see the BEOL stack-up in Fig. 2.31(a)) primarily because ThickAl is located at a higher elevation in the stack-up. The choice of GND plane metal plays an insignificant role, thus the analysis is not shown.

It is also evident from Fig. 2.40(a) that there exist multiple combinations of line width and spacing that result in an Z_{Line} of 100 Ω. In order to choose the dimensions of line width (w) and spacing (s), the following additional metrics are introduced.

- Layout Geometry: define the total width of the structure as $w_{\text{total}} = 2 \cdot w + s$. It is desirable to minimize w_{total} to avoid phase deviation during the 90° turns at the combiner structure corners due to the asymmetry (see Fig. 2.43). Therefore, w_{total} is set to 10 µm.
- Total Loss: opt for a combination of w and s that minimizes the total loss.

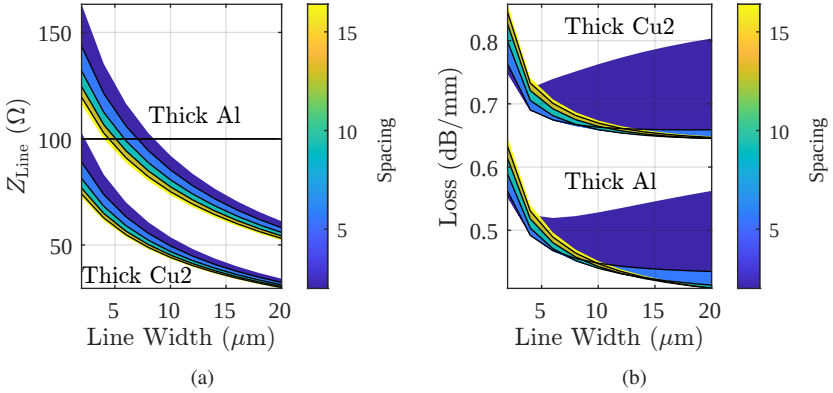


Figure 2.40: Analysis of CLs in terms of Z_{Line} (even-mode) and loss per unit length based on line width and spacing for different metal layers.

Fig. 2.41 presents the same data for ThickAl as depicted in Fig. 2.40(b), offering improved readability regarding how w and s influence even mode line impedance and loss. Generally, as shown in Fig. 2.41(b), decreasing s leads to lower losses due to a stronger coupling between the coupled lines, while a higher w is required to maintain Z_{Line} at desired 100 Ω. Maintaining an optimal w_{total} is crucial to preserve phase balance. Conversely, a lower w necessitates a higher s to satisfy the condition $Z_{\mathrm{L}} = 100\,\Omega$, resulting in increased losses. Considering these trade-offs, the following dimensions are selected: $w, s = 8$ µm, 2 µm yielding $Z_{\mathrm{L}} = 103\,\Omega$ and $w_{\mathrm{total}} = 18$ µm.

A visual representation of the output PAs, power combiner, and the pad modeling is presented in Fig. 2.42. An additional matching network is incorporated to counteract the effects of pad inductance and capacitance and have a better flexibility on arranging the length of the lines to ensure proper alignment with the spacing between PA_{1-4}. The layouts of the power divider and combiner are depicted in Fig. 2.43(a) and Fig. 2.43(b), respectively. It is noteworthy that the combiner in Fig. 2.43(b) utilizes an additional shunt stub to the GND to offset the pad effect.

Fig. 2.44(a) and Fig. 2.44(b) illustrate the performance parameters of the power divider and power combiner, respectively. Both divider and combiner

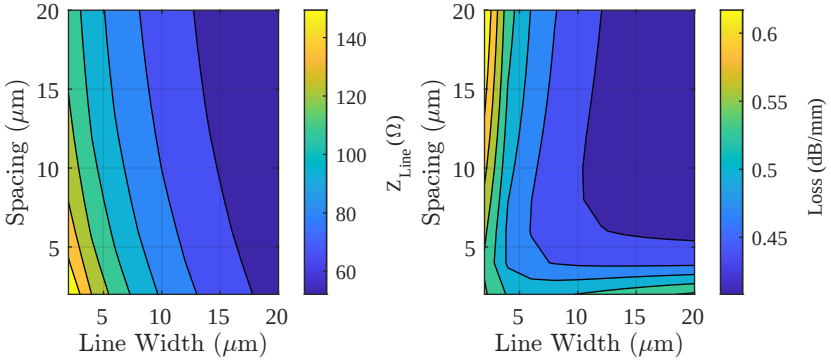


Figure 2.41: Analysis of Thick Al CLs in terms of Z_{Line} (even-mode) and loss per unit length based on line width and spacing.

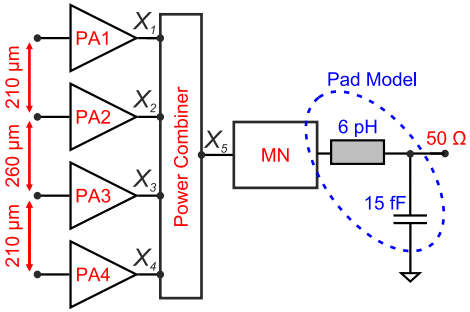


Figure 2.42: A block diagram representing the output PAs, power combiner, and the pad modeling.

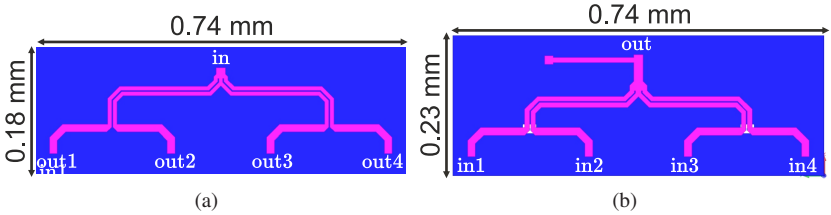


Figure 2.43: Representation of the four-way (a) Power divider. (b) Power combiner.

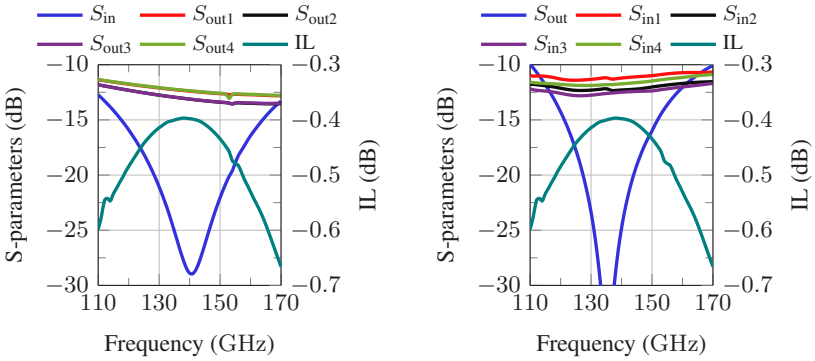


Figure 2.44: Simulated return losses and insertion loss of the (a) Power divider. (b) Power combiner.

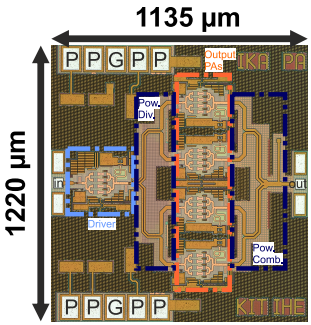


Figure 2.45: Chip micrograph of the four-way power-combined PA layout.

exhibit a total IL of around 0.4 dB at 140 GHz with return losses remaining better than −10 dB over the entire *D*-band frequency range. To enhance the overall gain and ensure sufficient input power for driving the output PAs, an additional driver amplifier, identical to the output amplifiers, is incorporated at the input.

The chip-micrograph of the four-way power-combined PA is presented in Fig. 2.45.

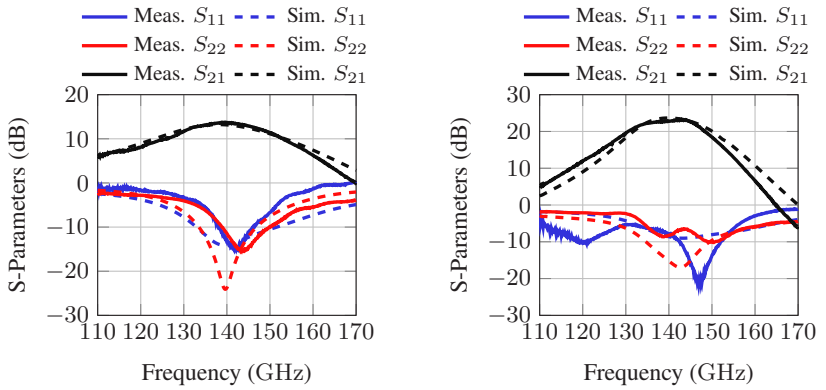


Figure 2.46: Simulated and measured small-signal S-parameters of the (a) Unit PA. (b) Four-way power-combined PA.

2.4.2 Measurement Results

Fig. 2.46(a) and Fig. 2.46(b) present the simulated and measured small-signal S-parameters of the unit and four-way power-combined PAs, respectively. The peak S_{21} values are measured to be 13.7 dB and 22.8 dB for the unit and four-way power-combined PAs, respectively.

The simulated and measured large signal results of the unit and the power combined PAs are illustrated in Fig. 2.47 and Fig. 2.48. At the operating frequency of 136 GHz, referring to Fig. 2.47, the unit PA achieves a P_{sat} of 18.7 dBm while attaining an O$P_{1\text{dB}}$ of 17.7 dBm. The relatively linear operation, characterized by a higher O$P_{1\text{dB}}$, is primarily attributed to the class A operation. For the same amplifier, the measured PAE peaks at 19.9 %, where a PAE of 18.9 % is observed at 1 dB compression-point. Meanwhile, the power-combined PA demonstrates a P_{sat} of 23.7 dBm with a PAE_{max} of 16.6 %, as can be seen in Fig. 2.48.

The large signal frequency response of the unit and power combined PAs is illustrated in Fig. 2.49. The $B_{3\text{dB}}$ in terms of the P_{sat} is measured to be from 125 GHz to 145 GHz for both amplifiers.

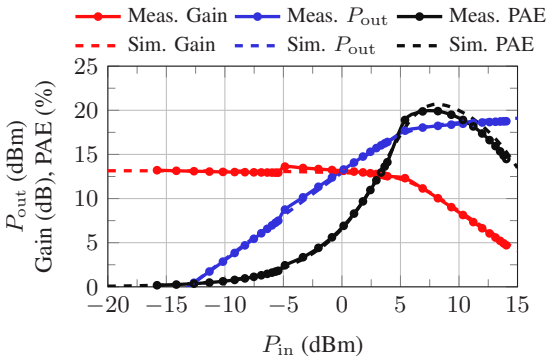


Figure 2.47: Simulated and measured P_{out}, Gain and PAE of the unit PA at 136 GHz.

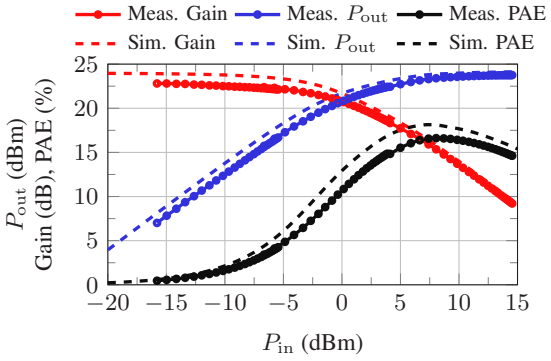


Figure 2.48: Simulated and measured P_{out}, Gain and PAE of the four-way power combined PA at 136 GHz.

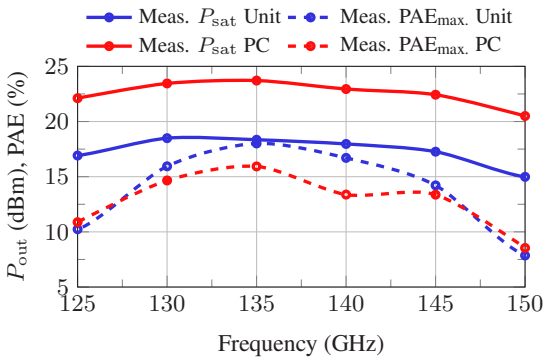


Figure 2.49: Simulated and measured P_{sat} and PAE$_{\mathrm{max.}}$ of the unit and four-way power combined PAs vs. frequency.

2.4.3 Conclusion

This section introduces a unit PA and a four-way power-combined PA implemented in an advanced 130 nm SiGe BiCMOS technology with a Cu BEOL. Initially, a detailed analysis is conducted on PA cores, evaluating their performance parameters after EM modeling for differently sized PA cores. Subsequently, the design of a coupled-line-based 4-1 power combiner/divider is discussed. At the end, the simulated and measured small and large signal performance parameters are illustrated. A comparison of the measured performance parameters with SoA is illustrated in Fig. 2.50, accompanied by Table 2.5 and Table 2.6.

2.5 Summary and Performance Comparisons

This dissertation provides an in-depth analysis of SiGe-based *D*-band PAs featuring three distinct unit and two power-combined PAs. It covers the design procedure of unit PAs and provides detailed insights into the power combiner techniques. Additionally, this section incorporates a comprehensive literature review, outlining the SoA PAs operating at *D*-band frequencies implemented in SiGe, CMOS, and III-V technologies. Fig. 2.50 presents a detailed comparison

of SoA PAs based on operating frequency, P_{sat}, and PAE. The outlined SiGe-based PAs are further detailed in Table 2.5, while Table 2.6 involves PAs implemented in CMOS and III-V technologies.

The PA discussed in Section 2.2 is denoted by the color blue. The power-combined PA detailed in Section 2.3 is represented by the color red, and the additional power-combined PA introduced in Section 2.4 is identified by the color purple. As can be seen from Fig. 2.50, there is a clear trend that demonstrates the superior performance of the III-V technologies. Meanwhile, among the Si-based PAs, the PA demonstrated in Section 2.4 exhibits the highest P_{sat} and PAE.

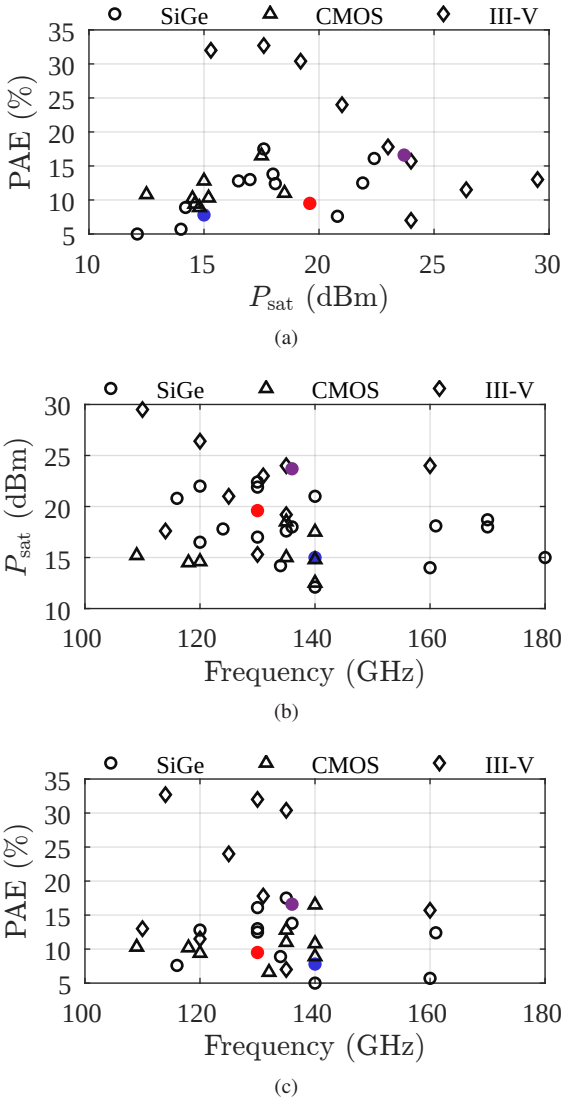


Figure 2.50: SoA PAs above 100 GHz demonstrated in various processes (a) P_{sat} and PAE. (b) P_{sat} and frequency. (c) PAE and frequency.

Table 2.5: SoA PAs above 100 GHz in SiGe technologies.

Ref.	Tech.[a]	Freq. (GHz)	B_{3dB} (GHz)	Gain (dB)	P_{sat} (dBm)	OP_{1dB} (dBm)	$PAE_{max.}$ (%)	Area (mm^2)	Pow. Com.[§]
[PRM21]	55 nm*	135	34	24	17.6	16.8	17.5	0.18†	1
[LR14]	90 nm*	116	24	15	20.8	17	7.6	4.95	8
[DB18]	90 nm*	120	30	7.7	22	13#	3.6	0.62	8
[RC21]	90 nm*	130	35	18.2	21.9	18.6	12.5	1.7	4
[OB22]	90 nm*	134	30#	9.3	14.2	10.1	8.9	0.14†	1
[YE15]	120 nm*	124	17	32	17.8	13.5	4.3	1.92	1
[KBW+17]	130 nm*	120	28	26.5	16.5	N.A	12.8	0.24†	1
[VVT+19]	130 nm*	130	30	34	17	14.7	13	0.35†	2
[LCW+22]	130 nm*	130	28	21.8	22.4	14.1#	16.1	0.58†	8
[AMKU22b]	130 nm*	130	18	16	19.6	14	9.5	1.86	4
[VHdM+20]	130 nm*	136	38	31	18	13	13.8	1.28	4
[SHZ+23]	130 nm*	140	60	14.5	21	19.6	2	9	8
[AMKU22a]	130 nm*	140	21	16.7	15	11	7.8	0.44	1
[KEKM21a]	130 nm*	140	60	21	12.1	10	5	0.19	1
[FAHS17]	130 nm*	160	49	27	14	11.4#	5.7	0.48	1
[LCL+22a]	130 nm*	161	40	30.7	18.1	14.5#	12.4	0.42	4
[KNK19]	130 nm*	170	25	30.2	18	15.6	4	0.85	8
[AYG+20]	130 nm*	170	27	23.6	18.7	15#	4.4	1.35	4
[SCE20]	130 nm*	180	80	19	15	13	3.5	0.92	4
Section 2.4	130 nm*	136	18	23.2	23.7	19	16.6	1.4	4

[a] Technology: * SiGe
graphical estimation
§ number of power combining
† core area only
& simulated

Table 2.6: SoA PAs above 100 GHz in CMOS and III-V compound technologies.

Ref.	Tech.[a]	Freq. (GHz)	B_{3dB} (GHz)	Gain (dB)	P_{sat} (dBm)	OP_{1dB} (dBm)	$PAE_{max.}$ (%)	Area (mm^2)	Pow. Com.[§]
[PR20]	16 nm△	135	22	20.5	15	9.2	12.8	0.04[†]	2
[TNM+21b]	22 nm△	140	30	33.6	12.5	9.4	10.8	0.024	1
[CB22a]	22 nm△	140	38	13.5	17.5	14[#]	16.5	0.37	4
[TNM+20]	28 nm△	132	22	22.5	8	5.2	6.6	0.03[†]	1
[SJK+19]	40 nm△	120	39	16	14.6	9.3	9.4	0.33	4
[SR18]	40 nm△	140	17	20.3	14.8	10.7	8.9	0.34	2
[LR22]	45 nm△	135	15	24.8	18.5	13.5	11	0.46[†]	8
[SJK+16]	65 nm△	109	17	20.3	15.2	12.5	10.3	0.34	4
[SLK+18]	65 nm△	118	17	22.3	14.5	12.2	10.2	0.34	2
[ĆBL+19]	100 nm*	120	20	29.5	26.4	N.A	11.5	7.5	4
[CSBE18]	150 nm*	110	16	20	29.5	26[#]	13	6.4	8
[CB22b]	250 nm◇	114	18	8.5	17.6	N.A	32.7	0.024[†]	1
[GZIR23]	250 nm◇	125	24	19.8	21	20.4	24	0.61	2
[NFRB20]	250 nm◇	130	30	7	15.3	14.4	32	0.2	1
[ASF+21]	250 nm◇	131	20	22.8	23	21[#]	17.8	1.34	8
[LNA+23]	250 nm◇	135	32	14	19.2	14.5	30.4	0.59	1
[GUR19]	250 nm◇	135	35	27.8	24	20	7	1.9	2
[GURT22]	250 nm◇	160	82	32	24	19.7	15.7	1.26	4

[a] Technology: ◇InP, *GaN, △CMOS
§ number of power combining
# graphical estimation
† core area only

3 Low-Noise SiGe Amplifiers at D-Band

3.1 Introduction

Designing RX channels that ensure high SNR levels is essential for successful reception. The SNR performance of RX channels is heavily dependent on the noise and gain performances of the first amplification stage. To illustrate this, consider an N cascaded stages RX channel shown in Fig. 3.1. The overall noise-factor (F) and gain of the cascaded system are given by Friis' formulas, in (3.1) and (3.2), where $G_{\mathrm{a},N}$ is the available power gain and F_N is the noise-factor, both associated with the N_{th} stage in the chain. Lastly, P_N represents the input referred 1 dB compression-point of each stage. The compression behavior of the cascaded stages will be discussed in Section 4.2.

$$F_{\mathrm{total}} = F_1 + \frac{F_2 - 1}{G_{\mathrm{a},1}} + \ldots + \frac{F_N - 1}{G_{\mathrm{a},1} G_{\mathrm{a},2} \ldots G_{\mathrm{a},N-1}} \tag{3.1}$$

$$G_{\mathrm{total}} = G_{\mathrm{a},1} + G_{\mathrm{a},2} + \ldots + G_{\mathrm{a},N} \tag{3.2}$$

As indicated by (3.1), the noise contribution of each stage diminishes with the cumulative gain from the preceding stages in the chain. This underscores

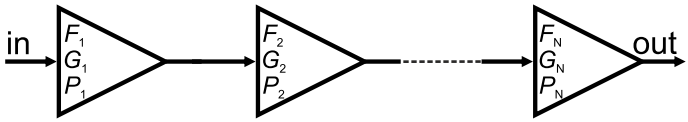


Figure 3.1: N stage RX channel with noisy cascaded stages.

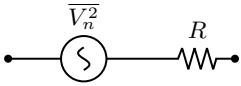


Figure 3.2: Resistor thermal noise model.

the significance of having a first-stage amplification with low noise-factor and high gain, as it mitigates the noise contribution from subsequent stages. In this regard, the utilization of LNAs as the first component at the RF path proves advantageous due to their low noise-figure and high gain.

Beyond noise considerations, additional factors come into play in RX design, including bandwidth and linearity. Overall, (3.3) and (3.4) are the equations for figure-of-merits (FoMs) used to assess LNA performances [TBG+18,AMU22].

$$\mathrm{FoM} = 1000 \cdot \frac{G \cdot \mathrm{I}P_{1\mathrm{dB}}\,[\mathrm{mW}]}{(F-1) \cdot P_{\mathrm{dc}}\,[\mathrm{mW}]} \tag{3.3}$$

$$\mathrm{FoM}_2 = 1000 \cdot \frac{G \cdot \mathrm{I}P_{1\mathrm{dB}}\,[\mathrm{mW}] \cdot B_{3\mathrm{dB}}\,[\mathrm{GHz}]}{(F-1) \cdot P_{\mathrm{dc}}\,[\mathrm{mW}] \cdot f_{\mathrm{c}}\,[\mathrm{GHz}]} \tag{3.4}$$

The primary noise sources in a BJT involve thermal noise resulting from inherent resistances at the base, emitter, and collector terminals. This type of noise is frequency-independent and can be modeled as in Fig. 3.2. The power spectral density (PSD) corresponding to this model is defined in (3.5), wherein k represents Boltzmann's constant, T denotes the absolute temperature in kelvins, and R is the resistance. Note that the PSDs expressed in this section omit the multiplication factor of Δf, as they are assumed to consistently denote the noise power within a 1 Hz bandwidth.

$$\overline{V_n^2} = 4kTR \tag{3.5}$$

Additionally, bipolar devices exhibit shot noise due to carrier transport, which can be modeled by current sources with PSDs as provided in (3.6) and (3.7), where I_{C} denotes the collector bias current and I_{B} represents the base bias current. Note that shot noise is also frequency-independent.

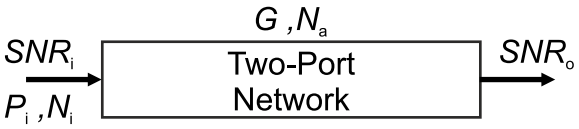


Figure 3.3: A representation of a noisy two-port network.

$$\overline{I_{n,b}^2} = 2qI_B = 2q\frac{I_C}{\beta} \tag{3.6}$$

$$\overline{I_{n,c}^2} = 2qI_C \tag{3.7}$$

Flicker noise has not been considered in this dissertation since the operating frequencies of the LNAs at focus exceed the $1/f$ flicker noise corner significantly, thus, the flicker noise does not impact the LNA performance.

It seems counter-intuitive that the noise performance of RXs worsens with the increasing frequency of operation, despite the fundamental noise sources such as thermal and shot noises are frequency-independent. However, to better understand the noise performance of any two-port network (e.g., amplifier, receiver, transistor, etc.), it is more meaningful to evaluate how SNR is impacted. Consider a noisy two-port network, as shown in Fig. 3.3. Here, G is the power gain of the network, N_a is the noise power added by the network, P_i is the input signal power, and N_i is the available noise power at the input. $\mathrm{SNR_i}$ and $\mathrm{SNR_o}$ denote the SNR values at the network's input and output, respectively.

The F of a two-port network is the ratio between the input and output SNRs, as shown in (3.8). It can be seen that F depends on the added noise power, the network's gain and the available noise power at the input. Assuming a fixed available and added noise power, a higher gain network yields a better F, translating to a better NF since NF is the logarithmic representation of F. However, as demonstrated in Fig. 2.2, the MAG of any two-port network formed by active devices diminishes with increasing frequency of operation. This reduction in gain primarily contributes to the deterioration of the overall noise performance at higher frequencies.

$$F = \frac{\mathrm{SNR_i}}{\mathrm{SNR_o}} = \frac{\mathrm{SNR_i}}{\frac{GP_i}{N_a+GN_i}} = \frac{\frac{P_i}{N_i}}{\frac{GP_i}{N_a+GN_i}} = 1 + \frac{N_a}{GN_i} \tag{3.8}$$

Fig. 3.4 illustrates the general design flow of mm-wave LNAs. The process begins with schematic level simulations to establish bias conditions, primarily focusing on collector current density. This stage involves a trade-off between minimizing the minimum noise figure ($\mathrm{NF_{min}}$), the minimum achievable NF when the device is presented with the optimum noise impedance, and optimizing the peak f_T/f_{MAX} performance to maximize MAG. Once the collector current density is determined, transistor sizing adjusts the optimum noise impedance (S_{opt}), the impedance that leads to $\mathrm{NF_{min}}$, for simpler matching network requirements. Emitter degeneration is often necessary to align the complex conjugate of S_{11} with S_{opt}, facilitating simultaneous noise and power matching.

Subsequently, the LNA core, comprising active devices and interconnects from the device terminals up to the metal layers that interface with matching networks, is laid out. Layout strategies focus on minimizing metal and via losses while reducing coupling between input and output terminals of active devices. EM modelling of the LNA core allows reevaluation of $\mathrm{NF_{min}}$; if significantly higher than schematic simulations, resizing the LNA core may simplify the layout. Otherwise, the design progresses to selection and EM modelling of matching networks. Finalization involves integrating the LNA core with EM modelled matching networks, verifying results, and routing DC connections.

This chapter covers the design, implementation and characterization of two different LNAs operating at *D*-band frequencies. Section 3.2 includes an LNA, implemented in 0.13 µm SiGe BiCMOS technology that features f_T/f_{MAX} of 300/500 GHz. Section 3.3 discusses an LNA, designed using a new generation 0.13 µm SiGe BiCMOS technology with f_T/f_{MAX} of 470/650 GHz. Section 3.4 summarizes the chapter and includes a comprehensive comparison to the SoA LNAs operating above 100 GHz.

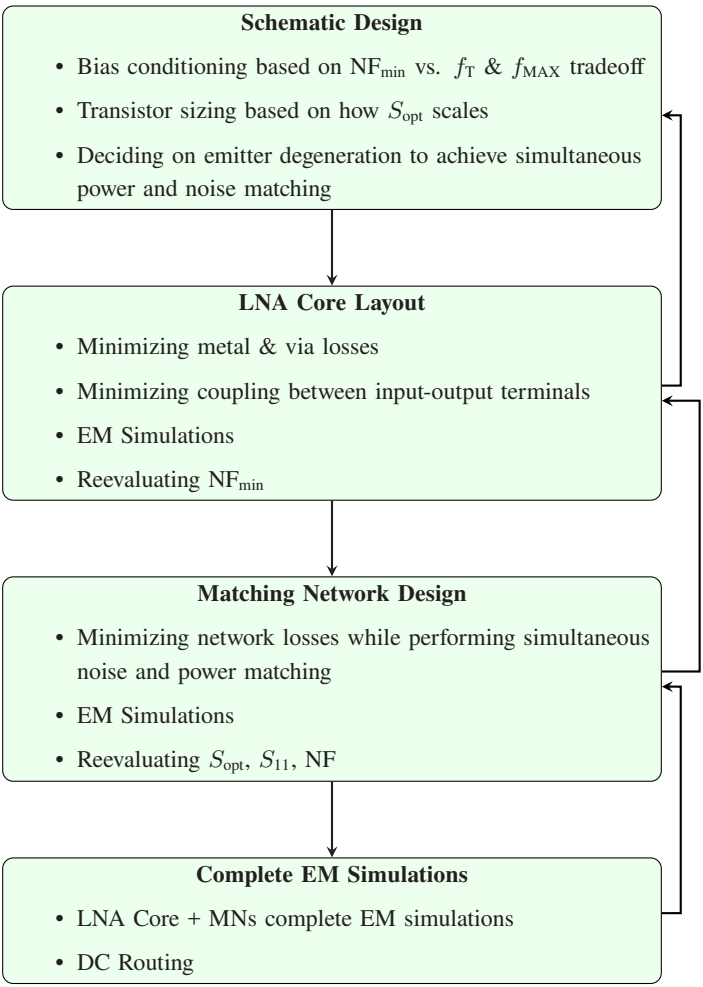


Figure 3.4: Design flow in mm-wave LNA design.

3.2 A Differential D-Band Low-Noise Amplifier in SiGe

This section includes content and material previously published in [4].

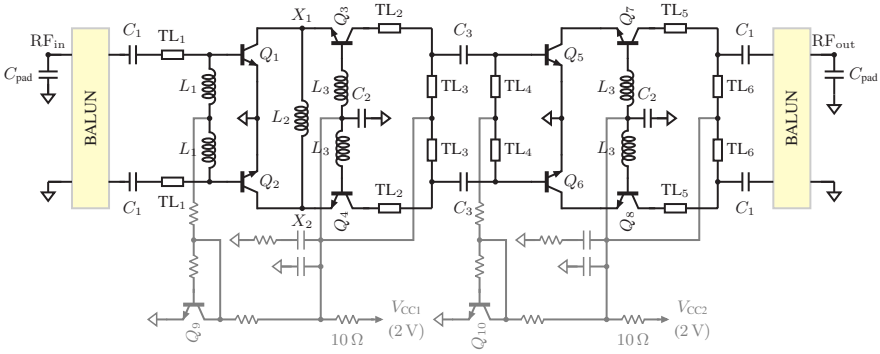
This section presents a differential two-stage cascode LNA operating in the *D*-band, using a 0.13 µm SiGe BiCMOS technology. This LNA incorporates both gain peaking and noise reduction techniques, accompanied by an interstage matching network to optimize linearity.

3.2.1 Design and Analysis

The circuit schematic of the two-stage amplifier is shown in Fig. 3.5(a), and the component values are given in Fig. 3.5(b). The convention distinguishing between a TL and an inductor is as follows: if the ground plane under the structure is cut, it is labeled as an inductor, whereas it is identified as a transmission line if the ground plane is present underneath the signal line.

The simplified circuit schematic of a cascode amplifier is depicted in Fig. 3.6(a). The noise modelling of this amplifier can be illustrated using both the small-signal equivalent circuit and noise source models, as demonstrated in Fig. 3.6(b). In this representation, $r_{n,b}$ refers to the base resistances, and $\overline{V_{n,b}^2}$ is the PSD of the thermal noise related to the base resistances. Additionally, $\overline{I_{n,c}^2}$ and $\overline{I_{n,b}^2}$ represent the PSDs of collector and base shot noises, respectively. In theory, increasing the device size leads to decreased base resistances and consequently smaller thermal noises. However, larger device sizes correspond to higher collector and base currents, resulting in larger shot noises, assuming constant current density. In the adopted technology, scaling the device size results in the same $\mathrm{NF_{min}}$, indicating that changes in thermal and shot noises due to device scaling offset each other.

As depicted in Fig. 3.4, when designing mm-wave LNAs, the initial schematic level phase involves determining the DC operating points. It is important to note that the current density flowing through the active devices of the LNA directly influences both $\mathrm{NF_{min}}$ and MAG. Depending on the chosen technology, the current density that optimizes MAG at the operational frequency might not



(a)

TL$_1$	120 µm @ 50 Ω	Q_{1-4}	$4 \times 0.07 \times 0.9\,\mu m^2$	C_1	0.7 pF
TL$_2$	110 µm @ 50 Ω	Q_{5-8}	$5 \times 0.07 \times 0.9\,\mu m^2$	C_2	1.6 pF
TL$_3$	85 µm @ 60 Ω	$Q_{9,10}$	$1 \times 0.07 \times 0.9\,\mu m^2$	C_3	1.2 pF
TL$_4$	90 µm @ 55 Ω	I_{cc1}	7 mA	L_1	65 pH
TL$_5$	80 µm @ 42 Ω	I_{cc2}	8.9 mA	L_2	120 pH
TL$_6$	50 µm @ 60 Ω	C_{pad}	17 fF	L_3	6 pH

(b)

Figure 3.5: (a) Circuit schematic of the LNA. (b) Component values. [4] © IEEE

necessarily minimize NF_{min}. In this work, a current density (J_c) of 0.78 mA is chosen, as depicted in Fig. 3.7(a), where the green strip represents the chosen value. This choice is made to minimize NF_{min} while accepting a reduction in MAG by around 2.6 dB.

In LNA design, any additional loss incurred in the input matching network contributes directly to the NF of the amplifier. Therefore, it is beneficial to choose a device size that positions the optimum noise impedance (S_{opt}), the impedance that leads to NF_{min} when the amplifier is presented with at its input, to a favorable location on Smith chart, thereby necessitating a more convenient input matching network with lower losses. This behavior is illustrated in Fig. 3.7(b). As can be seen, increasing the device size from $1 \times 900\,nm \times 70\,nm$ to $8 \times 900\,nm \times 70\,nm$ scales both S_{opt} and S_{11} and moves them towards the left part of the Smith chart. In this work, a device size of $4 \times 900\,nm \times 70\,nm$

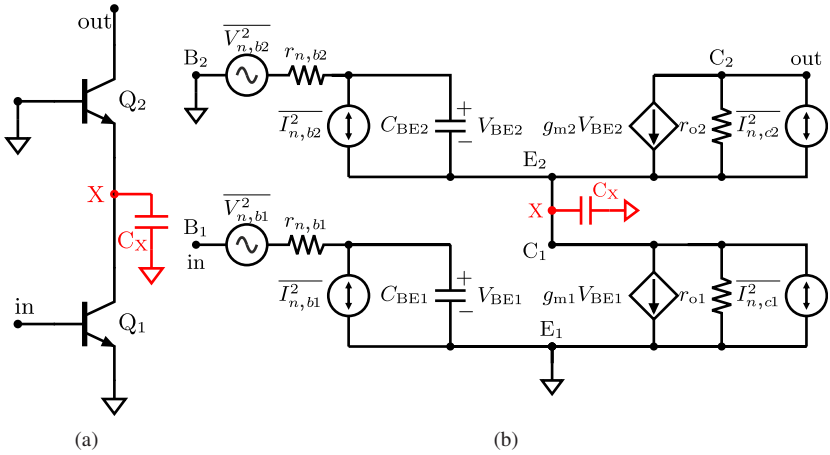


Figure 3.6: (a) Circuit schematic of a cascode amplifier. (b) Noise model of a cascode amplifier.

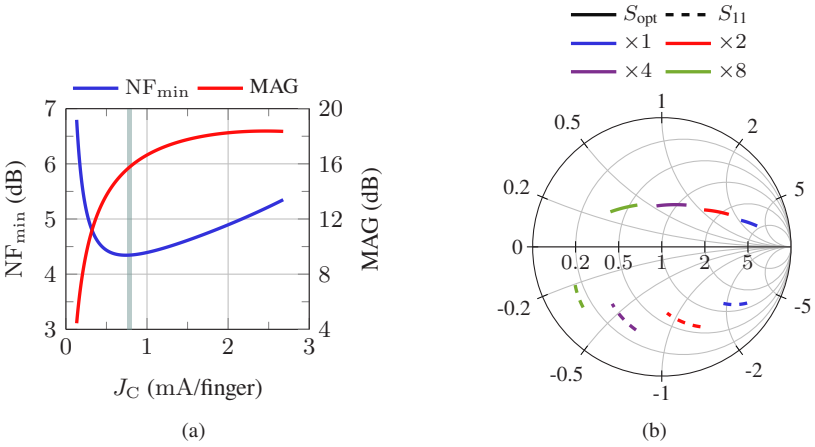


Figure 3.7: Impact of (a) J_c on NF and MAG at 140 GHz. (b) Transistor size on S_{11} and S_{opt}. [4] © IEEE

is chosen for the input stage devices that positions S_{opt} close to 50 Ω circle on Smith chart at the design frequency, indicating a low-loss input matching network.

In contrast to conventional amplifiers, the LNA design necessitates an additional consideration regarding noise. Thus, besides the power matching, achieving a simultaneous noise matching becomes crucial. To accomplish this, it is essential to position S_{opt} close to the complex conjugate of S_{11}. The schematic level S_{11} and S_{opt} curves are presented in Fig. 3.8(a) for a device size of $4 \times 900\,\text{nm} \times 70\,\text{nm}$. As expected, it can be observed that the real part of S_{11} is lower than that of S_{opt}. However, it should be noted that at these frequencies, significant parasitic effects can be introduced by the device interconnections [SUZC15]. In this design, the core layout and device interconnections have been optimized with consideration for these parasitic elements, resulting in a more suitable impedance behavior. As shown in Fig. 3.8(a), after the EM simulations of the core layout, it is observed that S_{11} and S_{opt} are positioned more favorably, allowing for simultaneous power and noise matching. On the other hand, when comparing the NF_{min} values derived from the schematic level to those obtained from the EM modeled LNA cores, as illustrated in Fig. 3.8(b), it is noticeable that the NF_{min} increases by 1 dB at the center frequency of 140 GHz due to parasitic effects introduced by the interconnections in the layout.

After recognizing the significant impact of the LNA core layout on noise performance, core layout optimization is implemented with the primary focus being the reduction of metal and via losses, particularly at the input to alleviate NF contributions from additional losses. For instance, examining the input transistor in the cascode topology reveals that the base contact of the HBT lies on the lowest metal layer, M_1, in the stack-up. This necessitates the use of a series of vias to elevate through the stack-up and access the top-most metal layer where the input matching network is realized. In terms of numerical values, the vias connecting M_1 to M_2, M_2 to M_3, and so on, demonstrate a resistivity of 9 Ω/via. This yields a cumulative resistance of 36 Ω just to reach M_5, prior to even accessing the top-most metal layer. To minimize the via-related losses, large via arrays, consisting of 20×20 vias, are implemented. By doing so the previously estimated via loss of 36 Ω can be reduced all the way down to 0.1 Ω. Furthermore, wide metal tracks are used to minimize ohmic losses. Aside from the ohmic losses, another consideration includes reducing coupling between

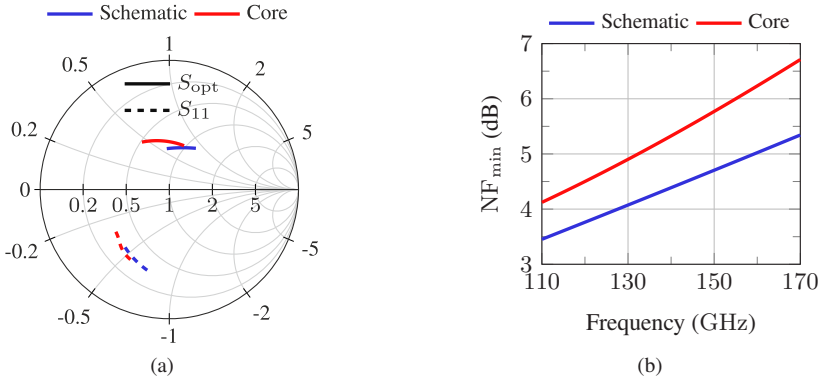


Figure 3.8: Schematic level and EM modelled LNA core (a) S_{opt} and S_{11} on Smith chart. (b) NF_{min} over frequency. [4] © IEEE

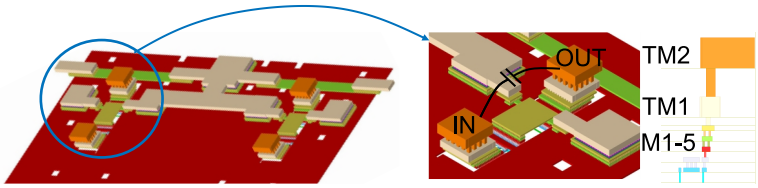
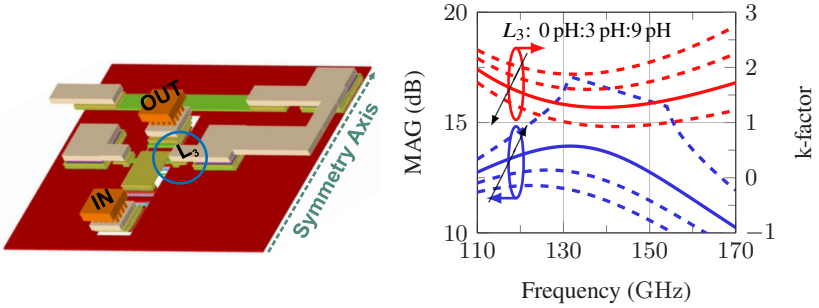


Figure 3.9: 3D view of the differential LNA core layout. [4] © IEEE

input and output terminals by adopting a stairway-based layout approach. This is especially important regarding the stability concerns. Eventually, the LNA core layouts are EM modelled to obtain more realistic results for NF_{min}, S_{opt}, and S_{11}. The differential cascode LNA core is depicted in Fig. 3.9.

Due to the limited available gain at D-band frequencies, one approach in mm-wave LNA core design is to employ a gain peaking inductance [USK+15], L_3, that is placed at the base terminal of the CB device terminals before the AC ground to enhance the MAG, as shown in Fig. 3.10(a). However, it is important to note that the base connection of the CB device is sensitive and prone to instability in the D-band frequencies. Therefore, increasing L_3 continuously poses a risk to the stability of the cascode device. This trade-off across D-band frequencies is depicted in Fig. 3.10(b). As evident from this



(a) (b)

Figure 3.10: (a) The cascode core with gain peaking inductance, L_3. (b) Impact of L_3 on MAG and k-factor over frequency. [4] © IEEE

graph, as L_3 increases, MAG improves at the cost of stability. Thus, an L_3 of 6 pH is chosen as a compromise.

As the frequency of operation increases, the parasitic capacitances at the intermediate node (collector of the CE device or emitter of the CB device) of the cascode amplifier deteriorates the overall cascode amplifier performance. This intermediate node is marked with X_1 and X_2 on the circuit schematic of the realized LNA, as shown in Fig. 3.5(a). Taking a closer look at a cascode amplifier, as depicted in Fig. 3.6(a), the parasitic capacitances associated with this node can be denoted as C_X. C_X can be approximated as expressed in (3.9).

$$C_X \approx C_{be2} + C_{cs1} \tag{3.9}$$

At lower frequency ranges, C_X presents a high impedance at the intermediate node. Therefore, the noise contribution from the CB device in cascode amplifiers is degenerated by the output impedance of the CE device (r_{o1}, as shown in Fig. 3.6(b)). Assuming a large r_{o1}, the noise contribution of the CB device becomes negligible. However, when the frequency of operation increases, the impedance that C_X presents reduces and eventually becomes comparable to r_{o1}, thereby reducing the overall equivalent impedance. Consequently, the noise contribution from the CB device becomes more pronounced, leading to

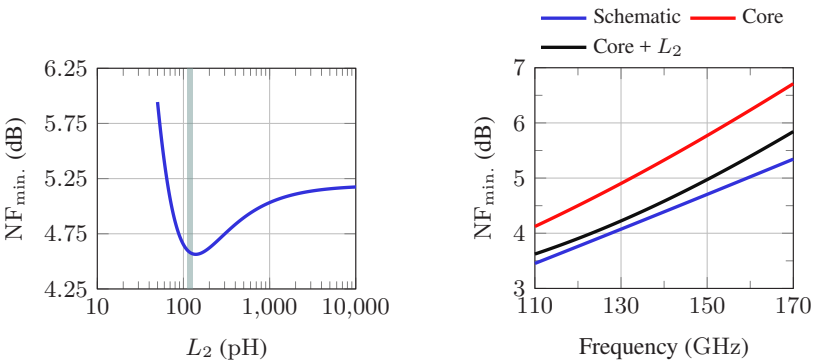


Figure 3.11: (a) Impact of the noise reduction inductance, L_2, on NF_{min} at 140 GHz. (b) The changes in NF_{min} over frequency after employing L_2 = 120 pH. [4] © IEEE

a degradation in the overall performance of the cascode amplifier. A more detailed analysis is given in [FZSS08, CL02, SRL00].

In order to nullify the impact of C_X, a noise reduction inductance (L_2 as shown in Fig. 3.5(a)) can be employed in a shunt configuration with C_X. When L_2 is selected in a way that a resonance is ensured at the frequency of operation with C_X, the noise contribution from the CB device is reduced [SRL00]. As depicted in Fig. 3.11(a), there is an optimal inductance L_2 that minimizes NF_{min}. It is important to note that arbitrarily large values of L_2 represent an open circuit condition, effectively simulating the absence of inductance. Conversely, arbitrarily small values of L_2 would lead to the differential nodes being shorted together, thereby destroying the differential operation. Choosing L_2 = 120 pH results in an NF_{min} improvement of about 0.7 dB compared to the scenario where no noise reduction inductance is adopted. Fig. 3.11(b) illustrates the simulated NF_{min} across the D-band frequency range, showing that most of the noise contributed through the core layout is compensated through the utilization of L_2.

The selection of device sizes and the co-optimization of the core layout with L_2 have allowed for the simplification of the input matching network. This simplified input matching network consists of only a single shunt element, L_1,

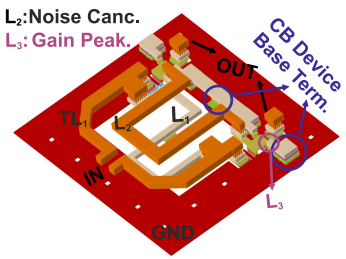


Figure 3.12: 3D view of the input stage LNA core with the input matching network. [4] © IEEE

allowing for simultaneous noise and power matching. This simplification is particularly advantageous, as any losses incurred in the input matching network would directly lead to an increase in NF_{min}. Fig. 3.12 shows the complete 3D representation of the input stage LNA core, input matching network, formed by L_1 and TL_1, and inductances, L_2 and L_3, that are employed for noise reduction and gain peaking purposes. Note that TL_1 has a characteristic impedance of $50\,\Omega$ and does not affect input matching. Its sole purpose is to serve as a connection to the input pads. To enhance the quality factor of the inductances, the ground layer beneath L_1 and L_2 is removed. The resulting positions of S_{11} and S_{opt} after the input matching network is illustrated in Fig. 3.13(a). As can be seen, both S_{11} and S_{opt} are brought close to the $50\,\Omega$ point on Smith chart, owing to the simultaneous power and noise matching. Moreover, Fig. 3.13(b) shows the change in NF_{min}, after the input matching network is implemented. The input matching network results in an increase in NF_{min} of around 0.75 dB, corresponding to the loss experienced in the input matching network. Additionally, an analysis of the magnetic coupling between L_1 and L_2 is performed and it has been found that the coupling has an adverse impact on NF_{min}. To mitigate this, L_1 and L_2 are carefully positioned with a certain offset, resulting in a low coupling factor of 0.1. This amount of coupling led to a minor 0.1 dB increase in NF_{min}.

Since a two-stage cascode design has been employed to achieve a larger gain, the interstage matching network plays an important role on linearity performance of the LNA. By adjusting the impedance levels at the interstage, the voltage gain of the first stage and the second stage are regulated in a way that the second

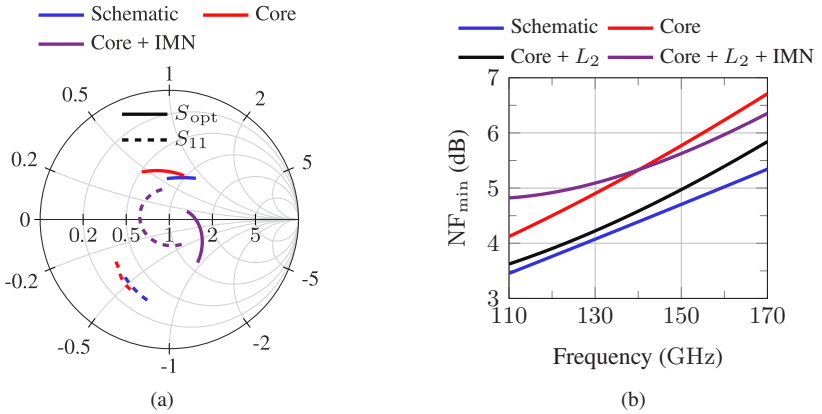


Figure 3.13: Impact of input matching network on (a) S_{opt} and S_{11} on Smith chart. (b) NF_{min} over frequency. [4] © IEEE

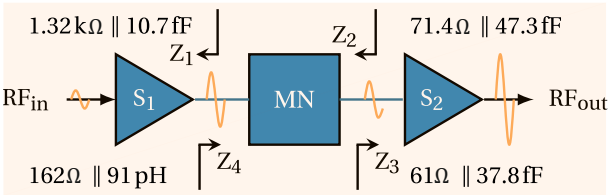


Figure 3.14: Impedances at the interstage. [4] © IEEE

stage is prevented from saturating. Fig. 3.14 depicts these relative impedance levels and offers insights into voltage swings.

The first stage is loaded with $Z_4 = 162\,\Omega \parallel 91\,\text{pH}$, tuning the gain of the first stage to 10 dB. Note that the output of the first stage is not terminated with the complex conjugate of Z_1. Concurrently, the input of the second stage is presented with $Z_2 = 71.4\,\Omega \parallel 47.3\,\text{fF}$. Due to this impedance transformation, the voltage swing at the input of the second stage is approximately halved. This results in simultaneous compression behavior within both the first and second stages for a boosted linearity, instead of a dominating compression behavior of the second stage.

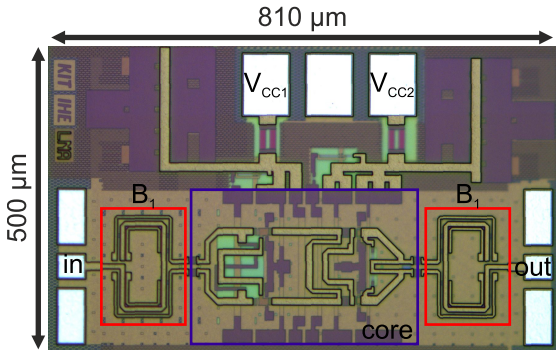


Figure 3.15: Chip micrograph of the fabricated LNA with total chip area (0.81 mm × 0.5 mm) and LNA core dimensions (0.36 mm × 0.28 mm). [4] © IEEE

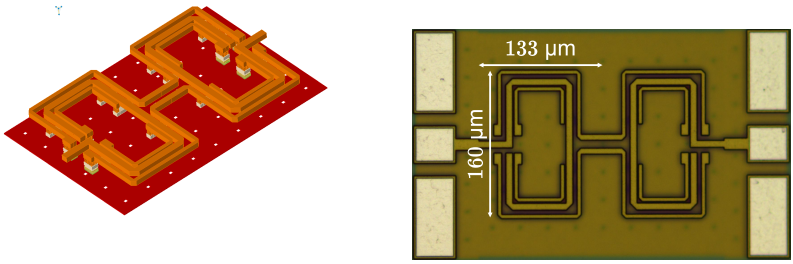
3.2.2 Characterization

The fabricated chip micrograph is shown in Fig. 3.15. The LNA measures 0.81 mm × 0.5 mm, including the pads while the LNA core has dimensions of 0.36 mm × 0.28 mm, occupying 0.1 mm^2.

The differential LNA employs marchand balanced-unbalanced units (baluns), B_1 referring to Fig. 3.15, to facilitate single ended on-wafer probing during measurements. Since they are not parts of the differential LNA, the balun is also taped out in back-to-back configuration and characterized separately. A 3D image of the back-to-back baluns is displayed in Fig. 3.16(a) and the chip micrograph is shown in Fig. 3.16(b). A single balun measures 0.13 mm × 0.16 mm.

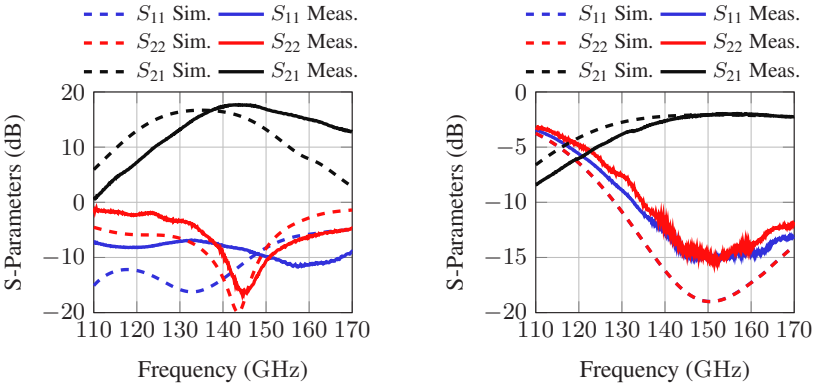
The small-signal S-parameter characterization of the fabricated LNA and the back-to-back baluns are conducted using a PNA-X network analyzer connected to a pair of *D*-band frequency extension modules, as illustrated in Fig. 2.14(a). The simulated and measured small-signal behaviors of the LNA are shown in Fig. 3.17(a). At 140 GHz, the measured small-signal gain is 17.4 dB, with a B_{3dB} spanning 31 GHz, ranging from 132 GHz to 163 GHz (≈ 22.1 % of relative bandwidth).

Fig. 3.17(b) displays the measured and simulated S-parameters of the back-to-back baluns. The insertion loss of the back-to-back structure is measured to be



(a) (b)

Figure 3.16: Back-to-back baluns (a) 3D layout image. (b) Chip micrograph. [4]. © IEEE



(a) (b)

Figure 3.17: Small-signal S-parameters of the (a) LNA with the integrated back-to-back baluns. (b) Back-to-back baluns. [4] © IEEE

2.6 dB at 140 GHz. A scalar de-embedding is performed at the input and output terminals of the LNA in order to extract the differential circuit performance.

The measurement setup shown in Fig. 2.15 is used for the large-signal characterization. Fig. 3.18(a) illustrates P_{out} and gain behavior with varying P_{in}. At 140 GHz, the measured input-referred 1 dB compression-point ($IP_{1\text{dB}}$) is −18.4 dBm. After de-embedding the insertion losses of the input and output

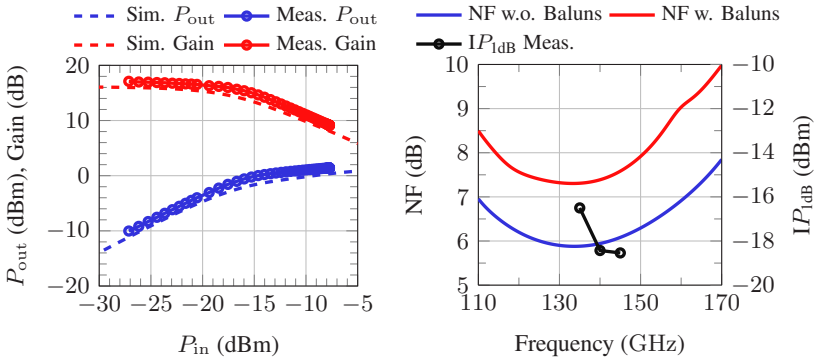


Figure 3.18: (a) Measured large-signal parameters of the LNA with varying P_{in}. (b) Simulated NF performance with and without the baluns, and compression behavior with frequency. [4] © IEEE

baluns, the IP_{1dB} at the same frequency is determined to be −19.8 dBm. Fig. 3.18(b) shows the measured IP_{1dB} behavior, including the baluns, across the frequency range of 135 GHz to 145 GHz.

NF measurements could not be performed due to the unavailability of suitable measurement equipment. However, Fig. 3.18(b) presents simulated NF values both with and without the baluns. As anticipated, at 140 GHz, the NF exhibits a difference that is equal to the insertion loss of the input balun between the scenarios, one with the baluns included and the other without them. According to the simulations, the NF without the baluns remains below 6 dB between 124.8 GHz and 142.1 GHz, and stays below 8 dB across the entire *D*-band. A NF of 5.9 dB is achieved at 140 GHz.

3.2.3 Conclusion

A differential *D*-band LNA is presented. The LNA exhibits a simulated NF of 5.9 dB and a measured gain of 20 dB at 140 GHz. The proposed amplifier attains an IP_{1dB} of −19.7 dBm while consuming a total power of 31.8 mW

from a 2 V supply. The entire chip occupies an area of 0.4 mm^2, inclusive of the pads, with the core accounting for 0.1 mm^2.

A comparison of the performance parameters to the SoA is illustrated in Fig. 3.31 and listed in Table 3.1 and Table 3.2. The LNA demonstrates one of the best FoMs among the Si based LNAs operating at above 100 GHz, primarily owing to the high $G \times IP_{1dB}$ product, achieved while maintaining a moderate DC power consumption and a moderate NF.

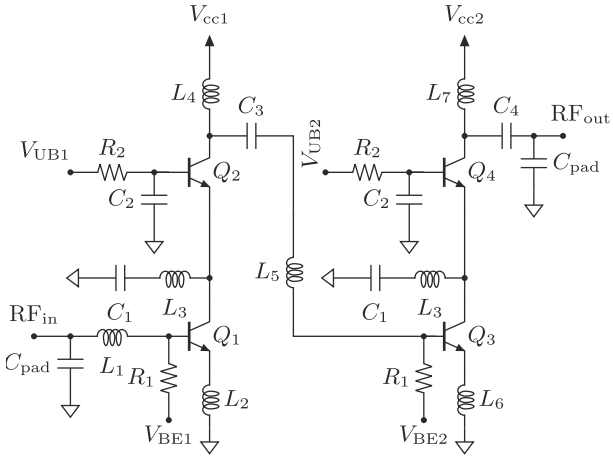
3.3 A D-Band LNA in an Advanced 130-nm SiGe

This section presents a two-stage cascode LNA operating in the *D*-band, using a latest generation 130 nm SiGe BiCMOS technology with f_T/f_{MAX} of 470/650 GHz. The LNA utilizes the same noise reduction technique introduced in Section 3.2. Additionally, the performance of the realized LNA is compared to that of the LNA implemented in the previous SiGe BiCMOS technology in terms of MAG and noise performance.

3.3.1 Design and Analysis

The simplified circuit schematic of the LNA is shown in Fig. 3.19(a), with corresponding component values listed in Fig. 3.19(b). The transistors Q_{1-4} each have 4 emitter fingers, resulting in an emitter area of $4 \times 0.07 \times 0.9\ \mu m^2$. A two-stage single-ended cascode topology is used. Note that while the LNA discussed in Section 3.2 employs a differential topology, this particular LNA does not use the differential configuration. The motivation behind this decision is to avoid the ambiguity introduced by the marchand baluns positioned at the inputs and outputs.

To compare the performance of the previous SG13G2 technology to the SG13G3 technology employed in this design, the NF_{min} and MAG have been plotted against J_c at 140 GHz for a single-stage cascode amplifier. These plots are shown in Fig. 3.20(a). After identifying the optimal current densities that minimize NF_{min}, the corresponding NF_{min} and MAG values for each technology are presented in Fig. 3.20(b) at 140 GHz. The MAG at this optimal current density is known as associated gain. As evident, the SG13G3 tech-



(a)

C_{pad}	17 fF
L_1	78 pH
L_2	35 pH
L_3	80 pH
L_4	56 pH
L_5	8 pH
L_6	20 pH
L_7	56 pH
$Q_{1,2}$	×4
$Q_{3,4}$	×4
C_1	0.5 pF
C_2	1.2 pF
C_3	26 fF
C_4	23 fF
R_1	6 kΩ
R_2	2 kΩ

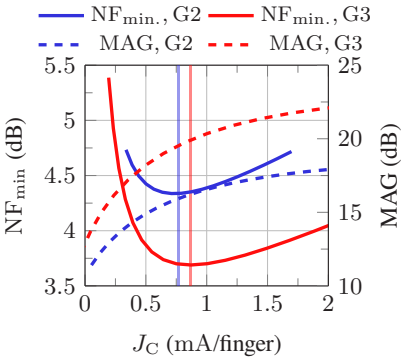
(b)

Figure 3.19: (a) Simplified circuit schematic of the two-stage LNA. (b) Values of the schematic components.

nology exhibits a 0.6 dB reduction in NF_{min} while achieving a 4 dB boost in MAG compared to SG13G2. This improvement in MAG is attributed to the enhanced f_{MAX}, while the reduced NF_{min} stems from the improved device parasitic resistances as well as the enhanced f_{MAX}.

After determining the optimum current density (J_c = 0.85 mA/finger) that minimizes NF_{min}, the device size of the first stage of the LNA transistors is scaled to bring S_{opt} closer to the 50 Ω circle on Smith chart. The impact of this device scaling on S_{11} and S_{opt} is illustrated in Fig. 3.21. As a result of this analysis, a device size of $4 \times 900\,nm \times 70\,nm$ is selected and the resulting S_{opt} and S_{11} are found to be 38 + j15 Ω and 23 - j10 Ω, respectively.

The LNA core layout is shown in Fig. 3.22(a) with the marked base, emitter and collector terminals. B_1, E_1 and C_1 are the device terminals of the CE device in the cascode topology, while B_2, E_2 and C_2 represent the device terminals of the CB device. For reference regarding the naming and coloration of metal



(a)

@ 140 GHz	SG13G2	SG13G3
NF$_{min.}$ (dB)	4.3	3.7
MAG (dB)	15.7	19.7

(b)

Figure 3.20: Simulated performance comparison of schematic level cascode LNAs in SG13G2 and SG13G3 in terms of (a) NF$_{min}$ and MAG vs. J_c at 140 GHz. (b) NF$_{min}$ and MAG at the individually optimized current densities.

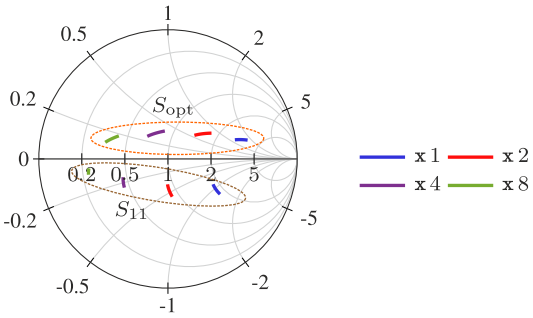
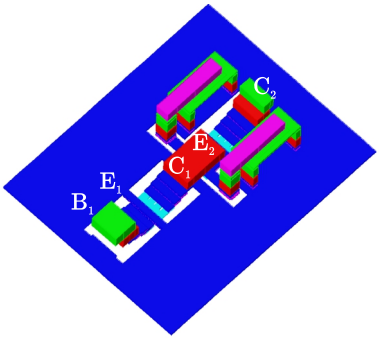
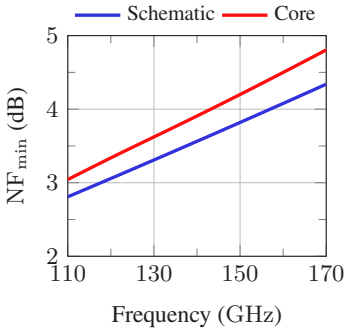


Figure 3.21: The impact of device scaling on S_{11} and S_{opt}.



(a)



(b)

Figure 3.22: (a) A 3D representation of the input stage core layout. (b) NF_{min} vs. frequency for schematic level and EM modelled input stage LNA core.

layers, refer to the stack-up depicted in Fig. 2.31(a). The resulting NF_{min} over frequency for the schematic level and EM modelled input stage LNA core are shown in Fig. 3.22(b). An increase of NF_{min} as low as 0.4 dB is observed after the EM modeling of the LNA core, thanks to the layout strategy aiming to minimize ohmic losses over metal layers and vias.

As explained in Section 3.2.1, a noise reduction inductance can be integrated in a shunt configuration at the intermediate node of CE and CB devices within the cascode topology to achieve resonance at the frequency of operation. Fig. 3.23(a) illustrates that an optimal inductance L_3 exists that minimizes NF_{min}. By selecting $L_3 = 80$ pH, an NF_{min} improvement of approximately 0.7 dB is achieved compared to the case without the integration of noise reduction inductance. Fig. 3.23(b) demonstrates the simulated NF_{min} across the D-band frequency range, indicating that the majority of noise introduced through the core layout is mitigated with the incorporation of L_3.

In order to facilitate a simultaneous power and noise matching, an inductive emitter degeneration technique is adopted. Including the emitter degeneration inductance raises the real part of the input impedance, moving the S_{11} to the left on Smith chart, while having minimal impact on S_{opt}. It can be seen how the input impedance of a metal-oxide-semiconductor field-effect transistor (MOSFET) changes with the inductive emitter degeneration as derived

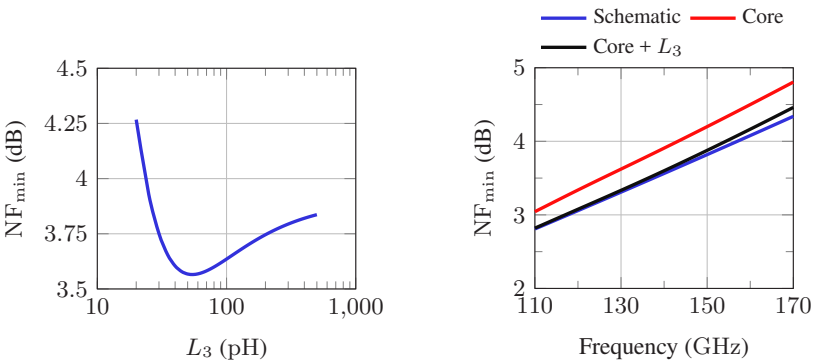


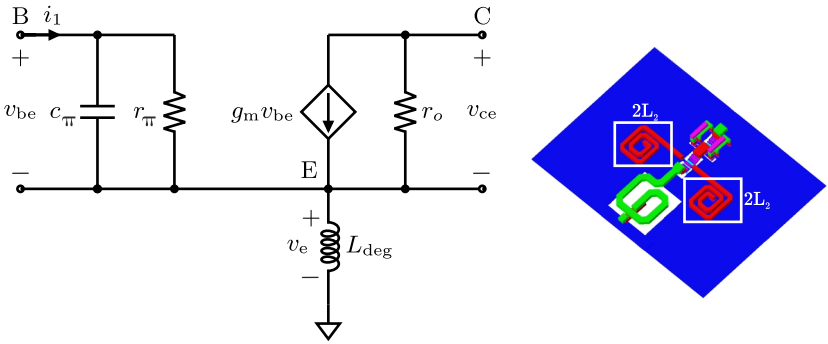
Figure 3.23: (a) Impact of the noise reduction inductance, L_3, on NF_{min} at 140 GHz. (b) The changes in NF_{min} over frequency after employing $L_3 = 80$ pH.

in [Voi13]. The same analysis can be repeated for a single HBT in CE configuration using the small-signal equivalent circuit, shown in Fig. 3.24(a). Note that C_{cb} and C_{ce} are neglected for the sake of simplicity.

Referring to the small-signal equivalent circuit depicted in Fig. 3.24(a), (3.10) expresses the input impedance, Z_{in}, the input current, i_1, and the voltage over the degeneration inductance, v_e.

$$\begin{aligned} Z_{in} &= \frac{v_{be} + v_e}{i_1} \\ i_1 &= \frac{v_{be}}{r_\pi + \frac{1}{j\omega C_\pi}} \\ v_e &= (i_1 + g_m v_{be}) j\omega L_{deg} \end{aligned} \tag{3.10}$$

After substituting i_1 into v_e and Z_{in}, a new expression for Z_{in} can be obtained, as represented in (3.11).



(a) (b)

Figure 3.24: (a) Small-signal equivalent circuit of a HBT. (b) 3D representation of the inductive emitter degeneration.

$$
\begin{aligned}
Z_{in} &= \frac{v_{be} + j\omega L_{deg}\left(g_m v_{be} + \frac{v_{be} j\omega C_\pi}{1+j\omega C_\pi r_\pi}\right)}{\frac{v_{be} j\omega C_\pi}{1+j\omega C_\pi r_\pi}} \\
&= \frac{1+j\omega C_\pi r_\pi}{v_{be} j\omega C_\pi}\left[v_{be} + g_m v_{be} j\omega L_{deg} + \frac{j\omega L_{deg} v_{be} j\omega C_\pi}{1+j\omega C_\pi r_\pi}\right] \\
&= \frac{1+j\omega C_\pi r_\pi}{j\omega C_\pi}\frac{(1+j\omega C_\pi r_\pi)\, g_m L_{deg}}{C_\pi} + j\omega L_{deg}
\end{aligned}
\tag{3.11}
$$

After further simplifications, (3.12) can be obtained. Finally, the real part of Z_{in} can be extracted, as expressed in (3.13). As can be seen, the real part of the input impedance increases with the raising degeneration inductance values.

$$
Z_{in} = r_\pi + \frac{g_m L_{deg}}{C_\pi} + j\omega\left(r_\pi + L_{deg} - \frac{1}{\omega^2 C_\pi}\right) \tag{3.12}
$$

$$
\Re(Z_{in}) = r_\pi + \frac{g_m L_{deg}}{C_\pi} \tag{3.13}
$$

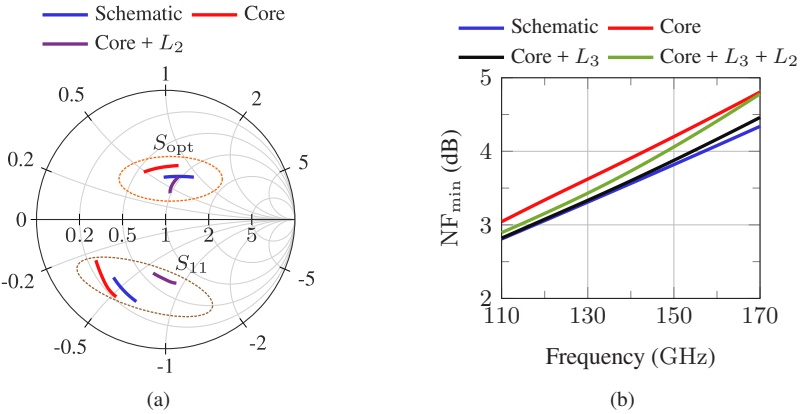
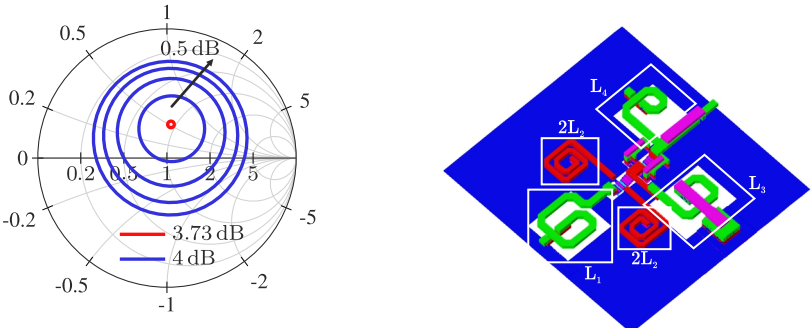


Figure 3.25: (a) Small-signal equivalent circuit of a HBT. (b) The changes in NF_{min} over frequency after employing $L_2 = 35$ pH.

In this work, an emitter degeneration inductance of 35 pH is selected and the layout implementation is illustrated in Fig. 3.24(b). The emitter degeneration inductance is realized by connecting two inductors in parallel, each with twice the desired inductance value, at the emitter node of the CE amplifier to maintain symmetry. The resulting locations of S_{11} and S_{opt} after the emitter degeneration are illustrated in Fig. 3.25(a). As expected, with the increase in the real component of the input impedance due to emitter degeneration, the S_{11} curve shifts rightward on the Smith chart, while the changes in S_{opt} are comparatively minor. The slight change in S_{opt} can be attributed to the finite quality factor (Q) of the degeneration inductance and associated parasitics. Fig. 3.25(b) illustrates the change in NF_{min} after introducing the emitter degeneration inductance, resulting in a 0.15 dB increase in NF_{min}.

Prior to designing the input matching network, the noise circles are depicted on the Smith Chart, as illustrated in Fig. 3.26(a). The red circle denotes $S_{opt} = 48 + j25\,\Omega$, yielding in NF_{min} of 3.73 dB. Meanwhile, the blue circles represent impedance values corresponding to NF values starting at 4 dB, with increments of 0.5 dB. The input matching network is composed of a series inductance, $L_1 = 78$ pH with a Q of 22 and the assumed pad capacitance of 17 fF. After the input matching network is implemented, the design proceeds



(a) (b)

Figure 3.26: (a) Noise circles of the input stage LNA core. (b) 3D representation of the input stage core layout, L_1, L_2, L_3 and L_4 inductances.

with the interstage and output matching networks, which implement complex conjugate matching strategy. The complete input stage core layout, L_1, L_2, L_3 and L_4 inductances are illustrated in Fig. 3.26(b).

The second stage of the LNA is implemented to increase the overall gain. The device sizing is the same as in the first stage and the second stage devices has a slightly higher collector current density for improved gain performance. To further understand the impact of total currents of first and second stages, I_{cc1} and I_{cc2}, on NF, gain and the resulting FoM, the following contour plots are generated at 135 GHz, as shown in Fig. 3.27. At the end, choosing an I_{cc1} of 3 mA and I_{cc2} of 3.5 mA results in a gain of 20.6 dB and an NF of 4.6 dB, demonstrating the highest FoM. The supply voltages, V_{cc1} and V_{cc2}, are set at 2 V, leading to a total power consumption of 13 mW.

3.3.2 Simulation Results

The chip layout of the LNA is shown in Fig. 3.28. The LNA core occupies a compact area of 0.075 mm^2, measuring 0.3 mm $\times$ 0.25 mm. The implementation of emitter degeneration enables simultaneous noise and power matching. The simulated small-signal S-parameters are depicted in Fig. 3.29(a), showing that S_{21} reaches a peak of 20.6 dB at 135 GHz. Across the D-band, S_{11}

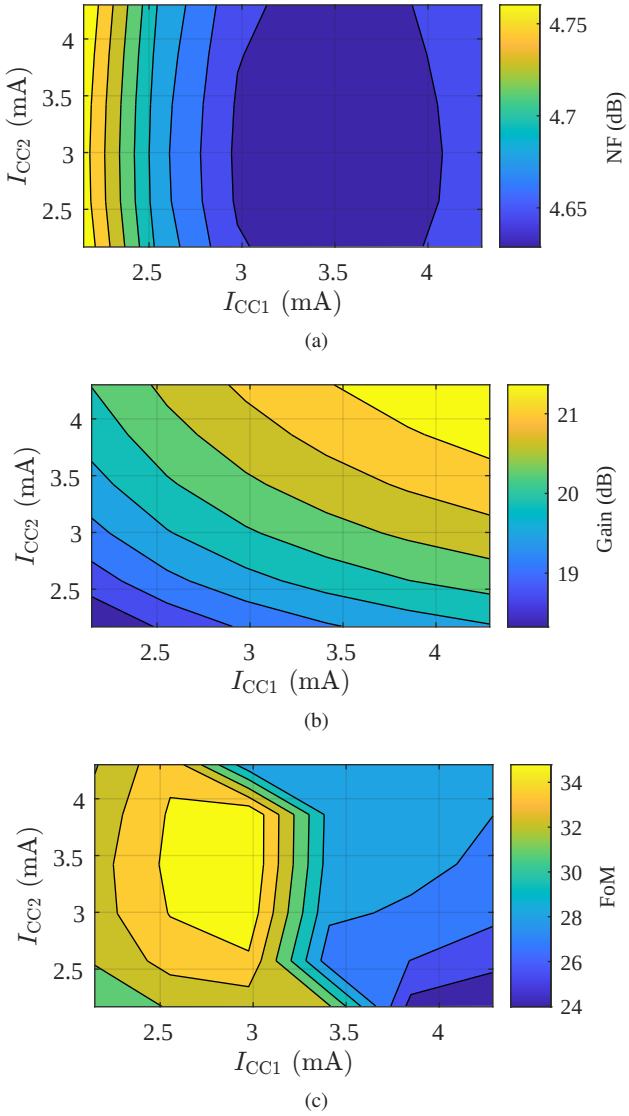


Figure 3.27: Simulated dependency of (a) NF on I_{cc1} and I_{cc2}. (b) Gain on I_{cc1} and I_{cc2}. (c) FoM on I_{cc1} and I_{cc2}.

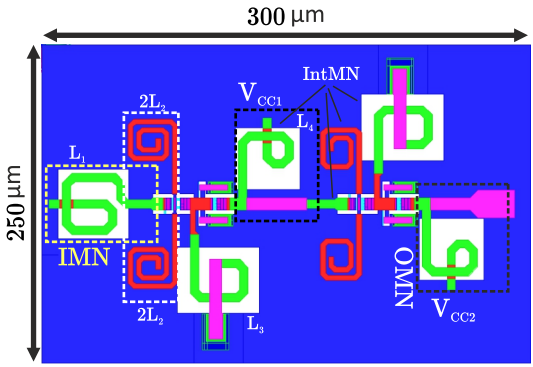


Figure 3.28: Chip layout of the LNA.

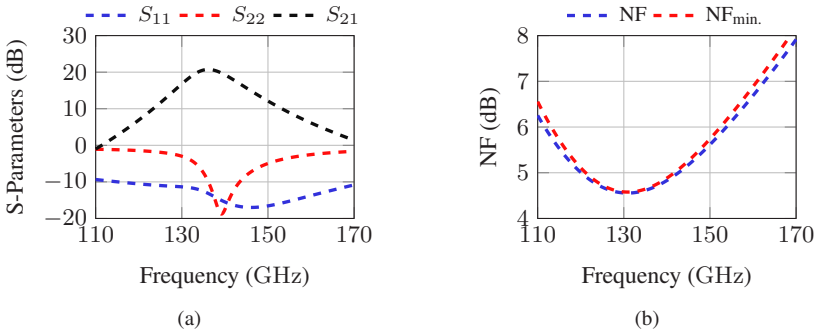


Figure 3.29: Simulated (a) Small-signal S-parameters. (b) NF and NF_{min}.

maintains a relatively flat profile, consistently remaining below −10 dB. Fig. 3.29(b) illustrates the variation of NF and NF_{min} with frequency. At 135 GHz, the difference between NF and NF_{min} is less than 0.1 dB, indicating an excellent noise matching. This close matching in noise extends across the entire *D*-band, preserving a flat profile with minimal differences between NF and NF_{min}.

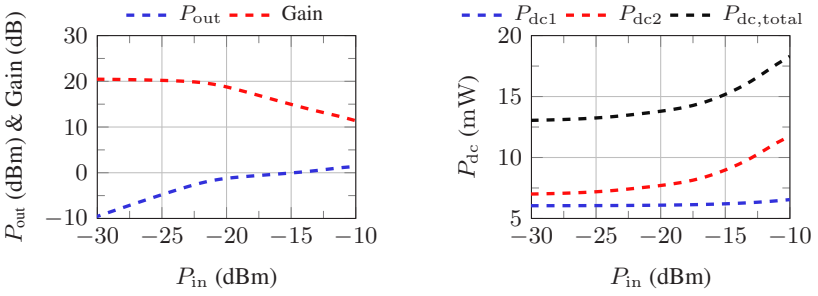


Figure 3.30: Simulated (c) P_{out} and Gain vs. P_{in} at 135 GHz. (d) Corresponding P_{dc} of first and second LNA stages and total P_{dc} vs. P_{in}.

The simulated large-signal performance parameters are illustrated in Fig. 3.30(a). At 135 GHz, an IP_{1dB} of −21.5 dBm is achieved, corresponding to an OP_{1dB} of −2 dBm. The P_{dc} vs. P_{in} is also depicted in Fig. 3.30(b).

3.3.3 Conclusion

A *D*-band LNA in an advanced SiGe technology is presented. At 135 GHz, the small-signal gain is simulated to be 20.6 dB with a B_{3dB} of 13 GHz. Moreover, the LNA demonstrates a simulated NF of 4.6 dB and exhibits an IP_{1dB} of −21.5 dBm. The core of the amplifier occupies 0.08 mm^2. The LNA consumes a total DC power of 13 mW from a 2 V supply. The LNA core occupies an IC area as compact as 0.075 mm^2. Additionally, a performance comparison between the SG13G2 and SG13G3 technologies is demonstrated, providing an analysis of the impact of technology on mm-wave LNA performances.

A comparison of the simulated performance parameters with SoA is illustrated in Fig. 3.31, accompanied by Table 3.1 and Table 3.2. As far as the simulation results are considered, the LNA demonstrates the best FoM among the Si based LNAs operating at above 100 GHz.

3.4 Summary and Performance Comparisons

This chapter has explained SiGe-based *D*-band LNAs, presenting two distinct LNA designs. It thoroughly examines the design methodology and strategies employed in mm-wave LNAs. Moreover, this section incorporates a comprehensive literature review, outlining the SoA LNAs operating above 100 GHz and implemented in SiGe, CMOS and III-V technologies. Fig. 3.31 provides a detailed comparison of SoA LNAs based on operating frequency, NF, gain, OP_{1dB}, and FoM. The outlined SiGe-based LNAs are further elaborated in Table 3.1, while Table 3.2 includes LNAs implemented in CMOS and III-V technologies.

The LNA discussed in Section 3.2 is denoted by the color red. The LNA detailed in Section 3.3 is represented by the color purple.

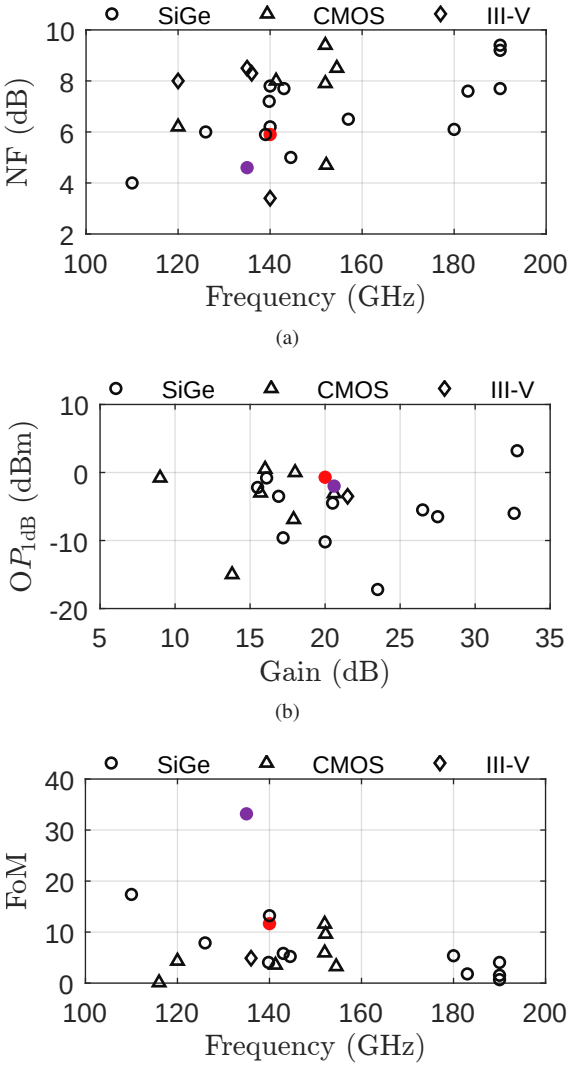


Figure 3.31: SoA LNAs above 100 GHz demonstrated in various processes (a) Frequency and NF. (b) Gain and OP_{1dB}. (c) Frequency and FoM.

Table 3.1: SoA LNAs above 100 GHz in SiGe technologies.

Ref.	Tech.[a]	Freq. (GHz)	B_{3dB} (GHz)	Gain (dB)	NF (dB)	IP_{1dB} (dBm)	Area (mm^2)	P_{dc} (mW)	FoM	FoM2
[MRC23]	90 nm*	140	37.6	26.5	7.2	-31	0.69	20.6	4.05	1.1
[MTB23]	130 nm*	180	80	15.5	6.1	-16.7	0.48	46	5.37	2.38
[TBG+18]	130 nm*	144.5	52	32.6	5	-37.6	1	28	5.22	1.88
[YSE15]	90 nm*	140	28	30	6.2	n.a	0.53	45	n.a	n.a
[USK+15]	130 nm*	126	17#	27.5	6	-33&	0.39	12	7.88	1.06
[CUS+16]	130 nm*	183	35	17.2	7.6	-25.8	0.77	16.1	1.8	0.35
[ZLJ+20]	130 nm*	190	34	23.5	7.7&	-39.7	1.05	3.2	1.53	0.27
[SFCE17]	130 nm*	190	20	20	9.2&	-29.2	0.48	24.2	0.68	0.07
[AMU22]§	130 nm*	140	31	20	5.9&	-19.7	0.1†	31.8	11.66	2.58
[AMU22]‖	130 nm*	140	31	17.4	7.4&	-18.4	0.1†	31.8	5.55	1.23
[HRP+19]	130 nm*	143	32#	16.1	7.7	-15.9&	0.1†	36.8	5.82	1.3
[UTC+18]	130 nm*	139	44	25.3	5.9	n.a	n.a	0.56	30	n.a
[MPK+21]	130 nm*	157	55	20.5	6.5	n.a	n.a	0.1	50	n.a
[UKV+13]	130 nm*	110	20	20.5	4	-24&	0.41	17	17.38	3.16
[AHKW18]	130 nm*	140	23.2	32.8	7.8&	-28.6	0.07†	39.6	13.22	2.19
[FCE14]	130 nm*	190	44	16.9	9.4&	-19.4	n.a	18	4.05	0.94
Section 3.3&	130 nm*	135	13	20.6	4.6	-21.5	0.075†	13	33.2	3.2

[a] Technology: * SiGe
† core area only
# graphical estimation
& simulated
§w. baluns deembedded
‖ w.o. baluns deembedded

Table 3.2: SoA LNAs above 100 GHz in CMOS and III-V technologies.

Ref.	Tech.[a]	Freq. (GHz)	B_{3dB} (GHz)	Gain (dB)	NF (dB)	IP_{1dB} (dBm)	Area (mm^2)	P_{dc} (mW)	FoM	FoM2
[YPM+21]	65 nm*	152.2	11	17.9	4.7	-23.8	0.19	13.7	9.62	0.69
[PVK+18]	28 nm*	154.5	23	15.7	8.5	-17.7	0.34†	32	3.24	0.48
[HSB+20]	45 nm*	141.3	31.5	16	8	-14.5	0.07†	75	3.55	0.79
[FSAR19]	22 nm*	135	44	16	8.5&	n.a	0.09†	44	n.a	n.a
[TNM+21b]	22 nm*	136#	13.5#	21.5	8.3	-24	0.03†	20	4.88	0.48
[ALH+23]	22 nm*	152	11	9	7.9	-8.8	0.09†	17.5	11.58	0.84
[ALH+23]	22 nm*	152	11	18	9.4	-17	0.09†	27.5	5.94	0.43
[KKR17]	65 nm*	116	11	13.8	10.8	-27.8	0.6	40	0.09	0.01
[JJK+20]	40 nm*	120	40.6	20.6	6.2	-22.7	0.22	45	4.32	1.46
[WML17]	50 nm§	140	67	30.8	3.4	n.a	1.5	57.6	n.a	n.a

[a] Technology: * CMOS § III-V † core area only
graphical estimation & simulated

4 An Integrated Differential D-Band I/Q Transceiver in SiGe

This chapter includes content and material previously published in [2], [9], and [13].

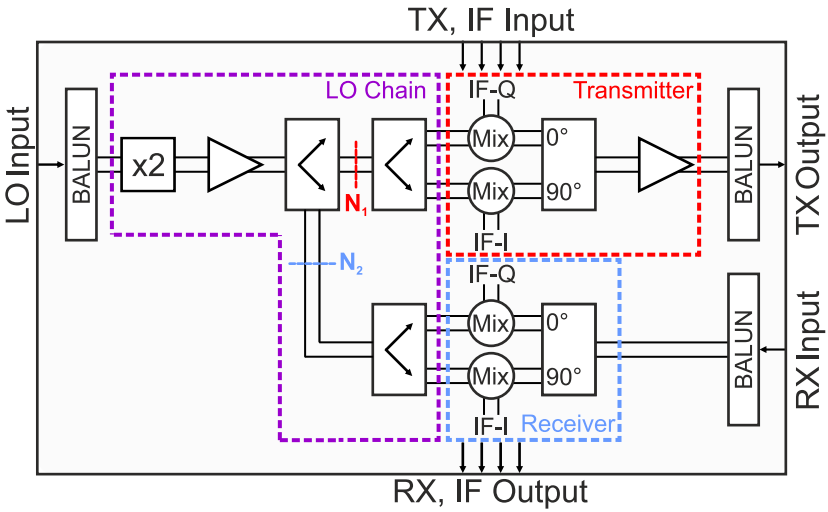
4.1 Introduction

This chapter investigates the design, implementation, and characterization of a *D*-band I/Q TRX chip, implemented in a 0.13 µm SiGe BiCMOS technology.

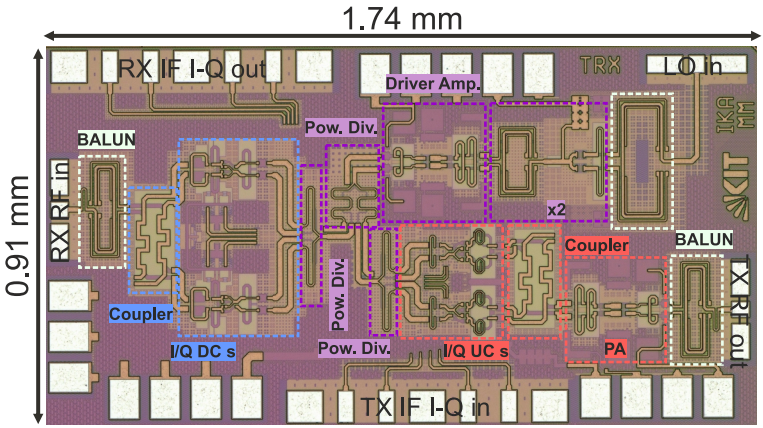
4.2 Transceiver Architecture

The TRX comprises various components, including an LO core with a frequency doubler (x2), a driver amplifier, and power dividers. The TX core consists of I/Q upconversion mixers, a power amplifier, and a hybrid coupler. The RX core employs an active mixer-first design, featuring I/Q downconversion mixers and a hybrid coupler. The complete block diagram of the implemented TRX is depicted in Fig. 4.1(a), while the chip micrograph is illustrated in Figure 4.1(b).

Most of the *D*-band TRXs reported in literature commonly incorporate a RX channel with an LNA as the first component in the RF path. This approach offers a distinct advantage, considering the excellent noise performance characteristic of LNAs. For instance, at *D*-band frequencies, Si LNAs with a NF of lower than 6 dB and a gain of around 20 dB have been presented, as demonstrated in Section 3.2 and Section 3.3. This implies that subsequent blocks in the RX channel have less stringent NF requirements, as explained through Friis' formulas in (3.1). While acknowledging these benefits, it is essential to



(a)



(b)

Figure 4.1: I/Q TRX (a) Block diagram. (b) Chip micrograph.

understand that LNAs also suppress the IP_{1dB} of following blocks. In reference to Fig. 3.1, (4.1) illustrates the linearity performance of the cascaded chain in terms of the input third-order intercept point (II$P3$), as given in [Voi13]. II$P3_N$ denotes the II$P3$ of each stage, while $G_{a,N}$ stands for the available power gain of each stage. They are both expressed in the linear domain. Based on this formula, enhancing the overall II$P3$ of the entire chain (II$P3_{total}$) requires designing subsequent stages with higher linearity metrics, given the amplification of the signal across the cumulative gain of prior stages. This often necessitates larger DC power consumption and increased design complexity, potentially demanding additional linearization techniques. The same concept can be applied to the compression point performance of the cascaded chain as well.

In radar applications, the monostatic TRX configuration, which utilizes a single antenna for both transmit and receive functions, incorporates a coupler at the antenna interface to ensure proper isolation between TX and RX paths. However, the limitations of the isolation of the coupler lead to signal leakage from TX to RX, referred to as "TX to RX spillover". Especially during high output power transmission, the leaked signal can be large enough to cause compression of the LNA. Additionally, the leaked signal may alter the operating point of the LNA, leading to a worse noise performance due to degraded noise matching. The TX to RX spillover issue becomes even more pronounced in an RX chain with a lower IP_{1dB}.

Various techniques, involving additional active circuitries and passive elements, are proposed in the literature [MGV+15, PWJS16, CPLW18, KKN18] to cancel this leakage. While effective, these solutions often come at the cost of increased power consumption, larger chip area, and greater design complexity. Instead, this work pursues an alternative approach to mitigate the IP_{1dB} suppression issue, by eliminating the LNA and employing an I/Q downconversion mixer pair as the first element in the RF path. Moreover, downconversion mixers can be tailored for low noise operation, resulting in an improved RX performance with optimized compression behavior and noise characteristics. Detailed information on noise optimization of the employed downconversion mixers and design considerations are given in Section 4.4.1. The overall design procedure of the RX chain is explained in Section 4.4.

$$\frac{1}{\mathrm{II}P3_{\mathrm{total}}} = \frac{1}{\mathrm{II}P3_1} + \frac{G_{\mathrm{a},1}}{\mathrm{II}P3_2} + \frac{G_{\mathrm{a},1}G_{\mathrm{a},2}}{\mathrm{II}P3_3} + \ldots + \frac{G_{\mathrm{a},1}G_{\mathrm{a},2}\ldots G_{\mathrm{a,N-1}}}{\mathrm{II}P3_{\mathrm{N}}} \tag{4.1}$$

The TRX adopts a quadrature topology due to its inherent ability to reject noise in the image band after the downconversion. The necessary 90° phase offset for I/Q operations is generated by differential hybrid couplers and can be introduced either at RF or LO ports. Regardless of the port where the 90° phase shift is introduced, there is a requirement for differential power dividers to split the signal at the port where I/Q generation does not occur. For instance, if the I/Q generation happens at the RF port, the LO input signal must be divided for distribution among the I/Q mixers.

The reasoning behind the decision to generate I/Q signals at the RF port is as follows. Firstly, as demonstrated in Section 4.3, the differential hybrid coupler exhibits lower excess losses compared to the differential power divider. Considering the mixer-first architecture of the RX channel, utilizing the differential hybrid coupler proves more beneficial than using the differential power divider at the RF port, as the excess loss of the utilized passive component directly contributes to the NF performance of the receiver. A similar logic also applies to the TX channel, due to the fact that the excess loss performance of the adopted passive component at the RF output of the upconversion mixers, referring to Fig. 4.1(a), directly impacts the ability to drive the subsequent PA. Furthermore, the broadside coupler exhibits a superior matching performance over a wide frequency range in comparison to the power divider, as shown in Section 4.3. Achieving a better matching at the RF port holds greater importance than at the LO port. For instance, when the RX channel is considered, an impedance mismatch at the RF port directly increases noise, while a mismatch at the LO port reduces the available LO power, resulting in a relatively minor degradation in noise performance. Additionally, since the I and Q mixers are completely identical in both RX and TX channels, they also enjoy increased tolerance against the impedance mismatches, thanks to the balanced topology. Finally, to mitigate I/Q cross-talk, the passive component utilized at the RF port must offer significant isolation between the ports that connect to the mixers. For instance, as illustrated in Fig. 4.1(a), the hybrid coupler in the RX channel should ensure high isolation between its output ports to prevent any leakage between downconversion mixers. The hybrid coupler delivers isolation ex-

ceeding 20 dB across the *D*-band, whereas the power divider demonstrates significantly poorer isolation, at around only 5 dB.

Further details regarding the differential coupler are outlined in Section 4.3.1. A differential power divider is designed for LO distribution, as explained in Section 4.3.2. Marchand baluns are employed at the RF and LO ports to convert the differential signals into single-ended signals, facilitating single-ended on-wafer probing during measurements. Their design is discussed in more detail in Section 4.3.3.

The upconversion mixers and the PA are explained in Section 4.5. Lastly, the design details of the LO blocks, including the frequency doubler and the driver amplifier (DA) chain are discussed in Section 4.6, along with the additional optimization considerations at the LO distribution network.

4.3 Passives

In this TRX configuration, differential hybrid couplers are employed to generate I/Q signals at the RF path, while the LO distribution is facilitated by differential power dividers. On-chip marchand baluns are employed at the RF and LO ports to enable single-ended on-wafer probing during measurements.

The main considerations in passive designs are as follows: they occupy the most IC area, thus, are optimized to have a compact footprint with a proper geometry to fit to the rest of the chip layout. Furthermore, the focus is on achieving excess losses as small as possible while simultaneously ensuring good phase and amplitude imbalance characteristics.

4.3.1 Differential Hybrid Coupler

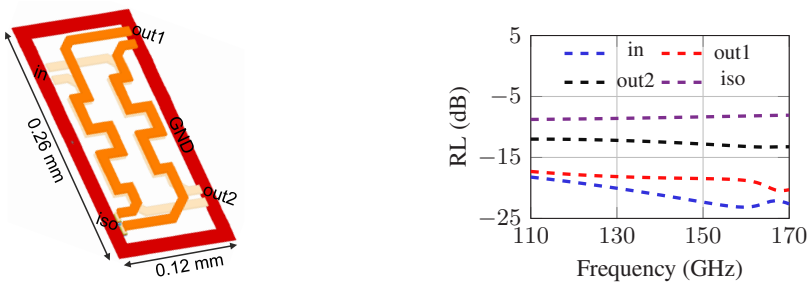
Branch-line and Lange couplers, as depicted in Fig. 4.2, along with broadside couplers shown in Fig. 4.3(a), are commonly employed for generating quadrature signals in mm-wave frequencies. Design considerations for these couplers include producing output signals with equal amplitude and a 90° phase offset, maintaining a broad frequency range, minimizing IC footprint, and ensuring compatibility with the overall IC layout geometry. Branch-line couplers exhibit

Figure 4.2: Corresponding ports, P_2: in, P_1: out1, P_3: out2, P_4: iso for (a) Branch-line coupler. (b) Lange coupler. [2] © IEEE

competent performance in terms of loss and imbalance, but they often require a significant IC area. On the other hand, Lange couplers, although compact and widely used at lower frequencies, pose challenges at higher frequencies since their implementation requires narrower strip widths at higher frequencies. The implementation of narrower strip widths results in increased losses and may even be constrained by technology design rules.

Broadside couplers offer the best trade-offs between the loss and imbalance performances, frequency range, IC area, and layout compatibility. However, their design complexity requires extensive efforts in EM modeling. In this work, a broadside coupler is utilized in the RF path due to its advantages, including wideband matching, competent loss and imbalance performance, isolation of approximately 25 dB between output ports that help preventing I/Q cross-talk, and compact layout geometry thanks to implementing coupled lines with multiple bends. The designed coupler measures $0.26\,\text{mm} \times 0.12\,\text{mm}$, as shown in Fig. 4.3(a).

The design process starts by designing a quarter-wave long line at the frequency of operation. Initially, this yields a coupler with perfect performance, exhibiting 0 dB amplitude mismatch and a 90° phase difference between the I and Q signals, only at a narrow bandwidth at the center frequency. To broaden the bandwidth, alternative couplers with different center frequencies can be designed and cascaded. This approach is known as multi-section coupling and suffers from considerable IC area.

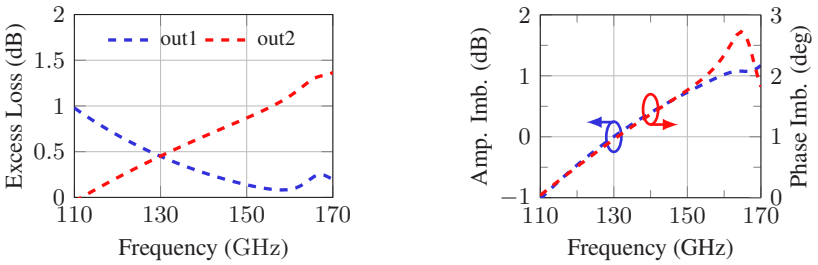


(a) (b)

Figure 4.3: Coupler (a) 3D image with port naming at RX mode. (b) Simulated return losses (RL) at each port. [2] © IEEE

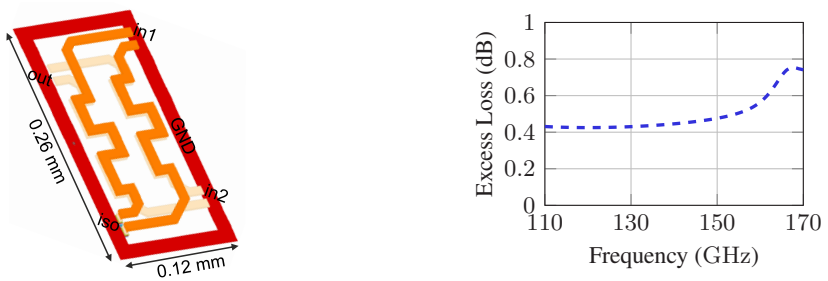
Alternatively, one can specify target values for amplitude and phase mismatches, and tune the coupling between broadside-coupled lines. A wideband frequency response can be achieved by over-coupling the broadside-coupled lines. As the coupler is integrated at the RF ports, its excess loss directly contributes to the RX NF and impacts the TX output power. To improve loss performance, the broadside coupler is implemented using the top two thick metal layers with ground cut-outs. Simulated return loss (RL) for all ports are presented in Fig. 4.3(b). The return losses at the input and output ports remain to be better than −12 dB across the *D*-band, while the return loss at the isolated port stays around −8 dB across the frequency range.

When the coupler is used at the RX channel, the simulated excess losses between the input port and each output ports are illustrated in Fig. 4.4(a). The loss experienced between the input and the first output port (out1) is less than 1 dB across the *D*-band while the minimum loss is achieved towards the higher end of the *D*-band. Meanwhile, the loss between the input and the second output port (out2) is minimized at the lower frequency end of the *D*-band. The losses between the input and each of the output ports have the same value of approximately 0.5 dB around 130 GHz. Furthermore, amplitude and phase imbalances between the output signals (out1 and out2, referring to Fig. 4.3(a)) influence the image rejection-ratio (IRR), determining the extent of noise rejection at the image band. These imbalances are shown over the



(a) (b)

Figure 4.4: Coupler (a) Simulated excess loss performance. (b) Simulated amplitude and phase imbalances. [2] © IEEE



(a) (b)

Figure 4.5: Coupler (a) 3D image with port naming at TX mode. (b) Simulated excess loss. [2] © IEEE

D-band in Fig. 4.4(b). The amplitude and phase imbalances remain below ±1 dB and ±3° across the entire *D*-band.

When the coupler is used at the TX channel, the coupler combines the outputs of the quadrature upconversion mixers with 90° phase offset. The naming of the coupler ports when used at the TX channel is illustrated in Fig. 4.5(a). The excess loss experienced while combining the 90° apart output signals of the I/Q upconversion mixers is shown in Fig. 4.5(b). An excess loss of 0.45 dB is observed at 140 GHz.

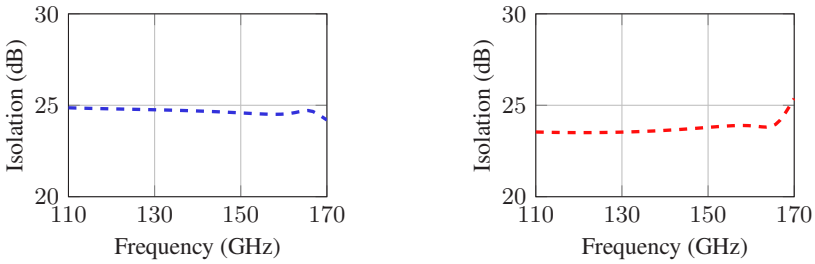


Figure 4.6: Simulated isolation between the coupler (a) Input and isolated ports. (b) Two output ports. [2] © IEEE

A high isolation between the input port and the isolated port prevents signal leakage. Fig. 4.6(a) demonstrates that the isolation between the input port and the isolated port is around 25 dB. Additionally, considering the previously discussed TX-to-RX spillover issue in monostatic TRX configurations and the risk of I/Q cross-talk, a high isolation between the output ports is crucial. This coupler presents a simulated isolation of better than 23 dB between its output ports, as shown in Fig. 4.6(b).

4.3.2 Differential Power Divider

For the distribution of LO signals, two different differential power dividers based on the Wilkinson architecture have been designed, focusing on achieving low excess loss behavior and balanced output signals. The implementation involves utilizing the top two thick metal layers, each with an electrical length of $\lambda/4$ at 140 GHz, while maintaining a characteristic impedance of $Z_0\sqrt{2}$. To optimize the IC area and ensure compatibility with the overall layout, the tracks have multiple bends.

The first power divider, integrated at the LO interface of the RX and TX channels, occupies a total IC area of 0.25 mm × 0.08 mm, as depicted in the 3D image in Fig. 4.7(a). The second power divider, positioned immediately after the LO driver amplifier, measures 0.12 mm × 0.135 mm, as shown in

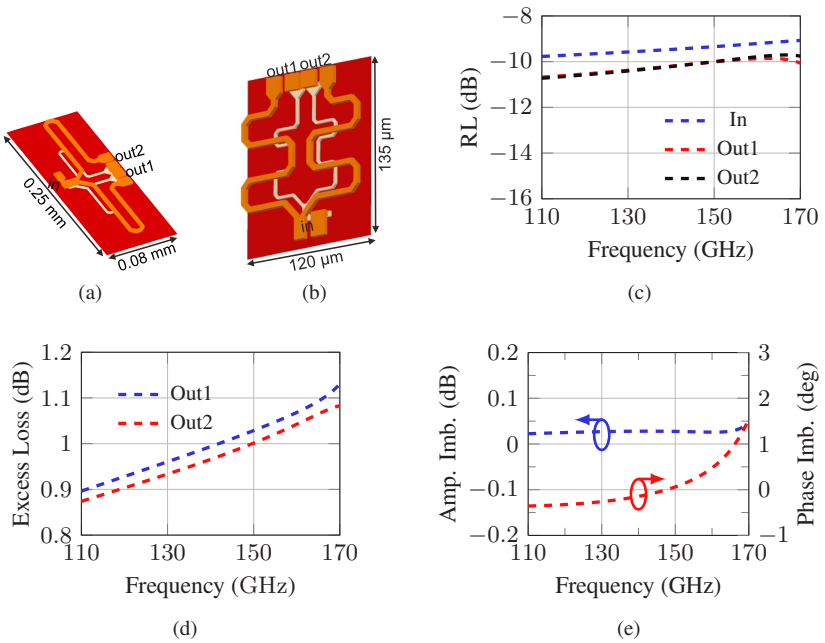
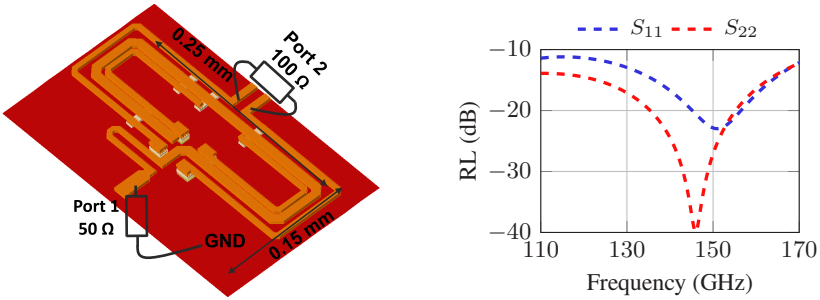


Figure 4.7: Power divider (a) 3D image. (b) 3D image of the second version. (c) Simulated return losses at each port. (d) Simulated insertion loss performance. (e) Simulated amplitude and phase imbalances. [2] © IEEE

the 3D image in Fig. 4.7(b). The utilization of two different power dividers is driven by the need to match the rest of the layout geometry and minimize the overall IC area. The design decisions behind both power dividers are essentially the same and their performance parameters are also similar.

The return and excess losses throughout the entire *D*-band are illustrated in Fig. 4.7(c) and Fig. 4.7(d), respectively. The return losses remain to be better than −9 dB over the entire *D*-band, while the power divider demonstrates an excess loss of approximately 1 dB. Additionally, Fig. 4.7(e) shows the amplitude and phase imbalances between the output ports, with the amplitude imbalance remaining below 0.1 dB and the phase imbalance staying below 1.5° across the *D*-band frequencies.



(a) (b)

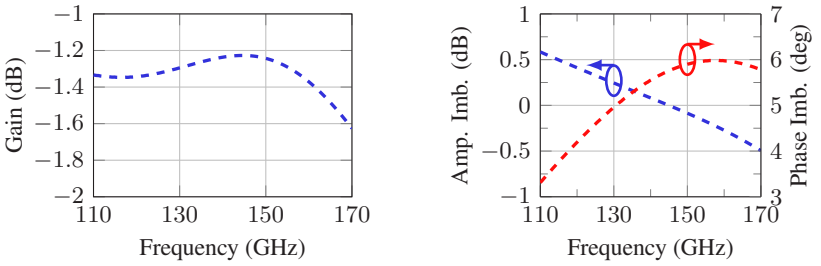
Figure 4.8: Balun (a) 3D image. (b) Simulated return losses at each port. [2] © IEEE

4.3.3 Marchand Balun

Since the TRX is implemented in fully differential configuration, the RX RF input, TX RF output and LO input have differential interfaces. However, as high-performance differential probes operating at *W* and *D*-band frequencies are unavailable, the RF and LO ports incorporate on-chip marchand baluns to facilitate single-ended on-wafer probing during measurements. The baluns rely on asymmetric coupled lines, detailed in [AYJ+19]. In Fig. 4.8(a), a 3D representation of the *D*-band marchand balun is provided, featuring an inner line with an electrical length of $\lambda/2$ coupled to two $\lambda/4$ lines. The *W*-band balun is also implemented following the same principles.

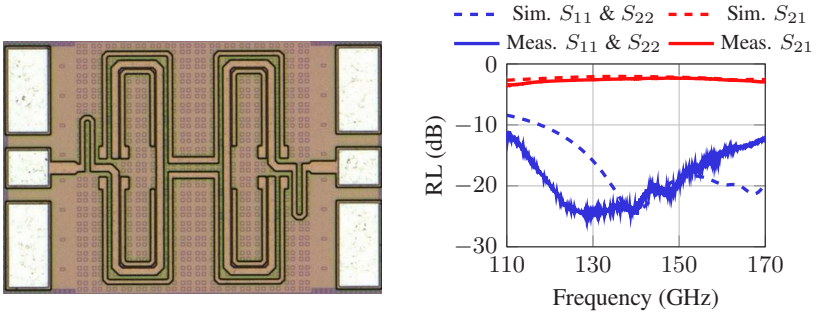
Fig. 4.8(b) illustrates the simulated return losses at the differential and single-ended ports, terminated by 100 Ω and 50 Ω, respectively. At 140 GHz, the insertion loss is approximately 1.2 dB, as demonstrated in Fig. 4.9(a). Furthermore, Fig. 4.9(b) displays amplitude and phase imbalances between the positive and negative terminals of the differential output when both terminals are terminated by 50 Ω.

The marchand balun is taped out and characterized independently in a back-to-back configuration. The chip micrograph depicting the back-to-back baluns is presented in Fig. 4.10(a). As the on-chip baluns are not parts of the TRX, the measured insertion losses of the baluns, illustrated in Fig. 4.10(b), are de-embedded.



(a) (b)

Figure 4.9: Balun (a) Simulated loss performance. (b) Simulated amplitude and phase imbalances in between the positive and negative terminals of the differential port. [2] © IEEE



(a) (b)

Figure 4.10: (a) Chip micrograph of the back-to-back baluns. (b) Measured and simulated S-parameters of the back-to-back baluns. [2] © IEEE

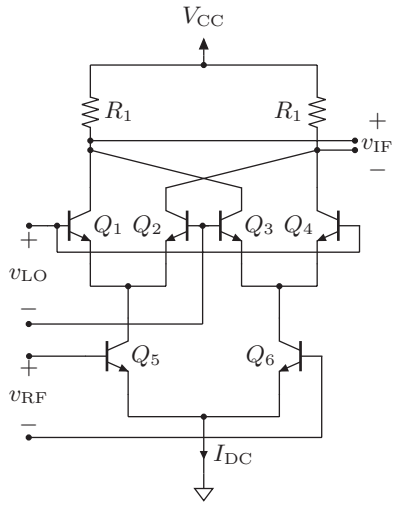


Figure 4.11: Circuit schematic of a double-balanced Gilbert cell downconversion mixer.

4.4 Receiver Channel

The RX channel adopts a mixer-first architecture utilizing Gilbert cell based downconversion mixers. A differential power divider is used for LO distribution and a differential hybrid coupler is employed for I/Q generation in the RF path. The noise performance of the downconversion mixers becomes quite crucial since they are the first components in the RF path after the LNA is eliminated. This section explains the design of downconversion mixers, and details the design decisions for simultaneously improved noise and linearity performances.

4.4.1 I/Q Downconversion Mixers

The double-balanced Gilbert cell architecture is employed for downconversion mixers. Referring to the circuit schematic of a double-balanced Gilbert cell, shown in Fig. 4.11, the following equations regarding the total DC current, I_{DC}, can be derived.

$$I_{DC} = I_5 + I_6 = I_1 + I_2 + I_3 + I_4 \tag{4.2}$$

The difference and sum of the currents through Q_1 and Q_2 can be expressed in (4.3) and (4.4).

$$I_5 = I_1 + I_2 = I_S \left[\exp\left(\frac{V_{BE1}}{V_T}\right) + \exp\left(\frac{V_{BE2}}{V_T}\right) \right] = I_S \exp\left(\frac{V_{BE2}}{V_T}\right) \left(\exp\left(\frac{v_{LO}}{V_T}\right) + 1 \right) \tag{4.3}$$

$$\Delta I = I_1 - I_2 = I_S \left[\exp\left(\frac{V_{BE1}}{V_T}\right) - \exp\left(\frac{V_{BE2}}{V_T}\right) \right] = I_S \exp\left(\frac{V_{BE2}}{V_T}\right) \left(\exp\left(\frac{v_{LO}}{V_T}\right) - 1 \right) \tag{4.4}$$

Expressing $\Delta I_{1,2}$ in terms of I_5 and I_6 results in (4.5). Similarly, $\Delta I_{3,4}$ can also be expressed as in(4.6).

$$\Delta I_{1,2} = I_1 - I_2 = I_5 \tanh\left(\frac{v_{LO}}{2V_T}\right) \tag{4.5}$$

$$\Delta I_{3,4} = I_4 - I_3 = I_6 \tanh\left(\frac{v_{LO}}{2V_T}\right) \tag{4.6}$$

Afterwards, the difference in the currents of the input transistors, I_5 and I_6, can be represented as shown in (4.7).

$$\Delta I_{5,6} = I_5 - I_6 = I_{DC} \tanh\left(\frac{v_{RF}}{2V_T}\right) \tag{4.7}$$

Finally, the difference in the currents at the IF terminal, ΔI_{IF}, can be expressed as in (4.8). After substituting $\Delta I_{5,6}$ with the expression in (4.7), (4.9) can be obtained.

$$\Delta I_{\mathrm{IF}} = (I_1 - I_2) - (I_4 - I_3) = (I_5 - I_6)\tanh\left(\frac{v_{\mathrm{LO}}}{2V_{\mathrm{T}}}\right) \tag{4.8}$$

$$\Delta I_{\mathrm{IF}} = (I_5 - I_6)\tanh\left(\frac{v_{\mathrm{LO}}}{2V_{\mathrm{T}}}\right) = I_{\mathrm{DC}}\tanh\left(\frac{v_{\mathrm{RF}}}{2V_{\mathrm{T}}}\right)\tanh\left(\frac{v_{\mathrm{LO}}}{2V_{\mathrm{T}}}\right) \tag{4.9}$$

ΔI_{IF} in (4.9) can be used to calculate v_{IF} as shown in (4.10), where R_1 is the termination resistance at the output of the Gilbert cell.

$$v_{\mathrm{IF}} = -R_1 I_{\mathrm{DC}}\tanh\left(\frac{v_{\mathrm{RF}}}{2V_{\mathrm{T}}}\right)\tanh\left(\frac{v_{\mathrm{LO}}}{2V_{\mathrm{T}}}\right) \tag{4.10}$$

Assuming a small signal operation at the RF port, $\tanh\left(\frac{v_{\mathrm{RF}}}{2V_{\mathrm{T}}}\right)$ can be approximated to $\left(\frac{v_{\mathrm{RF}}}{2V_{\mathrm{T}}}\right)$. Afterwards, assuming sinusoidal signals at the RF and LO ports, $\left(\frac{v_{\mathrm{RF}}}{2V_{\mathrm{T}}}\right)$ can be rewritten as $\left(\frac{V_{\mathrm{RF}}\cos(\omega_{\mathrm{RF}}t)}{2V_{\mathrm{T}}}\right)$, where V_{RF} is the amplitude. Finally, (4.10) can be rewritten as (4.11).

$$v_{\mathrm{IF}} = -R_1 I_{\mathrm{DC}}\left(\frac{V_{\mathrm{RF}}\cos(\omega_{\mathrm{RF}}t)}{2V_{\mathrm{T}}}\right)\tanh\left(\frac{v_{\mathrm{LO}}}{2V_{\mathrm{T}}}\right) \tag{4.11}$$

The transconductance of the input stage transistors, $Q_{5,6}$, can be expressed as in (4.12).

$$g_{\mathrm{m}_{5,6}} = \frac{I_5}{V_{\mathrm{T}}} = \frac{I_6}{V_{\mathrm{T}}} = \frac{I_{\mathrm{DC}}}{2V_{\mathrm{T}}} \tag{4.12}$$

Replacing $\frac{I_{\mathrm{DC}}}{2V_{\mathrm{T}}}$ in (4.11) with $g_{\mathrm{m}_{5,6}}$, (4.13) can be derived.

$$v_{\mathrm{IF}} = -R_1 g_{\mathrm{m}_{5,6}} V_{\mathrm{RF}}\cos(\omega_{\mathrm{RF}}t)\tanh\left(\frac{v_{\mathrm{LO}}}{2V_{\mathrm{T}}}\right) \tag{4.13}$$

When the magnitude of V_{LO} reaches large enough values, specifically at around 5 to 6 times of V_T, $\tanh\left(\frac{v_{LO}}{2V_T}\right)$ swings between ± 1 and the Fourier expansion can be written as in (4.14).

$$\tanh\left(V_{LO}\cos(\omega_{LO}t)\right) = \frac{4}{\pi}\cos(\omega_{LO}t) + \frac{4}{3\pi}\cos(3\omega_{LO}t) + \frac{4}{5\pi}\cos(5\omega_{LO}t) + \ldots \tag{4.14}$$

Consequently, after filtering out the higher harmonics in (4.14), conversion gain (CG) can be derived as the ratio between v_{IF} and v_{RF}, as expressed in (4.15).

$$A_{VC} = \frac{v_{IF}}{v_{RF}} = -R_1 g_{m_{5,6}} \frac{2}{\pi} \tag{4.15}$$

From in (4.15), CG of the Gilbert cell based downconversion mixer is a function of the load resistance as well as the transconductance of the input stage transistor. Additionally, as explained through tanh function, there is a specific voltage swing required for the switching operation. The required LO power corresponding to this voltage swing depends on the input impedance at the LO port. As the device size increases, the input impedance at the LO port drops and the required LO power raises. Therefore, the required LO power is an important consideration while choosing the device size.

The circuit schematic of the adopted downconversion mixers, based on the double-balanced Gilbert cell architecture, is depicted in Fig. 4.12. The mixer core utilizes switching-quad devices Q_{1-4} with the smallest available device size in the adopted process, measuring $1\times0.07\times0.9\ \mu m^2$, to relax the LO drive requirements, and reduce overall power consumption. The input stage devices, Q_{5-6}, are sized at $2\times0.07\times0.9\ \mu m^2$ each to maintain the same current density with Q_{1-4}. A 3D representation of the mixer core is presented in Fig. 4.13(a). The core layout is implemented with the effort to preserve symmetry within the core layout, particularly at the high-frequency RF and LO ports. High Q matching networks based on *L-C* components are integrated to minimize the NF contribution from the matching network at the RF port. Inductors are designed with ground cut-outs, and metal-oxide-metal (MOM) capacitors are implemented to enhance the Q values. A current mirror based bias circuit is

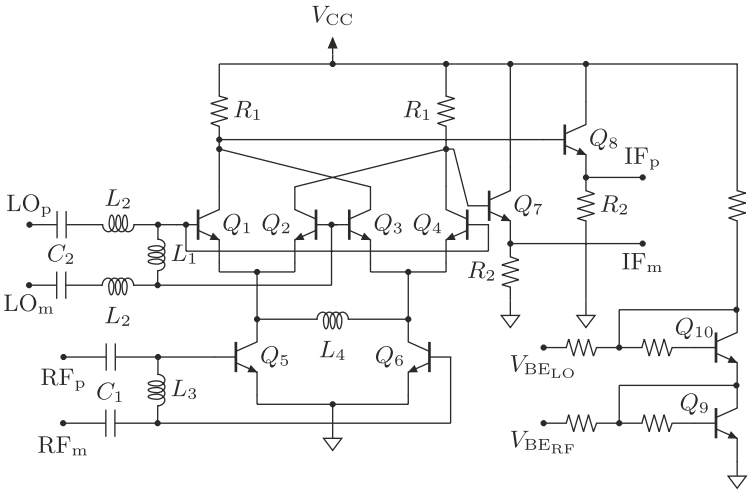
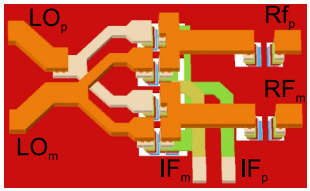


Figure 4.12: Circuit schematic of the double-balanced downconversion mixer with bias circuit. [2] © IEEE



(a)

L_1	110 pH	Q_{1-4}	×1
L_2	35 pH	$Q_{5,6}$	×2
L_3	90 pH	$Q_{7,8}$	×10
L_4	100 pH	$Q_{9,10}$	×1
C_1	60 fF	R_1	300 Ω
C_2	0.5 pF	R_2	150 Ω

(b)

Figure 4.13: (a) 3D image of the Gilbert cell core. (b) List of the schematic components in 4.12. [2] © IEEE

adopted to bias the input stage and switching-quad transistors. A single supply is used to power the entire circuit. The list of schematic components is given in Fig. 4.13(b).

After setting the switching-quad device size to the smallest available in the process, to limit the power consumption and the LO drive requirement, the design proceeds with choosing the current density. The current density has

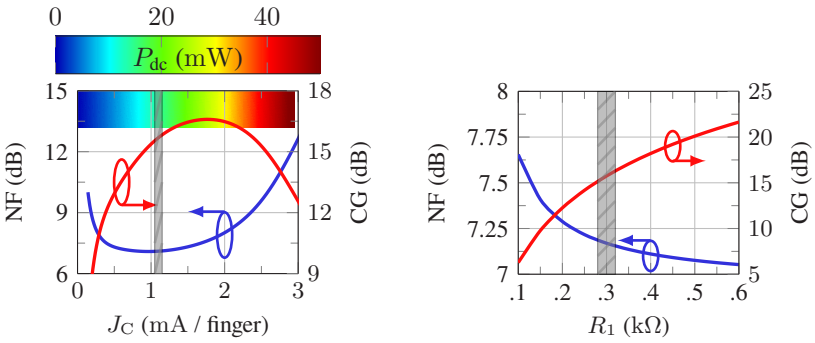


Figure 4.14: The gray bars indicate the chosen values. Impact of (a) Current density J_c on DSB NF, CG and P_{dc}. (b) R_1 on DSB NF and CG. [2] © IEEE

an impact on CG, power consumption, and NF. For a fixed transistor size, increasing the current density improves the transconductance of the input stage devices, thereby giving rise to CG, as shown in (4.15). Given that the power consumption is the product of I_{cc} and V_{cc}, larger current densities lead to an increase in I_{cc}. Additionally, V_{cc} rises with higher current density due to the voltage drop across R_1. The noise derivation is given for CMOS Gilbert cell downconversion mixers in [Raz11]. Similar to the discussions in LNA design, there is an optimum collector current density leading to the minimum NF. In this study, as illustrated in Fig. 4.14(a), a current density of 1.1 mA per finger is selected to minimize NF while maintaining P_{dc} at a moderate level. This choice involves sacrificing a CG of 1 dB. The simulation results are based on a differential LO input power of −5 dBm at the LO port of the I/Q downconversion mixers.

Afterwards, a resistor-based termination (R_1) is chosen at the output of the downconversion mixer due to the relatively lower frequency of the down-converted signal. Opting for larger R_1 values results in higher CG, as evidenced in (4.15). Additionally, R_1 introduces thermal noise, contributing to the overall NF. Larger R_1 values contribute less to NF compared to smaller R_1 values, given that R_1 is in a shunt configuration. The impact of R_1 on CG and NF is illustrated in Fig. 4.14(b).

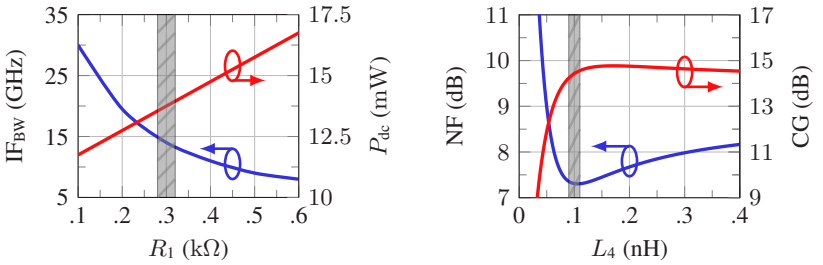


Figure 4.15: The gray bars indicate the chosen values. Impact of (a) R_1 on $\mathrm{IF_{BW}}$ and P_{dc}. (b) L_4 on DSB NF and CG. [2] © IEEE

Despite the benefits of increasing R_1 in terms of CG and NF, choosing a larger R_1 reduces the IF bandwidth and increases the P_{dc}. As depicted in Fig. 4.15(a), larger R_1 reduces IF bandwidth since a low pass filter is formed at the output of the downconversion mixers through the combination of R_1 and output capacitance of the switching-quad devices. P_{dc} also raises with higher R_1 values since V_{cc} has to be increased to account for the voltage drop over R_1. Based on these considerations, an R_1 of 300 Ω is chosen.

The noise reduction technique, as discussed in detail in 3.2.1, is implemented to the Gilbert cell as well. The motivation behind this decision is as follows. During the positive cycle of the LO signal, the switching-quad devices Q_1 and Q_4 are in the ON state, while Q_2 and Q_3 are OFF. Consequently, the pairs Q_5 / Q_1 and Q_6 / Q_4 function as cascode devices. The parasitic capacitances at the nodes between Q_5 and Q_1 as well as Q_6 and Q_4 to the ground increase the noise contribution of switching-quad devices Q_{1-4}, similar to the discussion made for cascode amplifiers. To counteract this effect, a shunt inductance is introduced at these nodes to neutralize the impact of the parasitic capacitances. This behavior is illustrated in Fig. 4.15(b). By selecting an L_4 value of 100 pH, the NF can be reduced by 1.2 dB.

Additionally, a differential common collector (CC) buffer, comprising Q_{7-8}, is connected at the mixer output to isolate the Gilbert cell from the differential 100 Ω load posed by the measurement environment, preventing the drop in the CG. It is important to note that the CC buffer has a unity total voltage gain,

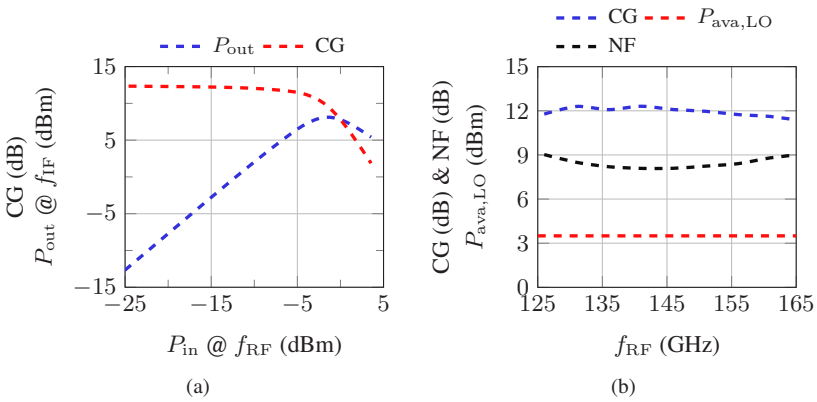


Figure 4.16: Simulated RX performance (a) CG and P_{out} vs. P_{in}. (b) CG and NF vs. f_{RF}. [2] © IEEE

thus it does not contribute to the IF amplification. The buffer draws a total current of 41.2 mA from a 3 V supply.

4.4.2 Receiver Summary

The simulated CG and P_{out} with varying P_{in} at an RF frequency of 140 GHz and an IF frequency of 1 GHz is illustrated in Fig. 4.16(a). A simulated CG of 12.3 dB is achieved with an I$P_{1\text{dB}}$ of −4.5 dBm while the O$P_{1\text{dB}}$ is 6.9 dBm and the maximum output power is 8.1 dBm. Fig. 4.16(b) demonstrates CG and NF with respect to changing RF frequency when the IF frequency is kept constant at 1 GHz. As can be seen, CG demonstrates a flat frequency profile covering all the way from 125 GHz to 165 GHz, owing to the wideband characteristics of the power divider as well as the hybrid coupler. Similarly, NF does not change drastically over the frequency, remaining below 9.1 dB between 125 GHz to 165 GHz while the lowest NF of 8.1 dB is achieved at the RF frequency of 141 GHz.

Lastly, Fig. 4.17(a) presents the change in CG and NF with respect to the available LO power at an RF frequency of 140 GHz and an IF frequency of

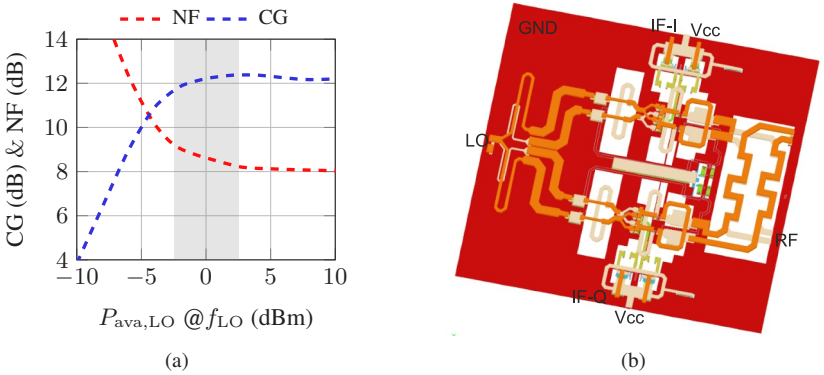


Figure 4.17: Simulated RX performance (a) CG and NF vs. available LO power. (b) 3D view and EM setup of the downconversion mixers, power divider and coupler. [2] © IEEE

1 GHz. The maximum performance is observed when the LO power at the input of the differential power divider remains between −2.5 dBm and 2.5 dBm, as shown with the gray bar. The EM setup of the RX channel is shown in Fig. 4.17(b). A further discussion on IRR performance can be found in Section 4.7.2.

4.5 Transmitter Channel

The TX channel includes upconversion I/Q mixers, featuring a double-balanced Gilbert cell core. The I/Q RF outputs from these mixers are then connected to a hybrid coupler, and the resulting signal is directed into a PA. A differential power divider is employed at the LO port for the LO feeding. This section explains the design choices for the upconversion mixers and the PA.

4.5.1 I/Q Upconversion Mixers

The upconversion I/Q mixers employ a double-balanced Gilbert cell architecture, and their circuit schematic is depicted in Fig. 4.18. A layout view of the

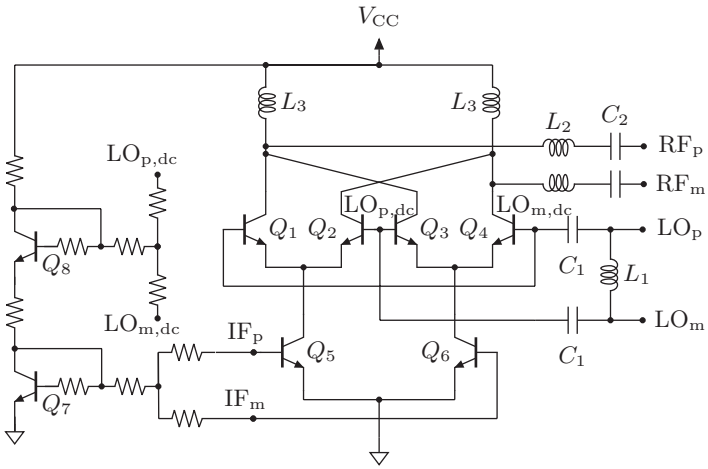
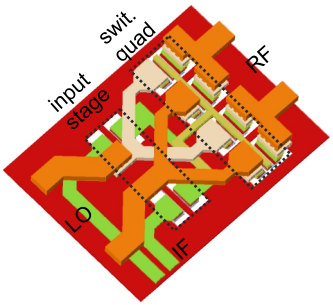


Figure 4.18: Circuit schematic of the double-balanced upconversion mixer with the bias circuitry. [9] © IEEE

double-balanced Gilbert cell mixer core is presented in Fig. 4.19(a), and the schematic component values are shown in Fig. 4.19(b). In the upconversion Gilbert cell configuration, the differential input IF signal is applied through $Q_{5,6}$, and the differential RF output signal is generated at the Gilbert cell output (the collectors of the switching-quad devices, Q_{1-4}). In contrast to downconversion mixer configuration, the output of the upconversion Gilbert cell is inductively terminated, since the output signal has a much higher frequency. This relaxes the voltage headroom and requires a lower V_{cc} compared to the downconversion mixer configuration. Revisiting the CG equation derived for downconversion mixers, (4.15), the upconversion mixer CG can be represented in a similar fashion, as expressed in (4.16), where $R_{eq.}$ is the equivalent parallel resistance of the collector inductance at resonance.



(a)

L_1	50 pH
L_2	170 pH
L_3	67 pH
C_1	0.27 pF
C_2	0.5 pF
Q_{1-4}	×2
$Q_{5,6}$	×4
$Q_{7,8}$	×1

(b)

Figure 4.19: (a) 3D image of the Gilbert cell core. (b) Upconversion mixer schematic component values. [9] © IEEE

$$\begin{aligned} A_{\mathrm{VC}} &= \frac{v_{\mathrm{RF}}}{v_{\mathrm{IF}}} \\ &= \frac{-R_{\mathrm{eq.}} g_{\mathrm{m}_{5,6}} V_{\mathrm{IF}} \tanh\left(\frac{v_{\mathrm{LO}}}{2V_{\mathrm{T}}}\right)}{V_{\mathrm{RF}}} \\ &= -R_{\mathrm{eq.}} g_{\mathrm{m}_{5,6}} \tanh\left(\frac{v_{\mathrm{LO}}}{2V_{\mathrm{T}}}\right) \\ &= -R_{\mathrm{eq.}} g_{\mathrm{m}_{5,6}} \frac{2}{\pi} \end{aligned} \tag{4.16}$$

As can be deducted from (4.16), the CG of upconversion mixers is in direct proportionality with the current density and transistor size, as higher current density and larger transistor size lead to higher $g_{\mathrm{m}_{5,6}}$. This relation is illustrated in Fig. 4.20. The influence of current density (J_{c}) on CG is shown in Fig. 4.20(a), revealing a trade-off between CG and P_{dc}. In this work, a current density of 0.5 mA per finger is chosen for transistors Q_{1-6} to moderate P_{dc}.

When the following PA is operated at 1 dB compression, the required input power at the PA input is −6 dBm. Considering the excess loss of the hybrid

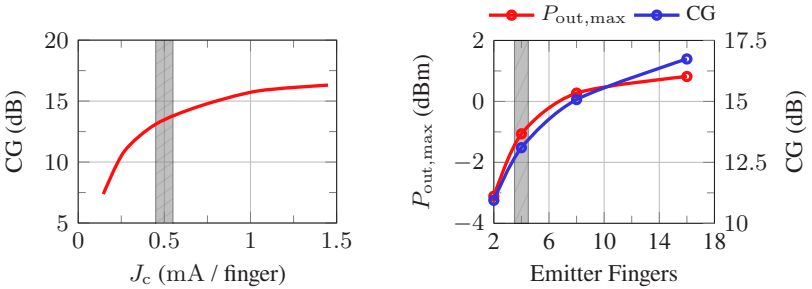


Figure 4.20: The gray bars indicate the chosen values. Simulations showing the impact of (a) Current density (J_c) on CG. (b) Transistor size (Q_{5-6}) on $P_{out,max}$ and CG. [9] © IEEE

coupler, located between the output of upconversion mixers and the PA input, the target output power of the I/Q upconversion mixers is around −5 dBm. The size of the upconversion mixer active devices is set to align with this specification. Fig. 4.20(b) illustrates how the device size of the input stage transistors ($Q_{5,6}$) (and consequently Q_{1-4} to maintain the same current density) influences both CG and the maximum achieved output power ($P_{out,max}$). Despite the favorability of increasing device sizes for both CG and $P_{out,max}$, a transistor size of $4 \times 0.07 \times 0.9\,\mu m^2$ for Q_{5-6} and $2 \times 0.07 \times 0.9\,\mu m^2$ for Q_{1-4} are chosen to ease LO drive requirements and maintain a low P_{dc}. The correlation between the necessary LO power and transistor size aligns with the discussion in Section 4.4.1. A larger device size leads to lower impedances at the LO port, consequently requiring higher LO power levels for a given voltage swing. Moreover, the reason for the output power increase with larger transistor size is as follows: as the device size increases, the CG also increases, resulting in a larger voltage swing at the output of the Gilbert cell for a given input power, leading to larger output power.

Finally, the matching networks at the RF and LO ports are optimized through load-pull and source-pull simulations. The inductors at the RF output of the Gilbert cell are optimized with ground cut-outs to minimize losses over the output matching network. An individual breakout consisting of the I/Q upconversion mixer pair connected to the power divider and the coupler is also

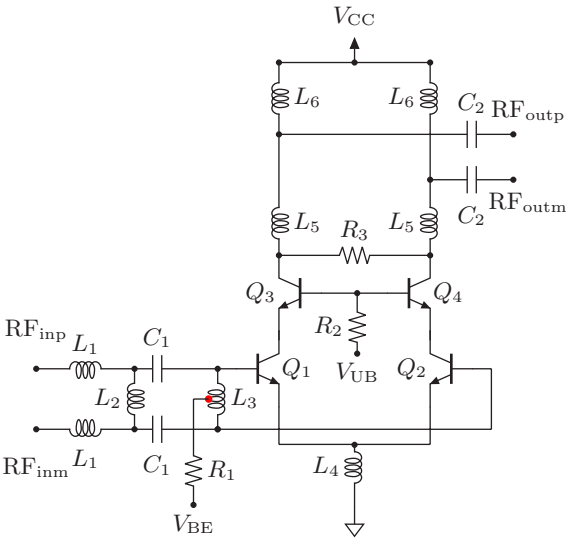
taped out and characterized separately. The measured results are presented in Section A.1.

4.5.2 Power Amplifier

A fully differential single stage cascode topology is adopted for the PA. The amplifier circuit schematic is shown in Fig. 4.21(a) with the schematic component values displayed in Fig. 4.21(b). As shown through the analysis in Fig. 2.19(a), the device sizing has a direct impact on P_{sat}. A saturated output power of 6 dBm is targeted for the transmitter, and choosing a moderate device size of 5 fingers ($5 \times 0.07 \times 0.9\,\mu\mathrm{m}^2$) for Q_{1-4} is simulated to be sufficient to achieve that. Based on the output power capabilities of the preceding stage (I/Q upconversion mixers), a small-signal gain of 10 dB is targeted so that the amplifier can achieve an OP_{1dB} of around 4 dBm. At D-band frequencies, 10 dB of small-signal gain can be obtained through a single stage cascode amplifier when the amplifier operates at a current density of 1.5 mA per finger, close to the peak f_{T} & f_{MAX} performance, facilitating relatively high compression point performance. A supply voltage of $V_{\mathrm{cc}} = 3$ V is chosen for the PA.

The output matching network, consisting of L_5, L_6, and C_2, is designed with a focus on presenting the optimum load-pull impedance over a broad bandwidth. To achieve this, the Q of the output matching network is reduced by introducing a differentially connected shunt resistor, $R_3 = 600\,\Omega$ to extend the bandwidth at the cost of 3 dB reduction in the gain. The simulated small-signal S-parameters are shown in Fig. 4.22(a). S_{21} peaks at 10.5 dB at 140 GHz, with a B_{3dB} spanning from 118 GHz to 162.5 GHz totaling up to 42.5 GHz.

The large-signal performance at 135 GHz is shown in Fig. 4.22(b). An OP_{1dB} of around 3.5 dBm is achieved while P_{sat} reaches up to 6 dBm with the maximum PAE being 5.6 %. It is worth noting that employing R_3 also leads to relatively lower PAE values. The PA is also taped out separately as a breakout and the details are given in Section A.2.

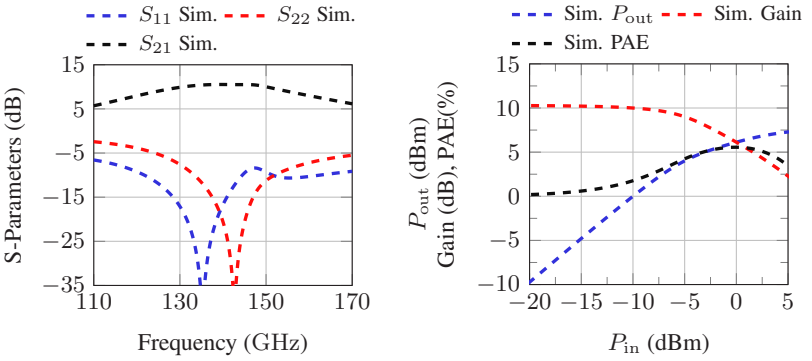


(a)

L_1	75 pH
L_2	85 pH
L_3	95 pH
L_4	8 pH
L_5	24 pH
L_6	28 pH
Q_{1-4}	×5
C_1	50 fF
C_2	0.5 pF
R_1	250 Ω
R_2	1 kΩ
R_3	600 Ω

(b)

Figure 4.21: (a) Simplified circuit schematic of the PA. (b) Values of the schematic components. [13] © IEEE



(a) (b)

Figure 4.22: Simulated PA performance (a) S-parameters. (b) P_{out}, Gain and PAE vs. P_{in} at 135 GHz.

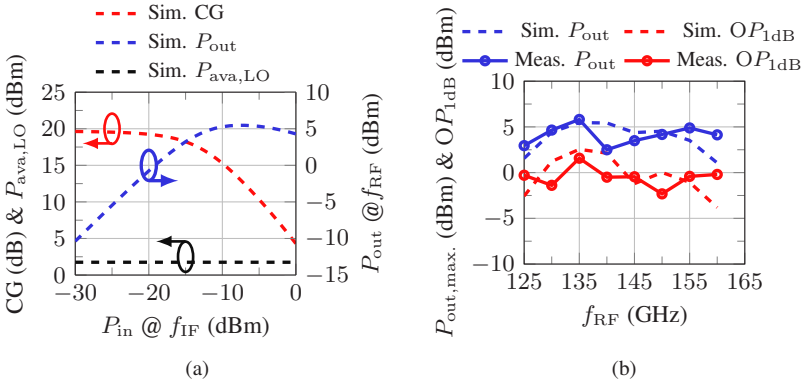
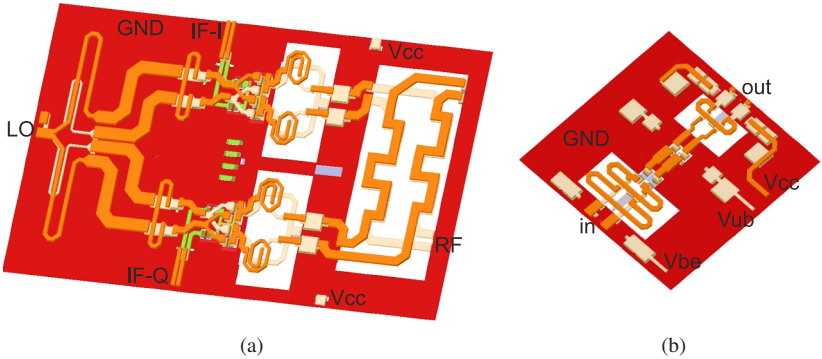


Figure 4.23: Simulated large-signal performance of the TX at 135 GHz (a) P_{in} vs. P_{out} and CG. (b) f_{RF} vs. P_{out} and OP_{1dB}.

4.5.3 Transmitter Summary

The large-signal performance of the presented TX comprising of I/Q upconverters and a PA is illustrated in Fig. 4.23 at an RF frequency of 135 GHz and an IF frequency of 1 GHz. The TX chain exhibits a CG of 19.6 dB and an OP_{1dB} of around 2.5 dBm. This is 1 dB lower compared to the one that the standalone PA demonstrates. The difference arises due to the fact that the OP_{1dB} of the upconversion mixers reaches up to −5.5 dBm, at which the PA is already compressed by 1 dB. This issue can be mitigated either by pushing up the compression point of the PA or ensuring that the upconversion mixers do not enter compression when generating the output power that drives the PA into 1 dB compression. The TX chain demonstrates a $P_{\text{out,max}}$ of 5.5 dBm. The change in $P_{\text{out,max}}$ and OP_{1dB} with respect to the changing RF frequency is illustrated in Fig. 4.23(b). A 3 dB RF bandwidth of around 35 GHz is observed when taking the $P_{\text{out,max}}$ performance into consideration.

The EM simulation setups for the upconverters and the PA are also shown in Fig. 4.24(a) and Fig. 4.24(b). The TX consumes 64.8 mW when operating at linear region, and 88 mW when driven to the $P_{\text{out,max}}$.



(a) (b)

Figure 4.24: 3D view of the layouts and EM simulation setup for the (a) Upconversion mixers, power divider and coupler. (b) PA.

4.6 LO Generation

The targeted LO power for both the up and downconversion mixers is set to be −5 dBm. Accounting for losses due to power splitting (2-times splitting loss = 6 dB) and the insertion loss of the differential power dividers (2-times excess loss ≈ 2 dB), the objective is to generate an LO power of at least 3 dBm at the *D*-band. The LO generation chain involves a push-push frequency doubler, and an LO DA forming a doubler-amplifier chain (DoAC). The LO power distribution optimization is detailed in Section 4.6.1.

4.6.1 Optimization in LO Distribution

To achieve 3 dBm of power at the *D*-band, several strategies have been considered. The first option involves high-power frequency multiplication to potentially reduce or eliminate the need for further amplification at the *D*-band. However, this approach results in the highest overall power consumption, as frequency multiplication is less efficient than amplification. Therefore, a moderate power output at the frequency doubler is targeted. The second option is to perform *D*-band amplification right after the frequency doubler, followed by power division and distribution to the TX and RX channels. This approach

requires an LO DA with relatively larger output device sizes due to the need for higher power handling capability. Finally, the third option is to employ two LO DAs at nodes $N_{1,2}$, as marked in Fig. 4.1(a), after the first power divider at the LO core. In theory, compared to option two, this approach results in the same DC power consumption since the output device size of the amplifiers can be halved. Nonetheless, the third option comes with significantly increased IC area, as the IC area of the amplifiers does not scale linearly with their output power capabilities. Therefore, the second option — a single DA with larger output power capabilities right after the frequency doubler — is chosen as the optimized approach in terms of power consumption, IC area, and design complexity.

4.6.2 Push-Push Frequency Doubler

Push-Push Frequency Doubler is designed by Matthias Möck, and included in this thesis for the sake of completeness.

The circuit schematic of the push-push frequency doubler (PPFD) is given in Fig. 4.25. Transistors Q_1 and Q_2 are biased in Class B with $N_\mathrm{f} = 8$ fingers to maximize the 2^{nd}-harmonic output power. A small emitter degeneration inductance is introduced, enhancing even-mode impedance. While harmonic reflectors could boost conversion gain [MAU22], they are omitted due to their narrow bandwidth. The PPFD's single-ended output signal is converted to a differential signal through a D-band marchand balun. Further details can be found in [MAU24].

4.6.3 Driver Amplifier

The DA shares the same topology as the PA illustrated in Section 4.5.2 and the same circuit schematic as in Fig. 4.21(a). The output matching network, consisting of L_5, L_6, and C_2, is designed with a focus on presenting the optimum load-pull impedance over a broad bandwidth. To achieve this, the output matching network's quality factor is reduced by introducing a differentially connected shunt resistor, $R_3 = 600\,\Omega$. This approach extends the DA's $B_{3\mathrm{dB}}$ to 42.5 GHz. The simulated S-parameters are shown in Fig. 4.22(a), and the large signal performance is shown in Fig. 4.22(b).

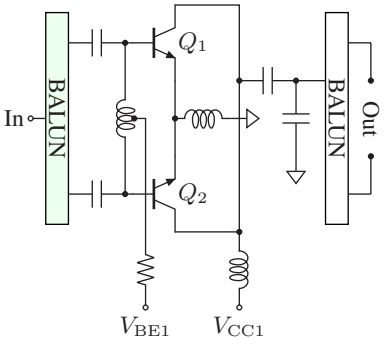


Figure 4.25: Circuit schematic of the PPFD. [13] © IEEE

4.6.4 LO Generation Summary

Simulation results in Fig. 4.26(a) display the co-design process aimed at maximizing bandwidth. $P_{out,PPFD}$ represents the input power of the DA. The PPFD's maximum output power ($P_{out,PPFD}$) peaks at 120 GHz. Conversely, the DA gain reaches its maximum at 160 GHz, coinciding with a local minimum of $P_{out,PPFD}$. This cascaded peaking results in a flatter frequency profile, contributing to an expanded bandwidth for the combined output power ($P_{out,DoAC}$) of the DoAC. This co-design approach leads to a remarkable enhancement in bandwidth.

Fig. 4.26(b) depicts maximum CG and fundamental rejection ratio (FRR), both with and without the DA. Simulations indicate that adding the DA results in up to 10 dB improvement in CG, as expected. Additionally, the fundamental suppression of the DoAC remains better than 34 dBc across the entire D-band.

The simulated large-signal performance of the doubler-amplifier chain is illustrated in Fig. 4.27. Fig. 4.27(a) demonstrates P_{in} vs. P_{out} at the input frequency of 70 GHz. As can be seen, an output power of around 4.3 dBm is achieved when the frequency doubler is supplied with an input power of 4.6 dBm. Furthermore, Fig. 4.27(b) shows the frequency response of the doubler-amplifier chain in terms of the maximum output power with respect to the output frequency. The peak large-signal performance is achieved around

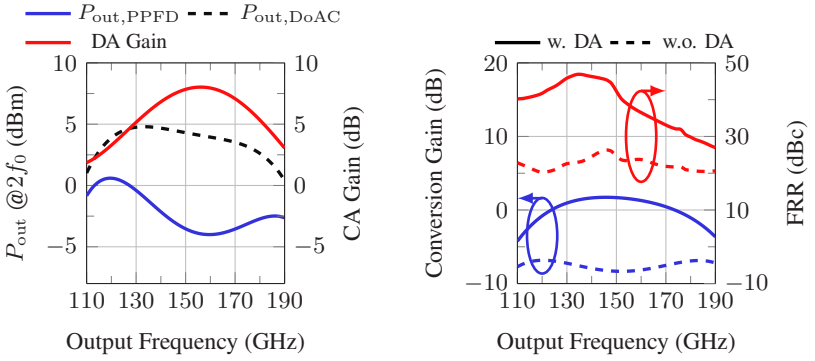


Figure 4.26: Simulations showing (a) Cascaded gain peaking technique. (b) CG and FRR with and without the driver amplifier. [13] © IEEE

135 GHz with a flat frequency profile owing to the cascaded gain peaking technique.

This LO chain has also been taped out and characterized separately. The measurement results show a peak P_{out} of approximately 5 dBm with a $B_{3\text{dB}}$ covering the entire D-band, the detailed characterization results are given in Section A.3.

4.7 Transceiver Characterization

The TRX is tested separately at both TX and RX modes. In TX mode measurements, the RX input, the RX output and DC connections of the RX remain open circuits. Fig. 4.28 shows the wire bonding of the TRX IC to a printed circuit board (PCB) for the TX mode measurements. In this configuration, the LO input and TX RF output are probed, while the DC and TX IF connections are first wire bonded to a PCB and then routed over PCB to be connected to the external connectors. A high performance RF substrate, Rogers R3006, with dielectric constant of 6.15 and thickness of 0.635 mm is used for the PCB.

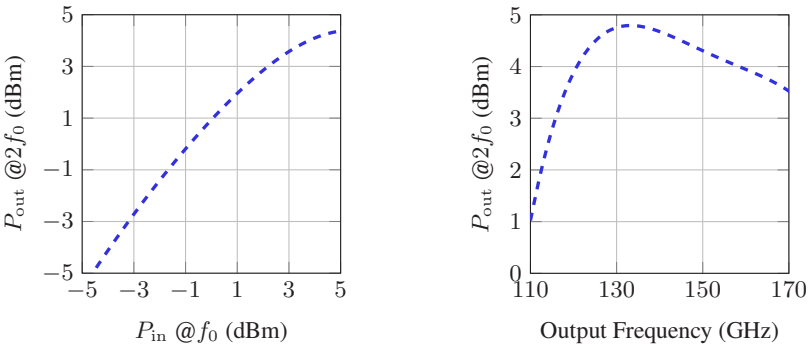


Figure 4.27: Simulated results for the doubler-amplifier chain (a) P_{in} vs. P_{out} at the input frequency of 70 GHz. (b) Output frequency vs. $P_{\text{out,max}}$. [13] © IEEE

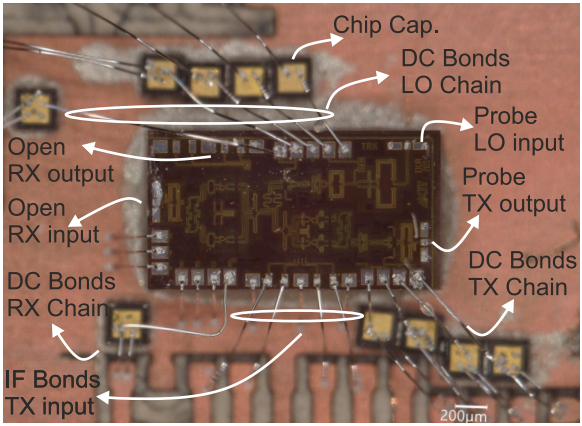


Figure 4.28: Illustration of wire bonds for the TRX IC for TX mode measurements.

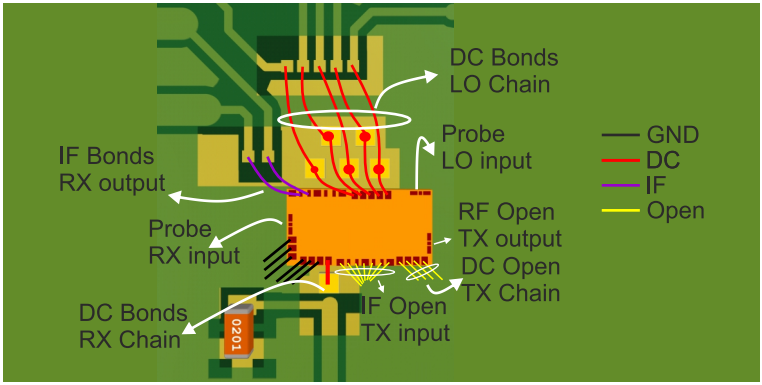


Figure 4.29: Illustration of the planned wire bonds for the TRX IC for RX mode measurements.

Similarly, for the RX mode measurements, the IC is diced to be wire bonded to a different PCB. The planned wire bonding of the IC is illustrated in Fig. 4.29. However, it has proved to be physically challenging to wire bond the DC connections of the LO chain and the RX IF connections at the same time. Therefore, the RX mode measurements are performed on the RX breakout chip. Further details of the TRX characterization in the RX mode are presented in Section 4.7.2.

The measurement setup for the TX mode measurements is depicted in Fig. 4.30(a), which is discussed in depth in Section 4.7.1. The planned measurement setups for the large-signal and noise measurements of the TRX in RX mode are also shown in Fig. 4.30(b) and Fig. 4.30(c). Fig. 4.30(b) demonstrates the planned measurement setup for the TRX in RX mode for the large-signal characterization. Here, the transmitter input and output terminals are left open, while the upconversion mixers and the PA are powered off. The LO signal is applied through a *V*- or *W*-band external source module. The RF input signal is applied through a *D*-band external source module, and its output power is varied through a DC control. The resulting I output IF signal is also left open (since it can not be bonded to the PCB due to physical limitations), while the wire bonded Q output of the differential IF signal is converted to a single-ended signal through an external balun. The resulting single-ended signal is then connected to the spectrum analyzer and the output power is recorded. All the losses due to the external components and cables are calibrated. For the NF

measurements, the measurement setup illustrated in Fig. 4.30(c) is planned. The measurement setups for the RX breakout chip are slightly different than the ones presented in Fig. 4.30(b) and Fig. 4.30(c) due to the differences in the TRX chip and the RX breakout, although the logic behind them are exactly the same. The gain method is adopted for the noise measurements, and more detailed explanations are given in Section 4.7.2.

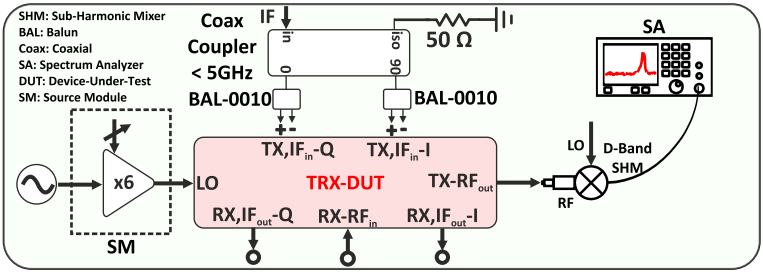
4.7.1 Transceiver Characterization in TX Mode

For the large-signal measurements in TX mode, the LO signal at *V*- (50 – 75 GHz) and *W*- (75 – 110 GHz) band is fed through VDI SGX-M *V*- and *W*-band source modules, to be frequency doubled on chip to the *D*-band. At the TX IF input, differential I/Q IF signals (0°, 90°, 180°, 270°) are generated using an external coaxial coupler and two off-chip coaxial baluns. The TX RF output at *D*-band is downconverted through a *D*-band sub-harmonic downconversion mixer and the spectral content is analyzed using a spectrum analyzer. All losses attributed to external cables and equipment are de-embedded. The measurement setup is depicted in Fig. 4.30(a).

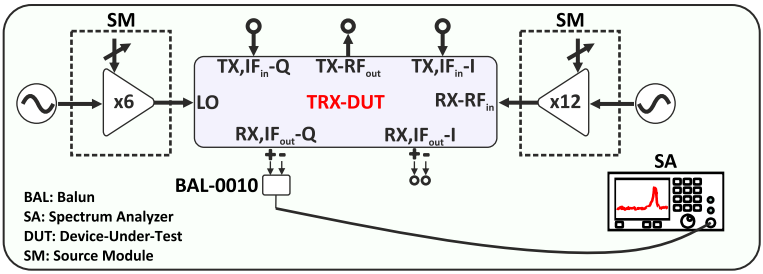
The simulated and measured large-signal performances of the TRX at TX mode are illustrated in Fig. 4.31(a) at an f_{RF} of 135 GHz and f_{IF} of 1 GHz when the DUT is supplied with an $P_{ava,LO}$ of 2 dBm. As can be seen, the simulated and measured results are in good agreement. A CG of 20 dB is observed with an OP_{1dB} of 1.6 dBm, and $P_{out,max}$ of 5.8 dBm. The TX consumes a total P_{dc} of 65 mW at small-signal region, and P_{dc} of 88 mW when driven to the $P_{out,max}$. Meanwhile, P_{dc} of the LO chain is 66 mW.

The OP_{1dB} and $P_{out,max}$ are also plotted against the f_{RF} in Fig. 4.31(b), demonstrating a B_{3dB} of 35 GHz from 125 – 160 GHz.

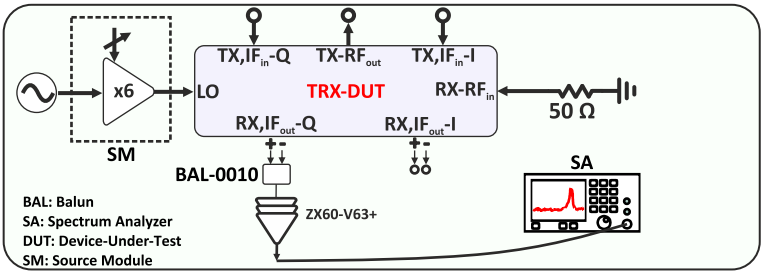
Additionally, the impact of $P_{ava,LO}$, at *V*-band, on $P_{out,max}$ is also illustrated in Fig. 4.32(a) at f_{RF} = 135 GHz, f_{IF} = 1 GHz. It can be seen that choosing an LO power at *V*-band between −1 dBm and 3 dBm results in a $P_{out,max}$ of around 4 dBm and 6 dBm. This is due to the fact that CG of the upconversion mixers is a function of $P_{ava,LO}$. This dependency is also measured for the upconversion mixers breakout, as detailed and illustrated in Section A.1, specifically in Fig. A.5(b).



(a)



(b)



(c)

Figure 4.30: Measurement setups for (a) TX P_{in}, P_{out} and CG. (b) RX P_{in}, P_{out} and CG. (c) RX NF.

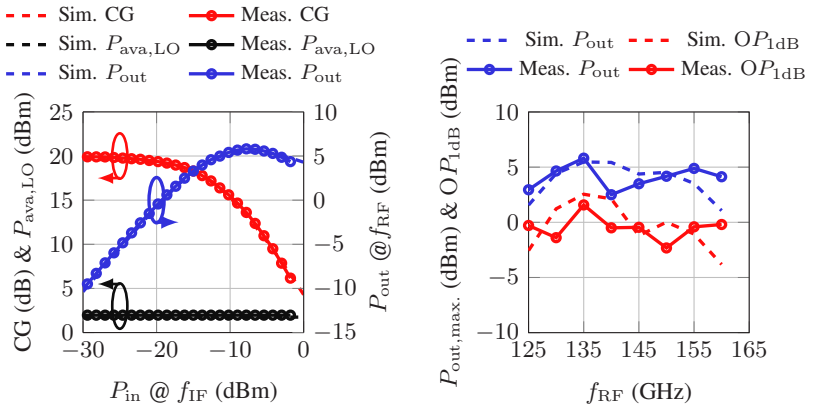


Figure 4.31: Measured and simulated TRX performance at TX mode (a) CG, P_{out} and $P_{\mathrm{ava,LO}}$ vs. P_{in} at f_{RF} = 135 GHz, f_{IF} = 1 GHz. (b) $P_{\mathrm{out,max}}$ and $OP_{1\mathrm{dB}}$ vs. f_{RF} at f_{IF} = 1 GHz.

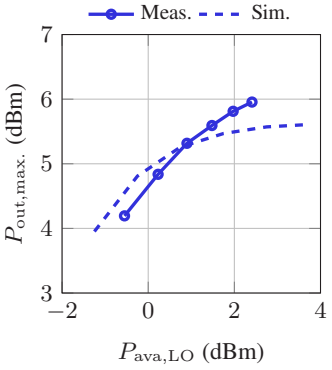


Image Suppression	33.2 dB
LO Leakage	-18 dBm

(b)

Figure 4.32: Measured and simulated TRX performance at TX mode (a) $P_{\mathrm{ava,LO}}$ vs. $P_{\mathrm{out,max}}$ at f_{RF} = 135 GHz, f_{IF} = 1 GHz. (b) LO leakage and image suppression at f_{RF} = 135 GHz, f_{IF} = 1 GHz.

Fig. 4.32(b) depicts the image suppression and LO leakage at f_{RF} = 135 GHz, f_{IF} = 1 GHz. The image suppression, the difference between the fundamental tone and the image tone, is measured as 33.2 dB. Ideally, in I/Q configuration, the image is suppressed infinitely, if the amplitude and phase imbalances are 0 dB and 0°. However, in reality, due to the non zero imbalances, the image suppression is also finite and determined by the formula given in (4.17).

As depicted in Fig. A.12, an input LO power of 2 dBm yields an output power of 4 dBm at the output power of the driver amplifier within the LO chain operating at *D*-band frequencies. This output signal is then distributed among the TX and RX mixers. A power level of −18 dBm is measured at the TX RF port for the LO frequency tone, indicating an LO leakage power of approximately −27 dBm at the output of the upconversion mixers (assuming a PA gain of 10 dB, and a coupler excess loss of 1 dB), demonstrating a mixer LO suppression of about 30 dB.

4.7.2 Transceiver Characterization in RX Mode

As mentioned in Section 4.7, the wire bonding of the TRX IC has proved to be physically quite challenging. Therefore, the RX breakout is used for the characterization in RX mode. The chip micrograph of the RX breakout is shown in Fig. 4.33. Note that the breakout chip does not include the frequency doubler and the LO buffer at the LO path, and has an LO input at *D*-band. At the RF and LO ports, marchand baluns have been adopted to facilitate the single ended on-wafer probing, and their losses are de-embedded.

The small-signal S-parameters of the RX breakout is shown in Fig. 4.34. As can be seen, the measured RL remains better than −10 dB over the whole *D*-band, mainly due to the wideband characteristics of the hybrid coupler as well as the marchand balun placed at the RF port. Between the frequency range of 124 −160 GHz, the LO port also exhibits a RL of below −10 dB. A high port-to-port isolation of more than 30 dB, is measured between the RF and LO ports.

The large-signal measurement setup is illustrated in Fig. 4.35(a). The LO signal is generated through a PNA-X connected to a *D*-band frequency extension module. This LO signal is further amplified by an external *D*-band waveguide amplifier. At the RF port, A VDI SGX-M source module is used to supply the

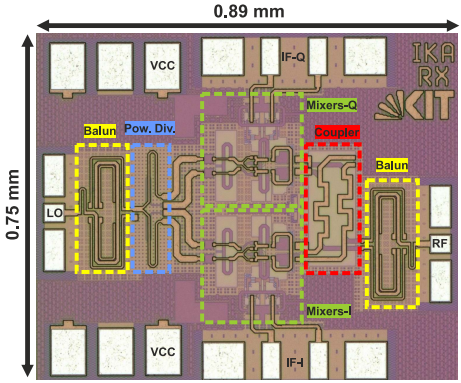


Figure 4.33: Chip micrograph of the RX breakout.

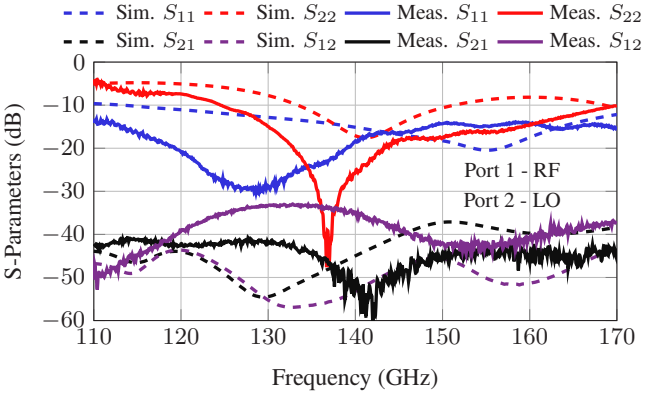
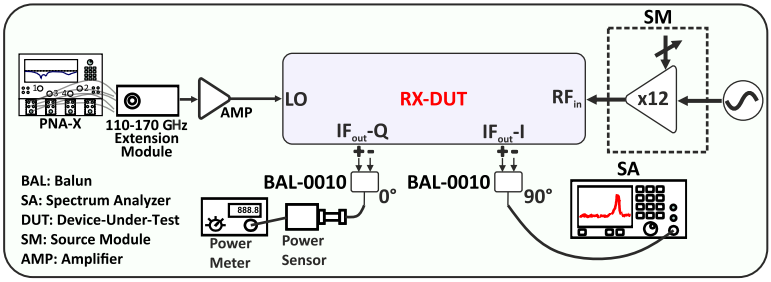
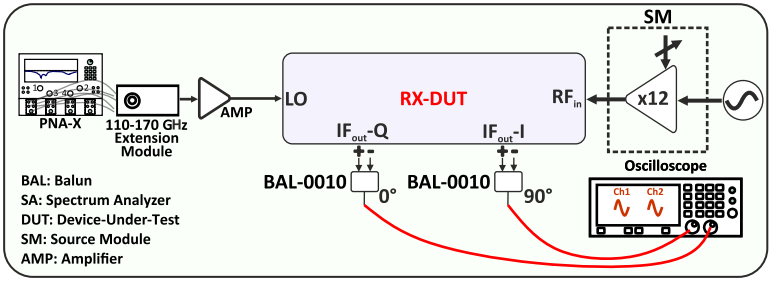


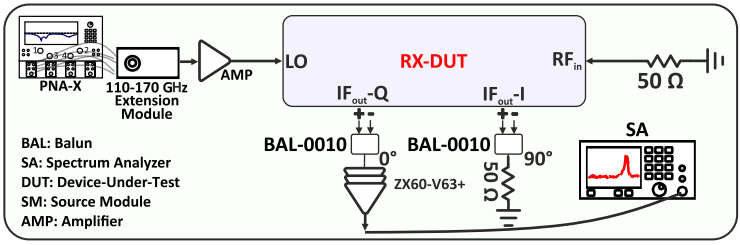
Figure 4.34: Measured and simulated S-parameters of the RX breakout.



(a)



(b)



(c)

Figure 4.35: Measurement setups for RX breakout (a) P_{in}, P_{out} and CG measurements. (b) Imbalance measurements. (c) single-sideband (SSB) NF measurements.

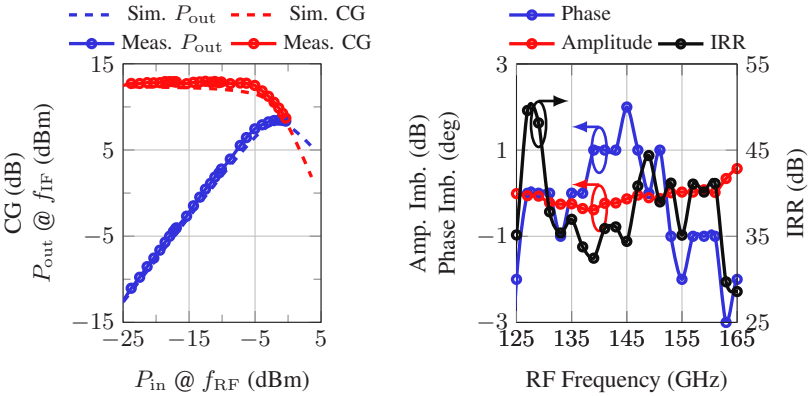


Figure 4.36: (a) Measured and simulated CG and P_{out} versus P_{in} at f_{RF} = 140 GHz and f_{IF} = 1 GHz. (b) Measured amplitude and phase imbalances, together with calculated IRR over RF B_{3dB}, at a fixed f_{IF} = 5 MHz.

RF signal, and its amplitude is varied through an external DC source. Finally, the resulting I/Q IF outputs exhibiting four distinct phases (0°, 90°, 180°, 270°) are connected to external coaxial baluns, resulting in the single ended I (90°, 270° combined) and Q (0° and 180° combined) outputs. Among them, the I signal is connected to a spectrum analyzer to analyze the spectral content while the Q signal is channeled to a power meter.

The graph in Fig. 4.36(a) illustrates the changes in CG and P_{out} with varying P_{in}. At an RF frequency of 140 GHz and an IF frequency of 1 GHz, the measured CG is 12.7 dB when the DUT is supplied with an available LO power of 1.9 dBm. A notable IP_{1dB} of −3.5 dBm is achieved, while the maximum output power reaches as high as 8.5 dBm.

The characterization of amplitude and phase imbalances between the I and Q channels is conducted across the B_{3dB} at a constant f_{IF} = 5 MHz. The choice of a relatively lower f_{IF} is intended to mitigate the influence of imperfections in the measurement setup. These imperfections may include mismatched cables, imbalances introduced by external baluns, and other similar factors. The voltage waveforms of the I/Q outputs are observed using an oscilloscope. The

measurement setup is illustrated in Fig. 4.35(b). Using the measured amplitude and phase imbalances, the IRR is calculated according to (4.17), where A and θ represent amplitude and phase imbalances, respectively, as detailed in [Raz97]. The obtained imbalances and the corresponding calculated IRR over f_{RF} are presented in Fig. 4.36(b). The IRR is calculated to be above 27 dB between 125 GHz and 165 GHz.

$$\mathrm{IRR} = -10\log_{10}\left(\frac{1 + A^2 - 2A\cos\theta}{1 + A^2 + 2A\cos\theta}\right) \tag{4.17}$$

The SSB NF is determined through the gain method [OHP12]. Initially, the differential IF outputs from the I/Q channels are converted to single-ended signals. Subsequently, the single-ended Q output signal is amplified through three consecutive ZX60-V63+ amplifiers and is connected to the spectrum analyzer. Simultaneously, the RF input and single-ended I output are terminated by 50 Ω. The gain of the stacked ZX60-V63+ amplifiers and the losses attributed to external equipment, such as cables and external baluns, are individually characterized. The output noise power density is then measured using the spectrum analyzer. The measurement setup is depicted in Fig. 4.35(c).

As explained in Section 4.2, the I/Q RX architecture facilitates the rejection of noise from the image band at the digital domain. Consequently, the actual NF of the RX corresponds to its DSB NF value, which is 3 dB better than the SSB NF for an infinite IRR. As the measured amplitude imbalance and phase error values of the IF signals (Fig. 4.36(b)) are less than 0.6 dB and 3° over the B_{3dB}, the IRR remains above 25 dB, resulting in an increase of less than 0.1 dB in DSB NF [Raz97].

The RX channel achieves a measured SSB NF of 11.2 dB at 140 GHz, corresponding to a DSB NF of 8.2 dB. Additionally, both SSB NF NF and DSB NF remain below 12 dB and 9 dB between 130 GHz and 165 GHz, respectively. The measured CG and DSB NF over f_{RF}, along with the corresponding $P_{\mathrm{ava,LO}}$ for each frequency point, are presented in Fig. 4.37. From the same figure, it can be deduced that the CG exhibits a B_{3dB} of 40 GHz, spanning the frequency range from 125 GHz to 165 GHz.

The measurements also include the impact of $P_{\mathrm{ava,LO}}$ on CG and NF. Fig. 4.38(a) provides the simulated and measured CG and DSB NF at f_{RF} of

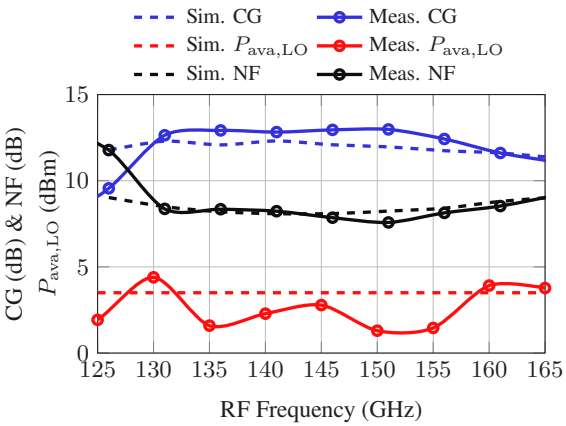


Figure 4.37: Measured and simulated CG and DSB NF over RF B_{3dB}, at a fixed f_{IF} = 1 GHz, with respective $P_{ava,LO}$.

140 GHz and f_{IF} of 1 GHz for varying $P_{ava,LO}$. The results indicate that an optimal performance is achieved within the range of $P_{ava,LO}$ from −2.5 to 2.5 dBm.

Furthermore, CG is measured at a constant f_{RF} of 140 GHz while varying f_{IF} from 1 GHz to 5 GHz. Fig. 4.38(b) illustrates a B_{3dB} IF bandwidth of 5 GHz, which aligns well with the simulation results.

4.7.3 Transceiver Characterization General Considerations

Fig. 4.39(a) shows the distribution of power consumption over the TRX components when the TX is operated at the small-signal operation, while Fig. 4.39(b) displays the same distribution with the TX is driven to the $P_{out,max}$. Note that DC MXs stand for the downconversion mixers, while UC MXs denote the upconversion mixers. When the TX is operated at the small-signal region, the total power consumption is around 166 mW. On the other hand, when the input power of TX rises, the power consumption of the upconversion mixers as well as the PA also increase. When the TX is driven into the maximum output power, total power consumption of the entire TRX rises to around 189 mW.

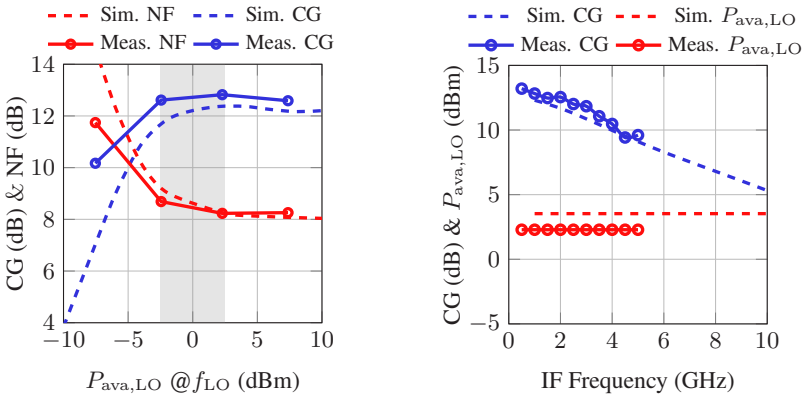


Figure 4.38: Measured and simulated (a) CG and DSB NF versus $P_{\text{ava,LO}}$, at a fixed f_{IF} = 1 GHz and f_{RF} = 140 GHz. (b) CG versus f_{IF}, at a fixed f_{RF} = 140 GHz, with respective $P_{\text{ava,LO}}$.

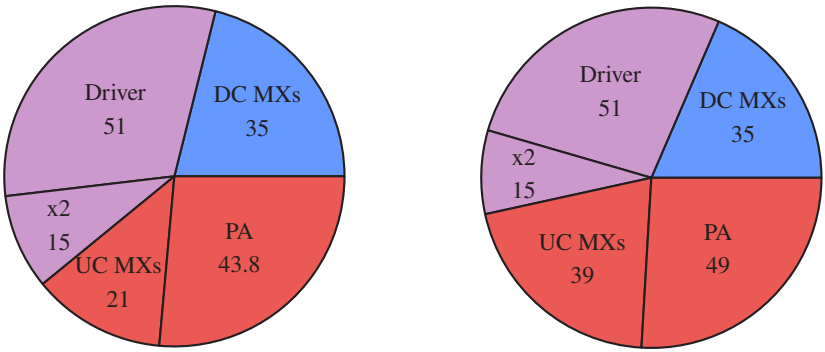


Figure 4.39: Distribution of power consumption when TX operating at (a) Small-signal. (b) $P_{\text{out,max}}$.

4.8 Conclusion

This chapter has introduced a *D*-band I/Q TRX implemented in a 130 nm SiGe BiCMOS technology with f_T/f_{MAX} of 300/500 GHz. The TX to RX spillover issue in monostatic TRXs is addressed through the mixer-first RX architecture. In comparison to RXs that conventionally incorporate LNAs, the RX demonstrated in this work exhibits superior compression behavior. Thorough examination of the noise performance of the downconversion mixers has guided design decisions to achieve the lowest possible NF. Additionally, a comprehensive comparison of various coupler types is also conducted, optimizing both the coupler and power divider to occupy the smallest IC area while maintaining favorable loss and imbalance performances. The TRX has been characterized, and the measurement results have been discussed.

A comparative study is conducted to assess how the mixer-first RX architecture in this TRX compares to a conventional RX architecture that employs an LNA as the first element in the RF path. Towards that purpose, the differential LNA presented in Section 3.2 is connected to the downconversion mixers demonstrated in this TRX, and the resulting chain consisting of the LNA and downconversion mixers is simulated. The simulation results are then compared to the mixer-first RX. Table 4.1 summarizes the performance comparison. As can be seen, the simulated NF performance of the chain including the LNA outperforms the mixer-first RX by 2.2 dB. However, the compression characteristics, namely IP_{1dB}, is improved by around 19.5 dB, while still maintaining a better OP_{1dB} behavior when the mixer-first RX is pursued. At the same time, eliminating the LNA almost halves the P_{dc}, and the total IC area is reduced by 29.5 %. If needed, the lower CG of the mixer-first RX can be compensated through off-the-shelf low-frequency amplifiers by cascading them at the IF outputs. After careful comparison, it is evident that the demonstrated mixer-first RX effectively addresses the problem of TX to RX spillover without the need for additional circuitry. As a result, this approach leads to significant savings in DC power consumption and occupied IC area.

It is worth mentioning that, while a highly isolated coupler remains crucial in monostatic TRXs to minimize TX to RX spillover, the proposed RX notably eases the isolation demands on the coupler, offering an extra degree of design freedom. Moreover, in applications where spillover is exceptionally critical,

Table 4.1: Performance comparison of the receiver architectures.

	NF (dB)	**CG (dB)**	**IP_{1dB} (dBm)**	**OP_{1dB} (dBm)**	**P_{dc} (mW)**	**Area (mm^2)**
Mixer-First	8.2	12.7	-3.5	8.2	34[a]	0.24
LNA	5.9	20	-19.7	-0.7	32	0.1
LNA-First	6	30.6	-23	6.6	66[a]	0.34

[a] excluding CC buffers

the proposed RX can still be combined with leakage cancellation methods to enhance resilience against spillover to an even higher degree.

In Table 4.2, a compilation of recently published SoA complete TRX chains is listed. Among these, the demonstrated TRX stands out by achieving the second lowest NF, thanks to its NF-focused mixer design, even without employing an LNA, while presenting the highest IP_{1dB} in terms of RX performance. Additionally, the proposed TRX is quite compact and exhibits one of the least DC power consumption. The same comparison is illustrated in Fig. 4.40.

Table 4.2: SoA TRXs above 100 GHz in Si technologies.

Ref.	Tech.[a]	Freq. (GHz)	B_{3dB} (GHz)	RX			TX			RX/TX for chipsets	
				CG (dB)	IP_{1dB} (dBm)	NF (dB)	CG (dB)	OP_{1dB} (dBm)	$P_{out,max}$ (dBm)	Area (mm^2)	P_{dc} (W)
[KAKM23]	130 nm*	140	60	22	-15.6	10.1	8.4	-11#	-8	27.2	4.1
[CZHB21]	130 nm*	126	30	27	-24	10&	23	-2#	0	1.54/1.54	0.28/0.24
[KEKM21b]	130 nm*	140	60	28.3	-28#	11.5	22.4	7#	9.5	2.04	0.99
[KANK21]	130 nm*	168	20	24	-18	11	n.a	n.a	13	8.4	1.05
[NKAK17]	130 nm*	122	12	21	-11	12.7&	n.a	n.a	5	3.72	0.63
[DCJ+23]	28 nm§	150	60	17	-5	16	n.a	8.3	13	9.2	1
[ZBD+21]	22 nm§	151	n.a	15	-20	7.5	n.a	n.a	5	2.75	1.13
This Work	130 nm*	140	35TX	12.7	-3.5	8.2	20	2.5	5.8	1.58	0.19

[a] Technology: * SiGe § CMOS # graphical estimation & simulated † core area only

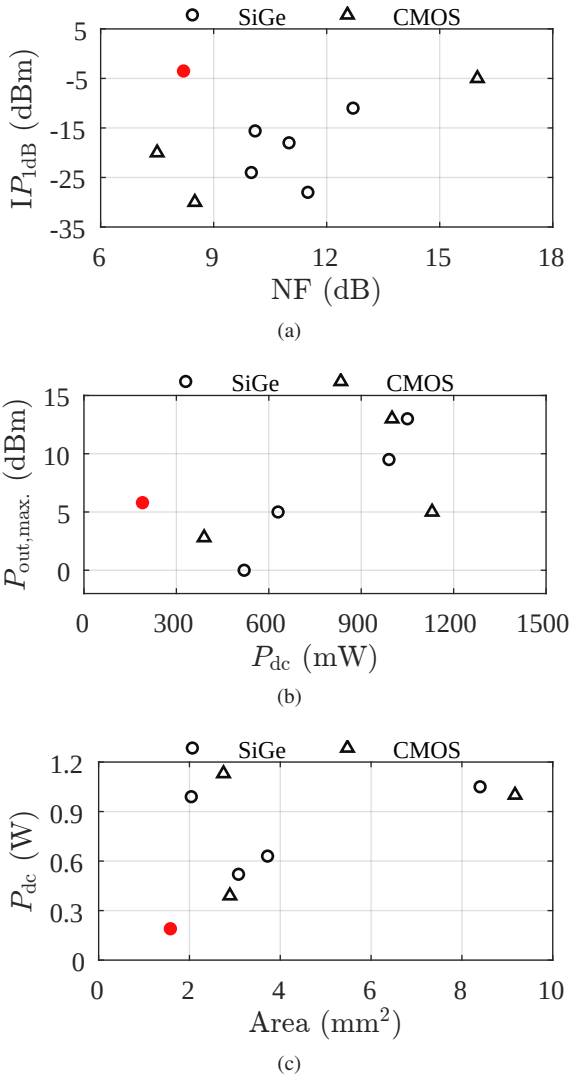


Figure 4.40: SoA TRXs above 100 GHz in Si technologies (a) NF and IP_{1dB} at the RX channel. (b) Total P_{dc} and P_{sat} of TX channel. (c) Total area and total P_{dc}.

5 Conclusion

This dissertation investigates silicon transceiver technologies operating at *D*-band frequencies for communication and radar applications, with the primary focus on two crucial aspects: high-power amplification and low-noise receiving. The investigation delves into the limitations of adopted Si-based technologies, presenting systematic design and optimization methods for mm-wave RF front ends.

A dedicated chapter explores *D*-band PAs. The exploration starts with a two-stage cascode PA implemented in a 130 nm SiGe BiCMOS technology, serving as a benchmark design for subsequent PAs discussed within the chapter. This PA operates at the center frequency of 140 GHz and achieves a small-signal gain of 16.7 dB, a saturated output power of 15 dBm, and a maximum PAE of 7.8 %, all achieved without employing any power combining technique. Following the identification of improvement points, a second PA is designed using the same SiGe BiCMOS technology with a modified-cascode approach, treating the cascode amplifier as a two-stage CE-CB device. This approach optimizes the CB device at its input terminal by introducing an interstage matching network. After optimizing the unit PA, a Wilkinson-based power combiner is added to further enhance the output power. Detailed analyses of device sizing, core layout, and matching network design result in a four-way power-combined PA with a saturated output power of 19.6 dBm and a maximum PAE of 9.5 %. This design also incorporates a bias circuit that presents a low impedance and therefore can sink the DC current at the base terminal of the CB device. The application of this bias network, as evidenced by simulations, demonstrates enhanced resilience to temperature variations. This robustness is further confirmed through the measurements, where the PA is subjected to the input power leading to 1 dB gain-compression over a 2 h duration. The resulting output power and collector current exhibit minimal deviations over time under these conditions.

Given that operating frequencies at D-band are in close proximity to the f_T and f_{MAX} of the adopted technologies, certain limits are imposed on the generated output power due to technology-related factors. The finite available gain at the output stage transistors imposes a fundamental limit on the achievable voltage swing at the output without driving the output stage device into compression at its input. This differs from low frequency PAs, where output voltage swing is primarily constrained by breakdown or supply voltages, as the active devices typically offer sufficient gain. Moreover, RF routing and increased parasitic effects further diminish the effective f_T and f_{MAX}, increasing the reduction in available gain. To address these challenges, another PA is implemented utilizing a successor SiGe BiCMOS technology with larger f_T and f_{MAX} values, potentially enhancing available gain and thus output power for D-band PAs. Employing a cascode topology, this PA exhibits improved MAG due to the enhanced f_T and f_{MAX}, resulting in boosted output power. Furthermore, leveraging the Cu BEOL in the employed technology in contrast to previous designs, reduces the losses due to RF routing and the matching networks. Additionally, a four-way Wilkinson power combiner, based on coupled lines and featuring an insertion loss of 0.4 dB, is designed, leading to an enhancement of 5.6 dB in output power compared to the unit PA. At the end, the four-way power combined PA achieves a measured saturated output power of 23.7 dBm with a maximum PAE of 16.6 %. This IC operates at the center frequency of 136 GHz and occupies an area of 1.4 mm^2.

The next chapter focuses on LNAs, one of the key components in wireless receivers. Two different LNAs are developed for the D-band applications both utilizing 130 nm SiGe BiCMOS technologies. The first features a two-stage differential cascode topology. To counteract the limited MAG at D-band frequencies, a gain boosting technique is employed by introducing a series inductance at the base terminal of the CB transistors before the AC ground. Balancing the trade-off between the amount of gain boosting and stability, a gain boosting inductance of 6 pH is chosen as a compromise. Furthermore, because of the increased frequency of operation, layout-induced parasitic capacitances becomes quite crucial. The introduced parasitic capacitances at the intermediate node between the CE and CB devices lead to a reduction in cascode device gain, effectively increasing the noise contribution of the CB. By placing a shunt inductance to resonate out the parasitic capacitances at this node, a 0.7 dB improvement is observed in NF_{min}. The measured gain of this LNA is 20 dB with an IP_{1dB} of −19.7 dBm at 140 GHz. The power

consumption is 31.8 mW and the core area occupies 0.1 mm^2. Due to the unavailability of reliable noise sources at *D*-band frequencies, NF measurements could not be performed. The simulated NF is 5.9 dB. It is worth mentioning that this differential LNA incorporates Marchand baluns at the input and output terminals for single-ended on-wafer probing during measurements. Therefore, the marchand baluns are separately taped out in a back-to-back configuration, and the measured losses are de-embedded to assess the performance of the plain differential LNA. The second LNA is developed using a successor SiGe BiCMOS technology. The evolution of active devices switching from predecessor to successor SiGe BiCMOS technology yields an improvement of 0.6 dB in $\mathrm{NF_{min}}$ at 140 GHz for cascode LNAs. Meanwhile, the associate gain — achieved when the LNA operates at the collector current density leading to the minimum $\mathrm{NF_{min}}$ — is increased by around 4 dB. Capitalizing on these technology-related advancements, a two-stage cascode LNA is simulated to have the following performance parameters at 135 GHz: a NF of 4.6 dB and a gain of 20.6 dB with an $\mathrm{IP_{1dB}}$ of −21.5 dBm while consuming a total power 13 mW. With the presented simulation results, the LNA demonstrates the best FoM among the Si based LNAs operating above 100 GHz.

The last chapter investigates a fully differential *D*-band I/Q TRX, developed using a 0.13 µm SiGe BiCMOS technology with $f_\mathrm{T}/f_\mathrm{MAX}$ of 300/500 GHz. Traditional TRXs encounter challenges with TX to RX spillover when employing an LNA as the initial component in the receiver RF path. This issue manifests as the LNA faces compression during high-power transmission at the TX output, due to poor $\mathrm{IP_{1dB}}$ performance of the LNAs. Additionally, the leaked signal can modulate the operating point of the LNA, introducing additional noise due to worsened noise matching. To address these challenges, the realized TRX adopts a mixer-first architecture in the RX channel, eliminating the LNA and tailoring the downconverting mixers for low-noise operation. This approach mitigates the TX to RX spillover issue, without requiring further leakage cancellation methods that often come with increased IC area or higher power consumption. As a result, compared to an LNA, the mixer-first RX demonstrates an $\mathrm{IP_{1dB}}$ improvement of 16.2 dB at the expense of 2.3 dB of NF, presenting a measured DSB NF of 8.2 dB and an $\mathrm{IP_{1dB}}$ of −3.5 dBm. Furthermore, the highly integrated TRX includes a frequency doubler and an LO buffer cascaded together for LO generation. The *V*- or *W*-band LO input signal frequency is doubled to the *D*-band, and amplified to generate the required LO power for the up– and downconverting mixers. The frequency

doubler and the LO buffer are co-designed for maximized bandwidth through a cascaded gain peaking approach, ensuring a flatter frequency response in the LO chain. This is targeted since the RX and TX channels exhibit wideband operation. Besides, the LO power distribution is optimized in terms of power consumption and IC area, and a moderate output power frequency doubler is chosen with a single amplification stage. In the TX channel, a differential power divider feeds the LO power to upconverting mixers operating in I/Q fashion. The resulting quadrature output signals at the RF terminals are combined through a differential hybrid coupler and then connected to a PA, achieving a maximum output power of 5.8 dBm with an OP_{1dB} of 1.6 dBm at an RF frequency of 135 GHz and an IF frequency of 1 GHz. The dimensions of the TRX are 0.91 mm by 1.74 mm, occupying 1.58 mm^2. The total power consumption is 165.7 mW when the TX channel operates in the small signal region, increasing to 189 mW when driven to the maximum output power.

This dissertation provides detailed design strategies for mm-wave PAs and LNAs, including the design, tape-out and characterization of various *D*-band PAs and LNAs with SoA performances. Beyond the design decisions, the dissertation includes thorough literature reviews and performance comparisons, enhancing the comprehension of the presented strategies. The culmination of this dissertation lies in the final chapter, which demonstrates the combination of high-power generation and low-noise receiving capabilities within an integrated TRX. This TRX comprises various building blocks, presenting a comprehensive approach to the RF front end design for mm-wave wireless systems. The TRX further exemplifies a thorough understanding of how different components work together, creating a foundation for designing mm-wave RF front ends.

A Transceiver Breakouts

Expanding on the exploration of TRX components detailed in this thesis, individual breakouts have been taped out and independently characterized. Within this chapter, the measurement results of these breakouts are presented.

The first section, Section A.1, presents a breakout where the I/Q upconversion mixers are connected to the power divider and the hybrid coupler. The measured results of this individual breakout are presented. To understand the TX capabilities further, the PA employed within the TRX is also taped out as an individual breakout and the characterization results are demonstrated in Section A.2. Lastly, Section A.3 explains the characterization of the LO chain, where the frequency doubler and the driver amplifier are cascaded together and taped out as another individual breakout.

The primary aim behind the individual characterization of the breakouts is to pinpoint the optimal operating parameters for each specific TRX block. This approach is deemed essential due to the inherent complexity involved in determining these operating points within the context of the entire TRX operation. By isolating each block separately, it becomes more feasible to fine-tune and optimize the performance of individual components. In addition to optimizing operating points, having individual breakouts of the main TRX blocks enhances the system's debug ability. By characterizing each TRX block independently, the troubleshooting process becomes more streamlined. This becomes particularly valuable in the event of unexpected behaviors or anomalies within the overall TRX system. The isolated characterization allows for a more granular analysis, facilitating the identification and resolution of any issues that may arise during the operation of the TRX.

Fig. A.1 depicts the complete die reticle developed at Institute of Radio Frequency Engineering and Electronics (IHE) with the relevant breakouts highlighted by the dashed rectangles. All the visible ICs are designed by the

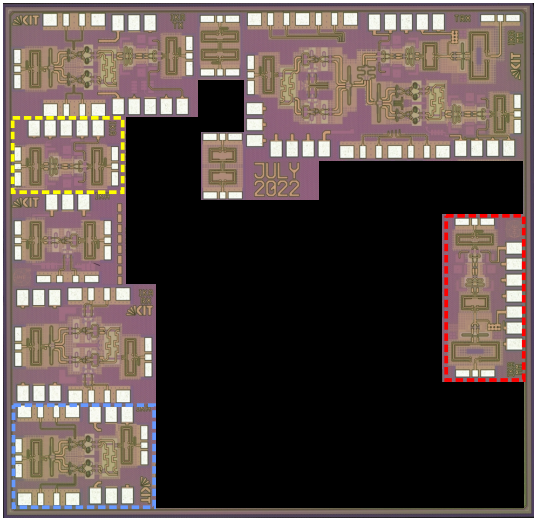


Figure A.1: Chip micrograph of the entire reticle with the marked breakouts.

author of this dissertation, and are characterized separately as well. Only the most relevant breakouts and results are displayed.

A.1 I/Q Upconverter

This section includes content and material previously published in [9].

The chip micrograph of the fabricated I/Q upconverter breakout is presented in Fig. A.2. The occupied chip area is $860 \times 630\,\mu m^2$, including the pads, and the core of the chip measures $480 \times 315\,\mu m^2$.

For the large-signal measurements, the differential I/Q IF signals (0°, 90°, 180°, 270°) are generated using an external coaxial coupler and two off-chip coaxial baluns. The LO signal is introduced through a VDI SGX-M *D*-band source module. At the RF output, a *D*-band sub-harmonic down-conversion mixer is connected to downconvert the RF signal, and the spectral content is analyzed using a spectrum analyzer. All losses attributed to external cables

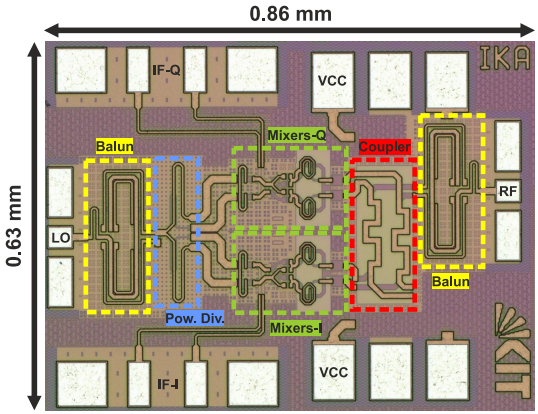


Figure A.2: Chip micrograph of the transmitter breakout. [9] © IEEE

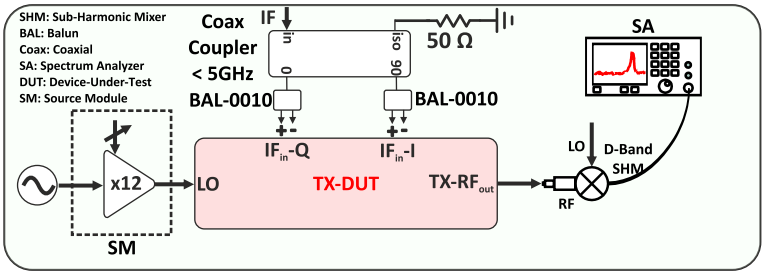


Figure A.3: Measurement setups for the I/Q upconverter breakout for large-signal measurements. [9] © IEEE

and equipment are de-embedded. The measurement setup is depicted in Fig. A.3.

Fig. A.4(a) illustrates the simulated and measured upper sideband CG and P_{out} at f_{RF} of 145 GHz and f_{IF} of 3 GHz. The CG measures at 11.2 dB, with the $OP_{1\text{dB}}$ reaching −5.5 dBm. The measured $P_{\text{out,max.}}$ is −2.2 dBm under a supply of an available LO power $P_{\text{ava,LO}}$ of 4.5 dBm and an IF power of −5.7 dBm. The IRR exceeds 20 dBc, indicating a maximum phase imbalance of 11°, a maximum amplitude imbalance of 1.7 dB, or a combination of both [Raz97], while the simulated IRR surpasses 25 dBc. The observed discrepancies can

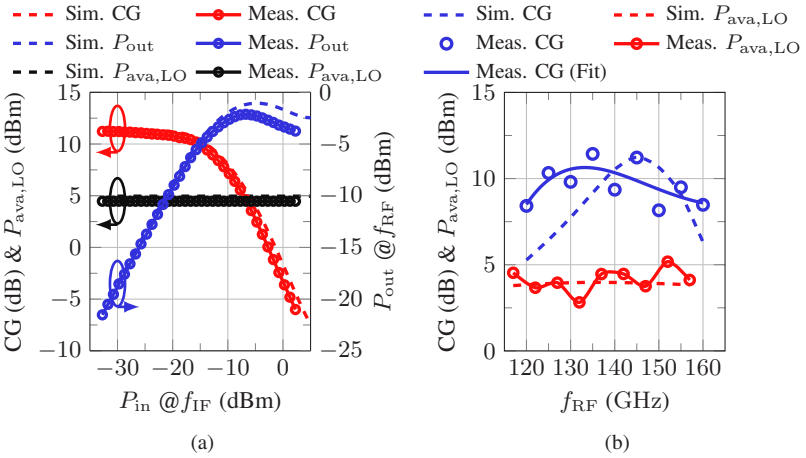


Figure A.4: (a) Measured and simulated CG and P_{out} versus P_{in} at f_{RF} = 145 GHz and f_{IF} = 3 GHz. (b) CG vs. f_{RF} at f_{IF} = 3 GHz. [9] © IEEE

be attributed to imperfections in the measurement setup, such as unmatched cables and imbalances in the external hybrid and baluns, which complicate achieving precise differential I/Q feed at the IF input.

The B_{3dB} f_{RF} is measured by keeping f_{IF} at a constant value of 3 GHz and varying f_{LO}. Fig. A.4(b) presents the CG across f_{RF}. The B_{3dB} f_{IF} is measured with a fixed f_{RF} of 145 GHz. The external coaxial-hybrid, with a cut-off frequency of 5 GHz, limits the measurement to f_{IF} up to 4 GHz. Fig. A.5(a) displays the measured and simulated CG concerning varying f_{IF}. The agreement between measurement and simulation results within the measured f_{IF} range supports assuming a B_{3dB} f_{IF} exceeding 20 GHz.

The influence of $P_{ava,LO}$ on CG and $P_{out,max}$ is depicted in Fig. A.5(b). This measurement is conducted at f_{RF} of 145 GHz and f_{IF} of 3 GHz. The plot suggests that beyond a certain point, increasing $P_{ava,LO}$ results in marginal enhancements in both parameters. The reported values are based on $P_{ava,LO}$ of 4.5 dBm. Alternatively, $P_{ava,LO}$ can be reduced to 1.7 dBm at the expense of 0.3 dB CG and 1.2 dB $P_{out,max}$.

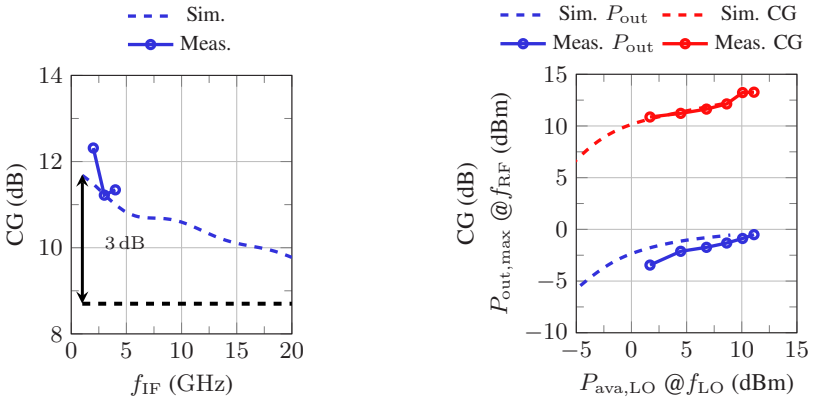


Figure A.5: Measured and simulated (a) CG vs. f_{IF} at f_{IF} = 145 GHz. (b) CG and $P_{out,max}$ vs. $P_{ava,LO}$ at f_{RF} = 145 GHz and f_{IF} = 3 GHz. [9] © IEEE

A.2 Power Amplifier

This section includes content and material previously published in [13].

The chip micrograph of the amplifier is shown in Fig. A.6, measuring 0.65 × 0.45 mm^2, including the pads as well as the marchand baluns at the input and output.

The measured and simulated small-signal measurement results are shown in Fig. A.7. Note that the S-parameter results include the impact of marchand baluns. The peak small-signal gain of 8.2 dB is measured at 145 GHz, indicating that the PA has a small-signal gain of around 10 dB when the marchand baluns are de-embedded.

The large-signal characterization setup of the PA is shown in Fig. 2.15. The PA employs a moderate device size of $5 \times 0.07 \times 0.9$ µm^2. After de-embedding the input and output marchand balun losses, the gain and P_{out} vs. P_{in} behavior are shown in Fig. A.8(a) at 134 GHz. Additionally, the P_{out} vs. the operating frequency is also illustrated at an P_{in} = 0 dBm in Fig. A.8(b). As can be

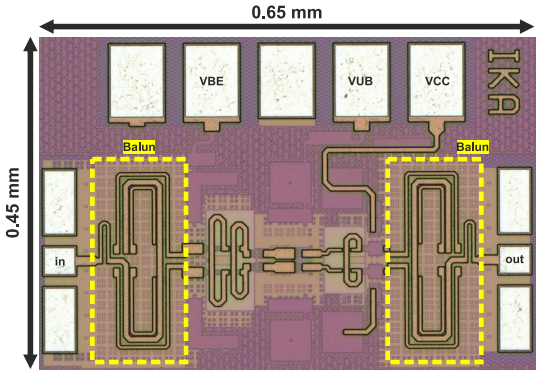


Figure A.6: Chip micrograph of the power amplifier breakout.

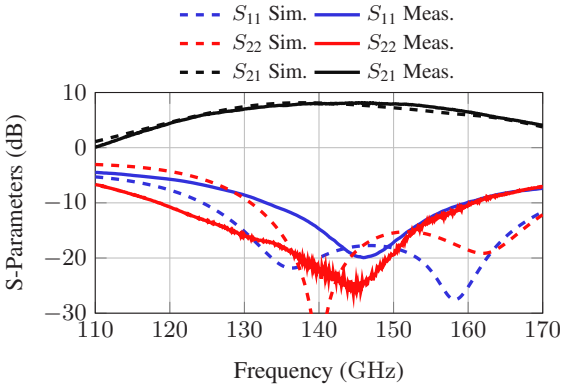


Figure A.7: Measured and simulated small-signal S-parameters of the power amplifier.

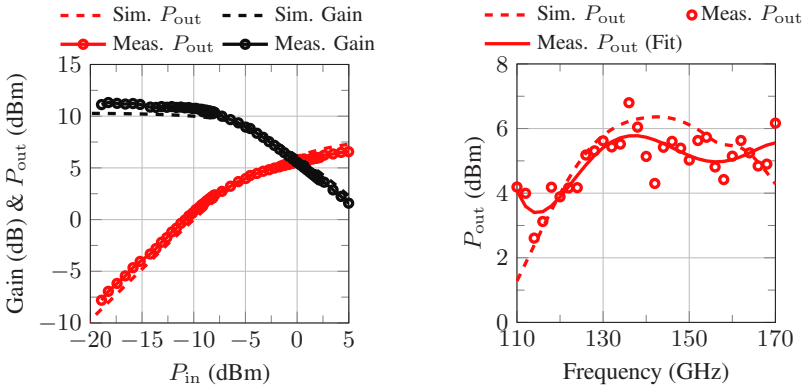


Figure A.8: Measured and simulated (a) P_{out} and Gain vs. P_{in} at 134 GHz. (b) P_{out} vs. Frequency at $P_{\text{in}} = 0$ dBm.

seen, the PA exhibits a measured O$P_{1\text{dB}}$ of 2.7 dBm while the P_{sat} is as high as 5 dBm. Similarly, as can be seen in Fig. A.8(b), the P_{out} peaks at around 134 GHz, while achieving a large-signal $B_{3\text{dB}}$ of as high as 54 GHz, covering 116 – 170 GHz.

A.3 Frequency Doubler Amplifier Chain

This section includes content and material previously published in [13].

The chip micrograph of the frequency doubler and amplifier chain is shown in Fig. A.9.

Two measurements setups have been built, where the setup in Fig. A.10(a) is used to analyze the spectral content and make sure that the frequency doubling is functional. Afterwards, the output power is measured using the setup shown in Fig. A.10(b). In both setups, the input is applied both in *V*- and *W*-bands, to cover the entire *D*-band frequency range at the output.

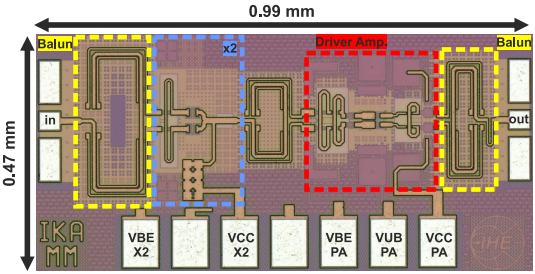
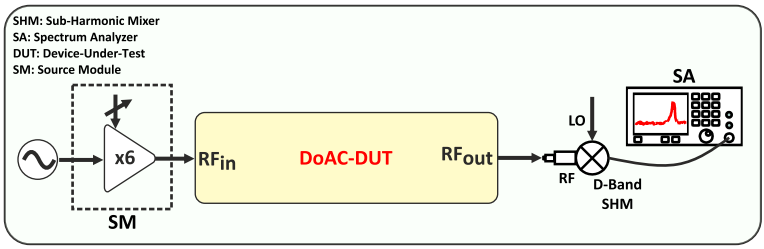
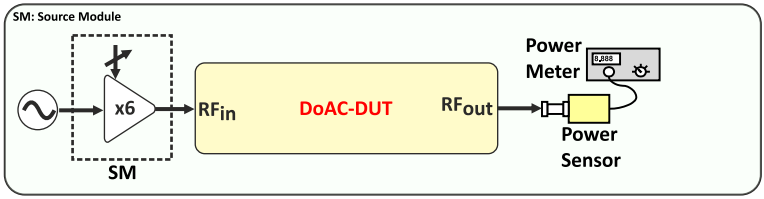


Figure A.9: Chip micrograph of the frequency doubler and driver amplifier chain breakout. [13] © IEEE



(a)



(b)

Figure A.10: Doubler-amplifier chain measurement setup for: (a) Spectrum analysis. (b) Output power. [13] © IEEE

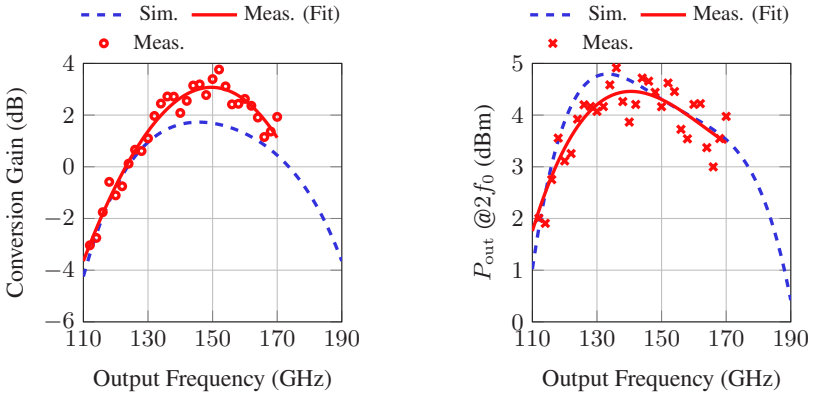


Figure A.11: Measured and simulated results: (a) Maximum conversion gain vs. frequency. (b) Maximum output power vs. frequency. [13] © IEEE

The plots in Fig. A.11(a) and Fig. A.11(b) illustrate the maximum conversion gain and maximum output power across the output frequency, respectively. In both cases, the input power is varied, and the maximum value is recorded for each frequency point. A peak conversion gain of 3.1 dB is observed at an input power of 0 dBm. Despite the measurement range being confined to 110 – 170 GHz, the strong correlation between simulations and measurements indicates a $B_{3\text{dB}}$ spanning from 123 – 173 GHz.

As depicted in Fig. A.11(b), the doubler-amplifier chain exhibits a measured peak output power of 4.5 dBm with a $B_{3\text{dB}}$ spanning from 123 – 186 GHz (51.3 %). As illustrated in Fig. 10, the maximum output power is attained at an input power level of 4 dBm, with the doubler and amplifier drawing 29 mA and 17 mA from their respective 1.2 V and 3 V supplies. This results in a total DC power consumption of 86 mW. The measured DC-RF efficiency ($\eta_{\text{dc}} = P_{\text{out}}/P_{\text{dc}}$) reaches a peak of 3.4 % and remains above 2 % across the entire D-band frequency range.

Fig. A.12 illustrates how the output power changes with respect to the input power for various frequencies. The output power reaches its maximum when an input power of around 4 dBm is applied.

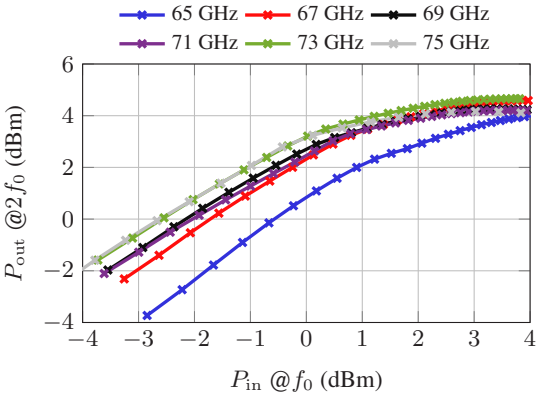


Figure A.12: Measured output power vs. input power for various input frequencies. [13] © IEEE

List of Figures

List of Tables

Bibliography

[AFAS16] Faisal Ahmed, Muhammad Furqan, Klaus Aufinger, and Andreas Stelzer. A SiGe-based broadband 100–180-GHz differential power amplifier with 11 dBm peak output power and 3THz GBW. In *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, pages 257–260. IEEE, 2016.

[AHKW18] E. Aguilar, A. Hagelauer, D. Kissinger, and R. Weigel. A low-power wideband D-band LNA in a 130 nm BiCMOS technology for imaging applications. In *2018 IEEE 18th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pages 27–29. IEEE, 2018.

[AIW20] Erick Aguilar, Vadim Issakov, and Robert Weigel. A Fundamental-Frequency 122 GHz Radar Transceiver with 5.3 dBm Single-Ended Output Power in a 130 nm SiGe Technology. In *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, pages 1215–1218, August 2020. ISSN: 2576-7216.

[AKE+21] Wael Abdullah Ahmad, Maciej Kucharski, Arzu Ergintav, Salah Abouzaid, Jan Wessel, Herman Jalli Ng, and Dietmar Kissinger. Multimode W-Band and D-Band MIMO Scalable Radar Platform. *IEEE Transactions on Microwave Theory and Techniques*, 69(1):1036–1047, 2021.

[ALH+23] Patrick James Artz, Quang Huy Le, Dang Khoa Huynh, Philipp Scholz, Thomas Kämpfe, Steffen Lehmann, Thomas Mausolf, and Friedel Gerfers. Design and Characterization of a Variable Gain D -Band LNA for Optimized Link Budgeting for a 6G Receiver in 22FDX. *IEEE Transactions on Microwave Theory and Techniques*, pages 1–10, 2023.

[AMKU22a] İbrahim Kağan Aksoyak, Matthias Möck, Mehmet Kaynak, and Ahmet Çağrı Ulusoy. A D-Band Power Amplifier with 15 dBm Psat in 0.13μm SiGe BiCMOS Technology. In *2022 IEEE 22nd*

Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), pages 5–8, 2022.

[AMKU22b] İbrahim Kağan Aksoyak, Matthias Möck, Mehmet Kaynak, and Ahmet Çağrı Ulusoy. A D-Band Power Amplifier With Four-Way Combining in 0.13 μm SiGe. *IEEE Microwave and Wireless Components Letters*, 32(11):1343–1346, 2022.

[AMU22] İbrahim Kağan Aksoyak, Matthias Möck, and Ahmet Çağrı Ulusoy. A Differential D-Band Low-Noise Amplifier in 0.13 μm SiGe. *IEEE Microwave and Wireless Components Letters*, 32(8):979–982, 2022.

[ASF+21] Ahmed S.H. Ahmed, Munkyo Seo, Ali A. Farid, Miguel Urteaga, James F. Buckwalter, and Mark J.W. Rodwell. A 200mW D-band Power Amplifier with 17.8% PAE in 250-nm InP HBT Technology. In *2020 15th European Microwave Integrated Circuits Conference (EuMIC)*, pages 1–4, 2021.

[AYG+20] Abdul Ali, Jongwon Yun, Franco Giannini, Herman Jalli Ng, Dietmar Kissinger, and Paolo Colantonio. 168-195 GHz Power Amplifier With Output Power Larger Than 18 dBm in BiCMOS Technology. *IEEE Access*, 8:79299–79309, 2020.

[AYJ+19] Abdul Ali, Jongwon Yun, Herman Jalli Ng, Dietmar Kissinger, Franco Giannini, and Paolo Colantonio. High Performance Asymmetric Coupled Line Balun at Sub-THz Frequency. *Applied Sciences*, 9(9):1907, 2019.

[BJPM15] Christoph Baer, Timo Jaeschke, Nils Pohl, and Thomas Musch. Contactless Detection of State Parameter Fluctuations of Gaseous Media Based on an mm-Wave FMCW Radar. *IEEE Transactions on Instrumentation and Measurement*, 64(4):865–872, 2015.

[BZR18] Jan Barowski, Marc Zimmermanns, and Ilona Rolfes. Millimeter-Wave Characterization of Dielectric Materials Using Calibrated FMCW Transceivers. *IEEE Transactions on Microwave Theory and Techniques*, 66(8):3683–3689, 2018.

[CB22a] Jeff Shih-Chieh Chien and James F. Buckwalter. A 111-149-GHz, Compact Power-combined Amplifier With 17.5-dBm P_sat, 16.5% PAE in 22-nm CMOS FD-SOI. In *ESSCIRC 2022-*

IEEE 48th European Solid State Circuits Conference (ESSCIRC), pages 453–456, 2022.

[CB22b] Jeff Shih-Chieh Chien and James F. Buckwalter. A Compact, 114-GHz, High-efficiency Power Amplifier in a 250-nm InP HBT Process. In *2022 IEEE/MTT-S International Microwave Symposium - IMS 2022*, pages 452–455, 2022.

[ĆBL+19] Maciej Ćwikliński, Peter Brückner, Stefano Leone, Christian Friesicke, Hermann Maßler, Roger Lozar, Sandrine Wagner, Rüdiger Quay, and Oliver Ambacher. D-Band and G-Band High-Performance GaN Power Amplifier MMICs. *IEEE Transactions on Microwave Theory and Techniques*, 67(12):5080–5089, 2019.

[CEP18] CEPT ECC. ECC Recommendation (18) 01 on Radio frequency channel/block arrangements for Fixed Service systems operating in the bands 130-134 GHz, 141-148.5 GHz, 151.5-164 GHz and 167-174.8 GHz. 2018.

[CL02] Choong-Yul Cha and Sang-Gug Lee. A 5.2GHz LNA in 0.35μm CMOS utilizing inter-stage series resonance and optimizing the substrate resistance. In *Proceedings of the 28th European Solid-State Circuits Conference*, pages 339–342, 2002.

[CN02] John Cressler and Guofu Niu. *Silicon-Germanium Heterojunction Bipolar Transistors*. 2002.

[CPLW18] Taiyun Chi, Jong Seok Park, Sensen Li, and Hua Wang. A Millimeter-Wave Polarization-Division-Duplex Transceiver Front-End With an On-Chip Multifeed Self-Interference-Canceling Antenna and an All-Passive Reconfigurable Canceller. *IEEE Journal of Solid-State Circuits*, 53(12):3628–3639, 2018.

[CQP+20] Vittorio Camarchia, Roberto Quaglia, Anna Piacibello, Duy P. Nguyen, Hua Wang, and Anh-Vu Pham. A Review of Technologies and Design Techniques of Millimeter-Wave Power Amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 68(7):2957–2983, 2020.

[CSBE18] Edmar Camargo, James Schellenberg, Lani Bui, and Nicholas Estella. F-Band, GaN Power Amplifiers. In *2018 IEEE/MTT-S International Microwave Symposium - IMS*, pages 753–756. IEEE, 2018.

[CTZ+20] Yen-Wei Chang, Tsung-Ching Tsai, Jie-Ying Zhong, Jeng-Han Tsai, and Tian-Wei Huang. A 28 GHz Linear and Efficient Power Amplifier Supporting Wideband OFDM for 5G in 28nm CMOS. In *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, pages 1093–1096. IEEE, 2020.

[CUS+16] Christopher T. Coen, Ahmet Cagri Ulusoy, Peter Song, Adrian Ildefonso, Mehmet Kaynak, Bernd Tillack, and John D. Cressler. Design and On-Wafer Characterization of G -Band SiGe HBT Low-Noise Amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 64(11):3631–3642, 2016.

[CZHB21] Sona Carpenter, Herbert Zirath, Zhongxia Simon He, and Mingquan Bao. A fully integrated D-band direct-conversion I/Q transmitter and receiver chipset in SiGe BiCMOS technology. *Journal of Communications and Networks*, 23(2):73–82, 2021.

[DB15] Saeid Daneshgar and James F. Buckwalter. A 22 dBm, 0.6 mm^2 D-Band SiGe HBT Power Amplifier Using Series Power Combining Sub-Quarter-Wavelength Baluns. In *2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pages 1–4. IEEE, 2015.

[DB18] Saeid Daneshgar and James F. Buckwalter. Compact Series Power Combining Using Subquarter-Wavelength Baluns in Silicon Germanium at 120 GHz. *IEEE Transactions on Microwave Theory and Techniques*, pages 1–16, 2018.

[DBM+20] Jean-Baptiste Dore, Didier Belot, Eric Mercier, Simon Bicais, Gregory Gougeon, Yoann Corre, Benoit Miscopein, Dimitri Ktenas, and Emilio Calvanese Strinati. Technology Roadmap for Beyond 5G Wireless Connectivity in D-band. In *2020 2nd 6G Wireless Summit (6G SUMMIT)*, pages 1–5. IEEE, 2020.

[DCJ+23] Wei Deng, Zipeng Chen, Haikun Jia, Pingda Guan, Taikun Ma, Angxiao Yan, Shiyan Sun, Xiangrong Huang, Guopei Chen, Ruichang Ma, Shengnan Dong, Luqiang Duan, Zhihua Wang, and Baoyong Chi. A D-Band Joint Radar-Communication CMOS Transceiver. *IEEE Journal of Solid-State Circuits*, 58(2):411–427, 2023.

[DDT+19] Kaushik Dasgupta, Saeid Daneshgar, Chintan Thakkar, James Jaussi, and Bryan Casper. A 26 dBm 39 GHz Power Amplifier

with 26.6% PAE for 5G Applications in 28nm bulk CMOS. In *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 235–238. IEEE, 2019.

[DSH+19] Andre Durr, Dominik Schwarz, Stephan Hafner, Martin Geiger, Fabian Roos, Martin Hitzler, Philipp Hugler, Reiner Thoma, and Christian Waldschmidt. High-Resolution 160-GHz Imaging MIMO Radar Using MMICs With On-Chip Frequency Synthesizers. *IEEE Transactions on Microwave Theory and Techniques*, 67(9):3897–3907, 2019.

[DST+23] David Del Rio, Juan F. Sevillano, Rolando Torres, Andoni Irizar, Pascal Roux, Mahmoud M. Pirbazari, Andrea Mazzanti, Jussi Saily, Antti Lamminen, Jesus de Cos, Mario Giovanni Luigi Frecassetti, Maurizio Moretto, Andrea Pallotta, and Vladimir Ermolov. A D -Band 16-Element Phased-Array Transceiver in 55-nm BiCMOS. *IEEE Transactions on Microwave Theory and Techniques*, 71(2):854–869, 2023.

[EHH+20] Mohamed Elkhouly, Michael J. Holyoak, David Hendry, Mike Zierdt, Amit Singh, Mustafa Sayginer, Shahriar Shahramian, and Yves Baeyens. D-band Phased-Array TX and RX Front Ends Utilizing Radio-on-Glass Technology. In *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 91–94, 2020.

[FAHS17] Muhammad Furqan, Faisal Ahmed, Bernd Heinemann, and Andreas Stelzer. A 15.5-dBm 160-GHz High-Gain Power Amplifier in SiGe BiCMOS Technology. *IEEE Microwave and Wireless Components Letters*, 27(2):177–179, 2017.

[FCE14] David Fritsche, Corrado Carta, and Frank Ellinger. A Broadband 200 GHz Amplifier with 17 dB Gain and 18 mW DC-Power Consumption in 0.13μm SiGe BiCMOS. *IEEE Microwave and Wireless Components Letters*, 24(11):790–792, 2014.

[FSAR19] Ali A. Farid, Arda Simsek, Ahmed S. H. Ahmed, and Mark J. W. Rodwell. A Broadband Direct Conversion Transmitter/Receiver at D-band Using CMOS 22nm FDSOI. In *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 135–138, 2019.

[FSCE17] David Fritsche, Paul Starke, Corrado Carta, and Frank Ellinger. A Low-Power SiGe BiCMOS 190-GHz Transceiver Chipset With Demonstrated Data Rates up to 50 Gbit/s Using On-Chip Antennas. *IEEE Transactions on Microwave Theory and Techniques*, 65(9):3312–3323, 2017.

[FZSS08] Xiaohua Fan, Heng Zhang, and Edgar SÁnchez-Sinencio. A Noise Reduction and Linearity Improvement Technique for a Differential Cascode LNA. *IEEE Journal of Solid-State Circuits*, 43(3):588–599, 2008.

[GBRC+15] Jesus Grajal, Alejandro Badolato, Gorka Rubio-Cidre, Luis Ubeda-Medina, Beatriz Mencia-Oliva, Antonio Garcia-Pino, Borja Gonzalez-Valdes, and Oscar Rubinos. 3-D High-Resolution Imaging Radar at 300 GHz With Enhanced FoV. *IEEE Transactions on Microwave Theory and Techniques*, 63(3):1097–1107, 2015.

[GUR19] Zach Griffith, Miguel Urteaga, and Petra Rowell. A Compact 140-GHz, 150-mW High-Gain Power Amplifier MMIC in 250-nm InP HBT. *IEEE Microwave and Wireless Components Letters*, 29(4):282–284, 2019.

[GURT22] Zach Griffith, Miguel Urteaga, Petra Rowell, and Lan Tran. A 150–175 GHz 30-dB S _21 G-band Power Amplifier with 0.25-W P _out and 15.7% PAE in a 250-nm InP HBT Technology. In *2022 IEEE/MTT-S International Microwave Symposium - IMS 2022*, pages 444–447, 2022.

[GZIR23] Senne Gielen, Yang Zhang, Mark Ingels, and Patrick Reynaert. A D-band 20.4 dBm OP1dB Transformer-Based Power Amplifier With 23.6% PAE In A 250-nm InP HBT Technology. In *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 309–312, 2023.

[HBB+22] Steffen Hansen, Christian Bredendiek, Gunnar Briese, Andre Froehly, Reinhold Herschel, and Nils Pohl. A SiGe-Chip-Based D -Band FMCW-Radar Sensor With 53-GHz Tuning Range for High Resolution Measurements in Industrial Applications. *IEEE Transactions on Microwave Theory and Techniques*, 70(1):719–731, 2022.

[Hey21] Payam Heydari. Transceivers for 6G Wireless Communications: Challenges and Design Solutions. In *2021 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–8. IEEE, 2021.

[HFA+18] Hiroshi Hamada, Takuya Fujimura, Ibrahim Abdo, Kenichi Okada, Ho-Jin Song, Hiroki Sugiyama, Hideaki Matsuzaki, and Hideyuki Nosaka. 300-GHz. 100-Gb/s InP-HEMT Wireless Transceiver Using a 300-GHz Fundamental Mixer. In *2018 IEEE/MTT-S International Microwave Symposium - IMS*, pages 1480–1483. IEEE, 2018.

[HRP+19] Julio Heredia, Miquel Ribo, Lluis Pradell, Selin Tolunay Wipf, Alexander Goritz, Matthias Wietstruck, Christian Wipf, and Mehmet Kaynak. A 125–143-GHz Frequency-Reconfigurable BiCMOS Compact LNA Using a Single RF-MEMS Switch. *IEEE Microwave and Wireless Components Letters*, 29(5):339–341, 2019.

[HSB+20] Abdelaziz Hamani, Alexandre Siligaris, Benjamin Blampey, Cedric Dehos, and Jose Luis Gonzalez Jimenez. A 125.5-157 GHz 8 dB NF and 16 dB of Gain D-band Low Noise Amplifier in CMOS SOI 45 nm. In *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, pages 197–200, 2020.

[JJK+20] Tae Hwan Jang, Kyung Pil Jung, Jin-Seob Kang, Chul Woo Byeon, and Chul Soon Park. 120-GHz 8-Stage Broadband Amplifier With Quantitative Stagger Tuning Technique. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 67(3):785–796, 2020.

[Joh65] E. Johnson. Physical limitations on frequency and power parameters of transistors. In *IRE International Convention Record*, volume 13, pages 27–34. Institute of Electrical and Electronics Engineers, 1965.

[KAKM23] Alper Karakuzulu, Wael Abdullah Ahmad, Dietmar Kissinger, and Andrea Malignaggi. A Four-Channel Bidirectional D -Band Phased-Array Transceiver for 200 Gb/s 6G Wireless Communications in a 130-nm BiCMOS Technology. *IEEE Journal of Solid-State Circuits*, 58(5):1310–1322, 2023.

[KANK21] Maciej Kucharski, Wael Abdullah Ahmad, Herman Jalli Ng, and Dietmar Kissinger. Monostatic and Bistatic G -Band BiCMOS

Radar Transceivers With On-Chip Antennas and Tunable TX-to-RX Leakage Cancellation. *IEEE Journal of Solid-State Circuits*, 56(3):899–913, 2021.

[KAS+11] Ingmar Kallfass, Jochen Antes, Thomas Schneider, Fabian Kurz, Daniel Lopez-Diaz, Sebastian Diebold, Hermann Massler, Arnulf Leuther, and Axel Tessmann. All Active MMIC-Based Wireless Communication at 220 GHz. *IEEE Trans. THz Sci. Technol.*, 1(2):477–487, 2011.

[KBW+17] Maciej Kucharski, Johannes Borngräber, Defu Wang, Dietmar Kissinger, and Herman Jalli Ng. A 109–137 GHz power amplifier in SiGe BiCMOS with 16.5 dBm output power and 12.8% PAE. In *2017 47th European Microwave Conference (EuMC)*, pages 1021–1024, 2017.

[KEKM21a] Alper Karakuzulu, Mohamed Hussein Eissa, Dietmar Kissinger, and Andrea Malignaggi. A Broadband 110–170-GHz Stagger-Tuned Power Amplifier With 13.5-dBm Psat in 130-nm SiGe. *IEEE Microwave and Wireless Components Letters*, 31(1):56–59, 2021.

[KEKM21b] Alper Karakuzulu, Mohamed Hussein Eissa, Dietmar Kissinger, and Andrea Malignaggi. Full D-Band Transmit–Receive Module for Phased Array Systems in 130-nm SiGe BiCMOS. *IEEE Solid-State Circuits Letters*, 4:40–43, 2021.

[KKN18] Maciej Kucharski, Dietmar Kissinger, and Herman Jalli Ng. A Monostatic E-Band Radar Transceiver with a Tunable TX-to-RX Leakage Canceler for Automotive Applications. In *2018 IEEE/MTT-S International Microwave Symposium - IMS*, pages 591–594. IEEE, 2018.

[KKR17] Dong-Hyun Kim, Doyoon Kim, and Jae-Sung Rieh. A D -Band CMOS Amplifier With a New Dual-Frequency Interstage Matching Technique. *IEEE Transactions on Microwave Theory and Techniques*, 65(5):1580–1588, 2017.

[KNK19] Maciej Kucharski, Herman Jalli Ng, and Dietmar Kissinger. An 18 dBm 155-180 GHz SiGe Power Amplifier Using a 4-Way T-Junction Combining Network. In *ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)*, pages 333–336, 2019.

[LCL+22a] Xingcun Li, Wenhua Chen, Shuyang Li, Yunfan Wang, Fei Huang, Xiang Yi, Ruonan Han, and Zhenghe Feng. A High-Efficiency 142–182-GHz SiGe BiCMOS Power Amplifier With Broadband Slotline-Based Power Combining Technique. *IEEE Journal of Solid-State Circuits*, 57(2):371–384, 2022.

[LCL+22b] Xingcun Li, Wenhua Chen, Shuyang Li, Huibo Wu, Xiang Yi, Ruonan Han, and Zhenghe Feng. A 110-to-130GHz SiGe BiCMOS Doherty Power Amplifier With Slotline-Based Power-Combining Technique Achieving textbackslash-textgreater22dBm Saturated Output Power and Power Back-off Efficiency. In *2022 IEEE International Solid- State Circuits Conference (ISSCC)*, pages 316–318. IEEE, 2022.

[LCW+22] Xingcun Li, Wenhua Chen, Huibo Wu, Shuyang Li, Xiang Yi, Ruonan Han, and Zhenghe Feng. A 110-to-130 GHz SiGe BiCMOS Doherty Power Amplifier With a Slotline-Based Power Combiner. *IEEE Journal of Solid-State Circuits*, 57(12):3567–3581, 2022.

[LNA+23] Eythan Lam, Kang Ning, Ahmed S.H. Ahmed, Mark Rodwell, and James F. Buckwalter. A Multi-stage 19.2-dBm, 30.4%-PAE D-band Power Amplifier in a 250-nm InP HBT Process. In *2023 IEEE/MTT-S International Microwave Symposium - IMS 2023*, pages 1042–1045, 2023.

[LR14] Hsin-Chang Lin and Gabriel M. Rebeiz. A 110–134-GHz SiGe Amplifier With Peak Output Power of 100–120 mW. *IEEE Transactions on Microwave Theory and Techniques*, 62(12):2990–3000, 2014.

[LR21] Siwei Li and Gabriel M. Rebeiz. A 130-151 GHz 8-Way Power Amplifier with 16.8-17.5 dBm Psat and 11.7-13.4% PAE Using CMOS 45nm RFSOI. In *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 115–118. IEEE, 2021.

[LR22] Siwei Li and Gabriel M. Rebeiz. High Efficiency D-Band Multiway Power Combined Amplifiers With 17.5–19-dBm Psat and 14.2–12.1% Peak PAE in 45-nm CMOS RFSOI. *IEEE Journal of Solid-State Circuits*, 57(5):1332–1343, 2022.

[MAU22] Matthias Möck, İbrahim Kağan Aksoyak, and Ahmet Çağrı Ulusoy. A High-Efficiency D-Band Frequency Doubler in 22-nm

FDSOI CMOS. In *2022 17th European Microwave Integrated Circuits Conference (EuMIC)*, pages 272–275. IEEE, 2022.

[MAU24] Matthias Möck, İbrahim Kağan Aksoyak, and Ahmet Çağrı Ulusoy. A 4.5 dBm SiGe Doubler-Amplifier Chain Covering the Entire D-Band. In *2024 IEEE 24th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pages 29–32, January 2024. ISSN: 2474-9761.

[MCA17] Ali Mostajeran, Andreia Cathelin, and Ehsan Afshari. A 170-GHz Fully Integrated Single-Chip FMCW Imaging Radar with 3-D Imaging Capability. *IEEE Journal of Solid-State Circuits*, 52(10):2721–2734, 2017.

[MGV+15] Alaa Medra, Davide Guermandi, Kristof Vaesen, Qixian Shi, Piet Wambacq, and Vito Giannini. An 80-GHz low noise amplifier resilient to the TX-spillover in phase-modulated continuous-wave radars. In *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 323–326. IEEE, 2015.

[MKM+14] A. Margomenos, A. Kurdoghlian, M. Micovic, K. Shinohara, D. F. Brown, A. L. Corrion, H. P. Moyer, S. Burnham, D. C. Regan, R. M. Grabar, C. McGuire, M. D. Wetzel, R. Bowen, P. S. Chen, H. Y. Tai, A. Schmitz, H. Fung, A. Fung, and D. H. Chow. GaN Technology for E, W and G-Band Applications. In *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pages 1–4, 2014.

[MMW+19] Thomas Merkle, Dominik Meier, Sandrine Wagner, Axel Tessmann, Michael Kuri, Hermann Massler, and Arnulf Leuther. Broadband 240-GHz Radar for Non-Destructive Testing of Composite Materials. *IEEE Journal of Solid-State Circuits*, 54(9):2388–2401, 2019.

[MPK+21] Tim Maiwald, Julian Potschka, Katharina Kolb, Marco Dietz, Klaus Aufinger, Akshay Visweswaran, and Robert Weigel. A Full D-Band Low Noise Amplifier in 130 nm SiGe BiCMOS using Zero-Ohm Transmission Lines. In *2020 15th European Microwave Integrated Circuits Conference (EuMIC)*, pages 13–16, 2021.

[MRC23] Arya Moradinia, Sunil G. Rao, and John D. Cressler. A SiGe HBT D-Band LNA Utilizing Asymmetric Broadside Coupled Lines. *IEEE Microw. Wireless Tech. Lett.*, 33(6):707–710, 2023.

[MTB23] Yash Mehta, Sidharth Thomas, and Aydin Babakhani. A 140–220-GHz Low-Noise Amplifier With 6-dB Minimum Noise Figure and 80-GHz Bandwidth in 130-nm SiGe BiCMOS. *IEEE Microwave and Wireless Technology Letters*, 33(2):200–203, 2023.

[NFRB20] Kang Ning, Yihao Fang, Mark Rodwell, and James Buckwalter. A 130-GHz Power Amplifier in a 250-nm InP Process with 32% PAE. In *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 1–4. IEEE, 2020.

[NKAK17] Herman Jalli Ng, Maciej Kucharski, Wael Ahmad, and Dietmar Kissinger. Multi-Purpose Fully Differential 61- and 122-GHz Radar Transceivers for Scalable MIMO Sensor Platforms. *IEEE Journal of Solid-State Circuits*, 52(9):2242–2255, 2017.

[NSL+19] Mehrdad Nosrati, Shahram Shahsavari, Sanghoon Lee, Hua Wang, and Negar Tavassolian. A Concurrent Dual-Beam Phased-Array Doppler Radar Using MIMO Beamforming Techniques for Short-Range Vital-Signs Monitoring. *IEEE Transactions on Antennas and Propagation*, 67(4):2390–2404, 2019.

[OB22] Everett O'Malley and James F. Buckwalter. A 1-W/mm2, 140-GHz SiGe HBT Power Amplifier using Optimized Embedding Techniques. In *2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, pages 53–56, 2022.

[OHP12] Erik Ojefors, Bernd Heinemann, and Ullrich R. Pfeiffer. Subharmonic 220- and 320-GHz SiGe HBT Receiver Front-Ends. *IEEE Transactions on Microwave Theory and Techniques*, 60(5):1397–1404, 2012.

[ORW+15] Michael A. Oakley, Uppili S. Raghunathan, Brian R. Wier, Partha Sarathi Chakraborty, and John D. Cressler. Large-Signal Reliability Analysis of SiGe HBT Cascode Driver Amplifiers. *IEEE Transactions on Electron Devices*, 62(5):1383–1389, 2015.

[PR20] Bart Philippe and Patrick Reynaert. A 15dBm 12.8%-PAE Compact D-Band Power Amplifier with Two-Way Power Combining

in 16nm FinFET CMOS. In *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, pages 374–376, 2020.

[PRM21] Ibrahim Petricli, Domenico Riccardi, and Andrea Mazzanti. D-Band SiGe BiCMOS Power Amplifier With 16.8dBm P_1dB and 17.1% PAE Enhanced by Current-Clamping in Multiple Common-Base Stages. *IEEE Microwave and Wireless Components Letters*, 31(3):288–291, 2021.

[PVK+18] Dristy Parveg, Mikko Varonen, Denizhan Karaca, Ali Vahdati, Mikko Kantanen, and Kari A. I. Halonen. Design of a D-Band CMOS Amplifier Utilizing Coupled Slow-Wave Coplanar Waveguides. *IEEE Transactions on Microwave Theory and Techniques*, 66(3):1359–1373, 2018.

[PWJS16] Matthias Porranzl, Christoph Wagner, Herbert Jaeger, and Andreas Stelzer. Quasi-circulator based automotive monostatic transceiver with integrated leakage canceler. In *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, pages 13–16. IEEE, 2016.

[Raz97] B. Razavi. Design considerations for direct-conversion receivers. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 44(6):428–435, 1997.

[Raz11] Behzad Razavi. *RF Microelectronics (2nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series)*. Prentice Hall Press, USA, 2nd edition, 2011.

[RC21] Sunil G. Rao and John D. Cressler. A D -Band SiGe Power Amplifier Using a Four-Way Coupled-Line Wilkinson Combiner. *IEEE Microwave and Wireless Components Letters*, 31(11):1239–1242, 2021.

[RKF+17] Lingyun Ren, Lingqin Kong, Farnaz Foroughian, Haofei Wang, Paul Theilmann, and Aly E. Fathy. Comparison Study of Noncontact Vital Signs Detection Using a Doppler Stepped-Frequency Continuous-Wave Radar and Camera-Based Imaging Photoplethysmography. *IEEE Transactions on Microwave Theory and Techniques*, 65(9):3519–3529, 2017.

[SCE20] Paul Starke, Corrado Carta, and Frank Ellinger. High-Linearity 19-dB Power Amplifier for 140–220 GHz, Saturated at 15 dBm,

in 130-nm SiGe. *IEEE Microwave and Wireless Components Letters*, 30(4):403–406, 2020.

[Sch08] Hermann Schumacher. *Modern Semiconductor Devices - Lecture Notes*. 2008.

[SFCE17] Paul Stärke, David Fritsche, Corrado Carta, and Frank Ellinger. A 24.7 dB low noise amplifier with variable gain and tunable matching in 130 nm SiGe at 200 GHz. In *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, pages 5–8, 2017.

[SHZ+23] Mustafa Sayginer, Michael Holyoak, Mike Zierdt, Mohamed Elkhouly, Joe Weiner, Yves Baeyens, and Shahriar Shahramian. A 110-170 GHz Phase-Invariant Variable-Gain Power Amplifier Module with 20-22 dBm Psatand 30 dBm OIP3 Utilizing SiGe HBT RFICs. In *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 305–308, 2023.

[SJK+16] Hyuk Su Son, Joo Young Jang, Dong Min Kang, Hae Jin Lee, and Chul Soon Park. A 109 GHz CMOS Power Amplifier With 15.2 dBm Psat and 20.3 dB Gain in 65-nm CMOS Technology. *IEEE Microwave and Wireless Components Letters*, 26(7):510–512, 2016.

[SJK+19] Hyuk Su Son, Tae Hwan Jang, Seung Hun Kim, Kyung Pil Jung, Joon Hyung Kim, and Chul Soon Park. Pole-Controlled Wideband 120 GHz CMOS Power Amplifier for Wireless Chip-to-Chip Communication in 40-nm CMOS Process. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 66(8):1351–1355, 2019.

[SLK+18] H. S. Son, C. J. Lee, D. M. Kang, T. H. Jang, H. S. Lee, S. H. Kim, C. W. Byeon, and C. S. Park. A D-band CMOS power amplifier for wireless chip-to-chip communications with 22.3 dB gain and 12.2 dBm P1dB in 65-nm CMOS technology. In *2018 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, pages 35–38. IEEE, 2018.

[SPD+16] Sherif Shakib, Hyun-Chul Park, Jeremy Dunworth, Vladimir Aparin, and Kamran Entesari. A Highly Efficient and Linear Power Amplifier for 28-GHz 5G Phased Array Radios in 28-nm

CMOS. *IEEE Journal of Solid-State Circuits*, 51(12):3020–3036, 2016.

[SR18] Dragan Simic and Patrick Reynaert. A 14.8 dBm 20.3 dB Power Amplifier for D-band Applications in 40 nm CMOS. In *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 232–235, 2018.

[SRK+22] Badou Sene, Daniel Reiter, Herbert Knapp, Hao Li, Tobias Braun, and Nils Pohl. An Automotive D -Band FMCW Radar Sensor Based on a SiGe-Transceiver MMIC. *IEEE Microwave and Wireless Components Letters*, 32(3):194–197, 2022.

[SRL00] H. Samavati, H. R. Rategh, and T. H. Lee. A 5-GHz CMOS wireless LAN receiver front end. *IEEE Journal of Solid-State Circuits*, 35(5):765–772, 2000.

[SS75] N.O. Sokal and A.D. Sokal. Class E-A new class of high-efficiency tuned single-ended switching power amplifiers. *IEEE Journal of Solid-State Circuits*, 10(3):168–176, 1975.

[SS04] Adel S. Sedra and Kenneth C. Smith. *Microelectronic Circuits*. Oxford University Press, fifth edition, 2004.

[SUZC15] Robert L. Schmid, Ahmet Çağrı Ulusoy, Saeed Zeinolabedinzadeh, and John D. Cressler. A Comparison of the Degradation in RF Performance Due to Device Interconnects in Advanced SiGe HBT and CMOS Technologies. *IEEE Transactions on Electron Devices*, 62(6):1803–1810, 2015.

[SYV+15] Thomas Spreng, Shuai Yuan, Vaclav Valenta, Hermann Schumacher, Uwe Siart, and Volker Ziegler. Wideband 120 GHz to 140 GHz MIMO radar: System design and imaging results. In *2015 European Microwave Conference (EuMC)*, pages 430–433. IEEE, 2015.

[TAD+23] Esref Turkmen, Ibrahim Kagan Aksoyak, Pavle Djondovic, Selahattin Berk Yilmaz, Wojciech Debski, Wolfgang Winkler, and Ahmet Çağrı Ulusoy. A 223–276-GHz Cascadable FMCW Transceiver in 130-nm SiGe BiCMOS for Scalable MIMO Radar Arrays. *IEEE Transactions on Microwave Theory and Techniques*, pages 1–20, 2023.

[TBG+18] Esref Turkmen, Abdurrahman Burak, Alper Guner, Ilker Kalyoncu, Mehmet Kaynak, and Yasar Gurbuz. A SiGe HBT D

-Band LNA With Butterworth Response and Noise Reduction Technique. *IEEE Microwave and Wireless Components Letters*, 28(6):524–526, 2018.

[THL16] Jianxuan Tu, Taesong Hwang, and Jenshan Lin. Respiration Rate Measurement Under 1-D Body Motion Using Single Continuous-Wave Doppler Radar Vital Sign Detection System. *IEEE Transactions on Microwave Theory and Techniques*, 64(6):1937–1946, 2016.

[TNM+20] Xinyan Tang, Johan Nguyen, Alaaeldien Medra, Khaled Khalaf, Akshay Visweswaran, Bjorn Debaillie, and Piet Wambacq. Design of D-Band Transformer-Based Gain-Boosting Class-AB Power Amplifiers in Silicon Technologies. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 67(5):1447–1458, 2020.

[TNM+21a] Xinyan Tang, Johan Nguyen, Giovanni Mangraviti, Zhiwei Zong, and Piet Wambacq. A 140 ghz t/r front-end module in 22 nm fd-soi cmos. In *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 35–38. IEEE, 2021.

[TNM+21b] Xinyan Tang, Johan Nguyen, Giovanni Mangraviti, Zhiwei Zong, and Piet Wambacq. A 140 GHz T/R Front-End Module in 22 nm FD-SOI CMOS. In *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 35–38. IEEE, 2021.

[UKV+13] A. Cagri Ulusoy, Mehmet Kaynak, Vaclav Valenta, Bernd Tillack, and Hermann Schumacher. A 110 GHz LNA with 20dB gain and 4dB noise figure in an 0.13μm SiGe BiCMOS technology. In *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, pages 1–3. IEEE, 2013.

[USK+15] A. Cagri Ulusoy, Peter Song, Wasif T. Khan, Mehmet Kaynak, Bernd Tillack, John Papapolymerou, and John D. Cressler. A SiGe D-Band Low-Noise Amplifier Utilizing Gain-Boosting Technique. *IEEE Microwave and Wireless Components Letters*, 25(1):61–63, 2015.

[UTC+18] Berktug Ustundag, Esref Turkmen, Barbaros Cetindogan, Alper Guner, Mehmet Kaynak, and Yasar Gurbuz. Low-Noise Amplifiers for W-Band and D-Band Passive Imaging Systems in SiGe BiCMOS Technology. In *2018 Asia-Pacific Microwave Conference (APMC)*, pages 651–653. IEEE, 2018.

[VHdM+20] Akshay Visweswaran, Alexander Haag, Carmine de Martino, Karina Schneider, Tim Maiwald, Bastien Vignon, Klaus Aufinger, Marco Spirito, Thomas Zwick, and Piet Wambacq. An integrated 132-147GHz power source with +27dBm EIRP. In *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 219–222. IEEE, 2020.

[VHv+05] H. Veenstra, G.A.M. Hurkx, D. van Goor, H. Brekelmans, and J. R. Long. Analyses and design of bias circuits tolerating output voltages above BV/sub CEO. *IEEE Journal of Solid-State Circuits*, 40(10):2008–2018, 2005.

[Voi13] Sorin Voinigescu. *High-frequency integrated circuits*. Cambridge University Press, 2013.

[VVT+19] Akshay Visweswaran, Bastien Vignon, Xinyan Tang, Steven Brebels, Bjorn Debaillie, and Piet Wambacq. A 112-142GHz Power Amplifier with Regenerative Reactive Feedback achieving 17dBm peak P sat at 13% PAE. In *ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)*, pages 337–340, 2019.

[WML17] Rainer Weber, Hermann Massler, and Arnulf Leuther. D-band low-noise amplifier MMIC with 50 % bandwidth and 3.0 dB noise figure in 100 nm and 50 nm mHEMT technology. In *2017 IEEE MTT-S International Microwave Symposium (IMS)*, pages 756–759. IEEE, 2017.

[WW20] Fei Wang and Hua Wang. 24.1 A 24-to-30GHz Watt-Level Broadband Linear Doherty Power Amplifier with Multi-Primary Distributed-Active-Transformer Power-Combining Supporting 5G NR FR2 64-QAM with >19dBm Average P _out and >19% Average PAE. In *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, pages 362–364. IEEE, 2020.

[WWW20] Fei Wang, Adam Wang, and Hua Wang. A 22-37 GHz Broadband Compact Linear Mm-Wave Power Amplifier Supporting 64-/256-/512-QAM Modulations for 5G Communications. In *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, pages 1105–1108. IEEE, 2020.

[Yan88] E.S. Yang. *Microelectronic Devices*. Electrical Engineering. McGraw-Hill, 1988.

[YE15] Roee Ben Yishay and Danny Elad. A 17.8 dBm 110–130 GHz Power Amplifier and doubler chain in SiGe BiCMOS technology. In *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 391–394, 2015.

[YPM+21] Byeonghun Yun, Dae-Woong Park, Hafiz Usman Mahmood, Doyoon Kim, and Sang-Gug Lee. A D -Band High-Gain and Low-Power LNA in 65-nm CMOS by Adopting Simultaneous Noise- and Input-Matched Gmax -Core. *IEEE Transactions on Microwave Theory and Techniques*, 69(5):2519–2530, 2021.

[YSE15] Roee Ben Yishay, Evgeny Shumaker, and Danny Elad. A 122-150 GHz LNA with 30 dB gain and 6.2 dB noise figure in SiGe BiCMOS technology. In *2015 IEEE 15th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pages 15–17. IEEE, 2015.

[ZBD+21] Alireza Zandieh, Shai Bonen, M. Sadegh Dadash, Ming Jia Gong, Juergen Hasch, and Sorin P. Voinigescu. 155 GHz FMCW and Stepped-Frequency Carrier OFDM Radar Sensor Transceiver IC Featuring a PLL With <30 ns Settling Time and 40 fs rms Jitter. *IEEE Transactions on Microwave Theory and Techniques*, 69(11):4908–4924, 2021.

[ZCY+20] Peigen Zhou, Jixin Chen, Pinpin Yan, Jiayang Yu, Huanbo Li, Debin Hou, Hao Gao, and Wei Hong. A 150-GHz Transmitter With 12-dBm Peak Output Power Using 130-nm SiGe:C BiCMOS Process. *IEEE Transactions on Microwave Theory and Techniques*, 68(7):3056–3067, 2020.

[ZLJ+20] Yaxin Zhang, Wenfeng Liang, Xiaodi Jin, Mario Krattenmacher, Sophia Falk, Paulius Sakalas, Bernd Heinemann, and Michael Schröter. 3.2-mW Ultra-Low-Power 173–207-GHz Amplifier With 130-nm SiGe HBTs Operating in Saturation. *IEEE Journal of Solid-State Circuits*, 55(6):1471–1481, 2020.

Own Publications

Journal Papers

[1] **İ. K. Aksoyak**, H. Poensgen, and A. Ç. Ulusoy, "A D-Band Power Amplifier with a Coupled Line-Based Four-Way Power Combiner in SiGe Technology," *IEEE Transactions on Microwave Theory and Techniques*, (to be submitted).

[2] **İ. K. Aksoyak**, M. Möck, and A. Ç. Ulusoy, "A Highly Linear D-Band I/Q Receiver With Active Mixer-First Architecture in SiGe Technology," *IEEE Transactions on Microwave Theory and Techniques*, pp. 1–9, 2023.

[3] **İ. K. Aksoyak**, M. Möck, M. Kaynak, and A. Ç. Ulusoy, "A D-Band Power Amplifier With Four-Way Combining in 0.13−μm SiGe," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 11, pp. 1343–1346, 2022.

[4] **İ. K. Aksoyak**, M. Möck, and A. Ç. Ulusoy, "A Differential D-Band Low-Noise Amplifier in 0.13 − μm SiGe," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 8, pp. 979–982, 2022.

[5] E. Turkmen, **İ. K. Aksoyak**, P. Djondovic, S. B. Yilmaz, W. Debski, W. Winkler, and A. Ç. Ulusoy, "A 223–276-GHz Cascadable FMCW Transceiver in 130-nm SiGe BiCMOS for Scalable MIMO Radar Arrays," *IEEE Transactions on Microwave Theory and Techniques*, pp. 1–20, 2023.

[6] M. Möck, **İ. K. Aksoyak**, and A. Ç. Ulusoy, "A K_a-Band Colpitts–Clapp VCO With 30% Tuning Range and High Output Power," *IEEE Microw. Wireless Tech. Lett.*, vol. 33, no. 4, pp. 439–442, 2023.

[7] E. Turkmen, **İ. K. Aksoyak**, W. Winkler, and A. Ç. Ulusoy, "A 220–261 GHz Frequency Multiplier Chain (×18) With 8-dBm Peak Output Power in 130-nm SiGe," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 7, 2022.

[8] E. Turkmen, **İ. K. Aksoyak**, W. Debski, W. Winkler, and A. Ç. Ulusoy, "A 225–265 GHz I-Q Receiver in 130-nm SiGe BiCMOS for FMCW Radar

Applications," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 7, 2022.

Conference Papers

[9] **İ. K. Aksoyak**, M. Möck, and A. Ç. Ulusoy, "A SiGe-Based Quadrature D-Band Up-Converter with High Output Power," in *2024 IEEE 24th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*. IEEE, 2024, pp. 33–36.

[10] **İ. K. Aksoyak**, M. Möck, M. Kaynak, and A. Ç. Ulusoy, "A D-Band Power Amplifier with 15 dBm P_{sat} in 0.13 − μm SiGe BiCMOS Technology," in *2022 IEEE 22nd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*. IEEE, 2022, pp. 5–8.

[11] **İ. K. Aksoyak**, A. Chletsou, J. Papapolymerou, and A. Ç. Ulusoy, "A High Sensitivity RF Energy Harvester for Diverse Environments," in *2020 50th European Microwave Conference (EuMC)*. IEEE, 2021, pp. 444–447.

[12] **İ. K. Aksoyak**, K. Balaban, H. Torun, and G. Dundar, "Compact model based design space exploration for CMOS hall effect sensors," in *2017 14th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*. IEEE, 2017, pp. 1–4.

[13] M. Möck, **İ. K. Aksoyak**, and A. Ç. Ulusoy, "A 4.5 dBm SiGe Doubler-Amplifier Chain Covering the Entire D-Band," in *2024 IEEE 24th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*. IEEE, 2024, pp. 29–32.

[14] M. Möck, **İ. K. Aksoyak**, and A. Ç. Ulusoy, "A High-Efficiency D-Band Frequency Doubler in 22-nm FDSOI CMOS," in *2022 17th European Microwave Integrated Circuits Conference (EuMIC)*. IEEE, 2022, pp. 272–275.

[15] A. Chletsou, **İ. K. Aksoyak**, J. Papapolymerou, and A. Ç. Ulusoy, "UHF Rectenna for Implanted and Free Space Communications," in *2019 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*. IEEE, 2019, pp. 641–642.