Improved Test Circuit for Characterization of the Dynamic On-Resistance of GaN-HEMTs over a Wide Operating Range

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***Abstract*—GaN-HEMTs show excellent switching and conduction characteristics and are an excellent candidate to replace Si-based power semiconductors with voltage ratings of up to $650\,\mathrm{V}$. However, trapping phenomena, such as the dynamic on-resistance $dR_{\mathrm{ds,on}}$, have not yet been fully eliminated. As these can significantly influence the conduction losses and reliability of GaN-HEMTs, suitable characterization methods are required. This paper presents an improved test circuit to characterize the dynamic on-resistance $dR_{\mathrm{ds,on}}$ over a wide operating range. This includes positive and negative drain currents I_{d}, adjustable gate-voltages V_{gs} and temperatures T_{c}. In order to stimulate trapping phenomena, the bias voltage on the device under test (DUT) in the off-state V_{ds} is adjustable in magnitude and duration (soak time). In addition, the drain current I_{d} of the DUT only flows for the duration of the measuring interval, which leads to less self-heating. For an improved measurement of the drain-source voltage V_{ds} in the on-state, an improved clamp-circuit was developed. With small modifications to the test circuit, switching characteristics can also be measured.**

***Index Terms*—Dynamic on-state resistance, gallium nitride high-electron-mobility transistors (GaN-HEMT), half-bridge, hard-switching (HS), power semiconductor device characterization, switching-losses, conduction-losses, clamp-circuit, double pulse test (DPT)**

I. Introduction

Power transistors based on the wide-bandgap semiconductor gallium-nitride (GaN) feature very low switching and conduction losses. This is mainly due to the high critical field strength of GaN, which allows a smaller distance between the drain and the source terminals. As a result, the on-resistance $R_{\mathrm{ds,on}}$ decreases significantly, which leads to lower conduction losses. Further, parasitic capacitances are reduced, which leads to faster switching and therefore lower switching losses. Besides, the currently commercially available GaN-transistors are high-electron mobility transistors (HEMTs). In such devices, a two-dimensional electron gas (2DEG) in intrinsic GaN is the current contributor, which features a superior electron mobility compared to a MOSFET. This further decreases the $R_{\mathrm{ds,on}}$ [1]. Apart from these excellent properties, trapping effects limit the device's performance. Traps are defects in the semiconductor structure that can be ionized by gate or drain bias [1], [2]. The longer the voltage bias is applied, the more traps are ionized, until a saturation occurs. Since traps have a charge, they can deplete the 2DEG. As a result, there is a mostly temporary change of output and transfer characteristics, which in turn leads to the so called dynamic on-resistance $dR_{\mathrm{ds,on}}$.

For an accurate calculation of conduction losses or to make predictions regarding reliability, the $dR_{\mathrm{ds,on}}$ must be taken into account [3]. Consequently, there is a need to characterize the $dR_{\mathrm{ds,on}}$, which generated lots of academic attention in recent years [3]–[10]. Most of the proposed test setups for characterizing the $dR_{\mathrm{ds,on}}$ are based on a modified double pulse test (DPT) setup. The most important necessary modification of the DPT is the clamp-circuit, which allows to measure the $R_{\mathrm{ds,on}}$ immediately after turn-on with high accuracy [5], [7], [8], [10], [11].
However, to better control the initial condition of the $dR_{\mathrm{ds,on}}$, further modifications of the DPT are necessary. In [3] the DPT was extended by two additional transistors to adjust the soak time. The soak time is the period of time during which a certain voltage bias V_{ds} is applied to the device under test (DUT) in its off-state. Thereby, further investigations on the $dR_{\mathrm{ds,on}}$ are possible, because the soak time strongly influences the ionization of the traps.

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In order to investigate soft-switching, the DPT was modified by two additional capacitors in [6]. It was shown that the $dR_{\mathrm{ds,on}}$ behaves differently under soft-switching conditions. Another test setup, which in addition to soft switching also allows the investigation of reverse conductivity of a cascode GaN-HEMT, is presented in [9].
Apart from the DPT approach, a modified pulsed I-V-setup with adjustable soak time was presented in [4]. The DUT was switched under zero current conditions. One advantage of the test circuit is that the drain current I_{d} can be kept constant, which leads to a more accurate measurement of the slightly current dependent $R_{\mathrm{ds,on}}$. It should be noted that in conventional DPTs the drain current I_{d} of DUT increases after turn-on with a slope dependent on the inductance L_{DPT} and the full blocking voltage V_{DC}. Depending on the size of L_{DPT} and the magnitude of V_{DC}, this may introduce error in the $R_{\mathrm{ds,on}}$-measurement.

This paper presents an improved DPT setup that extends the operating range of a conventional DPT setup under hard-switching conditions (Fig. 1). One of the fundamental improvements is that the characterization of the $dR_{\mathrm{ds,on}}$ can also be carried out in the third quadrant. Compared to the test setup presented in [9], which also allows third quadrant characterization, only one inductor is needed. In addition, self-heating is reduced to a minimum, as the DUT only conducts during the measurement phase, when the inductance is already charged. This property is only given by the pulsed I-V setup from [4], which in turn does not allow third-quadrant characterization. Further, the DUT is not switched under hard-switching conditions in [4]. Compared to a conventional DPT circuit, only the forward voltage of two conductive GaN transistors is applied to the inductor in the measurement state instead of V_{DC}. As a result, the current slope is reduced significantly and is independent of V_{DC}. This allows the $dR_{\mathrm{ds,on}}$ to be measured over a longer period of time at an almost constant operating point. In addition, the soak time is also adjustable by selecting the freewheeling state of the circuit.

The $R_{\mathrm{ds,on}}$ can be measured at different positive and negative gate voltages V_{gs}. This allows the investigation of the reverse conductivity at different negative gate voltages V_{gs}. Due to the high temperature coefficient of GaN-HEMTs, the test setup is equipped with a temperature control circuit to ensure that the measurement is always carried out at a defined case temperature T_{c}. For further improvement of the measurement accuracy of V_{ds} in the on-state, an improved clamp-circuit was developed. With small modifications to the setup, it is possible to measure the switching losses.

The paper is structured as follows: First, the operating principle of the circuit is explained for the relevant operating points. This is followed by sections explaining the improved clamp-circuit and the temperature control circuit. Subsequently, the practical implementation of the setup is discussed. Finally, the advantages of the test setup are demonstrated by means of measurements.

II. Operating Principle of the Proposed Test Circuit

A. Overview

The proposed DPT-circuit is illustrated in Fig. 1. It basically consists of a full-bridge with an additional device (LS1) connected in parallel to the DUT. As with conventional DPTs, an inductive load L_{DPT} is used. It is connected to the two switching nodes of the full-bridge. It is assumed that the parallel-connected device LS1 does not affect the $R_{\mathrm{ds,on}}$-measurement of the DUT, if it can be assured that it never conducts during the measurement phase.
However, if the switching losses are to be measured, the dynamic characteristics of the DUT are affected by LS1 due to its output capacitance C_{oss}. In this case, LS1 must be removed.

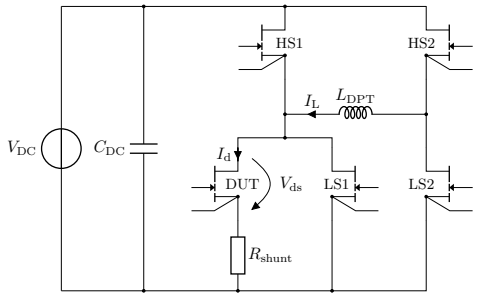


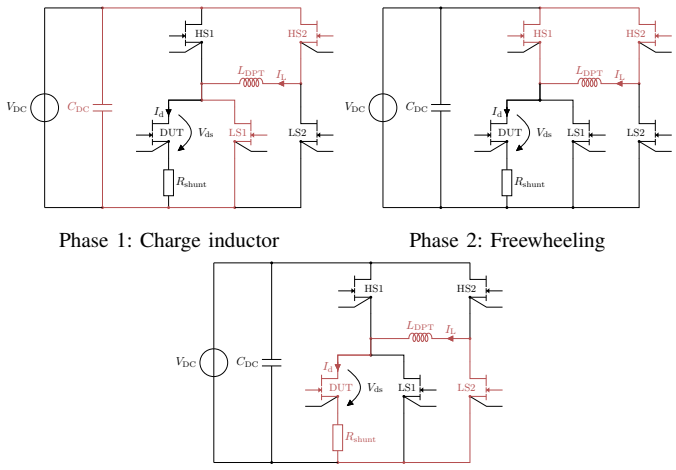
Fig. 1: Proposed test circuit

B. Positive Test Current

The procedure to apply a positive drain current I_{d} is divided into three phases as illustrated in Fig. 2. First, the inductor needs to be charged by turning on the transistors HS2 and LS1. As in a conventional DPT, the duration of this phase t_{charge} is the control variable to adjust the current I_{d}. In the simplest case, this can be calculated using the inductance L_{DPT} and the DC-link voltage V_{DC}:

$$t_{\mathrm{charge}} = \frac{L_{\mathrm{DPT}}}{V_{\mathrm{DC}}} \cdot I_{\mathrm{d}}. \tag{1}$$

Besides the DC-link voltage V_{DC}, the inductor L_{DPT} and the charging duration t_{charge}, I_{d} also depends on the DC-link capacitor, the duration of the succeeding phases and the resistive elements in the circuit. However, this requires a more sophisticated model of the circuit and is beyond the scope of this paper.
In the second phase, LS1 is turned off and HS1 is turned on, which is the upper freewheeling state. This phase is optional, if the DUT needs to be switched under voltage.
Next, the measurement phase is initiated. Thereby, a transition is made to the lower freewheeling state by turning HS1 and HS2 off and turning the DUT and LS2 on. In this phase, the voltage across the inductor is only the on-state voltage of the two conducting transistors. This significantly reduces the



Phase 1: Charge inductor Phase 2: Freewheeling

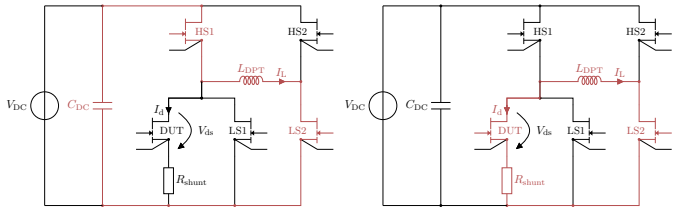
Phase 3: Measurement

Fig. 2: Measurement procedure for $I_{\mathrm{d}} > 0$

current slope compared to a conventional DPT and makes it independent of V_{DC}. By choosing the inductor L_{DPT} properly, an almost constant current I_{d} in the measurement phase can be achieved. As the on-resistance $R_{\mathrm{ds,on}}$ is slightly current-dependent, this leads to a more accurate measurement. Once the measurement has been completed, a switch is made to the idle state, which is explained further in section II-D.

C. Negative Test Current

The procedure for applying a negative current to the DUT is shown in Fig. 3 and is divided into two phases. As with the procedure for positive currents, L_{DPT} must first be charged for the time period t_{charge}, to achieve the desired drain current I_{d}. This is done by turning HS1 and LS2 on. Subsequently, the measurement state is entered by turning HS1 off and turning the DUT on. As the gate voltage of the DUT V_{gs} is adjustable, it is possible to investigate the self-commutated reverse conduction (SCRC) characteristics at different negative gate voltages. However, it must be ensured that the parallel-connected transistor LS1 does not become conductive in this case. This is ensured by keeping the gate voltage of LS1 $V_{\mathrm{gs,LS1}}$ always lower than the gate voltage of the DUT $V_{\mathrm{gs,DUT}}$.

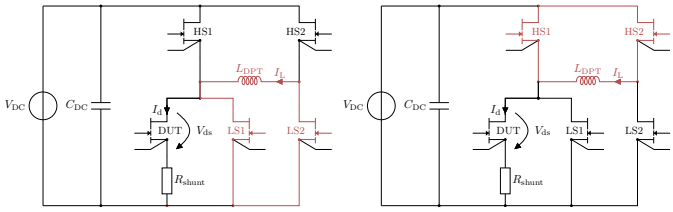


Phase 1: Charge inductor Phase 2: Measurement

Fig. 3: Measurement procedure for $I_{\mathrm{d}} < 0$

D. Idle State

In order to stimulate the trapping effects, it is important to select a suitable idle state. As the excitation of these effects significantly depends on the magnitude and duration (soak time) of the applied blocking voltage [3], [4], the two freewheeling states of the circuit are suitable for this purpose (see Fig. 4). By selecting the upper freewheeling state, the DC-link voltage V_{DC} is applied to the DUT, which leads to an ionization of the traps. If the lower freewheeling state is chosen, the DUT is short-circuited, resulting in a drain-source voltage V_{ds} of 0 V, as soon as the inductor is discharged. In this case, the charge carriers are released from the traps. This enables comprehensive investigations of the dynamic on-resistance $dR_{\mathrm{ds,on}}$. Another purpose of the idle-state is to discharge the inductor after a measurement. In this case, the DUT always remains in the off-state to prevent further self-heating.



Lower freewheeling state Upper freewheeling state

Fig. 4: Idle states for preconditioning

III. Improved Clamp-Circuit

The majority of GaN-HEMTs currently available on the market allow blocking voltages V_{ds} of up to 650 V. In on-state, however, V_{ds} is only a few hundred millivolts and needs to be measured with high accuracy to determine the $R_{\mathrm{ds,on}}$. To achieve this and to prevent clipping or even damage of the measurement equipment, a clamp-circuit is required [5], [7], [8], [10], [11].

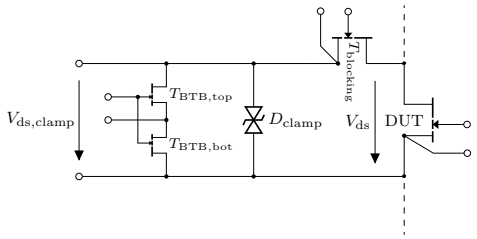


Fig. 5: Improved clamp-circuit

In this paper, an improved clamp-circuit is presented that further improves the measurement accuracy at low V_{ds} by enabling an optimized measurement range. It is shown in Fig. 5 and is based on the one presented in [5], [8]. The major modifications are the two back-to-back (BTB) connected transistors $T_{\mathrm{BTB,top}}$ and $T_{\mathrm{BTB,bot}}$. Instead of two anti-parallel connected diodes, a bidirectional TVS-diode D_{clamp} with a clamp voltage V_{clamp} of ± 8 V and a reverse working

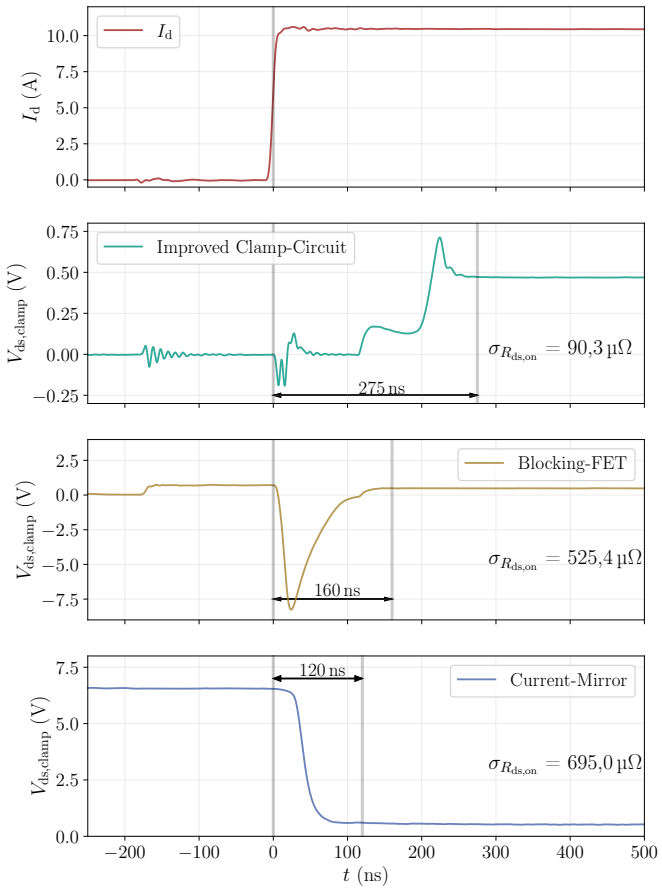


Fig. 6: Comparison of clamp-circuits

maximum voltage V_{RWM} of $\pm 5.5\,\mathrm{V}$ is used. This allows a higher maximum measurement range of about $\pm 5\,\mathrm{V}$.

Without the two BTB-transistors, the measurement range of the oscilloscope is not optimally utilized. It always has to be adjusted to the clamp voltage V_{clamp}, even if V_{ds} is only a few hundred millivolts. This is due to the capacitive currents flowing through the output capacitance C_{oss} of the Blocking-FET T_{blocking} during a switching event and forcing the TVS-diode to become conductive. In this case, the output of the clamp-circuit $V_{\mathrm{ds,clamp}}$ transiently becomes $\pm V_{\mathrm{clamp}}$. The current-mirror-based circuit presented in [10], [11] have a similar problem. With this circuit, $V_{\mathrm{ds,clamp}}$ permanently becomes $\approx V_{\mathrm{RWM}}$ in the off-state of the DUT.

By switching the two BTB-transistors $T_{\mathrm{BTB,top}}$ and $T_{\mathrm{BTB,bot}}$ complementary to T_{blocking}, only the maximum expected V_{ds} is applied to the output. The low $R_{\mathrm{ds,on}}$ of the two BTB-transistors will short the output of the clamp-circuit outside of the measurement interval. This enables the oscilloscope's measuring range to be optimally utilized, which improves accuracy.

Alternatively to the BTB-transistors, it is also possible to use a single FET, such that the circuit depicted in Fig. 5 has a configuration similar to a half-bridge. In this case, however, the measurement range in the third quadrant, resp. for negative I_{d}, will be limited to V_{F} of the body diode of the FET.

Fig. 6 shows a comparison between the improved clamp-circuit shown in Fig. 5, the circuit with Blocking-FET introduced in [5], [8] and the current-mirror-based circuit presented in [10], [11]. The behavior of the clamp-circuit with Blocking-FET can be achieved by simply not switching $T_{\mathrm{BTB,top}}$ and $T_{\mathrm{BTB,bot}}$ when using the improved circuit. Measurements with the current-mirror-based circuit were conducted with an earlier version of the test setup that uses this circuit. All measurements were carried out under the conditions described in VI-A and the DUT current I_{d} was set to about $10\,\mathrm{A}$. It can be clearly seen, that the required measurement range of the improved clamp-circuit is an order of magnitude smaller than in the other circuits. On the one hand the measurement noise, quantified by the standard deviation $\sigma_{R_{\mathrm{ds,on}}}$ of $R_{\mathrm{ds,on}}$, is reduced. On the other hand, the reduced measurement range will also improve gain and offset accuracy of the measurement.

However, the response time of $275\,\mathrm{ns}$ of the improved circuit is significantly higher than the lowest, which is the one of the current-mirror-based circuit with $120\,\mathrm{ns}$. The high response time may result from the fact that Si-MOSFETs have been used up to now. It can be assumed that the response time can be reduced by using GaN-HEMTs. So far, the longer response time of the circuit has not turned out to be an issue, as $dR_{\mathrm{ds,on}}$ does not change significantly in the lower microsecond-range with the selected DUT [12].

IV. Temperature Control Circuit

Power semiconductors based on GaN have a strong positive temperature coefficient. For this reason, it is important, that all measurements are carried out at a defined temperature T_{c}. In the given case, the temperature is controlled using a thermoelectric cooler (TEC). In comparison to a conventional thermostat, TECs are more compact and react more dynamically. A similar dynamic and compactness can be achieved with heat resistors as used in [3]. However, a TEC has the additional advantage to actively cool the

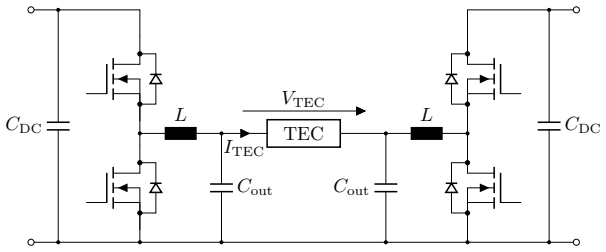


Fig. 7: DC-DC converter for the TEC

DUT, which makes temperatures below room temperature possible. Further, transitions from higher temperatures to lower temperatures are faster. A disadvantage of the TEC is the limited temperature range and cooling power. In order to use the full temperature range, proper thermal isolation of the DUT is necessary. With the current setup using a TEC from *Quick-Cool* with 8.6 W cooling power [13], case temperatures T_c from $-15\,°C$ up to $95\,°C$ are possible.

To operate the TEC both in cooling and in heating mode, the voltage across the TEC V_{TEC} needs to be reversible, which in turn requires a DC-DC converter with reversible output voltage. It is depicted in Fig. 7 and consists of two buck converters, which are connected similar to a full-bridge. A similar circuit was used in [14] for temperature control of a fiber optic laser.

To control the case temperature T_c of the DUT, a digital control algorithm is used. It basically consists of two cascaded PI-controllers. The inner controller controls the current I_{TEC} of the TEC and the outer controller controls the case temperature T_c. As temperature sensor, a thermistor is used, which is thermally well-connected to the DUT in order to measure T_c as accurately as possible.

V. Realization of the Test Setup

The practical realization of the test setup is depicted in Fig. 8 and Fig. 9. The main part of the setup is the mainboard, on which an easily exchangeable test fixture is mounted. It further contains the control circuit for the setup and the isolated power supplies for the gate drivers. On the test fixture, the proposed test circuit is mounted with the DUT, auxiliary devices, gate drivers and a local DC-link capacitance for commutation. Additionally, it contains the clamp-circuit, the temperature sensor for T_c, a shunt resistor and measurement-connectors for V_{ds}, $V_{ds,clamp}$, V_{gs} and I_d.

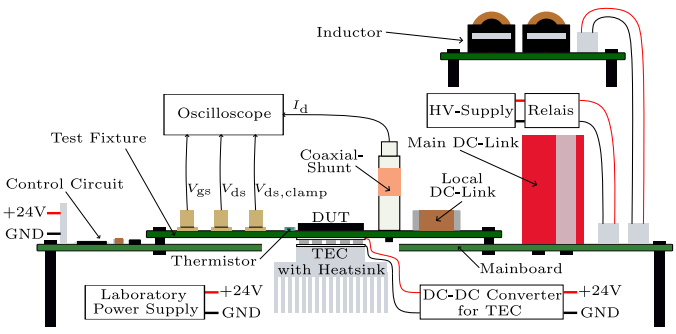


Fig. 8: Illustration of the test setup

A high voltage power supply supplies the DC-link of the test circuit, whose poles are disconnected, when a measurement is conducted. This all-pole separation is achieved by using two relais and reduces capacitive coupling during the measurement. In order to provide sufficient energy for charging the inductor, which is located on a separate printed circuit board, a large DC-link capacitance of $500\,\mu F$ is mounted on the mainboard. The DC-DC converter for temperature control of the DUT consists of two buck converters which are connected in a full-bridge-configuration, whereas each converter output is connected to the TEC. Both the DC-DC converter and the mainboard is supplied by a separate laboratory power supply with an output voltage of 24 V.

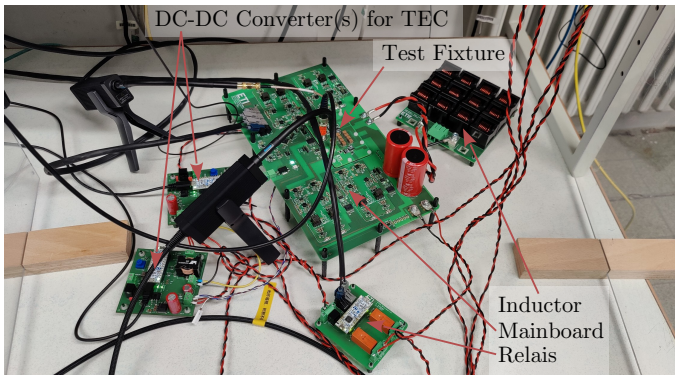


Fig. 9: Picture of the test setup

The test setup can be operated fully automatically. The oscilloscope, the mainboard, the two buck converters and the high-voltage power supply unit are controlled via corresponding communication interfaces, such as Ethernet or UART.

VI. Measurements

A. Measurement Conditions

In order to demonstrate the proposed test setup with its novel test circuit, measurements were carried out using the GS66508B GaN-HEMT from GaN Systems with a Schottky-p-GaN gate [12]. This chip has a current rating of 30 A and a voltage rating of 650 V.

Depending on the sign of the current I_d, the measurement procedure for positive currents (see II-B) or negative currents (see II-C) is chosen. During the measurement procedure, all poles of the high-voltage power supply unit are disconnected from the test setup using two relays. The main DC-link capacitance is $500\,\mu F$ and supplies the required energy during the charging process of the inductor L_{DPT}. The inductor itself has a value of $90\,\mu H$. For all measurements, the measurement intervall $t_{measure}$ is $5\,\mu s$ long. In case of a positive current, the freewheeling state prior to the measurement phase has a duration $t_{freewheel}$ of $1\,\mu s$.

The following procedure is used to calculate the $R_{ds,on}$: First, the on-resistance $R_{ds,on}(t)$ over time is calculated by using the oscilloscope measurements of $V_{ds,clamp}(t)$ and $I_d(t)$ within the measurement interval. The average value of $R_{ds,on}(t)$ over the measurement interval is then considered as the measured on-resistance $R_{ds,on}$.

As the device's behavior is also influenced by the conditions on the gate [2], all measurements are carried out under the

same conditions as far as possible.
For that purpose, the on-state gate-voltage $V_{\mathrm{gs,on}}$ was set to 6 V and the off-state gate-voltage $V_{\mathrm{gs,off}}$ was set to 0 V. In order to minimize feedback effects on the gate during switching, the measurements are conducted at a reduced switching speed with a turn-on gate-resistance $R_{\mathrm{g,on}}$ of 20 Ω and a turn-off gate-resistance $R_{\mathrm{g,off}}$ of 5.6 Ω.

For data acquisition, an oscilloscope of the type *WavePro 404HD* with 4 GHz bandwidth, 12-bit resolution and 0.5 % full-scale gain accuracy from *LeCroy* is used [15]. As the bandwidth requirements for on-resistance measurements are low, it is limited to 20 MHz. Additionally, a noise filter was used. For the measurement of I_{d}, a coaxial shunt with 10 mΩ of the type *SSDN-414-01* from *T&M Research* is used [16], whose voltage drop is measured using an optically isolated probe of the type *SigOFIT MOIP02P* from *Micsig* [17]. The output voltage of the clamp-circuit $V_{\mathrm{ds,clamp}}$ is directly connected to the input of the oscilloscope.

B. On-Resistance

To demonstrate that the test setup is capable of measuring $R_{\mathrm{ds,on}}$ under different operating conditions, measurements were carried out at different currents I_{d} and temperatures T_{c}. For all measurements, the DC-link voltage V_{DC} is chosen to 150 V. Further, the lower freewheeling state was always selected in order to reduce the influence of trapping as much as possible. In the case of negative currents, the inherent soak time of the measurement procedure is the duration t_{charge} of the inductor charging state. In case of the maximum considered current of $I_{\mathrm{d}} = \pm 50$ A, t_{charge} is about 35 µs. For positive currents, the inherent soak time is only 1 µs caused by the freewheeling state prior to the measurement state.

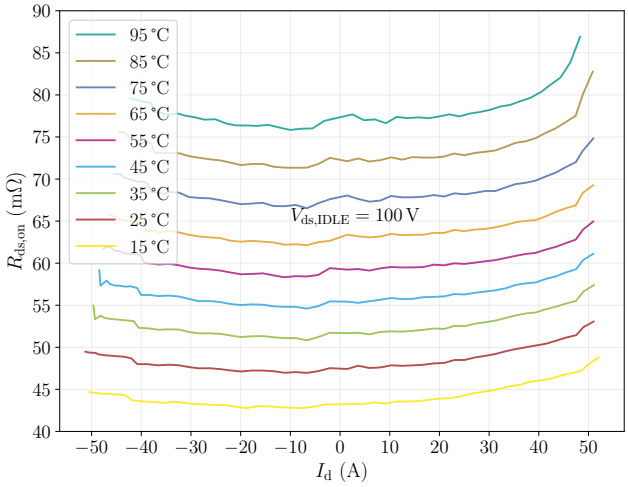


Fig. 10: $R_{\mathrm{ds,on}}$ over I_{d} at different T_{c}

The results are shown in Fig. 10. As expected, there is a significant increase of $R_{\mathrm{ds,on}}$ with increasing T_{c} due to the positive temperature coefficient of GaN-HEMTs. Further, it can be seen that the $R_{\mathrm{ds,on}}$ increases both with negative and positive currents I_{d}. This behavior is partially attributable to the self-heating of the DUT. Although the self-heating can be significantly reduced with the new test circuit, it is not completely negligible (see also VI-D). However, as the I_{d}-dependency depends on the sign of the current, the effect is not solely due to self-heating.

C. Dynamic On-Resistance

In order to show that the test setup is capable of measuring the dynamic on-resistance $dR_{\mathrm{ds,on}}$, measurements at different voltages V_{ds} and temperatures T_{c} were conducted.
Instead of evaluating the $dR_{\mathrm{ds,on}}$ over time immediately after turn-on within a timescale of microseconds, as is the case in [5]–[7], [11], a larger timescale in the range of tens of minutes is considered. Over a period of about 50 min, the $R_{\mathrm{ds,on}}$ was measured every 5 s by using the procedure described in VI-A. This method was chosen because no significant change of $R_{\mathrm{ds,on}}$ could be detected within the measurement interval.

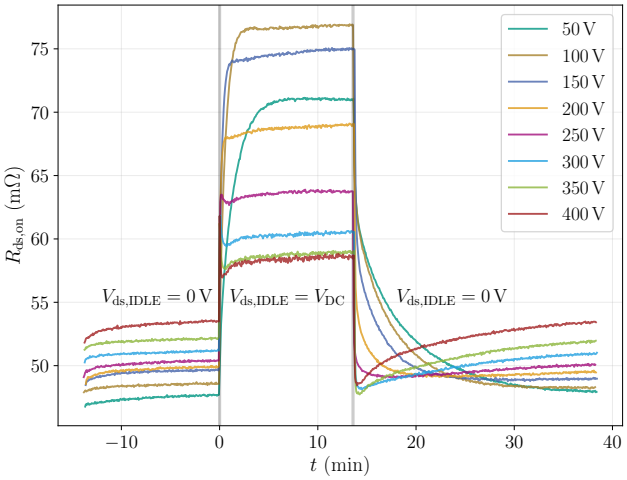


Fig. 11: $dR_{\mathrm{ds,on}}$ at different voltages V_{ds} at $I_{\mathrm{d}} = 30$ A and $T_{\mathrm{c}} = 25$ °C

The results are depicted in Fig. 11 and Fig. 12. At $t = 0$ min, a transition was made from the lower to the upper freewheeling state. It can be clearly seen, that there is a significant increase of $R_{\mathrm{ds,on}}$ over time as soon as the blocking voltage V_{DC} is applied to the DUT. Similarly, it can be seen that the $R_{\mathrm{ds,on}}$ decreases again with time as soon as there is a transistion back to the lower freewheeling state at $t = 13$ min.

Considering both results, it is visible that the time constants of the $dR_{\mathrm{ds,on}}$ decrease both with increasing blocking voltage V_{ds} and temperature T_{c}. With regard to the $dR_{\mathrm{ds,on}}$-swing, there is a decrease with increasing V_{ds} from 100 V and an increase with increasing temperature T_{c}. At V_{ds} of 50 V, the $dR_{\mathrm{ds,on}}$-swing is lower than at 100 V, which indicates an increase of the $dR_{\mathrm{ds,on}}$-swing up to a V_{ds} of about 100 V. A similar V_{ds}-dependent $dR_{\mathrm{ds,on}}$-behavior was also shown in [4].

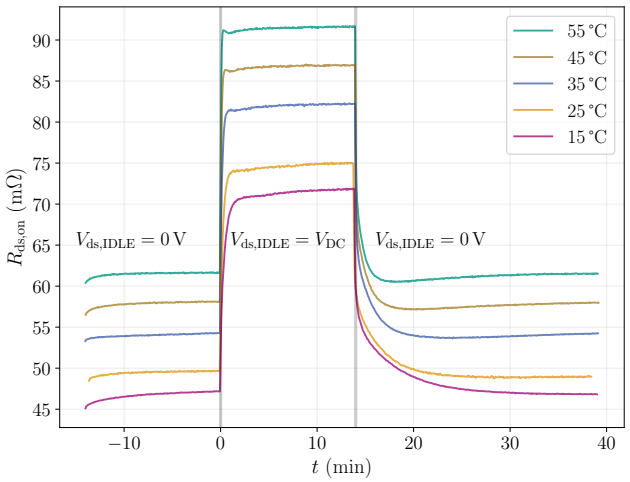


Fig. 12: $dR_{ds,on}$ at different temperatures T_c at $I_d = 30\,A$ and $V_{ds} = 150\,V$

D. Self-Heating Comparison

In order to investigate to which extent the self-heating of the DUT is reduced with the proposed circuit, comparative measurements were conducted. In a first measurement, the DUT was turned on during the charging phase of the inductor, as is the case with a conventional DPT. Thereby, switch LS1 remained in off-state. In another measurement, the procedure for a positive current described in section II-B was applied. Otherwise, the measurements were carried out under the same conditions as far as possible. The DC-link voltage V_{DC} was 150 V in both cases, a T_c of 25 °C was set and the charging time of the inductor t_{charge} was 32.5 µs in each case. To further increase comparability, the upper freewheeling state was also selected as the idle state in the proposed circuit (see section II-D).

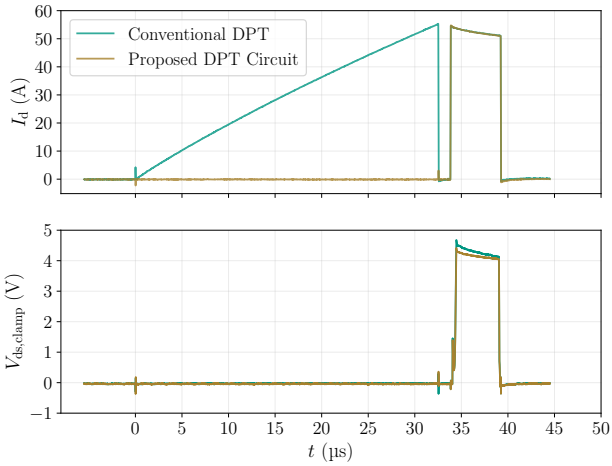


Fig. 13: Self-heating comparison

The results are shown in Fig. 13. First, it can be cleary seen, that no current flows in the DUT during the charging phase of the inductor L_{DPT} when the proposed circuit is used. In both cases, an almost identical drain current I_d was measured in the measurement phase. However, in the case of the conventional DPT, the measured drain-source voltage $V_{ds,clamp}$ in the measurement interval was higher than in the proposed circuit. This results from a slightly increased $R_{ds,on}$. As this has a positive temperature coefficient in GaN HEMTs, it can be assumed that the self-heating at the given operating point is higher in the case of conventional DPTs. Both measurements were carried out a total of 20 times. Statistics on the measurements are shown in TABLE I.

	Conventional DPT	Proposed DPT Circuit
$\mu_{R_{ds,on}}$	82.74 mΩ	79.50 mΩ
$\sigma_{R_{ds,on}}$	0.331 mΩ	0.242 mΩ
min	82.09 mΩ	78.79 mΩ
max	83.24 mΩ	79.87 mΩ

TABLE I: Self-heating measurement statistics

To further provide an estimate of how the absolute self-heating of the DUT behaves and how the proposed test circuit compares to the conventional DPT, a simulative environment was set up using the thermal model of the DUT from the datasheet [12]. Thereby, a constant $R_{ds,on}$ of 80 mΩ was assumed, to which the corresponding patterns of I_d from Fig. 13 were applied as close as possible. The resulting power loss was fed into the thermal model.

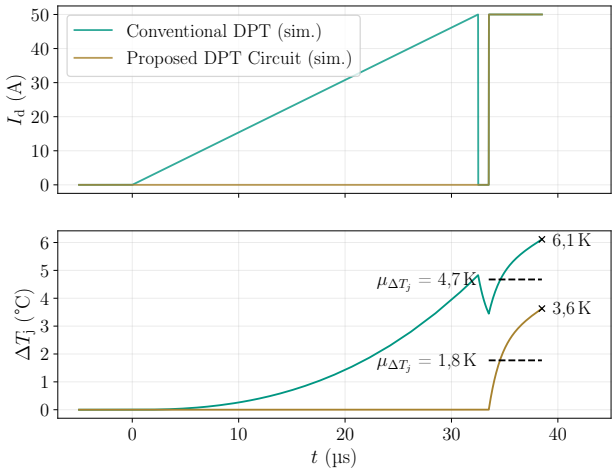


Fig. 14: Simulative comparison of self-heating

From the results, which are shown in Fig. 14, it can be seen that there is a significant reduction of self-heating when using the proposed test circuit. The simulated mean value of temperature rise ΔT_j within the measurement interval $\mu_{\Delta T_j}$ could be reduced by 62 %. However, it should be noted that the achievable reduction in self-heating always depends on the configuration of the setup. A smaller inductance L_{DPT} and a longer freewheeling interval $t_{freewheel}$ reduces the benefit. In addition, absolute self-heating can be further reduced in both types of setups if a shorter measurement interval $t_{measure}$ is chosen.

VII. Conclusion

Within this contribution, an improved DPT-circuit is presented. It enables the characterization of GaN-HEMTs over a wide operating range, which includes different drain-source voltages V_{ds}, different case-temperatures T_{c} and positive and negative drain currents I_{d}. Further, the gate-source voltage V_{gs} is adjustable to investigate SCRC-characteristics at different negative V_{gs}. Moreover, it is possible to characterize the GaN-specific dynamic on-resistance $dR_{\mathrm{ds,on}}$.

Compared to a conventional DPT, the measurement range and accuracy for the dynamic on-resistance $dR_{\mathrm{ds,on}}$ could be improved under some operating conditions. First, self-heating of the DUT is reduced and the soak-time is adjustable. Second, the improved clamp-circuit offers increased accuracy at low drain-source voltages V_{ds} in the on-state, which improves the accuracy of the $dR_{\mathrm{ds,on}}$-measurement. The temperature control for the DUT, which is based on a TEC, allows fast transitions between different temperatures.

In the future, the test setup will provide data from several GaN-HEMTs for compact circuit models. With small modifications to the setup, converter operation will be possible, allowing the compact models to be validated.

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