Design of a GaN-Based DC-DC Converter with HiLEM Topology for Efficient MPP-Tracking

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***Abstract*—The rapid expansion of solar energy generation is increasing the importance of efficiency in large-scale Photovoltaic (PV) systems, especially under non-optimal conditions such as shading, soiling, ageing, defects or asymmetric string configuration. For this reason, multi Maximum Power Point Tracking (multi-MPPT) at string level is becoming more and more important to increase the yield per area. The single Maximum Power Point Tracking (single-MPPT) in a central inverter, which is common in large scale PV systems, has significant disadvantages under difficult operating conditions. Therefore, this paper presents the hardware design of a Gallium Nitride (GaN)-based DC-to-DC converter (DC-DC converter) with the High Efficiency Low Effort MPPT (HiLEM) topology as a Partial Power Converter (PPC) for a string-based multi-MPPT. Measurements of a hardware prototype show the general functionality of the used topology. Finally, the losses of the power semiconductors of an conventional multi-MPPT topology are compared with those of the HiLEM topology.**

***Index Terms*—Photovoltaic, DC-DC converter, Partial Power Converter, MPPT**

I. Introduction

From the beginning, central inverters have been used to cost-effectively feed solar power into the public grid when operating large ground-mounted Photovoltaic (PV) systems. The centralized approach with PV strings connected in parallel and single Maximum Power Point Tracking (single-MPPT) in the central inverter has advantages for large PV systems under certain conditions. The key benefits of using central inverters are the lower investment costs and the efficient power conversion under optimal system conditions [1]. Since existing large ground-mounted PV systems have been optimized for operation with central inverters and single-MPPT, the yield differences between multi Maximum Power Point Tracking (multi-MPPT) and single-MPPT systems under these conditions are marginal [2]. If the boundary conditions are no longer optimal, for example due to heterogeneous shading, soiling, ageing, defects or asymmetric string configuration, then inverters with multi-MPPT can significantly increase the yield of the overall system [1], [3]. In the case of solar energy generation in residential or industrial sector, string inverters with multi-MPPT have been dominating the market for a long time [4]. String inverters are the preferred solution in this application due to the small scale structure and the advantages in difficult system conditions caused by external influences or challenging system conditions.

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The Maximum Power Point Tracking (MPPT) topology described in this paper is primarily intended to be applied to large ground-mounted PV systems. Since the economic reasons for central inverters often dominate in the mentioned large PV systems [5], the presented circuit shows a very efficient method for multi-MPPT, which can improve the economic disadvantages of the string-based MPPT. In addition, the further expansion of large ground-mounted PV systems in the future, will make it necessary to use areas with less than ideal conditions. Existing shading due to neighboring buildings or topographical conditions will have to be accepted. For this reason, an increasing demand for inverters with multi-MPPT for large-scale PV systems is to be expected in the future [5].

In this paper, the hardware design of a DC-to-DC converter (DC-DC converter) for multi-MPPT with the High Efficiency Low Effort MPPT (HiLEM) [6] topology for a prototype system will be presented. Following measurements on the hardware prototype will show the switching characteristics and the principle functionality. A further section deals with the comparison of an efficiency assessment against a conventional multi-MPPT topology. A synchronous boost converter topology is used as DC-DC converter with a conventional multi-MPPT topology. Mainly the losses in the switching semiconductors will be analyzed and compared here. A complete comparison between the two converter topologies will not be discussed in this paper.

Nowadays, Insulated-Gate Bipolar Transistor (IGBT) or Silicon Carbide MOSFET (SiC-MOSFET) semiconductors with blocking voltages from 1200 V are usually used in most central and string inverters with a system voltage of 1000 V respectively 1500 V. Using the HiLEM topology mentioned above as a partial DC-DC converter, it is possible to realize the multi-MPPT with semiconductors having a blocking voltage of less than 1200 V. This makes it possible to use very efficient Gallium Nitride (GaN) semiconductors with a blocking voltage of 650 V or less for multi-MPPT at a system voltage of 1000 V or 1500 V. In addition to the possibility of using semiconductors with a lower blocking voltage, a further

advantage of the design with this topology is the use as a Partial Power Converter (PPC), which reduces the losses of the semiconductors.

This paper is structured as follows: First, the functionality and structure of the HiLEM topology used is described. In Section III the hardware design of the HiLEM circuit is described in detail, based on the system concept presented in [7]. The subsequently presented signal processing system is described in Section IV. The functionality of the prototype is then tested at some significant set points. Finally, a theoretical loss comparison for the semiconductors between HiLEM topology and a conventional multi-MPPT DC-DC converter topology is done to show the benefits of the topology in relation to the switching losses.

II. Overview and Functionality of the HiLEM Topology

The HiLEM circuit was developed to enable a highly efficient multi-MPPT for multiple PV strings. The topology was first introduced in [8] and makes use of the aspect that it is not required for an efficient MPPT to be capable of lowering the input voltage range of the converter down to 0 V. The special circuit arrangement of HiLEM is designed in that way, that it only needs to switch the voltage difference $u_{\mathrm{G,diff}} = u_{\mathrm{G,max}} - u_{\mathrm{G,min}}$ between the Maximum Power Point (MPP) voltage of the lowest string $u_{\mathrm{G,min}}$ and the MPP voltage of the highest string $u_{\mathrm{G,max}}$ [9]. This feature is implemented by splitting the DC link into an upper (W1 to W2) and lower (W2 to W3) part, as shown in Fig. 1. As described in [6], there are a total of three different versions of the HiLEM topology. For the following consideration, only the second topology HiLEM-2 is shown in detail and the layout and design are explained. Each PV string gets its own input

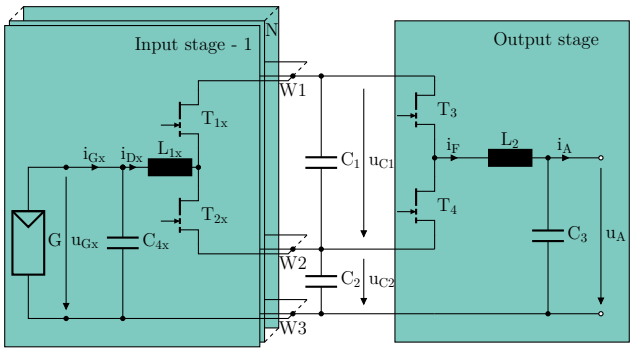

Fig. 1. Circuit design of the HiLEM-2 topology with one to N input stages and a single output stage

stage seen on the left of Fig. 1, consisting of the capacitors C_{4x}, the inductor L_{1x} and the semiconductors T_{1x} and T_{2x} with $x \in \{1 \dots N\}$. The single output stage on the right side of Fig. 1 consists of the semiconductors T_3 and T_4, the inductor L_2 and the capacitor C_3. The input stages are connected by W1, W2 and W3 with the output stage by the split DC link with the capacitors C_1 and C_2.

The MPP voltages of the input stages $u_{\mathrm{G}x}$ can be varied in the range between $u_{\mathrm{C2}} \leq u_{\mathrm{Gx}} \leq u_{\mathrm{C2}} + u_{\mathrm{C1}}$. The components used and the blocking voltages of the semiconductors determine the limits for the voltage u_{C1} in the upper DC link. For efficient operation, the voltage u_{C1} is selected to be as low as possible and u_{C2} as high as possible, which minimizes the switching losses in the semiconductors. The mean value of the DC output voltage u_{A} is always between the MPP voltages $u_{\mathrm{G,min}}$ and $u_{\mathrm{G,max}}$, if the losses were neglected. To illustrate the characteristics, the voltage levels for switching semiconductors are shown in Fig. 2.

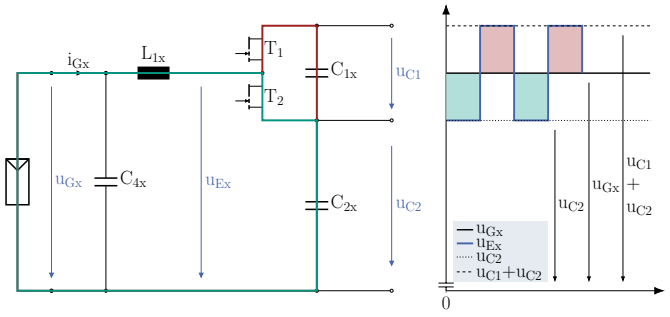

Fig. 2. Setting the input voltage with the different voltage levels of the HiLEM topology

III. Design of the GaN Based HiLEM Circuit

The HiLEM circuit described below will implement string-based MPPT in a PV research plant. Therefore, the boundary conditions for the design of the HiLEM input and output stages are derived from the conditions of the PV research plant. As presented in [7], the total output of the PV research plant is nearly 62 $\mathrm{kW_p}$, with half of this being realized with the MPPT through the HiLEM circuit. Half of the system, meaning 31 $\mathrm{kW_p}$, is divided into four PV strings with 7.7 $\mathrm{kW_p}$ each. This means that four HiLEM input stages are required for the individual MPP control of each PV string. These four input stages are combined to a common HiLEM output stage. A maximum system voltage of 1000 V was specified due to the PV research plant. However, due to the design of the HiLEM circuit with a separate DC link, it is very easy to raise the system voltage up to 1500 V. Thereby only the voltage level of the lower DC-link would be increased, which in turn would not require semiconductors with a higher blocking voltage. The input stage have an output power of approximately 10 kW, the output stage has a power of about 35 kW. The power is not directly converted by the semiconductors, because of the split DC link, the semiconductors only switch part of the total voltage.

In Fig. 2 it is easy to see that the voltage of the upper DC link is only a fraction of the system voltage. For reasonable control, the voltage u_{C1} only needs to be slightly higher than the differential voltage $u_{\mathrm{G,diff}} = u_{\mathrm{G,max}} - u_{\mathrm{G,min}}$. As only a small voltage difference is to be expected between the string with the highest voltage and the string with the lowest voltage, even if several modules are heavily shaded,

the maximum voltage of u_{C1} was fixed at 400 V. This makes it possible to use very efficient GaN semiconductors with 650 V blocking voltage to enable all the advantages of a high switching frequency of over 100 kHz. A modified design using semiconductors with lower blocking voltages of 200 V, for example, would be possible in order to generate even lower switching losses. In order to have the greatest possible degree of freedom for the voltage in the upper DC link for operation in the PV research pant, the semiconductors with 650 V blocking voltage were selected.

As described in [6], the input voltages u_{Gx}, the DC link voltages u_{C1} and u_{C2} and the output voltage u_A must be measured to control the HiLEM circuit. In addition, a current measurement of the PV input current in each input stage i_{Gx} and a measurement of the output current i_A is required.

The following sections will deal with the design of the input stages and the output stage.

A. Design of the HiLEM input stage

The most important components of the HiLEM circuit have already been mentioned in Section II. At this point, the design of the inductor L_{1x} for the input stage, the semiconductors T_{1x} and T_{2x} and the DC link capacitance C_1 and C_2 will be determined.

When selecting the semiconductors for T_{1x} and T_{2x}, one of the main criteria was to achieve a high switching frequency such that the passive components could be kept as small as possible. As mentioned in Section III, a switching frequency of at least 100 kHz should be possible. Furthermore, the current to be switched from one string will not exceed 15 A and the maximum switching voltage is kept less than 400 V. The GaN High-Electron-Mobility Transistor (HEMT) (GS66508T) [10] from *GaN Systems* was selected with these constraints in mind. A maximum drain-source current of 30 A and a blocking voltage of 650 V makes this semiconductor suitable for this application.

The first step in designing the input-side inductor L_{1x} is to determine the input-side current ripple Δi_{Dx}. For this purpose, the voltages of the divided DC link are selected in such a way that $u_{C2} = u^*_{G,min}$, which is the minimum input voltage of all input stages, and $u_{C1} + u_{C2} = u^*_{G,max}$, which is the maximum voltage of all input stages. The current ripple Δi_{Dx} of the inductors L_{1x} then results in [6]:

$$\Delta i_{Dx} = \frac{u^*_{G,max}}{L_{1x} \cdot f_{SW}} \cdot \left(-\frac{u^2_{Gx,n}}{u_{G,diff,n}} + \frac{2 \cdot u_{Gx,n}}{u_{G,diff,n} - 1} - \frac{1}{u_{G,diff,n}} + 1\right) \tag{1}$$

In this case, f_{SW} stands for the switching frequency and the voltages $u_{Gx,n}$ and $u_{G,diff,n}$ were normalized with:

$$u_{Gx,n} = \frac{u_{Gx}}{u^*_{G,max}} \tag{2}$$

$$u_{G,diff,n} = \frac{u_{G,diff}}{u^*_{G,max}}. \tag{3}$$

The maximum current ripple $\Delta i_{Dx,max}$ results from Eq. 1 in the possible range of $u_{Gx,n}$ [6] to:

$$\Delta i_{Dx,max} = \frac{u^*_{G,max}}{L_{1x} \cdot f_{SW}} \cdot \frac{u_{G,diff,n}}{4} \tag{4}$$

The maximum current through the inductor L_{1x} is defined as:

$$i_{Dx,max} = i_{Gx,max} + \frac{1}{2} \cdot \Delta i_{Dx,max} \tag{5}$$

$$\Delta i_{Dx,max} = \delta_i \cdot i_{Gx,max} \tag{6}$$

The inductance of the input-side inductor L_{1x} is given by:

$$L_{1x} = \frac{u^*_{G,max}}{\delta_i \cdot f_{SW} \cdot i_{Gx,max}} \cdot \frac{u_{G,diff,n}}{4} \tag{7}$$

From the previously defined values for the switching frequency $f_{SW} = 100$ kHz, the maximum current $i_{G,max} = 15$ A, the differential voltage $u_{G,diff} = 400$ V and with a related current ripple $\delta_i = 25\,\%$, Eq. 7 results in an inductance of $L_{1x} = 266.67$ µH. In order to be able to place this inductance on the Printed Circuit Board (PCB) in a space-saving manner, four inductors with 65 µH [11] each were connected in series to form a total inductance of 260 µH.

In addition to the layout of the inductors, the dimensioning of the capacitors in the divided DC link is of great interest. Since the entire circuit is modular with several input stages and one output stage, it is advisable to distribute the capacitance of C_1 and C_2 between the individual stages. For the total capacity of C_1 375 µF were determined and for the total capacitance of C_2 33 µF were selected, the detailed dimensioning of the total capacities can be found in [8]. The distribution of the capacity is composed as follows, the capacity C_1 in every input stage was selected as 75 µF and the capacity C_2 as 3.3 µF.

In addition to the passive components, a so called Local Control Unit (LCU) is used to control the semiconductors, the input voltage regulation with MPPT and for communication with the higher-level system control using fiber optic cables. The LCU consists of its own PCB and is plugged onto the HiLEM PCB. An Intel® MAX®10 Field Programmable Gate Array (FPGA) with 16000 logic units [12] is used, which also takes over the evaluation of the current measurement of i_{Gx} and the analysis of the voltage measurement of u_{Gx}, u_{C1} and u_{C2}.

An image of the input stage PCB for the designed HiLEM circuit is shown in Fig. 3

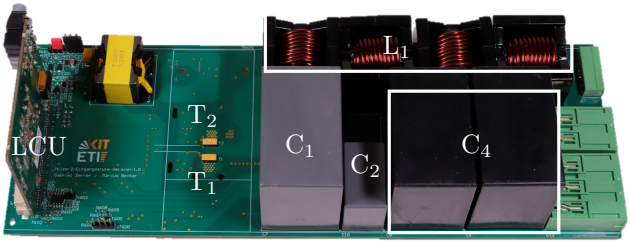

Fig. 3. Image of the HiLEM input stage PCB without the heat sink

B. Design of the HiLEM output stage

The purpose of the HiLEM output stage is to merge the currents delivered by the four input stages and provide the sum of all these currents to the output. As all input stages and the output stage have the same DC link, the blocking voltage requirements of the power semiconductors are identical. The switching frequency of $f_{\mathrm{SW}} = 100\,\mathrm{kHz}$ is also identical to the input stage. As the output stage needs to convert the sum of all currents of the input stage, the current rating of the switches need to be higher. Therefore, the GaN HEMT (GS66516T) from *GaN Systems* [13] were chosen for the transistors T_3 and T_4. They enable a maximum drain-source current of 60 A and are suitable for the HiLEM output stage.

Equivalent to the input stage, it is necessary to determine the output inductor L_2. For this purpose the method using the maximum current ripple is also chosen. Initially, the output-side current ripple $\Delta \mathrm{i}_{\mathrm{F}}$ is determined with the normalized output voltage $u_{\mathrm{A,n}} = \frac{u_{\mathrm{A}}}{u^*_{\mathrm{G,max}}}$ [8] as:

$$\Delta \mathrm{i}_{\mathrm{F}} = \frac{u^*_{\mathrm{G,max}}}{\mathrm{L}_2 \cdot f_{\mathrm{SW}}} \cdot \left(-\frac{u^2_{\mathrm{A,n}}}{u_{\mathrm{G,diff,n}}} + \frac{2 \cdot u_{\mathrm{A,n}}}{u_{\mathrm{G,diff,n}} - 1} - \frac{1}{u_{\mathrm{G,diff,n}}} + 1\right) \tag{8}$$

The maximum current ripple in the range $u_{\mathrm{A,n}}$ and the maximum current through the output-side inductor L_2 therefore result in:

$$\Delta \mathrm{i}_{\mathrm{F,max}} = \frac{u^*_{\mathrm{G,max}}}{\mathrm{L}_2 \cdot f_{\mathrm{SW}}} \cdot \frac{u_{\mathrm{G,diff,n}}}{4} \tag{9}$$

$$i_{\mathrm{F,max}} = \bar{i}_{\mathrm{F,max}} + \frac{1}{2} \cdot \Delta \mathrm{i}_{\mathrm{F,max}} \tag{10}$$

$$\Delta \mathrm{i}_{\mathrm{F,max}} = \delta_i \cdot \bar{i}_{\mathrm{F,max}} \tag{11}$$

Which results in the inductance of the output inductor L_2:

$$\mathrm{L}_2 = \frac{u^*_{\mathrm{G,max}}}{\delta_i \cdot f_{\mathrm{SW}} \cdot \bar{i}_{\mathrm{F,max}}} \cdot \frac{u_{\mathrm{G,diff,n}}}{4} \tag{12}$$

From the previously defined values, a related current ripple δ_i reduced to 20 % and an average maximum output current with four connected input stages in the stationary case of $\bar{i}_{\mathrm{F,max}} = 60\,\mathrm{A}$, the capacitance L_2 was determined to be 83.33 µH. In order to achieve the determined capacitance value for L_2, six inductors with 15 µH [14] each were connected in series to a total inductance of 90 µH.

The total capacitance of the DC link capacitors mentioned in subsection III-A is divided for the output stage. The capacitance C_1 is selected as 75 µF whilst the capacitance in the lower DC link C_2 is selected as 19.8 µF.

Furthermore, a pluggable LCU equivalent to the input stage is used for the interpretation of the measured values i_{F}, u_{A}, u_{C1} and u_{C2}, as well as for the communication and control tasks. Since the control and regulation effort for the HiLEM output stage is higher, a LCU with an Intel® MAX®10 FPGA with 25000 logic units [12] is used.

An image of the output stage PCB for the designed HiLEM circuit is shown in Fig. 4

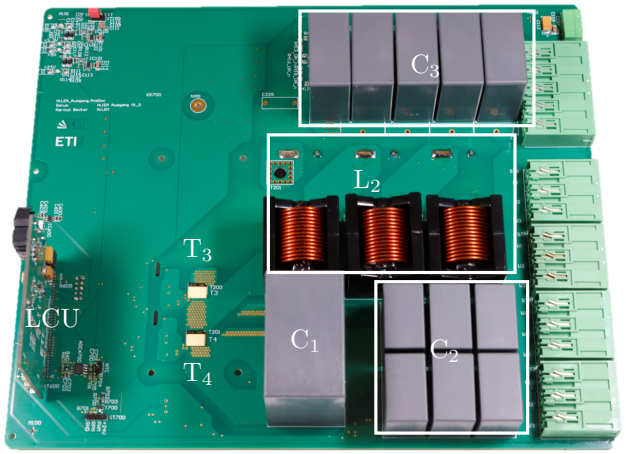

Fig. 4. Image of the HiLEM output stage PCB without the heat sink

IV. Structure of the Entire Signal Processing System

This section deals with the signal processing of the individual HiLEM input and output stages and then describes the higher-level signal processing system as a Central Control Unit (CCU). As described in Section III, each stage has its own LCU. This is intended for controlling the power semiconductors with the corresponding Pulse Width Modulation (PWM) signal on each stage and makes the measurement value acquisition of the respective ΔΣ-Analog-Digital-Converter (ΔΣ-ADC).

Furthermore, each LCU has a fiber optic interface to communicate by Fiber Optic Cable (FOC) with the higher-level signal processing system [15], the CCU.

The control of each input stage is also implemented on the respective $\mathrm{LCU}_{\mathrm{IN}}$ of the input stage. This includes the voltage controller with a subordinate current controller for the input voltage $u_{\mathrm{G}x}$ as well as the MPPT algorithm to specify the optimum voltage setpoint $u_{\mathrm{G}x}$. To be able to use a MPPT algorithm, the measured voltage $u_{\mathrm{G}x}$ and the measured current $\mathrm{i}_{\mathrm{G}x}$ are used. The MPPT method to be used in the future is a Perturb and Observe or Incremental Conductance MPPT algorithm. The two measured voltages u_{C1} and u_{C2} of the divided DC link are also used for the control of the input voltage $u_{\mathrm{G}x}$.

In the output stage, the $\mathrm{LCU}_{\mathrm{OUT}}$ also fulfills the function of measuring the values by a ΔΣ-ADC and controlling the semiconductors. The $\mathrm{LCU}_{\mathrm{OUT}}$ also controls the two voltages u_{C1} and u_{C2}. u_{C2} is controlled by the duty cycle of the two semiconductors T_3 and T_4, u_{C1} by the output voltage u_{A}. For this purpose, the appropriate setpoint for u_{A} is determined by the control of the output stage and is sent to the subsequent converter, in this case the grid sided DC-to-AC converter (DC-AC converter). In addition, the measured values of the individual input stages are transferred to the output stage by the CCU for the overall system control.

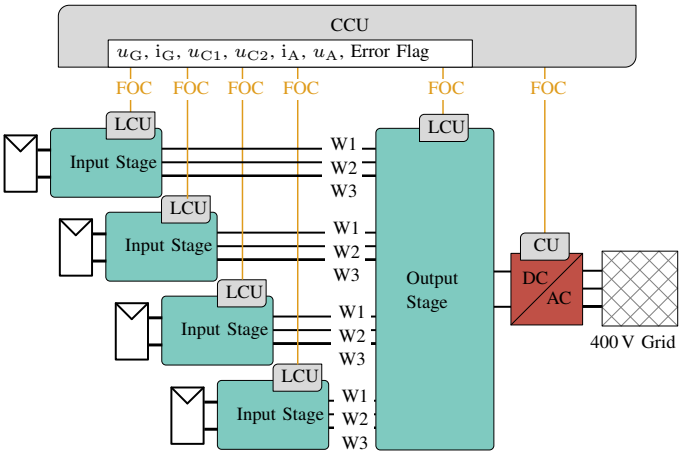

Fig. 5. Structure of the entire HiLEM system with interconnection to the higher-level CCU

The already mentioned in-house developed higher-level signal processing system [15] is used as the CCU for monitoring and controlling the overall system. In addition, it is the communication interface between the individual LCUs' and has further research tasks and is used for recording measurement data. The system structure with the interconnections between the devices is illustrated in Fig. 5. It also shows the main measurements that are sent to the CCU and exchanged with the LCUs'. Furthermore, possible error flags are also exchanged in order to safely control the higher-level system.

The Control Unit (CU) of the DC-AC converter is also connected to the CCU by FOC. It also exchanges measurement values and error flags to safely control the higher-level system. It also transmits the control setpoints to the DC-AC converter to operate it together with the HiLEM circuit.

V. Prototype Measurements

The presented design was verified by initial measurements of the coupled input and output stage of the HiLEM circuit. For this purpose, the switching behavior was first investigated at the fixed switching frequency $f_{SW} = 100\,\text{kHz}$. The switching characteristics for the active switch T_2 of the input stage are shown in Fig. 6 and the switching characteristics for the active switch T_3 of the output stage are shown in Fig. 7. All measurements were performed at a fixed voltage of the lower DC link of $u_{C2} = 100\,\text{V}$. The rise time (10 % to 90 %) of the input stage transistor T_2 with $U_{ds} = 400\,\text{V}$ and an input current $i_G = 3\,\text{A}$ results to 32 ns. The fall time (90 % to 10 %) of T_1 results equivalent to 32 ns. From Fig. 7 a rise time for the output side transistor T_3 results to 22 ns with $U_{ds} = 400\,\text{V}$ and an output current of $i_A = 3\,\text{A}$. The fall time of T_4 results equivalent to 22 ns.

The functional principle of the HiLEM topology is based on the fact that there is a divided DC link between the input and output stage. Fig. 8 shows the most significant voltages when using one input stage with one output stage at different operating points for the input voltage u_G. The measured values of the measurements shown in Fig. 8 are listed in Table I.

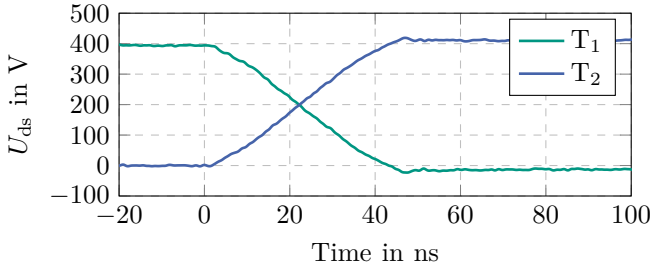

Fig. 6. Switching characteristics of the HiLEM input stage

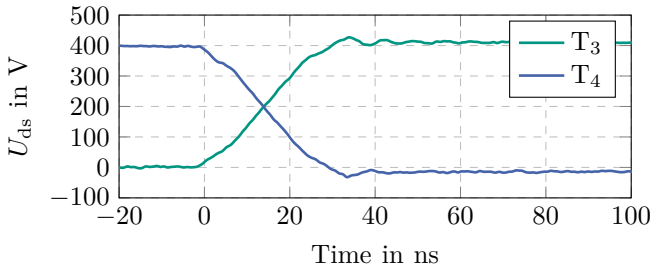

Fig. 7. Switching characteristics of the HiLEM output Stage

It is apparent that the input voltage u_G is always in a range between u_{C2} and $u_{C1} + u_{C2}$. The measurements show that the output voltage u_A is just below the input voltage u_G, this is due to the measured setup with only one HiLEM input stage, whereby u_A is only below u_G due to the occurring losses within the circuit. If more than one input stage is used, an average value of the voltages u_{Gx} weighted by the power is achieved. Boost operation for u_A above the highest input voltage u_{Gx} is not possible with the HiLEM topology. The voltage shown for u_G in measurement 1 of around 850 V also corresponds to the maximum MPP voltage to be expected for reasonable operation at a system voltage of maximum 1000 V.

VI. HiLEM Loss Comparison

In this section, the possible efficiency gain by using the HiLEM topology as a DC-DC converter for multi-MPPT is compared to a standard synchronous boost converter topology for multi-MPPT. In this comparison, the losses of the semiconductors of both topologies are primarily analyzed. Other losses, such as those in the inductors, capacitors or the dead time losses are neglected. In order to make a reasonable comparison, the possible system voltage of both topologies must be comparable. Therefore GaN semiconductors (GPIXV30DFN) from *GaNPower* with 1200 V blocking voltage [16] are used

TABLE I
Measured values of the HiLEM circuit at two different operating points

Measurement	u_G	u_{C1}	u_{C2}	u_A	i_G
1	855 V	160 V	710 V	853 V	3 A
2	551 V	99 V	458 V	548 V	3 A
3	253 V	50 V	210 V	252 V	3 A

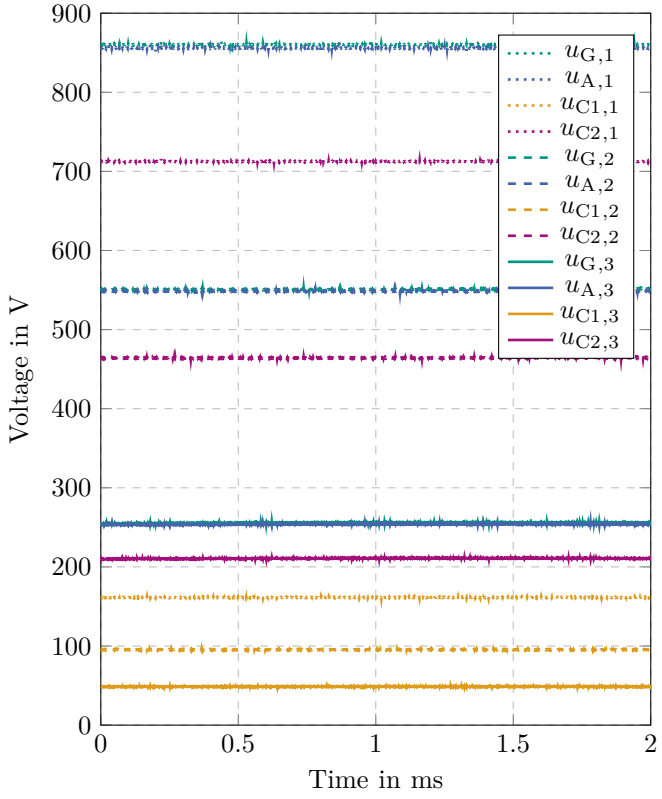

Fig. 8. Operation of the HiLEM input and output stage with different voltage levels

for the analytical loss estimation of the reference synchonous boost converter. First, the total losses of the two topologies are calculated, consisting of the switching losses and the conduction losses. The total losses are then compared for variable voltage differences $u_{\mathrm{G,diff}}$ and input currents $i_{\mathrm{G,eff}}$.

The total losses $P_{\mathrm{loss,total}}$ or $P_{\mathrm{l,t}}$ of both circuits are the sum of all dynamic and conduction losses $P_{\mathrm{l,t}} = P_{\mathrm{loss,dyn}} + P_{\mathrm{loss,con}}$. The dynamic losses consist of the switching losses $P_{\mathrm{loss,sw}}$, the losses for discharging the output capacity C_{oss} $P_{\mathrm{loss,oss}}$ and the losses in the gate $P_{\mathrm{loss,iss}}$

$$P_{\mathrm{loss,sw}} = \frac{1}{2} \cdot (t_{\mathrm{R}} + t_{\mathrm{F}}) \cdot U_{\mathrm{ds}} \cdot I_{\mathrm{d}} \cdot f_{\mathrm{SW}} \tag{13}$$

$$P_{\mathrm{loss,oss}} = \frac{1}{2} \cdot C_{\mathrm{oss}} \cdot U_{\mathrm{ds}}^2 \cdot f_{\mathrm{SW}} \tag{14}$$

$$P_{\mathrm{loss,iss}} = C_{\mathrm{iss}} \cdot U_{\mathrm{gs}}^2 \cdot f_{\mathrm{SW}} \tag{15}$$

where t_{R} and t_{F} are the voltage rise and fall time respectively and U_{gs} is the gate voltage. The conduction losses result from the drain source resistance $R_{\mathrm{ds,on}}$, the Root-Mean-Square (RMS) value of the current I_{d} and the Duty Cycle d. The losses in the high-side $P_{\mathrm{loss,con,High}}$ semiconductor and the low-side $P_{\mathrm{loss,con,Low}}$ semiconductor result in the conduction losses $P_{\mathrm{loss,con}}$:

$$P_{\mathrm{loss,con}} = R_{\mathrm{ds,on}} \cdot I_{\mathrm{d}}^2 \tag{16}$$

For the power losses just described, a test scenario is now defined for a setup with four PV strings. The HiLEM circuit described in Section III is compared with a synchronous boost converter circuit shown in Fig. 9. The total power loss $P_{\mathrm{l,t}}$ at

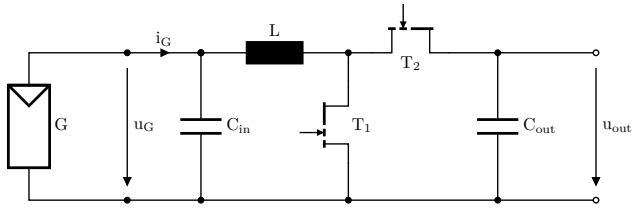

Fig. 9. Circuit of the Boost converter used for comparison

a variable difference of the string voltage $u_{\mathrm{G,diff}}$ is determined for both circuits seen in Fig. 10.

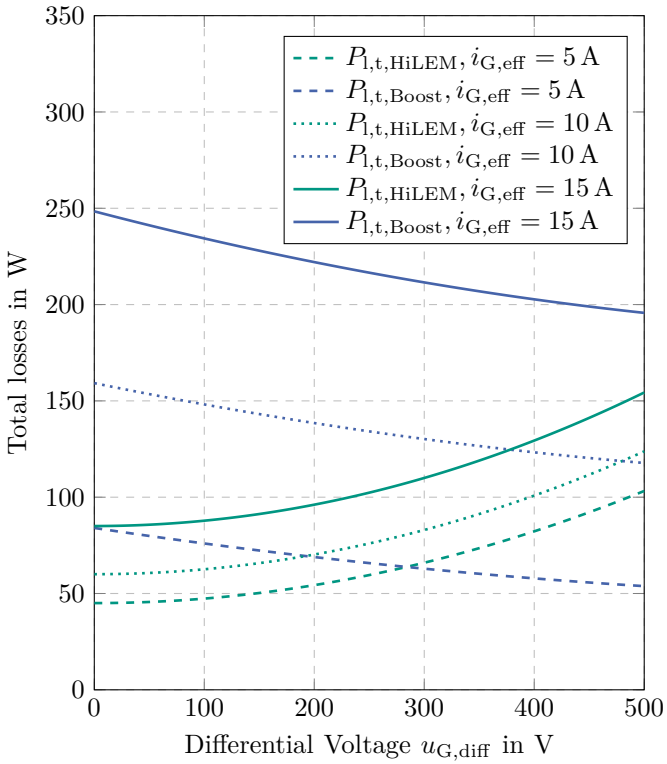

Fig. 10. Total losses $P_{\mathrm{l,t}}$ of the HiLEM and Boost Converter topology for variable $u_{\mathrm{G,diff}}$ and different $i_{\mathrm{G,eff}}$

In order to calculate the illustrated losses, it is assumed that three strings have a fixed input voltage of 850 V and one string has a variable input voltage of 350 V to 850 V. The differential voltage $u_{\mathrm{G,diff}}$ shown in Fig. 10 is the voltage between the fixed 850 V and the variable voltage of one string. For simplicity, the losses were plotted for three different MPP input currents $i_{\mathrm{G,eff}}$ = 5 A, 10 A and 15 A.

In [9], the switching power of the semiconductors of the HiLEM topology is compared in principle with the switching power of a boost converter topology. Based on the assumptions

that are made, the switching power of the HiLEM circuit is lower as long as the differential voltage $u_{\mathrm{G,diff}}$ is less than 50 % of $u_{\mathrm{G,max}}$. Since the approach described here includes the specific switching losses as well as the conduction losses, the fixed limit of 50 % is not applicable for this consideration. The intersection of the loss curves between HiLEM and boost converter in Fig. 10 depends primarily on the number of strings with low input voltage $u_{\mathrm{G}x}$ and the conduction losses. In addition, it is apparent that at a lower current $i_{\mathrm{G,eff}}$, the intersection of the two power losses already occurs at a lower differential voltage $u_{\mathrm{G,diff}}$.

In Fig. 11, the total losses for both topologies were calculated for a fixed differential voltage of one string with $u_{\mathrm{G,diff}} = 100\,\mathrm{V}$ below the variable input voltage $u_{\mathrm{G}x}$ of the other three strings. It can be seen that the absolute value

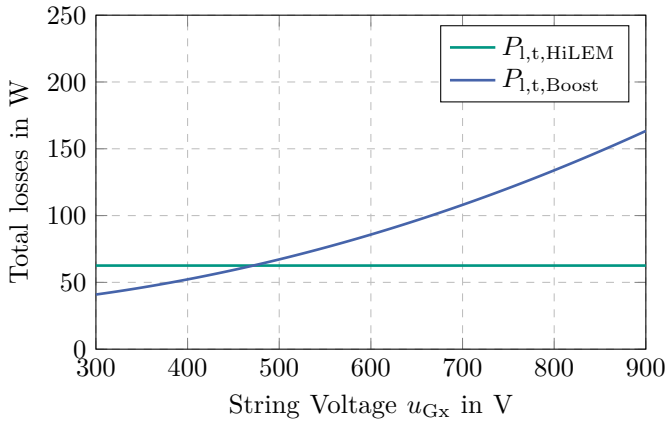

Fig. 11. Total losses of HiLEM and Boost Converter topology for variable $u_{\mathrm{G}x}$

of the string voltages $u_{\mathrm{G}x}$ is not significant for the losses in the HiLEM circuit. This characteristic makes the HiLEM topology suitable for high string voltages with system voltages of up to 1500 V, as the switching losses do not depend on the input voltage $u_{\mathrm{G}x}$ and therefore do not increase with increased string voltages, in contrast to the boost converter topology. If there is no partial shading or other influences on the PV strings, the voltage difference u_{C1} can be selected as small as possible, which means that the switching losses in these states are extremely low. In order to further optimize the switching losses, a predictive control of the upper DC link voltage u_{C1} during operation is reasonable. For this purpose, the control must regulate the voltage u_{C1} in such a way that all strings can be operated in MPP and a global MPP is also possible at times. At the same time, the voltage should be kept as low as possible most of the time in order to reduce overall switching losses.

VII. Conclusion

This contribution describes the key features of the hardware design of a GaN based DC-DC converter with the HiLEM topology for very efficient multi-MPPT. It is used to enable string-based MPPT in large scale PV systems and offers an efficient alternative to conventional topologies for mMPPT because of its property as a PPC. The resulting reduced switching voltage of the HiLEM circuit enables the use of GaN semiconductors with a blocking voltage of 650 V at a system voltage of 1000 V. The separation of switching and system voltage allows a higher system voltage of for example 1500 V to be easily realized with the use of the same semiconductors. The presented design was developed for a prototype with a total power of approximately 35 kW consisting of four input stages for the multi-MPPT of four independent PV strings.

The overall system structure with a central CCU and the LCU of the individual input and output stages enables a maximum possible flexibility in the configuration and operation of the system. Measurements on the real hardware setup were used to validate the functionality of the presented design at selected operating points. Further Measurements in the future will be done with implemented Perturb and Observe or Incremental Conductance MPPT algorithm for the control of the input stage $\mathrm{LCU_{IN}}$. A promising approach for further optimization is the predictive control of the upper DC link voltage u_{C1} during operation, which can actively influence and optimize the switching losses.

A concluding loss analysis against a conventional boost converter topology demonstrates the potential for an efficient multi-MPPT with the HiLEM circuit. Two efficiency characteristics became particularly noticeable. On the one hand, the shown HiLEM circuit is very efficient if the voltage difference $u_{\mathrm{G,diff}}$ between the highest string voltage $u_{\mathrm{G,max}}$ and the lowest string voltage $u_{\mathrm{G,min}}$ is kept low. This is possible because the voltage difference of the string voltages in the MPP between different strings, especially in large PV systems, are very close to each other [1]. On the other hand, it could be demonstrated that the losses of the HiLEM circuit do not depend on the level of the input voltages $u_{\mathrm{G}x}$, making operation at high system voltages of up to 1500 V very efficient.

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