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The description of the steps of the Q&A test and detector module assembly of the CBM-STS

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ABSTRACT

The Silicon Tracking System (STS) is the core detector system of the Compressed Baryonic Matter (CBM) experiment at FAIR (Facility for Antiproton and Ion Research). The CBM will study matter at the highest baryonic densities in collisions of nuclear beams with a stationary target. The expected long latency for identification and the changing signature of the events drive us to use self-triggered streaming readout. The CBM data collection will be based on time-stamped detector data into a compute farm. Event reconstruction and physics analysis are performed online at up to 10 MHz collision rates. In the presented work, we will discuss step-by-step how the CBM-STS detector components are rigorously selected and prepared for assembly. It starts with carefully testing the readout ASICs. The various parameters are recorded to select the chip. The next step is to test the micro cable's TAB (Tape Automated Bonding) bonding quality on the ASIC. Later, the 16-chip cables are bonded to the silicon strip sensor. All test results are stored and available for later use in a specially designed database using custom software applied to each step in the assembly process. After assembly of 1/3 of the modules (896), we will overview the acquired experience.

1. Introduction

The main goal of the CBM experiment is to study the properties of strongly interacting matter at high baryon densities. One objective is to study the phase structure of Quantum Chromodynamics (QCD) matter at high net baryon densities and moderate temperatures. This includes the search for the critical point of the QCD phase transition between baryonic matter and the quark-gluon plasma. In addition, the experiment aims to understand the behavior of matter under extreme conditions, such as those found in the cores of neutron stars or the Universe's early stages. This includes the study of collective flow, particle correlations, and fluctuations. Advanced detectors and data acquisition systems are used to analyze the resulting particle interactions and properties [1].

Based on silicon strip sensors, the STS provides precise tracking of charged particles produced in heavy-ion collisions for reconstructing tracks in the 1 T field of the superconducting dipole. The eight layers of sensors also assist in reconstructing the primary and secondary vertices of particle collisions, helping to identify short-lived particles and study their decay properties. It will operate efficiently at high collision rates, ensuring reliable data collection [2]. The thorough test of all components during the assembly is very crucial due to restricted access after installation. Also, the lowered temperature (down to −20 °C) of the readout electronics and the very high radiation environment, up to 10^{13} n/cm^2 (1 MeV equivalent) demand the possibly highest quality assurance from the assembly process.

2. Test procedures during the assembly

The very first step of the assembly process is to select individually tested read-outs and LDO ASICs. The readout ASIC (XYTER 2.2) fabricated at the UMC CMOS 180 nm process Fig. 1, is very sophisticated, 128 channel, 5-bit amplitude and 14-bit timestamp, dual polarity high bit-rate (max. 5 × 320 Mbps/link) and low power chip. In addition, the ASIC is equipped with an internal diagnostic circuit that measures the charge sensing amplifier (CSA) voltage and chip temperature. More than 14 000 XYTER chips are necessary for the STS readout. The individual ASIC test can be done using a pogo-pin socket or directly on a silicon wafer using a dedicated IP-bus-based software interface via an FPGA board. However, only around 4000 chips were tested manually, and more than 75 wafers, each containing 360 chips, are under automated testing. After testing about 30 wafers, only 5% of chips are rejected on average. During the ASIC test, all registers are tested for

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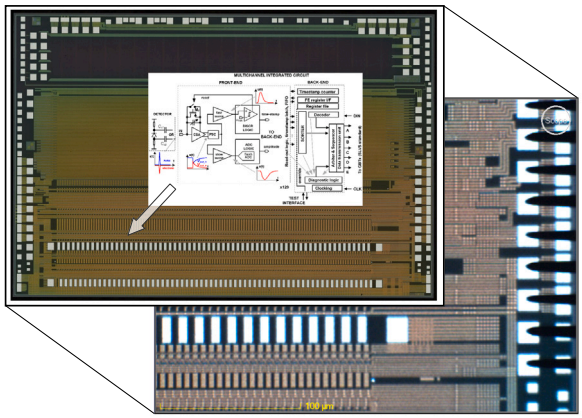

Fig. 1. The 10×6.75 mm^2 XYTER chip with 128 input channels, a schematic diagram-inlet, and a microscope picture of the wafer prober needles-back.

read and write, all 128 readout channels for both polarities and the internal diagnostic circuit is calibrated (Fig. 2). The XYTER chip is powered by three input voltages: 1.2 V for CSA and twice 1.8 V for digital and analog circuits. During testing, each line is continuously monitored (Figs. 3 and 4). When the test is successful, the 64-bit individual ID is burned, and all the data is stored in the database (see Fig. 5).

After readout chips are proven okay, the custom-made micro-cables of ultra-thin aluminum-polyimide are TAB-bonded on the chip. This step is also tested using ESD materials, contacting the cables, reading the chip using a pogo-pin socket for a minimal charge input, and validating the bonding quality (Fig. 2 lower). If the test shows all wires are connected, they are glued; otherwise, they are inspected and TAB-bonded again. This data is also stored in a dedicated database.

In parallel, the front-end boards (FEB) are cleaned in an ultrasound bath, and each component is optically inspected. The LDOs are wire-bonded on FEBs, of which four types are due to the detector concept. The fast FEB plays a pivotal role in our assembly process. It connects each readout ASIC with five uplinks for central modules and two for peripheral ones. We have two types for the positive and negative silicon side readout, which are geometrically mirrored. The LDO chips are tested in four steps: For no load, minimal power consumption; then, nominal power consumption; and finally, we push to maximum over-current to cause their custom function of automatic shut down, after which we power cycle and test briefly with nominal power again. When we collect eight readout chips with micro-cables bonded and tested and the FEB with LDOs bonded and tested, the corresponding side of the sensor can be assembled (Fig. 6). Before the silicon sensor is tab-bonded, testing both FEBs with 8 ASICs for digital communications and power consumption is made to ensure the quality of wire bonds and glob tops minimize the risk of errors. If all proves to be okay, the sensor will be TAB-bonded from both sides, and the bonds will be fixed with glue onto this assembled module. However, several steps remain before the module is mounted on a ladder and ready for assembly in the detector stations. The FEBs are glued to the cooling fins using two-component thermal glue. After that, the sensor will be biased to test dark current in silicon and prove that no current is leaking through the cooling fins. The module will be covered with electrical shielding panels and glued to the cooling fins. In the end, a thorough final characterization will be performed [3]. Here, we must emphasize that the whole assembly and testing procedure are done in a clean room environment. Each module undergoes cooling stress to meet the requirements of the detector's environment of negative 20 degrees. A climatic chamber filled with nitrogen controls the cooling of the modules from room temperature to negative 20 degrees. Five consequence powering cycles, on and off, and readout tests are performed at low temperatures.

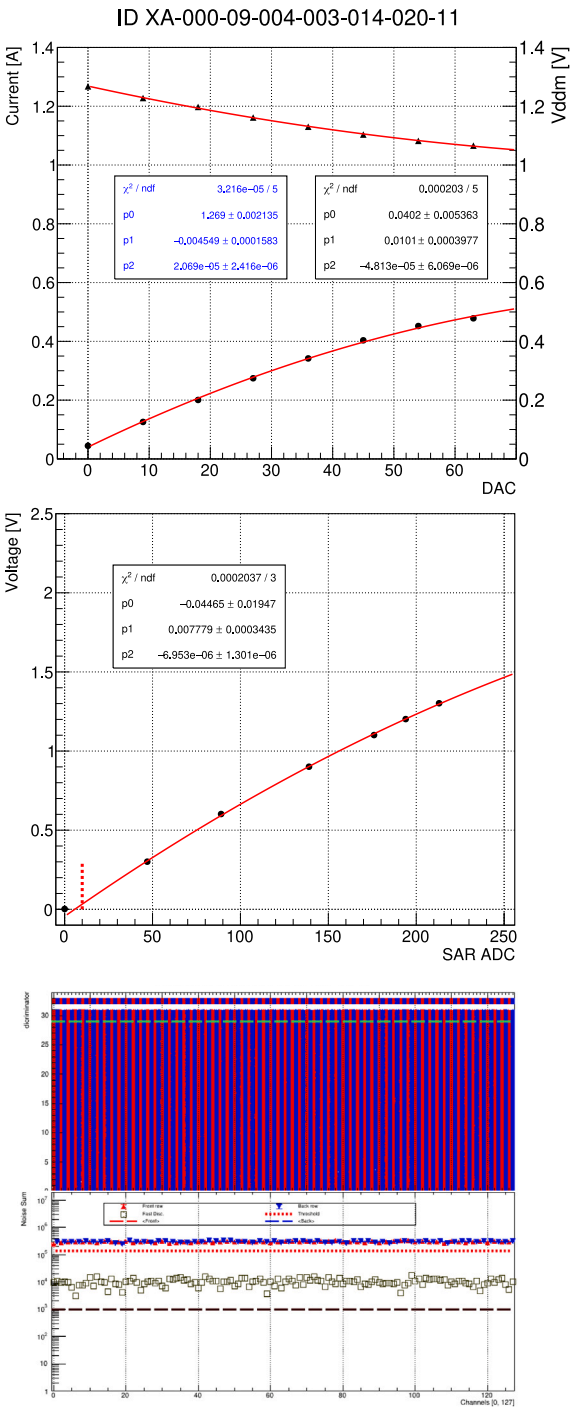

Fig. 2. Top-CSA calibration for different voltage and current. Middle-internal diagnostic ADC calibration. Lower-testing of all 128 channels time and 5-bit discriminators.

3. Summary

Two assembly sites with two well-trained teams were formed to meet the high production rate without compromising quality. While the whole module assembly and testing process is performed at GSI and KIT in parallel, wafer-level tests, module final characterization, and the final detector assembly will only be performed at GSI.

All the test results, including the calibration data from all steps and the raw measurement data, are collected in a centralized database at

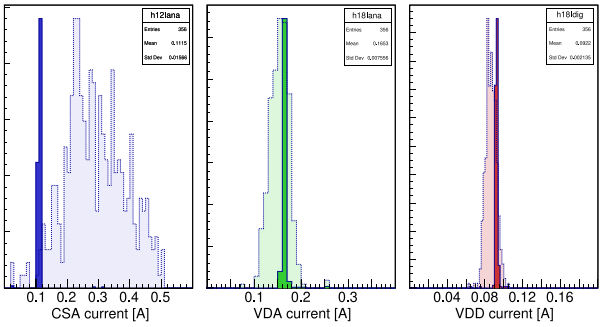

Fig. 3. The histograms of the current consumption of the XYTER chips at the powering up (transparent) and after initialization on a typical wafer.

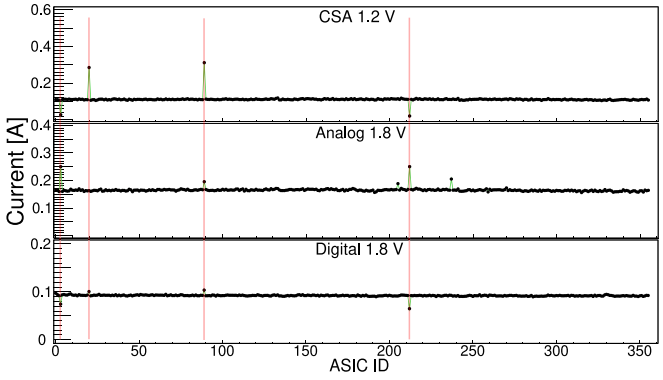

Fig. 4. The graph of all power lines vs. ASIC index after the chip initialization for the wafer level test.

the GSI computing infrastructure [4]. A dedicated PostgreSQL database with a custom-developed PHP and Phyton-based back-end is developed to monitor and exchange information using real-time API between both sites. About 900 modules are expected to be built and characterized for the final configuration. About 1/3 has already been produced and tested successfully. Only 13 out of the 267 assembled modules have been rejected, primarily due to increased sensor leakage current. Improved production quality throughput and further accumulation of experience are expected. We are optimistic that we will finish the project by 2028 and have a fully functional CBM-STS detector tested in the laboratory. The CBM experiment at the FAIR is scheduled to begin commissioning in 2028. This timeline aligns with the broader FAIR project schedule, which anticipates completing construction and starting scientific operations in the late 2020s.

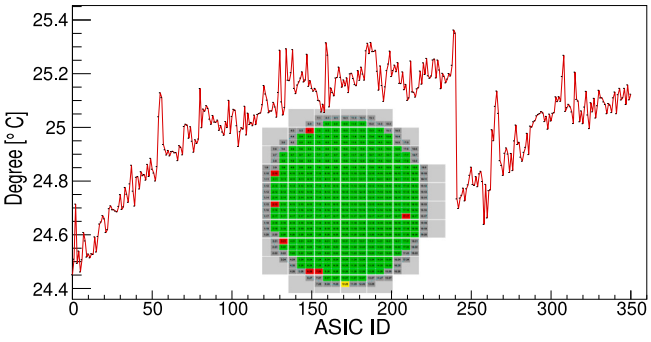

Fig. 5. The wafer temperature increase was measured using a digital thermometer attached to the chuck. The test was paused at index 240 and resumed the next day.

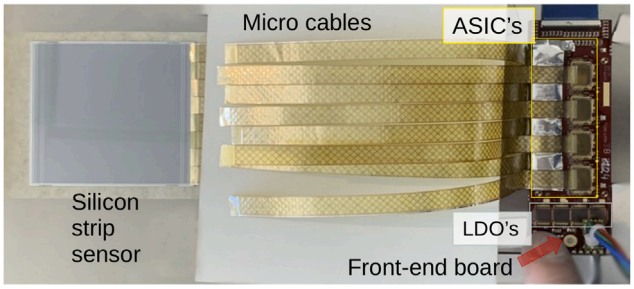

Fig. 6. The silicon sensor is at the last stage of assembly and testing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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