Solid-state reactions at the metal-semiconductor interface

Ohmic and Schottky contacts are common building blocks of semiconductor devices. They are based on metal/semiconductor interfaces, and thus prone to solid-state reactions forming silicides or germanides. Using a combination of in situ x-ray and optical curvature measurements, we could reveal the interplay between material reservoir, phase, and structure formation of as-deposited and thermally treated Pd/Ge bilayer systems. Our results illustrate how the microstructure evolution affects electrical resistivity and stress build-up, two exemplary figures of merit characterizing the device performance.

Interface-mediated solid-state reactions during annealing can be employed for tailoring the electronic properties of metal/semiconductor interfaces. However, already during deposition an ultrathin silicide or germanide layer can form at the interface. Our aim was to clarify the impact of this as-deposited interlayer on the solid-state reaction during subsequent annealing. We have combined real-time x-ray measurements during sputter deposition and annealing of only few nm thick palladium layers deposited on amorphous germanium (a-Ge). Interface-mediated reactions take place sequentially. In case of Pd deposition on Ge, Pd_2Ge is expected to form before PdGe. To study the influence of the material reservoir on the structure formation, we have varied the Pd:Ge ratio while maintaining the expected Pd_2Ge thickness constant. The growth study was performed using a customized, portable sputter chamber installed at the MED station of SIXS. The layer formation was monitored using a combination of x-ray reflectivity, grazing incidence x-ray diffraction, and optical curvature measurements [1].

Results

We found that the initially amorphous Pd_2Ge interlayer crystallizes after deposition of 1.5 nm Pd, forming a sharp interface with the subsequently growing Pd layer. Both layers are polycrystalline and highly textured. Our results confirmed the isostructural interlayer formation of Pd/a-Si [2] and Pd/a-Ge. In both cases, the interlayer serves as template for the subsequent Pd growth. The interference pattern and the similar texture of the Pd(111) and $Pd_2Ge(111)$ Bragg peaks indicate local epitaxial growth within each crystallite (Fig. 1). This implies a different lattice mismatch between Pd and Pd_2Ge or Pd_2Si, which was confirmed by qualitatively similar, but quantitatively slightly different real-time stress evolutions for both systems. The stoichiometric, but amorphous compound formation during early growth stages was verified by complementary in situ XPS measurements.

The structure evolution during deposition affects application-relevant properties of the bilayers: the crystallization of Pd_2Ge induces a tensile stress, which is counteracted by the lattice mismatch between Pd and Pd_2Ge, resulting in peak of the film force per unit width, F/w. Comparing the structural evolution with real-time electrical resistance measurements [3], we found that the interlayer crystallization (not the percolation of the Pd film) dominates the resistance drop during deposition. (Fig. 2). The films were annealed up to a temperature of 600 K. The interface-mediated Pd_2Ge formation during annealing takes place continuously (i.e., without critical temperature) via coherent growth of the as-deposited Pd_2Ge seed layer crystals (Fig. 3). The texture of the as-deposited interlayer is maintained. If the Ge supply is sufficiently large, PdGe nucleates at a critical temperature of 583 K. This second phase is also textured, confirming the importance of the interface for both phases.

Conclusion

We evidenced in real-time the impact of the as-deposited Pd_2Ge interlayer on stress and electrical resistivity changes during deposition, and on the microstructure evolution during subsequent annealing. The understanding and control of interlayer formation is of utter importance for the miniaturization of microelectronic devices, as it imposes a lower limit for the formation of self-organized metal/semiconductor compound layers and determines the quality of thermally grown silicide and germanide layers.

Figure 1

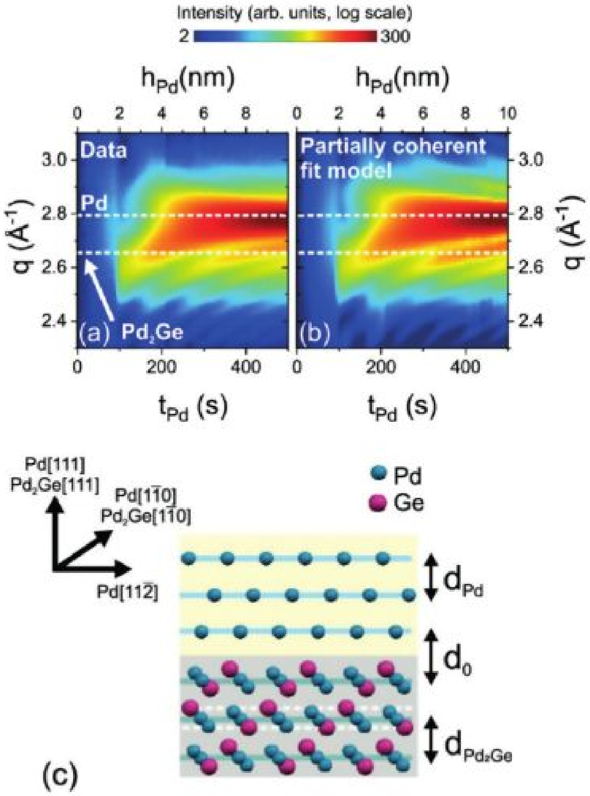


Figure 2

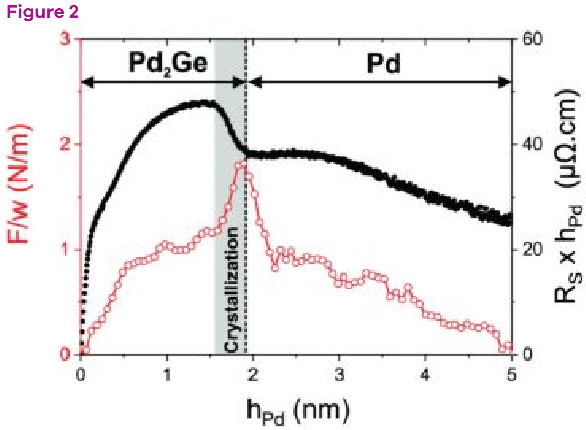
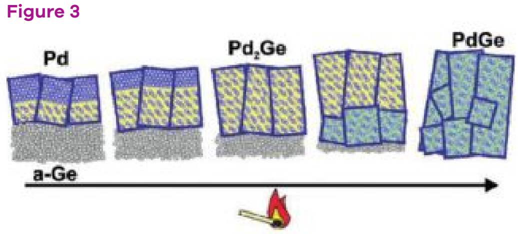


Figure 3



SIXS BEAMLINE

Associated publication

In Situ Study of the Interface-Mediated Solid-State Reactions during Growth and Postgrowth Annealing of Pd/a-Ge Bilayers.

B. Krause, G. Abadias, D. Babonneau, A. Michel, A. Resta, A. Coati, Y. Garreau, A. Vlad, A. Plech, P. Wochner & T. Baumbach.

ACS Applied Materials & Interfaces, 15(8): 11268 (2023).

References

[1] B. Krause *et al.*, ACS Appl. Mater. Interfaces, 8, 50, 34888 (2016).
[2] B. Krause *et al.*, ACS Appl. Mater. Interfaces 11, 42, 39315 (2019).
[3] J. Colin *et al.*, Nanomaterials, 10, 2225 (2020).

Corresponding author

Bärbel KRAUSE
Institut für Photonenforschung und Synchrotronstrahlung (IPS)
Karlsruher Institut für Technologie,
Eggenstein-Leopoldshafen 76344
Germany
baerbel.krause@kit.edu

Captions

Figure 1: (a) Experimental and (b) simulated XRD data, showing the evolution of the XRD signal during deposition. (c) Structural model assumed for the simulations.

Figure 2: Real-time curvature signal (red open circles, force per unit width) and resistivity (black dots) during deposition. The resistivity data were taken from Ref. [2]

Figure 3: Schematic of the phase formation during sputter deposition and subsequent annealing of Pd/a-Ge.