Broadband BPSK Transmitter Systems with Beam Steering at mm-Wave Frequencies

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Abstract

This thesis explores the uncharted territory of circuits, packaging solutions, and antenna systems for broadband high-datarate systems operating in the sub-THz spectrum. The thesis first presents the necessary theoretic basics and investigations to fully contextualize the design task. Further, the circuit design of the crucial power amplifier is unveiled and discussed. Next, the antenna choices are evaluated and the chosen designs are meticulously investigated. Based on this, the packaging of the whole transmitter is analyzed and detailed. The work concludes with the measurements of the implemented transmitters, revealing the groundbreaking performance of the realized systems.

The sub-THz frequency range between 100 GHz to 300 GHz offers a vast spectrum with currently little regulation. Firstly, principle investigation of the physical constraints is done to evaluate influences such as signal to noise ratio (SNR) and harmonic spurs. Further, limitations in the available measurement equipment are investigated to highlight issues in performance evaluation. A compact and efficient power amplifier (PA) is designed by carefully analyzing the state of the art of published PAs in the employed frequency range. Concluding this analysis, the decision is made to implement a pseudo-differential cascode topology in silicon-germanium (SiGe) as it offers the best trade-off between radio frequency (RF) performance, system integration and integration density. Based on this decision, two available metal stack-ups are analyzed and compared against each other to guide the choice of the best possible technology. With the technology choice fixed, the multi-stage design is investigated. The design is frequency-staggered and optimized for the necessary bandwidth and output power by employing transformer-coupled stages and carefully implemented feedback paths. Analysis of the whole system shows the excellent performance of the PA, which exceeds the state of the art in bandwidth, non combined output power, and compactness. Simulation and physical verification show a bandwidth of 74 GHz and an output power of 8 dBm in at a very small chip core area of 0.045 mm^2.

A novel approach within this thesis is the usage of a differential RF inter-

connect. Hence, differential antennas are investigated to exploit the system performance fully. For this, two different approaches are investigated. The first approach are printed circuit board (PCB) based antennas, successfully implemented and evaluated for the first time at this frequency range. The second approach uses a shorted bow-tie feeding element to achieve a compact and wideband on-chip antenna without using localized backside-etching (LBE) or through-substrate radiation. This design is novel and pushes the state of the art in on-chip antennas significantly in terms of integration, efficiency, and bandwidth. Reaching above 20 % relative bandwidth pushes the state of the art. The on-chip design employs either a 3D-printed resonator or a thin-film processed glass sheet as a parasitic resonator to enhance the bandwidth and efficiency. The PCB based design uses series-fed frequency staggered patches to achieve wideband operation on substrates with a solid ground plane and is a first of its kind at the tested frequencies.

Everything is tied together with a novel packaging approach using impedance-tailored differential bond wires connecting the monolithic microwave integrated circuit (MMIC) to the antennas. The RF-transition is analyzed in detail, and the design methodology is explained. Further, the packaging solutions for the 64 GHz local oscillator (LO) signal and the wideband baseband (BB) signal with frequencies up to 50 GHz are explained.

Lastly, the implemented transmitter systems are investigated. In total, four different systems are built. Two transmitters with a single chip, each using either a PCB-antenna or the resonator-loaded antenna, and two phased arrays with a 1x2 and 1x4 configuration using the resonator-loaded antennas are investigated. All systems are measured for their RF-performance and the antenna pattern. Further, a novel investigation of bit error rate (BER) over angle, bit-rate, distance, and beam-steering is done to analyze the static behavior and the truly achievable data rates over real-world conditions. The presented results and the demonstrated system exceed the state-of-the-art regarding the tested data-rate with rates up to 32 Gbit s^{-1} and array steering evaluations. In comparison to the state of the art the system shows an excellent efficiency of 41.4 pJ bit^{-1} while being smaller than any other reported system.

Together, the results of this thesis not only contribute to the academic understanding of the technologies for the sub-THz band but also pave the way for its future commercial exploitation. The novel RF transition and the ability to shrink system size while increasing design flexibility are the stepping stones for future high data-rate systems, inspiring a new era of possibilities in the field.

Zusammenfassung

Diese Arbeit erforscht neue und innovative Lösungen im Bereich der Integrierten Schaltkreise, Aufbautechniken und Antennen für hoch-integrierte Sendesysteme im sub-THz Frequenzbereich. Die Arbeit stellt zunächst die notwendigen theoretischen Grundlagen und Untersuchungen vor, um die Entwurfsaufgabe vollständig zu kontextualisieren. Darauf aufbauend wird der Schaltungsentwurf der Schlüsselkomponente Leistungsverstärker vorgestellt und diskutiert. Anschließend werden die möglichen Antennenlösungen identifiziert, gegeneinander Bewertet und anhand von Messungen qualifiziert. Darauf aufbauend wird die Aufbautechnik des gesamten Senders analysiert und detailliert beschrieben. Die Arbeit wird konkludiert durch die Messungen der implementierten Sender, die die ausgezeichnete Leistung der Sende unterstreicht.

Der Sub-THz-Frequenzbereich zwischen 100 GHz und 300 GHz bietet ein breites verfügbares Frequenzspektrum mit derzeit wenig rechtlichen Einschränkungen. Daraus ergibt sich eine Vielzahl an möglichen Realisierungen. Um die Auswahl einzugrenzen und zu Begründen wird eine grundlegende Untersuchung der physikalischen Beschränkungen durchgeführt. Dabei werden Einflüsse wie SNR und harmonische Spurs im Gesamtkontext bewertet. Weiterhin werden die Limitationen der derzeitig verfügbaren Messgeräte untersucht, um Probleme bei der Leistungsbewertung aufzuzeigen.

Aufbauend auf dem Stand der Technik werden die Realisierungsmöglichkeiten des Leistungsverstärkers eingegrenzt. Als Resultat dieser Analyse wird die pseudo-Differentielle Kaskodentopologie ausgewählt. Diese bietet die beste Abwägung zwischen Funktionalen Aspekten und der Integrationsdichte. Auf der Grundlage dieser Entscheidung werden zwei verfügbare Metall-Stack-ups analysiert und miteinander verglichen, um die Technologiewahl detailliert zu begründen. Basierend darauf wird ein mehrstufiger Verstärkeransatz untersucht. Das Design ist Frequenzgestaffelt und für die erforderliche Bandbreite und Ausgangsleistung optimiert. Dies wird durch den Einsatz von Transformatoren zwischen den Stufen und sorgfältig gewählten Rückkopplungspfaden

ermöglicht. Die anschließende Analyse des Gesamtsystems und die Diskussion der gewonnenen Erkenntnisse zeigen die hervorragende Leistung des Verstärkers, der den Stand der Technik in Bezug auf Bandbreite, nicht kombinierte Ausgangsleitung und Kompaktheit übertrifft. Simulationen und Messungen zeigen eine Bandbreite von 74 GHz und eine Ausgangsleistung von 8 dBm in einer Fläche von gerade einmal 0.045 mm^2.
Ein neuer Ansatz in dieser Arbeit ist die Verwendung einer differentiellen RF-Verbindung. Diese erfordert auch differentielle Antennen, wofür zwei verschiedene Ansätze untersucht werden. Der erste Ansatz betrachtet PCB-basierte Antennen, die in dieser Arbeit zum ersten Mal in diesem Frequenzbereich erfolgreich implementiert wurden. Der zweite Ansatz nutzt ein kurzgeschlossenes Bow-Tie-Speiseelement, um eine kompakte und breitbandige On-Chip-Antenne ohne Verwendung von LBE oder Strahlung durch das Substrat zu realisieren. Dieses Design ist neuartig und bringt den Stand der Technik bei On-Chip-Antennen in Bezug auf Integration, Effizienz und Bandbreite erheblich voran. Mit relativen Bandbreiten über 20 % wird der Stand der Technik deutlich übertroffen. Das On-Chip-Design verwendet wahlweise einen 3D-gedruckten Resonator oder Metallische Resonatoren auf einem Glasplättchen, um die Bandbreite und Effizienz zu erhöhen. Das PCB-basierte Design verwendet seriengespeiste, frequenzversetzte Patches, um die Breitbandigkeit auf Substraten mit durchgehender Massefläche zu erreichen. Dieser Ansatz ist der erste dieser Art in dem gewählten Frequenzbereich.
Die Aufbautechnik basiert auf einem innovativen Konzept, bei dem impedanzangepasste differentielle Bonddrähte den MMIC mit den Antennen verbindet. Der RF-Übergang wird im Detail analysiert, und die Entwurfsmethodik wird erläutert. Außerdem werden die Packaging-Lösungen für das 64 GHz LO-Signal und das breitbandige BB-Signal mit Frequenzen bis zu 50 GHz erläutert.
Abschließend werden die implementierten Sendersysteme untersucht. Insgesamt wurden vier verschiedene Systeme gebaut. Zwei Sender mit je einem Chip, die jeweils entweder eine PCB-Antenne oder die resonatorgeladene Antenne verwenden. Dazu werden zwei Phased-Arrays mit einer 1x2 und 1x4 Konfiguration unter Verwendung der resonatorgeladenen Antennen untersucht. Alle Systeme werden hinsichtlich ihrer RF-Performance und des Antennendiagramms gemessen. Außerdem wird eine Analyse des BER über Winkel, Bitrate, Entfernung und Strahlsteuerung durchgeführt, um das statische Verhalten und die tatsächlich erreichbaren Datenraten unter realen Bedingungen zu analysieren. Die vorgestellten Ergebnisse und das demonstrierte System übertreffen den Stand der Technik hinsichtlich der getesteten Datenratenraten

bis hin zu 32 Gbit s^{-1} und dem Detailgrad der Untersuchung im Bezug auf BER über Winkel und Distanz. Dabei zeigt sich im Vergleich die hohe Effizienz von 41.4 pJ bit^{-1} bei gleichzeitig kompakten Aufbau des binary phase shift keying (BPSK)-Transmitters als besonders positiv.
Zusammenfassend tragen die Ergebnisse dieser Arbeit nicht nur zum akademischen Verständnis der Technologien für das Sub-THz-Band bei, sondern ebnen auch den Weg für dessen zukünftige kommerzielle Nutzung. Der neuartige RF-Übergang und die Fähigkeit, die Systemgröße zu verringern und gleichzeitig die Design-Flexibilität zu erhöhen, sind ein Sprungbrett für künftige Systeme mit hoher Datenrate.

Preface

This thesis was written during my time as a research associate at the Institute of Radio Frequency Engineering and Electronics (IHE) at the Karlsruhe Institute of Technology (KIT).
First of all, I would like to thank Prof. Dr.-Ing. Dr. h.c. Thomas Zwick for enabling me to pursue this scientific journey and giving me the freedom to explore many different aspects. I want to extend my sincere thanks to Prof. Dr. sc. techn. habil. Dipl. Betriebswissenschaften Frank Ellinger for his interest in my work and for willingly accepting the co-lecture. I would also like to thank Prof. Dr.-Ing. Cagri Ulusoy for the discussions about integrated circuits and the possibilities of being part of the circuit design team of IHE. Lastly, many thanks go out to Luca Steinweg for the good time on our shared journey tackling our project.
I also want to express my appreciation for those who have been with me through the ups and downs of my scientific journey. Christian Bohn, in particular, has been a valuable discussion partner, providing support and insights during the many hours we spent navigating our scientific challenges. I am also grateful to Alexander Quint and Elizabeth Bekker, who have been both roommates and friends, offering companionship and support over the years. I also want to acknowledge the contributions of Luca Valenziano, Marius Kretschmann, and Georg Gramlich, who provided valuable scientific input and offered a much-needed distraction from our academic pursuits. Lastly, a heartfelt thank you to all the people within the IHE and around the campus who supported me with valuable discussions their help.

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Berlin, September 2024

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Symbols and Abbreviations

Abbreviations

AC alternating current
ACP air co-planar
ASK amplitude shift keying
AWG arbitrary waveform generator
AWGN additive white gaussian noise
BB baseband
BEOL back-end of line
BER bit error rate
BPG bit pattern generator
BPSK binary phase shift keying
CMA characteristic mode analysis
CMIM capacitor with metal isolation metal layer
CMOM capacitor with metal oxide metal layer
CMOS complementary metal-oxide-metal
CPW coplanar waveguide
DAC digital to analog converter
DC direct current
DFG Deutsche Forschungsgemeinschaft
DRC design rule check
DSP digital signal processor
DUT device under test
EIRP equivalent isotropic radiated power
EM electro-magnetic
EVM error vector magnitude

FEC forward error correction
FFC flat-flex connector
FSK frequency shift keying
FSPL free space path loss
GCPW grounded coplanar waveguide
GSG ground signal ground
GSSG ground signal signal ground
HBT heterojunction bipolar transistor
IC integrated circuit
IF intermeditate frequency
ILA integrated lens antenna
ISS impedance standard substrate
LBE localized backside-etching
LCP liquid crystaline polymer
LDO low dropout regulator
LO local oscillator
MMIC monolithic microwave integrated circuit
MOS metal oxide semiconductor
MSG maximum stable gain
OP1DB output referred 1 dB compression point
PA power amplifier
PAE power added efficiency
PAPR peak-to-average power ratio
PBO power amplifier back-off
PC personal computer
PCB printed circuit board
PLL phase locked loop
PSK phase shift keying
QAM quadrature amplitude modulation
QPSK quadrature phase shift keying
RF radio frequency
SAP semi additive processing
SiGe silicon-germanium

SLA stereolithography
SMD surface mounted device
SMU source measurment unit
SNR signal to noise ratio
TDR time domain reflectometry
T/R combined transmit and receive
UE user equipment
USB universal serial bus
VIA vertical interconnect access
VNA vector network analyzer
WiFi set of standard relating to wireless LAN

List of Symbols

α	Attenuation constant
a_i	Complex power-wave flowing into port i in $\sqrt{\mathrm{W}}$
A_i	Amplitude
$A\,(\omega)$	Transfer function
β	Phase constant
b_i	Complex power-wave flowing out of port i in $\sqrt{\mathrm{W}}$
BW	Bandwidth in Hz
C	Capacitance in F
C	Channel capacity in bit s^{-1}
γ	Complex propagation constant
Δz	Infinitesimal length in m
D	Antenna directivity
d	Distance in m

η	Efficiency
ϵ_r	Relative permittivity
f	Frequency in Hz
f_0	Center frequency in Hz
$f_\mathbf{t}$	Transit frequency in Hz
$f_\mathbf{max}$	Maximum oscillation frequency in Hz
G	Conductance in S
$G_\mathbf{re}$	Realized gain
g_n	Size identifier in m
h_n	Height in m
k	Wavenumber in m^{-1}
L	Inductance in H
l	Length in m
λ	Wavelength in m
$\mathbf{M}$	Transforming matrix
N	Multiplication factor
ω	Angular frequency in rad
P	Power in W
ϕ	Phase in rad
Q	Quality factor
Q_n	Transistor identifier
R	Resistance in Ω
r_n	Radius in m
S	Radiation intensity in W

S_0	Radiation intensity of an isotropic source in W
$\mathbf{S}$	S-parameter matrix
S_{ij}	S-parameter with wave impeding on port j and exiting port i
$\mathbf{S_M}$	Mixed-mode S-parameter matrix
s_n	Separation in m
SNR	Signal-to-noise ratio
t	Time in s
$\tan\delta$	Dielectric loss tangent
V	Voltage in V
v^+	Voltage on the positive node of a differential node in V
v^-	Voltage on the negative node of a differential node in V
w_n	Width in m
Z_0	Complex Impedance in Ω
z_n	Height in z-direction in m

1 Introduction

Since its inception three decades ago, the internet has seen unprecedented growth in not only the usage of computers, digital services, and data transmission but also due to the desire of humans to connect and communicate. Where in the past time, phone lines were realized as physical cables and were always bound to a physical location, the introduction of the wireless phone and associated standards marked a shift in how we communicate. The advent of smartphones marked another significant change. With fully featured computers portable and accessible to many, connected wirelessly to a seamless network of computers, servers, and overall, people, the desire for more and better data links is more pressing than ever.

The underlying technology is often underrepresented in its role of advancing the internet and enabling the digital world as we know it. New developments in complementary metal-oxide-metal (CMOS), SiGe, and III-V semiconductor technology pushed the technically possible. Especially fiber optics saw a significant improvement over the years, achieving over 1 Pbit s^{-1} per fiber [RLP+22] building the backbone of the internet. But not only optical communication has proliferated. Wireless technologies profited massively from better analog circuits, higher efficiencies, and more computational power. Higher modulation schemes and more compensation for non-ideal RF behavior continuously push the achievable data rate even in congested urban environments and adverse conditions. However, these staggering speeds are often brought with bulky and power-hungry equipment unsuitable for direct consumer interaction or implementation in user equipment (UE).

Even though technology is advancing fast, wireless links are also limited by the available bandwidth and government regulations. The frequency range below 6 GHz is limited in the available bandwidth and shared between many different services. Hence, industry and research are looking into higher operating frequencies offering more bandwidth. This incentive created new frequency bands at 28 GHz and 60 GHz. However, predictions show that these new bands

will not suffice, so even higher frequencies are targeted. The largest window currently planned ranges from 64 GHz to 71 GHz but even higher frequencies are considered [Fed22].

Operating frequency alone is not the only factor limiting data-rate. Congestion on shared channels and regulations force a lot more overhead on the protocol layer, further decreasing the data-rate. To make the most of the available channel bandwidths and transmission windows higher order modulations are used. These necessitate power hungry IQ-Systems and pre-distortion to exploit the analog hardware and channel to the fullest. The set of standard relating to wireless LAN (WiFi) chipset in a smartphone needs between 1.3 nJ bit^{-1} to 5 nJ bit^{-1} to achieve a speed of 400 Mbit s^{-1} [AGB+21]. Even worse is 5G with an energy per bit of 500 nJ bit^{-1} depending on traffic [XZZ+20].

Considering the mentioned points, seeking higher operating frequencies to bridge the gap between backbone infrastructure and UE becomes detrimental. Increasing the frequency also reduces antenna sizes to the point where high-gain antennas or larger antenna arrays can fit comfortably, even in smartphones. In contrast, larger absolute bandwidth availability in the frequency spectrum allows simpler modulation schemes to reduce power consumption and circuit complexity. A possible downside is the higher atmospheric attenuation coupled with free space path loss limiting the range. However, this can also be seen as a benefit in crowded scenarios as spatial multiplexing becomes more manageable. Even simple physical objects like thin walls can serve as effective shielding between multiple transmission channels, reducing the necessary protocol layer.

Choosing a new, significantly higher frequency band is constrained by certain physical limitations. Water absorption windows in the atmosphere drive the choice of suitable channels outside of applications in space. One such window is around 140 GHz and is currently under investigation for the upcoming 6G standard [AAKG23]. Nevertheless, as advancements in the silicon-based transistor technology offer us transistors exceeding an $f_{\max}$ of 500 GHz, even higher frequencies can be investigated. This is mainly driven by advancements in SiGe-based transistors, where the base region of a vertical NPN-transistor is doped with germanium to enhance the drift velocity and increase the operating frequency. IHP was the first to offer transistors with an $f_{\max}$ over 500 GHz (DotFIVE) in 2015 [CCL+10] and recently offered the next gener-

ation of technology with an f_{max} of over 700 GHz (DotSEVEN) [SBd+16]. However, the latter technology was introduced too late to be used in this work.

Concerning the transmission medium and frequency the absorption window around 254 GHz offering up to 100 GHz of bandwidth [PAB+21] is quite interesting. Which, if utilized with a quadrature amplitude modulation (QAM) 1024 signal, could lead to 1 Tbit s^{-1} data transmission. As work in this range is under investigation, no real spectrum assignment by governing bodies is present. First attempts in standardization are done with IEEE 802.15.3d, describing a channel from 252 GHz to 325 GHz for point to point communication with up to 100 Gbit s^{-1} [IEE17]. However, neither the American Federal Communication Commission (FCC) [Fed22] nor the European Electronic Communications Committee (ECC) [Ele23] have allocated this standard or anything else above 275 GHz and only rudimentary satellite bands between 100 GHz to 275 GHz, making it still a free space to explore different concepts and frequencies.

1.1 Objective of this Thesis

In the Deutsche Forschungsgemeinschaft (DFG) funded project "ADAMIS" (Adaptive Millimeter Wave Transmitters), the aim is to develop a power-efficient and compact BPSK transmitter with beam steering capability. Fig. 1.1 illustrates the system's general concept. The LO and BB signals are externally generated and fed into the MMIC to be designed. The LO signal is fed into a phase shifter ranging from 0° to 90°. It precedes the times four multiplier chain to achieve a continuous 0° to 360° phase shift in the RF domain. An amplifier buffers the multiplied LO-signal before it drives the modulator. The modulator is a modified gilbert cell which uses the BB signal to switch the LO signal between 0° and 180°, creating the BPSK modulation. The output signal is fed into the PA, which is connected to the antenna. A phased array system is realized by combining multiple MMICs.

A low-order modulation scheme like BPSK reduces the spectral efficiency but also the circuit complexity. BPSK modulation can directly be created by the use of a modulator. Not needing a digital to analog converter (DAC) and a digital signal processor (DSP) chain to calculate high bit-rate modulation waveforms decreases overall system complexity severly and reduces power consumption. Baseband circuits with a binary output are currently available

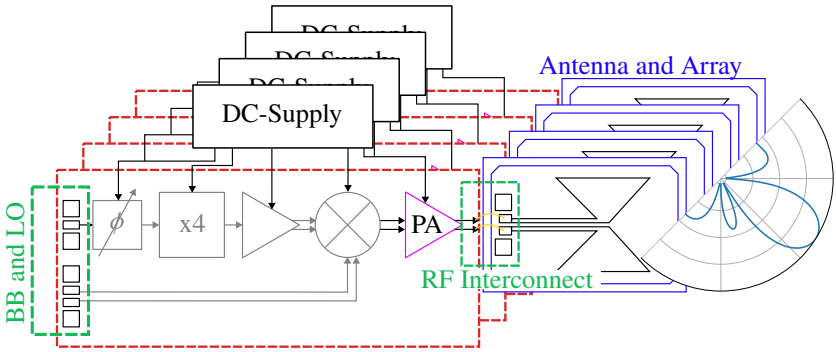


Figure 1.1: Overview of the system architecture with designated tasks and array configuration.

up to 28 Gbit s^{-1} [HCY+13], hence a BPSK system can directly feed the binary bitstream into the modulator bypassing a large portion of traditional transmitter circuitry.

The components shaded in gray in Fig. 1.1 are developed by the *Chair of Circuit Design and Network Theory* at *Technische Universität Dresden*, as described in the dissertation of *Luca Steinweg* [Ste23]. This works investigates besides the wideband PA also wideband antennas, packaging for wideband signals, and adaptivity at both MMIC and system levels. Previous efforts in this frequency range have been limited by fixed setups, hindering their versatility across usage scenarios, a limitation this work aims to overcome.

Considering these factors, the decision was made to operate around 246 GHz, providing ample bandwidth of at least 50 GHz. This avoids equipment limitations and offers more headroom for transistors. This choice of frequency center allows for technological and practical benefits without current regulation constraints.

Furthermore, this dissertation focuses on developing a system suitable for future applications within the last-meter domain, distinct from high-gain antenna-based systems designed for long-range communication. The emphasis is on creating a flexible chip and packaging concept that can adapt to various applications within the last meter domain or UE scenarios. Hence a phased array solution is sought that adapts dynamically to the presented scenario.

The thesis covers three main areas of work: designing a power amplifier that meets bandwidth, output power, and efficiency requirements while being co-designed with system interconnect solutions and antenna concepts; developing RF interconnect solutions, including packaging that balance performance with flexibility and adaptability; and designing an antenna concept suitable for phased array applications with targeted data rates, ensuring seamless integration with the overall system design. Finally all three parts are tied together to realize a phased array transmitter system.

1.2 Structure of this Thesis

The first chapter describes the work's motivation and the objectives and framework wherein this work is done.

Chapter 2 provides an introduction into the necessary theoretical concepts to contextualize the work of this theses. First the mathematical representation of differential RF circuits are presented. Next the conductor based transmission of such signals is investigated. This is concluded by a short overview of antennas theory. Further, digital modulation schemes are explained and lastly the circuit design aspects of PA design is detailed.

Chapter 3 introduces system aspects and considerations, presenting mathematical and physical groundwork for the used target metrics and goals. Physical limitations and trade-offs are also described to contextualize the results.

Chapter 4 introduces the power amplifier design and the measurement results of the amplifier itself. After presenting a thourogh state of the art analysis the proposed design is introduced and explained. Different possible technologies are compared against each other and the best option chosen. The desgin details are highlighted and the final design characterized.

Chapter 5 introduces the antenna concept, and chapter 6 presents the packaging of the whole system.

Finally, chapter 7 presents the measurement of the realized transmitter samples over many measured metrics. For this, the measurement setup is introduced and described. Then, two different concepts of a single MMIC with antenna is measured and compared against each other. Using BER measurements

as a direct transmission quality metric, the transmitters are evaluated over transmission angle, distance, and data rate. Based on these measurements, two phased-array systems are measured and compared against each other.

Lastly, chapter 8 concludes and gives an outlook for future research.

2 Physical Background

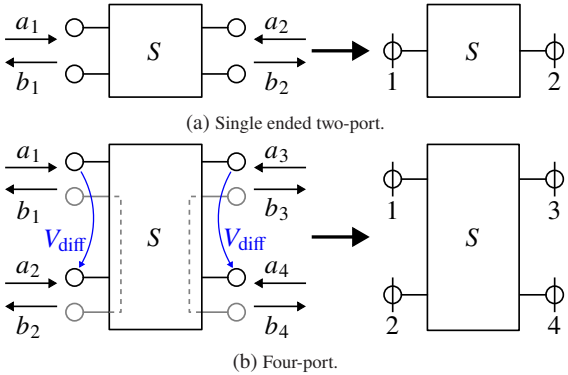
Pushing the state of the art in mmWave and THz transceivers means pushing the boundaries of the technologically possible. This necessitates a deeply rooted understanding of many of the underlying physical concepts and their implication for the design, analysis and measurement. In the following, certain key aspects will be presented and the intricate details explained.

2.1 Differential S-Parameters

S-Parameters are a highly effective metric to analyze and characterize RF systems and components and found widespread use in the realm of RF system design [Poz05]. One main advantage over time domain voltages and currents is the possibility to measure them at high frequencies and on wave guiding structures, that have no definition for voltage nodes and currents. Further, they are mathematically cascadable allowing to calculate the overall performance based on component wise measurements. Hence they play a vital role in analyzing circuits, transitions and antennas designed within this work.
The definition of S-parameters is based on single ended circuits as shown in Fig. 2.1(a). Each port of the exemplary 2-port device is constituted of two pins to complete a current loop in circuit analysis. Conceptually, a power wave a_1 is impinging on port 1 of the device, which results in a partly reflected wave b_1 and a transmission on port 2 with b_2. The power waves are defined as

$$a_i = \frac{1}{2} k_i \left(V_i + Z_i I_i \right), \tag{2.1}$$

$$b_i = \frac{1}{2} k_i \left(V_i + Z_i^* I_i \right), \tag{2.2}$$



(a) Single ended two-port.

(b) Four-port.

Figure 2.1: Schematic S-parameter definitions.

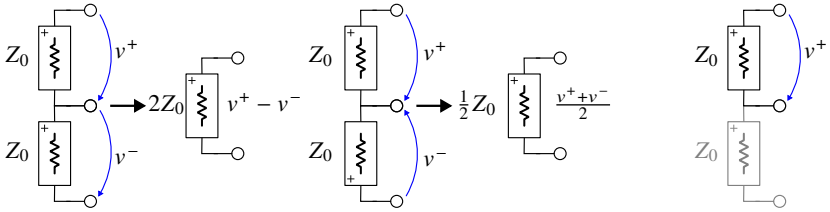
with k_i being

$$k_i = \left(\sqrt{\mathbb{R}\{Z_i\}}\right)^{-1}. \tag{2.3}$$

They relate the voltage V_i on port i to the current I_i with the characteristic impedance on the respective port Z_i. Hence, the have the unit $\sqrt{\mathrm{W}}$ as the represent a quasi power wave [Kur65].
The S-parameters for the two-port shown in Fig. 2.1(a) are then calculated as

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0}, \quad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0},$$
$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0}, \quad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}.$$

Expanding this formulation for differential systems is not directly possible. Differential signaling is based on two signal conductors that are 180° out of phase. The signal is the difference between both signal conductors, resulting in a cancellation of common mode currents and voltages. Based on this, the voltages and currents used for the definition of a_i and b_i are not clearly defined. One approach to overcome this limit is the extension of the differential port into two independent single ended ports as indicated in Fig. 2.1(b) by using an additional reference pin on each port [Poz05]. This extension is however only



(a) Odd-Mode (b) Even-Mode (c) Single-Ended

Figure 2.2: Possible stimuli for a differential port.

applicable in very specific circumstances. Investigating the electrical behavior on a differential port, three distinct cases can be identified as shown in Fig. 2.2. The ideal case, also called odd-mode, is the differential feed with the electrical signals on both pins 180° apart as shown in Fig. 2.2(a). Fed from two single ended sources with impedance Z_0, this yields a virtual feeding impedance of $2Z_0$. The opposing case is the even-mode, where both signals are in-phase, yielding the stimulus shown in Fig. 2.2(b). Here both sources are in parallel yielding a virtual impedance of $0.5Z_0$. A third extreme case is the feed with only a single signal on one of the differential pins [Poz05].

Concerning the voltages v^+ and v^- we can write them as

$$v^+ = A_1 e^{j(\omega t + \phi_1)}, \tag{2.4}$$

$$v^- = A_2 e^{j(\omega t + \phi_2)}. \tag{2.5}$$

The differential voltage across the two pins of the terminal is then

$$V_{\text{diff}} = v^+ - v^-, \tag{2.6}$$

$$V_{\text{diff}} = A_1 e^{j(\omega t + \phi_1)} - A_2 e^{j(\omega t + \phi_2)}. \tag{2.7}$$

The three cases in Fig. 2.2 can now be described by the relation of amplitude and phase of each signal. For the symmetric stimulus the amplitudes are the same $A_1 = A_2$ but the phase difference either $\phi_1 - \phi_2 = 0$ or $\phi_1 - \phi_2 = 180$ for even and odd-mode respectively. The single ended case sees one amplitude to be zero. However, any combination of phase and amplitude is possible which is described as the superposition of the three distinct cases.

Lastly, if the device under test (DUT) can be assumed to be a linear network the superposition of the input signals has to be possible. This allows to measure or simulate a differential two-port as a single-ended four port device. The resulting single-ended 4x4 S-parameter matrix **S** then can be used to calculate the odd- and even-mode response. This can be handily achieved by a matrix multiplication

$$\mathbf{M} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix}, \tag{2.8}$$

(2.9)

resulting in the mixed mode S-parameter matrix

$$\mathbf{S_M} = \mathbf{M} \cdot \mathbf{S} \cdot \mathbf{M^{-1}}. \tag{2.10}$$

The matrix **M** is used to calculate the two cases of odd- and even mode stimulus. The resulting mixed mode matrix

$$\mathbf{S_M} = \begin{bmatrix} S_{\mathrm{dd11}} & S_{\mathrm{dd12}} & S_{\mathrm{dc11}} & S_{\mathrm{dc12}} \\ S_{\mathrm{dd21}} & S_{\mathrm{dd22}} & S_{\mathrm{dc21}} & S_{\mathrm{dc22}} \\ S_{\mathrm{cc11}} & S_{\mathrm{cc12}} & S_{\mathrm{cc11}} & S_{\mathrm{cc12}} \\ S_{\mathrm{cc21}} & S_{\mathrm{cc22}} & S_{\mathrm{cc21}} & S_{\mathrm{cc22}} \end{bmatrix} \tag{2.11}$$

consists out of the differential and common-mode S-parameters as well as the common-to-differential and differential-to-common mode parameters [Zhu10]. That is the common-mode response to a differential-mode stimulus and vice versa. This analysis approach can also be used for three port devices such as

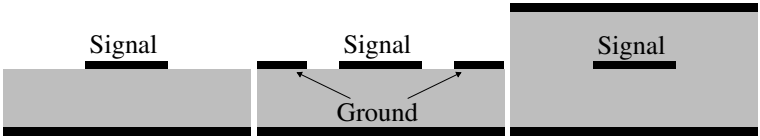
baluns, that convert a single ended input to a differential output. Assuming the single ended port to be port three, the matrix is

$$\mathbf{M}_{\text{mixed}} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 \\ 1 & 1 & 0 \\ 0 & 0 & \sqrt{2} \end{bmatrix}, \tag{2.12}$$

$$\mathbf{S_M} = \begin{bmatrix} S_{\text{cc11}} & S_{\text{dc11}} & S_{\text{sc12}} \\ S_{\text{cd11}} & S_{\text{dd11}} & S_{\text{sd12}} \\ S_{\text{cs21}} & S_{\text{ds21}} & S_{33} \end{bmatrix}. \tag{2.13}$$

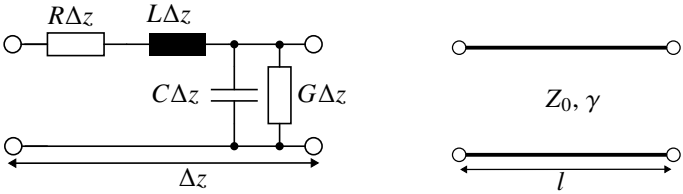
With these new formed two-port matrices, established analysis tools like rollet-k factor or maximum stable gain (MSG) can be applied to study the linear differential circuit. While these calculations are fairly easy and yield accurate results, they are only applicable to linear systems such as passive circuits and small-signal analysis of active circuits. Non-linear systems necessitate a true to real world stimulus, which is however not necessarily defined. As evident from Eq. 2.7 any combination of amplitude and phase might be present at the input of a device, which theoretically needs to be evaluated to check for instability or other issues. This is impractical and has to be reduced to the stimulus expected within the application.

One last issue with differential circuit analysis is the presented impedance for the different stimulus cases shown in Fig. 2.2. The simple approach to model the feed as two independent sources with impedance Z_0 is only valid in some applications. There are however antennas, transmission lines or transformers that do not present themselves as two sources but present rather different impedances for the different cases. A transformer should present itself as an open circuit to a common-mode signal as the current through the coil is zero, while the differential signal will couple through. Practically this can cause common-mode voltage swing issues with the common-mode wave being reflected back into the DUT if not properly designed [WRE06].



(a) Microstrip (b) (G)CPW (c) Stripline

Figure 2.3: Cross section through different planar transmission lines.



(a) Distributed Model (b) Lumped Model

Figure 2.4: Different Model Views.

2.2 Differential Planar Transmission Lines

Transmission lines are conductor based waveguides essential in almost all RF systems. Some of the most common planar types are the microstrip line, the coplanar waveguide (CPW) and the strip line as shown in Fig. 2.3. Within planar circuits and especially MMICs the microstrip and grounded coplanar waveguide (GCPW) lines are favored [Raz98].

From [Poz05], a transmission line can be approximated by a series inductor and resistor as well as a parallel capacitor and conductance as shown in Fig. 2.4(a). This network has to be distributed along the length z of the conductor in steps Δz significantly smaller than the wavelength $\Delta z << \lambda/10$. As calculating the response of a large network of small elements is time consuming, a lumped element model of a transmission line is developed. It is based on the apparent line impedance Z_0, a complex propagation constant γ and the physical length l.

The characteristic impedance relates to the elements of the distributed model with

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.14}$$

as shown in [Poz05]. If the losses in the transmission line are negligible small, which is the desired state in most transmission lines Eq. 2.14 simplifies to

$$Z_0 \simeq \sqrt{\frac{L}{C}}. \tag{2.15}$$

The complex propagation constant is

$$\gamma = \sqrt{(R + j\omega L)\,(G + j\omega C)}. \tag{2.16}$$

With the assumption that the lines are low loss, which is expected in most applications, it can be expanded to

$$\gamma = \alpha + \beta, \tag{2.17}$$

$$\alpha \simeq \frac{1}{2}\left(\frac{R}{Z_0} + GZ_0\right), \tag{2.18}$$

$$\beta \simeq \omega\sqrt{LC}, \tag{2.19}$$

as shown in [Poz05].

To extend the single-ended microstrip line to a differential line, an additional signal conductor is placed in parallel to the first one as shown in Fig. 2.5. From the plotted field lines a significant difference between the single ended and differential case is visible. The coupling between the lines significantly influences the characteristic impedance of the even and odd modes. Close spacing of the conductors or a far away ground plane create the case of a two-wire line with strong coupling between the two conductors. Wide separation of the lines or a close ground plane will remove any coupling and two independent microstrip-lines are present. In the later case tuning the impedance of each line to 50 Ω will create a 100 Ω odd mode impedance and a 25 Ω common impedance. However, the lines are independent and can have significant phase shift between each other, increasing mode conversion. Spacing the lines

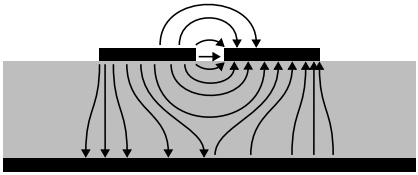


Figure 2.5: Differential microstrip line.

closer together the even-mode impedance can change significantly and phase-deviations between the two lines are minimized.

2.3 Wideband Planar Antennas

The targeted application necessitates wideband antennas with efficient radiation. To qualify the achieved results first the theoretical limits have to be introduced. Antennas are described in terms of their physical size, efficiency, directivity and the bandwidth.
The physical size of an antenna is often non-trivial to determine as all physical elements that significantly interact with the antenna have to be considered. While theoretical assumptions can ignore the physical environment, this simplification cannot be done in modern day complex scenarios such as on-chip or highly integrated on-substrate antennas. Hence, careful analysis of the antenna and interactions in the near field have to be done to accurately estimate the antennas performance. Related to this is the boundary between the near-field, radiating near-field and the far-field as depicted in Fig. 2.6. The near-field describes the reactive region of the fields where interactions directly influence an antennas radiation pattern and hence have to be included in the physical size. The far-field region describes the region where the transmitted energy behaves optically and no influence on the antenna is present. The region in between is the radiating near-field, which for some antennas might not be present at all [Bal16].
The efficiency relates the radiated power P_{rad} to the accepted incident power P_{in} by

$$\eta = \frac{P_{\text{rad}}}{P_{\text{in}}}. \tag{2.20}$$

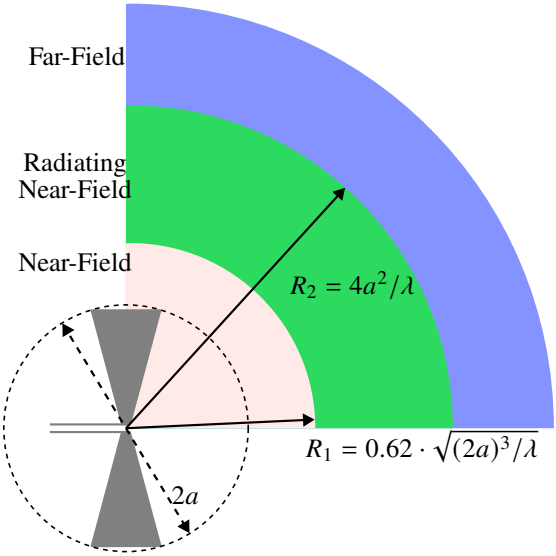


Figure 2.6: Radiating field definitions on an arbitrary antenna with a as the radius of the smallest sphere encompassing the antenna.

Hence, the efficiency quantifies ohmic and dielectric losses in the designed antenna. The directivity describes the relative radiation in a specific direction to the average radiation intensity of the antenna or an equivalent isotropic antenna

$$D = \frac{S}{S_0} = \frac{4\pi S}{P_{\text{rad}}}. \tag{2.21}$$

S is the radiation intensity at a specific point and U_0 the radiation intensity of an isotropic source. The directivity does not include the efficiency of an antenna. Hence practical antennas are quantified by their realized gain which related to the directivity by

$$G_{\text{re}}(\theta, \phi) = \eta \cdot D(\theta, \phi). \tag{2.22}$$

It includes all the losses of the antenna and represents the gain observable in a measurement setup.

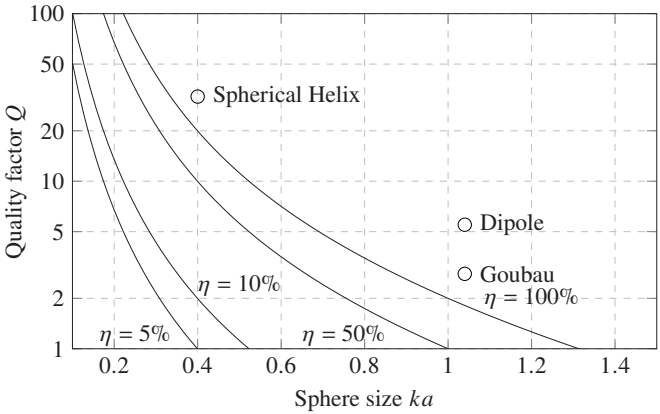


Figure 2.7: Chu-Harrington limit of single-mode antenna radiation [Han81].

The bandwidth of an antenna can be related to either the input return loss or the frequency range where its intended radiation behavior stays nearly the same. With the assumption of high efficiency and consequently low loss the input return loss should indicate radiation and hence offers itself as a valid metric. However, with low efficiency it indicates ohmic losses rather than radiation. Hence, other metrics such as the realized gain are used. This is also true in scenarios where the input match cannot be accurately measured such as directly connected antennas.

Based on these definitions fundamental limits of antennas can be deducted. A first theoretical limit was introduced by the works of Chu [Chu48] and Harrington [Har60] and reviewed by Hansen [Han81] and relates the physical size of an antenna to the achievable quality factors concerning different efficiencies as plotted in Fig. 2.7. The quality factor relates to the bandwidth with

$$BW = \frac{1}{Q}. \tag{2.23}$$

The size of an antenna is measured as the smallest sphere with radius a that encompasses the antenna itself [Han81]. k is the wavenumber. The curves plotted in Fig. 2.7 represent the theoretical lower limit. Further some points

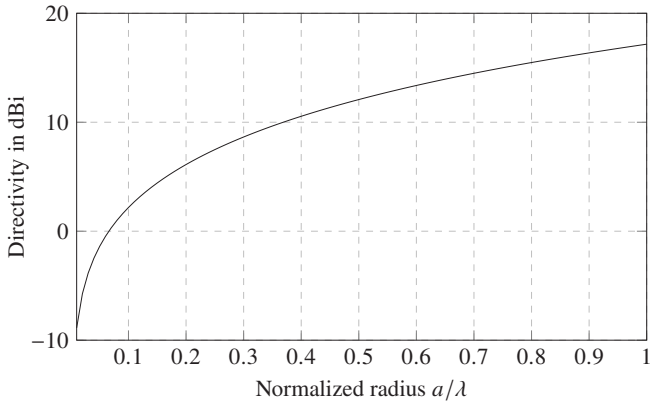


Figure 2.8: Directivity limit over antenna size [Bal16].

for ideal antennas are plotted as reference. The main observation of this plot is that bandwidth of an antenna necessitates a larger structure.

Another fundamental limit is the achievable directivity for a given aperture size plotted in Fig. 2.8. Again it is observable that higher directivity necessitates a larger aperture and hence a larger antenna.

For planar antennas these two limits pose some interesting challenges. Due to inherent limitation of a planar antenna the volumetric efficiency of the engulfing sphere is poor. Any increase in antenna size causes the sphere to increase as well. Hence, concepts have to be followed that utilize the 3D volume better to enhance the performance of the antenna. The second implication of Fig. 2.8 is the maximum gain achievable.

2.4 Planar Phased Arrays

In the previous section, single antenna elements that should provide a large radiation bandwidth with a small physical size were investigated. However, due to the free space path loss (FSPL) at sub-THz frequencies, high gain is necessary to establish robust transmission links over distances above a few meters of range. As Fig. 2.8 shows, the directivity is directly linked to the

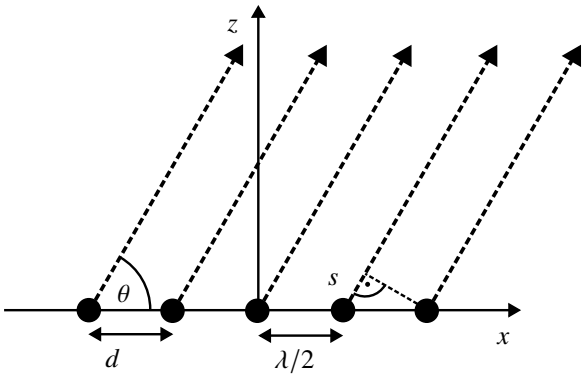


Figure 2.9: Schematic of a phased array.

antenna's physical size. This yields a conflict where, on one hand, a small antenna element is desired, and simultaneously, a large aperture is required.
Another solution to increase an antenna configuration's aperture is placing multiple radiators in a geometrical arrangement called an array. The overall antenna pattern is the vector sum of each element, with the constraint that the elements have to be placed within the near-field regions of each other. Feeding all antennas a correlated signal creates constructive and destructive interference in the near-field zone, shaping the radiation pattern.
Investigating the most straightforward case, a 1D-array of isotropic radiators, a configuration shown in Fig. 2.9 is present. The elements are spaced $\lambda/2$ apart, which is the best case for an antenna array. If each element is fed with the same sinusoid and zero phase shift between each other, the field should be added constructively in z-direction. Introducing a phase-shift between each element, the constructive interference happens at an angle θ. This is a very interesting use case for phased arrays, as it allows us to change the beam direction of such an array electrically. Evidently, from Fig. 2.9, tilting the beam creates a time delay between the individual elements that, for a pure sinus signal, translates to a phase shift. The physical additional length of the individual signals depends on the steering angle θ by $s = d \cdot \cos(\theta)$. The overall radiated field can be

calculated by the field of a single radiating element and a function called the *array factor*

$$\mathrm{AF}(\hat{r}) = \sum_{n=}^{N} a_n e^{jk\hat{r}\cdot\overrightarrow{r_n}}, \tag{2.24}$$

which is a function of the physical location of all radiators $\overrightarrow{r_n}$, their complex excitation a_n and the direction unit vector$\hat{r}$ [Bal16]. The array factor is calculated assuming isotropic radiators and is applied to an arbitrary radiator by multiplication

$$\mathbf{E}_{\text{array}} = \mathbf{E} \times \mathrm{AF}. \tag{2.25}$$

The AF for the linear uniform five-element array shown in Fig. 2.9 is

$$\mathrm{AF} = \sum_{n=1}^{5} e^{j(n-1)(kd\cos\theta+\beta)}, \tag{2.26}$$

with β the phase difference between two adjacent elements.
The increase in directivity of the array depends on the array factor. For the linear array with isotropic radiators with broad-side radiation, the directivity is

$$D_0 \simeq \frac{Nkd}{\pi} = 2N\left(\frac{d}{\lambda}\right). \tag{2.27}$$

While this equation suggests a larger spacing of the elements will increase the directivity, this does not mathematically hold. First, the assumptions to derive the equation assume a spacing well below λ [Bal16]. Next, increasing the spacing also increases the aperture, so an antenna array with more elements spanning the same physical area should be considered for a fair comparison. Effectively, one can assume an N-times increase in directivity for an N-element array.
As evident so far, the spacing of the elements plays a crucial role in the correct operation of the phased array. Spacing above $\lambda/2$ causes increased phase shift between elements and causes additional zeros and maxima. This increases secondary radiation peaks called side lobes, especially for steering. This is often unwanted as it reduces the directivity of the main beam and radiates energy in unwanted directions. Spacings below below $\lambda/2$ increase the coupling between antenna elements. This either necessitates much larger currents in the antennas to achieve the desired pattern or creates radiation in the

x-direction, called end-fire. Contrary, as explained in Sec. 2.3, some antennas cannot be physically smaller than $\lambda/2$ to suffice the spacing requirement. The concepts of the 1D array can be extended to a planar 2D or even a 3D array.
All investigations so far assume a narrow-band signal that a sinusoid can approximate to simplify the mathematical modeling. However, investigating Fig. 2.9, one can deduce that the distance s is the physical distance a signal has to travel. This means that the phase shift has to change with frequency for correct operation over a wider bandwidth. Keeping a constant phase shift, as this is physically easier to implement, an effect called beam-squint happens. This is a change in beam angle over frequency, causing a loss of signal power. To avoid beam-squinting, the signals have to be time-delayed to be able to be overlaid correctly [Bal16].

2.5 Digital Modulation

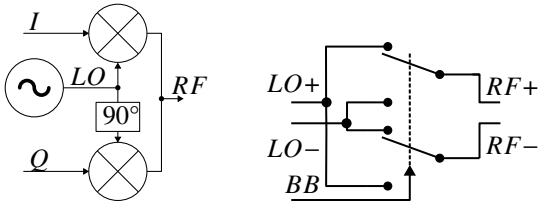
Digital modulation is a process where a digital data stream is encoded onto a carrier signal for transmission over a communication channel. It involves mapping the digital data bits onto variations in one or more characteristics of the carrier signal, such as amplitude, frequency, or phase. The three fundamental digital modulation techniques per [Poz05] are:

1. amplitude shift keying (ASK): In ASK, the amplitude of the carrier signal is varied to represent the binary data. For example, a high amplitude can represent a binary one, while a low amplitude represents a binary zero.

2. frequency shift keying (FSK): In FSK, the frequency of the carrier signal is shifted between discrete values to represent the binary data.

3. phase shift keying (PSK): In PSK, the phase of the carrier signal is varied to represent the binary data. Different phase shifts correspond to different binary values. Common examples include BPSK and quadrature phase shift keying (QPSK).

More advanced digital modulation techniques, such as QAM, combine amplitude and phase modulation to increase the data rate and spectral efficiency.



(a) IQ Modulator (b) BPSK Modulator

Figure 2.10: RF up-conversion circuits.

A differentiation between symbols and bits is done to distinguish the different operating principle of digital modulation compared to binary data representation. Within one time frame one symbol is transmitted, which can encode more than one bit of information. In case of a QPSK this is two bits, a QAM-1024 would encode 10-bit. Hence a mapping of bits to symbols is necessary as a first step in the digital modulation scheme. Next is the modulation of the analog LO signal. This can be done in different ways depending on the targeted modulation and system constraints.

The universal mathematical approach to modulation is the superposition of scaled in-phase(I) and quadrature(Q) components. This is achieved by splitting the LO signal into a direct branch and one 90° shifted signal. Those two components are then multiplied by individual weighting factors and the result summed together. A circuit implementation is shown in Fig. 2.10(a). This approach can generate any form of digital modulation by feeding in the correct amplitudes to the I and Q component. A simpler approach for lower order modulations is the BPSK modulator shown in Fig. 2.10(b). Here the data-signal, called BB, is driving two synchronous switches, which in turn change the polarity of the LO signal. This generates the modulated RF output with a dual-sideband characteristic.

2.6 Power Amplifiers

Amplification is a common task in RF systems, so amplifiers are ubiquitous. Amplifier topologies and approaches are classified by output power, noise

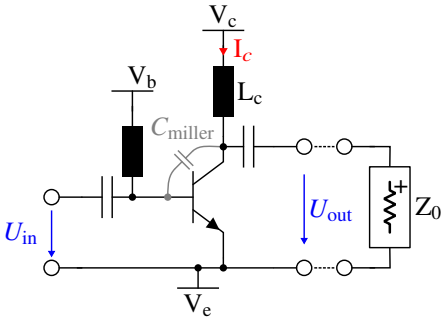


Figure 2.11: Schematic of a SiGe power amplifier.

contribution, bandwidth, or linearity metrics. Power amplifiers, in particular, differentiate themselves by providing the highest output power possible given the operational and technological constraints. In this context, efficiency is also a crucial aspect optimized for PAs as cooling and overall power consumption are important factors. Other constraints limiting the design are bandwidth and linearity constraints [Raz98].

A simple amplifier circuit realized with SiGe heterojunction bipolar transistors (HBTs) is shown in Fig. 2.11. The circuit consists of a common-emitter amplifier circuit with reactive collector loading through the inductor L_c. The input and output are capacitively coupled. A power amplifier aims to provide the largest output voltage swing U_{out} into a load with impedance Z_0. However, it is evident that the transistor output voltage swing is limited by the collector supply voltage V_c and can, with reactive loading, only ever rise to $2 \cdot V_c$. The maximum collector voltage is limited by the breakdown voltage of the transistors, which is a technology-dependent parameter. The current through the transistor can be controlled by the number of transistors in parallel and, hence, can be increased to a certain degree. Consequently, power amplifiers tend to have a very low output impedance as it is easier to increase the collector current to get more power than to increase the collector voltage through stacking. This then necessitates some form of reactive impedance transformer to change the near-short impedance of the PA back to typically $50\,\Omega$ system impedance [Raz98].

The increased power of more transistors in parallel is limited by the input *RC* constant formed by the base-emitter capacitance and the base resistance.

Hence, as frequency increases, the number of parallel transistors decreases for a given technology. Another limiting factor is the matching bandwidth of an input and output matching network. The closer the output tends to a short circuit, that is, very high currents with minimal voltage swing, the more narrowband and lossy a matching network becomes. Hence, proper design has to trade-off losses in the matching networks, transistor sizing and surface area for the matching networks. Another limiting factor is the miller capacitance denoted C_{miller} in Fig. 2.11. It is the intrinsic and parasitic collector-base capacitance and presents a feedback path, causing stability issues. A common approach to reducing the miller-effect is using a cascode, which has another common-base amplifier on top of the common-emitter amplifier, which keeps the voltage on the collector node close to the input signal and limits the coupling effect [Raz98].

To characterize a PA the following metrics are used within this work:

1. **Saturated Output Power**

   The highest output power achieved under single tone stimulus.

2. **Small Signal Bandwidth**

   Defined as the 3 dB bandwidth of S_{21}.

3. **Large Signal Bandwidth**

   Defined as the 3 dB bandwidth of the output power over frequency.

4. **Power Consumption**

   Consumed direct current (DC) power over all circuit parts that are part of the PA.

5. **Efficiency, power added efficiency (PAE)**

   The efficiency relates the delivered RF output power to the consumed DC power. However, low gain amplifier stages tend to also translate a significant amount of input RF power, hence the PAE is used as a metric to include that. PAE is defined as PAE = $\frac{P_L - P_{in}}{P_{DC}}$.

6. **output referred 1 dB compression point (OP1DB)**

1 dB compression point of the single-tone output power, referred to the achieved output power.

7. **Size**

   The physical size of the PA as a metric of spatial efficiency.

8. **Stability**

   Not a direct metric per se, but analyzed to ensure stable operation over all conditions.

2.7 Frequency Staggering

A common issue with increasing data rates is the necessary bandwidth in all components. Improving an amplifier's operating bandwidth is not as straightforward as modifying a matching network, as the Bode-Fano limit puts mathematical bounds to reactive matching and bandwidth [Poz05]. One approach to overcome this limit is the traveling wave approach, which tries to compensate the transistor's input capacitance by cascading multiple transistors with inductive line segments that form a pseudo transmission line. While this approach can achieve extreme bandwidths, it also consumes a large surface area and increases power consumption [Raz98].
Hence, another solution is used in the form of frequency staggering. The basic idea is the superposition of detuned bandpass filter responses of cascaded amplifiers, resulting in a broadband gain. This concept is plotted in Fig. 2.12. The basic bandpass response is assumed as

$$A(\omega) = \frac{A_0}{1 + Q \cdot \left(\frac{\omega_0}{\omega} + \frac{\omega}{\omega_0} \right)}. \tag{2.28}$$

The superposition of correctly tuned responses results in the dashed line in Fig. 2.12 and yields a bandwidth enhancement. It should be noted that the transfer function of a real amplifier is more complicated than assumed in Eq. 2.28. Hence, a realistic design requires more effort to correctly tune the amplitude and phase response to get a correct overlay response. Another limitation comes with non-linearity. While the additivity and homogeneity

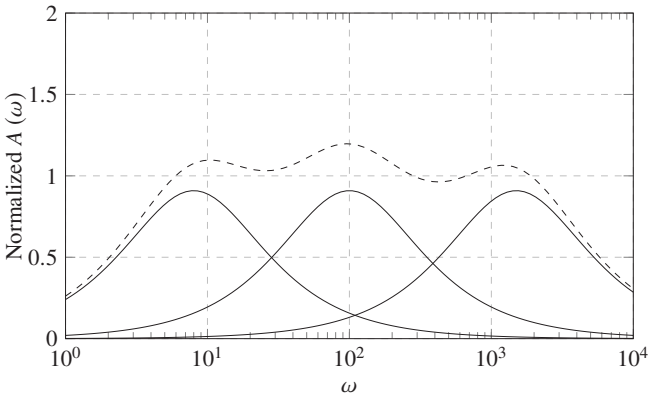


Figure 2.12: Superposition of stagger tuned bandpass filter responses.

under small-signal stimulus are valid, large signal conditions will drastically influence the overall response.

3 System and Implementation Constraints

Figure 1.1 presents an abstract representation of the targeted system architecture. The selected operating frequency range presents both advantages and challenges. The absence of regulatory constraints and frequency allocation allows for flexibility in bandwidth occupation, signal strength and center frequency. However, this lack of external limitations also requires the careful determination of system design parameters.
Tying directly into these considerations is the choice of modulation scheme. Hence in the following section the benefits and downsides of different modulation schemes is discussed and analyzed. Going further, the physical constraints for the phased array antenna are discussed based on a study of the state of the art. Following the interaction between the MMIC and antenna is analyzed. Finally some measurement constraints are presented that are considered for the system conception.

3.1 Choice of Modulation Type

The achievable data rate in an additive white gaussian noise (AWGN) channel is given by the Shannon-Hartley theorem:

$$C = BW \log_2 (1 + SNR) . \tag{3.1}$$

Hence, to increase the data rate either the channel bandwidth or the SNR ratio have to be increased. However, the capacity increase of the SNR is due to using spectrally more efficient modulations, hence has to be seen as a trip point. The overall interaction between these factors is analyzed in [DR24]. Fig. 3.1 shows the theoretical link capacity for a communication link using SiGe transceivers over distance, center frequency f_0, and different modulation schemes. The

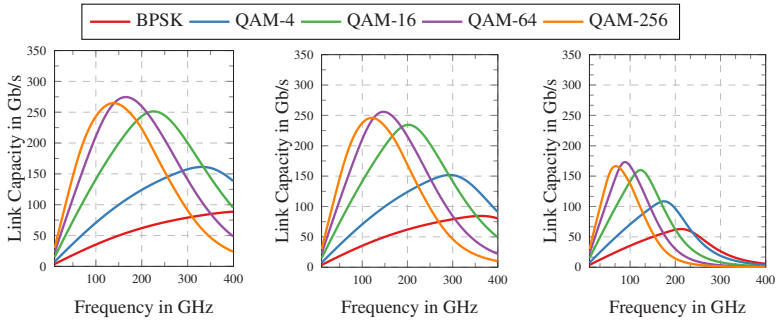


Figure 3.1: Theoretical link capacity for a realistic SiGe link for different modulation schemes over (a) 1 m, (b) 5 m and (c) 10 m, modified from [DR24] © IEEE 2024.

plots are calculated based on [DR24]. One immediate observation is a peak in the link capacity that shifts down in frequency with increasing distance. This results from the frequency-dependent FSPL and shrinking antenna aperture, causing the SNR to decrease while available bandwidth increases.
Another interesting result from this simulation is that lower-order modulation schemes help maximize the available link budget as SNR degrades. This is due to the lower necessary back-off for a PA and better peak-to-average power ratio (PAPR) for the lower order modulation schemes. However, the difference between QAM-4 and BPSK is not as significant as between the higher-order modulation schemes. It also shows the lower spectral efficiency of BPSK, a trade-off for simplicity in the system design. Similar to this is that QAM-256 has a lower peak link capacity than QAM-64. This is again due to the higher linearity requirements of the higher order modulation, which are disadvantageous as frequency and bandwidth increase.
The last observation is that for the system values assumed within the simulation, no 100 Gbit s^{-1} is possible for BPSK. This is, however, an artifact of the assumed relative bandwidth. The used value of 20 % relative bandwidth can be increased in practice [DR24].

3.2 Physical Antenna Array Implementation

Concerning the physical construction of the phased array, we can investigate the survey reported in [WLM24]. Fig. 3.2 shows the reported physical size of the antenna elements within phased arrays in the sub-THz spectrum. The blue line represents $\lambda/2$. One can observe that the physical size of antenna elements stays somewhat constant over frequency, as shown by the green line. This causes a turning point at 100 GHz, where the elements are no longer below the half-wavelength. Another turning point is observable around 300 GHz, shown in the red curve, where antenna elements shrink again. The behavior below 300 GHz can be explained by two factors. Firstly, the available channel bandwidth increases with frequency, and hence, necessary aperture size increases, while the physical size decreases. Secondly, due to fabrication limits of well established technologies a gap in realizable physical sizes is present. Below 100 GHz or 3 mm free space wavelength PCB based structures are viable to create $\lambda/2$ spacing and electrically small elements. Above this frequency structure sizes fall below the currently manufacturable dimensions of standard PCB processes and necessitate special processes and substrates. Simultaneously, the dimensions are to large for monolithic integration within thin-film processes or on-chip structures. Starting at around300 GHz or 1 mm free space wavelength on-chip antennas can be economically integrated within the same MMIC to achieve $\lambda/2$ spacing.
For the system, this indicates that an antenna element size below $\lambda/2$ is a challenge and should not be aimed at. Especially considering the bandwidth target. The target realized gain should be below 10 dBi to stay within antenna size targets and allow broader beam steering.

3.3 MMIC Antenna Co-Design

One part of the system is achieving good performance on the MMIC. An equally crucial aspect is the antenna, especially the integration with the power amplifier. The antenna does not only need to match the bandwidth of the amplifier. It also needs to be placed within an array. For the phased array, antenna spacing and antenna count are critical. This leaves the question of the general approach to the antenna and interconnect to the MMIC and

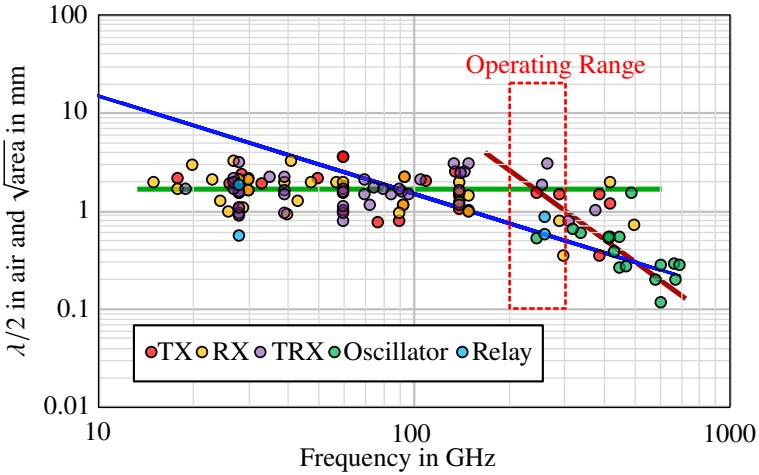


Figure 3.2: Survey of phased array antennas element size and surface area versus frequency as presented in [WLM24].

general structure of the phased array. Based on previously published work, the following potential antenna concepts are possible:

1. On-chip Antenna [LZRR22]
2. Off-chip antenna on thick film substrate [AdGW+22]
3. Waveguide feed [HMK+24]
4. On-chip launcher with reflectarray [WLZ+18]

Evaluating the presented options and the state-of-the-art monolithically integrated on-chip antennas were ruled out. A significant limitation with monolithically integrated on-chip antennas is the lack of measurement opportunities of the underlying MMIC. There is no direct way of evaluating the RF performance of the MMIC and the antenna separately, leaving many aspects unclear. Manufacturing a separate chip to test the antenna and MMIC alone adds costs and does not solve the in-situ test issue.

A waveguide feed is a straightforward way of implementing systems at terahertz frequencies. However, waveguides are only useful in test and measurement scenarios as they lack adaptivity, are costly, and are bulky.
This leaves the decision for off-chip structures connected to the amplifier. Due to the lack of differential measurement equipment, single-ended circuits are preferred. However, employing single-ended connections removes the benefit of the differential amplifier and poses a significant challenge in the interconnect between MMIC and antenna. An alternative that is chosen is a differential wire-bond interface to connect the MMIC and antenna.

3.4 Harmonic Content in the Multiplier Chains

Generating the necessary LO signals at the targeted RF frequencies is still an active field of research. Systems generating the RF tone directly by the use of a fundamental oscillator and stabilized through a phase locked loop (PLL) circuit or injecting locking are rare and have issues with tuning range, output power, and stability [NH20]. Another disadvantage of integrated LO generation is the synchronization for phased array applications. Using a low frequency signal to synchronize PLLs together faces significant challenges for coherence.
Hence, many systems utilize frequency multiplier circuits, which ease these requirements significantly. Based from a strong lower frequency source harmonics are generated in a non-linear device. By tuning and filtering the desired multiple of the input frequency a strong and stable LO tone can be generated.

One issue emerging from the fundamental principle is harmonic suppression. Due to the strong non-linearity of the multiplier, all harmonics are generated with varying strength and will find their way to the output. While the system designed here works around this by choosing a low multiplication factor and a large harmonic spacing, not all parts of the measurement setup have this liberty. The receiving mixer in the measurement setup uses a multiplication of 24 times, causing harmonics to land within the bandwidth of the usable signal. This limits the maximum data rate measurable with this receiver.

Fig. 3.3 shows the result of simulations quantifying this effect. The simulation creates an RF waveform, including the next harmonics of the LO for the upconversion. The downconversion process assumes a mixer converting to an intermeditate frequency (IF) with the LO spaced 30 GHz apart from the RF

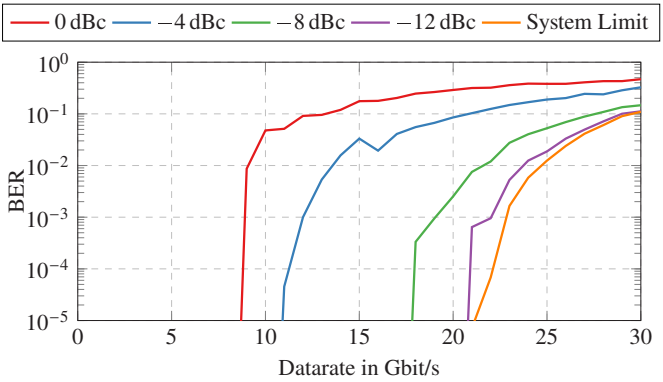


Figure 3.3: Calculated theoretical BER limit due to LO harmonic content from the multiplier chain [5] © IEEE 2024.

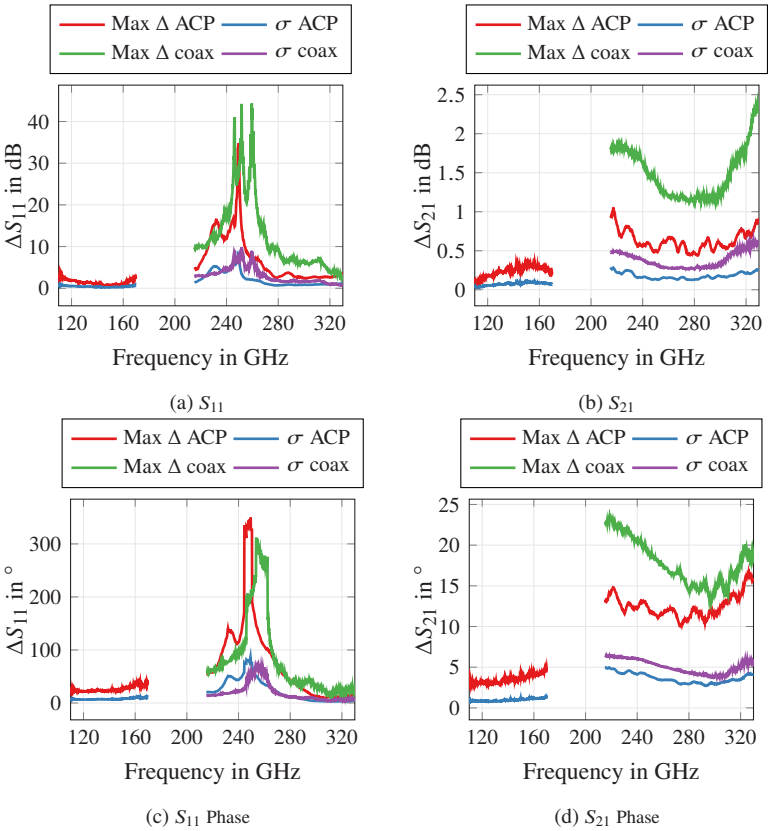
signal. A software receiver then demodulates the IF signal and evaluates the BER. Due to the 30 GHz offset and the chosen demodulation algorithm, a system BER limit is present approaching a modulation bandwidth of 15 GHz, corresponding to a data rate of 30 Gbit s^{-1}, half the IF center frequency. The simulation shows that an average carrier offset of 12 dBc increases the BER over the system limit. Even less suppression leads to significant system limitations with the extreme case of 0 dBc limiting the maximum datarate to be lower than the LO tone spacing. This is also true for the receiving side, limiting the measurement setup used in this work as presented in [2].

3.5 Measurement Uncertainty

The characterization and analysis of various circuits and systems, particularly antennas and transitions, necessitate accurately measured samples. However, inherent limitations in the measurement equipment introduce uncertainty into the acquired data. To quantify this uncertainty, a two-step approach is implemented. First, the repeatability of on-wafer two-port measurements is evaluated. Subsequently, an investigation into the radiation characteristics of the utilized probes is conducted.

3.5.1 On Wafer Measurement Repeatability

An issue due to the small wavelength is the repeatability of on-wafer probing. Comparably small absolute deviations in the position on the probe pad influence the coupling into the MMIC. This effect is present even in best-case scenarios and is amplified by the fact that most measurements done within this work are done on individual samples. Each device has to be probed separately, causing changes in the alignment of the probe to the pad in translation and rotation.
A silicon wafer with thru lines is measured over multiple fields to evaluate this uncertainty over frequency. This is done in two nonoverlapping bands from 110 GHz to 330 GHz. 8 samples are measured within the D-band, and 16 samples are measured for two types of probes within the H-band; One air co-planar (ACP) style probe shown in Fig. 3.5(b) and one coax probe with 50 µm pitch shown in Fig. 3.5(a) From all these measurements, the deviation between the measurements is calculated. One metric is the absolute difference between the two measurements that are the furthest apart, and the other metric is the standard deviation over frequency. The results are plotted in Fig. 3.4 with the coax-style probe plotted in dashed lines.
At D-band frequencies, the uncertainty in transmission is at maximum 0.3 dB and on average better than 0.1 dB with a maximum of 4° and 1° standard phase deviation. In reflection, these values are worse, which is expected due to the smaller values. The amplitude has a maximum deviation of 2.8 dB and a standard deviation of better than 0.9 dB. The phase deviates more with a maximum of 38° and a standard deviation of better than 12°.
Going to H-band, the deviation becomes significantly worse. The ACP style probe achieves a standard deviation in the transmission of 0.25 dB and is better than 5°. The coax style probe is significantly worse with a standard deviation in transmission of 0.3 dB to 0.5 dB and a phase uncertainty of better than 7°. Looking at the maximum deviations, the discrepancy becomes even wider.
The worst case is, however, the input match, where significant deviations over the frequency band are consistently higher than the ACP style probes. This is partly because the coax-style probes radiate energy, causing unwanted coupling and interaction with the DUT [7].



(a) S_{11} (b) S_{21}

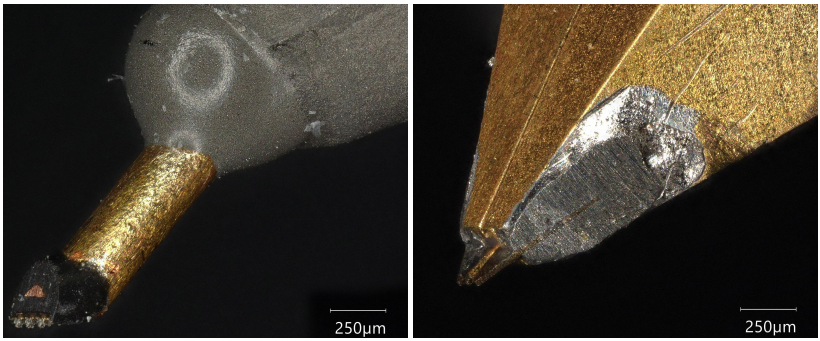
(c) S_{11} Phase (d) S_{21} Phase

Figure 3.4: Measured Phase and Magnitude of S_{21} over 8 thru line samples which are individually probed.

3.5.2 mmWave Probe Radiation Behaviour

On-wafer probes are ubiquitous in evaluating high-frequency circuits, as expensive connectors or waveguide transitions can be omitted. However, these probes are not free of side effects, and radiation being one of them. Previous works investigated the radiation behavior of probes at lower frequencies below 67 GHz [YWS+21], [ZZ22], [LRJ+18], [RvDSH15]. No measurements were presented within the mmWave regime except those done within this work and presented in [7]. To evaluate the radiation, different probes are mounted in the center of a spherical free space antenna measurement system [BZ10]. The receiver is rotated around the probes, and the radiation in the E-plane and H-plane is captured. In total, nine distinct probes are measured in two different styles. One is a coax cable terminated with a small polyimide film that contains a transition from coax to microstrip to a ground signal ground (GSG) interface with probe tips shown in Fig. 3.5(a). These style of probes are available in 100 µm and 50 µm pitch. The other style is the ACP type shown in Fig. 3.5(b). This probe has a transition from coax to an air-coplanar type CPW structure.

Table 3.1 lists the used probes, their alias, the pitch, and the manufacturing year. Three of each type of probe are measured.
Fig. 3.6 and Fig. 3.7 compare the radiation of the ACP and coax probes across



(a) Coax Probe (b) ACP Probe

Figure 3.5: Micrograph of the used RF probes. 3.5(a) shows the coax probe with the micro coax going to the probe tip. 3.5(b) shows the ACP probe with the CPW forming the probe tip. From [7] under CC-BY.

Table 3.1: Used probes and their designation

Designation	Type	Pitch	Year
C1 50 µm	Micro-Coax	50 µm	2021
C2 50 µm	Micro-Coax	50 µm	2021
C3 50 µm	Micro-Coax	50 µm	2023
C4 100 µm	Micro-Coax	100 µm	2022
C5 100 µm	Micro-Coax	100 µm	2022
C6 100 µm	Micro-Coax	100 µm	2023
ACP 1	ACP	80 µm	2016
ACP 2	ACP	80 µm	2014
ACP 3	ACP	80 µm	2014

the E-plane. Evidently, the coax probes have significant radiation to the 0° and 180° achieving almost 0 dBi. The ACP probes have maximum of −13 dBi. Comparing the radiation across the H-plane in Fig. 3.8 and Fig. 3.9, this trend continues. Here the coax probes reach 0 dBi in the −30° direction. The ACP probes stay below −13 dBi. Investigating the radiation at boresight, that is 0°, over frequency in Fig. 3.10, the coax probes show an increase in radiation with frequency exceeding 0 dBi above 290 GHz. The ACP probes stay rather constant below −13 dB. Another interesting aspect is the large variation in the measurement results of the coax probes. Fig. 3.10(a) shows a variation of more than 12 dB between the worst and best case, which does not correlate to any specific probe kind.

These measurements with the probe in air are one extreme case, which is not the typical use case. Therefore, a short, open, and load standard on an impedance standard substrate (ISS) are measured to investigate the behavior while contacting a DUT. This is only done for the coax-style probes as the ACP-style probes have considerably lower radiation. The results are plotted in Fig. 3.11. Both open scenarios with the probe in the air compared to the open standard on the ISS behave quite similarly with some attenuation through the substrate. Interestingly, the lowest radiation is achieved by contacting a shorting bar instead of the 50 Ω termination. This hints at the possible mechanic of ground currents running on the outside of the coax body.

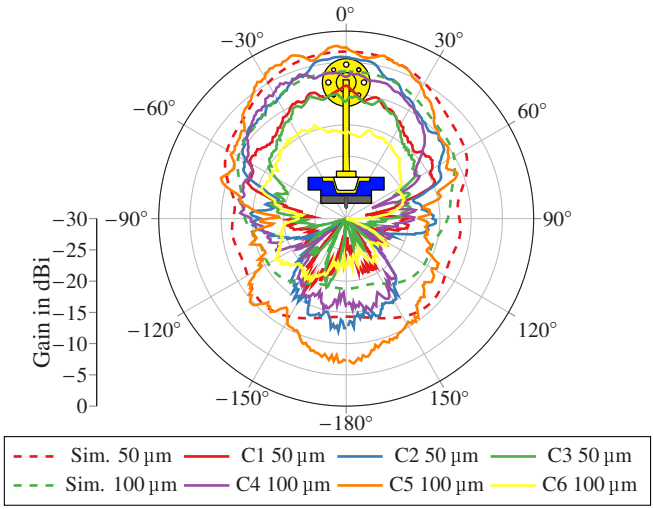


Figure 3.6: E-Plane radiation measurement at 280 GHz of the tested coax probes open in air. In dashed lines are the simulation results for 50 µm and 100 µm pitch. From [7] under CC-BY.

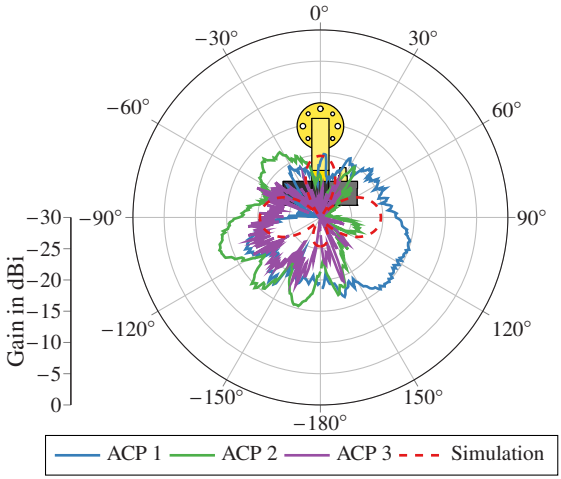


Figure 3.7: Measured E-plane radiation behavior at 280 GHz of the tested ACP probes open in air. In dashed lines is the simulation. From [7] under CC-BY.

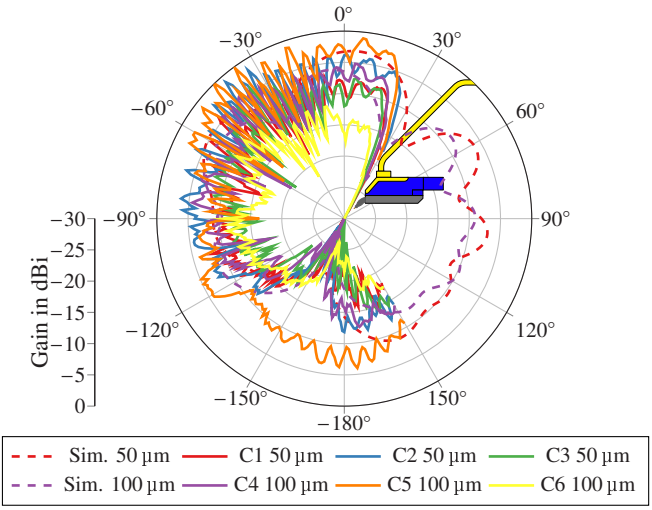


Figure 3.8: H-Plane radiation measurement at 280 GHz of the tested coax probes open in air. In dashed lines are the simulation results for 50 µm and 100 µm pitch. From [7] under CC-BY.

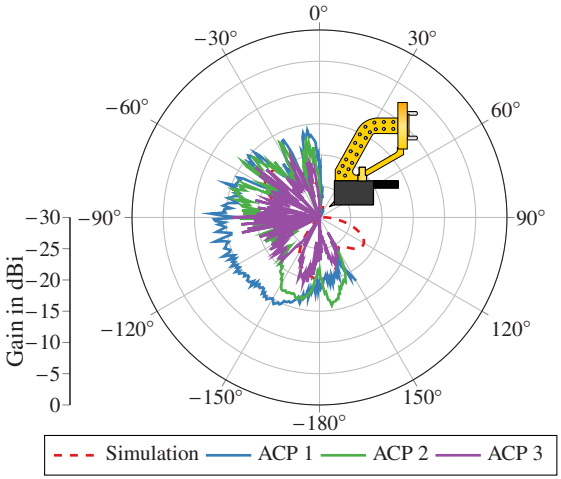
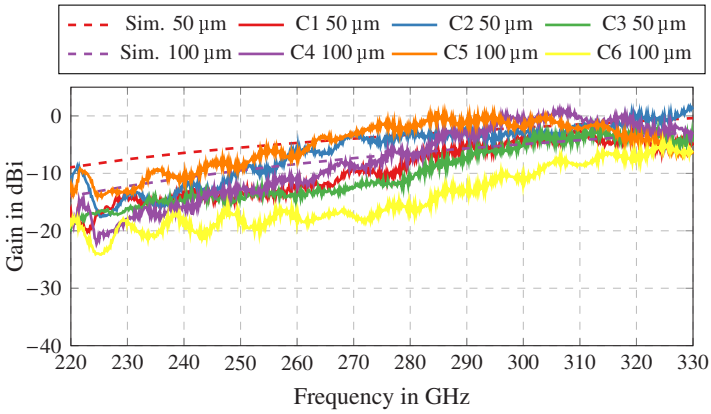
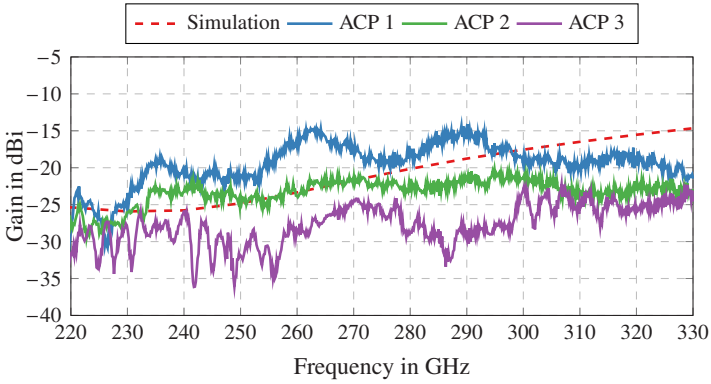


Figure 3.9: Measured H-plane radiation behaviour at 280 GHz of the tested ACP probes open in air. In dashed lines is the simulation. From [7] under CC-BY.



(a) Coax probes



(b) ACP

Figure 3.10: Measured radiation at boresight over frequency. The dashed lines show the simulation results for the 50 µm and 100 µm coax probes in 3.10(a) and for the ACP probe in 3.10(b). From [7] under CC-BY.

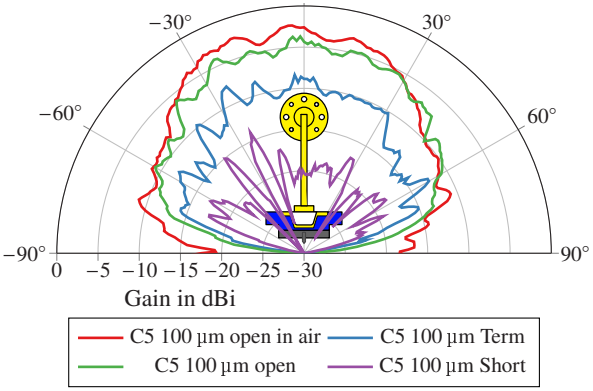


Figure 3.11: Measured pattern with C5 100 µm contacting open, short and load standards on an ISS at 280 GHz. From [7] under CC-BY.

These measurements show that the coax probes can have a significant influence due to radiation onto measurements, which has to be considered especially for structures containing $\lambda/2$ sized elements such as antennas or baluns. Using ACP probes to avoid these issues is advisable. However, the tested ACP construction style has issues with robustness due to very limited allowable conformity of the probe tips. Also the compact design is problematic for antenna measurements due to strong reflections at the probe body.

4 Power Amplifier Design and Evaluation

The power amplifier is a fundamental part of the proposed system and directly influences the overall performance. The bandwidth and achieved output power directly influence the maximum achievable distance and data rate. But output power is not the only important aspect. Broadband operation and linearity are just as essential as high power amplifier back-off (PBO) negates any higher saturated output power benefit. This chapter describes the considerations and design of the employed power amplifier. First, a detailed overview of the state of the art is given to justify the topological and technological choices. Further, as the selected technology is offered in two different metal back-ends, both back-end of line (BEOL) stacks are compared against each other to choose the optimal option for the desired application at 246 GHz center frequency. Next, the design of the power amplifier is described and evaluated based on simulation and measurement results where possible. Design details are highlighted and presented. The final design is shown and evaluated in detail using stimulative and measurement results where possible. Some final considerations about the test and measurement of these amplifiers are highlighted.

4.1 State of the art in PA MMICs

Many different topologies for RF PA design have been published in the literature. However, as operating frequency increases, these solutions become infeasible as component losses increase and matching structures are no longer well below the wavelength. Further, the available P_{sat} decreases with increasing frequency due to the Johnson Limit [Joh65], evidently present in the survey shown in Fig. 4.1 which is presented in [WCA+24]. This is due to the superposition of base input RC limitations, electron drift velocity, and frequency-dependent losses. This effect also limits the theoretically achiev-

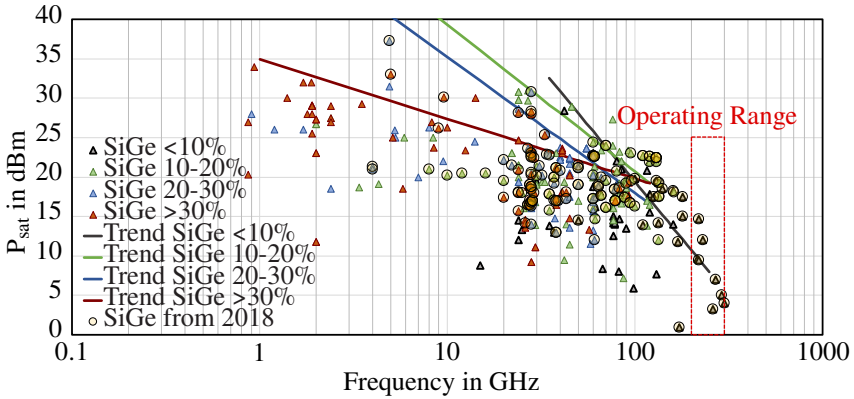


Figure 4.1: Survey of power amplifier as presented in [WCA+24]. Plotted is the saturated output power over frequency for SiGe power amplifiers. The plot is grouped by the respective reported PAE in four groups from below 10 % to above 30 %.

able PAE and amplifier operating class [BRN+21]. The survey concludes that an output power above 10 dBm is not practically achievable if simultaneous wideband operation and high PAE are desired.

Tab. 4.1 present the state-of-the-art in PA circuits operating above 200 GHz, which gives some interesting insights. Firstly, very few publications are based on CMOS. While [YPL23] presents a very competitive design in terms of P_{sat}, the achieved bandwidth is insufficient for the targeted application here. The only other published approach presented in [Mom13] achieves low output power.

On the other hand, designs based on III-V semiconductors achieve higher saturated output power and very competitive bandwidths compared to SiGe. However, they need large chip areas and higher power to achieve this. Also, the lack of a natural oxide or passivation layer typically limits the number of metal layers. This leaves SiGe as the technology of choice for systems in the H-band, offering competitive output power, bandwidth, and optimal integration density.

Investigating the published SiGe amplifiers reveals the prevalence of differential cascode topologies. The cascode improves the common-emitter circuit by adding another common base stage, minimizing the miller capacitance. This capacitance is a significant limitation at sub-THz frequencies, so this topology is convenient. Further, utilizing a differential circuit improves the output power by 3 dB while easing the DC routing, as the RF currents cancel out at

the common nodes for class-A and class-AB designs. This improves stability and minimizes the risk of oscillation when assembled. The additional output power comes at the cost of twice the power consumption of transistor devices and is a form of power combining. Thus, all amplifiers in SiGe presented in Tab. 4.1 use a pseudo-differential approach. In the context of a PA, fully differential stages are not used, as the tail current source presents itself as a capacitance, introducing a complex, frequency-dependent impedance at the common ground. This negates all common-mode suppression effects from the tail current source without contributing RF power or small-signal gain while increasing DC power consumption [16]. However, it is still possible to achieve sufficient common-mode suppression by utilizing different techniques [16].

Another aspect of the presented SiGe designs is the prevalence of multi-stage designs with at least 3-stages. While the last stage dominates the output power, the number of stages increases the gain and helps in broadband operation. A widespread technique is frequency staggering, where the frequency response of each stage is shifted to broaden the overall response. Here, each additional stage helps improve the frequency of response.

Due to availability, cost, and performance, only three candidates are interested in all the available SiGe technologies. *IHPs SG13G2*, *Infineons* BF11HFC and *STs 90nm BiCMOS*. However, only the first technology is available in small numbers through *Europractice*, offering the highest performance [SBd+16]. Hence *IHP* technology will be used for all designs.

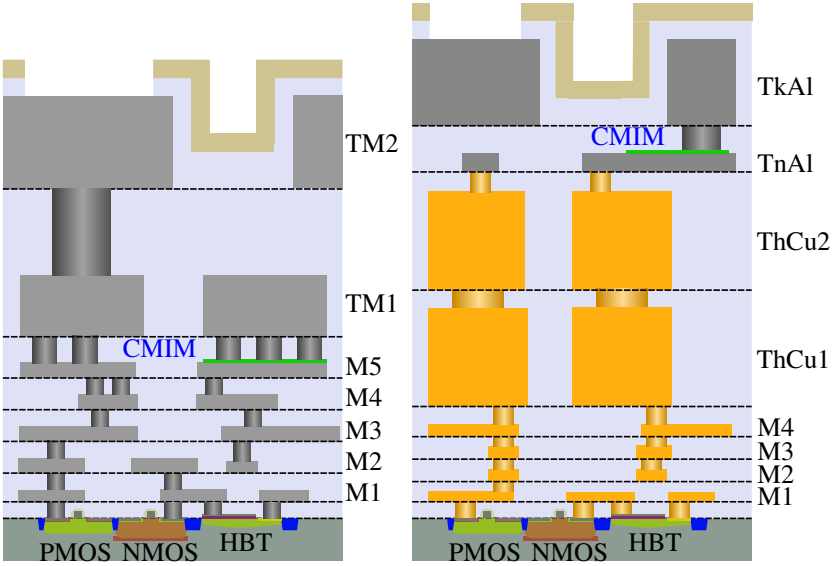
4.2 Technology Overview

The SiGe technology offered by *IHP* has two different metal stack options. Both options are drawn to scale in Fig. 4.2. One uses seven aluminum layers with five thin and two thick layers. The other offers four thin and two thick copper layers and one thin and one thick aluminum layer on top and an additional capacitor with metal isolation metal layer (CMIM) option. The higher conductivity of copper, which is about 1.5 times that of aluminum, makes the copper BEOL an obvious choice, especially for PA applications where the emitter current density is highest. Another direct advantage is the lower vertical interconnect access (VIA) resistivity, which is only a tenth of that in the aluminum back-end. Considering only the ohmic losses, a significant

Table 4.1: State-of-the-art in H-Band Power Amplifiers.

Ref.	Technology	Topology	N.S	Gain	P_{sat}	PAE	Center Frequency	Bandwidth	Power	Area
[YPL23]	65 nm CMOS	Single Ended CS, 4-Way Combining	6	28 dB	10.5 dBm	2.7 %	243 GHz	7 GHz	407 mW	0.909 mm^2
[YPL23]	65 nm CMOS	Single Ended CS, 2-Way Combining	6	26 dB	9.2 dBm	3.9 %	245 GHz	5.2 GHz	217 mW	0.444 mm^2
[Mom13]	65 nm CMOS	Single Ended CS	4	9.2 dB	−3.9 dBm	1.35 %	257 GHz	12.2 GHz	28 mW	0.144 mm^2
[ASS+21]	250 nm InP	4-Way Power Combining	4	20.5 dB	16.8 dBm	4 %	257 GHz	48 GHz	1090 mW	0.832 mm^2
[GUR17]	250 nm InP	Cascode, 16 Way Power Combined	3	24 dB	20.6 dBm	4.1 %	228 GHz	68 GHz	-	3.380 mm^2
[JTL+20]	35 nm InGaAs	SE Cascode + SE CS	5	22 dB	13.7 dBm	2.4 %	304 GHz	48 GHz	-	0.385 mm^2
[BGH+21]	SG13G3	Diff cascode, Coupler	3	20 dB	6.7 dBm	0.92 %	268.5 GHz	59 GHz	417 mW	0.068 mm^2
[BGH+22]	SG13G3	Diff cascode, Coupler	3	20 dB	9.7 dBm	1.95 %	270.5 GHz	63 GHz	360 mW	0.260 mm^2
[LCH+20]	SG13G2	Diff cascode, Transformer	3	21.5 dB	0 dBm	0.3 %	252.5 GHz	11 GHz	149 mW	0.090 mm^2
[EMK19]	SG13G2	Diff cascode, 4 Way Combiner	3	12.5 dB	12 dBm	1 %	227.5 GHz	55 GHz	740 mW	0.830 mm^2
[LCL+21]	SG13G2	Diff cascode, TL matching	3	22.5 dB	9.5 dBm	1.6 %	221.5 GHz	35 GHz	245 mW	0.067 mm^2
[ZCL+23]	130nm SiGe	Diff cascode, 2 Way Combiner	4	21.4 dB	12.5 dBm	2.6 %	259 GHz	33 GHz	653 mW	0.175 mm^2
[GZGO23]	SG13G2	Diff cascode, 4 Way Combining	4	13.5 dB	7.5 dBm	0.39 %	290 GHz	13 GHz	1008 mW	0.490 mm^2
[LCZ+22]	130nm SiGe	Diff cascode, 4 Way Combining	4	15 dB	5 dBm	1.19 %	280.5 GHz	67 GHz	268 mW	0.059 mm^2
This	SG13G2	SE cascode, Lumped Matching	2	10 dB	-	-	230 GHz	50 GHz	-	0.059 mm^2
This [17]	SG13G2	Diff cascode, Transformer	3	24.3 dB	7.4 dBm*	0.38 %	242.5 GHz	29 GHz	435 mW	0.041 mm^2
This [17]	SG13G2Cu	Diff cascode, Transformer	2	26.4 dB	6.9 dBm*	1.13 %	234.5 GHz	17 GHz	259 mW	0.047 mm^2
This	SG13G2	Diff cascode, Transformer	3	19 dB*°	8 dBm*°	2.7 %	254 GHz*°	74 GHz*°	252 mW	0.045 mm^2

*Simulation, ° verified in system



(a) Al BEOL (b) Cu BEOL

Figure 4.2: To scale comparison of the two investigated BEOL options.

enhancement in RF design should be possible within the copper back-end. However, this simple consideration neglects substrate losses, transmission line limitations, and constraints due to design rules. To evaluate this, several investigations were conducted using simulations to quantify the differences between the two stack-ups.

4.2.1 Transmission Lines

To compare both stack-ups, 1 mm of 50 Ω microstrip line is simulated for different layer combinations, which might be used in practical systems. Due to the changing distance between the signal conductor and the ground plane, the signal conductor width is changing as given with the results in Tab. 4.2. Line 1 is used as a reference for comparison, as it is a commonly used line for the *SG13G2* stackup. Using M3 as a ground plane allows for shielded DC routing

Table 4.2: Losses for 1 mm of 50 Ω transmission line for different configurations at 245 GHz in both metal stack-ups from [17].

Nr.	BEOL	Metals	Signal width	Loss per mm
Ref.	Al	TM2-M3	12 µm	0.894 dB
2	Al	TM2-M1	15 µm	0.712 dB
3	Cu	ThCu2-M3	5.9 µm	1 dB
4	Cu	ThCu2-M1	8.3 µm	0.786 dB
5	Cu	ThCu1-M1	2.4 µm	1.7 dB
6	Cu	TkAl-M3	15.7 µm	0.65 dB
7	Cu	TkAl-M1	18.4 µm	0.565 dB

underneath the microstrip line without discontinuities.
In the copper backend different configurations are analyzed. Line 3 and 4 show the upper thick copper layer in both versions with the ground plane. Line 5 shows the case with the lower thick copper layer. The last two lines show the results for using the upper thick aluminum layer.
Using only the copper layers, line 4 shows the lowest losses. However, there only a small improvement of 0.108 dB over the reference is achieved. This is due to the close proximity of the signal conductor to the ground plane, limiting the signal conductor's size and negating any improvement due to the better conductivity. Conversely, an improvement can be achieved by using the topmost aluminum layer in *SG13G2Cu*, where in a best-case scenario, line 7, an improvement of 0.329 dB is achieved. While this is significant, some auxiliary factors must be considered. Due to the high position in the BEOL additional losses for the connection to transistors and capacitors are present.

4.2.2 Transformers

PA designs employ differential circuits and transformer coupling to enhance their performance. Two equally sized transformers are simulated in both back-ends to evaluate the possible gain due to the copper coils' lower loss. In the aluminum back-end, metals TM1 and M4 and M5 together are used to form the coils [QAU19] while ThCu1 and ThCu2 are used in the copper back-end.

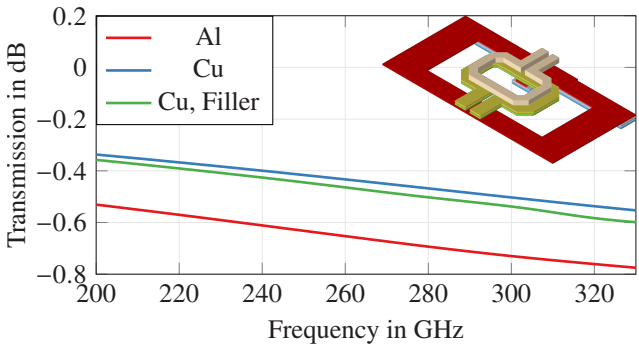
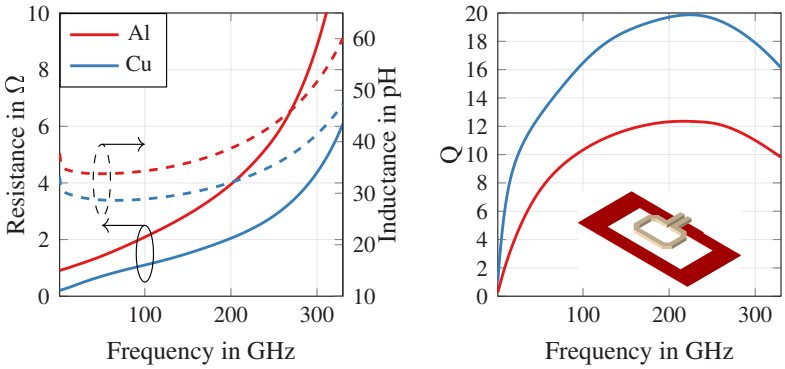


Figure 4.3: The transmission loss in equally sized transformers in both back-ends over frequency in the targeted range. In the upper right corner is the layout of the aluminum back-end shown [17] © IEEE 2022.

The coils are 15 µm wide and 30 µm long, and due to the physical geometry, they should have similar inductance and coupling. The layout of the aluminum process, as well as the losses simulated for both processes, are shown in Fig. 4.3. The loss is calculated from the S-parameters as

$$loss = 1 - \left(|S_{11}|^2 + |S_{21}|^2\right). \tag{4.1}$$

As expected, the loss in the transformer utilizing the copper is lower, but only by 0.25 dB or a factor of 1.06. This is partly due to the substrate losses that affect both transformers roughly equally. A limitation from the copper design rule check (DRC) rules for the metal density forces the transformer to have filler cells on TnAl. Including these in the simulation, the loss increases by another 0.025 dB. This evaluation ignores resulting self-inductance, coupling factor, or parasitic capacitances, causing the transformer to change more severely depending on the application. Therefore, the significance of this singular investigation is limited. To alleviate this, the upper coil of the transformers is simulated, and resistance, inductance, and Q-factor are extracted. The results are shown in Fig. 4.4. The copper stack-up has half the resistance compared to the aluminum back-end due to the higher skin depth of copper. However, the inductance is lower due to the larger metal cross-section, which is 6 pH. The quality factor has a peak of 20 for the copper back-end, while in aluminum, it



(a) Resistance and Inductance

(b) Quality Factor

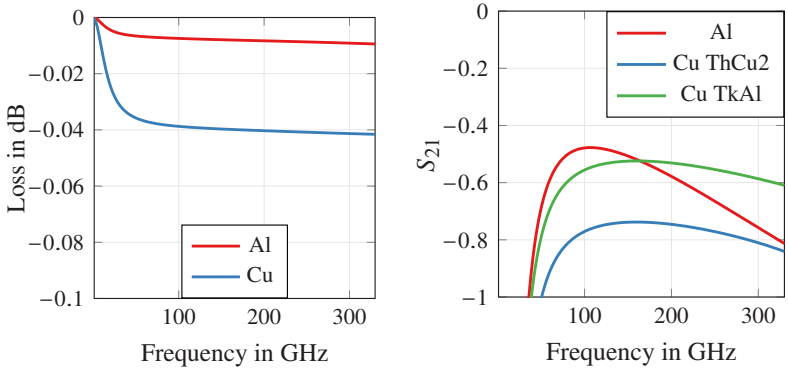
Figure 4.4: Simulation of equal transformer coil's resistance, inductance and quality factor both investigated BEOL options [17] © IEEE 2022.

is 12. Extracting the full model parameters is omitted to simplify the evaluation.

4.2.3 Capacitors

The capacitor, a crucial and intricate component in RF design, has a variety of realization methods. In the case of CMOS, we encounter metal oxide semiconductor (MOS)-capacitances that utilize the gate to drain and source capacitance of a transistor, the capacitor with metal oxide metal layer (CMOM) between two adjacent metal parts, or a unique isolation layer that creates a CMIM. Both BEOL stackups offer a CMIM, a design that warrants detailed analysis.

Practically, the copper back-end, despite its superior specific area capacitance, faces a challenging position within the metal stack, as depicted in Fig. 4.2. It is situated high in the stack-up, between the thin and thick aluminum layers, and is inaccessible directly from underneath by a VIA connection for manufacturing reasons. In contrast, the capacitor in the aluminum back-end is closer to the substrate and can be accessed directly from underneath. This real-world positioning has significant implications on the performance, as demonstrated



(a) Capactitor Loss

(b) AC Thru Loss

Figure 4.5: Losses through a 100 fF capacitor in a (a) direct scenario and (b) as a DC-block capacitor within a transmission line for both BEOL options [17] © IEEE 2022.

by simulating a 100 femtofarad capacitor in both BEOL configurations using *ADS Momentum*. The simulation results are illustrated in Fig. 4.5(a).

Furthermore, to evaluate real-world implications, an alternating current (AC) coupling structure within a transmission line with the same capacitance is simulated, and insertion loss is analyzed. For the copper back-end, simulations are conducted for transmission lines employing ThCu2 and TkAl. The outcomes are presented in Fig. 4.5(b). The CMIM in copper exhibits a 3% higher loss due to the connection through the thin aluminum layer. While higher area capacitance is generally advantageous, it reduces available metal cross-section, thereby increasing losses. Another issue with applications at sub-THz frequencies is that the necessary smaller capacitance cannot be realized reliably with the CMIM. The smaller the capacitor, the more severe the manufacturing tolerances, limiting the usefulness of the higher specific area capacitance.

In the case of transmission line AC coupling, the metal stack-up placement also presents challenges. When the signal conductor is in the uppermost aluminum layer, the loss is comparable to or better than the reference in the aluminum back-end. However, in scenarios where the signal conductor is in ThCu2, the loss is elevated by up to 0.3 dB.

4.2.4 Technology Selection

Analyzing the results of the aforementioned simulations yield no significant benefit of the copper BEOL over the aluminum one. Further, there are some practical aspects that speak for the aluminum back-end as well. Firstly, the DRC rules for the copper back-end are disadvantageous for RF designs. There are stricter rules for metal free zones limiting the actual size and forcing more parasitic metal withing transformers and other RF structures. Further, the minimum and maximum metal density rules force openings in metal connections increasing the resistance. Secondly, an additional hatching to all thin metals is applied, causing hard to simulate effects in the RF design [16].
Concluding, the aluminum back-end is used for the final amplifier and system design. For completeness of the comparison Sec. 4.4.2 compares two amplifiers in both technologies.

4.3 Single Ended Amplifier Evaluation

While the state of the art is dominated by differential designs, a single-ended design might have advantages: Reducing the simulative effort and easing analysis might lead to an improved design. The maximum possible output power without combining will be lower by 3 dB compared to a differential design. However, this effect is reduced if necessary output balun losses are considered for the measurement and usage of the differential PA. Hence, a single-ended PA is designed and measured to evaluate possible merits. The schematic of the designed amplifier is shown in Fig. 4.6. It features a two stage design with quasi lumped element matching. Both stages use a single-ended cascode with times four transistor multiplier. The input matching is a multipole network with a series C, L, and C and a shunt series LC to enhance the bandwidth of the input matching. The collector current is fed through a collector inductor. The interstage matching is realized again as a multipole network with a series LLC network and a shunt capacitor. The output matching is achieved by a series C-L-L-L network with two shunt-series LC networks. The layout of the cascode cores is identical.

The realized chip is shown in Fig. 4.7. The core measures 330 µm by 180 µm. The feeding line is a weakly coupled GCPW line where the ground walls

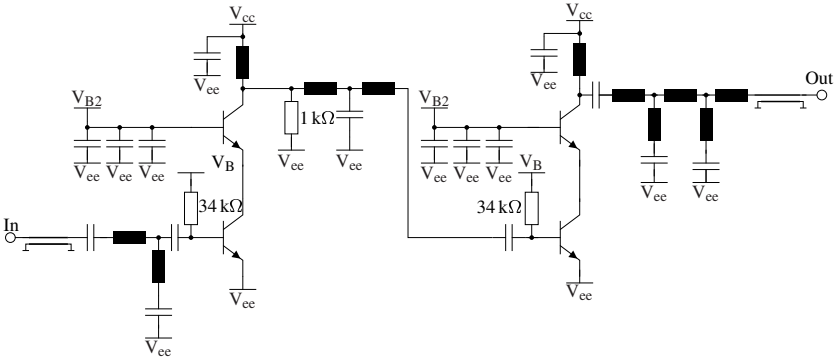


Figure 4.6: Schematic of the single ended amplifier.

and plane extend directly into the RF amplifier to ensure proper shielding. The matching components are implemented as quasi-lumped elements, using sections of thin lines that are short enough to ensure proper lumped element modeling. This improves the quality factor of the matching sections.

The amplifier is measured on-wafer with a probe station, a *Keysight PNA-X*, and *OML V03VNA2* frequency extension modules. The DC is fed from a *NI SMU* to on-wafer DC-probes. The measured S-parameter is shown in Fig. 4.8. The measured small signal gain is higher than the simulation anticipated, which improves the bandwidth from 205 GHz to 255 GHz. The gain is about 10 dB. The input match is better than −10 dB from 200 GHz to 250 GHz. Interestingly, the input match in simulation tends to go to 0 dB above 290 GHz while the measurement shows an improvement in match. The output matching does not fit the simulation and shows better than −10 dB from 205 GHz to 262 GHz. This might indicate either a transistor modeling issue or, more severe, an instability issue.

A main limitation in single-ended amplifier design proved to be the layout. Due to the inherent asymmetry with the matching networks, great care has to be taken to ensure no frequency-dependent layout issues are present. Further, no transformers or couplers can be used to interconnect the stages, forcing a design with many lumped elements that need to be designed and verified. Especially the DC feed through the inductor is very sensitive to the physical layout and suffers from coupling into the base biasing paths. This leads to the

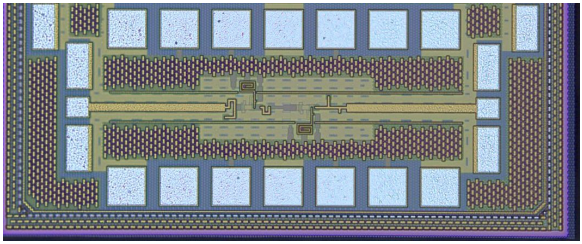


Figure 4.7: Micrograph of the manufactured single ended amplifier.

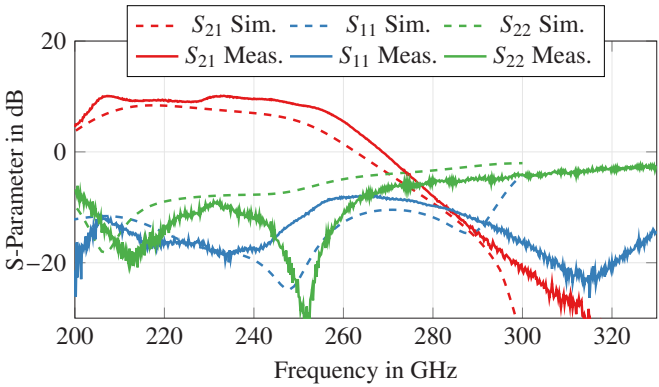


Figure 4.8: Measured and simulated S-parameter of the single ended amplifier.

conclusion that a single-ended amplifier does not offer any benefit in stimulative assessment or performance.

4.4 Differential Amplifier Design

The crucial concept about a differential amplifier opposed to the single-ended architecture is the opposing currents in the two signal lines and, consequently, the cancellation of any RF signal on any common node. To achieve these two properties, great care has to be taken to ensure proper symmetry in the circuit and proper differential operation. Another important benefit is the utilization

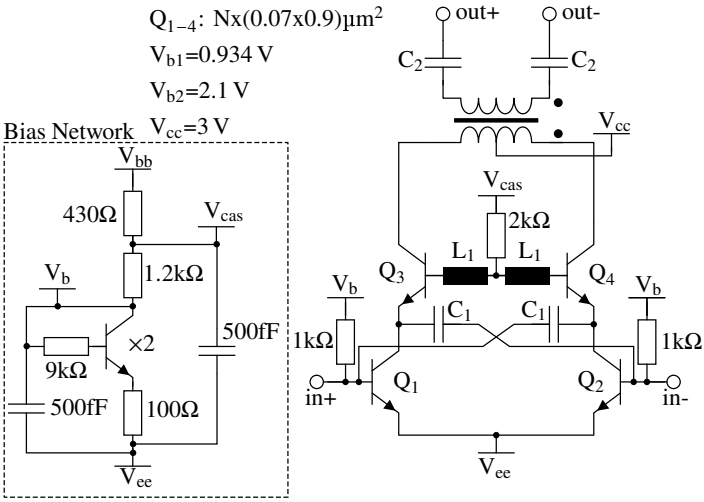


Figure 4.9: Schematic of the differential cascode core with all possible tuning elements [17] © IEEE 2022.

of transformers for easy AC coupling and differential feedback, which can be utilized to minimize miller capacitance and create certain filter characteristics.

4.4.1 Core Design

The core of the amplifier is a differential cascode stage. The schematic is shown in Fig. 4.9. A diode-connected transistor and resistive voltage divider generate the bias voltages for the core. The diode-connected transistor ensures the base voltage for the lower transistors is always dependent on the collector current of the diode and, therefore, compensates for manufacturing tolerances and heat-dependent effects. The base voltage for the upper transistor is generated by a voltage divider, ensuring a similar ratio when changing V_{bb}. The bias network is replicated on both core sides to ensure symmetric loading. All bias voltages are buffered by 500 fF CMIM capacitors. The core itself has no tail transistor. The output to the next stage is coupled through a transformer. To ensure some common-mode suppression and prevent common-mode instability, only a single center tap on the transformer is present [16], [FR15].

The first tuning parameter to improve the gain and frequency behavior of the stage is the output transformer itself. Its self-inductance, paired with the collector-emitter capacitance, has a self-resonance frequency that can be tuned to create frequency staggering. The next option are the capacitors C_2 on the transformer output to the next stage. Together with the transistor input capacitance of the proceeding stage, they form a capacitive divider, helping in tuning the frequency response.

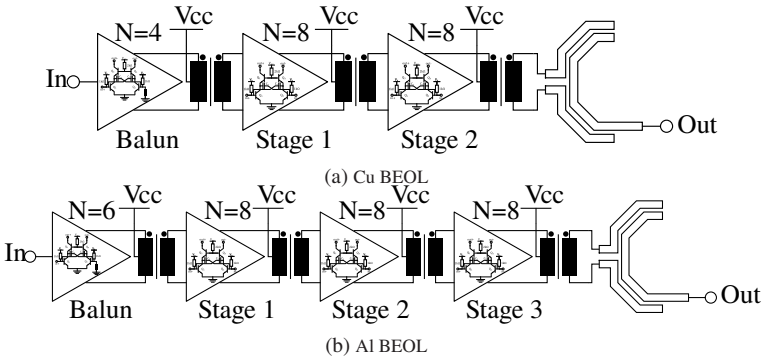
Another option is the use of the capacitive neutralization capacitors C_1. By coupling back the opposing signal, the Miller effect can be compensated. Crucial with this feedback is a short distance to prevent excessive inductance in the path. One last tuning option is the base inductance L_1. By adding this inductance, the gain and broadband behavior of the cascode can be improved [BGH+22].

Together with the transistor sizing, four tuning parameters for RF performance and matching are present in the form of cross-coupling capacitance C_1, interstate capacitance C_2 and the base inductor L_1. However, not all tuning elements can be present in all stages, as stability concerns limit the amount of peaking and feedback.

4.4.2 Comparison PA in Copper and Aluminium Back-end

Using the aforementioned core design, two differential amplifiers are built. Fig. 4.10(a) shows the amplifier build in the copper back-end. It has an active balun as an input stage and two successive stages with a passive Marchand balun at the output for measuring. Fig. 4.10(b) shows the differential amplifier built in the aluminum BEOL. Again, an active balun is used as the input stage, followed by three subsequent stages to improve small signal gain and bandwidth. The output is again attached to a passive Marchand balun.

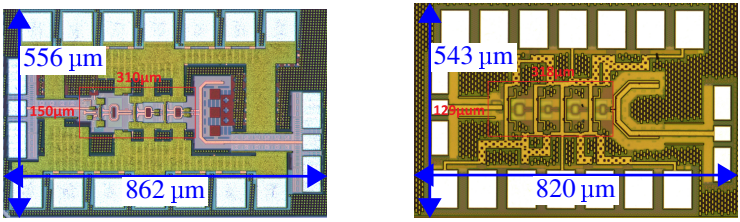
The realized amplifiers are shown in Fig. 4.11(a) and Fig. 4.11(b). The core size of the amplifier, the size excluding pads and seal ring, in the aluminum back-end is 310 µm x 150 µm and in the copper back-end 318 µm x 129 µm. Using transformer coupled stages and compact matching allows for very compact amplifiers that are equal or better to the state of the art presented in in Tab. 4.1.



(a) Cu BEOL

(b) Al BEOL

Figure 4.10: Schematic of two amplifiers build in copper and aluminum back-end. The transistor multiplier for each stage is annotated [17]© IEEE 2022.



(a) Cu, core size 310 µmx150 µm

(b) Al, core size 318 µm x 129 µm

Figure 4.11: Chip micrograph of both realized amplifiers [17] © IEEE 2022.

The small signal behavior of both amplifiers is captured and presented in Fig. 4.12. The simulation target is depicted in red, and the measurement is depicted in blue. The amplifier in the aluminum back-end is designed to peak at 270 GHz with 24.3 dB of gain. The amplifier in copper is designed to peak at 240 GHz with a gain of 26.4 dB. However, the measurements show a significant deviation from the simulation targets. The amplifier in the aluminum back-end shows a shift in frequency and a broader bandwidth than anticipated. Also, the input match shown in Fig. 4.12(c) shows a large deviation. The second resonance peak at 270 GHz is not present in the measurement, while the resonance at 250 GHz is there. The output match shown in Fig. 4.12(e) shows some deviation, while the output match of the amplifier in the copper back-end shows a severe deviation in Fig. 4.12(f). The measured input match

shown in Fig. 4.12(d) shows another resonance at 225 GHz, which is not as strongly present in the simulation. The output shows a shifted resonance with a lower peak.
To evaluate possible underlying issues, a Monte Carlo simulation is run, and the resulting gain curves are plotted in shaded red in Fig. 4.12(a) and 4.12(b). Both amplifiers show a significantly large range of gain values. This is due to the employed feedback methods to enhance the bandwidth and gain being sensitive to the realized base resistance and collector-base capacitance. The results indicate the possibility of instability for some combinations and comparably poor performance for others. Both measurements are within the possible range of gain values obtained by the Monte Carlo simulation. Consequently, the design has to consider options to compensate for manufacturing tolerances or use less feedback to prevent issues.
Another known effect is the substrate node connection of the transistors and their modeling within the simulation. A simple approach is to connect all substrate nodes from the transistor model to a global shared net with the assumption that the slightly conductive substrate will create an equal potential within the MMIC. However, this is not true as physically separated devices have more impedance between them as physically close devices. For larger distances relative to the wavelength, wave propagation effects become relevant. Simulations show that small changes to the substrate node cause large deviations in performance, especially for circuits with feedback. Hence, all further simulations will model these effects by grouping transistors that are physically close within one shared net that is connected into the electro-magnetic (EM)-simulation model with the appropriate position of the substrate tap to also include effects of currents traveling on the ground plane.

The amplifier in the aluminium back-end draws 435 mW from a 3 V supply while the amplifier in the copper back-end consumes 259 mW from a 3 V supply. The higher power consumption of the first PA is due to the additional stage. This also directly influences the simulated PAE for both amplifiers. The PA in the aluminum BEOL only achieves a PAE of 0.38% while the copper PA achieves 1.13%. This achievement is, however, a trade-off between bandwidth and gain. The output power could not be measured, so simulation values were used. It is expected that both amplifiers achieve around 5 dBm of saturated output power. This is below the expected limit of 10 dBm from the survey in Fig. 4.1 and below the published results for other PAs in Tab. 4.1. However, the 9.7 dBm achieved in [BGH+22] uses the successor technology to the here

employed SG13G2 technology. Improvements in the transistors allow for better results without any improvements to the underlying circuit architecture. Consequently, for the used technology, a realistic saturated output power below 7 dBm is to be expected to fulfill the requirements on bandwidth and efficiency.

4.4.3 Model Dissection for Stability and Linearity Analysis

As already presented, stability is a major concern in any PA. Leveraging the full performance of any technology is only possible by employing strong feedback and cancellation techniques that bring any PA inherently close to oscillation. Multiple simulations are run to fully understand the designed power amplifier's oscillation behavior. The most straightforward analysis is the Rollet k-factor run on all four quadrants of the mixed-mode matrix as a result of the small-signal S-parameter simulation [WRE06]. However, this does not capture any internal oscillations. To accurately simulate the interaction between the stages and input and output matching, a correct dissection of the EM-model has to be done. Simulation without an EM-model is nearly impossible as parasitic elements are non-negligible, and parasitic extraction does not accurately capture the resulting inductances.

To correctly dissect the layout for proper simulation partition, the design is split into a core layout consisting of the four transistors of the differential cascode and the biasing networks. The transformers, providing impedance matching between the stages, are further separate models that directly attach to a microstrip-like interface on the core layout. The input and output matching are further blocks that are connected. A strong focus is put on simulating the ground current return paths, which can have detrimental effects if incorrect. Hence, all signal pins have a corresponding ground return from which the current is expected to return. This strategy is also employed for the transformers, which contain a ground ring with a cutout to capture any coupling into the ground plane.

By cascading these elements in simulation, a model that closely resembles the true layout is obtained, allowing for deeper insights. The use of Gamma-probes between the stages captures internal oscillations, which are then used to fine-tune the different tuning elements. The knowledge gained from this

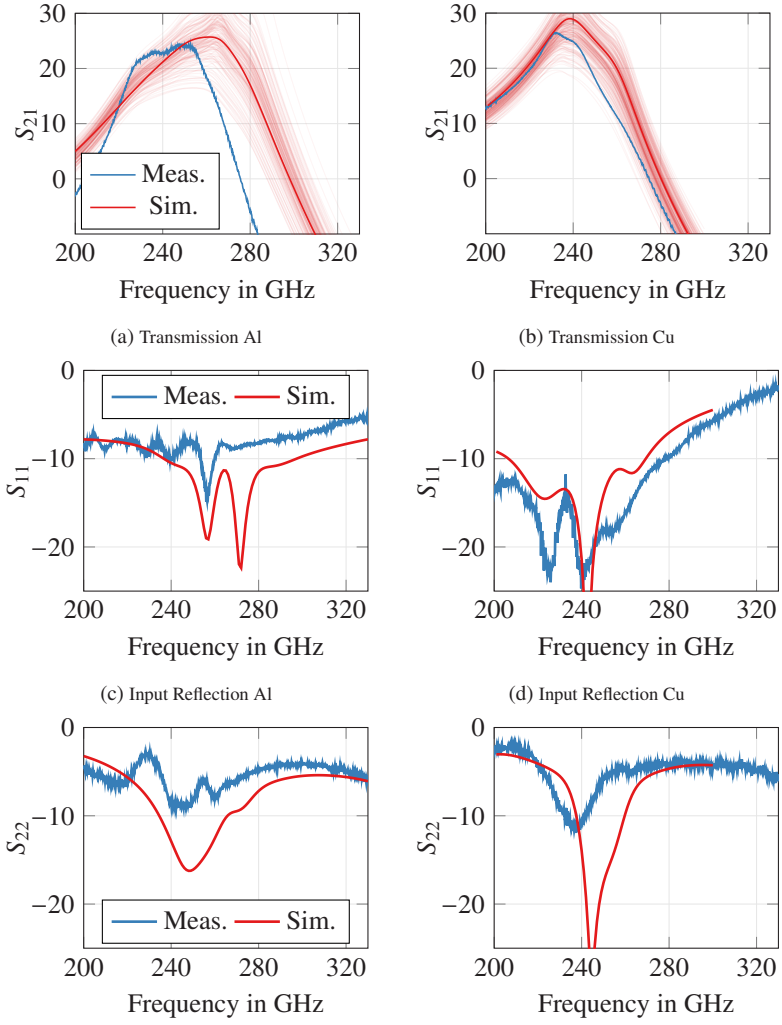


Figure 4.12: Shown are the small-signal S-parameters measured and simulated for both amplifiers. S_{21} also shows the variance through process variations by use of a Monte Carlo simulation as a reference for the measurement results [17] © IEEE 2022.

simulation is also applied to adjust the frequency staggering, demonstrating the practical application of simulation in power amplifier design.

Lastly, a large signal simulation is performed, and the current and voltage waveforms are analyzed on the collector and base nodes. While the class-A and close to f_t operation attenuates most harmonics significantly, certain effects can still be observed in peaking currents or a phase shift under large signal input conditions, indicating a problematic feedback mechanism.

Non-linearity in amplifiers is a complex topic with numerous detailed analyses attempting to capture various effects. As the operating frequency approaches the transit frequency, many higher-order tones are attenuated by the drift velocity of the electrons. However, in frequency-staggered designs, multi-tone analysis is crucial. As different stages are designed to peak at different frequencies, a two-tone stimulus can reveal if any stage will experience adverse effects due to one tone compressing the transistors. A case investigated here are two tones spaced symmetrically around the LO frequency to emulate the dual sideband output of the modulator. Fig. 4.13 illustrates this behavior over two tone spacing and input power, compared to the single tone sweep in dashed lines, providing a clear visual representation of the potential issues.
Single-tone and two-tone sweeps are equal for low powers and show the expected continuous response. As input power increases, we can observe the upper sideband drop faster than the lower sideband until -12 dBm input power, where the upper sideband collapses and reaches power levels below lower input powers. The one-tone sweep shows a peak between 250 GHz and 260 GHz, which is not present in the two-tone simulation showing the compression behavior.

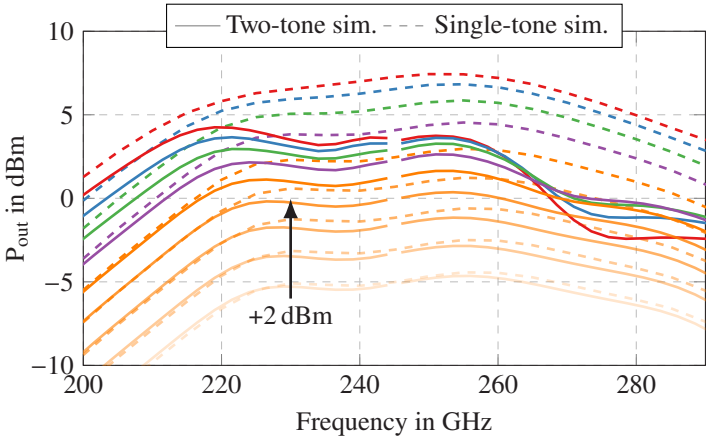


Figure 4.13: Power Amplifier two tone output power over tone spacing around 246 GHz mapped to the corresponding frequency and single tone output power in dashed lines. The input power is swept in 2 dBm increments from −26 dBm to −10 dBm.

4.4.4 Final Design

The final version of the differential power amplifier for the overall system is designed considering the previously presented design aspects. It consists of a frequency-staggered, three stage design using different transistor multipliers in each stage. All stages are coupled with transformers.

Fig. 4.14 shows the schematic of the first stage of the power amplifier. This stage is fed from the differential output of the BPSK modulator. The modulator is connected through a transformer to save space. Hence, the modulator and transformer impedance are considered while sizing the stage. It was found that no cross-coupled capacitors are necessary, as the lower input capacitance of the smaller transistors is sufficient to have the desired bandwidth. The base boost inductor was used and sized within practical limitations to maximize bandwidth. A value of 11 pH gave the best result. The output is transformer coupled to the next stage with 40 fF of series capacitance to tune the frequency response.

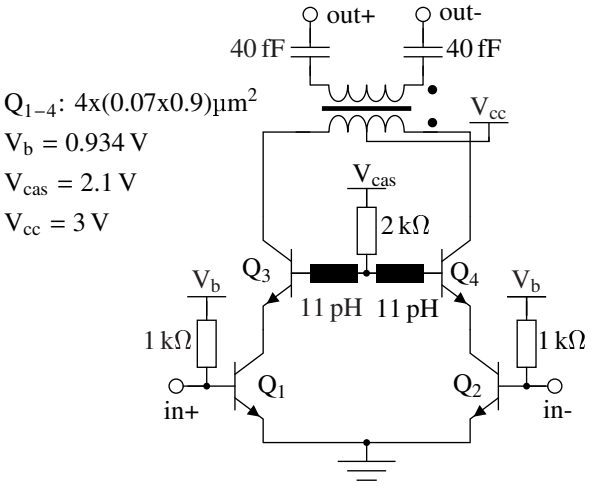


Figure 4.14: Schematic of the input stage of the final power amplifier [2] © IEEE 2023.

The schematic of the second stage is shown in Fig. 4.15. Here, cross-coupled capacitors are used as it was found necessary to boost the high-frequency response. The base boost inductor is 11 pH. The output is coupled with 60 fF as the output stage has larger transistors.

Fig. 4.16 shows the power stage of the amplifier. No base boost inductor is used. Further, no center tap for the upper base is used due to the larger size and current requirements. Instead, they are shorted together and feed symmetrically from the outside. Cross-coupled capacitors are also used to tune the frequency response. The output is connected through a transformer to allow for AC-coupling and collector current supply. Further, it was found easier to match the circuit with the transformer and two shorted stubs of 25 Ω impedance and 35 µm length. The output is differential and connected to a 100 Ω differential output pad.

A cut-open layout view of the amplifier core of a single stage is shown in Fig. 4.17. The design lies within a differential GCPW channel with fixed spacing for the ground walls. Adjacent to these ground walls are the fully shielded bias networks. The shielding should ensure no coupling path between the RF output and the bias connections. The four transistors of the core are

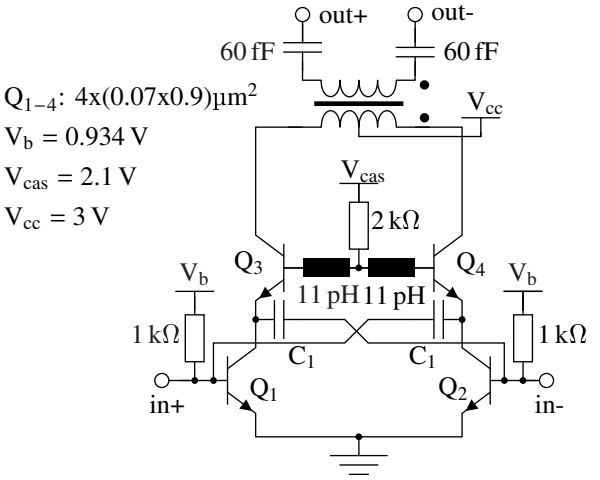


Figure 4.15: Schematic of the second stage of the final power amplifier [2] © IEEE 2023.

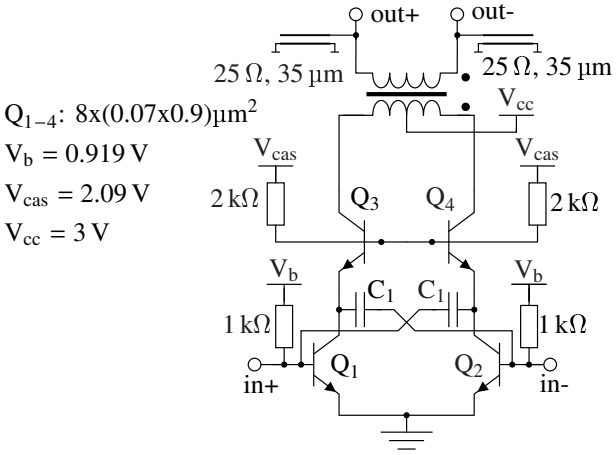


Figure 4.16: Schematic of the power stage of the final power amplifier [2] © IEEE 2023.

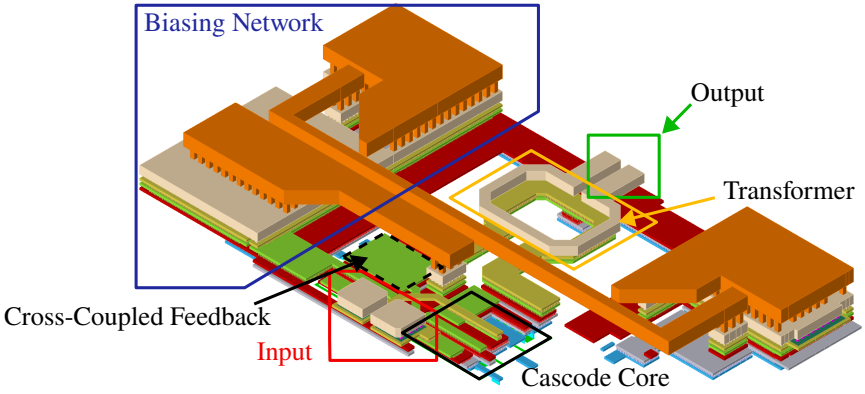


Figure 4.17: Amplifier core layout view with removed elements for better visibility of internal features.

physically close enough to equalize the temperature between them, and a local, shorted substrate net is used to model the interaction. The collector voltage and current are fed through the transformer, which is connected through a tap going down to metal 1 and 2. The upper and lower base voltage is fed through metal 1 connections from either side. A larger Top Metal 2 bar connects both grounds and has a center connection to ensure proper ground potential between the two halves of the differential pair. Another Top metal 2 bar connects the bias supply voltages to ensure an equal potential on both sides.

The RF input connects through a capacitor down through a tapered transition to the entire width of the metal 1 base connection. The cross-coupled capacitors are realized as CMOM capacitors over the emitter-collector connection. The base boost inductor is realized as a section of metal 1 line feeding the base. The overall ground plane is on metal 3. Fig. 4.18 shows the simulated small signal gain. The gain response is very broadband and flat, with a final 3 dB bandwidth from 217 GHz to 291 GHz and a maximum gain of 19 dB. Fig. 4.19 shows the simulated output power over input power and the PAE. The saturated output power is 8 dBm at 250 GHz. The OP1DB is 4.5 dBm and the peak PAE is 2.7 %. The final circuit is shown in Fig. 4.20. The PA core measures 225 µm x 200 µm. It shows the amplifier within the final MMIC with the modulator to the left feeding the three stages of the PA. In the center, the

differential output pad is visible with the on-wafer test structure, consisting of a differential pad and a passive balun. This structure can be wire-bonded to the MMIC for direct on-wafer measurements. The MMIC has to be diced along the included dicing lines to connect an antenna. Also visible are the two matching stubs at the output and the ground bridges over the core to equalize the potential. The whole surface around the PA is covered in top metal 2 ground to increase shielding. The DC feeds are brought in from the pads through shielded zero-ohm lines [TFL+15].

Dedicated measurements of the final design were not conducted for two reasons. Firstly budgetary constraints limited the available chip area for manufacturing. Secondly the available time did not allow for a dedicated fabrication run of a stand-alone amplifier. This lack of measurement data is however compensated by elaborate simulative assessment and the chosen adaptive packaging solution. The latter one allows for indirect measurements and evaluation of the PA.

The last entries in Tab. 4.1 list the presented PAs from this work. The final design achieves very competitive results regarding output power for a system without power combining. The small-signal bandwidth exceeds all previously published PAs. The power consumption is quite typical for a SiGe PA as the class-A operation does not leave much efficiency to gain. In terms of efficiency the design exceeds the state of the art in simulation with a calculated PAE of 2.7 %. With additional losses in the transition and feeding lines the real circuit will have a lower PAE. Due to the transformer matching, the presented PAs are the smallest of their kind and offer the best integration density.

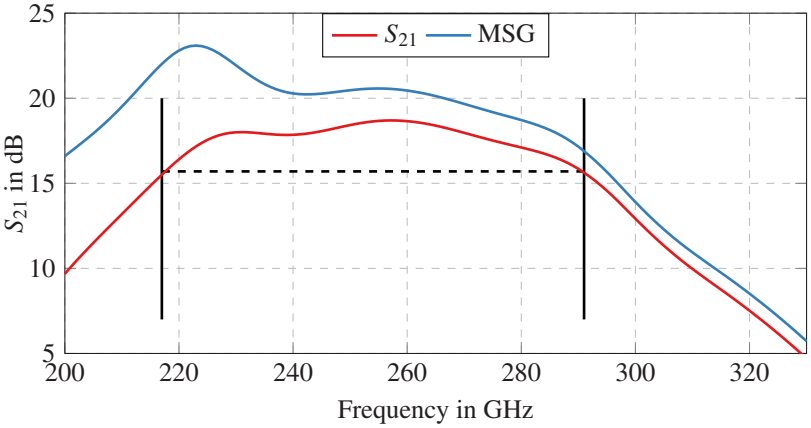


Figure 4.18: Simulated small signal gain of the final amplifier.

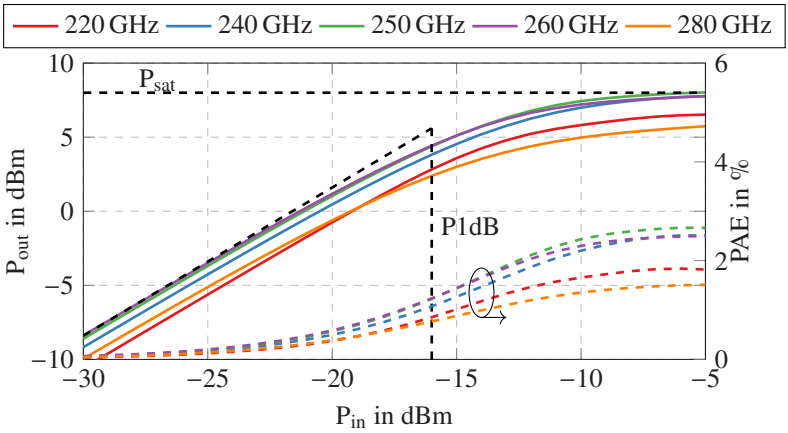


Figure 4.19: Simulated output power over frequency and input power.

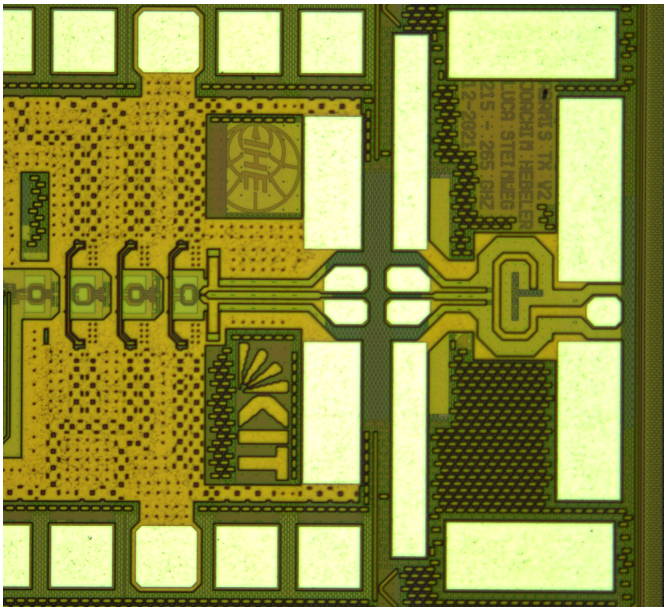


Figure 4.20: Micrograph of the final power amplifier within the transmitter chip with the differential output pad and external balun for direct measurement.

5 Wideband Phased Array Antenna Designs

The design targeted within this work requires wideband antennas operating in the sub-THz regime and tying into the MMIC. Such wideband antennas, suited for operating within a phased array, are widely known and used at lower frequencies. However, the specific challenges of operating above 200 GHz and achieving at least 50 GHz of bandwidth limit the applicability of many such designs. One of the main integration challenges is the availability of suitable materials and machining options. With a free space wavelength of 1 mm at 300 GHz, the necessary feature sizes smaller than $\lambda/10$ are below 100 µm. Depending on the ϵ_r of the chosen substrate, precision down to the micrometer range is necessary, which many economic widespread manufacturing techniques cannot offer.

Hence, looking at state of the art presented in Fig. 5.1, most published antennas connected to a MMIC are realized as planar on-chip antennas utilizing the sophisticated and highly accurate metal processing of the semiconductors BEOL. While the metal can be structured to sub-µm precision, the thickness of the stack-up is comparably low and creates efficiency problems. This drawback shrinks as frequency increases, making them very interesting for the THz regime above 300 GHz. However, the targeted operating frequency lies in the sub-THz region. To alleviate this drawback, one approach presented in [EMW+18] or [3] is the utilization of a backside metallization. By attaching the MMIC to a metal plate, the distance between the antenna element and the reflector can be tuned by the bulk silicon thickness. However, this approach puts some major constraints on the overall assembly and necessitates precise grinding of the bulk silicon or risks significant resonant frequency change. Another issue is the increased loss of the doped silicon bulk material. Lastly, due to the high dielectric constant of bulk silicon substrate and parallel plate waves propagate perpendicular to the antennas radiation direction. One approach to compensate for this is by locally etching away the bulk silicon, called

LBE. The cavity created by this process influences the antenna resonance and creates additional costs [3]. Further the precision of the etching is comparably low as the etching depth is comparably large. Hence, LBE should be avoided where possible.

Another approach in compensating for the poor performance of on-chip antennas are integrated lens antennas (ILAs). The ones presented in Fig. 5.1 show exceptional bandwidth, high gain, and good efficiencies. However, they are not applicable for phased array systems as the high gain beam limits the steering angle significantly, and the focal point of the lens has to align with the array. Further, in raw materials and assembly, ILAs are expensive. Lastly, ILAs are not usable within UE applications as their physical size restricts their usage. The same considerations are true for external dielectric lenses. An alternative to lenses is using resonators to load the antenna, as presented in [DLL+15]. This promises good efficiencies and bandwidth.

A different approach was chosen in [AdGW+22] with a Vivaldi antenna on a 50 µm liquid crystaline polymer (LCP) substrate feed by a flip chip transition. While LCP has many beneficial properties for mm-Wave applications [TTJ+04], it is not without issues. One severe problem it faces is the inherent anisotropic heat expansion with an almost ten times higher expansion in the z-direction [BK20]. This limits compatibility with classical FR-4-like substrates but also poses issues with the reliability of formed VIAs. Further, measured dielectric losses of LCP are not significantly better compared to current generation RF substrates with measured tan δ values around 0.02 [ML22]. Hence LCP is not further investigated as it does not fit within the overall goals of this work. Another approach using organic PCB substrates is presented in [LGB+17]. There the presented results suffered heavily from manufacturing differences but is promising.

A Vivaldi-like antenna is inherently wideband; however, it also includes disadvantages. The antenna presented in [AdGW+22] works because only a single substrate layer is used. Using the same concept in a multi-layer stack necessitates cavities around the antenna. Another issue is the inherent side-firing of the classical Vivaldi, making integrating within an MMIC problematic. All CMOS MMICs are manufactured with a seal ring, a distinct metal structure around the die to prevent crack formation during cutting. This seal-ring would shield the EM-wave from exiting the substrate. Removing the seal ring to expose the antenna would cause reliability concerns. In [JKHP15], a broadside

radiating Vivaldi-like antenna is presented. While interesting, it shows poor performance. Another disadvantage is the more complicated differential feed of most Vivaldi antenna designs.

One last consideration is the decision between a differential and a single-ended antenna. The latter is easier to implement and test, as all on-wafer measurement equipment is single-ended. Further, the inherent asymmetry of a single-ended feed allows for more antenna designs. However, the power amplifier within the MMIC is differential. Hence, a balun would be required to attach to the single-ended antenna. This introduces losses and additional chip-surface area. Therefore, only differential antennas are investigated. The analysis of the state-of-the-art yields two possible approaches. The first approach is differential antennas on a PCB-like substrate for maximum integration within the system. The second approach is some form of resonator-loaded on-chip antenna.

5.1 PCB Antennas

Antennas on PCBs are widely used at lower frequencies. However, with increasing center frequency, feature sizes shrink below the average capabilities of common manufacturers, and prepreg thicknesses are within a significant fraction of the wavelength. This limited the use of PCB substrates for antennas in this frequency range in the past. However, fabrication is improving, and with semi additive processing (SAP), copper feature sizes below 50 µm on commercially available PCB substrates are readily achievable [SMK+99]. Further, the availability and quality of RF-specific substrates are increasing. Thus, in [LGB+17] a first PCB based antenna above 200 GHz was presented. An issue accentuated by the necessary thin substrates is variations in the final substrate thickness [LLK+23]. With changes in the metal density, the realized thickness changes, resulting in changes to the antenna. Only those antennas with a solid ground plane are investigated to minimize the effect.

As substrates *Megtron 6* and *Megtron 7* from *Panasonic* are used. The classical patch antenna is the obvious choice for a broadside radiating antenna over a solid ground plane within a planar process. However, achieving at least the necessary 50 GHz of bandwidth requires an antenna with more than 20 % of relative bandwidth. This is not achievable due to the physically small

Table 5.1: State-of-the-art of MMIC connected antennas.

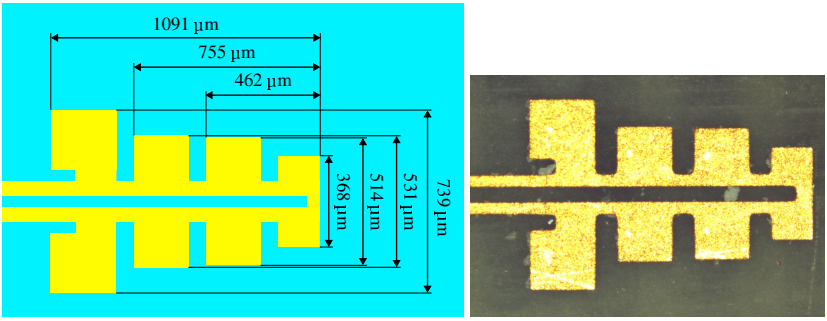
Ref	Type		Substrate	Gain in dBi	BW in GHz	Rel. BW	f_C in GHz	Efficiency	Area mm^2
Reference									
Standard gain horn		SE	Metal	25	110	41.51 %	265	90 %	
Planar									
[YS15]	Dipole antenna with backside reflector	Diff	CMOS	4	25	19.61 %	127.5		0.904
[TRCE18]	Dipole with bondwires	SE	CMOS	2	0.2	12.50 %	160		0.6
[JKHP15]	Half-cloverleaf	SE	CMOS	3	65	34.67 %	187.5		0.84
[JKHP15]	Slot bow-tie	SE	CMOS	4	80	44.44 %	180		0.6
[HKP15]	Broadside Vivaldi	SE	CMOS	1.2	23	23.20 %	178.5		0.8
[EMW+18]	Double dipole	SE	CMOS	7*	40*	16.67 %*	240*	65 %*	0.904
[PKT+12]	Leaky wave MS	SE	CMOS	4.5	30	11.76 %	255	26.50 %	1.25
[3]	Bow-tie with LBE	Diff	CMOS	7.5	16	5.25 %	305	42.50 %	1.44
[DLL+15]	On-chip patch, DRA	SE	CMOS, Alumina DRA	10	41	12.08 %	339.5	80 %	0.49
[DLL+15]	On-chip patch, parasitic resonator	SE	CMOS, PCB	5*	66*	27.62 %*	239*		0.56
[AdGW+22]	Vivaldi on LCP	SE	LCP	10*	40*	15.38 %*	260*	65 %*	10.95
[LGB+17]	Slot fed patch	SE	PCB	5	22	9.87 %	223		
[WLY23]	Higher-order mode	SE	PCB	13.5	40	20 %	200	63 %	11.7
ILA									
[GPK+17]	ILA	SE	CMOS. 12mm Si Lens	24.9	120*	46.15 %*	260*	90 %*	
[SRG+21]	Bow-tie with Si lens	Diff	CMOS, 10mm Si Lens	24.7*	80*	33.33 %*	240*	65 %*	
[GSSP15]	ILA	Diff	CMOS, 9mm Si Lens	25*	290*	101.75 %*	285*		
[HNSK+21]	DFCLS, Lens	Diff	CMOS, 10mm Si Lens	15	70	31.11 %	225	31 %	
Dielectric Lens									
[JBP13]	Patch with lens	Diff	CMOS, Dielectric Lens	2.26*	24*	9.96 %*	241*		
This Work									
PCB v1 [6]	Staggered Patch	Diff	PCB	3.2	75	30.93 %	242.5	70 %*	0.99
PCB v2	Staggered patch	Diff	PCB	6	80	33.33 %	240	72 %*	0.88
Glass resonator	Shorted bow-tie w. resonator	Diff	CMOS, Glass	4.1	58	23.29 %	249	65 %*	0.64
3D-print	Shorted bow-tie w. resonator	Diff	CMOS, 3D-Print	5.4	62	22.96 %	270	55 %*	0.64

*Simulated Values

size of the classical patch antenna limiting the best case bandwidth and efficiency [GTC14]. Hence, the design is based around a frequency-staggered design using multiple series feed resonators to increase the aperture and enhance the bandwidth. The final geometry of the antennas is found by numerical optimization.

5.1.1 PCB Antenna Version 1

The initial version of the PCB antenna is shown in Fig. 5.1(a). Four series fed patches with different sizes form the wideband antenna. This is a variation of the series-fed patch antenna with non-uniform patches. The used substrate is *Panasonic Megtron 6* with a layer thickness of 60 µm. The first and largest patch has insets for matching. The last patch shorts the two differential lines together and features an inset for matching. The realized geometry is shown in Fig. 5.1(b). The antenna length is 1.6λ on the given substrate. The manufacturing causes some deviations. Especially the inside 90° angles are rounded with a radius of 15 µm. Investigating the manufacturing tolerances yield deviations of up to 33 % of the nominal values [6]. Especially the narrow tranches have deviations of up to 20 µm. All structures are over-etched with an average deviation of 8 µm.



(a) Antenna Layout (b) Antenna Micrograph

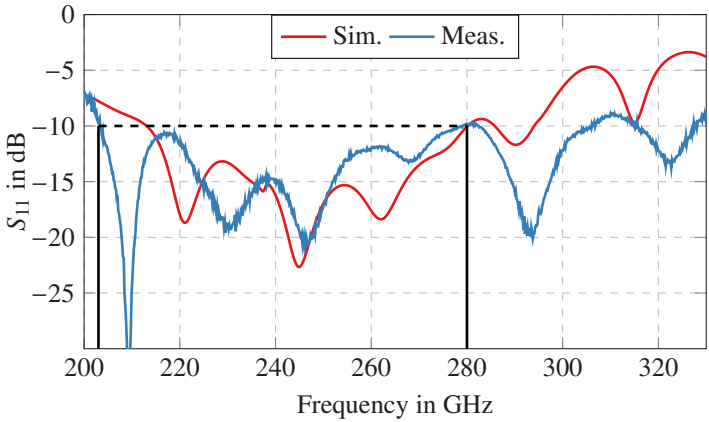
Figure 5.1: The realized antenna geometries. Four resonators enhance the bandwidth of the antenna. The first antenna element has an inset to match the feed line. The fourth resonator shorts the feed line. The dimensions are shown in the layout view in (a) and the micrograph in (b) [6] © PIER L 2023.

The differential antenna is not directly measurable due to the lack of appropriate measurement equipment. Instead, an external balun is connected to the differential line. Fig. 5.2(a) shows the assembly's measured and simulated input match. Measurement and simulation agree; however, the measured response shows a stronger resonance at 210 GHz. The measured input return loss is better than −10 dB from 205 GHz to 280 GHz, yielding a 75 GHz bandwidth. The realized gain at boresight over frequency shown in Fig. 5.2(b) shows a stronger deviation from the simulation. The gain is lower than anticipated and shows a distinct peak at 240 GHz with a measured value of 3.2 dBi. The observed drop in measured gain is in line with the expected 2 dB drop in the differential bondwire transition and 1.2 dB loss in the employed balun. This yields a corrected realized gain of about 6 dBi.

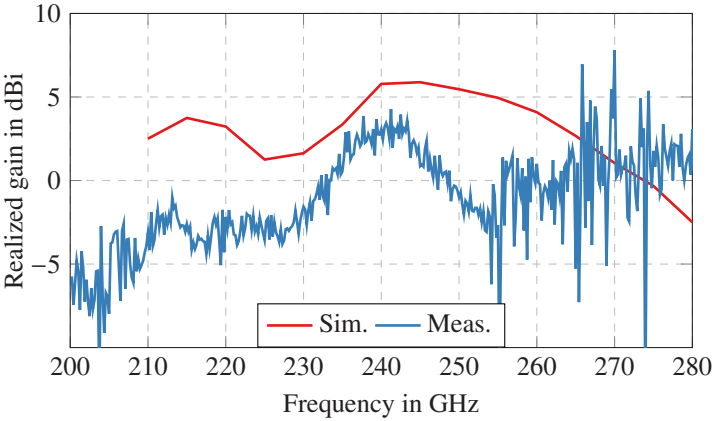
Investigating the radiation patterns shown in Fig. 5.3(a) and Fig. 5.3(b), a good agreement between measurement and simulation is visible. The additional ripple is due to radiation from the balun and probes as described in 3.5.2. Also plotted in Fig. 5.3(a) is the antenna simulation without the balun and transition, showing the gain loss due to transmission losses. While the realized antenna has achieved the desired bandwidth and performance goals, a notable issue with its geometry is a strong, frequency-dependent beam tilt. This is primarily due to the arrangement of the different resonators, which requires further attention.

5.1.2 PCB Antenna Version 2

In a second version, the frequency tilting issue is sought to be alleviated. By rearranging the resonators and merging the two middle ones, the geometry shown in Fig. 5.4 is realized. The dimensions are given in Tab. 5.2. A major difference to version 1 is the used substrate. The antenna is realized on a 89 µm thick *Megtron 7* prepreg layer. Another difference to the previous antenna is the measurement approach. Before, an external balun was connected to create the differential stimulus. However, this process step is introducing many unknowns and also necessitate a suitable balun, which was not available for this measurement. Hence, another approach is pursued. For this the differential 100 Ω line is connected by the the center pin and one ground pin of a GSG on-wafer probe. The impedance between the center pin and each ground pin is also 100 Ω. Therefore no severe impedance mismatch is present

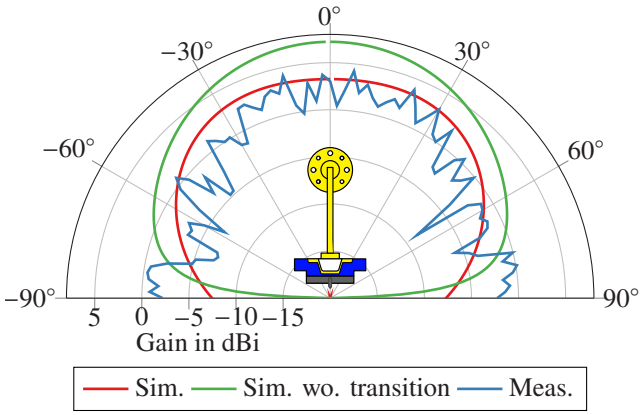


(a) Input match

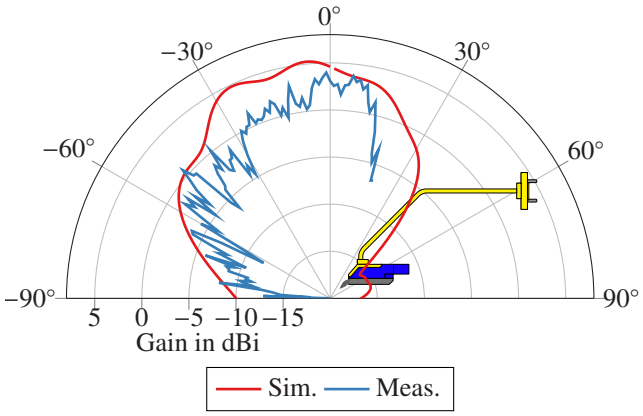


(b) Gain over frequency

Figure 5.2: Measured and simulated input match (a) and gain at boresight (b) over frequency for the first version of the PCB antenna [6] © PIER L 2023.



(a) E-Plane



(b) H-Plane

Figure 5.3: Simulated and measured pattern of the realized PCB antenna for version 1 at 240 GHz. Figure (a) shows the E-Plane and (b) the H-Plane [6] © PIER L 2023.

Table 5.2: Antenna dimensions as labeled in Fig. 5.4.

h_1	h_2	h_3	h_4	h_5	w_1
248 µm	313 µm	659 µm	720 µm	1004 µm	699 µm
w_2	w_3	w_4	s_1	s_2	s_3
404 µm	786 µm	65 µm	46 µm	45 µm	72 µm

and only the additional parasitics of the asymmetric probing influence the measurement. Simulations show that this approach is repeatable and reliable enough to extract information about the radiation pattern. Alternatives like non-contact characterization are not applicable, as the cost and wafer space for the additional test structures were not available [SNS22].
The simulated and measured input match is plotted in Fig. 5.5. The antenna simulation shows a good input match over almost the whole H-band, except for a range around 255 GHz. The measured input match deviates due to the special probing. Hence, the simulation, including the probe, is repeated and plotted in green in Fig. 5.5. Measurement and simulation agree well, indicating the overall good performance of the antenna. Fig. 5.6 shows the measured and simulated gain over frequency. The measured gain at boresight is higher than simulated. This is an artifact of the measurement as the radiated wave reflects at the probe body and increases the measured gain.
This is even more evident in the measured field patterns shown in Fig. 5.7(a) and Fig. 5.7(b). In the E-plane, the pattern shows a shift to negative angles. In the H-plane, the probe shadowing is visible for angles larger than 25° and subsequently, the increase in gain for lower angles is also present [7]. However, the frequency-dependent tilting is minimized. Overall, the antenna fulfills the requirements and marks a significant improvement over the state of the art.

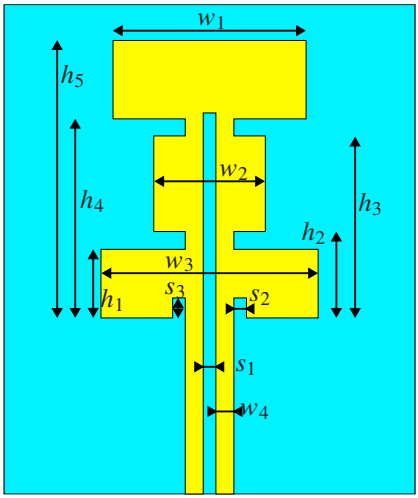


Figure 5.4: Layout of the second version of the PCB antenna [5] © IEEE 2024.

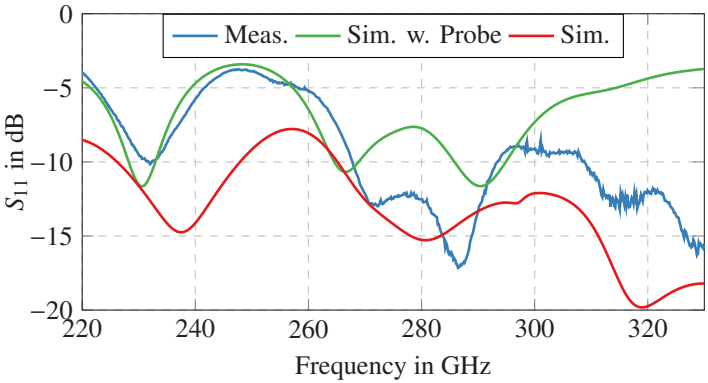


Figure 5.5: Simulated and measured input match over frequency for the second version of the antenna.

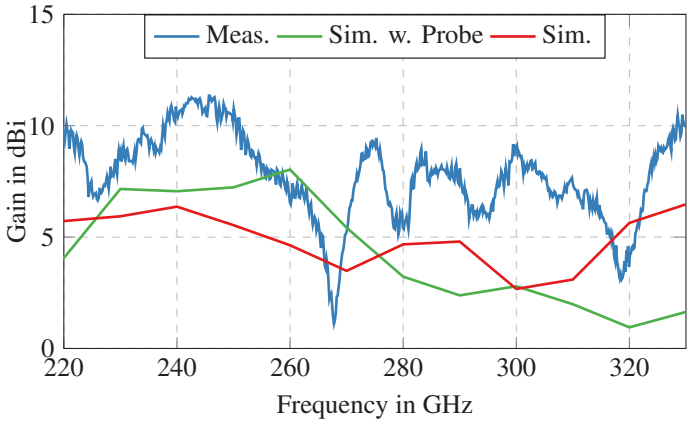
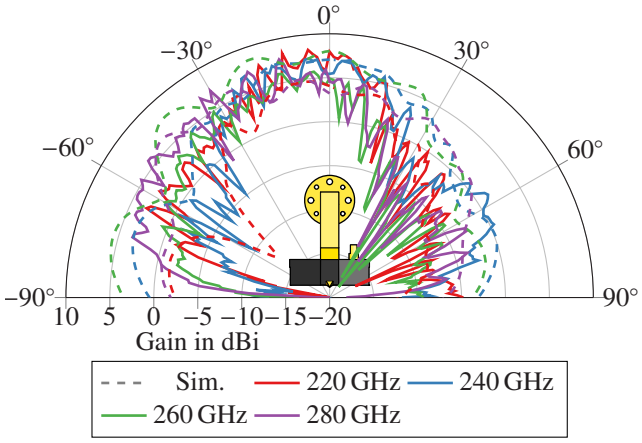
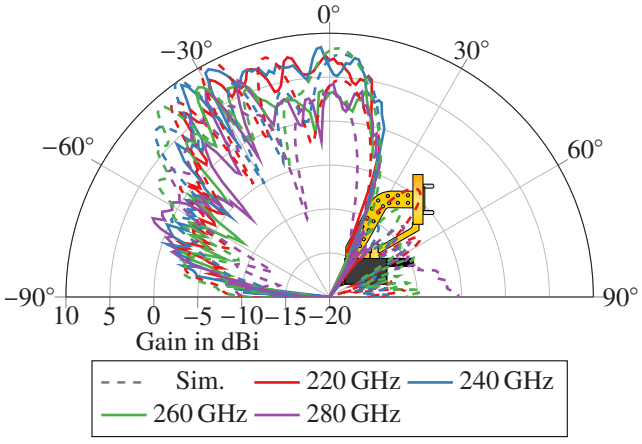


Figure 5.6: Simulated and measured and gain over frequency for the second version of the antenna.



(a) E-Plane

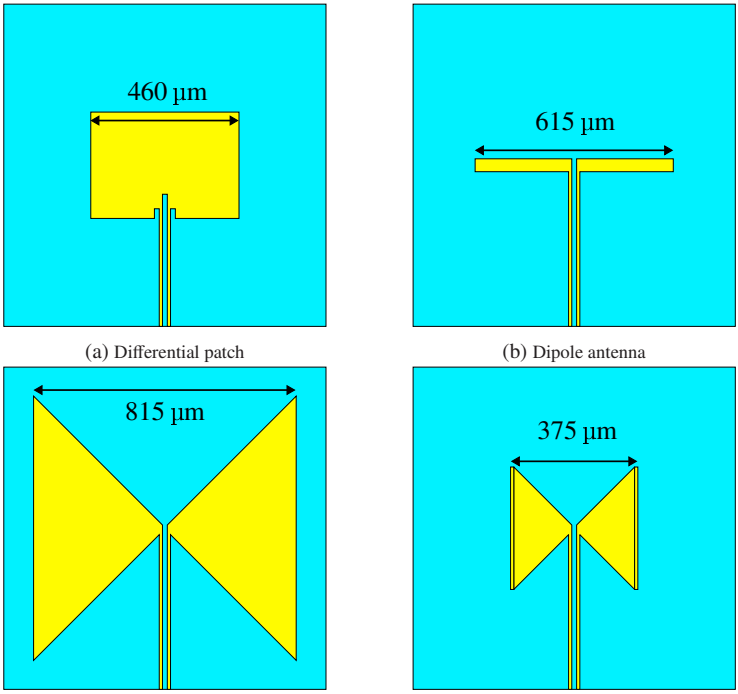


(b) H-Plane

Figure 5.7: Measured field pattern in the E- and H-plane of the PCB antenna version 2.

5.2 On-Chip Antennas

On-chip antennas have seen quite a lot of utilization as the state of the art presented in Fig. 5.1 shows. However, many of the designs presented face serious issues and drawbacks. The main hurdle to overcome is the lacking flexibility in the stack-up. While structures down to the nm-range can be manufactured in x- and y-direction, the total thickness of the stack-up is limited to 10 µm to 20 µm. This height is not sufficient to place a reflector behind a patch for example. Approaches using the thickness of the bulk chip suffer from the high resistivity silicon and the necessary precise grinding of the die. Utilizing LBE to remove the bulk silicon helps in reducing losses, but does not change the issues related to the manufacturing. Utilizing lenses to boost the gain and efficiency is costly and does not fit the application.
Hence, an antenna topology is to be developed that does not necessitate any backside reflector while achieving wide bandwidth, high efficiency and moderate gain. A promising solution is the use of resonator loaded antennas [DLL+15], [CBZL23]. While dielectric resonators can be quite compact, they face several other manufacturing issues, especially achieving proper mechanical dimensions is challenging [VHdM+20]. Hence, a design with a parasitic patch similar to [CBZL23] is investigated. Crucial for this approach besides the differential construction is the wideband operation of the fundamental feeding structure.
To obtain an optimal feeding structure, four different approaches are identified and compared against each other using *CST Microwave Studio*. These are the differential patch shown in Fig. 5.8(a), the differential dipole shown in Fig. 5.8(b), the classical bow-tie antenna shown in Fig. 5.8(c) and the shorted bow-tie antenna shown in Fig. 5.8(d). Shorting the bow-tie ends is an extension of the shorted patch antenna in [HWGH10] to the bow-tie concept. By electrically shorting the elements the length of the bow-ties can be halved.
To compare the different elements, they are simulated without resonator. From these simulations the input match and radiated power are investiagted and compared, which is shown in Fig. 5.9. All radiating elements show poor input match, as is expected. Their design is aimed to work with an additional resonator, hence the radiating element itself performs rather poor. From these results the shorted bow-tie construction offers the best tradeoff between wideband input match and radiation compared to the other three. Both the differential patch and the classical bow-tie antenna have a very distinct resonance,



(a) Differential patch (b) Dipole antenna

(c) Bow-tie antenna (d) Shorted bow-tie antenna

Figure 5.8: Simulated layouts of possible on-chip wideband differential antenna geometries without backside reflector.

which results from a high-Q resonator in the structure itself. Such a behavior is not desired for wideband operation, as it limits the achievable bandwidth and efficiency.

Going on from this evaluation a shorted bow-tie feeding element on-chip is designed. The resulting layout is shown in Fig. 5.10(a). The width and height of the overall antenna is $w_1 = 800\,\mu\text{m}$ by $h_1 = 800\,\mu\text{m}$ and the antenna elements themselves are $w_2 = 400\,\mu\text{m}$ by $h_2 = 400\,\mu\text{m}$. The realized MMIC is shown in Fig. 5.10(b). The parasitic patch to enhance the performance of the antenna can be realized in different technologies. This work investigates a

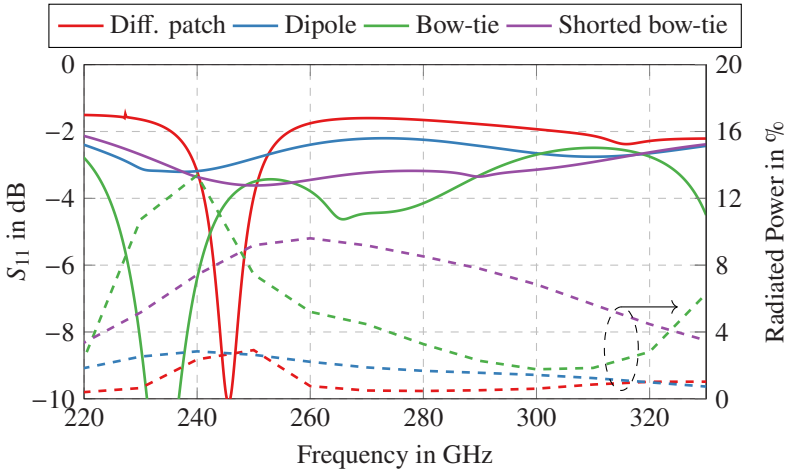
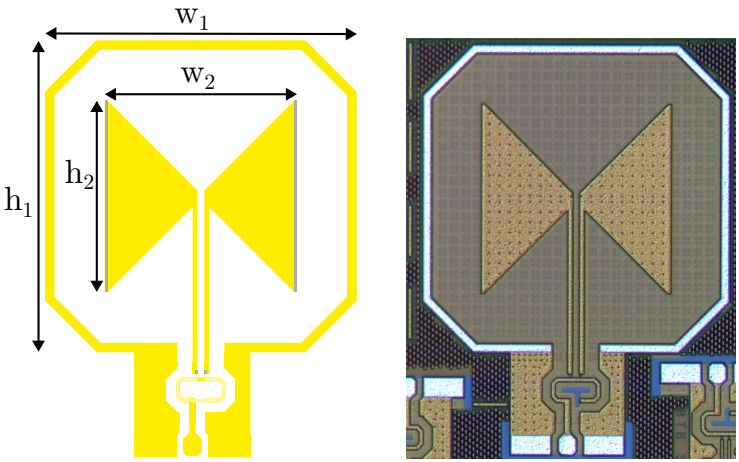


Figure 5.9: Simulated input match and radiated power of the four tested feeding elements without resonator for initial comparison.



(a) Layout

(b) Fabricated Chip with shorted bow-tie antenna

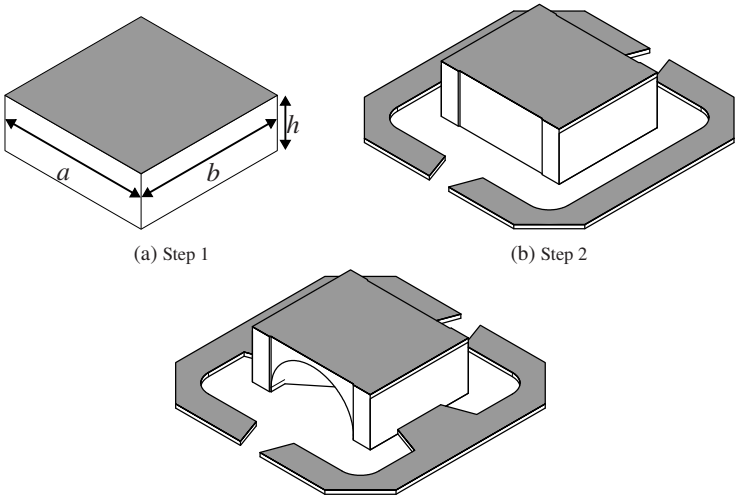
Figure 5.10: Layout and chip micrograph of the realized bow-tie antenna.

novel 3D-printing approach and a more classical thin film approach on a glass substrate.

5.2.1 On-Chip Resonator Design

To enhance the radiation of the designed feeding structure a parasitic patch is to be introduced. This is done by 3D-printing a base structure that is then metallized. While 3D-printing offers great flexibility in terms of surface design, many features, especially metallized 90° walls are not realizable in the chosen approach. Hence the design of the resonator has to be adapted to the constraints of the printing process. The start of the design is a simple rectangular metal patch that is rudimentary optimized in terms of edge lengths and height above the feeding antenna to give the best possible solution for this shape. The initial design is shown in Fig. 5.11(a).

With this initial step, a characteristic mode analysis (CMA) is performed to analyze possible modes of excitement. This yields multiple strong possible modes due to the rectangular structure of the patch. The electric field strength of the three most significant modes are shown in Fig. 5.12(a), 5.12(b) and 5.12(c). Due to the resonator's square shape, both Fig. 5.12(a) and Fig. 5.12(b) are rotation symmetric. The third possible mode sees the electric field in the corners. For the best possible excitement with the bow-tie feeder, only the first mode should be excited and possible to resonate. Elongating one side helps to suppress mode 2. Further, a split ring on a lower height is added to suppress the excitement of the corners, yielding the structure shown in Fig. 5.11(b). The CMA analysis yields the field distributions shown in Fig. 5.12(d) to 5.12(f). There are still three possible modes. However, they are more distinct and have less commonality. The first mode is the desired one. The second mode sees only the ring exited, which is unwanted. The third mode sees the field below the ring's metal, which will not be possible in the final assembly due to the feeding structure. Indents to the ring close to the center resonator are added to suppress the other modes, yielding the structure shown in Fig. 5.11(c). Further, the 3D-printed substrate block is hollowed out to reduce dielectric losses and keep the impedance of the feeding microstrip line on the chip constant. The resulting mode is shown in Fig. 5.12(g). The ring is excited at the splits, and the resonator is excited as intended. As a comparison, a more classical approach of a 9 element parasitic patch resonator on 100 µm glass is shown in



(a) Step 1

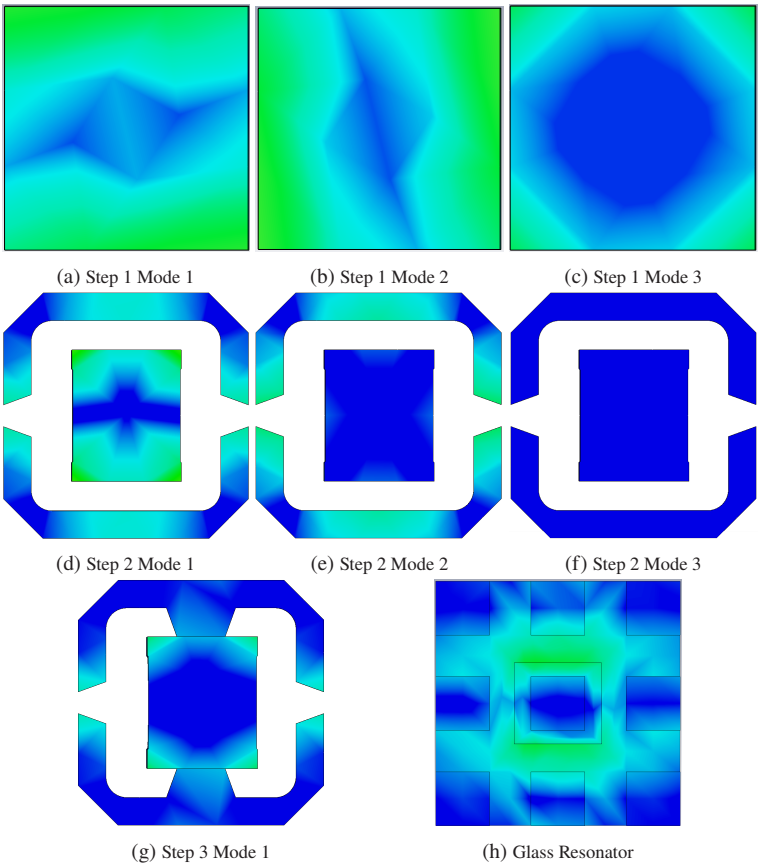
(b) Step 2

(c) Step 3

Figure 5.11: Step-by-step improvement of the resonator layout by using CMA analysis to prevent unwanted modes.

Fig. 5.12(h). While the structure is both mirror and rotation symmetric, there are more possible modes than the one shown. However, due to the excitement, the field distribution is split alongside the bow-ties symmetry plane, which is horizontal.

After the optimization of the resonators metal structure simulations are run to evaluate the influence of the 3D-printed dielectric. Material measurements of the resin show an ϵ_r of 3.1 and a $\tan\delta$ of 0.01. To avoid excessive losses in the resin one might seek to utilize the 3D-printing process to include more voids. To evaluate the influence of the different materials a simulation of the complete antenna assembly is done in *CST*. The metal thickness on the resonator is assumed to be 600 nm of copper, which is a typical value for the sputtering process used. Extracting the losses per material gives the plot in Fig. 5.13. Evidently the dielectric losses are the smallest part with about 10 % of power dissipated. Much more detrimental to the overall efficiency are the losses in the metals and especially the loss in the top most metal layer of the BEOL stack with close to 20 % of loss.



(a) Step 1 Mode 1 (b) Step 1 Mode 2 (c) Step 1 Mode 3

(d) Step 2 Mode 1 (e) Step 2 Mode 2 (f) Step 2 Mode 3

(g) Step 3 Mode 1 (h) Glass Resonator

Figure 5.12: Electric field strength distribution over the four iterations of the resonator and different significant modes as well as a classical 9 element metallic parasitic resonator.

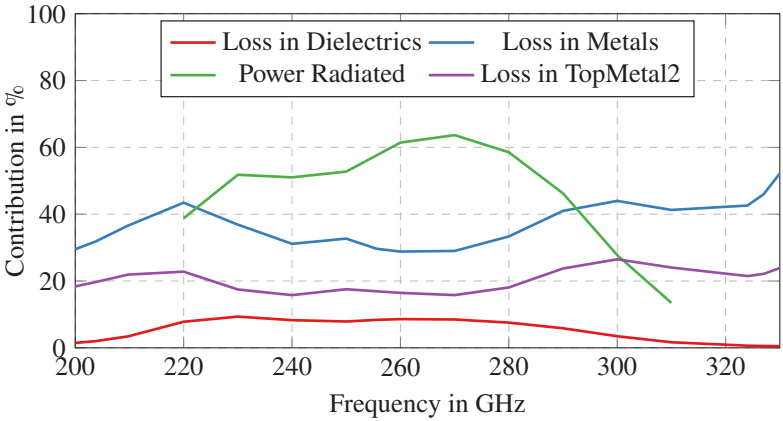
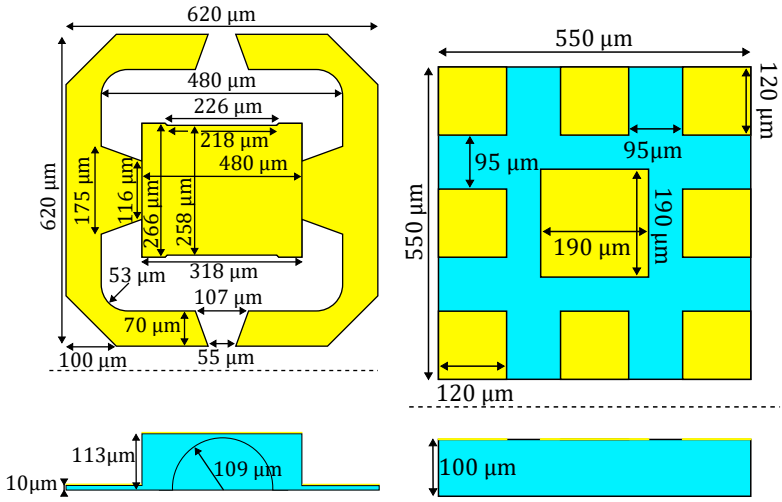


Figure 5.13: Simulated percentage of radiated power and losses in dielectrics and metals.

The layouts of both implemented designs are shown in Fig. 5.14 and their respective design value are annotated in the figure as well.

5.2.2 Resonator Sample Manufacturing

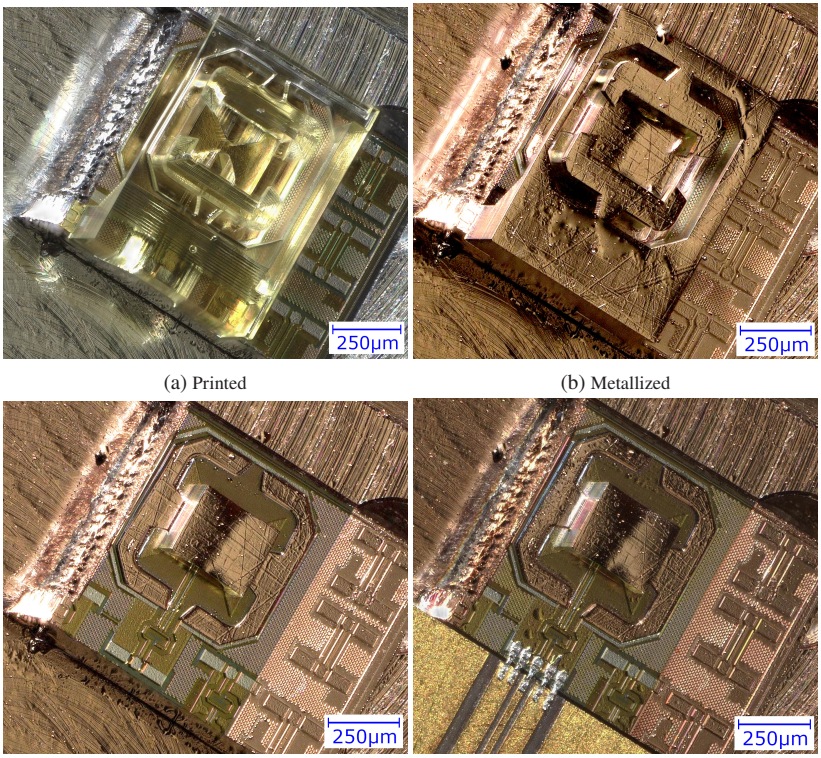
The bow-tie antenna is realized in the BEOL process of *IHPs* 130 nm *SG13G2* technology using top metal 2 for the bow-tie element and feed lines as well as metal 2 for the ground plane. The stack up is shown in Fig. 4.2(a). The distance between top metal 2 and metal 2 is 8.74 µm. To ease the integration into a system and give a well-defined border for the antenna, a ground wall is placed 100 µm around the antenna itself. The chip micrograph is shown in Fig. 5.10(b). The antenna is built in two versions: The first is directly connected to an on-chip balun to ease measurements and is shown here. A second version has a differential pad presented in [15]. In order to 3D-print on the antenna, the chips are glued to a carrier. This carrier is mounted into a *Boston Manufacturing BMF3D* enhanced stereolithography (SLA) printer, which in this setup can print features down to 1 µm in x- and y- direction and 5 µm in z-direction. The alignment of the 3D-printed structure is done with the integrated vision system utilizing the same optics as the laser for the process. After alignment, the structure and the shadowing structures are printed in situ.



(a) 3D-Printed (b) Glass Resonator

Figure 5.14: Top and side view of the two different resonators designed.

The antenna is small enough to avoid lateral stitching of the scan fields to avoid issues at the boundary. The antenna with the 3D-printed structure is shown in Fig. 5.15(a). After printing, the structure is mounted in a sputtering system where the surface is first activated by a thin layer of titanium and chrome and finally sputtered with copper. The final thickness is 600 nm. The sample after the metallization step is shown in Fig. 5.15(b). After sputtering, the shadowing structures of the antenna are removed manually, revealing the physical structure. This is shown in Fig. 5.15(c).
During the integrated circuit (IC) design, an oversight was placing the probe pad close to the antenna. As shown in in chapter 3, the used wafer probes radiate significant power and influence the antenna pattern measurement significantly. To compensate for this issue, 10 mm of CPW line on alumina is connected to the probe pad via bond-wires to move the probe further away from the antenna. The CPW loss is measured separately and removed from the measurement results. While this helps reduce the wafer probes' effects and influences, the CPW line itself and the bond-wire transition add issues to the measurement. In order to keep the distance between the pad and the CPW short, the edges of both the IC and CPW lines are carefully ground down to a perfect 90°



(a) Printed (b) Metallized

(c) Without shadowing (d) Final assembly

Figure 5.15: The different manufacturing steps of the 3D-printed antenna.

angle. Grinding the sides of the samples allows for a small gap of less than 10 µm between the two parts. The distance is bridged with 17 µm of aluminum bond-wire. The final assembly is shown in Fig. 5.15(d). The alumina of the CPW has a thickness of 254 µm while the IC has a thickness of 300 µm. To compensate for the height difference, a metal shim is laser cut and glued with conductive die-attach film underneath the CPW line. This yields a maximum height difference of 5 µm. The final assembly of the glass resonator design is shown in Fig. 5.16.

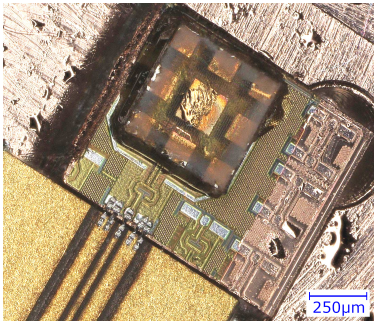


Figure 5.16: Glass resonator assembled.

5.2.3 3D-Printed Resonator Measurement

The 3D-printed resonator shown in Fig. 5.14(a) is measured. Fig. 5.17 shows the pattern in the E-plane, and Fig. 5.18 shows the pattern in the H-plane. The CPW line loss is de-embedded from the measured gain. In the E-Plane, a good match between simulation and measurement is achieved for 240 GHz and 260 GHz while the pattern at 220 GHz is severely reduced. The present ripple in the H-plane is an artifact of the probe body reflecting the radiated energy, as evident from the small ripple angle. As the ripple is heavily frequency dependent, no proper gain over frequency value can be given directly. To compensate for the ripple, the average gain in a 15° window around boresight is calculated and plotted in Fig. 5.19. There is an agreement for the simulation and measurement for some frequencies, especially the high-frequency roll-off towards 300 GHz, there is a reduction in gain around 230 GHz and 265 GHz.

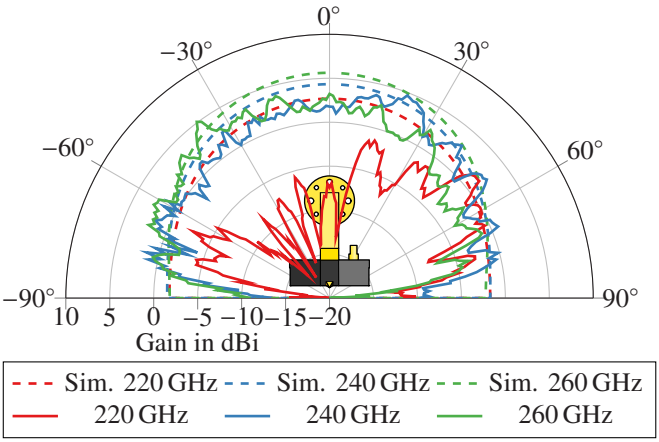


Figure 5.17: E-plane field pattern of the 3D-printed resonator antenna.

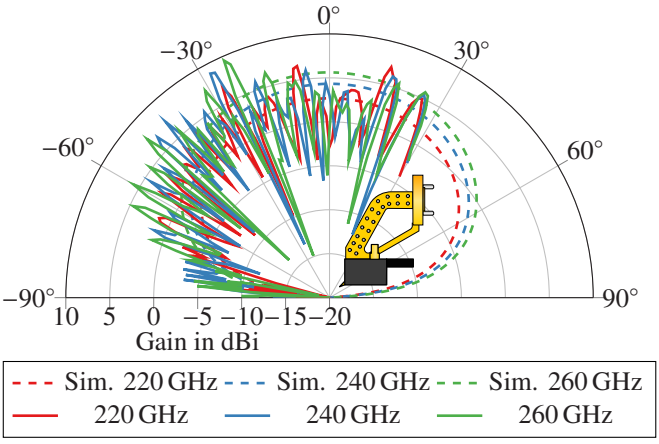


Figure 5.18: H-plane field pattern of the 3D-printed resonator.

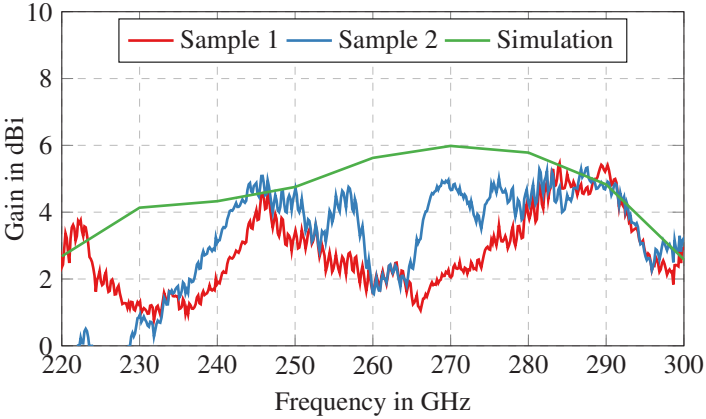


Figure 5.19: Measured and simulated gain at boresight of the 3D-printed resonator. Measured are two different samples.

5.2.4 Glass Resonator Measurement

Next, the glass resonator design is measured. Fig. 5.20 and Fig. 5.21 show the measured E-plane and H-plane patterns. In the E-plane, a strong tilt to 30° is visible, which should not be possible from the design. The antenna and resonator are strictly symmetric; they should have a symmetric pattern. Here, the root cause is most likely a shift in the alignment of the resonator to the antenna itself. Concerning the gain over frequency at boresight, shown in Fig. 5.22, a reduction in gain of around 1 dB is visible up to 275 GHz, after that the radiated power drops significantly, which should not be the case from the simulation.

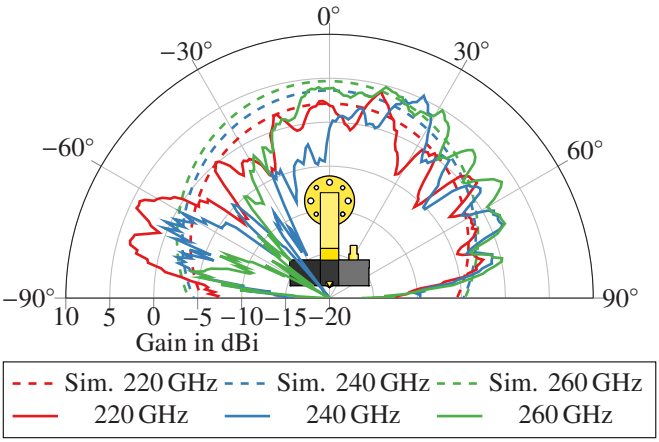


Figure 5.20: E-plane field pattern of the glass resonator antenna.

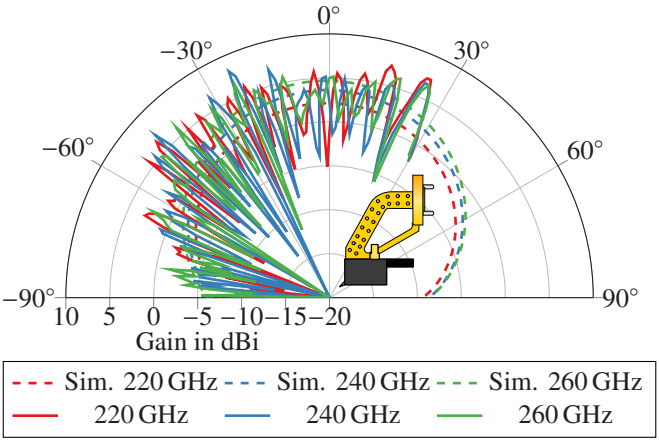


Figure 5.21: H-plane field pattern of the glass resonator antenna.

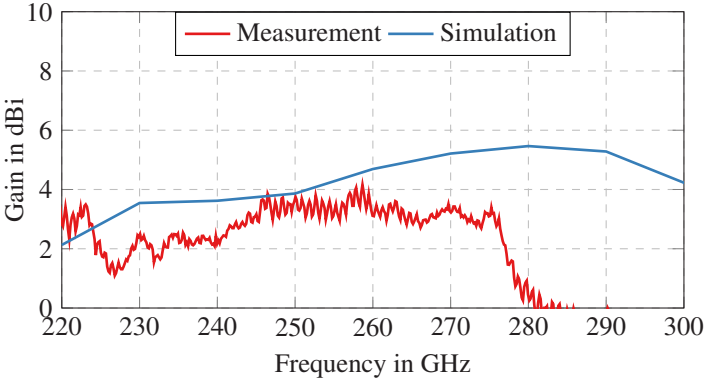


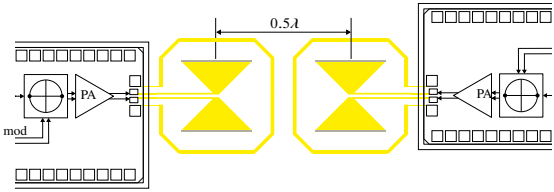
Figure 5.22: Measured and simulated gain at boresight of the glass resonator antenna.

5.3 mmWave Phased Arrays

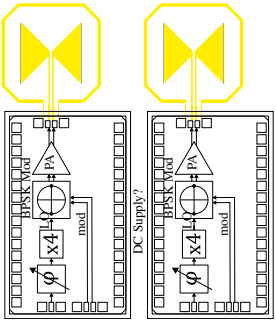
Phased arrays are based on the superposition of multiple single antennas. Due to interference, an increase in radiation power in one direction is observable. The array factor is dependent on the distance between the antenna elements and the phase of each antenna. Consequently, having an adjustable phase for each antenna allows for an electronically steerable beam. Phase steering works well for pure sinusoids. However, real signals have a bandwidth. With increasing relative bandwidth, the targeted steering angle, and array size, the steering error becomes excessive, and phase-steering is not possible anymore. In such a case, true time delay or digital time correction becomes necessary.

An optimal grating lobe free distance of the antenna elements is $\lambda/2$. This distance at 246 GHz is 0.61 mm, which is smaller than the edge of the realized MMIC with 800 µm. Hence, placing many elements together is not only a challenge in antenna design but also a routing challenge. One way to overcome this is by placing many transmitters on a single chip, reducing additional elements like DC pads. However, this increases chip size and cost and has other detrimental effects. DC routing on-chip can be problematic and cause significant performance loss, as reported in [KAKM23].

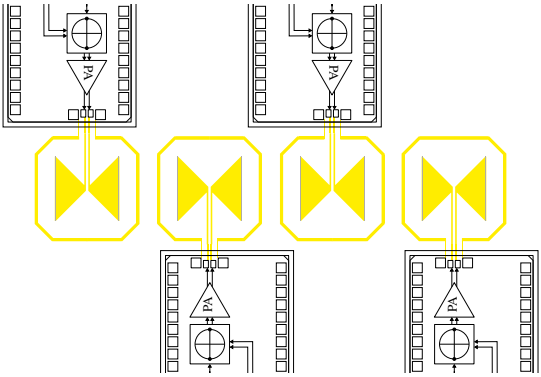
Investigating possible arrangements yields the three cases presented in Fig. 5.23. The first sees two MMICs opposing each other with the antennas in the middle. This yields a possible configuration where the antenna spacing can reach 0.5λ. However, this configuration does not allow a larger array than 1x2, highlighting the challenges of antenna distribution. The naive approach of aligning two or multiple chips next to each other is shown in Fig. 5.23(b). The challenge is the antenna spacing and the DC routing. With the DC pads along the side of the MMIC, a significant space between two MMICs is necessary to route the different signals. Optimizing this yields a configuration shown in Fig. 5.23(c). Here, the rotation symmetry of the antennas is used to place the MMICs alternatively on opposing sides. This leaves more routing space between the MMICs, alleviating some issues in achieving proper antenna spacing.
This array configuration, however, also suffers from the inherent 1D limitation. Alternations of this or the concept in Fig. 5.23(b) were used in [AdGW+22]. There, a 1D-array of side-firing Vivaldi antennas was used, which still faces the same challenges of providing DC and BB signals to the chip in two of the three space dimensions. For future 2D-phased array systems, better RF signal distribution has to be investigated to allow off-chip antenna routing and more flexibility.



(a) Opposite Side



(b) Same Side



(c) Interleaved Side

Figure 5.23: Possible array configurations.

6 RF Interconnects for Chip to PCB and Chip to Antenna Connections

Targeting very wideband systems poses challenges on multiple layers. The system, as shown in Fig. 1.1, has multiple RF interconnects for the different parts of the assembly. To push up to 100 Gbit s^{-1} into the MMIC, the baseband transition has to work correctly up to at least 50 GHz analog bandwidth. Further, the LO signal at 64 GHz must be routed and distributed. The other significant challenge is the interconnection of the RF output from the MMIC to the antenna. Due to the high operating frequency, even small parasitic elements limit the usefulness of many approaches. A novel solution using differential bond-wires has been developed to solve the interconnect problem. Lastly, all these interconnects must be integrated reliably into a working mm-wave assembly combining multiple transmitters and antennas into a phased array. The system consists of three distinct parts that need to be connected. The first part is the MMIC itself, the second is the antenna, and the third is the carrier PCB. Traditional connectors bring the DC and RF signals from the measurement equipment through cables into the PCB. However, the connection between PCB and MMIC is a challenge. Two concepts are widely adopted: wire bond and flip-chip packaging. While flip-chip packaging promises higher connection bandwidths and integration density, it suffers from increased demands on the PCB, especially an additional manufacturing step in MMIC production to create the necessary bumps. This extra effort ruled out flip-chip for this specific application. Bond-wire interconnects without special attention and design suffer from the high impedance mismatch and inductance of the bond-wires. However, previous works showed that these hurdles can be overcome to achieve wideband connections bridging realistically achievable gaps between MMIC and PCB [9].

The used PCB stackup is shown in Fig. 6.1. In total 8 metal layers are possible with blind micro-VIAs. The micro-VIAs cannot be stacked. Three cavities are possible on the top side. They range from the top most layer down to layer

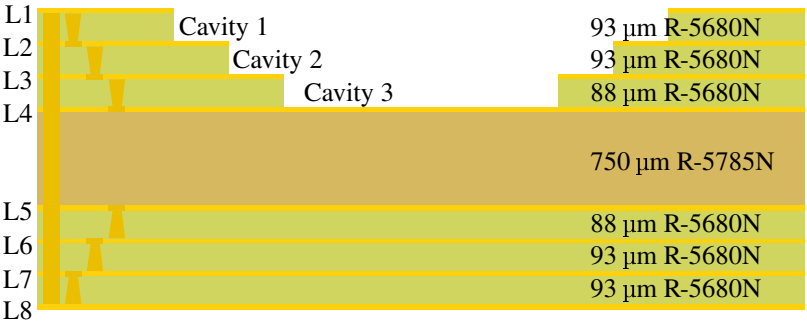


Figure 6.1: PCB-Stackup with annotated layer thickness and cavities.

two, three and four. The bottom of the cavity has to be fully metallized for the detaching process, hence no signal conductors can be placed on the bottom of the cavity. The three ranges allow for cavity depths of roughly 100 µm, 200 µm and 300 µm to allows for flush mounting of the MMIC and decoupling caps.

6.1 Wideband Coax to PCB Transitions

To feed in the various baseband signals and the LO a wideband transition from 1.85 mm coax to the PCB is necessary. Further, due to the large number of necessary connections, also an economical solution is sought. After identifying the correct connector part two additional problems needed solving to ensure proper operation from DC to 67 GHz. The first issue is additional capacitance underneath the signal pin due to stray fields, which is compensated by a cut in the ground plane. The second issue is additional inductance in the path for the return current. This is solved by adding a dense VIA fence and using side-plating. By exposing the ground plane to the side of the PCB it can be soldered to the connector, reducing the length the return current has to travel. Lastly this approach also ensured higher mechanical stability and prevents cracking of the solder while mating of the connectors.
Fig. 6.2 shows the geometry of the implemented connector transition. The ground cut is denoted **A**. The combined through and blind VIAs for the ground currents are denoted **B**, and the side plating of the PCB is denoted **C**. To verify the transition, a thru line is assembled and measured. The S-parameter

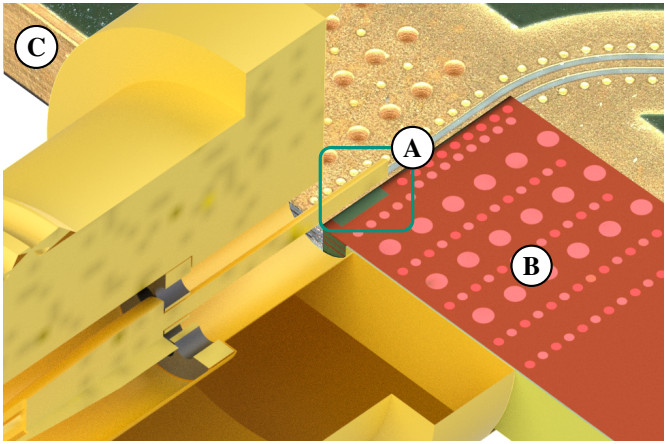


Figure 6.2: Wideband transition from the RF connector to the PCB [5] © IEEE 2024.

results are shown in Fig. 6.3. The input match is better than 10 dB over the entire frequency band. The 35 mm long microstrip line measures a loss of 3 dB at 67 GHz, resulting in a loss of 0.081 dB mm^{-1} at 67 GHz including the connectors. To further analyze the transition and validate the design, the time domain reflectometry (TDR) is calculated from the measurement and plotted in Fig. 6.4. Unlike the simulations, a dip below 50 Ω at the transitions is present, which can be attributed to excess solder causing an increase in capacitance. The microstrip line has an impedance of 57 Ω, resulting from a thickness mismatch between simulation and measurement of the prepreg layer.

6.2 On-PCB RF Signal Routing

While the application with a single MMIC is rather simplistic, building a phased array imposes some new challenges for signal distribution. Firstly, the LO signal has to be split and routed to all MMICs coherently. Secondly, the baseband signal has to be routed equally in all channels to avoid inter-channel skew, which worsens the result of the phase steering. To realize the power splitting, a few constraints have to be considered. Firstly, the operating range is only 60 GHz to 67 GHz. Secondly, the necessary power at each

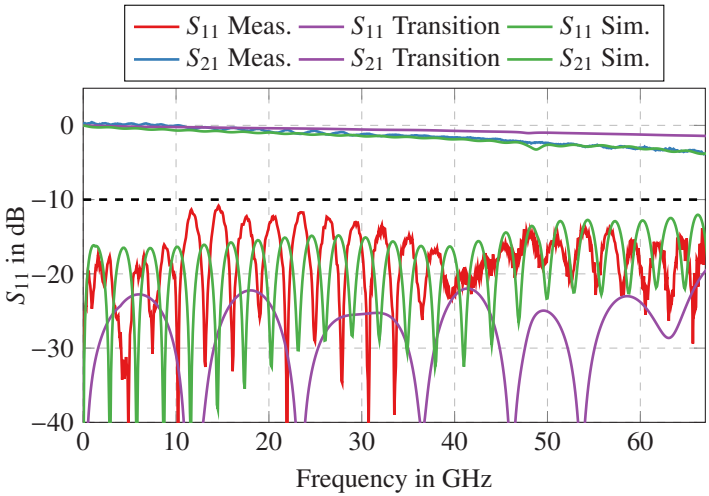


Figure 6.3: Measured S_{11} and S_{21} of the connector thru and simulated relfection and transmission of the transition itself [5] © IEEE 2024.

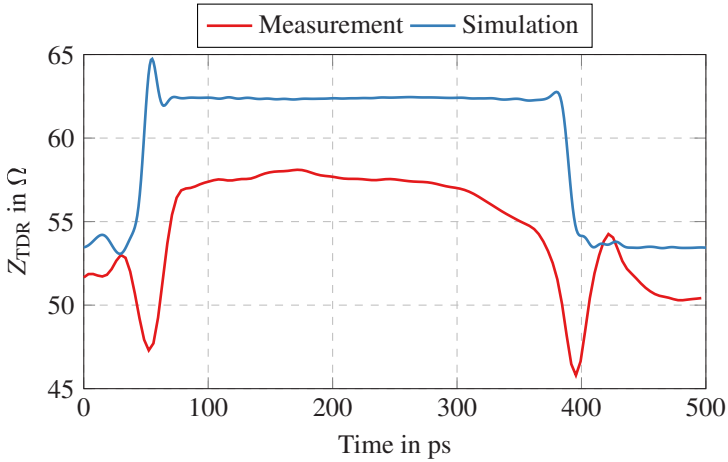
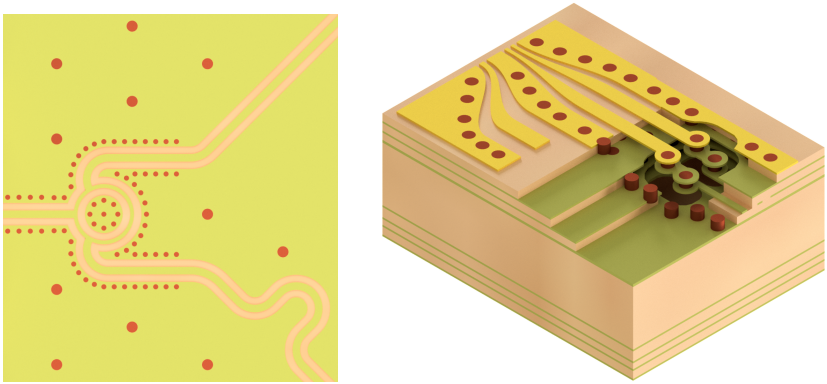


Figure 6.4: Measured and simulated TDR for the connector-microstrip-connector test structure [5] © IEEE 2024.

MMIC is −10 dBm. Hence, the input power has to be strong enough to drive the power splitter and compensate for the routing losses. Different solutions are investigated: external laboratory grade power splitters, surface mounted device (SMD) packaged resistive power dividers, the classical wilkinson, and a rat race power splitter [MA89]. The economy of the measurement setup imposes a significant challenge. This ruled out external power splitters due to the significant cost and complexity. SMD-type resistive power splitters offer a large bandwidth. However, they also impose high costs in both procurement and assembly. The Wilkinson divider, while very much suited, necessitates an expensive resistor and complicated assembly process. Left is the rat race splitter, which offers a simple solution for the problem of splitting the LO signal. The geometry is shown in Fig. 6.5(a). The ring has a diameter of 1.5 mm and a track width of 100 µm. The grounded CPW line coming from the connector and feeding the MMICs is 200 µm wide with a 200 µm gap. Due to the internal LOs phase steering, there is no direct necessity for an equal phase of the LO signal at all MMICs. However, to prevent issues, a length matching of the LO lines is implemented using rounded meanders. A test structure is assembled, and the transmission through the splitter is measured. The results are shown in Fig. 6.6. The design is centered around 64 GHz, with a lower cutoff of 40 GHz. The splitter shows an insertion loss of 3.4 dB per branch in the simulation, as shown in the green and purple lines. Feeding lines and connectors are necessary to measure the splitter. Thus, the simulation, including these elements, is also shown in dashed lines for proper comparison. The realized samples show reflection and an increased loss over the simulation. Further, a slight asymmetry is present. The asymmetry is due to the RFs connectors, as the splitter and feeding lines are mirror symmetric. The feeding lines, in theory, add 3 dB more loss, and the measurement shows a loss of an average of 4 dB. Overall, the splitter operates as expected and within performance and manufacturing tolerances.

Due to the LOs routing occupying the PCB top layer, the baseband signal differential lines need to transition into the PCBs. Further, the MMICs are tested for data rates exceeding 50 Gbit s^{-1}, necessitating the careful design of the differential lines to minimize skew, offset, and band-limitation. A differential microstrip to stripline transition is necessary to achieve the PCB transition. The principle construction is shown in Fig. 6.5(b). The main challenges are compensating the additional capacitance by the VIAs rest ring, reducing ground return inductance, and minimizing coupling between LOs and



(a) Rat Race Splitter (b) Differential Stripline Transition

Figure 6.5: Layout of the realized rat race splitter and differential wideband transition into the PCB as a stripline [4] © IEEE 2024.

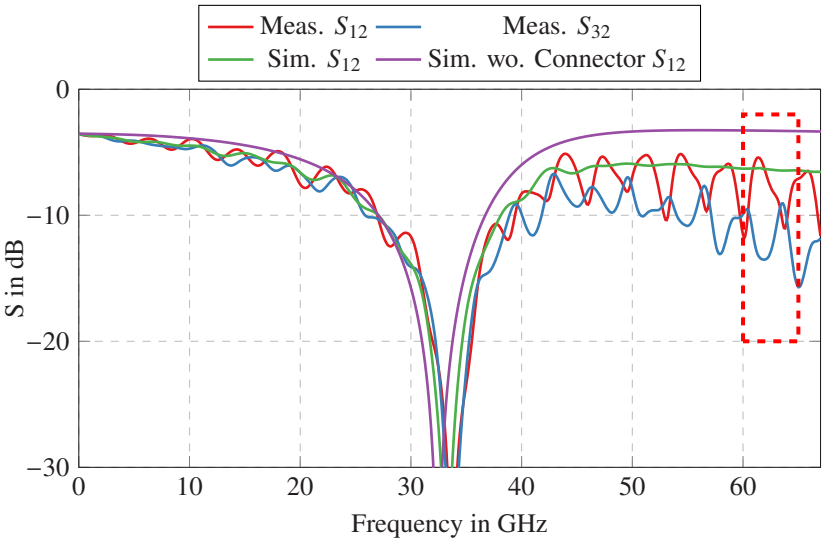


Figure 6.6: Measured and simulated S-parameters of the rat race power splitter. The simulated S_{12} and S_{32} are equal and hence only one trace is shown [4] © IEEE 2024.

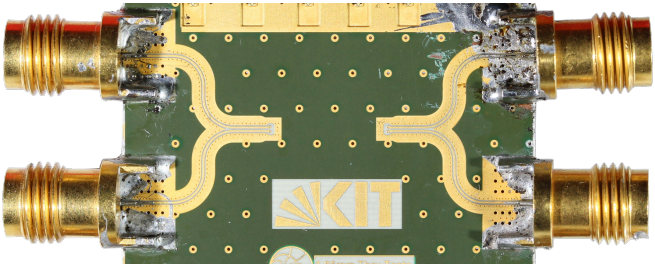


Figure 6.7: Test sample for the differential thru with the transition into the PCB [4] © IEEE 2024.

baseband. This is achieved by adding VIAs shielding around the transition and optimizing the ground profile around the signal VIAs. Adding a ground cut underneath the VIAs significantly reduces parasitic capacitance. A thorough test structure is measured to evaluate the transition. The assembly is shown in Fig. 6.7. The simulated and measured response for this thru test structure with the VIA transition into the PCBs back to back is shown in Fig. 6.8. The simulation shows an input return loss of less than −10 dB up to 42 GHz and an acceptably flat insertion loss. However the measurements show, that the input match exceeds −10 dB already at 32 GHz and an excessive loss after 50 GHz. Observing the impedance step response of both simulation and measurement presented in Fig. 6.9, a higher differential line impedance in the section connecting the RFs connectors to the stripline transition is present. This worsens the input match significantly. The root cause for this is suspected to be a change in prepreg layer height. The design uses a 89 µm prepreg layer, which can, however, be significantly higher due to the solid ground plane [14]. The transition is decent and shows only a slight capacitive behavior, less than in the simulation.

6.3 Bondwire MMIC to PCB Connection

Interfacing the MMIC with the PCB is done using bond-wires. Reactive matching was not an option to ensure wideband operation. Instead, the impedance profile of the feeding microstrip lines on the PCB is tapered to ensure wideband operation. Further, the height difference between the PCB and the MMIC

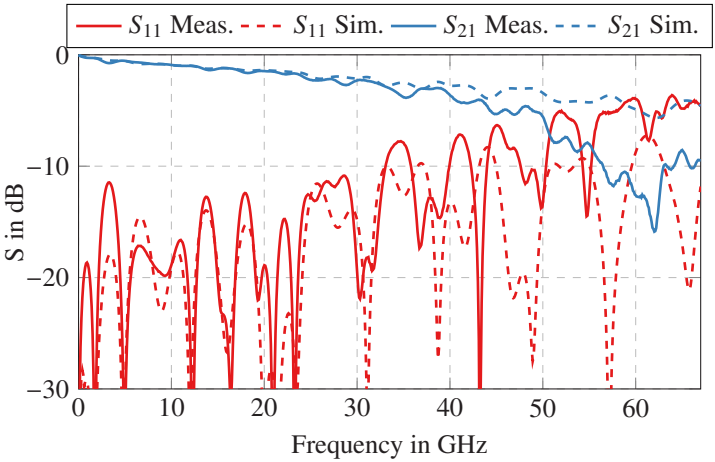


Figure 6.8: Measured S-parameter of the differential transition into the PCB [4] © IEEE 2024.

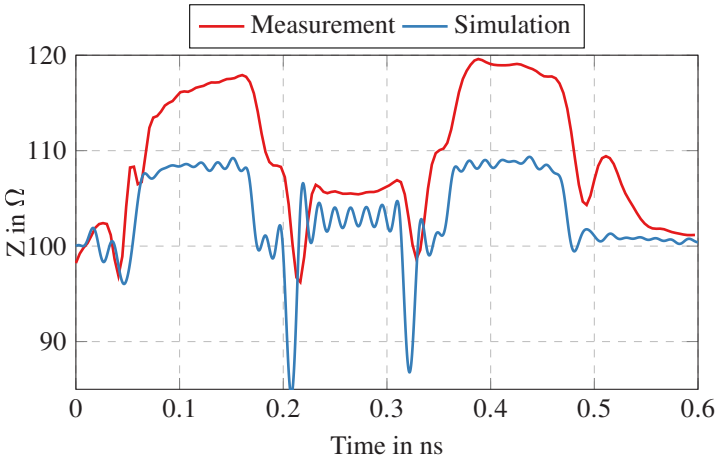


Figure 6.9: Measured and simulated TDR of the differential stripline transition [4] © IEEE 2024.

surface has to be minimized. This is done by creating a cavity in the PCB by selectively removing substrate material during manufacturing. However, the depth of the cavity is defined by the height of the used substrate layers, as evident from Fig. 6.1. The final depth of the cavity is about 80 µm larger than the height of the MMIC. To compensate for this, a laser cut metal shim is introduced using a picosecond laser.
Fig. 6.10 shows the cross-section of the assembly. The differential baseband lines, denoted **A**, are tapered using a sinusoidal function from a line width of 160 µm line and 120 µm space down to a width and space of 50 µm. The LO signal, denoted **B**, is brought to the chip with another sinusoidal taper bridging the distance and keeping a constant width ground layer between the LO and BB. This ground strip is wide enough for a VIA fence between LO and BB, ensuring shielding. Due to the surface of the MMIC being flush with the PCB surface, the length of the bond-wires is minimized. This allows for an easy and straightforward bonding of the samples.
The metal shim used to bridge the height gap is shown in Fig. 6.10 and denoted **C**. The shim is cut out of a copper foil by laser ablation. The shim contains holes for the excess glue to flow into, preventing overspill over the edge of the cavity. Further, the copper shim ensures proper thermal coupling to the ground layer of the PCB. During operation, the chip did not exceed a 25 K temperature increase over ambient measured by on-chip temperature diodes.
The manufactured cavity was smaller than the design requirements, causing the chip not to fit. This excess PCB material and copper buildup during plating is removed by laser ablation using fiducials already present on the PCB. With this process, a minimal gap of 25 µm around the chip could be achieved, easing alignment to the RF and DC bond pads and reducing rounding artifacts in the corners from the PCB manufacturing.
To validate the realized transition, the input return loss of both LO and BB are measured and shown in Fig. 6.11. Both LO and BB are open at low frequencies due to the internal circuit in the MMIC. The base of the transistor is directly exposed, yielding the observed behavior. The LO transition shows a resonance at 40 GHz and 60 GHz, which is however no issue for the application. The BB input was measured for differential and common mode input match, denoted S_{dd11} and S_{cc11} respectively. The transition has a very low common mode rejection. However, both measurements are similar, indicating good symmetry in both differential signal paths.

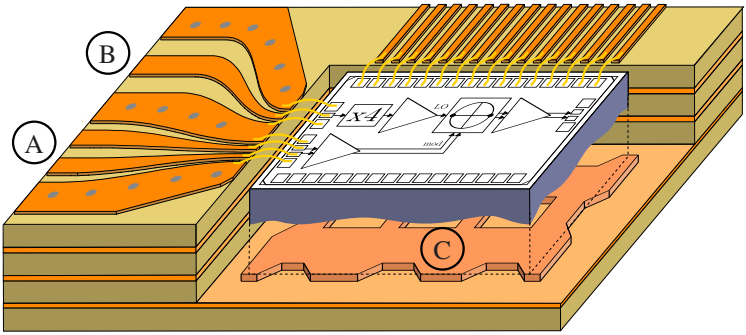


Figure 6.10: Cross section of the MMIC embedded in the PCB [5] © IEEE 2024.

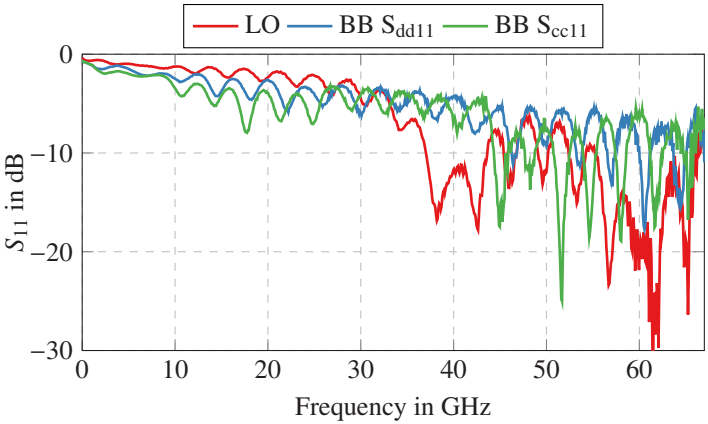


Figure 6.11: Measured S_{11} of the PCB to chip transitions. The differential port is measured for differential and common mode matching [5] © IEEE 2024.

6.4 Differential RF bond-wire Transition

As the last major packaging challenge, the connection between MMIC and antenna has to be realized. The MMIC and the antennas are separate parts and, hence, a few constraints have to be considered. Firstly there will always be a gap between MMIC and antenna. Empirical evaluation yields a minimum gap of 15 µm for specially prepared samples and a typical gap between 50 µm and 100 µm to account for glue spill-over and angled dicing edges. Secondly, the alignment of the top surfaces cannot be guaranteed to be perfectly parallel. Hence, the solution sought should be able to compensate for a reasonable tilt. An obvious solution is using bond-wires, which are already used within the packaging concept. However, bond-wires suffer from inherent inductance, creating a low-pass behavior limiting the applicable frequency range. Previously published solutions to compensate the inductance include capacitive matching structures [VSY+15], [BRD+11] or $\lambda/2$ self-matching [BGS+16]. An alternative presented in [TCE18] are coupled $\lambda/2$ bond-wires. Due to the reactive matching, these approaches again have limited bandwidth or see an increase in the occupied surface area and, hence, losses. An alternative approach are flip-chip interconnects [TMG+19]. These use short metallic bumps on the chip surface to minimize the distance between the two substrates. While it shows excellent electrical performance with measured bandwidths of up to 500 GHz [SDS+17], the associated requirements on the packaging ruled it out as a solution within this work.
Another recent approach that has been successful is 3D-printed interconnects using aerosol-jet printing [GRB+23]. In this process, the electrical contact is realized by printing silver ink on the exposed pads to connect them. The major limitation of this approach currently is the inherently low conductivity of the silver ink and the necessary heat sintering step. The heat treatment is incompatible with other used glues and the PCB stacks up.
The last alternative published is quilt packaging [KKBF14]. In this technology, the two substrates are ground down to expose the metal at the edge, and the leftover gap is bridged by silver epoxy or solder. While promising the necessary grinding of the MMIC was deemed risky, the additional assembly constraints were demanding.

With a clear candidate, the bond-wire interconnect solution is investigated in detail. While many previous publications approach a bond-wire as a lumped

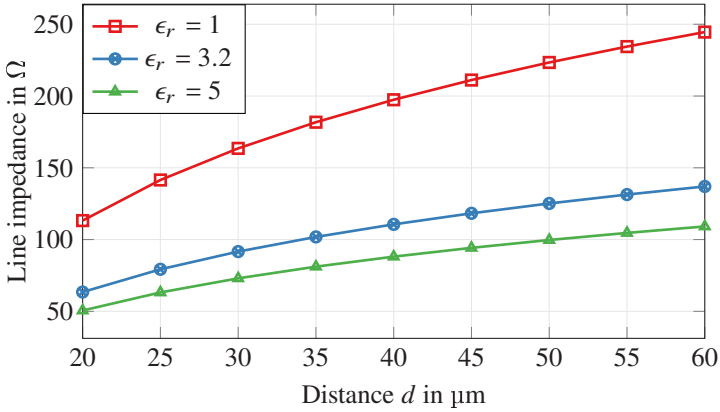


Figure 6.12: Line impedance of two parallel bond-wires with 17 µm diameter over the center to center distance d for different surrounding dielectric constants [15] © IEEE 2022.

element, assuming an inductance that needs compensation, the whole transition can also be viewed as a distributed element transmission line. Further, almost all publications concentrate on single-ended transitions due to measurement constraints. However, differential transitions might be capable of reducing the overall constraints as the targeted system impedance is 100 Ω instead of 50 Ω. Hence, as a starting point, the characteristic impedance of two parallel 17 µm bond-wires over their separation d is simulated and plotted in Fig. 6.12. It is evident that moving the two wires closer together increases the capacitance coupling and thus reduces the characteristic impedance. However, in the air, no physically achievable distance d would yield an impedance of 100 Ω. By filling the surrounding area with a dielectric, the capacitance can be increased, reducing the impedance. This is also simulated for an ϵ_r of 3.2, which corresponds to the dielectric properties of *PolyTec TC 430 T* [GWB+18], and an ϵ_r of 5, which corresponds to *Stycast FT 2850FT* [JSM18]. With an ϵ_r of 3.2 the 100 Ω can be achieved with a separation of 35 µm, which is below the empirically found limit of 38 µm. This limit is due to the placement accuracy of the bond-tool as well as the width of the tool itself. With an ϵ_r of 5 the 100 Ω impedance is reached with a separation of 50 µm, which is manufacturable. A further benefit of encapsulation is the additional mechanical stability and environmental protection.

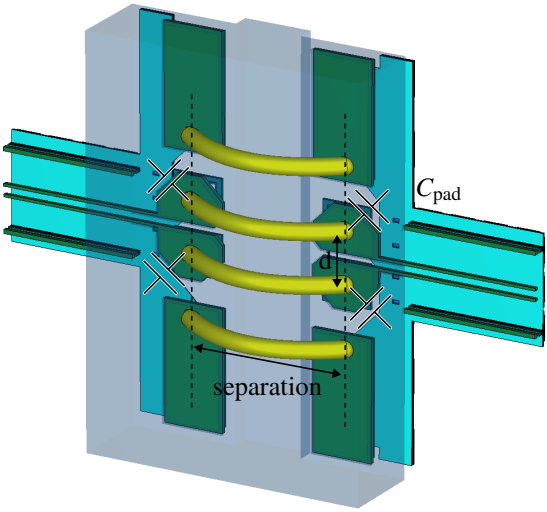
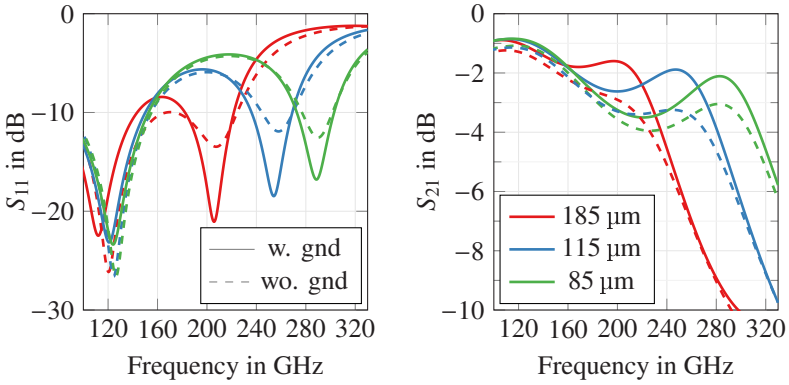


Figure 6.13: Simulation setup of the designed differential pad as well as the bond-wires with a separation between the center of the pads of 185 µm. Annotated is the pad capacitance. Modified from [15] © IEEE 2022.

Simulating the two bond-wires alone does not yield any information about the application's usability. To evaluate the usability in the application, a differential pad is designed in *IHP SG13G2* technology. The pad consists of a ground signal signal ground (GSSG) configuration with two signal pads that are as close as possible. The ground pads are technically unnecessary, as the differential signal only needs the two signal wires. However, it was deliberately added for bond testing during manufacturing, allowing DC and compensating some common-mode signals. The pad and the simulation setup are shown in Fig. 6.13. To accurately capture a real-world scenario, the simulation is repeated for three different separations between the pads, which are 85 µm, 115 µm and 185 µm. This corresponds to one on-wafer test structure and the application's best and worst-case separation value. Fig. 6.14 shows the simulated transmission and reflection of the test structure for all three separations. While in theory, the length should not play a role, as the impedance is kept at 100 Ω, there is a significant influence of the length visible. Further investigation shows this is due to excess pad capacitance, forming a π-style filter with the impedance



(a) Input Match

(b) Insertion loss

Figure 6.14: Simulated S_{11} and S_{21} of the differential transition encapsulated with a glue with an ϵ_r of 5. The distance between the center of the signal bond-wires is 40 µm. The dashed lines are the simulation results without ground wires, in solid lines with ground wires [15] © IEEE 2022.

of the bond-wires. Optimizing the pad structure can help reduce this effect, but due to the manufacturing constraints in the CMOS process, there is only limited potential to gain. The other aspect visible from the simulation is the influence of the ground bond-wires. As shown in solid lines in Fig. 6.14, adding the ground bonds reduces the transmission loss by up to 1 dB and helps a little with the matching. Hence, all further analyses will also use the ground bond-wires. Lastly, by achieving a sufficiently short connection, the upper-frequency limit of the transition can be shifted above the system's maximum operating frequency, making the approach viable for the system.

6.4.1 Fabrication

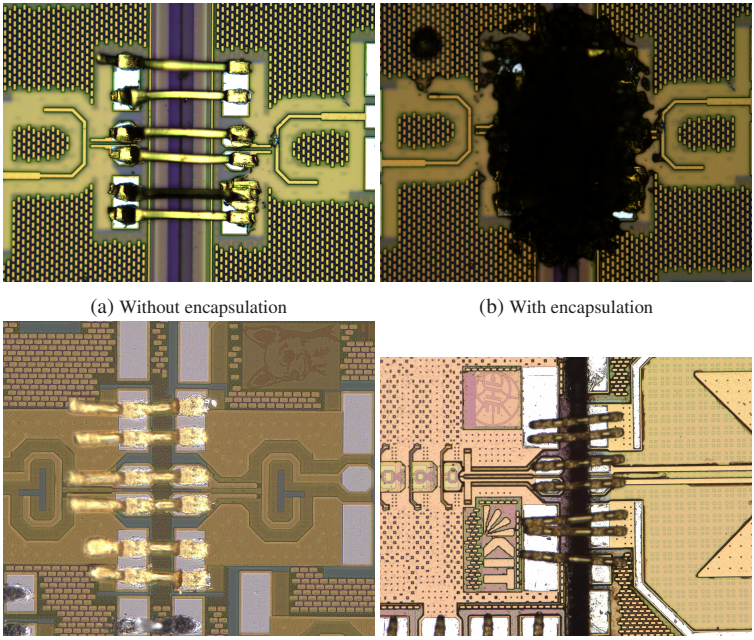
To validate the transition, a CMOS IC is manufactured containing the differential pad, a balun and a GSG pad. To measure the differential transition two baluns are bonded to each other. However, this superimposes the balun's response to the measurement, which has to be accepted. Fig. 6.15(a) shows the realized balun and pad.

Two chips are glued back to back with their seal ring around them on a carrier. The chips are carefully aligned to avoid excessive horizontal offset. Next, the transition is bonded with a wedge-wedge tool and 17 µm gold wire. The three bonded transitions shown in Fig. 6.15(a), Fig. 6.15(c), and Fig. 6.15(d) show the repeatability of the process. After bonding, the transition is encapsulated in either Polytec TC 430-T or Stycast 2850FT with catalyst 24LV.

The designed transition is affected by the many process variations present. Hence, a full characterization is only possible for a specific use case. However, the main difference is only the transition length, which should not change anything except for changing losses. Hence, the back-to-back transition in Fig. 6.15(b) checks the validity. The output of the DUT is connected to a balun for on-wafer characterization. Hence, the output match can be measured and compared to the simulation to validate the correct connection.

6.4.2 Measurement

Fig. 6.16 shows the measured and simulated S-parameters of the back-to-back interconnect shown in Fig. 6.15. The simulation includes the baluns used up to the microstrip line connecting the single-ended pad, which is set to the pad separation achieved with sample 1. Two samples were built and measured before, denoted a, and after encapsulation, denoted b. Due to the process variations, the two samples have a slightly shifted resonance frequency. This variation is also visible in the transmission. Adding the encapsulation shifts the resonance to lower frequencies, as expected. This causes the transmission to enhance by 1.5 dB from 250 GHz on. However, sample 2 shows a 1 dB increased loss after encapsulation in both transmission and reflection compared to sample 1, which is not as severe without encapsulation. A decent agreement between measurement and simulation can be found. However, the process has some variations in the placement and length of the bond-wires that must be taken into account in the simulation.
The loss for sample 1 is better than −8 dB in the frequency range from 210 GHz to 280 GHz with a flat response with only 2 dB of variation. This is contrary to the simulations shown in Fig. 6.14, which indicate a much steeper drop in the transmission from −2 dB down to below −10 dB. Also, the simulation before encapsulation shown in Fig. 6.16 has distinctively lower loss by about 2 dB but follows the overall shape of the measurement. After encapsulation, the



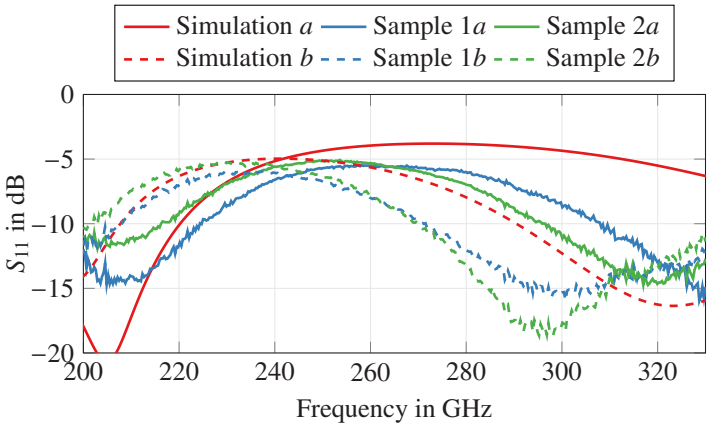
(a) Without encapsulation (b) With encapsulation

(c) On-chip bond (d) DUT bonded to the antenna

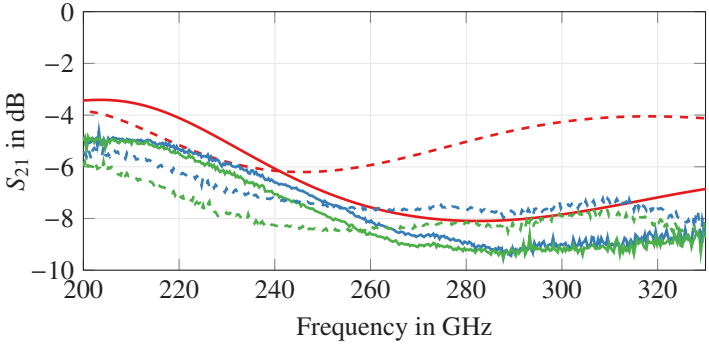
Figure 6.15: Two baluns connected back-to-back to measure the transition shown in (a) and (b). The pad separation measures 183 µm. (c) and (d) show two connections between the DUT and balun or antenna respectively [15] © IEEE 2022.

simulation would indicate an improvement of about 4 dB, which is not present in the measurement. This results from additional losses in the bond-wires not captured in the simulation.

Each balun has approximately 1 dB of loss in the target band, meaning the fabricated transition itself has a loss of better than −6 dB. The loss can be improved by tuning the separation and the dielectric used. The presented interconnect is comparable to or better than the measurements in [TCE18], which achieves a minimum loss of −5 dB at 220 GHz. Compared to flip-chip interconnects it has significantly more loss as the measured transition in [SDS+17] achieves 1.5 dB loss.



(a) Input match



(b) Transmission

Figure 6.16: Measured and simulated S-parameter reflection and transmission for the balun back-to-back structure. a denotes the measurement before, and b denotes the measurement after encapsulation [15] © IEEE 2022.

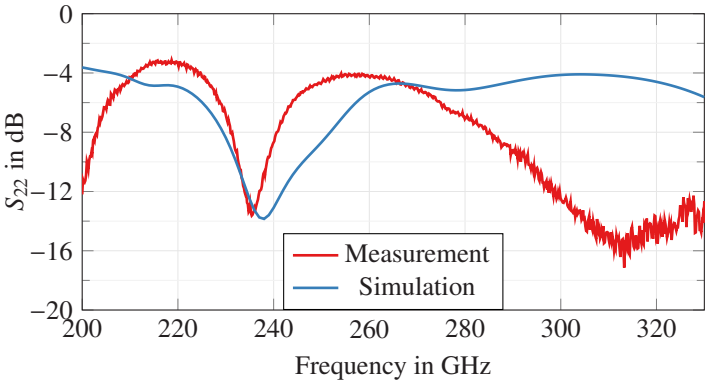
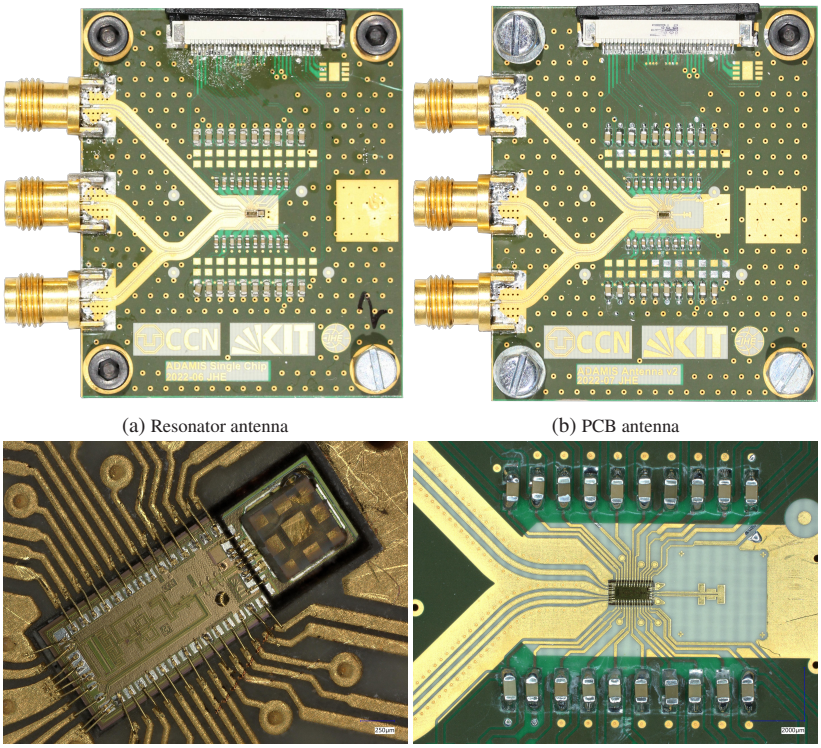


Figure 6.17: Measured and simulated output match of the DUT bonded to a Marchand balun [15] © IEEE 2022.

To evaluate the connection to the DUT, Fig. 6.17 compares the simulated and measured reflection. For the simulation, the transition with the fabricated pad separation is simulated and used as an S-parameter model in *ADS* in conjunction with the DUTs active circuit model. This approach achieves a remarkable match in the resonance frequency and return loss. However, some effects present are not captured. The resonance is much more narrow than simulated. Also, the drop above 270 GHz is not captured. The root cause for the mismatch could be modeling limitations in the DUTs PA stage. In the frequency range of interest from 210 GHz to 280 GHz, measurement and simulation match well, enabling the evaluation of the DUT.

6.5 Realized Transmitters

Using the introduced concepts, four different transmitter systems are realized, investigating different aspects of the system. To compare the PCB-based antennas to the resonator-based antennas, two transmitters with a single chip are realized featuring both antenna types. Fig. 6.18(a) shows the transmitter with the resonator-based antenna, which in the following will be referenced as *GR* for glass resonator. Fig. 6.18(b) shows the transmitter with a PCB antenna.



(a) Resonator antenna

(b) PCB antenna

(c) Micrograph resonator antenna

(d) Micrograph PCB antenna

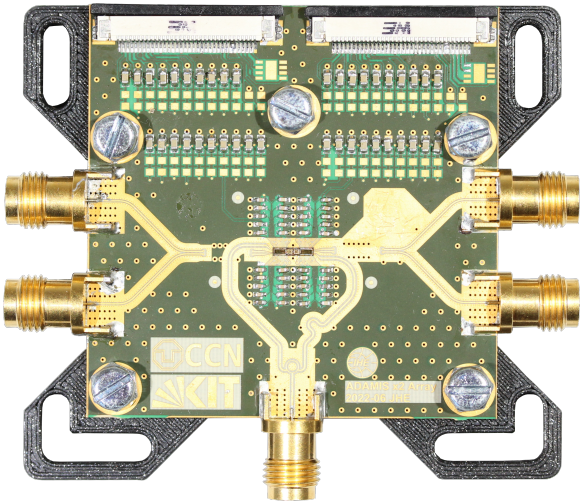
Figure 6.18: PCB photographs and close-ups of the MMIC for the two different single-chip modules [5] © IEEE 2024.

They share the same form factor and connectors. The RF connectors utilize the wideband transition presented in Sec. 6.1. The MMIC is embedded using the wideband bondwire transition presented in Sec. 6.3 and can be seen in Fig. 6.18(c) and Fig. 6.18(d). The antennas use the differential RF wirebond presented in Sec. 6.4.

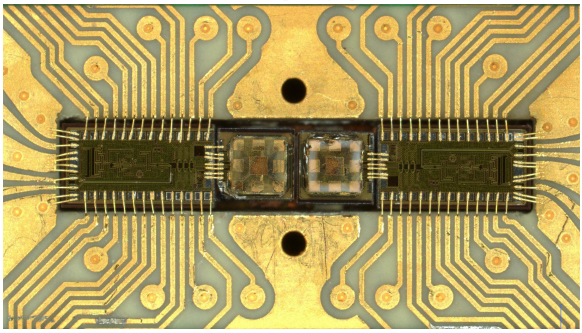
Extending the basic design of the single MMIC system shown in Fig. 6.18(a) gives a simple proof of concept phased array system with a 1x2 array configuration shown in Fig. 6.19(a). The two MMICs are back to back with the

antennas as close as possible. A significant hurdle during assembly is the correct orientation of all four ICs to each other, not only in the horizontal plane but also in height and angle. The glue must be dosed precisely to prevent overspill between the MMICs, increasing the distance or causing the glue to reach over the chips and contaminate the pads. The glass-based resonator is chosen for this setup as it is easier to integrate with the other necessary assembly steps, heat curing processes, and cleaning. Fig. 6.19(b) shows a closeup of the MMICs with their antennas. The baseband feed is symmetric, while the LO feed uses the rat race splitter and meander lines to compensate for the path difference of the rotated MMIC. As the LO signal has to cross the baseband line, both baseband feeds are brought into the PCB as a stripline mode.

Extending the array concept to a 1x4 array yields the array shown in Fig. 6.20(a). A main limitation of the antenna spacing is the routing of the DC signals. Multiple variants were investigated to solve the routing challenge. In the end, it was decided to choose the solution with the reduced assembly effort to minimize risk, and the antenna spacing is chosen to be 1625 µm or 1.33λ. This reduces the realized gain and increases the side lobes. Fig. 6.20(b) shows a close-up of the realized 1x4 transmitter.

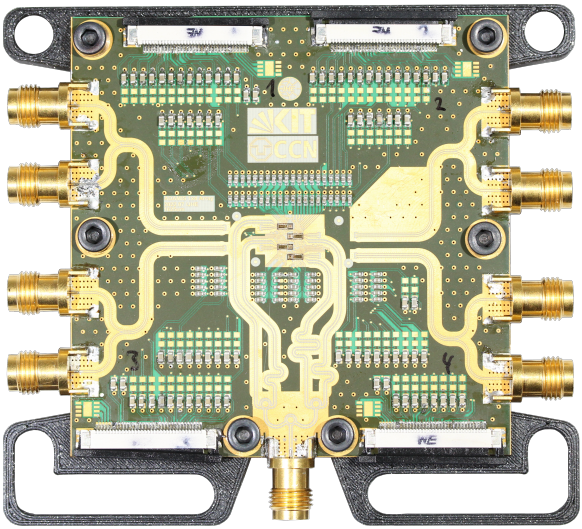


(a) PCB photograph

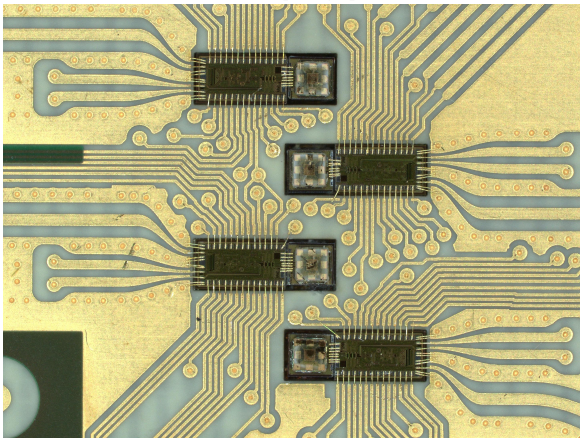


(b) Micrograph

Figure 6.19: Realized transmitter with 1x2 array based on resonator antenna [4] © IEEE 2024.



(a) PCB photograph



(b) Micrograph

Figure 6.20: Realized transmitter with 1x4 array based on the resonator antenna.

7 Full Transmitter Evaluation

Together with the system complexity the measurement and verification effort increases significantly. Even capturing a single tone RF behavior is not as straightforward. Due to the frequency translation in the modulator, classic S-parameter measurements become unfeasible. Further, the only accessible output of the system is the RF output of the power amplifier. Hence, all measurements contain the superposition of all effects of the LO generation, the modulator, and the power amplifier. Lastly, many systems using an on-chip antenna must characterize the system directly in free space, including even more effects and uncertainty [KAKM23]. A major benefit of the designed system presented in Sec. 6.5 is the use of off-chip antennas. Using an external balun, the MMIC could already be fully characterized in [2]. This information is now utilized to characterize the transmission behavior of the fabricated transmitter samples. First, the measurement setup is described, and the results for the four manufactured samples are discussed. The RF performance is captured as much as possible due to the superposition of the different measurement aspects. Lastly the BER is captured in many different scenarios to paint a realistic picture of the systems performance.

7.1 Measurement Setup

A major limitation already found in the analysis for the MMIC presented in [2] is the lack of appropriate measurement equipment matching the bandwidth. Especially signal generation of ultra-wideband binary sequences is challenging, as the rise-time of the output stage of either bit pattern generator (BPG) or arbitrary waveform generator (AWG) has to match the data rate. While in [2] a BPG with up to 64 Gbit s^{-1} was available, the measurements of the full transmitter had to be done differently due to lack of access to the BPG. Another limitation to [2] is the necessity to measure in free space. To achieve this, a

wideband fundamental mixer is used, which has limitations in the maximum data rate measurable as already presented in [2]. The samples are mounted on an antenna measurement system consisting of a two-axis rotating arm moving the receiver in a sphere with a radius of 36 cm around the DUT. The setup concept is shown in Fig. 7.1, and a photograph of the setup is shown in Fig. 7.2. The DUT and receiver LO are fed from two locked sources within a *Keysight N5247B* vector network analyzer (VNA). The baseband signal is generated by a *Keysight M8194A* AWG with 120 GSa s^{-1}. The output of the receiver is amplified by a *SHF 804 TL* wideband amplifier and sampled with a *Keysight UXR 1104A* 256 GSa s^{-1} oscilloscope for demodulation. Alternatively, the receiver's output is measured in the frequency domain with the *N5247B*. Multiple channels of the AWG are used to measure the phased array samples by outputting the same synchronous waveform. The steering is controlled via the phase shifter voltages.

A known source in the form of a *VDI VNAX WR3.4* combined transmit and receive (T/R) module is used to calibrate the receiver. This yields a received power as given in Eq. 7.1. The received power depends on the transmitted power $EIRP_{\mathrm{TX}} = P_{\mathrm{TX}}(f_{\mathrm{RF}}) \cdot G_{\mathrm{TX}}(f_{\mathrm{RF}})$, the free space path loss, the receiver antenna gain $G_{\mathrm{RX}}(f_{\mathrm{RF}})$ and the transfer function of the receiver $H_{\mathrm{RX}}(f_{\mathrm{RF}}, f_{\mathrm{LO}})$.

$$\begin{aligned} P_{\mathrm{RX}}(f_{\mathrm{IF}}) =& P_{\mathrm{TX}}(f_{\mathrm{RF}}) \cdot G_{\mathrm{TX}}(f_{\mathrm{RF}}) \cdot FSPL(f_{\mathrm{RF}}) \cdot \\ & G_{\mathrm{RX}}(f_{\mathrm{RF}}) \cdot H_{\mathrm{RX}}(f_{\mathrm{RF}}, f_{\mathrm{LO}}) \end{aligned} \tag{7.1}$$

$$\begin{aligned} P_{\mathrm{RX}}(f_{\mathrm{IF}}) =& EIRP_{\mathrm{TX}}(f_{\mathrm{RF}}) \cdot FSPL(f_{\mathrm{RF}}) \cdot \\ & G_{\mathrm{RX}}(f_{\mathrm{RF}}) \cdot H_{\mathrm{RX}}(f_{\mathrm{RF}}, f_{\mathrm{LO}}) \end{aligned} \tag{7.2}$$

$$H_{\mathrm{RX}}(f_{\mathrm{RF}}, f_{\mathrm{LO}}) = \frac{P_{\mathrm{RX}}(f_{\mathrm{IF}})}{EIRP_{\mathrm{TX}}(f_{\mathrm{RF}}) \cdot FPSL(f_{\mathrm{RF}}) \cdot G_{\mathrm{RX}}(f_{\mathrm{RF}})} \tag{7.3}$$

The RF signal f_{RF} is swept through the whole band, and the received power for different LO signal offsets f_{LO} is captured. As $P_{\mathrm{TX}}(f_{\mathrm{RF}})$ and $G_{\mathrm{RX}}(f_{\mathrm{RF}})$ are known, the equivalent isotropic radiated power (EIRP) is known. The free space path loss $FSPL(f_{\mathrm{RF}})$ and the receiver antenna gain $G_{\mathrm{RX}}(f_{\mathrm{RF}})$ are then absorbed into the transfer function $H_{\mathrm{RX}}(f_{\mathrm{RF}}, f_{\mathrm{LO}})$ of the receiver that is measured. With this information, the inverse can be calculated and used to calibrate the measurements.

The BER is measured by capturing 20 µs long data bursts with the real-time oscilloscope. These data chunks are then processed on the oscilloscope, and

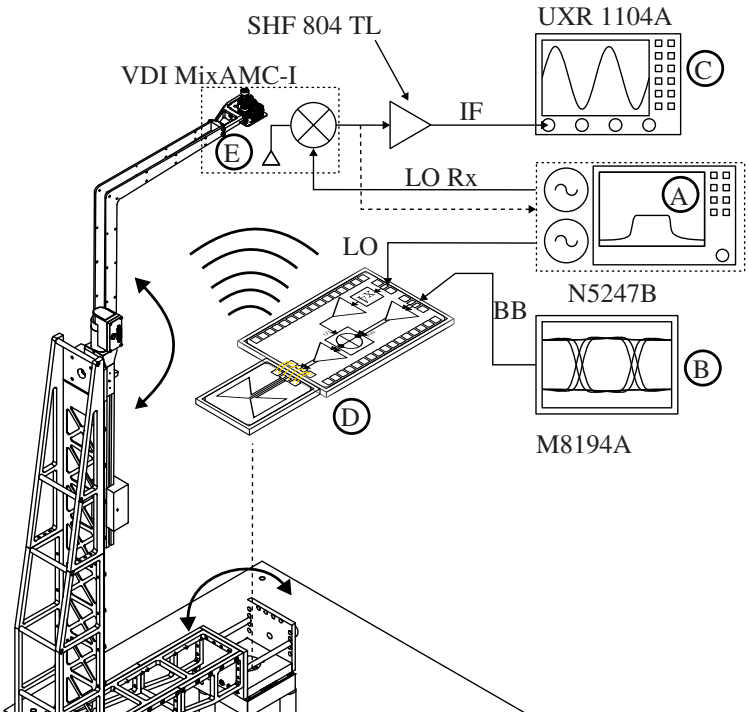


Figure 7.1: Schematic of the measurement setup showing the mechanical part on the left half with the rotating arm moving the receiver around the DUT and the used measurement equipment on the right side [5] © IEEE 2024.

the results are transmitted to a control computer. The demodulation signal chain is shown in Fig. 7.3. The IF signal from the receiver is down-converted digitally into an IQ stream without phase correction. The IQ data is then correlated to the transmitted sequence to recover the timing and phase over time. The phase has significant drift within one decoding frame and needs constant correction. Using this information, the IQ stream is corrected to have no additional phase shift, filtered using a matched filter, and equalized. The bits are extracted and compared to the transmitted sequence, calculating the bit error rate. All sources of the measurement setup are locked together with a 10 MHz reference. However, small drifts over time and mechanical

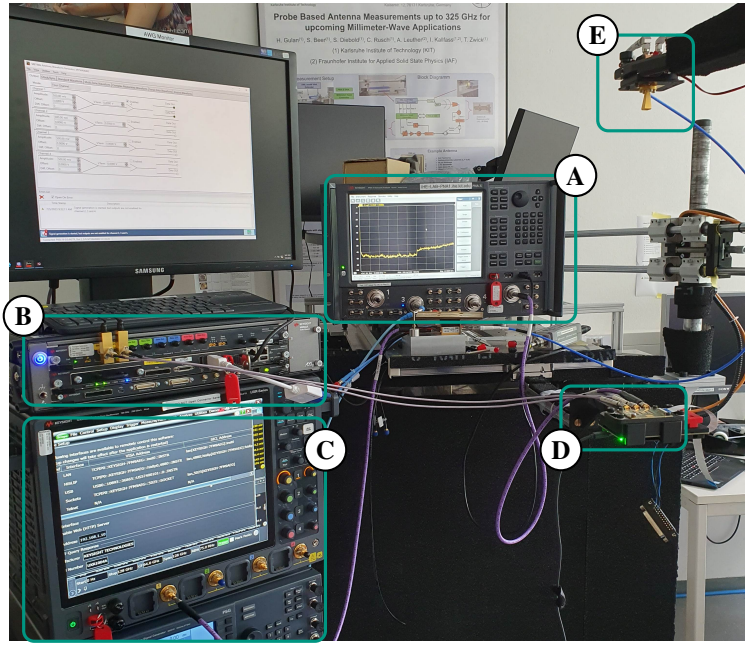


Figure 7.2: Photograph of the used measurement setup for the various RF and BER measurements [5] © IEEE 2024.

movement in the receiver cause a constant phase shift, thus rendering direct down conversion by adjusting the transmitter phase impossible for data rates above 4 Gbit s^{-1}.

7.1.1 DC Supply

The MMIC used needs 20 different DC voltages for its operation. Supplying these voltages also necessitates some degree of freedom to tune voltages for the best system operation and tuning of the phase shifter. To avoid complex assembly of the transmitter assemblies, no DC generation is included on the samples. Instead, the DC voltages and internal temperature diodes are brought out to a flat-flex connector (FFC). A custom DC supply is built featuring a

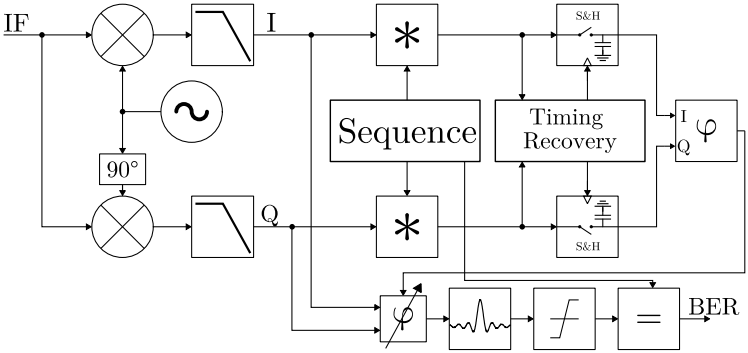


Figure 7.3: Block diagram of the receiving signal processing chain [4] © IEEE 2024.

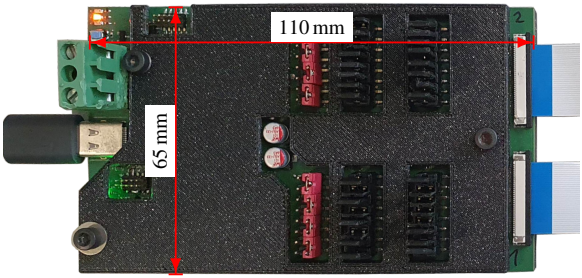


Figure 7.4: The used DC power supply. A 40-channel DAC and 8 LDOs provide the voltages for two separate chips through two FFC connectors [5] © IEEE 2024.

40-channel DAC part that can supply the different voltages for two MMICs. However, some parts of the circuit need more current than the DAC can handle; hence, low dropout regulators (LDOs) are added to supply these channels with a higher current. The system is powered and controlled through a universal serial bus (USB)-C connector, allowing easy integration with the control personal computer (PC). The DC supply is shown in Fig. 7.4. Internal current shunts further allow tracking of the current consumption in real-time.

To test the system, another adapter is assembled that allows the connection of a single MMIC to a 20-channel source measurment unit (SMU) with pA current measurement resolution, allowing precise evaluation of the systems and ensuring all bond-wire connections are made correctly. Tab. 7.1 lists the

Table 7.1: Measured DC currents for the different samples.

Name	Nom. Voltage	PCB S1	GR S2	x4 1	x4 2	x4 3	x4 4	x2 1	x2 2	Mean	Dev	%
vc-cBuffer	3.6 V	15 mA	13.86 mA	14.96 mA	14.81 mA	14.65 mA	14.65 mA	14.88 mA	14.5 mA	14.66 mA	0.25 mA	1.70
vccQuad	2.4 V	6.83 mA	6.1 mA	6.5 mA	6.39 mA	6.85 mA	6.71 mA	6.84 mA	6.98 mA	6.65 mA	0.24 mA	3.61
v1Quad	0.891 V	0.02 mA	0.02 mA	0.03 mA	0.02 mA	0.02 mA	0.02 mA	0.025 mA	0.024 mA	0.02 mA	0.003 mA	13.27
v2Quad	1.95 V	0.02 mA	0.03 mA	0.03 mA	0.02 mA	0.02 mA	0.02 mA	0.027 mA	0.023 mA	0.02 mA	0.004 mA	16.58
vc-cPhase	2.6 V	7.07 mA	6.64 mA	6.98 mA	6.83 mA	6.72 mA	6.8 mA	6.83 mA	6.78 mA	6.83 mA	0.1 mA	1.42
vinPhase	1.5 V	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0
ctrl-Phase	1.66 V	0.04 mA	0.05 mA	0.04 mA	0.05 mA	0.05 mA	0.04 mA	0.04 mA	0.04 mA	0.04 mA	0.01 mA	10.71
vbbPA	2.6 V	2.34 mA	2.08 mA	2.33 mA	2.28 mA	2.3 mA	2.26 mA	2.29 mA	2.29 mA	2.27 mA	0.05 mA	2.23
vbbIs	2.6 V	2.33 mA	2.07 mA	2.33 mA	2.17 mA	2.29 mA	2.26 mA	2.26 mA	2.27 mA	2.25 mA	0.06 mA	2.84
vccMod	3.6 V	9.35 mA	9.31 mA	9.4 mA	8.39 mA	8.79 mA	9.5 mA	9.41 mA	9.35 mA	9.19 mA	0.3 mA	3.25
modV2	2.85 V	0.34 mA	0.02 mA	0.33 mA	1 mA	0.37 mA	0.02 mA	0.017 mA	0.016 mA	0.26 mA	0.25 mA	93.09
modV1	1.734 V	0.02 mA	0.02 mA	0.02 mA	0.13 mA	0.02 mA	0.02 mA	0.02 mA	0.18 mA	0.05 mA	0.05 mA	94.19
ctrlMod	2.3 V	0.15 mA	0.07 mA	0.12 mA	0.12 mA	0.13 mA	0.12 mA	0.12 mA	0.123 mA	0.12 mA	0.01 mA	10.31
ctrl-Buffer	2.3 V	0.17 mA	0.11 mA	0.17 mA	0.15 mA	0.16 mA	0.15 mA	0.137 mA	0.157 mA	0.15 mA	0.01 mA	9.14
ctrl-Balun	2.48 V	0.01 mA	0.04 mA	0.01 mA	0.01 mA	0.01 mA	0.01 mA	0 mA	0.027 mA	0.01 mA	0.01 mA	64.53
vccPA	3 V	38.39 mA	29.28 mA	34.82 mA	36.1 mA	36.28 mA	36.11 mA	35.6 mA	36.29 mA	35.36 mA	1.65 mA	4.68
vccS2	3 V	23.69 mA	18.04 mA	21.65 mA	22 mA	23.4 mA	22.11 mA	21.6 mA	22.38 mA	21.86 mA	1.07 mA	4.90
vccIs	3 V	23.3 mA	18.31 mA	21.51 mA	22.83 mA	22.68 mA	22.03 mA	21.7 mA	22.46 mA	21.85 mA	1.01 mA	4.62
vc-cBalun	4 V	10.83 mA	9.84 mA	10.38 mA	10.18 mA	10.2 mA	10.58 mA	10.61 mA	10.07 mA	10.34 mA	0.26 mA	2.55
vbbS2	2.6 V	2.35 mA	2.06 mA	2.21 mA	2.26 mA	2.17 mA	2.26 mA	2.26 mA	2.27 mA	2.23 mA	0.06 mA	2.80
Power in mW		442.03	368.48	416.58	421.43	425.67	422.28	419.28	422.87	417.33	12.4	2.97

currents of the different samples and voltages to evaluate the manufacturing tolerances and internal bias networks. While the currents for the amplifier stages are within less than 5 % standard deviation of each other, the control voltages for various circuit parts have much more drastic deviations. This is partly due to manufacturing differences causing internal bias point shifts, but also PCB contamination and creeping currents play a role. Except for the sample with glass resonator, labeled *GR S2*, the consumed power is within 3 % of each other. The outlier has an issue with the power amplifier supply.

7.2 Single Chip Measurements

For better comparison, the samples with only a single MMIC are measured and evaluated first. This allows directly comparing the measurement results against the on-wafer measurements presented in [2].

7.2.1 RF Evaluation

In the initial measurement phase, a differential sinusoidal signal ranging from 1 GHz to 50 GHz is applied to the baseband inputs. At the same time, the LO remains fixed at 246 GHz to characterize the frequency response of the transmitter and antenna. The results, depicted in Fig. 7.5, represent EIRP. Notably, a gap exists between the lower and upper sidebands due to the 1 GHz minimum baseband frequency. The measurement of the MMIC itself is plotted in green dashed lines. The curve is already not smooth due to self-interference in the receiver leaking into the calibration. An issue with the chosen calibration method is the spectral purity of the used T/R module as a signal source. While they are designed to output only a single tone, they inherently also have harmonic content, causing interference as their amplitude changes with the center frequency. Another issue present is inter-modulation in the receiver.

Comparing the behavior of the sample with the PCB antenna and resonator antenna reveals differences. The PCB antenna exhibits lower gain and a sharper decline post 260 GHz compared to the resonator antenna, which closely matches the MMIC's RF behavior with a drop-off after 270 GHz, aligning with design expectations. This suggests that the antenna and transition components do not constrain the system significantly. Despite a reduced bandwidth with the PCB antenna, it remains within system performance targets. Challenges with the PCB antenna include metal surroundings causing pattern ripples. An additional issue with the tested system is an asymmetry in the bond-wires generating common mode signals and frequency-dependent resonances.

Subsequent measurements focus on select baseband frequencies while rotating the receiver around the DUT at a fixed distance in co- and cross-polarization to assess antenna patterns. Results displayed in Fig. 7.6 and Fig. 7.7 for the resonator antenna, and Fig. 7.8 and Fig. 7.9 for the PCB antenna show distinct characteristics.
The resonator antenna exhibits a radiation dip at $-55°$ in the E-plane possibly due to minor misalignment on the bowtie feeder. This ripple is absent in the H-plane shown in Fig. 7.7. The pattern follows the simulation well and shows that the antennas operate as expected. This highlights the challenges of probe-based antenna measurements as the results of the antenna stand-alone deviated quite significantly from the simulation, as shown in Fig. 5.20 and Fig. 5.21.
The PCB antenna E-plane pattern in Fig. 7.8 displays an angular-periodic

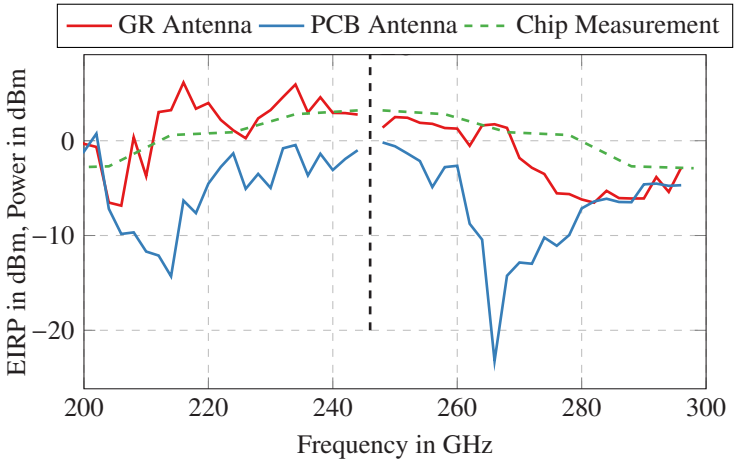


Figure 7.5: Measured frequency response at boresight with 246 GHz center frequency. The chip measurement is contacted on-wafer [5] © IEEE 2024.

ripple at 25° not present in simulations or the stand-alone measurement shown in Fig. 5.7(a). Simulation results indicate that additional metal near the antenna influences the radiation patterns. Interestingly, the ripple is only present in the E-plane, while the H-plane shows good agreement between measurement and simulations.

7.2.2 Bit Error Rate

The BER measurement uses the system described in 7.1. No eye diagrams are generated as the direct IF sampling approach keeps the complete baseband waveform in the digital domain. Hence, the eye-diagram is heavily influenced by the applied signal processing. Also, BER values exceeding the forward error correction (FEC) thresholds of approximately 3×10^{-3} are presented to illustrate how different operational conditions impact the reception and validate simulation outcomes [Ham50].
The initial measurement focuses on BER at boresight across various data rates with a receiver-to-DUT distance of 36 cm. Due to equipment limitations, data rates are assessed only up to 32 Gbit s^{-1}, with results depicted in

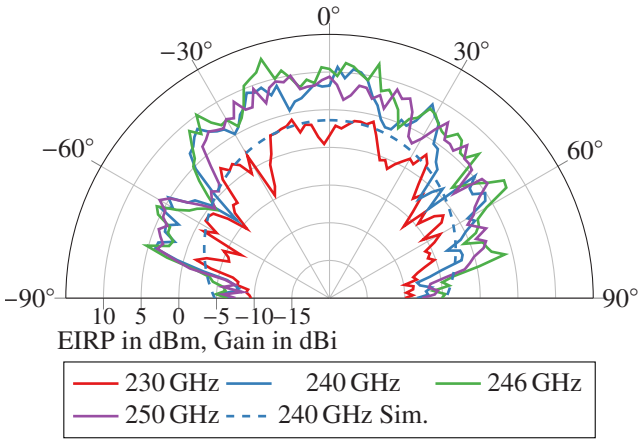


Figure 7.6: Measured and simulated pattern in the E-plane of the glass resonator antenna for different frequencies. The measured pattern is in EIRP while the simulation is in dBi [5] © IEEE 2024.

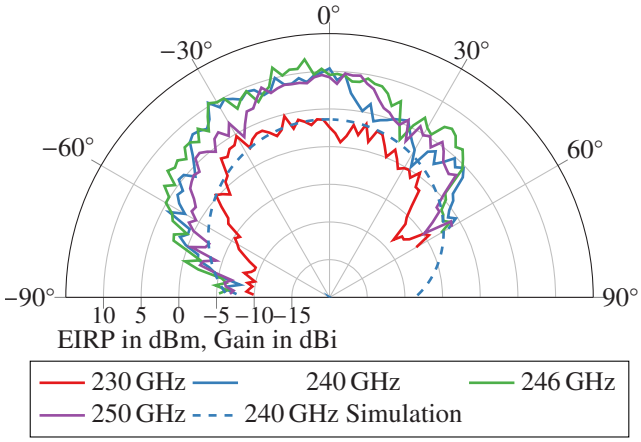


Figure 7.7: H-plane pattern of the glass resonator antenna at different frequencies. Due to geometrical limitations, the measurement ranges from −90° to 60° [5] © IEEE 2024.

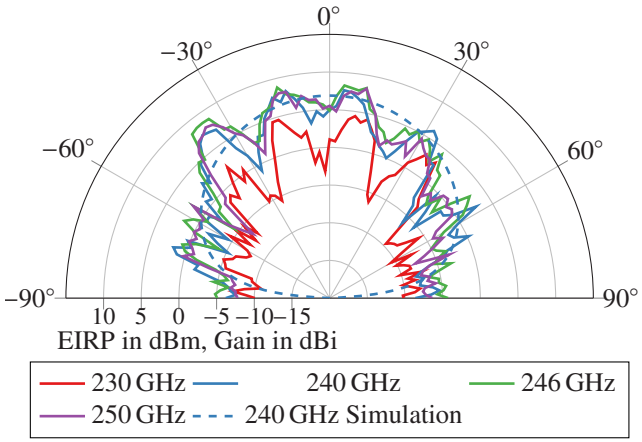


Figure 7.8: E-plane pattern of the realized PCB antenna at different frequencies. Shown are the simulated pattern in dBi and the measurement in EIRP [5] © IEEE 2024.

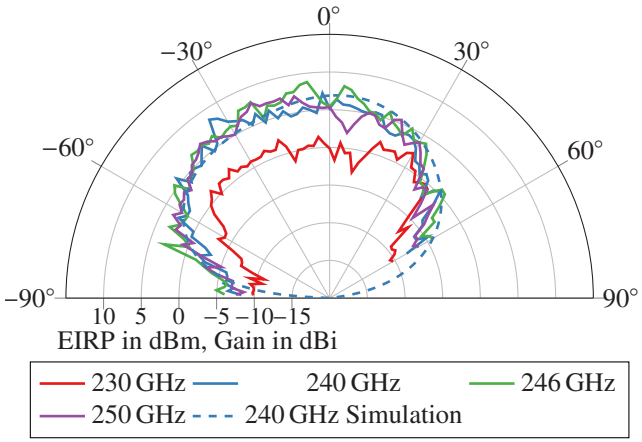


Figure 7.9: Measured and simulated H-plane pattern of the realized PCB antenna at different frequencies. Due to geometrical limitations, the measurement ranges from −90° to 60° [5] © IEEE 2024.

Fig. 7.10. As anticipated, BER rises with increasing data rates due to deteriorating SNR. A theoretical BER curve is fitted based on a single BER point assumption, considering BER dependence solely on SNR according to previous research [CZHN09]. The SNR is defined as

$$\mathrm{SNR} = \frac{E_0}{N_0}, \tag{7.4}$$

and the energy per bit depending on the data rate and transmitted output power P_{out} as

$$E_0 = \frac{P_{\mathrm{out}}}{f_{\mathrm{data}}} \tag{7.5}$$

and the noise depending on the data rate as

$$N_0 = 4kTB = 4kT \cdot f_{\mathrm{data}}. \tag{7.6}$$

The BER is depending on the SNR as

$$BER = \frac{1}{2} erfc\left(\sqrt{\frac{E_0}{N_0}}\right) \tag{7.7}$$

$$erfc(x) = \frac{2}{\sqrt{\pi}} \int_x^{\mathrm{inf}} e^{-x^2} dx \tag{7.8}$$

Assuming a given datarate f_0 and bit-error-rate BER_0, the BER at other datarates f_1 can be calculated as

$$SNR_0 = BER^{-1}(BER_0) \tag{7.9}$$

$$SNR_1 = SNR_0 \cdot \frac{f_0^2}{f_1^2} \tag{7.10}$$

$$BER_1 = BER(SNR_1). \tag{7.11}$$

We can observe a good agreement between theory and measurement using these equations. This indicates that the system BER up to the tested datarate of 32 Gbit s^{-1} is not limited by the MMIC or antenna but rather the sensitivity and limitations of the receiver chain. Further, looking at the measured antenna patterns for both systems in Fig. 7.6 and Fig. 7.8, a 5 dB difference can be

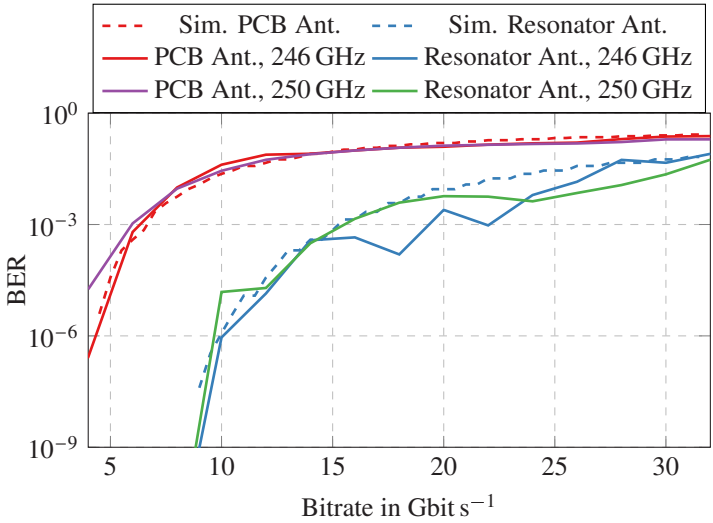


Figure 7.10: Measured BER at boresight and 246 GHz and 250 GHz LO frequency for the two systems and 36 cm distance between transmitter and receiver [5] © IEEE 2024.

observed. Due to the reduction in EIRP, the BER for the PCB antenna sample is worse, as verified by the measurements.

Going on, the sensitivity of the BER for different LO frequencies is evaluated, in part to investigate the influence of the antenna frequency response on the overall system and in part to assess the LO tuning range of the MMIC. The results are shown in Fig. 7.11 for the PCB antenna and Fig. 7.12 for the resonator antenna. Both samples show a sweet spot at 246 GHz and an increase in BER for lower LO frequencies. The PCB antenna, however, shows a more pronounced increase below 240 GHz. Hence, the useful LO tuning range is currently limited. Of note are the jumpy behavior of the lower data rates shown in Fig. 7.11 and Fig. 7.12. Here a fundamental issue is present, as for example 242 GHz is bad over all measured data rates while 240 GHz and 244 GHz are fine. This is true for both measurements. This is most likely due to some harmonic in the receiving mixer aligning with the destructively with the received signal.

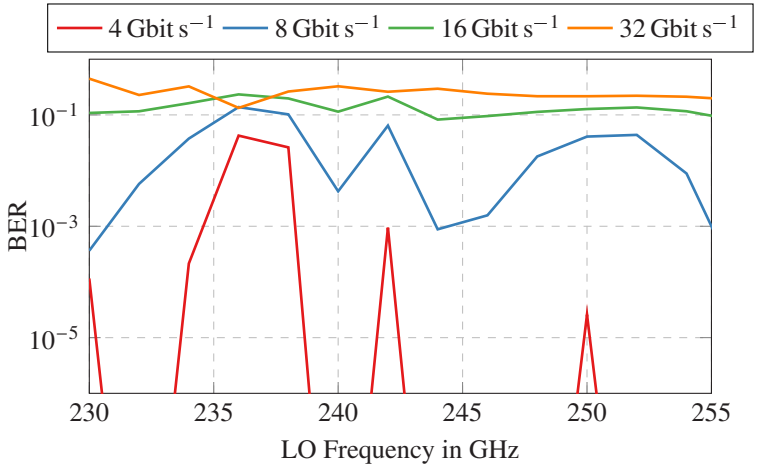


Figure 7.11: Measured BER at boresight sweept over LO frequency for the PCB antenna [5] © IEEE 2024.

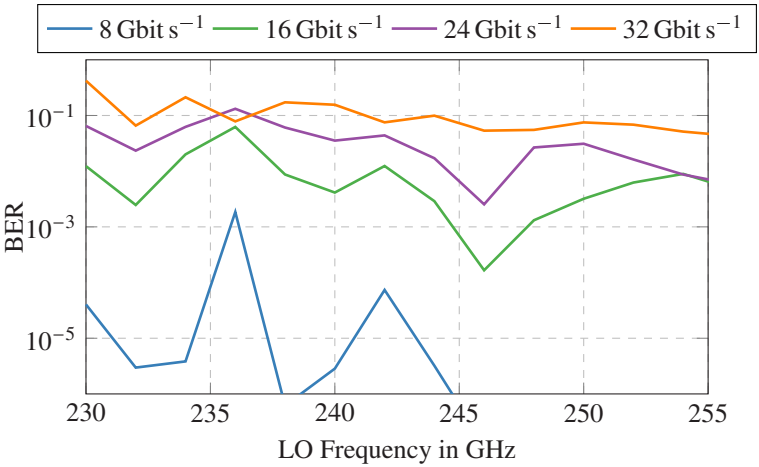


Figure 7.12: Measured BER at boresight sweept over LO frequency for the glass resonator antenna [5] © IEEE 2024.

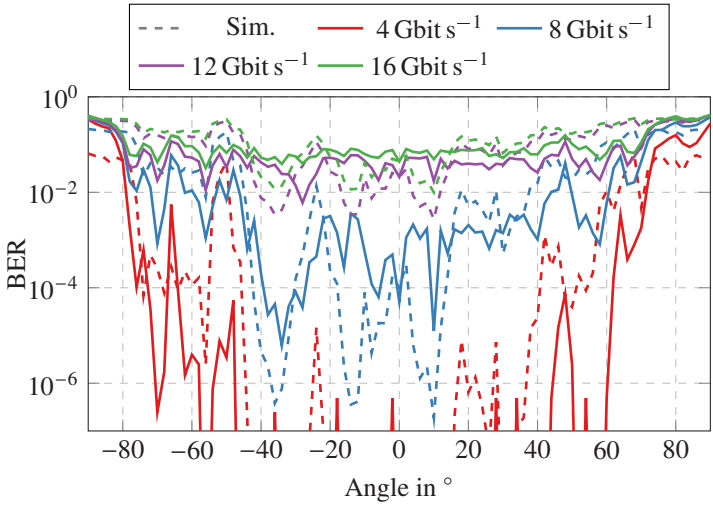


Figure 7.13: Measured BER over scanning angle in the E-plane for the PCB antenna. In dashed lines the theoretical BER curve is plotted based on the measured antenna pattern [5] © IEEE 2024.

Next, the BER over the antenna angle is measured. This is done by sweeping the receiver angle around the DUT and evaluating the BER for different data rates. Fig. 7.13 and Fig. 7.14 show the results. The degradation of the BER follows the antenna pattern used to calculate the theoretical curves in dashed lines. Visible in Fig. 7.14 is the radiation dip at −55° in the pattern of the antenna and the corresponding increase in the BER. Further, the slight asymmetry of the pattern is also visible when comparing Fig. 7.14 and Fig. 5.3(a). The theoretical patterns deviate at some points, which might be due to the changing pattern over frequency, which was not considered.

Concluding the characterization of the system, the BER over distance is measured. The measurement setup is shown in Fig. 7.15. The receiver is mounted on a tripod and the transmitter is rotated 90° to radiate horizontally. The receiver is moved through the lab, the distance is measured, and the BER for various bitrates is captured. The results of the BER measurements are shown

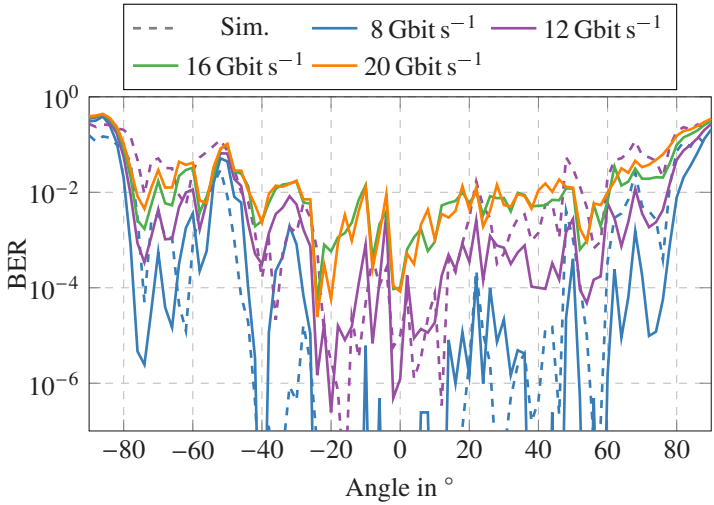


Figure 7.14: Measured BER over scanning angle in the E-plane for the glass resonator antenna. In dashed lines the theoretical BER curve is plotted based on the measured antenna pattern [5] © IEEE 2024.

in Fig. 7.16 and 7.17. The theoretical BER is calculated by modifying 7.5 to include the free space path loss:

$$\mathrm{FSPL} = \left(\frac{4\pi r}{\lambda}\right)^2 \tag{7.12}$$

to yield

$$E_0 = \frac{P_{\mathrm{out}}}{f_{\mathrm{data}} \cdot \mathrm{FSPL}}. \tag{7.13}$$

This gives for the ratio of the SNR

$$SNR_1 = SNR_0 \cdot \frac{r_0^2}{r_1^2}. \tag{7.14}$$

Observing the results for the resonator antenna in Fig. 7.16 a good agreement between expectation in dashed lines and measurement in solid lines is found. However, at close proximity, the BER is worse than anticipated. This is due to

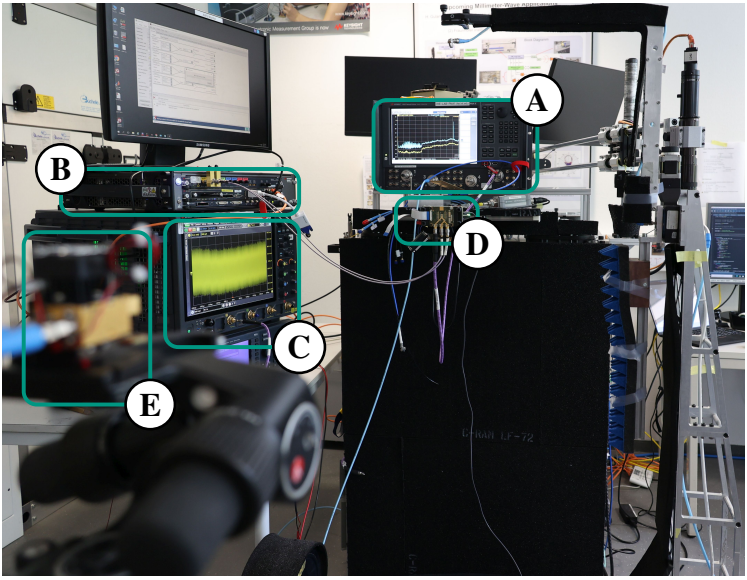


Figure 7.15: Photograph of the range measurements setup. The receiver is mounted on a movable tripod and the distance captured by means of a laser range finder [5] © IEEE 2024.

an alignment issue with the high-gain horn antenna at the receiver side. The closer the distance, the more critical minor alignment errors such as offsets and angle errors are. This is even more critical for the measurements of the PCB antenna shown in Fig. 7.17. Here, the BER at distances below 1 m are significantly worse than anticipated and even worse than the measurements done at 36 cm for the other evaluations. At increasing distances, the expectation and measurement converge again.

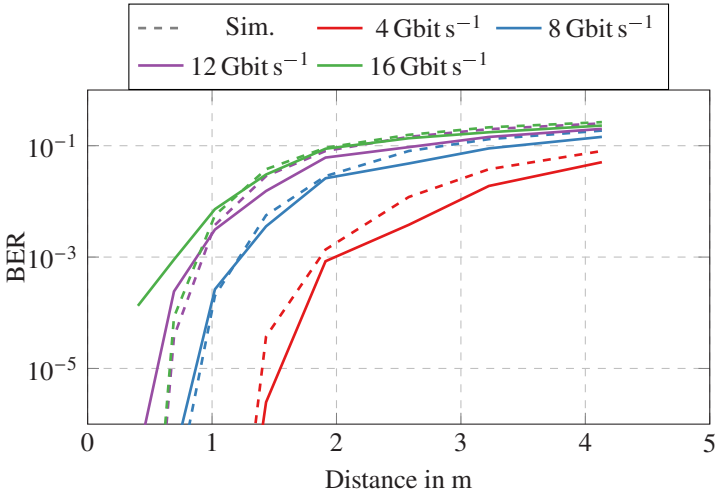


Figure 7.16: Measured BER at boresight sweept over distance for the glass resonator antenna. In dashed lines are the theoretical values, in solid lines the measurement [5] © IEEE 2024.

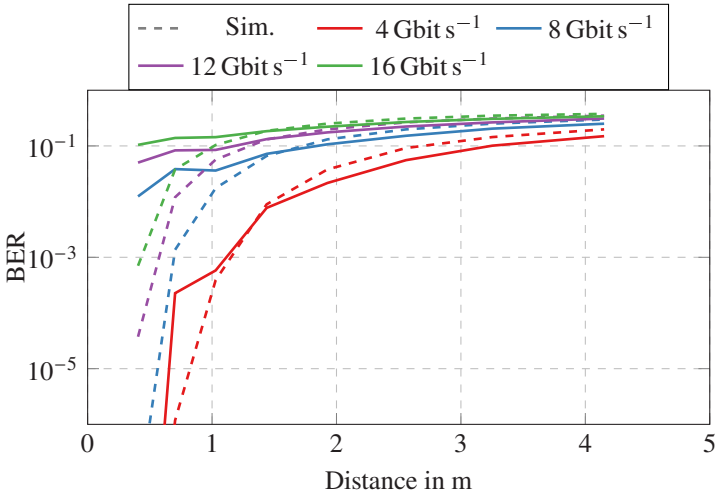


Figure 7.17: Measured BER at boresight sweept over distance for the PCB antenna. In dashed lines are the theoretical values, in solid lines the measurement [5] © IEEE 2024.

7.3 Phased Array Measurements

In the next step, the phased array systems are measured. This is done analogous way to the previous measurements with slight modifications to accommodate the increased number of channels. This includes using more channels from the AWG and two DC-supplies to feed the MMICs. One important step in phased-array systems is calibrating the phases to achieve proper superposition. This is done exhaustively for the two-element phased array by trying several phase control voltages on one MMIC while keeping the other one fixed and measuring the response. From the gathered data, the combination with the strongest peak is selected. This is done in 1° increments to calibrate the pattern over the steering angle.
The calibration process is repeated for the larger phased array with a more exhaustive 2D search map and reduced voltage resolution to find the optimal combinations. In a practical system, this process must be faster. This can be achieved by measuring each channel separately and pre-computing the optimum control voltages.
As before, the RF pattern is measured first, and the BER values afterwards over angle and steering. No BER over-distance measurements are done for the phased array systems.

7.3.1 RF Performance

Firstly, the phase calibration is done to center the beam to boresight for proper RF characterization. Calibrating the 1x4 array showed severe issues that could not be resolved within the measurement time frame. Hence, no boresight RF performance measurement was done. For the smaller array, the EIRP is captured over baseband frequency with the LO set to 246 GHz. The EIRP measurement is shown in Fig. 7.18. Shown in red is the frequency response of the glass resonator transmitter with only one MMIC. Below 240 GHz, the array shows a higher gain and more output power compared to the single MMIC transmitter as expected with up to 10 dB higher EIRP. However, above 246 GHz, the output power drops sharply, being 8 dB lower than the single antenna transmitter.
Firstly, the antenna pattern is investigated to rule out issues with the array. The simulation of the boresight gain of the two antennas is plotted in green dashed

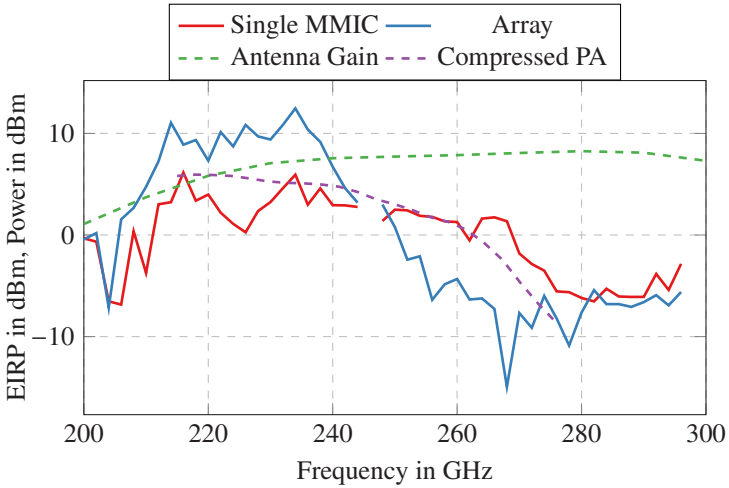


Figure 7.18: Measured frequency response at boresight with 246 GHz center frequency [4] © IEEE 2024.

lines. The array should have a very broad uniform gain; thus, it could not be the underlying issue, as the antenna simulations proved to be close to reality. Another aspect investigated is the two-tone response of the PA in compression. The simulation results are plotted in purple dashed lines. The PA will drop the output power of the upper sideband if operated into compression. This is in line with the observed behavior. An issue here might be the mutual coupling of both amplifiers through the antennas causing compression behavior.

Going on, the pattern of the 1x2 array is measured for different phase control settings at 246 GHz. For this, the receiver is swept around the DUT, and the EIRP is captured. The results are shown in Fig. 7.19. The resulting beam can be controlled $\pm 30^\circ$ around the center with grating lobes appearing for larger steering angles. This is due to the spacing larger than $\lambda/2$ of the antenna elements. The steering is relatively symmetric, as expected. The pattern matches the simulation results well, further proving the correct operation of the phased array.
Similar to this, the array steering behavior of the 1x4 array is captured for a few selected phase control combinations and plotted in Fig. 7.20. The

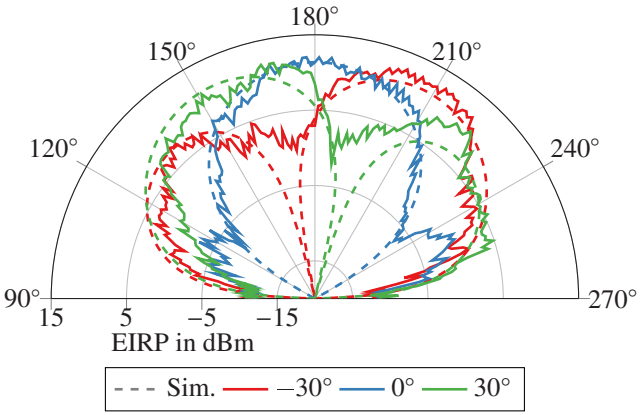


Figure 7.19: The antenna pattern in the E-plane for different steering values at 246 GHz. The grating lobes are an effect of the non $\lambda/2$ spacing of the antenna elements. The simulated pattern is shown in dashed lines [4] © IEEE 2024.

pattern is only captured from 90° to 210° due to mechanical limitations in the measurement setup. The transmitter is rotated 90° due to layout and routing challenges for the larger array. In the measurement, multiple strong grating lobes are visible. This results from the larger 1.6λ spacing to realize the 1x4 sample. Only little array steering of 20° can be observed. Further, the measured EIRP is lower compared to the 1x2 array. Here multiple issues are superimposed. Firstly, the large array spacing causes very strong grating lobes, reducing the overall gain of the array. Next, the tight integration of the four MMICs and antennas causes issues in assembly. A suspected broken bond-connection will cause destructive interference and lack of power in the pattern. This highlights the challenges faced in phased-arrays above 200 GHz. While the antennas shrink, the MMIC and DC routing stay rather constant in size.

7.3.2 Bit Error Rate

The BER of the 1x2 array is measured in three distinct measurements. Firstly, with the previously captured beam pointing calibration, the beam is pointed to boresight, and the BER is captured over data rate to see if there is an improvement over the single-chip transmitters and if the system operates correctly.

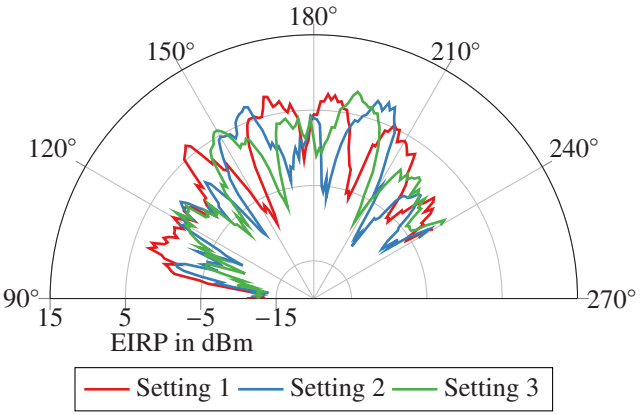


Figure 7.20: The antenna pattern in the H-plane for different steering values at 246 GHz. The grating lobes are an effect of the non $\lambda/2$ spacing of the antenna elements.

Next, the BER over angle is captured, pointing the transmitter to boresight and capturing the BER over receiver angle. Lastly, the receiver is targeted on the main lobe over the whole achievable steering range and the improvement in BER to the previous measurement is investigated. Due to the issues above, only the BER over angle is captured for the 1x4 array.
The first measurement is shown in Fig. 7.21. For data rates below 22 Gbit s^{-1}, the array significantly improves over the single-chip transmitter due to the higher signal power. However, they converge after 22 Gbit s^{-1}. This is most likely due to the smaller RF bandwidth indicated by Fig. 7.18. Next, the BER over angle is captured with the beam pointing to 190° and shown in Fig. 7.22. This is an artifact of erroneous phase calibration data and causes a spike in BER at 150°, which is in line with the antenna pattern. The theoretical BER curves are again calculated for the different data rates using the measured antenna pattern and plotted in dashed lines. The theoretical values and measurements line up below 16 Gbit s^{-1}. However, above 16 Gbit s^{-1} the BER at boresight is significantly worse than anticipated from the antenna pattern and also slightly worse than the boresight measurement shown in Fig. 7.21. This might be an issue with the superposition of the wideband signals for phase-steering outside of boresight.
Looking at the BER over angle for the 1x4 array shown in Fig. 7.23, a signif-

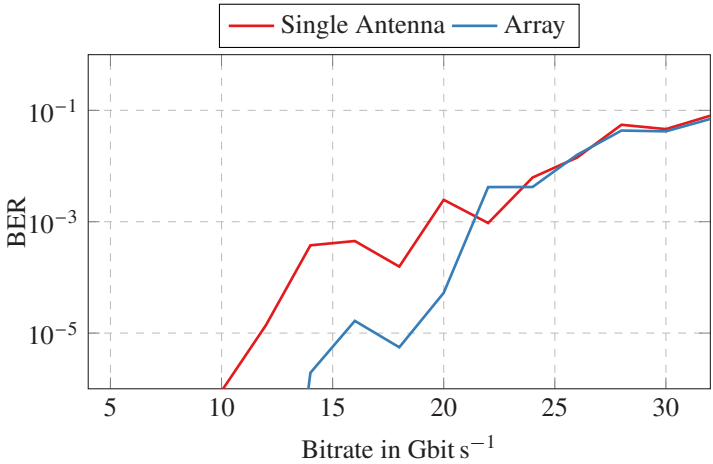


Figure 7.21: Measured BER at boresight for phased array an a single antenna transmitter [4] © IEEE 2024.

icant worsening is visible. The BER is above 10^{-1} for most of the steering angle. There are improvements at 150° and 200°, which coincide with the radiation peaks shown in Fig. 7.20 for setting 3. A significant issue is the lack of output power, the spreading over multiple lobes, and the even more problematic frequency-dependent superposition.

After measuring the BER over angle, the effect of the beam steering is analyzed. The beam is pointed to the receiver over the steering range, and the BER is captured for various data rates. The receiver is swept through the theoretical steering limit of 165° to 207°, which calculates the numerical center of the measured patterns. Due to ripple, this center is slightly different from the theoretical limits. The plot is shown in Fig. 7.24. It is interesting to observe that there is an improvement in transmission below 180°, which, from the system's inherent symmetry, should not be the case. Investigating Fig. 7.19 again, a slight asymmetry in the captured patterns is visible, hinting at an issue with the superposition of the two patterns. Comparing the curves with Fig. 7.22, an improvement and flatter response can be seen. LO phase steering is an acceptable beam steering method for the tested data rates, although the measurements show certain issues with the approach.

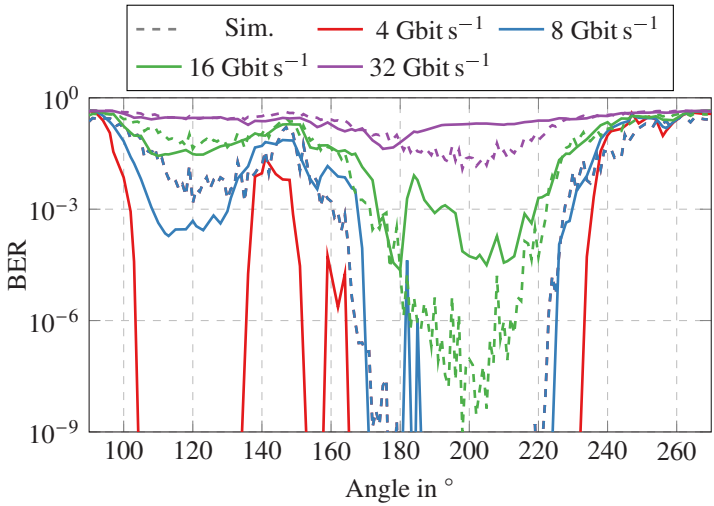


Figure 7.22: Measured BER for the 2x array with the beam pointed to 190° over angle. In dashed lines, the theoretical BER curves calculated from the antenna pattern are plotted [4] © IEEE 2024.

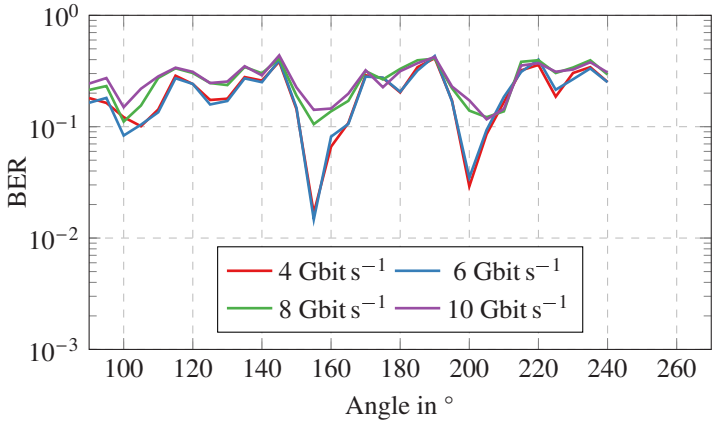


Figure 7.23: Measured BER for the 4x array with the beam pointed to 180° over angle.

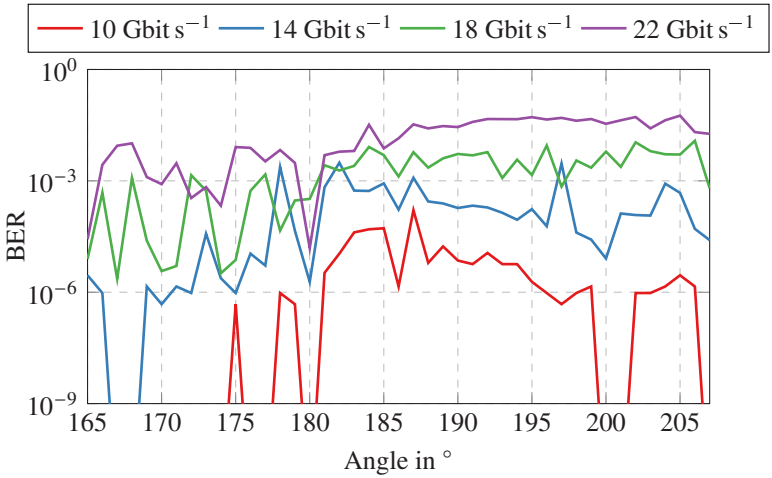


Figure 7.24: Measured BER for the 2x array with the beam pointed to the receiver [4] © IEEE 2024.

7.4 Comparison to the State of the Art

Comparing the presented work is done in two steps. First, we compare against similar transmitter systems operating above 200 GHz. While the sub-THz spectrum can be considered to start at 100 GHz, operating above 200 GHz still imposes certain challenges on antennas and packaging that would make comparison uneven. Tab. 7.2 presents the comparison to all major publications with transmitters operating above 200 GHz. In comparing the systems, a note has to be taken on a certain measurement aspect. As previously shown, the BER is primarily dependent on SNR, which short measurement distances and high gain antennas can improve. Further, metrics like transmit efficiency in pJ bit^{-1} depends on the achieved data rates. Hence, one can seek to maximize this figure by moving the transmitter and receiver very close together without any practical improvement in the system's performance. Even further, [AdGW+22] gives a measurement distance of 3.5 cm, that given the physical size of the antenna is below the far-field limit. Nevertheless, 10 Gbit s^{-1} measured at 1 m is chosen to give a comparison to the other works. A low transmit efficiency of 41.4 pJ bit^{-1} is achieved at this configuration. Increasing the antenna gain or

reciprocally reducing the measurement distance to improve the SNR by 10 dB would bring the BER at 32 Gbit s^{-1} below 10^{-3} and the transmit efficiency to 12.9 pJ bit^{-1}.

Comparing the work to the others presented in Tab. 7.2, we can present the smallest MMIC size and, therefore, an essential step to larger phased array systems. Further, given the reported EIRP values and antenna gains, we present the highest output power of all reported systems. Further, we present the most detailed transmission analysis of any presented system. Not only capturing data rate or BER over a single link but also over distance and scan angle. Many useful insights could be gained by measuring BER over these metrics instead of error vector magnitude (EVM). Critical aspects shown here are the frequency-dependent pattern of the used antennas as the phase and amplitude of different frequency components are influenced independently, causing some angles to be worse than anticipated by pure signal strength reduction. This is a first for any reported transmitter system above 200 GHz. Further, the presented system has a very good power consumption per MMIC and, even though not the best, still has a competitive transmit efficiency that exceeds those of current generation WiFi or 5G systems.

Next, Tab. 7.3 presents the comparison to phased-array systems. Here, only the 1x2 array is used for comparison, as many important metrics for the 1x4 array could not be captured. [AdGW+22] is listed in both tables for completeness. This work demonstrates the first phased array system above 200 GHz with tested data rates up to 32 Gbit s^{-1}. The measured steering angle and system bandwidth are competitive or exceeding the state of the art. Further, this work presents the most detailed analysis of a communication link above 200 GHz with BER measurements over angle and phase steering. Something comparable was done in [YWL+23] for a receiver system, although fewer data points were captured. Another very important aspect is the prospect of the chosen semiconductor technology. While III-V achieves excellent RF performance, this comes at the price of power consumption, as reported in [YWL+23]. Further, III-V does not offer the same level of integration as SiGe. Again, [YWL+23] presents a system consisting of multiple packaged function blocks while this work presents a single MMIC. This improves system reliability and reduces costs while also shrinking overall size. Further, the higher achievable output power and bandwidth is a significant benefit over CMOS, with [AdGW+22] and Tab. 4.1 reporting significantly lower output powers. Comparing the

presented work against systems in the same technology, such as [KAKM23] and [DLL+15], the output power could be significantly improved. The achieved EIRP is comparable to [DLL+15], with only half the transmitters. Even worse is the system presented in [KAKM23], with a reported EIRP of only −8 dBm. This is due to issues in the power supply routing. This shows the benefit of not integrating a phased array system on a single chip. By using a multilayer PCB, DC supply routing could be optimized.
Another aspect is the power consumption of an IQ architecture. [KAKM23] has a 56 % higher power consumption compared to a similar 1x4 system employing the MMIC presented here. While the spectral efficiency of higher order modulations is inherently better, the analysis presented in Sec. 3.1 shows that the improvement is marginal depending on the SNR.
The presented packaging concept here is a world first and highlights a significant step towards system integration of sub-THz systems. By allowing to measure the same MMIC directly, that is put into a system, a lot more insight into the system can be obtained than previously possible. Packaging the antenna through a differential wire-bond interface proved successful and allowed the use and demonstration of different antennas. Especially the possibility of completely packaging the whole system on a PCB without any additional lenses is a major step in the widespread adoption of the emerging technology.

Table 7.2: Comparison to the state-of-the-art for transmitters beyond 200 GHz

	This	[EMW+18]	[RVGHP19]	[AdGW+22]	[GRVM+22]
Technology	130 nm SiGe	130 nm SiGe	130 nm SiGe	65 nm CMOS	130 nm SiGe
Center Frequency	246 GHz	240 GHz	230 GHz	256 GHz	215 GHz - 240 GHz
Tx Integration	LO, Mod, PA	LO, Mixer, PA	LO, IQ Mixer, PA	LO, Mixer Last	LO, IQ Mixer, PA
Rx System	Lab Setup	Custom MMIC	Custom MMIC	Custom MMIC	Custom MMIC
Tx BW	60 GHz	20 GHz	26 GHz	-	20 GHz
Tx Chip Area	1.16 mm^2	4.16 mm^2	1.4 mm^2	4.17 mm^2	-
Modulation	BPSK	BPSK	16-QAM	QPSK	16-QAM/QPSK
LO Architecture	60 GHz x4	x8	x16	Subharmonic x4	x8
EIRP	10 dBm	13.2 dBm	30 dBm	-	28.5 dBm
Tx Antenna Gain	6 dBi	14 dBi	26 dBi	26 dBi	25 dBi
Tx Antenna Type	PCB/Bow-tie	On-Chip, Dielectric Lens	On-Chip, Si-Lens	Probed Horn Antenna	On-Chip, Si-Lens
Rx Antenna Gain	25 dBi	14 dBi	26 dBi	26 dBi	25 dBi
Range Meas.	0.3 m - 4 m	15 cm	1 m	3.5 cm	0.6 m
Symbol Rate	32 Gbd s^{-1}	25 Gbd s^{-1}	25 Gbd s^{-1}	26 Gbd s^{-1}	25 Gbd s^{-1}
Demonstrated Data Rate	32 Gbit s^{-1}	25 Gbit s^{-1}	100 Gbit s^{-1}	16 Gbit s^{-1}	100 Gbit s^{-1}
BER @Data Rate, Distance	$\leq 10^{-3}$ @ 10 Gbit s^{-1}, 1 m	$\leq 2.2 \cdot 10^{-4}$ @ 25 Gbit s^{-1}, 15 cm	$\leq 4 \cdot 10^{-3}$ @ 100 Gbit s^{-1}, 1 m	$\leq 4 \cdot 10^{-3}$ @ 16 Gbit s^{-1} [a], 3.5 cm	$\leq 5 \cdot 10^{-2}$ @ 100 Gbit s^{-1} [a], 60 cm
Tx P_{DC}	414 mW	375 mW	1410 mW	750 mW	2600 mW
Tx Efficiency	41.4 pJ bit^{-1}	18.75 pJ bit^{-1}	14 pJ bit^{-1}	46 pJ bit^{-1}	26 pJ bit^{-1}

[a] Calculated by tables given in [SRI06]

Table 7.3: Comparison to the state-of-the-art in THz phased array systems

	This Work	[LZRR22]	[DLL+15]	[AdGW+22]	[YWL+23]	[dRST+23]	[KAKM23]
Array	1x2	2x4	1x4	1x4	1x4	4x4	1x4
Technology	130 nm SiGe	45 nm CMOS	130 nm SiGe	45 nm CMOS	InP, GaAs	55 nm SiGe	130 nm SiGe
Scanning Angle	±30°	±35°	±12°	±18°	±30°	±30°	±45°
Antenna Type	Off-Chip Bowtie	On-Chip with Superstrate	SIW Cavity backed On Chip	Off-Chip Vivaldi	Reflector Antenna Array	Patch Antenna on PCB	On-Chip Patch and Lens
System Type	Tx	*Rx*	Tx	Tx/Rx	*Rx*	Tx/Rx	Tx/Rx
Power[a]	818 mW	1.16 W	1 W	750 mW	2.7 W	4.9 W	2.5 W
Center Frequency	246 GHz	140 GHz	320 GHz	256 GHz	215 GHz	150 GHz	140 GHz
Bandwidth	30 GHz	16 GHz	20 GHz	-	40 GHz	20 GHz	60 GHz
Distance	36 cm	35 cm	15 cm	3.5 cm	11.24 m	34 cm	15 cm
EIRP	12 dBm	-	10.6 dBm	−14 dBm[b]	-	26 dBm[c]	0.4 dBm[c]
Tested Data Rate	32 Gbit s^{-1}	10 Gbit s^{-1}	-	26 Gbit s^{-1}	32 Gbit s^{-1}	0.104 Gbit s^{-1}	200 Gbit s^{-1}

[a] Reported DC power for Tx if applicable.
[b] From measurement plot, not reported explicitly.
[c] Calculated from P_{sat} and theoretical antenna gain.

8 Conclusion and Outlook

In the presented work, new types of sub-THz BPSK transmitters are described that combine new system concepts with novel packaging and antenna solutions to solve many of the challenges currently present in exploiting the bandwidth available in the frequency range from 200 GHz to 330 GHz. The result is a comprehensive system that shows excellent adaptivity regarding system assembly, phased array operation, and data rate. A novel differential wire-bond transition is the main component in solving the packaging challenge. This connects a highly compact and broadband PA to either an innovative glass resonator loaded on-chip antenna with a shorted differential feeding structure or cutting edge PCB based wideband antennas. The final design is analyzed in depth by measuring both single-chip transmitters and phased arrays for one of the most detailed analyses of any presented sub-THz transmitter.

The PA as the first element in the chain is developed by firstly investigating the state of the art both in PA designs and available semiconductor materials. Next, a tight co-design with the modulation chain developed at *TUD* [Ste23] is done to maximize the bandwidth of the whole system. Using compact transformer coupling and a range of tuning elements, the amplifier is tuned to operate with one of the highest reported small signal bandwidths of 74 GHz for any H-band power amplifier. The output power is traded off between surface area and broadband operation and achieves a competitive peak at 8 dBm compared to systems without power combining. The output is directly matched to a 100 Ω differential pad, which is a world first at this frequency range.
The connection between the amplifier and a balun for direct measurement or the antennas is realized with impedance-tailored differential bond-wire transition. By approaching the transition as a transmission line, a novel concept of impedance tailoring is employed. By optimizing the spacing and using an encapsulation the characteristic impedance can be matched to the system impedance to achieve wideband operation. As the transition is now matched, length does not matter except for transmission line loss. Hence, the packaging

constraints are relaxed, and the placing of chips and antennas becomes less crucial, offering more flexibility. The transition is demonstrated to work for on-chip and chip-to-chip differential transitions as well as chip-to PCB connections.
Leveraging the novel packaging concept, multiple novel antenna structures have been designed. As a first-of-its-kind, PCB based antennas operating in the H-Band are presented, measured, and employed for the transmitter system. They achieve very competitive relative bandwidths larger than 30 %. An alternative approach uses a parasitic resonator on top of a novel shorted bow-tie feeding element, achieving wideband operation with relative bandwidths over 20 % with high efficiency above 55 % without the drawbacks of many of the previously published solutions. This concept is combined with a novel 3D-printing approach for resonator structures directly on the chip. The presented antennas further state of the art both in on-chip antennas and PCB based antennas for sub-THz systems.
The MMIC is designed for maximum adaptivity, which is demonstrated as the first of its kind in a detailed manner. Based on on-wafer measurements of the MMIC itself, the assembled transmitter packages with PCB antennas and resonator antenna are evaluated. This is done for simple RF scenarios with single-tone input and over-received data rate tested up to 32 Gbit s^{-1} by evaluating the BER. These measurements are done statically and over receiver angle and distance from 36 cm to 4 m. Further, an exemplary 1x2 phased array and a 1x4 phased array are assembled and measured, highlighting the unique adaptivity of the designed MMIC. These systems are also evaluated for their RF behavior and data transmission. The phased array systems are also evaluated for their BER over angle and beam steering, demonstrating the capabilities and shortcomings of the chosen approach.
The measurements show the excellent performance of the MMIC. The MMIC outperforms the measurement equipment or antennas in all measurement scenarios. While data transmission ranges suffer from the low antenna gain, it is demonstrated that the system is only limited by SNR. The pattern steering is evaluated within a single tone RF domain and over BER, a first-of-its-kind measurement for transmitters in this frequency range. Choosing a modulation scheme with low spectral efficiency, such as BPSK, has successfully presented itself as a viable option for short range wideband and next-generation communication links. The achieved efficiencies per bit are significantly better than current generation WiFi or 5G links with achieved values of 41.4 pJ bit^{-1}, even with much lower data rates to achieve higher ranges. Even under wors-

ening conditions, such a simple system can offer significant improvements to available bandwidth compared to current-generation wireless links without the necessity of complex modulation or power-hungry DAC systems.

Going further, a few issues should be investigated and alleviated. Firstly, the MMIC itself is larger than the antennas, limiting phased array size. This is a common problem with sub-THz systems and worsens with increasing frequency. A different approach in on-chip bias generation and multiple channels on a single chip can solve this to a degree and should be investigated in detail.

As the measurement equipment is a severe limiting factor of such wideband systems, a custom receiver architecture can improve the overall system performance and evaluation.

The antenna design can be improved by employing different thin-film technologies to enhance bandwidth and efficiency.

A Appendix

Several other antenna designs were build and measured, which are presented in Sec. A.1 to A.3. Due to time constraints these designs did not make it into the final system.
Sec. A.4 highlights some challenges for differential test and measurement and shows measurement results of the implemented passive and active baluns.

A.1 Series Fed Patch Antenna

Two alternative antenna concepts were investigated compared to chapter 5. The first is a series fed differential patch antenna with the layout shown in Fig. A.1. Four resonators are cascaded and loaded with parasitic patches to either side. As there is no direct on-PCB probe available a single ended ACP probe was used to contact the differential line. The GSG structure should present 100 Ω between the center pin and either outside ground plane. Simulations show that this approach yields usable results.

Fig. A.2 shows the measured and simulated behavior for both left and right contact and both ACP and coax-style probes as presented in 3.5.2. The left contact with the coax probe matches the simulation somewhat. Both measurements with the ACP show significant deviation from the simulation, which is most likely due to probe-wear. Investigating the E-plane pattern in Fig. A.3

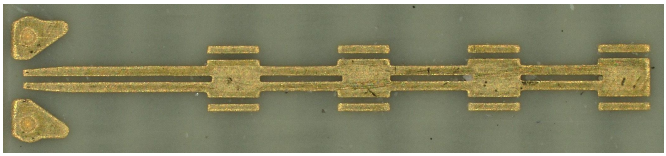


Figure A.1: Micrograph of a series fed patch antenna.

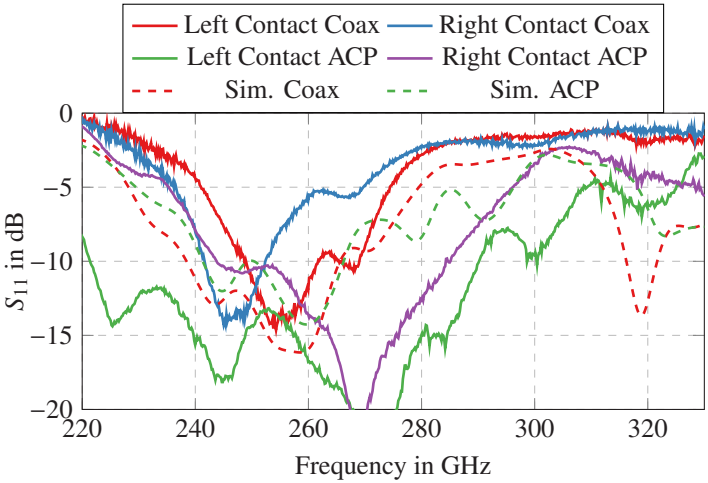


Figure A.2: Simulated and measured input match and gain over frequency for the series fed patch antenna.

and H-plane in Fig. A.4 shows that the realized gain is highest at 280 GHz, which would match the measurements done with the ACP probes.

Due to the reflection at the probe-body the pattern shows significant ripple in the E-plane and very strong lobes in the H-plane. The peak realized gain is 10 dBi with a shift to higher frequencies.

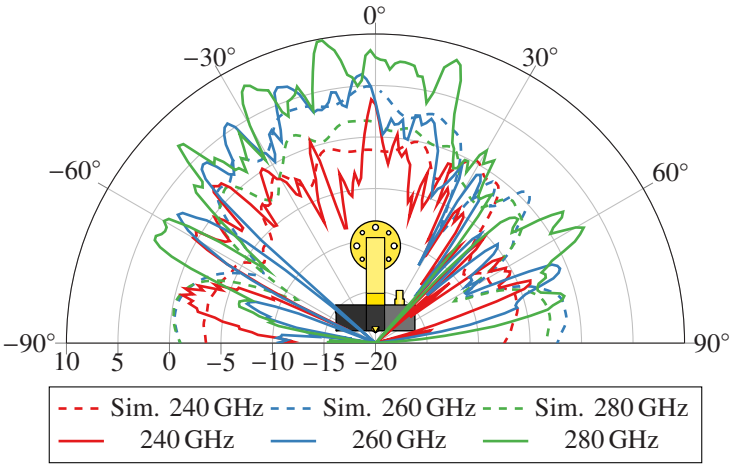


Figure A.3: E-plane field pattern of the series fed patch antenna.

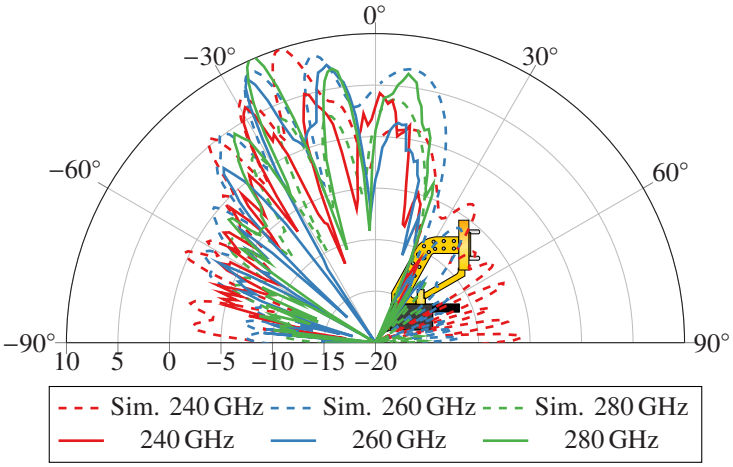
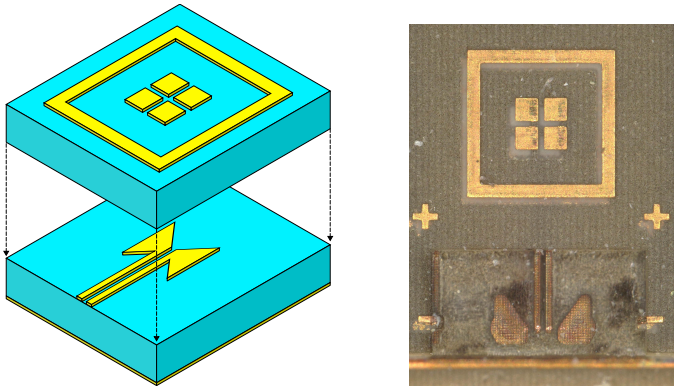


Figure A.4: H-plane field pattern of the series fed patch antenna.

A.2 Buried Feed Resonator Antenna

Another design tested is a buried feed resonator loaded antenna. A bow-tie element is placed on layer 2 in the PCB stackup and four rectangular patches placed on the top layer. The layout and the micrograph is shown in Fig. A.5. As the antenna feed is on layer 2, the contact pad had to be placed on layer 2 as well as the via inductance was prohibitive for a layer change in the H-band. To contact the antenna the substrate layer is removed with a pico-second laser, leaving the grid like artifacts on the metal. Further, due to manufacturing issues a thin film of metal contaminated the surface and was also removed by laser ablation. Incorrect alignment of the laser system caused the laser pattern to be off and creating the shadow like artifacts. Investigating the input match shown in Fig. A.6, a decent agreement of simulation and measurement is visible. While the simulation indicates a wideband input match from 220 GHz to 285 GHz, the measurement only shows an input match from 221 GHz to 260 GHz. However, the measured gain at boresight over frequency does match the simulation quite well. A peak gain of 10 dBi is observed at boresight and 250 GHz.
Comparing the E-plane pattern in Fig. A.7 with the H-plane pattern shown in Fig. A.8 shows a significant deviation at boresight. While the latter shows a



(a) Schematic View (b) Micrograph

Figure A.5: Schematic view and realized micrograph of the realized burried antenna.

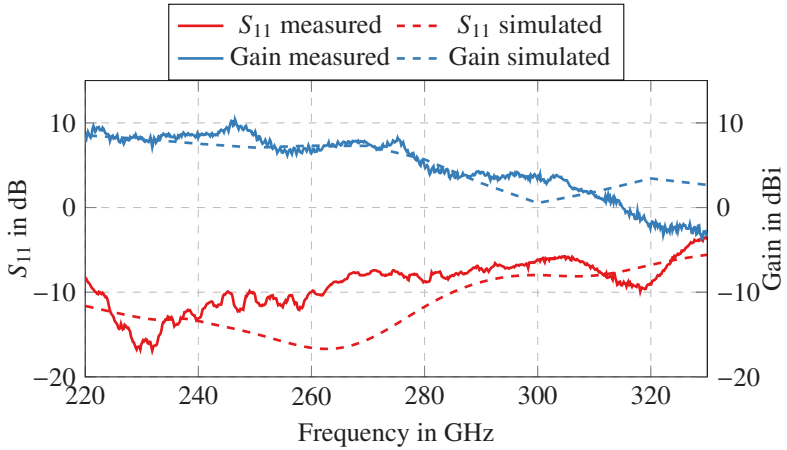


Figure A.6: Simulated and measured input match and gain over frequency for the burried resonator antenna.

peak realized gain in excess of 10 dBi, the E-plane measurement only shows 6.5 dBi, hinting at measurement issues. Each polarization had to be measured separately to allow mechanical changes to the receiver, hence causing probing differences. Overall the antenna shows excellent performance compared to the state of the art in Tab. 5.1. However, the necessity of laser ablating the substrate and peripheral issues made this design infeasible for the transmitter systems.

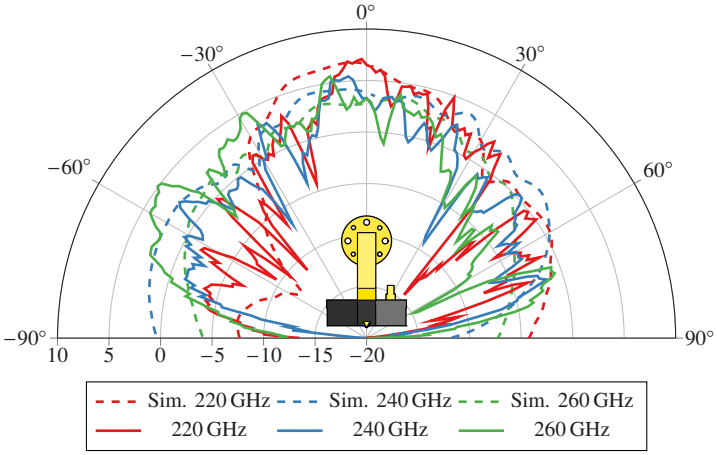


Figure A.7: E-plane field pattern of the burried parasitic patch.

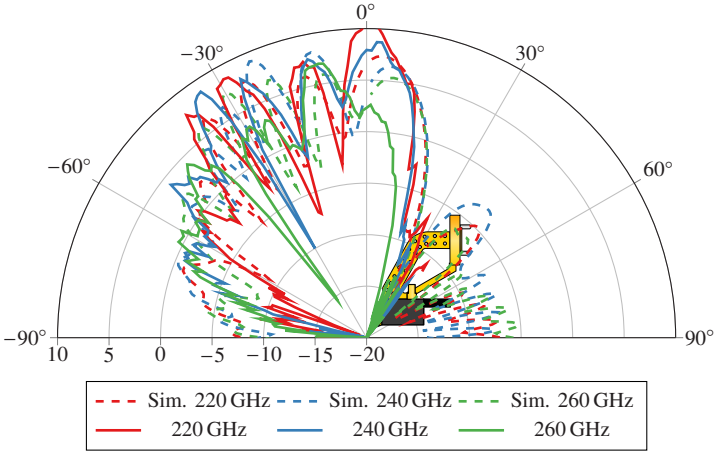


Figure A.8: H-plane field pattern of the burried parasitic patch.

A.3 3D-Printed Curved Antenna

A main benefit of using 3D-printing is the possibility of 3D-freeform structures. This option was also investigated and an antenna design with a curved resonator fabricated. The micrograph is shown in Fig. A.9. After manufacturing and testing it was found that the design is defective. Investigations showed that the layer step height was to large with 5 µm to be electrically connected in the sputtering process. Hence each step is electrically separated from each other. In [1] such structures were successfully fabricated, however using a different printer which achieves a z-resolution of 100 nm.

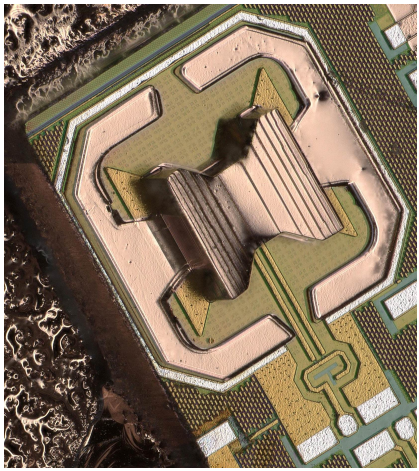


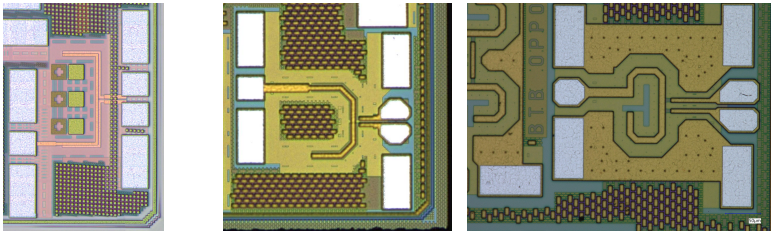
Figure A.9: Micrograph of the realized 3D shaped antenna.

A.4 Differential Test and Measurement

Building a differential amplifier creates challenges in testing and measuring the realized circuits. Current state of the art on-wafer measurement equipment is limited in its capabilities to measure differential circuits. Firstly, no on-wafer prove is available to contact the circuits in the targeted frequency ranges. Secondly is there currently no calibration standards available to synchronize the phase output of the used upconverter modules. Hence, other ways have to be sought to achieve a proper differential stimulus. This can be achieved by using a balun, either passive or active, which will be compared in detail in the following sections.

A.4.1 Passive Baluns

Three different Marchand baluns were designed as stand-alone parts to measure the various differential circuits within this work. Two more baluns were designed to match and connect the power amplifiers themselves. The three stand-alone baluns are shown in Fig. A.10. They are built by coupled $\lambda/4$ sections. Version 1 shown in Fig. A.10(a) is realized in the copper backend of *IHPs* SG13G2Cu process. The lines are on the same plane as the upper thick copper layer. The ends of the differential lines are shorted to the ground plane. The balun is folded to save space. The output pad is not optimized. The second version is realized in the aluminum backend and features an optimized differential pad with the removed ground and an optimized pad shape. The balun has a 45° section to reduce fringing fields. The coupling is happening between top layer two and top layer 1 of the BEOL. The single-ended line is significantly smaller to compensate for the increased capacitance of the coupled line. The last version of the balun is double-folded and also uses inter-layer coupling. A T-style slot in the ground plane helps optimize the symmetry by steering the ground currents better. The output pad is enlarged for better bondability, and the structure is designed as GCPW.



(a) Version 1 (b) Version 2 (c) Version 3

Figure A.10: The different version of the used stand alone baluns used for test and measurement of the antennas and final systems. Version 1 is realized in SG13G2Cu while version 2 and 3 are realized in SG13G2.

A.4.2 Active vs Passive Baluns

Baluns are widely used components at all frequency ranges. Passive implementations either use a transmission line 180° phase shift technique or a fundamental mechanism to create a counteracting current such as transformers quadrature hybrids. Balun design's main challenge is achieving broadband operation, low loss, and high-quality differential output. Secondary considerations include common and differential mode impedance, as a mismatched standard mode impedance can cause amplifier instability.

Another approach is using an active circuit to generate a differential signal. This can be achieved by having a differential pair with high common mode suppression that converts an input signal into a differential output signal. Such a circuit operating above 200 GHz was published for the first time in [16] as part of this work. A modified differential stage is at the core, as shown in Fig. A.11. The input branch is matched with a series L-C-L network. Matching the unconnected port with a specific impedance is very important to maximize common mode suppression. Cross-coupled capacitors reduce the Miller effect and introduce more single-ended to differential mode conversion. A significant part plays the output transformer. By avoiding a center tap on the secondary coil, a common mode suppression of better than −20 dB is achieved.

The base connection of the upper transistors is shared to allow for differential cancellation. Placing a larger capacitor at this node will allow common mode currents and should, therefore, be omitted. A small capacitance of 6 fF is added

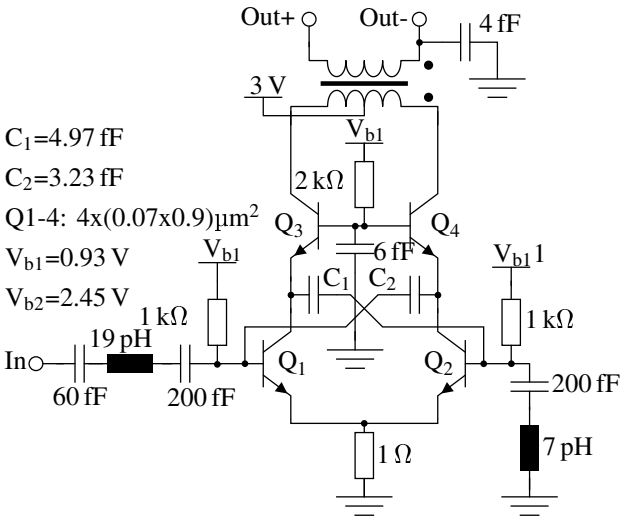


Figure A.11: Schematic of the active balun [16].

to support the gain and stability. The transformer has a significant capacitive coupling, so a small amount of common mode signal can couple through. To enhance the symmetry of the output signal, a small 4 fF capacitor is added to one side of the output transformer.

The realized circuit is shown in Fig. A.12. In order to measure the chip a passive balun is connected to the output and deembedded through simulation results. A major shortcoming in the manufactured chip is an additional hatching of the lower metal layers by the manufacturer. This is shown as a magnification in Fig. A.12. This hatching was not considered in the simulation and causes major deviations in the results. Due to the small size of the hatching grid it is not practically possible to include the slits in the EM-simulation of the complete circuit. The mesh cells increase to a non-feasible amount and are also too small causing a large amount of numeric errors that accumulate.

Using a transmission line and a series of simulations a simplified model of the hatching is constructed. The effect of the hatching is approximated by using a complex metal impedance from the original 43 103 000 S m^{-1} to 1 710 300 S m^{-1} $+j$300 000 S m^{-1} and an additional surface roughness of

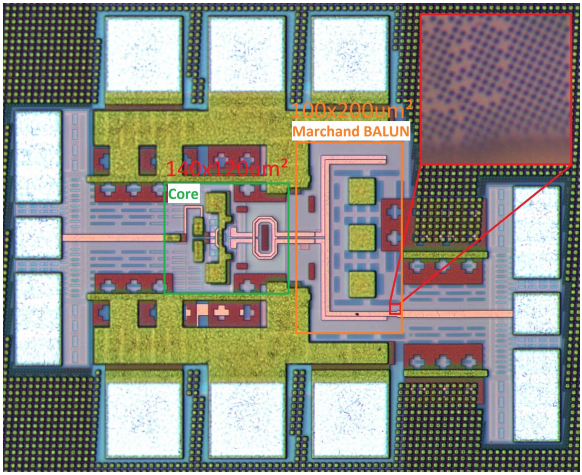


Figure A.12: Micrograph of the fabricated active balun test circuit [16].

0.5 µm and model "Smooth". The complex metal impedance should model the path elongation due to the hatching.

The chip is measured and the results are shown in Fig. A.13. As expected due to the hatching simulation and measurement do deviate more from another than pure measurement uncertainty. Especially the thru behavior S_{21} is not correctly modeled in neither simulation with modified metal conductivity nor an extensive simulation with the metal slits. This indicates a more deeply rooted issue in the metal stack. The input match can be approximated quite decently by the change in conductivity, while the output matching sees some deviation. Overall a 40 GHz bandwidth around 257 GHz is achieved with a maximum gain of 1 dB ignoring the output marchand balun losses.

This shows that an active balun can be utilized at H-band frequencies, although bandwidth and reciprocity might suffer. However, on the flip side the reverse isolation is quite helpful in preventing stability issues with changing input impedances due to bad probing.

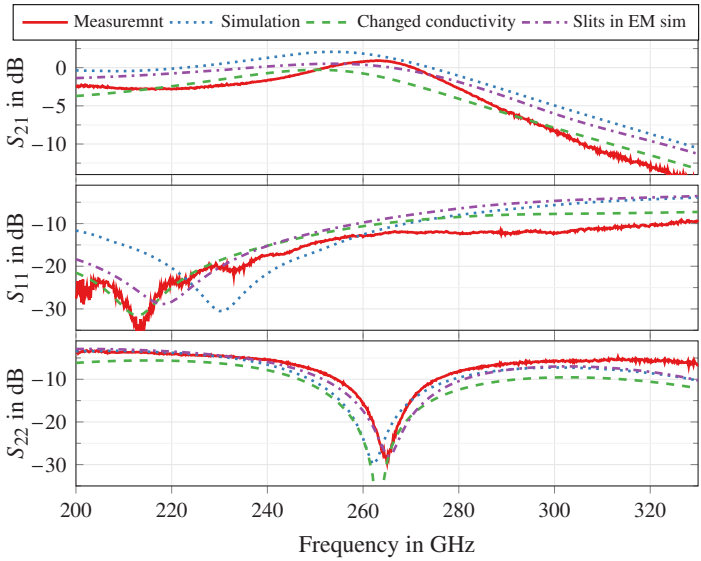


Figure A.13: Simulation and measurement results of the active balun. Plotted in red solid lines is the measurement; in blue dotted lines the simulation without the slits. In green dashed lines the metal conductivity was changed, and in purple the slits were considered in the EM simulation [16].

Table A.1: Performance comparison to other published works [16].

Reference	**Type**	**Freq.**	**IL**	**Amp. Balance**	$\Delta\phi$	**Size**
[AYJN+19]	3-line	94-177	−1.5 dB	1 dB	7°	0.026 mm^2
[AFS15]	Marchand	200-325	−2.3 dB	1.5 dB	10°	0.015 mm^2
[SCE19]	Three-Line	140-220	−0.7 dB	0.6 dB	3°	0.0064 mm^2
[LLK+15]	Active	113-133	−2 dB	1 dB	10°	0.21 mm^2
[YCL+20]	Active	135-165	1.5 dB	0.35 dB	5°	n.a
This [16]	Marchand	200-330	−2.5 dB	1.5 dB	2°	0.02 mm^2
This [16]	Active	237-277	1([a]) dBm	0.5 dB	5°	0.0168 mm^2

[a] After deembedding output balun losses.

References

[AAKG23] Wijdan K. Alsaedi, Hamed Ahmadi, Zaheer Khan, and David Grace. Spectrum options and allocations for 6G: A regulatory and standardization review. *IEEE Open Journal of the Communications Society*, 4:1787–1812, 2023.

[AdGW+22] Ibrahim Abdo, Carrel da Gomez, Chun Wang, Kota Hatano, Qi Li, Chenxin Liu, Kiyoshi Yanagisawa, Ashbir Aviat Fadila, Takuya Fujimura, Tsuyoshi Miura, Korkut Kaan Tokgoz, Jian Pang, Hiroshi Hamada, Hideyuki Nosaka, Atsushi Shirane, and Kenichi Okada. A bi-directional 300-GHz-band phased-array transceiver in 65-nm CMOS with outphasing transmitting mode and LO emission cancellation. *IEEE Journal of Solid-State Circuits*, 57(8):2292–2308, 2022.

[AFS15] Faisal Ahmed, Muhammad Furqan, and Andreas Stelzer. A 200–325 GHz wideband, low-loss modified marchand balun in SiGe BiCMOS technology. In *2015 European Microwave Conference (EuMC)*, pages 40–43, 2015.

[AFS18] Faisal Ahmed, Muhammad Furqan, and Andreas Stelzer. 120-GHz and 240-GHz broadband bow-tie antennas in eWLB package for high resolution radar applications. In *2018 48th European Microwave Conference (EuMC)*, pages 1109–1112, 2018.

[AGB+21] Shivang Aggarwal, Moinak Ghoshal, Piyali Banerjee, Dimitrios Koutsonikolas, and Joerg Widmer. 802.11ad in smartphones: Energy efficiency, spatial reuse, and impact on applications. In *IEEE INFOCOM 2021 - IEEE Conference on Computer Communications*, pages 1–10, 2021.

[ASS+21] Ahmed S. H. Ahmed, Utku Soylu, Munkyo Seo, Miguel Urteaga, and Mark J. W. Rodwell. A compact H-band power amplifier with high output power. In *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 123–126, 2021.

[AYJN+19] Abdul Ali, Jongwon Yun, Herman Jalli Ng, Dietmar Kissinger, Franco Giannini, and Paolo Colantonio. High performance asymmetric coupled line balun at sub-THz frequency. *Applied Sciences*, 9(9), 2019.

[Bal16] Constantine A Balanis. *Antenna theory*. Wiley-Blackwell, Hoboken, NJ, 4 edition, jan 2016.

[BGH+21] Thomas Bücher, Janusz Grzyb, Philipp Hillger, Holger Rücker, Bernd Heinemann, and Ullrich R. Pfeiffer. A 239–298 GHz power amplifier in an advanced 130 nm SiGe BiCMOS technology for communications applications. In *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, pages 369–372, 2021.

[BGH+22] Thomas Bücher, Janusz Grzyb, Philipp Hillger, Holger Rücker, Bernd Heinemann, and Ullrich R. Pfeiffer. A broadband 300 GHz power amplifier in a 130 nm SiGe BiCMOS technology for communication applications. *IEEE Journal of Solid-State Circuits*, 57(7):2024–2034, 2022.

[BGS+16] Akanksha Bhutani, Benjamin Goettel, Thomas Streitz, Steffen Scherr, Wolfgang Winkler, and Thomas Zwick. Low-cost antenna-in-package solution for 122 GHz radar module. In *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, pages 540–543, 2016.

[BK20] Soma Banerjee and Kamal K. Kar. *Introduction to Liquid Crystalline Polymers*, pages 1–26. Springer Berlin Heidelberg, Berlin, Heidelberg, 2020.

[BKU24] Kaan Balaban, Mehmet Kaynak, and Ahmet Çağrı Ulusoy. A highly efficient 240-GHz power amplifier in 0.13-um SiGe. *IEEE Microwave and Wireless Technology Letters*, 34(1):88–91, 2024.

[BRD+11] S. Beer, B. Ripka, S. Diebold, H. Gulan, C. Rusch, P. Pahl, and T. Zwick. Design and measurement of matched wire bond and flip chip interconnects for D-band system-in-package applications. In *2011 IEEE MTT-S International Microwave Symposium*, pages 1–4, 2011.

[BRN+21] James F. Buckwalter, Mark J. W. Rodwell, Kang Ning, Ahmed Ahmed, Andrea Arias-Purdue, Jeff Chien, Everett O'Malley,

and Eythan Lam. Fundamental limits of high-efficiency silicon and compound semiconductor power amplifiers in 100-300 GHz bands. *ITU Journal on Future and Evolving Technologies*, 2(7):39–50, October 2021.

[BZ10] Stefan Beer and Thomas Zwick. Probe based radiation pattern measurements for highly integrated millimeter-wave antennas. In *Proceedings of the Fourth European Conference on Antennas and Propagation*, volume 1, pages 1–5, 2010.

[CBZL23] Shuyuan Chu, Akanksha Bhutani, Thomas Zwick, and Teng Li. A sub-terahertz metasurface on-chip antenna. In *2023 IEEE 11th Asia-Pacific Conference on Antennas and Propagation (APCAP)*, volume volume1, pages 1–2, 2023.

[CCL+10] Alain Chantre, Pascal Chevalier, Thomas Lacave, Gregory Avenier, Michel Buczko, Yves Campidelli, Linda Depoyan, Ludovic Berthier, and Christophe Gacquière. Pushing conventional SiGe HBT technology towards "dotfive" terahertz. In *The 5th European Microwave Integrated Circuits Conference*, pages 21–24, 2010.

[Chu48] L. J. Chu. Physical Limitations of Omni-Directional Antennas. *Journal of Applied Physics*, 19(12):1163–1175, 12 1948.

[CZHN09] Zhiming Chen, Yue Ping Zhang, Ai Qun Hu, and Tung-sang Ng. Bit-error-rate analysis of UWB radio using BPSK modulation over inter-chip radio channels for wireless chip area networks. *IEEE Transactions on Wireless Communications*, 8(5):2379–2387, 2009.

[DLC+22] Ramraj Dangi, Praveen Lalwani, Gaurav Choudhary, Ilsun You, and Giovanni Pau. Study and investigation on 5G technology: A systematic review. *Sensors*, 22(1), 2022.

[DLL+15] Xiao-Dong Deng, Yihu Li, Jiankang Li, Chao Liu, Wen Wu, and Yong-Zhong Xiong. A 320-GHz 1×4 fully integrated phased array transmitter using 0.13-μm SiGe BiCMOS technology. *IEEE Transactions on Terahertz Science and Technology*, 5(6):930–940, 2015.

[DR24] Carl D'heer and Patrick Reynaert. When high-speed communication hits a speed bump: Exploring shannon's equation in mm-wave links. *IEEE Microwave Magazine*, 25(6):41–57, 2024.

[dRST+23] David del Rio, Juan F. Sevillano, Rolando Torres, Andoni Irizar, Pascal Roux, Mahmoud M. Pirbazari, Andrea Mazzanti, Jussi Säily, Antti Lamminen, Jesús de Cos, Mario Giovanni Luigi Frecassetti, Maurizio Moretto, Andrea Pallotta, and Vladimir Ermolov. A D-band 16-element phased-array transceiver in 55-nm BiCMOS. *IEEE Transactions on Microwave Theory and Techniques*, 71(2):854–869, 2023.

[EHH+20] Mohamed Elkhouly, Michael J. Holyoak, David Hendry, Mike Zierdt, Amit Singh, Mustafa Sayginer, Shahriar Shahramian, and Yves Baeyens. D-band phased-array TX and RX front ends utilizing radio-on-glass technology. In *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 91–94, 2020.

[Ele23] Electronic Communications Committee. The european table of frequency allocations and applications in the frequency range 8.3 kHz to 3000 GHz (eca table). Technical report, ECC, 2023.

[EMK19] Mohamed Hussein Eissa, Andrea Malignaggi, and Dietmar Kissinger. A 13.5-dBm 200–255-GHz 4-way power amplifier and frequency source in 130-nm BiCMOS. *IEEE Solid-State Circuits Letters*, 2(11):268–271, 2019.

[EMW+18] Mohamed Hussein Eissa, Andrea Malignaggi, Ruoyu Wang, Mohamed Elkhouly, Klaus Schmalz, Ahmet Cagri Ulusoy, and Dietmar Kissinger. Wideband 240-GHz Transmitter and Receiver in BiCMOS Technology With 25-Gbit/s Data Rate. *IEEE Journal of Solid-State Circuits*, 53(9):2532–2542, September 2018.

[Fed22] Federal Communications Commission. FCC online table of frequency allocations. Technical report, FCC, 2022.

[FR15] Brecht François and Patrick Reynaert. Highly linear fully integrated wideband RF PA for LTE-advanced in 180-nm SOI. *IEEE Transactions on Microwave Theory and Techniques*, 63(2):649–658, 2015.

[Fuj24] Minoru Fujishima. Advancements in terahertz communication: Harnessing the 300GHz band for high-efficiency, high-capacity wireless networks. *IEICE Transactions on Electronics*, advpub:2023CTI0002, 2024.

[GPK+17] Benjamin Goettel, Philipp Pahl, Christoph Kutschker, Stefan Malz, Ullrich R. Pfeiffer, and Thomas Zwick. Active multiple feed on-chip antennas with efficient in-antenna power combining operating at 200–320 GHz. *IEEE Transactions on Antennas and Propagation*, 65(2):416–423, 2017.

[GRB+23] Georg Gramlich, Martin Römhild, Holger Baur, Akanksha Bhutani, Uli Lemmer, Norbert Fruehauf, and Thomas Zwick. Ultra-precise deposition (upd) printing for millimeter wave interconnects in D-band. In *2023 Asia-Pacific Microwave Conference (APMC)*, pages 1–3, 2023.

[GRVM+22] Janusz Grzyb, Pedro Rodríguez-Vázquez, Stefan Malz, Marcel Andree, and Ullrich R. Pfeiffer. A SiGe HBT 215–240 GHz DCA IQ TX/RX chipset with built-in test of USB/LSB RF asymmetry for 100+ Gb/s data rates. *IEEE Transactions on Microwave Theory and Techniques*, 70(3):1696–1714, 2022.

[GSSP15] J. Grzyb, K. Statnikov, N. Sarmah, and U.R. Pfeiffer. A lens-integrated on-chip circular slot antenna for a 240 GHz power source in SiGe technology. In *2015 IEEE International Symposium on Antennas and Propagation and USNC/URSI National Radio Science Meeting*, pages 2055–2056, 2015.

[GTC14] Mats Gustafsson, Doruk Tayli, and Marius Cismasu. *Physical Bounds of Antennas*, pages 1–32. Springer Singapore, Singapore, 2014.

[GUR17] Zach Griffith, Miguel Urteaga, and Petra Rowell. 180–265 GHz, 17–24 dBm output power broadband, high-gain power amplifiers in InP HBT. In *2017 IEEE MTT-S International Microwave Symposium (IMS)*, pages 973–976, 2017.

[GWB+18] Benjamin Goettel, Wolfgang Winkler, Akanksha Bhutani, Florian Boes, Mario Pauli, and Thomas Zwick. Packaging solution for a millimeter-wave system-on-chip radar. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 8(1):73–81, 2018.

[GZGO23] Suprovo Ghosh, Frank Zhang, Haidong Guo, and Kenneth K. O. 305-GHz cascode power amplifier using capacitive feedback fabricated using SiGe HBTs with fmax of 450 GHz. In *2023*

IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pages 313–316, 2023.

[Ham50] R. W. Hamming. Error detecting and error correcting codes. *The Bell System Technical Journal*, 29(2):147–160, 1950.

[Han81] R.C. Hansen. Fundamental limitations in antennas. *Proceedings of the IEEE*, 69(2):170–182, 1981.

[Har60] Roger F. Harrington. Effect of antenna size on gain, bandwidth, and efficiency. *Journal of Research of the National Bureau of Standards, Section D: Radio Propagation*, page 1, 1960.

[HCY+13] Ganesh Hariharan, Raghunandan Chaware, Laurene Yip, Inderjit Singh, Kenny Ng, S. Y. Pai, Myongseob Kim, Henley Liu, and Suresh Ramalingam. Assembly process qualification and reliability evaluations for heterogeneous 2.5D FPGA with HiCTE ceramic. In *2013 IEEE 63rd Electronic Components and Technology Conference*, pages 904–908, 2013.

[HCYH18] Debin Hou, Jixin Chen, Pinpin Yan, and Wei Hong. A 270 GHz × 9 multiplier chain MMIC with on-chip dielectric-resonator antenna. *IEEE Transactions on Terahertz Science and Technology*, 8(2):224–230, 2018.

[HKP15] Ronny Hahnel, Bernhard Klein, and Dirk Plettemeier. Integrated stacked vivaldi-shaped on-chip antenna for 180 GHz. In *2015 IEEE International Symposium on Antennas and Propagation & USNC/URSI National Radio Science Meeting*, pages 1448–1449, 2015.

[HMK+24] Shinsuke Hara, Mohamed H. Mubarak, Akifumi Kasamatsu, Yoshiki Sugimoto, Kunio Sakakibara, Kyoya Takano, Takeshi Yoshida, Shuhei Amakawa, and Minoru Fujishima. 25.9-Gb/s 259-GHz phased-array CMOS receiver module with 28° steering range. In *2024 IEEE Radio and Wireless Symposium (RWS)*, pages 1–4, 2024.

[HNSK+21] S. M. Hossein Naghavi, Saghar Seyedabbaszadehesfahlani, Farzad Khoeini, Andreia Cathelin, and Ehsan Afshari. A 250 GHz autodyne FMCW radar in 55nm BiCMOS with micrometer range resolution. In *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, volume 64, pages 320–322, 2021.

[HWGH10] Jürgen Hasch, Uwe Wostradowski, Stefan Gaier, and Thomas Hansen. 77 GHz radar transceiver with dual integrated antenna elements. In *German Microwave Conference Digest of Papers*, pages 280–283, 2010.

[HWH19] Zhi Hu, Cheng Wang, and Ruonan Han. A 32-unit 240-GHz heterodyne receiver array in 65-nm CMOS with array-wide phase locking. *IEEE Journal of Solid-State Circuits*, 54(5):1216–1227, 2019.

[IEE17] IEEE. IEEE standard for high data rate wireless multi-media networks–amendment 2: 100 Gb/s wireless switched point-to-point physical layer. *IEEE Std 802.15.3d-2017 (Amendment to IEEE Std 802.15.3-2016 as amended by IEEE Std 802.15.3e-2017)*, pages 1–55, 2017.

[ITU05] ITU Telecommunication Standardization Sector. ITU-T rec. G.975.1 (02/2004) forward error correction for high bit-rate DWDM submarine systems. Technical report, ITU-T, 2005.

[JBP13] T. Jaeschke, C. Bredendiek, and N. Pohl. A 240 GHz ultra-wideband FMCW radar system with on-chip antennas for high resolution radar imaging. In *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, pages 1–4, 2013.

[JKHP15] Michael Jenning, Bernhard Klein, Ronny Hahnel, and Dirk Plettemeier. On-chip integrated antennas for 200 GHz applications. In *2015 IEEE International Conference on Ubiquitous Wireless Broadband (ICUWB)*, pages 1–5, 2015.

[Joh65] E. Johnson. Physical limitations on frequency and power parameters of transistors. In *1958 IRE International Convention Record*, volume 13, pages 27–34, 1965.

[JP14] Michael Jenning and Dirk Plettemeier. 180 GHz on-chip integrated bow-tie antenna. In *2014 IEEE Antennas and Propagation Society International Symposium (APSURSI)*, pages 362–363, 2014.

[JSM18] Karl Jacob, Arne Schröder, and Axel Murk. Design, manufacturing, and characterization of conical blackbody targets with optimized profile. *IEEE Transactions on Terahertz Science and Technology*, 8(1):76–84, 2018.

[JTL+20] Laurenz John, Axel Tessmann, Arnulf Leuther, Philipp Neininger, Thomas Merkle, and Thomas Zwick. Broadband 300-GHz power amplifier MMICs in InGaAs mHEMT technology. *IEEE Transactions on Terahertz Science and Technology*, 10(3):309–320, 2020.

[KAKM23] Alper Karakuzulu, Wael Abdullah Ahmad, Dietmar Kissinger, and Andrea Malignaggi. A four-channel bidirectional D-band phased-array transceiver for 200 Gb/s 6G wireless communications in a 130-nm BiCMOS technology. *IEEE Journal of Solid-State Circuits*, 58(5):1310–1322, 2023.

[KBM+15] Ingmar Kallfass, Florian Boes, Tobias Messinger, Jochen Antes, Anns Inam, Ulrich Lewark, Axel Tessmann, and Ralf Henneberger. 64 Gbit/s transmission over 850 m fixed wireless link at 240 GHz carrier frequency. *Journal of Infrared, Millimeter, and Terahertz Waves*, 36(2):221–233, February 2015.

[KKBF14] David P. Kopp, Mohammad A. A. Khan, Gary H. Bernstein, and Patrick Fay. Ultra-broadband chip-to-chip interconnects to 220 GHz for Si-based millimeter-wave systems. In *IEEE International Interconnect Technology Conference*, pages 293–296, 2014.

[KTA+16] K. Katayama, K. Takano, S. Amakawa, S. Hara, A. Kasamatsu, K. Mizuno, K. Takahashi, T. Yoshida, and M. Fujishima. A 300 GHz CMOS transmitter with 32-QAM 17.5 Gb/s/ch capability over six channels. *IEEE Journal of Solid-State Circuits*, 51(12):3037–3048, 2016.

[Kur65] K. Kurokawa. Power waves and the scattering matrix. *IEEE Transactions on Microwave Theory and Techniques*, 13(2):194–202, 1965.

[LCH+20] Huanbo Li, Jixin Chen, Debin Hou, Peigen Zhou, Jiayang Yu, Pinpin Yan, Lin Peng, Haiyan Lu, and Wei Hong. A 250-GHz differential SiGe amplifier with 21.5-dB gain for sub-THz transmitters. *IEEE Transactions on Terahertz Science and Technology*, 10(6):624–633, 2020.

[LCL+21] Zekun Li, Jixin Chen, Huanbo Li, Zuojun Wang, Debin Hou, Pinpin Yan, Zhe Chen, and Wei Hong. A 220-GHz power amplifier with 22.5-dB gain and 9-dBm Psat in 130-nm SiGe. *IEEE Mi-*

crowave and Wireless Components Letters, 31(10):1166–1169, 2021.

[LCZ+22] Xingcun Li, Wenhua Chen, Peigen Zhou, Yunfan Wang, Fei Huang, Shuyang Li, Jixin Chen, and Zhenghe Feng. A 250–310 GHz power amplifier with 15-dB peak gain in 130-nm SiGe BiCMOS process for terahertz wireless system. *IEEE Transactions on Terahertz Science and Technology*, 12(1):1–12, 2022.

[LGB+17] Elsa Lacombe, Frederic Gianesello, Aimeric Bisognin, Cyril Luxey, Diane Titz, Heiko Gulan, and Thomas Zwick. 240 GHz antenna integrated on low-cost organic substrate packaging technology targeting high-data rate sub-THz telecommunication. In *2017 47th European Microwave Conference (EuMC)*, pages 164–167, 2017.

[LKLS24] Seunghoon Lee, Junhyeong Kim, Kangseop Lee, and Ho-Jin Song. 248-GHz subharmonic mixer last transmitter with I/Q imbalance and LO feedthrough calibration. *IEEE Solid-State Circuits Letters*, 7:159–162, 2024.

[LLK+15] Chae Jun Lee, Hae Jin Lee, Dongmin Kang, In Sang Song, Hong Yi Kim, Seong Jun Cho, Joong Geun Lee, In-Yeal Oh, and Chul Soon Park. 120vGHz low power, high gain, wideband active balun for chip-to-chip communication. In *2015 IEEE 15th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pages 18–20, 2015.

[LLK+23] Dongmin Lee, Ahnwoo Lee, Minchul Kim, Wonseok Choe, Chungsik Lee, Kwansun Yoon, Mingeun Jeong, and Junghyun Kim. Modeling of practical substrate thickness in multilayer printed circuit board for millimeter-wave packaging. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 13(4):511–519, 2023.

[LRJ+18] Q. Liu, A.C.F. Reniers, U. Johannsen, M.C. van Beurden, and A. B. Smolders. Influence of on-wafer probes in mm-wave antenna measurements. In *12th European Conference on Antennas and Propagation (EuCAP 2018)*, volume 1, pages 1–5, 2018.

[LSAL+20] Antti Lamminen, Jussi Säily, Juha Ala-Laurinaho, Jesus de Cos, and Vladimir Ermolov. Patch antenna and antenna array on

multilayer high-frequency PCB for D-band. *IEEE Open Journal of Antennas and Propagation*, 1:396–403, 2020.

[LTW+14] U. J. Lewark, A. Tessmann, S. Wagner, A. Leuther, T. Zwick, and I. Kallfass. A 220 to 320 GHz broadband active frequency multiplier-by-eight MMIC. In *2014 9th European Microwave Integrated Circuit Conference*, pages 132–135, 2014.

[LZRR22] Siwei Li, Zhe Zhang, Bhaskara Rupakula, and Gabriel M. Rebeiz. An eight-element 140-GHz wafer-scale IF beamforming phased-array receiver with 64-QAM operation in CMOS RFSOI. *IEEE Journal of Solid-State Circuits*, 57(2):385–399, 2022.

[MA89] G.F. Mikucki and A.K. Agrawal. A broad-band printed circuit hybrid ring power divider. *IEEE Transactions on Microwave Theory and Techniques*, 37(1):112–117, 1989.

[MKK+22] E Meyer, D Kruglov, M Krivic, M Tanveer, R Argaez-Ramirez, Y Zhang, A Briseno Ojeda, K Smirnova, K Alekseev, M Safari Mugisho, B Cimbili, N Farid, Y Dang, M Shahid, M Ensan, J Banar, H Bao, M Matters-Kammerer, U Gustavsson, F Demuynck, T Zwick, M Acar, C Fager, M van der Heijden, M Ivashina, D Caratelli, M Hasselblad, C Ulusoy, AB Smolders, K Eriksson, M Johannson, R Maaskant, R Quay, D Floriot, M Bao, LA Bronckers, J Fridén, MC van Beurden, BP de Hon, C Kolitsidas, D Blanco, FMJ Willems, T Eriksson, A Filippi, F Ponzini, and U Johannsen. The state of the art in beyond 5G distributed massive multiple-input multiple-output communication system solutions. *Open Research Europe*, 2(106), 2022.

[ML22] Michael P. McGarry and Mark Lee. Broadband dielectric properties of integrated circuit packaging materials across the 6G spectrum. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 12(9):1575–1582, 2022.

[Mom13] Omeed Momeni. A 260GHz amplifier with 9.2dB gain and -3.9dBm saturated power in 65nm CMOS. In *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pages 140–141, 2013.

[NH20] Thanh Dat Nguyen and Jong-Phil Hong. A high fundamental frequency sub-THz CMOS oscillator with a capacitive load re-

duction circuit. *IEEE Transactions on Microwave Theory and Techniques*, 68(7):2655–2667, 2020.

[NHSN+13] Muhammad Imran Nawaz, Zhao Huiling, Muhammad Sabir Sultan Nawaz, Khalid Zakim, Shah Zamin, and Aurangzeb Khan. A review on wideband microstrip patch antenna design techniques. In *2013 International Conference on Aerospace Science and Engineering (ICASE)*, pages 1–8, 2013.

[PA20] Gia Ngoc Phung and Uwe Arz. Parasitic probe effects in measurements of coplanar waveguides with narrow ground width. In *2020 IEEE 24th Workshop on Signal and Power Integrity (SPI)*, volume 1, pages 1–4, 2020.

[PAB+21] Aarno Pärssinen, Mohamed-Slim Alouini, Markus Berg, Thomas Kuerner, Pekka Kyösti, Marko E. Leinonen, Marja Matinmikko-Blue, Earl McCune, Ullrich Pfeiffer, and Piet Wambacq. White paper on RF enabling 6G – opportunities and challenges from technology to spectrum. In *White Paper on RF Enabling 6G – Opportunities and Challenges From Technology to Spectrum*, 2021.

[PKT+12] Jung-Dong Park, Shinwon Kang, Siva V Thyagarajan, Elad Alon, and Ali M. Niknejad. A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication. In *2012 Symposium on VLSI Circuits (VLSIC)*, pages 48–49, 2012.

[PM18] Kumari Pushpa and Priyanka Mondal. A frequency tripler with suppressed harmonics for millimeter-wave applications. In *2018 3rd International Conference on Microwave and Photonics (ICMAP)*, pages 1–2, 2018.

[Poz05] David M Pozar. *Microwave engineering; 3rd ed.* Wiley, Hoboken, NJ, 2005.

[QAU19] J. A. Qayyum, J. D. Albrecht, and A. C. Ulusoy. A compact V-band upconversion mixer with 1.4-dBm OP1dB in SiGe HBT technology. *IEEE Microwave and Wireless Components Letters*, 29(4):276–278, April 2019.

[Raz98] Behzad Razavi. *Rf Microelectronics*. Prentice Hall, 1998.

[RLP+22] Georg Rademacher, Ruben S. Luís, Benjamin J. Puttnam, Nicolas K. Fontaine, Mikael Mazur, Haoshuo Chen, Roland Ryf,

David T. Neilson, Daniel Dahl, Joel Carpenter, Pierre Sillard, Frank Achten, Marianne Bigot, Jun Sakaguchi, and Hideaki Furukawa. 153 Peta-bit/s C-band transmission in a 55-mode fiber. In *European Conference on Optical Communication (ECOC) 2022*, page Th3C.3. Optica Publishing Group, 2022.

[RvDSH15] Ad C. F. Reniers, A. Rainier van Dommele, A. Bart Smolders, and Matti H. A. J. Herben. The influence of the probe connection on mm-wave antenna measurements. *IEEE Transactions on Antennas and Propagation*, 63(9):3819–3825, 2015.

[RVGHP19] Pedro Rodríguez-Vázquez, Janusz Grzyb, Bernd Heinemann, and Ullrich R. Pfeiffer. A 16-QAM 100-Gb/s 1-m wireless link with an EVM of 17GHz in an SiGe technology. *IEEE Microwave and Wireless Components Letters*, 29(4):297–299, 2019.

[RVGS+18] Pedro Rodriguez-Vazquez, Janusz Grzyb, Neelanjan Sarmah, Bernd Heinemann, and Ullrich R. Pfeiffer. A 65 Gbps QPSK one meter wireless link operating at a 255 GHz tunable carrier in a SiGe HBT technology. In *2018 IEEE Radio and Wireless Symposium (RWS)*. IEEE, January 2018.

[SBd+16] M. Schroter, J. Boeck, V. d'Alessandro, S. Fregonese, B. Heinemann, C. Jungemann, W. Liang, H. Kamrani, A. Mukherjee, A. Pawlak, U. Pfeiffer, N. Rinaldi, N. Sarmah, T. Zimmer, and G. Wedel. The EU DOTSEVEN project: Overview and results. In *2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pages 1–4, 2016.

[SCE19] Paul Stärke, Corrado Carta, and Frank Ellinger. A deembedding method for reciprocal three-port devices demonstrated with 200-GHz baluns. *IEEE Microwave and Wireless Components Letters*, 29(1):11–13, 2019.

[SCE22] L. Steinweg, C. Carta, and F. Ellinger. A 100-GHz-RF-bandwidth up-conversion mixer in 130 nm SiGe BiCMOS. In *2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2022.

[SDS+17] Siddhartha Sinha, Ralf Doerner, Franz-Josef Schmückle, Sirinpa Monayakul, Michael Hrobak, Nils G. Weimann, Viktor Krozer, and Wolfgang Heinrich. Flip-chip approach for 500 GHz broad-

band interconnects. *IEEE Transactions on Microwave Theory and Techniques*, 65(4):1215–1225, 2017.

[SMK+99] T. Shimoto, K. Matsui, K. Kikuchi, Y. Shimada, and K. Utsumi. New high-density multilayer technology on PCB. *IEEE Transactions on Advanced Packaging*, 22(2):116–122, 1999.

[SNS22] Seckin Sahin, Niru K. Nahar, and Kubilay Sertel. Noncontact characterization of antenna parameters in mmW and THz bands. *IEEE Transactions on Terahertz Science and Technology*, 12(1):42–52, 2022.

[SRG+21] Klaus Schmalz, Nick Rothbart, Alexandra Glück, Mohamed Hussein Eissa, Thomas Mausolf, Esref Turkmen, Selahattin Berk Yilmaz, and Heinz-Wilhelm Hübers. Dual-band transmitter and receiver with bowtie-antenna in 0.13 μm SiGe BiCMOS for gas spectroscopy at 222 - 270 GHz. *IEEE Access*, 9:124805–124816, 2021.

[SRI06] Rishad Ahmed Shafik, Md. Shahriar Rahman, and AHM Razibul Islam. On the extended relationships among EVM, BER and SNR as performance metrics. In *2006 International Conference on Electrical and Computer Engineering*, pages 408–411, 2006.

[SRS+20] Luca Steinweg, Vincent Rieß, Paul Stärke, Paolo Valerio Testa, Corrado Carta, and Frank Ellinger. A low-power 255-GHz single-stage frequency quadrupler in 130-nm SiGe BiCMOS. *IEEE Microwave and Wireless Components Letters*, 30(11):1101–1104, November 2020.

[STCE21] Luca Steinweg, Paolo Valerio Testa, Corrado Carta, and Frank Ellinger. A 5 dBm BiCMOS 90° phase shifter with single-voltage tuning for mm-wave beam steering. In *2021 International Conference on Microelectronics (ICM)*. IEEE, December 2021.

[Ste23] Luca Steinweg. *Analysis and Design of a Sub-THz Ultra-Wideband Phased-Array Transmitter*. Qucosa, 2023.

[TAK+17] Kyoya Takano, Shuhei Amakawa, Kosuke Katayama, Shinsuke Hara, Ruibing Dong, Akifumi Kasamatsu, Iwao Hosako, Koichi Mizuno, Kazuaki Takahashi, Takeshi Yoshida, and Minoru Fujishima. A 105Gb/s 300GHz CMOS transmitter. In *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 308–309, 2017.

[TCE18] Paolo Valerio Testa, Corrado Carta, and Frank Ellinger. Novel high-performance bondwire chip-to-chip interconnections for applications up to 220 GHz. *IEEE Microwave and Wireless Components Letters*, 28(2):102–104, 2018.

[TFL+15] G. Tretter, D. Fritsche, J.D. Leufker, C. Carta, and F. Ellinger. Zero-ohm transmission lines for millimetre-wave circuits in 28 nm digital CMOS. *Electronics Letters*, 51(11):845–847, 2015.

[TMG+19] Paolo Valerio Testa, Helmuth Morath, Panic Goran, Corrado Carta, and Frank Ellinger. A cost-effective flip-chip interconnection for applications from DC until 200 GHz. In *2019 IEEE Asia-Pacific Conference on Applied Electromagnetics (APACE)*, pages 1–6, 2019.

[TRCE18] Paolo Valerio Testa, Vincent Riess, Corrado Carta, and Frank Ellinger. Analysis and design of laterally and vertically radiating bondwires antennas for the 140–220 GHz band. In *2018 IEEE International RF and Microwave Conference (RFM)*, pages 143–146, 2018.

[TTJ+04] D.C. Thompson, O. Tantot, H. Jallageas, G.E. Ponchak, M.M. Tentzeris, and J. Papapolymerou. Characterization of liquid crystal polymer (LCP) material and transmission lines on LCP substrates from 30 to 110 GHz. *IEEE Transactions on Microwave Theory and Techniques*, 52(4):1343–1352, 2004.

[VHdM+20] Akshay Visweswaran, Alexander Haag, Carmine de Martino, Karina Disch, Tim Maiwald, Bastien Vignon, Klaus Aufinger, Marco Spirito, Thomas Zwick, and Piet Wambacq. An integrated 132-147GHz power source with +27dBm EIRP. In *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 219–222, 2020.

[VSY+15] Václav Valenta, Thomas Spreng, Shuai Yuan, Wolfgang Winkler, Volker Ziegler, Dragos Dancila, Anders Rydberg, and Hermann Schumacher. Design and experimental evaluation of compensated bondwire interconnects above 100 GHz. *International Journal of Microwave and Wireless Technologies*, 7(3-4):261–270, 2015.

[WCA+24] Hua Wang, Kyungsik Choi, Basem Abdelaziz, Mohamed Eleraky, Bryan Lin, Edward Liu, Yuqi Liu, Hossein Jalili, Mohsen Ghorbanpoor, Chenhao Chu, Tzu-Yuan Huang, Naga Sasikanth Mannem, Jeongsoo Park, Jeongseok Lee, David Munzer, Sensen Li, Fei Wang, Amr S. Ahmed, Christopher Snyder, Huy Thong Nguyen, and Michael Edward Duffy Smith. Power amplifiers performance survey 2000-present, 2024.

[WLM24] Hua Wang, Yuqi Liu, and Naga Sasikanth Mannem. Phased array survey 2010-present, 2024.

[WLY23] Peng Wu, Kebin Liu, and Zhongjun Yu. 220 GHz high-gain substrate integrated antennas with low fabrication cost based on higher order mode and PCB technology. *IEEE Transactions on Antennas and Propagation*, 71(1):18–28, 2023.

[WLZ+18] Meng Da Wu, Bin Li, Ying Zhou, Da Lu Guo, Yong Liu, Feng Wei, and Xin Lv. Design and measurement of a 220 GHz wideband 3-D printed dielectric reflectarray. *IEEE Antennas and Wireless Propagation Letters*, 17(11):2094–2098, 2018.

[WRE06] Bruce M. Thompson William R. Eisenstadt, Bob Stengel. *Microwave Differential Circuit Design Using Mixed Mode S-Parameters*. Artech House Publishers, 2006.

[WSE16] Owais Talaat Waheed, Ayman Shabra, and Ibrahim Abe M. Elfadel. Impact of fractional bandwidth on the bit error rate of a beamforming system. In *2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 1–4, 2016.

[XZZ+20] Dongzhu Xu, Anfu Zhou, Xinyu Zhang, Guixian Wang, Xi Liu, Congkai An, Yiming Shi, Liang Liu, and Huadong Ma. Understanding operational 5G: A first measurement study on its coverage, performance and energy consumption. In *SIGCOMM '20: Proceedings of the Annual conference of the ACM Special Interest Group on Data Communication on the applications, technologies, architectures, and protocols for computer communication*, pages 479–494, 07 2020.

[YCL+20] Jiayang Yu, Jixin Chen, Huanbo Li, Peigen Zhou, Debin Hou, Wei Hong, and Pinpin Yan. Transformer matched gilbert mixer

with active balun for D-band transmitter. *Microwave and Optical Technology Letters*, 62(8):2696–2702, 2020.

[YPL23] Byeonghun Yun, Dae-Woong Park, and Sang-Gug Lee. H-Band power amplifiers in 65-nm CMOS by adopting output power maximized Gmax-core and transmission line-based zero-degree power combining networks. *IEEE Journal of Solid-State Circuits*, 58(11):3089–3102, 2023.

[YS15] Shuai Yuan and Hermann Schumacher. 110–140-GHz single-chip reconfigurable radar frontend with on-chip antenna. In *2015 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM*, pages 48–51, 2015.

[YWL+23] Bo Yu, Zhigang Wang, Oupeng Li, Qiao Liu, Hua Cai, Yang Zhou, Guangjian Wang, Bo Yan, Ruimin Xu, and Yuehang Xu. A 200-GHz four-element phased-array receiver system-in-package using HTCC technology for sub-terahertz communications. *IEEE Transactions on Microwave Theory and Techniques*, pages 1–15, 2023.

[YWS+21] Qin-Hong Yang, Lin-Sheng Wu, Li-Yun Shi, Yue-Ping Zhang, and Jun-Fa Mao. Impact of on-wafer probe on the radiation measurement of a filtering antenna-in-package. In *2021 International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, volume 1, pages 1–3, 2021.

[ZCL+23] Rui Zhou, Jixin Chen, Zekun Li, Jiayang Yu, Dawei Tang, and Wei Hong. A 260-GHz power amplifier with 12.5-dBm Psat and 21.4-dB peak gain utilizing a modified coupled-line-balun network. *IEEE Transactions on Microwave Theory and Techniques*, pages 1–15, 2023.

[Zhu10] Vitaliy Zhurbenko. *Advanced Microwave Circuits and Systems*. IntechOpen, Rijeka, Apr 2010.

[ZZ22] Ziyang Zheng and Yue Ping Zhang. A study on the radiation characteristics of microelectronic probes. *IEEE Open Journal of Antennas and Propagation*, 3:4–11, 2022.

[ZZM24] Xin Zhang, Nengxu Zhu, and Fanyi Meng. A 185-to-240 GHz SiGe power amplifier using non-zero base-impedances for power gain and output power optimizations. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 14(1):67–74, 2024.

Own Publications

Journal Articles

[1] Pascal Maier, Alexander Kotz, **Joachim Hebeler**, Qiaoshuang Zhang, Christian Benz, Alexander Quint, Marius Kretschmann, Tobias Harter, Sebastian Randel, Uli Lemmer, Wolfgang Freude, Thomas Zwick, and Christian Koos. Freeform terahertz structures fabricated by multi-photon lithography and metal coating, 2024.

[2] Luca Steinweg, **Joachim Hebeler**, Tilo Meister, Thomas Zwick, and Frank Ellinger. 8.0-pJ/bit BPSK transmitter with LO phase steering and 52-Gbps data rate operating at 246 GHz. In *IEEE Transactions on Microwave Theory and Techniques*, volume 71, pages 3217–3226, 2023.

[3] Matteo Stocchi, Zhibo Cao, Christopher Hardly Joseph, Thomas Voss, Davide Mencarelli, Luca Pierantoni, Canan Baristiran Kaynak, **Joachim Hebeler**, Thomas Zwick, Matthias Wietstruck, and Mehmet Kaynak. Gain enhancement of BiCMOS on-chip sub-THz antennas by mean of meta-cells. *Scientific Reports*, 12(1), 3 2022.

[4] **Joachim Hebeler**, Luca Steinweg, Frank Ellinger, and Thomas Zwick. Wideband BPSK transmitter phased array operating at 246 GHz with ±30° steering range. *IEEE Access*, pages 1–1, 2024.

[5] **Joachim Hebeler**, Luca Steinweg, Thomas Zwick, and Frank Ellinger. Performance evaluation of ultra wideband 246 GHz BPSK transmitters on an organic substrate with external chip and substrate antenna. *IEEE Trans. Microw. Theory Techn.*, pages 1–12, 2024.

[6] **Joachim Hebeler** and Thomas Zwick. Differential wideband antenna on organic substrate at 240 GHz with a differential wirebond package. *Progress In Electromagnetics Research Letters*, 113:35–42, 2023.

[7] **Joachim Hebeler**, Thomas Zwick, and Akanksha Bhutani. Radiation behaviour of mm-wave on-wafer probes in H-band and the influence on antenna measurements. *Electronics Letters*, 60(3):e13116, 2024.

[8] Luca Valenziano, **Joachim Hebeler**, Georg Gramlich, Alexander Quint, Thomas Zwick, and Akanksha Bhutani. Advanced bond-wire interconnect solution for ultra-broadband applications covering DC to 210 GHz. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, pages 1–1, 2024.

[9] Luca Valenziano, **Joachim Hebeler**, Alban Sherifaj, Fabian Thome, Christian Koos, Thomas Zwick, and Akanksha Bhutani. A comprehensive packaging solution from DC to 113 GHz for InGaAs amplifiers. *Electronics Letters*, 60(6):e13143, 2024.

Conference Papers

[10] Christian Bohn, **Joachim Hebeler**, Christian Koos, Thomas Zwick, and Ahmet Çağri Ulusoy. PAM-4 driver amplifier using distributed power combining. In *2021 IEEE MTT-S International Microwave Symposium (IMS)*, pages 390–392, 2021.

[11] Georg Gramlich, **Joachim Hebeler**, Christian Bohn, Uli Lemmer, and Thomas Zwick. Aerosol jet printed microstrip lines on polyimide for D-band. In *2021 51st European Microwave Conference (EuMC)*, pages 551–554, 2022.

[12] Pascal Maier, Alexander Kotz, **Joachim Hebeler**, Qiaoshuang Zhang, Christian Benz, Alexander Quint, Marius Kretschmann, Tobias Harter, Sebastian Randel, Uli Lemmer, Wolfgang Freude, Thomas Zwick, and Christian Koos. 3d freeform millimeter-wave and thz structures based on multi-photon lithography. In *2024 Optical Fiber Communications Conference and Exhibition (OFC)*, pages 1–3, 2024.

[13] Alexander Quint, Luca Valenziano, **Joachim Hebeler**, Thomas Zwick, and Akanksha Bhutani. Modified bisection thru-only deembedding algorithm for long test fixtures. In *2024 IEEE 36th International Conference on Microelectronic Test Structures (ICMTS)*, pages 1–6, 2024.

[14] **Joachim Hebeler**, Akanksha Bhutani, and Thomas Zwick. Design and evaluation of a substrate integrated waveguide with solid side walls for H-band applications on organic substrate. In *2023 53rd European Microwave Conference (EuMC)*, pages 2–5, 2023.

[15] **Joachim Hebeler**, Luca Steinweg, and Thomas Zwick. Differential bondwire interface for chip-to-chip and chip-to-antenna interconnect above 200 GHz. In *2022 52nd European Microwave Conference (EuMC)*, pages 306–309, 2022.

[16] **Joachim Hebeler**, Ahmet Cagri Ulusoy, and Thomas Zwick. Active balun with 40 GHz bandwidth at 257 GHz in 130 nm SiGe:C. In *2022 IEEE 22nd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pages 9–12, 2022.

[17] **Joachim Hebeler**, Ahmet Cagri Ulusoy, and Thomas Zwick. Comparison of a copper and aluminium SiGe BEOL option for power amplifiers above 200 GHz. In *2022 24th International Microwave and Radar Conference, MIKON 2022*, 2022.

[18] **Joachim Hebeler**, Thomas Zwick, and Ahmet Cagri Ulusoy. Design and modelling of magnetic on-chip structures at 240 GHz. In *GeMIC 2020 - Proceedings of the 2020 German Microwave Conference*, pages 172–175, 2020.

[19] Tsung-Ching Tsai, Christian Bohn, **Joachim Hebeler**, Mehmet Kaynak, and Ahmet Çağrı Ulusoy. A linear and efficient power amplifier supporting wideband 64-QAM for 5G applications from 26 to 30 GHz in SiGe:C BiCMOS. In *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 127–130, 2021.