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Performance of the DAQ system of the PANDA Micro-Vertex Detector

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Abstract: The Micro-Vertex Detector (MVD) is the innermost subdetector of the PANDA (anti-Proton ANnihilations at DArmstadt) detector at FAIR. Its microstrip sensors are read out by custom front-end electronics called ToASt (Torino ASIC for Strip readout) [1]. The ToASt chips are locally managed by an MDC (Module Data Concentrator) [2]. The MDC processes incoming event data and forwards them to the off-detector readout cards based on the AMC (Advanced Mezzanine Card) standard. Both the MDC and the AMC readout card are currently under development at KIT [3]. The complete readout chain, including the double-sided microstrip sensor read by the ToASt chips and the FPGA implementation of the MDC, was successfully tested during a 2023 beam test at COSY (Forschungszentrum Jülich). This proof-of-concept validation of the MDC logic paves the way for the forthcoming ASIC version of the MDC, which is planned for submission in February 2025. Extensive performance characterization of the current readout chain has been achieved with the MDC-FPGA optically connected to an AMD-Xilinx ZCU102 evaluation card [4], which emulates the AMC off-detector card, through a Versatile Link+ Demo Board (VLDB+) [5]. This contribution presents the MDC-ASIC design, its integration with both the front-end and back-end electronics and the performance results of the complete readout chain.

Keywords: Data acquisition circuits; Front-end electronics for detector readout; Particle tracking detectors (Solid-state detectors); VLSI circuits

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1 Introduction

This paper presents the data acquisition system for the MVD (Micro-Vertex Detector) of the PANDA experiment [6]. The MVD, which will be placed in the innermost detector layer, will provide high-resolution tracking for primary interactions and secondary vertices of short-lived particles and delayed decays. It will consist of both pixel and double-sided microstrip detectors. Each microstrip detector module will integrate a complex hybrid structure that includes sensors, front-end chips, local data concentrators, and cooling pipes, all mounted on a lightweight carbon fiber support. The DAQ system for PANDA will employ a trigger-less acquisition model, allowing sub-detectors to operate continuously in a free-running mode. Data are zero-suppressed and only data with events are transmitted to COTS (Commercial Off-The-Shelf) computing nodes where the high-level trigger processes data to identify and extract relevant physics events. The paper is organized into two sections. Following the introduction, the first section presents the architecture and layout of the MDC, developed in UMC 110 nm CMOS technology. The second section covers the performance evaluation of the readout chain, along with a summary and conclusions.

2 Module Data Concentrator

The module data concentrator acts as a data controller from/to the front-end chips and the data acquisition (DAQ) system. This chip will be placed on the detector module inside the active area. The MDC is developed using the same commercial UMC 110 nm CMOS technology as the ToASt chip [1]. To ensure reliability in high-radiation environments, SEU (Single Event Upset) mitigation techniques, including triple modular redundancy, will be implemented across all critical logic blocks [7]. An overview of the internal architecture of the MDC is shown in figure 1. The main tasks of the MDC include reading out, decoding, and multiplexing data from the front-end ToASt chips and providing a data interface to the DAQ via two parallel serial lpGBT [8] (low-power GigaBit Transceiver) e-links, each operating at 320 Mb/s in double-data rate mode. Additionally, the MDC provides a time-skew-controlled clock distribution to the ToASt chips, dedicated logic for configuration and slow-control signals, and programmable calibration logic for performing on-detector S-curve calibration.

The MDC supports up to 16 high-speed input channels from the front-end ASICs, enabling a flexible number of front-end chips to be managed ranging from 8 front-end chips (with two links per chip for high-occupancy scenarios) to 16 front-end chips (one link per chip for low-occupancy scenarios) integrated into the detector module. Events are collected by the ToASt and transmitted

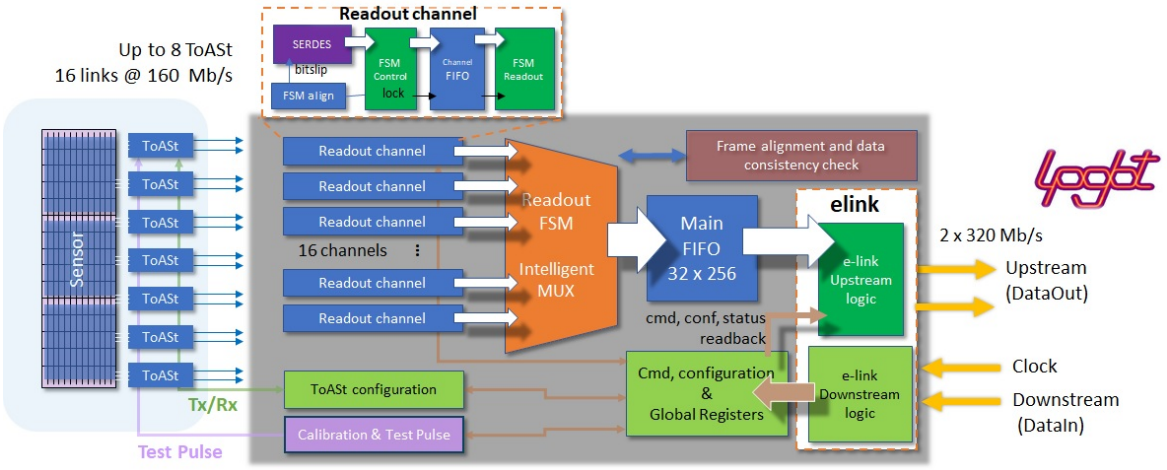

Figure 1. Internal architecture of the MDC, highlighting its core logic blocks: 16 high-speed input channels from front-end chips, a multiplexer for channel selection, an e-link interface compatible with the lpGBT device, command and configuration logic for front-end management and programmable calibration and test pulse logic.

to the MDC via serial lines operating at 160 Mb/s. Each serial line is managed by an input channel, capable of de-serializing the data stream from the ToASt and buffering only the event data in its local channel FIFO. A multiplexing system ensures efficient readout from each channel using a round-robin algorithm. The data are then temporarily stored in the main FIFO before being transmitted to the lpGBT through two parallel upstream connections, each operating at 320 Mb/s in double-data rate mode. Under real experimental conditions, particularly in the high-occupancy regions of the detector, the expected event rate is $\cong 0.31$ Mhits/s per ToASt chip. This corresponds to a data rate of $\cong 10$ Mb/s per chip (32 bits per hit) or $\cong 5$ Mb/s per channel. In high-occupancy scenarios, considering that the microstrip detector module employs 7 ToASt chips, the required data throughput for the MDC to sustain the module's readout is $\cong 70$ Mb/s. This value is below the upstream data link capability of the MDC, which can handle throughput rates of up to 640 Mb/s.

Expanding to 16 input channels is technically motivated, as it broadens the potential applications of the PANDA microstrip detector across various experiments. This flexibility allows for the integration of larger double-sided microstrip sensors, which is particularly valuable for large-area hadron-beam therapy used in tumour treatment, as well as for deployment in different experimental setups. Power consumption of the MDC is a critical design aspect, as it is located on the detector module where cooling resources are limited. To optimize power consumption, the input channels feature an auto-detection capability that activates the internal logic and establishes a data connection only when the serial link is dynamically enabled; otherwise, channels remain in a power-saving mode. The MDC includes command and configuration protection logic that detects and safeguards against potential communication errors from the counting room. If a command is unrecognized or if the sequence of commands is incorrect, the MDC sends an error flag back to the counting room. The configuration sequence for the ToASt is also internally verified by the configuration logic block. If validated, the MDC issues the commands to configure one or multiple ToASt chips in broadcast mode. After writing the configuration to the ToASt, it is automatically read back and compared by the MDC. In the event of any discrepancies, the MDC will automatically issue the necessary instructions to rewrite the configuration registers of the ToASt chips.

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Figure 2. Data distribution across two upstream data links to optimize e-link bandwidth. The data format includes: an MDC header with event number details, a ToASt header identifying the ToASt under readout, the payload data packets, a ToASt trailer indicating the number of channels with events and a CRC (Cyclic Redundancy Check) for error detection, and an MDC trailer reporting the internal status of the MDC.

As shown in figure 1, data temporarily stored in the main FIFO are transmitted to the counting room via two parallel e-link upstream connections. A data-balancing system automatically distributes data across these two channels to maximize e-link bandwidth. In cases of high data occupancy, data are evenly split between the two links, as illustrated in figure 2. When only a small amount of data needs to be sent, data are transmitted through link 0, avoiding the need to duplicate header and trailer packets. Thanks to its data balancing mechanism, the MDC is capable of supporting a detector occupancy of up to 50%. Programmable calibration and test pulse logic have been implemented to simplify and reduce the execution time for the detector calibration by the S-curves method. This logic block enables precise characterization of both the Time-over-Threshold (ToT) and Time-of-Arrival (ToA) for the ToASt chips. After configuring the global and local threshold parameters and setting the amplitude of the test pulse to be injected through the ToASt's integrated test capacitance, the MDC provides full programmability for the number of test pulses, their polarity, and the delay (in 6.25 ns increments) between an internal reference and the test pulse edge. Upon receiving the test pulse enable command, the MDC logic generates the test pulse sequences distributing the signal in parallel across all ToASt chips. The test pulse data are automatically sent to the counting room.

2.1 Layout implementation

The ASIC implements two independent power and ground domains for the IO pads and the digital core. To ensure a uniform power distribution across the digital core, four power rings enclosing the digital domain have been implemented. Both the digital core and the custom sLVS drivers and receivers are powered at 1.2 V. The final die dimensions including the seal-ring are $3.38 \times 3.38\ \mathrm{mm}^2$, which is suitable for the integration on the detector module. Figure 3 shows the final layout of the MDC ASIC including the sixteen input channels with the channel FIFO, the large main FIFO, the configuration logic block, the IO interface with pads on all four sides of the die and the central part covered completely by the readout core logic. To balance the speed and the low-power requirements several technology options have been employed for the final layout. Standard process regular Vt transistors were applied to the digital core logic, low-leakage transistors were selected for all FIFO blocks, and high-speed transistors were used for the sLVS drivers and receivers. This configuration results in a preliminary power consumption of approximately 51 mW at a 333 MHz clock toggle rate, where the static leakage power contributes only 0.14% of the total power consumption. As shown in figure 3, both channels and the main FIFO blocks, occupy a large fraction of area resources.

To optimize the area alongside the power consumption constraints, all memory blocks were implemented using of memory generator IPcore provided by Faraday Technology [9] in the low-leakage

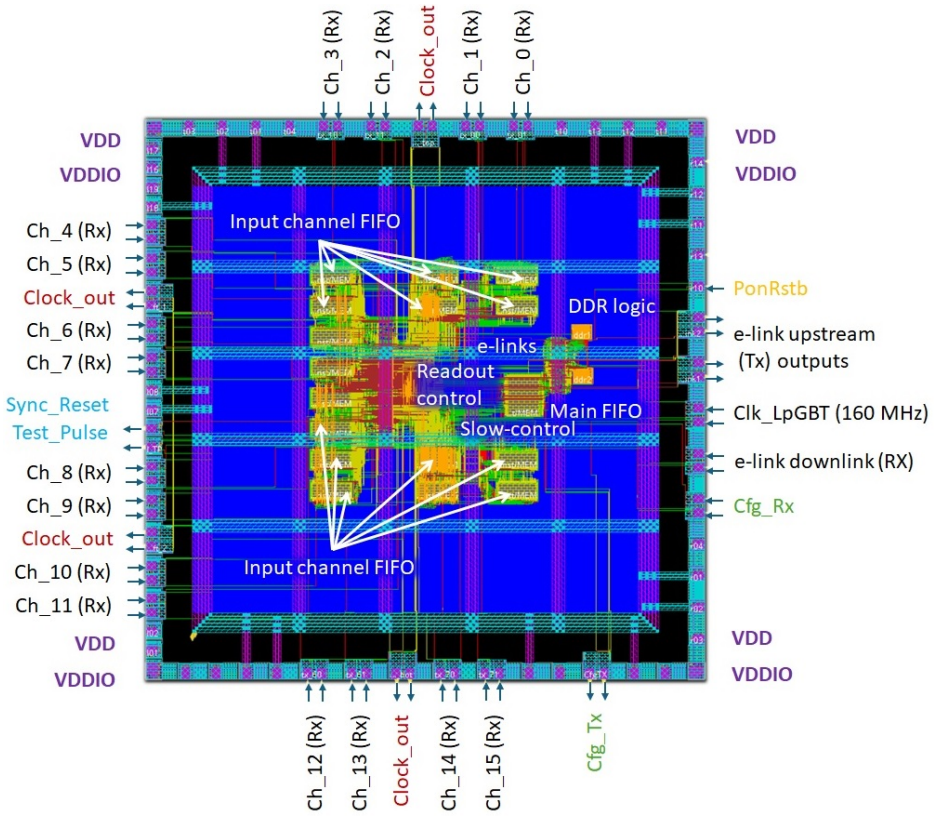

Figure 3. Final layout of the MDC ASIC.

process. This approach reduced power consumption by a factor of three compared to a full standard cell implementation and reduced occupancy from 40% (full standard cell implementation) down to 3.7% for the entire chip. To provide a robust and high-performance data throughput, the two e-links upstream (output) are driven by the Double-Data-Rate (DDR) logic block developed by INFN Turin and already successfully integrated into several ASICs. The DDR logic provides a very efficient parallel-to-serial conversion combined with an 8b/10b encoder logic. To ensure maximum flexibility of the placement and routing of the logic core, the standard cells are placed by flat-design mode where only, the FIFOs and the DDRs blocks are locally constrained.

3 MDC test setup and performance

A dedicated test setup was developed to validate the logic functionality of the MDC, as shown in figure 4. The setup consists of two ToASt chips connected to the Module Data Concentrator (MDC), which is implemented on an FPGA, via four sLVS serial lines. On the right side of the left figure, a ZYNQ evaluation card [4] simulates the off-detector electronics. Additionally, the lpGBT coupled with a VTRx, provided by CERN, converts the electrical link from the MDC into an optical data link. To assess the readout efficiency of the MDC, a test pulse sequence was executed, injecting test pulses into all channels of both ToASt chips. This resulted in occupancy of 128 hits per frame at a test pulse rate of 39.1 kTestPulses/s. The sequence corresponds to an input data rate of ≅ 160 Mb/s per detector module, significantly exceeding the expected data rate of ≅ 70 Mb/s per detector module under realistic high-occupancy conditions.

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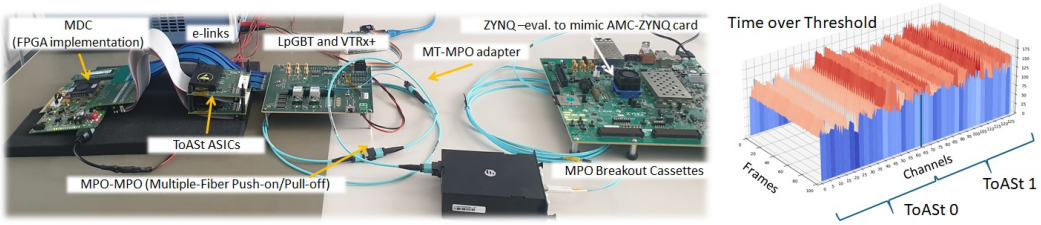

Figure 4. The MDC test setup is shown on the left, and the Time-over-Threshold (ToT) measurements are presented on the right, illustrating the simultaneous injection of test pulses into all channels of both ToASt chips. Each channel receives 100 test pulses. The observed variation in ToT across the channels results from the lack of calibration.

During each test pulse sequence, detailed metrics were collected, including the count of hit channels as well as precise Time-of-Arrival (ToA) and Time-over-Threshold (ToT) data, which are critical for assessing detector performance. Across all tests, the MDC consistently collected accurate ToA and ToT information without any observed loss in efficiency or measurement errors. This stability in data integrity and performance confirms the robust functionality of the MDC's logic architecture and its readiness for reliable operation within the readout chain.

4 Conclusion

Future hadron physics experiments impose very challenging requirements for both the front-end and the back-end electronics. In this context, the entire readout chain for the PANDA microstrip detector has been developed and its efficiency characterized. This system relies on a digital integrated circuit, the Module Data Concentrator (MDC), which acts as a local data controller and concentrator directly located on the detector module. The MDC has been implemented in UMC 110 nm CMOS technology and will be submitted in February 2025. To validate the MDC logic and the integration with the front-end chips, a dedicated test setup has been implemented to mimic the real readout chain of the microstrip detector. The preliminary test results confirm the robust functionality of the MDC's logic and its readiness for the ASIC submission.

Acknowledgments

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