Resistive Switching Devices Based on Solution Processable Metal Oxides

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- **H. Hu**, A. Scholz, Y. Liu, Y. Tang, G. C. Marques, and J. Aghassi-Hagmann, "A fully inkjet-printed unipolar metal oxide memristor for nonvolatile memory in printed electronics", *IEEE Transactions on Electron Devices*, vol. 70, no. 6, pp. 3051-3056, 2023.
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- **H. Hu**, A. Scholz, S. A. Singaraju, Y. Tang, G. C. Marques, and J. Aghassi-Hagmann, "Inkjet-printed bipolar resistive switching device based on ag/zno/au structure", *Applied Physics Letters*, vol. 119, no. 11, pp. 112103, 2021.
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Characteristics of Inkjet-Printed Electrolytegated Thin-Film Transistors", *IEEE Electron Device Letters*, vol. 42, no. 6, pp. 843-846, 2021.

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- Y. He, Y. Ting, **H. Hu**, T. Diemant, Y. Dai, J. Lin, G. C. Marques, H. Hahn, Y. Ma, T. Brzezinski, P. M. Kowalski, J. Aghassi-Hagmann, B. Breitung, "Emerging Sodium ion-modulated Non-Volatile Printed Memory based on Multicomponent Prussian Blue Material", 2024.

Conference Contributions

Oral Presentation

- **2023 Material Research Society (MRS) Spring meeting, San Francisco, California, USA**
  "2D/3D Printed Metal Oxide Transistor"
- **2022 Materials Systems Engineering (MSE) Day, Karlsruhe, Germany**
  "Printed Electronic Devices and Circuits"

Poster

- **2023 Material Research Society (MRS) Spring meeting, San Francisco, California, USA**
  "Printed Memristors for Memory, Computing and Hardware Security"
- **2022 3D Matters Made to Orders Conference, Schöntal Monastery, Germany**
  "Inkjet-printed Resistive Switching Devices Based on Metal Oxides"

Kurzfassung

Die gedruckte Elektronik ist eine aufstrebende Technologie, die im Vergleich zur klassischen CMOS (komplementären Metall-Oxid-Halbleiter) Technologie noch in den Kinderschuhen steckt. Sie bietet jedoch einzigartige Vorteile wie Transparenz, Dehnbarkeit, Skalierbarkeit in der Fläche, kostengünstige Herstellung und mechanische Flexibilität. Diese Eigenschaften erweitern das Anwendungsspektrum der Elektronik auf großflächige, leichte, flexible, nachhaltige und allgegenwärtige Szenarien. Allerdings bleiben die Komplexität, Integrationsdichte und Intelligenz der modernsten gedruckten Elektronik nach wie vor rudimentär, was ihre Fähigkeit zur Durchführung komplexer Aufgaben einschränkt. Dieses Phänomen ist hauptsächlich auf den Mangel an gedruckten Speicher- und Rechenkomponenten zurückzuführen. Das bloße Nachbilden konventioneller CMOS-Speicher- und Rechensysteme mit zeitgenössischer gedruckten elektronischen Bauelemente hat sich als unpraktikabel erwiesen, da die Leistung der gedruckten Transistoren moderat ist und die Drucktechniken und ihre Auflösung bei der Realisierung von großflächigen integrierten Schaltungen begrenzt sind. In diesem Zusammenhang dienen neuartige Arten von elektronischen Bauelemente zusammen mit ihren zugehörigen Speicher- und Rechenparadigmen als entscheidende Ermöglicher für ein intelligentes, vollständig gedrucktes elektronisches System. Gleichzeitig müssen diese neuartigen Bauelemente die technischen Beschränkungen der gedruckten Elektronik berücksichtigen.
Memristoren, auch als resistive Schaltbauelemente bezeichnet, sind eine Klasse neuartiger zweipoliger elektronischer Bauelemente, deren interner Widerstand von der Historie der angelegten Spannung und des Stroms abhängt. Die veränderten internen Widerstandszustände können für eine bestimmte Zeit ohne Energieversorgung aufrechterhalten werden und sind daher als Widerstände mit

Gedächtniseffekten angesehen. Die resistiven Schalteigenschaften von Memristoren bieten enormes Potenzial für die Implementierung speicherbasierter Anwendungen, einschließlich, aber nicht beschränkt auf nichtflüchtigen Speicher, neuromorphes Rechnen und Hardwaresicherheit.

Bis heute sind die Fortschritte in der Memristor-Forschung hauptsächlich auf vakuumverarbeitete Metalloxide zurückzuführen. Memristoren, die aus flüssigprozessierbaren Metalloxiden hergestellt werden, gewinnen aufgrund ihres kostengünstigen Herstellungsprozesses und ihrer Leistung, die mit der ihrer vakuumbasierten Gegenstücke vergleichbar ist, zunehmend an Interesse. Die Forschung zur Anpassung der flüssigprozessierbaren Metalloxide für gedruckte Memristoren, die Untersuchung der zugrunde liegenden Schaltmechanismen und der Schlüsselparameter für die entsprechenden Schaltungsarchitekturen sind jedoch noch kaum erforscht. Unter diesen Umständen zielt diese Arbeit darauf ab, resistive Schaltbauelemente zu entwickeln und charakterisieren, die mit flüssigprozessierbaren Metalloxiden gedruckt werden, und ihre Schlüsseleigenschaften für vielfältige Anwendungen in der gedruckten Elektronik zu bewerten, einschließlich nichtflüchtiger Speicher, neuromorphes Rechnen und Hardwaresicherheit.

Für die nichtflüchtige Datenspeicherung wurden Metalloxid-basierte Memristoren durch Tintenstrahldruck entwickelt. Das digitale resistive Schaltverhalten der gedruckten Memristoren wurde vollständig elektrisch charakterisiert und zeigte hervorragende Eigenschaften, die für nichtflüchtige Speicher eingesetzt werden können, einschließlich niedriger Betriebsspannung ($< 1\,\mathrm{V}$), gute Haltbarkeit (über $10^4\,\mathrm{s}$), großem Speicherfenster ($R_{\mathrm{off}}/R_{\mathrm{on}}$-Verhältnis über 10^7) und hohe Betriebszyklen (12672).

Um das Potenzial für neuromorphes Rechnen zu erforschen, wurden die flüchtigen und analogen resistiven Schalteigenschaften der mit Tintenstrahldruck gedruckten Memristoren untersucht. Die gedruckten Memristoren wurden als künstliche Synapsen eingesetzt und imitierten mehrere synaptische Funktionen. Diese umfassen die Paired-Pulse Facilitation (PPF), frequenzabhängige Integration und Filterung von Eingangssignalen, mehrere Formen der Kurzzeitplastizität einschließlich Fazilitation (10-177 ms), Augmentation ($10\,\mathrm{s}$) und Potenzierung

(35 s). Außerdem wurde eine höhere Ordnung der Kurzzeitplastizität, d.h. Metaplastizität, ebenfalls mit dem gedruckten Memristor emuliert.
Eine andere digitale Drucktechnik, der direkte Laserdruck mit noch kleineren möglichen Merkmalgrößen (bis zu $500\,\mathrm{nm}$ anstatt $10\,\mu\mathrm{m}$ wie beim Tintenstrahldruck) sowie einem überlegenen Konzept für metallische Verbindungen, wurde zur Herstellung von Dioden, Memristoren und integrierten Arrays von Memristoren verwendet. Der Laserdruck basiert auf Mehrphotonenabsorption in den Tinten und wurde in dieser Arbeit erstmals als überlegenes additives Fertigungsverfahren für Mikroelektronik nachgewiesen. Ein metalloxidbasierter Memristor mit der kleinsten Gerätefläche von $0.43\,\mu\mathrm{m}^2$ unter allen gemeldeten gedruckten Memristoren wurde durch Laserdruck erreicht. Zudem wurde ein memristives Kreuzschienen-Schaltung bestehend aus 6×6 Memristoren vollständig lasergedruckt. Diese Schaltung wurde später verwendet, um die physikalisch unklonbarer Funktionen (PUFs) zu implementieren, die ein hardwarebasiertes Sicherheitsprimitive ist. Der lasergedruckte memristive PUF erzeugte 36 binäre Zufallszahlen, die über 300 Iterationen ausgezeichnete Stabilität zeigten und keinen Bitfehler aufwiesen (Bitfehler = 0%).

Abstract

Printed electronics is an emerging technology still in its infancy when compared to classical CMOS (complementary metal-oxide semiconductors) technology. However, it offers unique advantages such as transparency, stretchability, scalability in area, low-cost manufacturing, and mechanical flexibility. These features broaden the application spectrum of electronics to large-area, lightweight, flexible-shape, sustainable, and ubiquitous scenarios. However, the complexity, integration density, and intelligence of state-of-the-art printed electronics still remain rudimentary, limiting their capacity for performing complex tasks. This phenomenon is mainly attributed to the scarcity of printed information storage and computing components. Simply replicating conventional CMOS memory and computing systems by employing contemporary printed electronics has been proven impracticable due to the moderate performance of the printed transistors and the constraint of printing techniques and their resolution in the realization of large-scale integrated circuits. In this context, novel types of electronic devices, along with their associated memory and computing paradigms, serve as pivotal enablers for an intelligent, fully-printed electronic system. At the same time, these novel devices must accommodate the technical constraints of printed electronics. Memristors, also referred to as resistive switching devices, are a class of novel two-terminal electronic components, of which the internal resistance depends on the history of the applied voltage and current. The changed internal resistive states can be maintained for a particular time without an energy supply and, thus, are regarded as resistors with memory effects. The resistive switching characteristics of memristors hold enormous potential to be exploited in implementing memory-based applications, including but not limited to non-volatile memory, neuromorphic computing, and hardware security.

To date, the remarkable advancements in memristor research are mainly attributed to vacuum-processed metal oxides. Memristors derived from solution-processed metal oxides are gaining more and more interest recently owing to their cost-effective fabrication process and performance that is on par with their vacuum-based counterparts. However, research on tailoring the solution-processed metal oxide for printed memristors, the investigation of the underlying switching mechanisms, and the key performance parameters for working in corresponding circuit architectures are still scarcely explored. Under this circumstance, this thesis aims to develop and characterize resistive switching devices printed with solution-processable metal oxides and to assess their key performance metrics for manifold applications in printed electronics, including non-volatile memory, neuromorphic computing, and hardware security.

For non-volatile data storage, metal-oxide-based memristors were developed by inkjet printing. The digital resistive switching behavior of printed memristors was fully electrically evaluated, exhibiting excellent figures of merit for non-volatile memory, including low-operation voltage ($< 1\,\mathrm{V}$), good retention performance (over $10^4\,\mathrm{s}$), large memory window ($R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio over 10^7), and the highest endurance cycles amongst reported printed memristor (12672).

To explore the potential for neuromorphic computing, the inkjet-printed memristors' volatile and analog resistive switching properties were investigated. The printed memristors were deployed as artificial synapses, remarkably mimicking multiple synaptic functions. These involve paired-pulse facilitation (PPF), frequency-dependent input signal integration and filtering, multiple forms of short-plasticity including facilitation (10-177 ms), augmentation ($10\,\mathrm{s}$), and potentiation ($35\,\mathrm{s}$). Besides, a higher order of short-term plasticity, i.e., metaplasticity, was also emulated with the printed memristor.

Another digital printing technique, direct laser printing with even lower possible feature sizes (down to $500\,\mathrm{nm}$ instead of $10\,\mu\mathrm{m}$ as in the case of inkjet printing) as well as with a superior concept for metallic interconnects was used to fabricate diodes, memristors and integrated arrays of memristors. Laser printing is based on multi-photon absorption in the inks and was proven as a superior additive manufacturing method for microelectronics for the first time in this thesis. A metal-oxide-based memristor with the smallest device area of $0.43\,\mu\mathrm{m}^2$ among

all reported printed memristors was achieved with laser printing. Moreover, a memristive crossbar circuit consisting of 6×6 memristors was fully laser-printed. This circuit was later used to implement the physical unclonable function (PUF), which is a hardware-based security primitive. The laser-printed memristive PUF generated 36 binary random numbers, which possess excellent stability over 300 iterations, showing no bit error (bit error = 0%).

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Contents

1 Introduction

1.1 Overview of Printed Electronics

Printing, an ancient technology, transfers patterns such as text or graphics from ink onto a carrier like paper or cloth. Electronics is a discipline where components that can manipulate electrons or other electrically charged particles are designed or fabricated. Printed electronics (PE) denotes the emerging technology that revolutionizes the fabrication of electronic devices and circuits with printing techniques in an additive, low-cost, and large-scale manner [1].

Nowadays, complementary metal oxide semiconductor (CMOS), as well as Si-based technology, has fostered the development of modern electronic engineering, which is fundamental to the boom in information technology. CMOS-based electronics are regarded as a technology of high performance, reliability, and high integration density. Printed electronics have never been targeted to replace conventional Si-based technology since its advent due to the inherent limitation of this technology. Compared to Si-based electronics, PE has a larger feature size (above micrometers), low performance, and low reliability. However, the research on PE has been booming in the past decades [2, 3, 4] because it is regarded as a complementary technology to CMOS and enables emerging applications where CMOS has limitations, such as disposable electronics, flexible electronics, and large-area applications [4, 5].

The fabrication of PE is an additive manufacturing process where devices are fabricated using a bottom-up drop-on-demand approach. The general process of printing an electronic component is to deposit inks such that the patterns of different functional material types (e.g., conductors, isolators, or semiconductors) are formed at the expected location on the substrate, followed by the formation of a

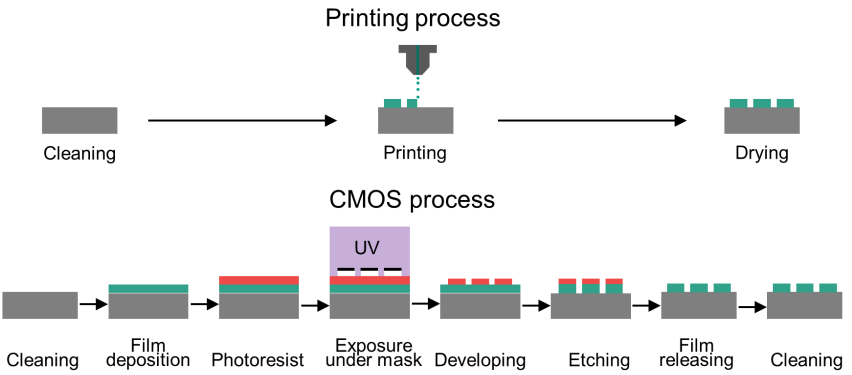


Figure 1.1: Schematics of comparison between printed electronics and conventional CMOS process.

thin film after an annealing step. This has significantly shortened the manufacturing process compared to conventional CMOS, which generally requires material deposition in vacuum, photolithography, and etching. Modern chip manufacturing requires over 300 sequenced processing steps [1, 6]. Figure 1.1 compares the fabrication processes of PE with conventional CMOS technology. Moreover, CMOS manufacturing is a subtractive process in which materials are deposited entirely on the substrate, creating areas where the material is unnecessarily deposited and needs to be removed in a subsequent etching step. This results in a tremendous amount of material waste. On the contrary, in PE, the materials are deposited on demand onto the substrate, significantly reducing the waste [1, 6].
In addition, although CMOS is advanced in achieving ultra-large-scale integrated circuits, the substrate is restricted to the rigid Si wafer of a limited size. On the contrary, PE is independent of the properties of the substrate, regardless of physical size or mechanical properties. The substrate can be as large as meters of rigid or flexible and stretchable materials, spanning from glass, over plastic, to even papers [1, 2, 6, 8]. Thanks to the aforementioned advantages, including cost-effective fabrication and independence of substrate property, PE emerges in future applications where cost and flexibility are more important than performance. These promising application scenarios include large-scale displays, large-scale sensing

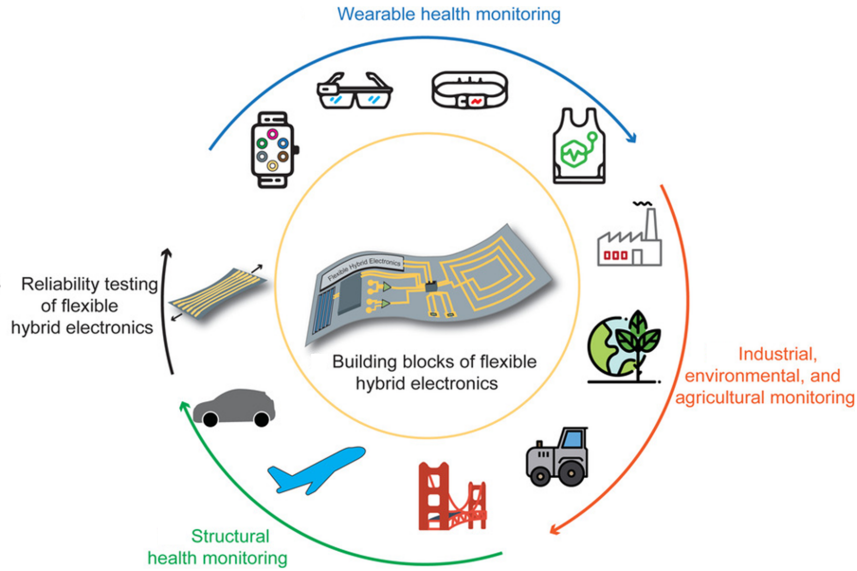


Figure 1.2: Spectrum of application with PE. Flexible hybrid electronics as an example to show possible application scenarios spanning from wearable health monitoring over industrial, environmental, and agricultural monitoring to structural health monitoring. © 2019 WILEY-VCH Verlag GmbH & CO. KGaA, Weinheim. Reproduced with permission from [7].

for monitoring (e.g., monitoring in transport tools and infrastructure, or industrial-, environmental-, and agricultural-related scenes), smart packaging in logistics, the Internet of Things (IoT), and wearable electronics for health monitoring, to name a few [4, 7, 9]. Figure 1.2 shows part of PE's promising applications.

1.2 Motivation

As introduced earlier, PE will play a complementary role to CMOS and will show advantages in specific application scenarios, including but not limited to wearable electronics, IoT, smart packages, large-scale displays and sensing, and so on. However, the main achievements in PE are still limited to discrete electronic

components, including field-effect transistor (FET) [10], various sensors [9], solar cells [11], diodes [12], light-emitting diodes (LED) [13], capacitors [14], and antennas [15]. Simple circuit based on printed transistors are also reported [3], such as inverters [16], ring oscillators [17], logic gates [18], decoders [19], latches [20], and so on. In a complex printed electronics system where data processing is required, a thinned Si-based microcontroller is needed for information storage and processing [5, 7], as illustrated in Figure 1.3. This hybrid system leverages the high performance of Si-based ICs while at the same time exploiting the low cost, conformability, and scalability of printed components [5, 7]. The incorporation of Si-based ICs largely enhances the intelligence of printed electronics systems, albeit the thinned Si microcontroller largely elevates the cost, which significantly weakens the advantage of printed electronics in low-cost manufacturing. Printed microcontrollers are highly sought after in this context, but their research confronts remarkable challenges [5, 21]. Two major challenges are the lack of appropriate printed information storage and computing components.

In the case of information storage, the performance parameters and manufacturing complexity of the existing memory technologies may not align with PE. For instance, transistor-based static random access memory (SRAM) and dynamic random access memory (DRAM) are two mainstream memory technologies in conventional Si-based ICs, but they are volatile memories requiring a consistent power supply to maintain the stored data [22], which imposes high requirements on the power-supply system and concurrently increases the complexity of related circuits. This presents considerable technical challenges in realizing complex circuits in printed electronics. Although printed transistor-derivative memory devices, including Flash memory and ferroelectric FETs (FeFETs), are non-volatile, but high operation voltage (over tens of volts) [23, 24, 25, 26] makes powering the memory through batteries not feasible. Other novel non-volatile memory technologies, such as magnetic random access memory (MRAM) and phase change memory (PCM) [22], have stringent material property requirements and thus present a challenge to be printed. In this context, a novel memory device that accommodates the constraints of printed electronics is highly demanded.

In the case of computing, the realization of the conventional von Neumann computing architecture with printed electronics presents significant challenges. First,

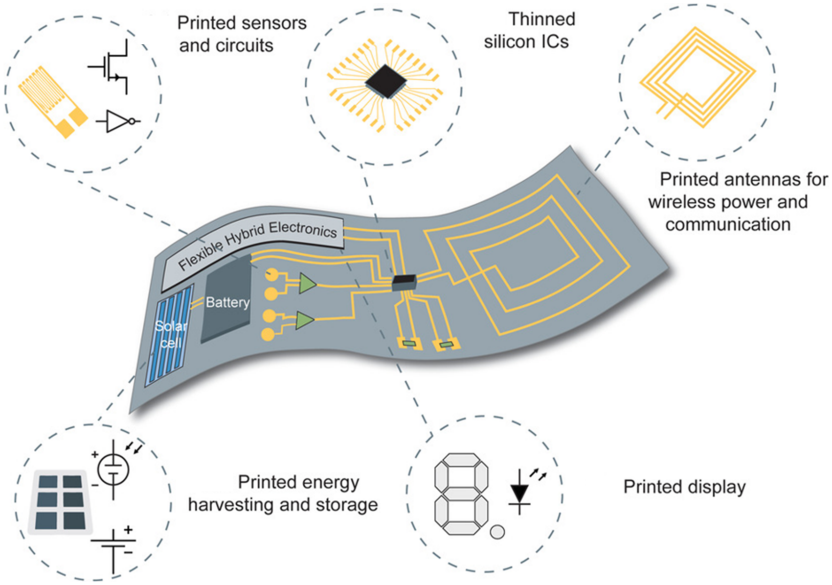


Figure 1.3: Schematics of a flexible embedded PE system. Display, antennas, sensors, and energy supply units (such as energy harvesting devices and batteries) are printed, while the information processing and storage units still rely on thinned silicon ICs. © 2019 WILEY-VCH Verlag GmbH & CO. KGaA, Weinheim. Reproduced with permission from [7].

the features of von Neumann architecture [27], including separation between computation and memory, binary data-based programming and communication, and clock-driven timing, require a large number of building blocks and sophisticated peripheral circuits. This imposes enormous challenges to current printing technologies due to low resolution and high variability in fabrication. Second, printed transistors, as the cornerstone of implementing computation, are still confronting low yield rates and high variability, which hinder the development of complex circuits from the technical perspective [10]. In addition, state-of-the-art printed transistors are still demanding significant improvements. The trade-off between high threshold voltage (up to tens of volts) and low switching speed (down to several hertz) is always met due to the lack of gating materials that confine well with the channel [10]. The moderate performance of the printed transistors

will exacerbate the inherent bottleneck of the von Neumann computing architecture, which eventually renders the printed computing units inadequate to perform signal processing tasks within the scope of printed electronics applications. Alternatively, neuromorphic computing, a new computing paradigm inspired by the human brain, aims to process data directly in the memory in a rather parallel manner [27]. Moreover, this event-driven computing paradigm performs computation only when data is available [27]. These features of neuromorphic computing will largely simplify the circuitry, thus mitigating the technical limitations of current PE. As shown in recent research, neuromorphic computing is an energy-efficient computing paradigm that is superior in dealing with specific tasks such as classification of unordered data, parallel signal processing, and self-learning [28, 29, 30]. Therefore, neuromorphic computing emerges as a promising enabler for intelligent printed electronics systems as the computing solution [31, 32, 33]. Implementing neuromorphic computing relies on memory devices, necessitating the advancement of novel memory devices tailored for printed electronics.

Memristors, also referred to as resistive switching devices, are novel two-terminal electronic devices, of which the internal resistance depends on the history of applied voltage and current [34, 35]. The changed internal resistive states can be maintained for a particular time without an energy supply and thus are regarded as resistors with memory effects. Compared to other memory devices, memristors show unparalleled advantages, such as: (a) Simple device structure, which promises to reduce fabrication complexity. (b) High device performance, including low operation voltage (down to hundreds mV), fast switching speed (down to ps), excellent retention and endurance properties. (c) Good mechanical flexibility. All these advantages render this class of two-terminal electronic devices promising in advancing the development of fully printed electronic systems. The current advancements in memristor research are mainly attributed to vacuum-processed metal oxides [36, 37, 38, 39, 40]. Memristors derived from solution-processed metal oxides [41, 42] are incrementally garnering interest, owing to cost-effective fabrication process and performance that is on par with their vacuum-based counterparts. However, the research on tailoring solution-processed metal oxide to be printable and investigating the performance of printed memristors is still in its infancy.

The primary objective of this thesis is to develop printed memristors derived from solution-processable metal oxides and systematically characterize and evaluate their performance to be used for non-volatile memory and neuromorphic computing within the domain of printed electronics. In addition to inkjet printing, one of the predominant printing techniques utilized in printed electronics, multi-material laser printing based on multi-photon absorption, will be exploited to fabricate sub-micrometer printed memristors for the first time. The successful implementation of hardware security with a laser-printed memristive crossbar circuit provides a proof-of-concept of employing printed memristors based on solution-processed metal oxides in circuit-level applications.

1.3 Structure of the Thesis

The remaining parts of this thesis are structured as follows:

- Chapter 2 introduces the fundamental concepts of current memory technologies, including resistive switching devices. Next, the basic concepts and working mechanisms of resistive switching devices corresponding to the device categories are systematically introduced. At the end of this chapter, the basic concepts of two printing technologies used in this thesis, inkjet printing and laser printing, are discussed.
- Chapter 3 describes the fabrication process of printed memristors, including inkjet printing and laser printing. The ink formulation and annealing steps are described in more detail. Moreover, the setup and test protocol for the electrical measurements are shown.
- Chapter 4 presents the results of inkjet-printed memristors for non-volatile memory. First, a brief review of current research progress on printed non-volatile memory is given. Next, three types of inkjet-printed memristors based on solution-processable metal oxide, i.e., Ag/ZnO/Au, Ag/ZnO/Ag, and Au/WO_{3-x}/Au are presented, including the properties of the materials, the resistive switching characteristics, the variability analysis in terms of

device-to-device and cycle-to-cycle, as well as the critical device performance metrics for non-volatile memory. Finally, the underlying mechanisms of resistive switching are discussed.

- Chapter 5 presents the results of exploiting the analog resistive switching characteristics of inkjet-printed Au/WO_{3-X}/Au in neuromorphic computing. First, a brief introduction to neuromorphic computing in printed electronics is given. The basic concepts in the field of neuromorphic computing are discussed. Next, volatile and analog resistive switching characteristics and underlying mechanisms are presented. Finally, the results of emulating synaptic behavior with printed Ag/WO_{3-x}/Au memristor are shown.
- Chapter 6 exploits the results of laser-printed Ag/ZnO/Pt memristors for the hardware security application. First, a brief introduction to hardware security based on memristors is given. Next, the device properties of laser-printed memristors are presented. Finally, the implementation of a physical unclonable function (PUF) with a fully laser-printed memristive crossbar is demonstrated.
- Chapter 7 summarizes the thesis and gives an outlook on future research topics.

2 Background

2.1 Technological Evolution of Information Storage Medium

The information contains knowledge or data that can be processed, stored, or transmitted [43]. The representation of information relies on its retrieval and storage in a reliable medium. For instance, biological information is encoded in DNA, knowledge is written in books, an event can be recorded on a magnetic tape, and so forth. In regards to representing information, the storage mediums in human society evolved from paintings and carvings to scribing and digitization [44], as shown in Figure 2.1(a). Digitalization is the most significant revolution in the development of storage technology and enables the storage of sounds, images, and words in a binary form. Thereafter, human society entered the information age, and the generated data expanded drastically within the last decade. According to a forecast from the International Data Corporation (IDC) [45], the global generated data volume will leap to 181 zettabytes (1 zettabyte = 10^{21} bytes) in 2025 (Figure 2.1(b)). To store such a huge amount of data, modern memory technologies are employed. In general, memory technologies are categorized into three groups according to the underlying mechanism, e.g., magnetic memories (such as magnetic tapes and hard discs), optical memories (such as CD, DVD, and Blu-ray), as well as electronic memories (such as SRAM, DRAM, EPROM, EEPROM, Flash, etc.). However, the focus of this thesis will be on electronic memories.

In recent years [22, 46], memory devices have attracted huge attention from both industry and academia for computing purposes. The popularity stems from the

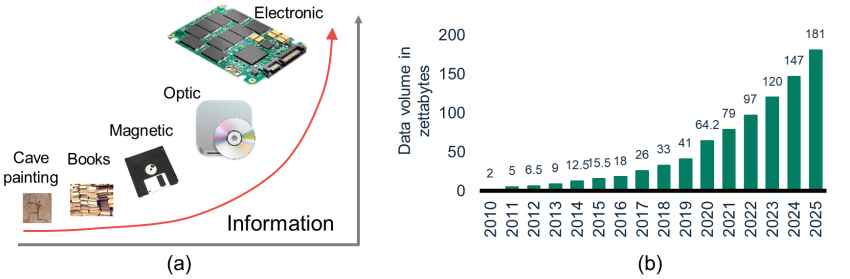


Figure 2.1: **(a)** Historical evolution of information storage medium. **(b)** Growth of the data volume generated in human society. Source: IDC, & Statistica.

bottleneck inherited from the conventional von Neumann Computing paradigm, mainly due to the memory wall [22, 47, 48]. Advanced central processing units (CPUs) operate within the GHz regime. However, the performance of the current computing system is severely limited by data transport between the memory unit and the CPU [4]. Under these circumstances, researchers seek new paradigms that allow faster and more energy-efficient computing. Two mainstream strategies are executing computation in memory (In-memory computing) and mimicking the brain (neuromorphic computing). These two new computing paradigms rely strongly on memory technologies and foster research in electronic memory devices.

Conventional electronic memory devices store information through the presence or absence of charges, as in DRAM, SRAM, and Flash memory [49]. Charge-based memories are mature technologies that dominate the memory unit in various applications. In addition, there is an emerging class of memory devices that store information through different resistance states, thus termed resistive memory. Resistive memories are mainly classified into two groups following the working mechanisms. The first type changes its resistance by altering the atomic arrangement within the active layer, while the second type relies on the change of the electron transport properties [22]. The working mechanism of the resistive memories will be systematically introduced in Section 2.4. In the following, a general introduction to charge-based memory technologies will be given.

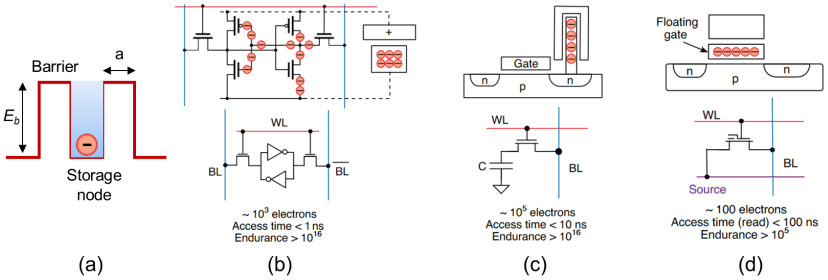


Figure 2.2: Basic concept and schematics of charge-based memory technologies. **(a)** Schematic of an electron that is trapped in a storage node, which is defined by the height and width of the energy barrier. **(b)** A SRAM cell consists of 6 CMOS transistors, which are configured as a pair of back-to-back inverters. The stored charge is confined between the FET channels and gate insulators. **(c)** A DRAM cell in a structure of 1-transistor-1-capacitor. The stored charge is blocked between the channels of the transistor and the dielectric layer of the capacitor. **(d)** A Flash memory cell incorporates a floating gate in a FET as the storage node, where the charge is stored. **(b)**, **(c)**, and **(d)** with © 2020 Springer Nature Limited. Reproduced with permission from [7].

2.2 Charge-based Memory

Charge-based memory technologies represent state-of-the-art memory in modern information and communication technologies. The essential idea of storing information in charge-based memory devices is to maintain the electrons within the storage node. In other words, the presence or absence of electrons in the storage node represents the states 0 and 1, respectively. In a storage node, energy barriers are exploited to preserve electrons, as demonstrated in Figure 2.2(a). The barrier height (E_b) and width (a) determine the retention time of memory cells [49]. Three different electronic devices are used to maintain electrons in charge-based memory cells. According to storage mechanisms, they are categorized into SRAM, DRAM, and Flash memory.

The common configuration of an SRAM cell consists of 6 transistors (Figure 2.2(b)), of which two transistors serve as selectors and two pairs of CMOS inverters are connected back to back. The output potential of one inverter is connected to the input of the other. Therefore, a feedback loop is formed to freeze the cell in a logic state [22, 49]. In this configuration, electrons are viewed

as being confined within the barriers formed by the field-effect transistor (FET) channel and gate insulator. The SRAM cell is known to be the fastest charge-based memory device with access times lower than $1\,\mathrm{ns}$. Due to the low barrier height between the channel and the gate insulator of FET ($0.5\,\mathrm{eV}$), electrons can tunnel through the barrier; thus, the SRAM cell needs to be always connected to the power supply to replenish the electrons constantly within the storage node [22]. A DRAM cell consists of a capacitor (storage node) and a FET (selector) in series (Figure 2.2(c)). The electrons are maintained between the capacitor and the FET. The barrier height at the FET side is lower and depends on the band-gap of the channel material (ca. $1.1\,\mathrm{eV}$ in silicon), which determines the retention time of a DRAM cell and is typically in the ms range [49]. It is worth mentioning that the DRAM cells require periodic refresh operations. A Flash memory cell is a special FET type that involves a floating gate sandwiched between the gate insulator (Figure 2.2(d)). During the write operation, the electrons from the channel are injected into the floating gate by tunneling. The floating gate serves as the storage node where the electrons are trapped by the high energy barrier of the gate insulator. The Flash memory cell is non-volatile since the barrier height (ca. $3.1\,\mathrm{eV}$) of the storage node is sufficient to guarantee long-term retention (ca. 10 years) [49]. Due to the barrier height, the access time of the Flash memory cell is about hundreds of $\mu\mathrm{s}$, which is the longest among the charge-based memory technologies [49].

2.3 Fundamentals of Memristors

2.3.1 Evolution of Memristive Devices

In 2008 [50], the Williams group at Hewlett-Packard Labs announced that “The missing memristor found”. The term “memristor” was first proposed by Leon Chua in 1971 [51] that there should be a fourth fundamental element in addition to the three fundamental passive circuit elements, e.g., the resistor, the capacitor, and the inductor. Chua postulated the existence of the fourth fundamental element based on a discussion of symmetrical mathematical relations connecting pairs of

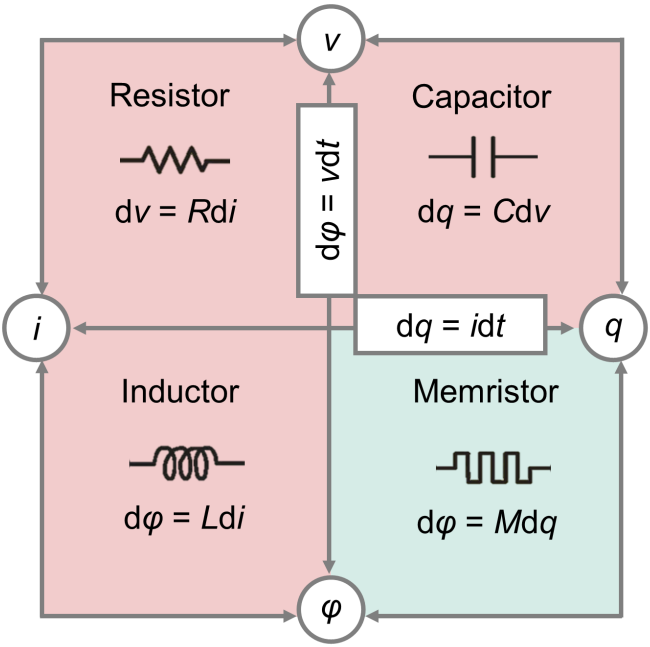


Figure 2.3: Theoretical prediction of the existence of memristor based on a discussion of symmetrical mathematical relations, each of which links a pair of the four fundamental circuit variables. Four fundamental circuit variables are: current i, voltage v, charge q, and magnetic flux φ. Existed and predicted passive fundamental circuits elements and related characteristic properties: resistor and resistance (R), capacitor and capacitance (C), inductor and inductance (L), and memristor and memristance (M).

the four fundamental circuit variables: electric current i, voltage v, charge q, and magnetic flux φ (Figure 2.3). Taking two of these variables randomly to build up a mathematical relation, there should be six different combinations. It is known: (a) charge and flux are time integral respectively of current and voltage (horizontal and vertical formula in Figure 2.3), and (b) three passive electrical elements related physical quantities can link two variables (I, II, and III quadrants in Figure 2.3). One mathematical relation is still missing at the bottom right corner, which can link the magnetic flux (φ) and the charge (q). Therefore, Chua supposed that,

theoretically, there is a missing element that can functionally link charge and flux. He named this missing element memristor (a contraction of memory resistor), and its characteristic property memristance "M" is derived from the differential equation:

$$M = \frac{\mathrm{d}\varphi}{\mathrm{d}q}. \tag{2.1}$$

If M is a constant, the memristor behaves more like a resistor. But if M itself is a function of q, this equation will indicate nonlinear characteristics of the memristor and thus is more interesting. In 1976 [52], Chua and Kang generalized the concept of the memristor to a much broader class of nonlinear dynamical systems that is referred to as the memristive system. According to the broader definition, a memristive system can be defined as current- or voltage-controlled. The current-controlled memristive system is represented by a differential form (the voltage-controlled form is in a bracket for comparison):

$$v = R(w, i)i \qquad [i = G(w, v)v)] \tag{2.2}$$

$$\frac{\mathrm{d}w}{\mathrm{d}t} = f(w, i) \qquad [\frac{\mathrm{d}w}{\mathrm{d}t} = f(w, v)], \tag{2.3}$$

in which v and i are the voltage and the current, w is a set of state variables. f, R, and G are in general explicit functions of time. Equation 2.2 indicates the unique property of a memristive system differing from an arbitrary dynamical device: no current will flow through the system when the applied voltage is zero, regardless of the state w. The above memristive equation was proven to model the $i - v$ characteristics of some devices and systems, such as thermistors, Josephson junctions, and even the Hodgkin-Huxley model of the neuron in Chua's work [52]. Although the theory of memristor was established in the 70s, the first physical model and experimental demonstration of a "real" memristor were announced by Hewlett-Packard labs in 2008 [50]. They showed that the memristance arises naturally in a two-terminal nanoscale system consisting of a stack of Pt/TiO_2/Pt. Solid-state electronic and ionic transport in this system are coupled under an external bias voltage. Some researchers [53] disagree with the claim of "Found of memristor" since they hold the opinion that the devices reported in 2008 were

not new. The hypothesized memristor requires magnetism but has no material memory in Chua's conceptual proposition, while in Hewlett-Packard's work, the reported devices constitute analog memory that can work without magnetism. Although the existence of a "real" memristor is still controversial, the special resistive switching phenomenon with memory effect is promising in many applications, such as novel non-volatile memory, new paradigms of computing, encryption, and radio-frequency communication [35]. Terms like "resistive switching" and "memristive" are more accepted when referring to this class of devices in the literature.

When discussing resistive switching, these phenomena have been studied since the early 1960s in various solid-state materials. A representative case is the anomalous negative differential resistance observed in metal oxides of a metal-insulator-metal (MIM) structure. The insulator material "I" spans from binary and multinary oxides, chalcogenides, and to group-IV, III-V, and II-IV semiconductors[49]. Due to the lack of sufficient analytic tools to understand the microscopic mechanism of the resistive switching overserved in metal oxides at that time and the significant advantages of Si semiconductor-based memories (such as DRAM, SRAM, and Flash), the research momentum of resistive switching devices was quenched. In the new informative era, the explosive growth of the generated data and the high cost of increasing the density of classical charge-based memory appeal to the research on novel memory devices. Resistive switching devices, as one group of novel memory elements, have again gained attention from both industry and academia. Nowadays, the papers published per year in the field of memristive devices contribute to a significant part in solid-state physics and nanoelectronic engineering [38]. In the past two decades, all major semiconductor research institutes and manufacturers have launched large research and development projects on resistive switching devices and systems. Samsung successfully demonstrated a ReRAM chip using $180\,\mathrm{nm}$ in 2004, Sandisk and Toshiba released 32 GB ReRAM chips in 2013, and Micron and Sony presented 16 GB ReRAM chips in 2014, to name a few [38].

2.3.2 Basic Working Concepts of Memristive Devices

Memristive devices are one class of emerging memory technologies and hold promise for various applications spanning from information storage, computation, hardware security, and radio-frequency communication [35]. A set of terminologies is defined to facilitate communication within the field.
Memristor is the most well-known name representing this class of two-terminal electronic devices. Due to the aforementioned debate about the memristor definition among the researchers, *resistive switching* or *memristive elements, devices, memories, or cells* are more mitigating ways to refer to these devices. These terms are also preferred and will be intensively used in later discussions. Resistive switching devices are initiated to serve as random-access memory (RAM). Therefore, upon the application, they are also known as *resistive RAM (ReRAM or RRAM)*. It is worth noting here that ReRAM is also used to refer to *redox-based resistive switching random access memory* to emphasize the mechanisms in some literature [38, 54, 55].
In general, a memristive device consists of a *top electrode (TE)*, a *bottom electrode (BE)*, and an *active layer* sandwiched between TE and BE (Figure 2.4(a)). From the perspective of a circuit designer, a memristive device serves as a two-terminal "switch", which determines the quantity of the current flow through the two-terminal element with distinct resistance levels when subjected to an electric field. The most reported memristive devices work in a binary form. That is to say, the devices are switched between their *low resistive state (LRS)* and *high resistive state (HRS)*. LRS and HRS are called *On* and *Off* states, respectively, to associate with the tree terminal transistor. Researchers who target applications for information storage, encryption, radio-frequency communication, and logic operations prefer devices with binary resistive switching. Other groups of researchers endeavor to explore multiple *intermediate resistive states (IRS)* between LRS and HRS, which is referred to as *multilevel storage*. These types of devices are promising for increasing memory density by storing more than one bit within one cell. Moreover, the devices with multilevel are intensively studied for in-memory computing (IMC).

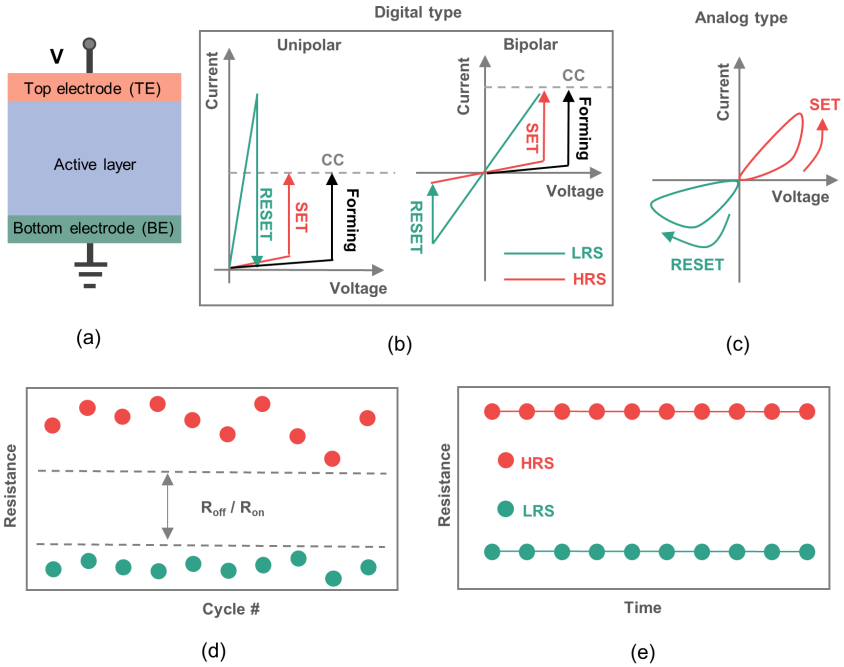


Figure 2.4: Basic concepts of memristive devices. **(a)** Schematics of a memristor in a cross-sectinal view. A common structure of memristors consists of a top electrode (TE), an active layer, and a bottom electrode (BE). TE is generally biased while the BE is grounded during the electrical measurements. **(b)** Schematic of typical $I - V$ characteristic curves of digital-type memristors: unipolar (left-hand side) and bipolar (right-hand side) resistive switching modes. **(c)** Schematic of typical $I - V$ characteristic curves of analog-type memristors. **(d)** and **(e)** Schematics of a typical results plot of endurance and retention.

Almost all of the reported memristive devices are in HRS as fabricated. The operation to initiate the first resistive switching, e.g., to bring the device from initial HRS to LRS, is called *Forming* process (Figure 2.4(b)). Accordingly, the voltage that is required to trigger Forming is termed as *Forming voltage*. The process to switch the device back to HRS is called *RESET* (also called *erase* when used as a memory device), while the reversed operation is termed as *SET* (also named *write* corresponding to RESET in information storage application). Although Forming and SET identically tend to bring devices from HRS to LRS, Forming generally requires a higher voltage than SET. Some researchers [56, 57, 58] claimed they developed a "*Forming-free*" device since the Forming cannot differentiate from the SET clearly. In the Forming and SET processes, the resistive switching from HRS to LRS results in a drastic increase in current, and a *compliance current (CC)* is commonly used to prevent the device from hard breakdown, as the gray dash lines shown in Figure 2.4(b). The operation to determine the resistance of the device after each SET and RESET is called *read*, which is achieved by applying a small voltage to the device. In reviews [36, 38, 59], it is suggested the read voltage should not exceed 1/10 of the SET voltage to avoid an unwanted resistance disturbance.

Depending on the polarity of the SET and RESET voltage, the memristive cells are classified into *bipolar* and *unipolar resistive switching devices*. Bipolar denotes that the SET and RESET operations are realized under opposite voltage polarities, while unipolar refers to the manner in which resistive switching always occurs under the same voltage polarity. In addition to the voltage polarity, memristive devices are categorized into two types. One is known as *digital type*, whose SET and RESET processes experience an abrupt change in current. The other one is termed as *analog type*, which, on the contrary, undergoes a gradual resistance change. The $I - V$ characteristics of bipolar, unipolar, digital, and analog-type memristive devices are represented by sketched curves in Figure 2.4(b) and (c).

A couple of parameters are commonly considered when evaluating the performance of a memristive cell. As a reversible electronic switch, the maximum number of resistance change cycles between two or multiple levels is of primary interest. This figure of merit is termed *endurance*, which is presented by plotting the value of LRS and HRS against the cycle numbers (Figure 2.4(d)). One needs

to consider the resistance ratio between HRS and LRS, $R_{\mathrm{Off}}/R_{\mathrm{On}}$, in the endurance plot. The endurance counts upon the $R_{\mathrm{Off}}/R_{\mathrm{On}}$ are still acceptable. One advantage of ReRAM over SRAM and DRAM is its non-volatility. Therefore, researchers will consider the time of each resistive state that can be maintained without a voltage supply. This critical parameter is called *retention* (Figure 2.4(e)). Other parameters need consideration, but it depends on the application scenarios. Endurance, retention, and $R_{\mathrm{Off}}/R_{\mathrm{On}}$ ratio are the essential figures of merit and thus will given especially attention throughout this thesis.

2.4 Categories of Working Mechanisms

Memristors, or memristive devices, are referred to as a family of electronic elements, of which resistive switching is the common characteristic. Nevertheless, the underlying physical mechanisms are manifold. From the natural perspective, resistive switching can be attributed to stoichiometric change induced by ions within the active layer, phase change of the active layer between high- and low-conductive states, magnetoresistive effects, electron trapping/de-trapping effect of the active layer, ferroelectric effect, and nano ionic redox phenomena [60, 61]. In an intuitional way, memristive devices are categorized into "filamentary" and "non-filamentary" types depending on whether the resistive switching occurs within a few localized conduction channels or uniformly across the entire area [60]. These two tags are widely used to indicate the resistive mechanisms. In the following, the abovementioned physical mechanisms will be introduced in detail under the filamentary and non-filamentary groups. Since the main work underlying the thesis involves filamentary and ion migration of non-filamentary types, they will be the focus of this section.

2.4.1 Filamentary

The filament type is the absolute dominating device category in the field of memristive devices. This type of memristive cell relies on the formation and

rupture of conductive channels within the active layer to realize resistive switching. Depending on the ion species that participate in the formation of the conductive filaments, this vast family of devices is further divided into three subgroups. The first subgroup is termed electrochemical mechanism (ECM), which relies on the cation-based redox reaction. The second subgroup is referred to as the valence change mechanism (VCM), which is based on the migration of anions in the active layer. A variation of ECM and VCM is called thermochemical mechanism (TCM), in which the filaments can be formed by cations or anions. The distinction between TCM and the other two types is the RESET process. For TCM, Joul heating induced by the high current flowing through the filaments plays a crucial role. In the following sections, the working mechanism of the microscopic aspects and the device characteristics of these three types of filamentary memristive devices will be elucidated and compared.

Electrochemical Metallization Mechanism (ECM)

As the term implies, electrochemical metallization (ECM) memristive devices rely on the electrochemical process of metal ions. In general, ECM is more frequently used in the literature when referring to the underlying mechanism of this class of devices. In fact, they were called programmable metallization cells (PMC) originally, which now refers to the technology platform that spans a variety of applications beyond memory. In the semiconductor industry, the term conductive bridging random access memory (CBRAM) was coined to refer to this memristive technology in a memory array [61].
ECM memristive cells are generally in a configuration of so-called “MIM”, which refers to a metal-ion conductor-metal system. One metal layer is called an active electrode (AE), made from electrochemically active metals such as Ag, Cu, and Ni. This class of metals tends to lose electrons when subjected to a positive bias and migrate within the ion conductor layer and the electrical field. In addition, Ag^{+} and Cu^{2+} are highly movable in solid electrolytes [62], which benefits the fast resistive switching process in ECM devices. On the contrary, the counter electrode in the MIM system consists of an electrochemically inert metal, such as

Table 2.1: List of typical reported ECM cells of different material stacks.

AE	Active layer	CE	$R_{\mathrm{off}}/R_{\mathrm{on}}$	Retention (s)	Endurance	Reference	Year
Cu	TiO_2	Pt	2×10^4	10^6	10^5	[63]	2018
Ag	ZnO	Pt	$> 10^2$	300	$> 10^3$	[64]	2018
Cu	GeSe	W	$> 10^2$	10^5	10^5	[65]	2010
Ag	$FAPbI_3$	Pt	10^5	3000	1200	[66]	2018
Ag	V_2C	W	10^4	2000	100	[67]	2021
Ag	PVP-PEDOT:PSS	Pt	10^4	10^5	1300	[68]	2020
Ag	h-BN	Pt	10^5	10^4	850	[69]	2023

Pt, Au, W, or metal nitride. These metal materials serve as the counter electrode (CE), where the metal cations stem from AE harvest electrons and then are reduced to their electrically neutral form. The middle layer between AE and CE works as a matrix supporting cation migration. The utilized material for this ion conductor layer covers a vast family of functional materials, including transition metal oxides, chalcogenides, perovskite, MXene, organic materials, 2D materials, and their related derivatives, and so forth. The typical materials for AE, CE, and ion conductors are summarized in Table 2.1, together with the reported ECM devices.

The underlying mechanism of resistive switching in ECM cells is attributed to the highly conductive metallic filaments formed within the active layer. The filaments can connect and disconnect the AE and CE reversibly, resulting in a switch from LRS to HRS and vice versa. The formation, rupture, and closing of the metal filament connection in the ECM cell involve a series of redox and electrical field-induced cation migrating processes. These physical and chemical processes account for the Forming, SET, and RESET operations over an ECM cell. Figure 2.5 is a schematic that elucidates the resistive switching processes of an ECM cell with respect to its redox and cation migration in a cross-sectional view. The sketched $I - V$ curves of ECM cells on a logarithmic scale capture the characteristics of each operation process.

In general, the CE is grounded (GND) while only the polarity of the voltage applied to the AE is changed between positive and negative (V+ and V-) during

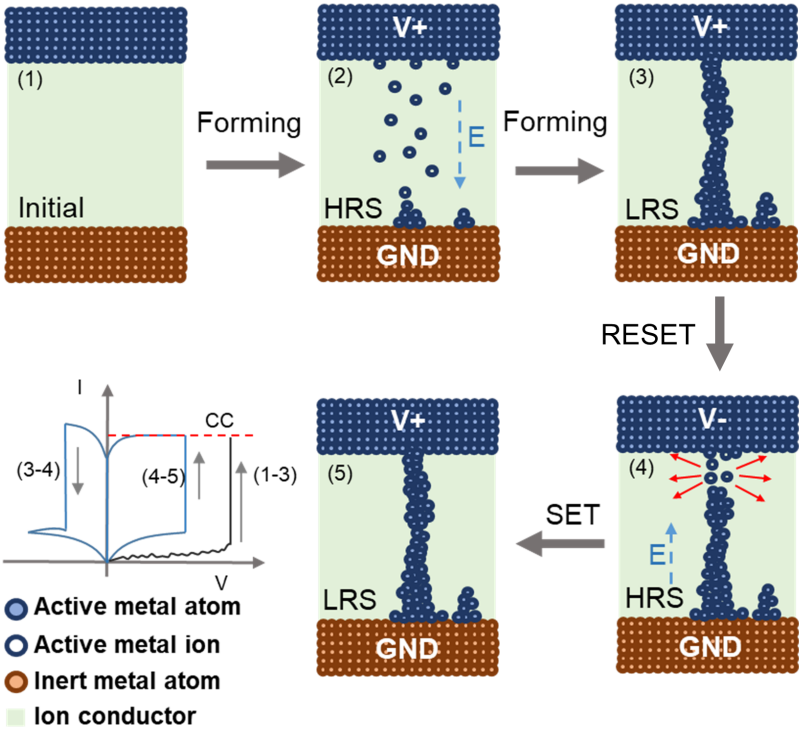


Figure 2.5: Mechanisms of ECM type memristors: A series of cross-sectional schematics illustrate the dynamic processes of the filament evolution behind Forming, SET, and RESET. The numbered processes relate to the sections involved in the typical $I - V$ curves on a semi-logarithmic scale.

the operations. For the Forming process (processes 1 to 3), the AE is positively biased, and a pair of redox reactions will be triggered respectively at the AE and CE. At the side of AE, the half-cell reaction occurs as follows:

$$\mathrm{Me} \rightarrow \mathrm{Me}^{z+} + ze^{-}. \tag{2.4}$$

The atoms Me of AE will lose z electrons (e^{-}) and be oxidized into cations Me^{z+}. The dissolved cations will migrate along the electrical field in the middle solid

electrolyte and harvest electrons as long as they arrive at the CE, where another half-cell reaction occurs:

$$\mathrm{Me}^{z+} + ze^{-} \rightarrow \mathrm{Me}. \tag{2.5}$$

These two half-cell reactions lead to the growth of active metal filaments from CE towards AE (processes 1 to 2 in Figure 2.5), and eventually, the filaments will bridge both electrodes (process 3 in Figure 2.5), resulting in a low resistive state of the ECM cell. This process is termed Forming, as introduced previously. Since the movement of the cations within the electrolyte layer is a stochastic process, the reduction and growth of the filament will happen simultaneously at several locations on the CE of an actual ECM cell. One of these filaments grows at the fastest speed and will "short" the cell first, and the growth of the other filaments will terminate. This winner filament will dominate the resistive switching phenomena later on. This is similar to the rule "winner takes all." For the RESET process, the AE is negatively biased. A high current flowing through the bridging filament generates local Joule heating. Firstly, the local heating will promote ion diffusion from the filament towards the surrounding ion conductor and lead to a rupture of the filaments at the thinnest location (near the AE). Secondly, as long as a gap induced by the rupture exists within the filament, the residual filaments connecting the CE serve as a cation supplier while the AE works as a cation receiver since the electrical field is opposite to the Forming process. Consequently, the active metal from the filaments will dissolve into the electrolyte and migrate towards the AE, switching the ECM cell back to HRS (process 3 to 4 in Figure 2.5). The SET process happens when the AE is again applied with a positive voltage. Thereby, a similar process as Forming will revert the cell to LRS by closing the filament at the gap (process 4 to 5 in Figure 2.5). Since the growth of filaments in the Forming process covers the entire length of the ion conductor layer, while in the SET process, a shorter gap needs to be closed, the SET voltage is lower than the Forming voltage. By manipulating the polarity of the applying voltage, the ECM can be reversibly switched between HRS and LRS. Due to the high mobility of the metal ions in the electrolyte, the resistive switching phenomena of ECM cells are drastic, which can be seen

from the abrupt fall/drop of current in the $I - V$ curves. The real dynamic process of forming and breaking filament in an ECM cell has been visualized through in- and ex-situ electron microscope technology during the past decades, including scanning electron microscope (SEM) [70, 71] and transmission electron microscope (TEM) [72, 73]. Thanks to the scalpel Atomic Force Microscope (AFM) technology, the CFs in ECM cells were visualized in 3D view [74, 75].

Valence Change Mechanism (VCM)

Valence change mechanism (VCM) based memristive cells are the other major filamentary devices. In comparison with ECM cells, this type of device relies on the migration of anions, mostly oxygen ions, in the transition metal oxides-based active layers [38]. In most of the transition metal oxide, oxygen ions are easier to move upon applying the external electrical field than the transition metal ions [76]. The migration of the oxygen ions away from its lattice leaves defects that are known as oxygen vacancy (V_o). V_o is regarded as positively charged and serves as a donor in n-type transition metal oxide semiconductors [77]. The enrichment or depletion of V_o results in a valence state change of the transition metal cations and consequently changes the conductivity of the transition metal oxide [76]. Many transition metal oxides have been reported as the active layer for VCM cells, including TaO_x [78, 79], TiO_x [50, 80], HfO_x [81, 82], WO_x [83, 84], YO_x [85, 86], and ZnO_x [87, 88], to name a few. Like ECM cells, VCM cells are also composed of two electrodes: active electrode (AE) and counter electrode (CE). For the AE, electrochemical stable metals such as Pt, Au, W, etc., with high work functions are required. AE is also termed Schottky electrode (SE) when discussing VCM cells. In an ECM cell, Ag and Cu are commonly used due to their electrochemical dissolution in the active layer, while for a VCM cell, the metal cation injection is unwanted. Instead, metals with high oxygen affinity are preferred for CE, such as Al, Ti, Ta, etc. The CE and the active layer generally form an Ohmic contact. Thus, CE is also called an Ohmic electrode (OE) in the discussion of VCM cells. Table 2.2 lists some reported VCM devices of different material stacks and their respective performances. To elaborate on the working

Table 2.2: List of typical VCM cells of different materials stack. Absence of parameter = "-" .

SE	Active layer	OE	$R_{\text{off}}/R_{\text{on}}$	Retention (s)	Endurance	Reference	Year
Pt	TaO_x	Ta	10	-	10^{10}	[78]	2010
Pt	TiO_x	Ti	10	10^4	2000	[89]	2020
TiN	HfO_x	Hf	10	-	10^{10}	[82]	2012
Pt	WO_x	Al	10	$> 10^4$	200	[90]	2016
Pt	YO_x	TiN	10^3	10^5	300	[90]	2016
Pt	ZO_x	Al	10^3	10^4	50	[91]	2013

mechanism of VCM cells from a microscopic point of view, a schematic in Figure 2.6 illustrates the processes of resistive switching in a generic VCM device model. The VCM memristive cells also rely on redox reactions between the electrode and the active layer. Differing from the ECM cells, the electrochemical reactions accounting for the resistive switching in VCM devices are generalized in the following three equations:

$$\mathrm{O_o^x} \rightarrow \mathrm{V_o^{\bullet\bullet}} + 2e^{'} + \frac{1}{2}\mathrm{O_2} \tag{2.6}$$

$$2\mathrm{Me}^{z+} + 2e^{'} \rightarrow 2\mathrm{Me}^{(z-1)+} \tag{2.7}$$

$$\mathrm{V_o^{\bullet\bullet}} + 2e^{'} + \frac{1}{2}\mathrm{O_2} \rightarrow \mathrm{O_o^x}. \tag{2.8}$$

In the above equations, $\mathrm{O_o^x}$ denotes the lattice oxygen ion, $\mathrm{V_o^{\bullet\bullet}}$ is the oxygen vacancy, $\mathrm{O_2}$ is oxygen oxidized from oxygen ions, and Me^{z+} represents lattice transition metal ion. In the Forming process, the positive voltage is applied to the SE, and while the OE is grounded, oxygen ions migrate towards the SE. The oxygen ions will be oxidized at the SE and released as gas, which is represented by Equation 2.6. The extraction of oxygen ions leaves oxygen vacancies behind [38]. As an equivalent view, this process can be described as the migration of positively charged Vo towards OE, resulting in the growth of the conductive path towards SE (processes (1) - (3) shown in Figure 2.6). Simultaneously, the sublattice metal ions along the filaments in the active layer are reduced to a lower valence state

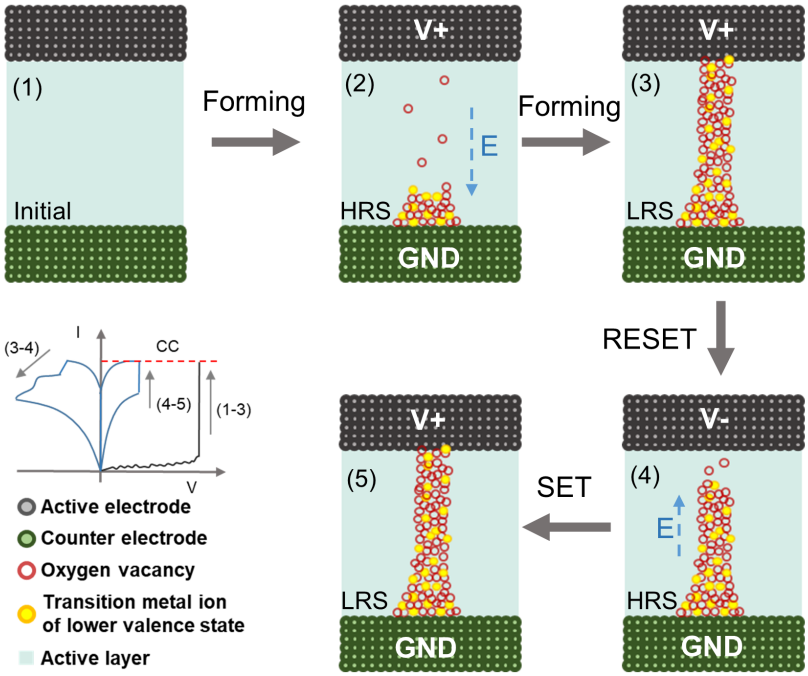


Figure 2.6: Mechanisms of VCM type memristors: A series of cross-sectional schematics illustrate the dynamic process of the filament evolution behind Forming, SET, and RESET. The numbered processes relate to the sections involved in the typical $I - V$ curves on a semi-logarithmic scale.

by combining with one free electron to complete the redox reaction pair, which is represented by Equation 2.7. For the RESET process, the SE is negatively biased. Thus, the oxygen vacancies are forced to be pushed away from the filaments and are filled again with oxygen ions, which are generated by reducing the oxygen at the SE (Equation 2.8 and processes (3) - (4) in Figure 2.6). Therefore, the cell is switched to HRS. The SET process is similar to Forming but is completed at a lower voltage since the conductive filaments are partially dissolved during the RESET. The introduced VCM mechanism here is only one typical model accepted by the community. The oxidation reaction can also happen at the OE by oxidizing the metals of high oxygen affinity, and the direction of the filament's growth can also be in the opposite manner. For a full spectrum of VCM cells, a comprehensive review [38] is recommended.

Thermochemical Mechanism (TCM)

Thermochemical mechanism (TCM) refers to the third class of filaments-based memristive devices that are derived from ECM and VCM but show unique resistive switching behavior. VCM and ECM cells show resistive switching in a bipolar manner, which implies the opposite polarity of SET and RESET voltages. On the contrary, the TCM cells work in unipolar form. For a TCM cell, the resistive switching between LRS and HRS can be triggered by a voltage of identical signs. Figure 2.7(a) demonstrates the typical $I - V$ curves of a VCM device. Similar to ECM and VCM devices, a Forming process is generally required for a TCM cell to initiate resistive switching. After the Forming, the SET and RESET can be achieved either under positive or negative bias. In general, the threshold voltage value of SET is higher than that of RESET. For the SET process, a CC is also needed to prevent a "hard breakdown" while for the RESET process, the CC is not required.

Both anion- and cation-based devices are reported to be categorized as TCM type. Therefore, the material selections of TCM devices overlap with ECM and VCM cells. The electrode materials include Pt, Au, Ag, and Cu. Almost all oxides reported in ECM and VCM also show TCM mechanism, including TiO_2 [92],

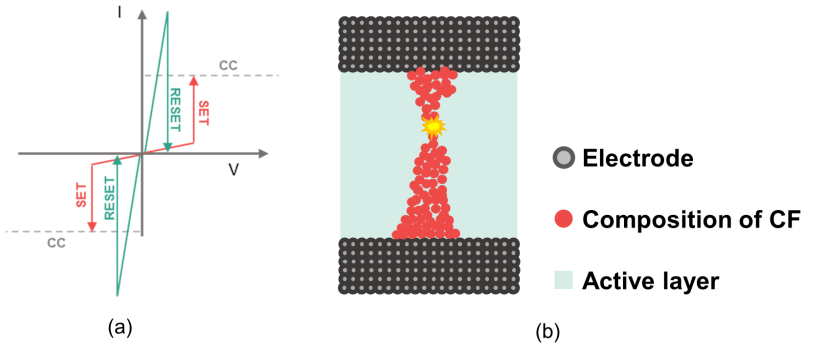


Figure 2.7: Schematics illustrates the resistive switching characteristics of TCM cells. **(a)** TCM cells show a unipolar resistive switching mode as the $I - V$ curves exhibit. **(b)** Rupture at the thinnest part in the middle of the filaments during the RESET.

HfO_2 [93], ZnO [94], Al_2O_3 [95], and NiO [96, 97]. Among them, the NiO system is the most well-known model to investigate the TCM mechanism since both metallic (Ni-based) and oxygen vacancy filaments are feasible to be formed within the NiO layer [61]. The Forming and SET mechanism of ECM and VCM cells can be applied to explain cation and anion-based TCM cells, while the RESET process of a TCM device, as the name implies, relies more on thermal effects that accelerate the ion migration between the filaments and surrounded metal oxide matrix. Compared to the ECM and VCM devices, the filaments in the TCM devices rupture in the middle instead of in the vicinity of either electrode (as Figure 2.7(b) shows). The ion diffusion process of RESET differs between anion and cation-based TCM cells. In an anion-based cell, the filaments are composed of highly conductive oxygen vacancies. The current flowing through the filaments leads to a local temperature increase, which promotes the movement of oxygen ions towards the oxygen ion depletion region. This leads to the oxidization of the filaments and breaks the conductive bridge at the weakest point. In a cation-based cell, the heating effect promotes the diffusion of the metal ion from the filaments radially toward the surrounding metal oxide matrix, resulting in a rupture at the thinnest part of the filament.

2.4.2 Non-filamentary

In addition to the filamentary-type memristive devices, there is another class of devices that function without the conductive path between the electrodes. For this type of device, the resistive switching occurs either at the interface between the electrode and active layer or within the whole active layer. Accordingly, this class of memristive devices is categorized as "non-filamentary". Compared to the filamentary type, the resistance values (two or multiple resistive states) of non-filamentary cells are dependent on the effective device area. In other words, the on- and off-currents will be scaled with the size of the device. In the case of filamentary devices, the on-current is independent of the device size until it shrinks to the dimension of the filaments [60]. In general, compared to the filament-type counterparts, non-filamentary devices show unique properties such as relatively slower resistive switching speed, shorter retention time, smaller range of resistive states, good uniformity, high device yield, forming-free, and low working current. There are no absolute advantages or disadvantages with respect to the device figure of merit. The discussion of the pros and cons needs to be drawn based on the applications. The filamentary devices are advantageous for non-volatile memory and logic-related applications, whereas the non-filamentary cells are powerful in implementing neuromorphic computing. The underlying mechanisms accounting for the non-filamentary resistive switching are manifold. They include but are not limited to "ion migration", "electron trapping/de-trapping", "ferroelectric effect", and "phase transition". In the following sections, the different types of non-filamentary devices will be briefly introduced.

Ion Migration

Metal oxides are the main family of materials that compose the MIM structure of memristive devices as the "I" layer. "I" stands not only for isolators but also can be semiconductors. With regard to memristive devices, transition metal oxides including TaOx [98], TiOx [99], and WOx [100] are reported to be used for resistive switching devices. In addition, some ternary and complex oxides (e.g.,

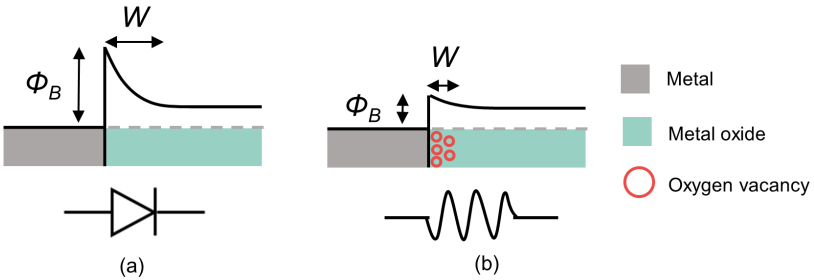


Figure 2.8: Oxygen vacancy concentration dependent band structure at the metal/metal oxide interface. **(a)** Schottky barrier height (ϕ_B) and the width (W) results in a current rectifying characteristic. **(b)** An Increase in the oxygen vacancy concentration at the metal/metal oxide interface can reduce both the barrier height and width, which elevates the conductance of the junction and changes the junction to a resistor-like characteristic.

LSMO [101], PCMO [77], and Nb-doped $SrTiO_3$ [102]) are also investigated as the active layer of the memristive cell. Within the MIM structure, the selected metal oxide semiconductor layer will form a Schottky contact with one of the metal electrodes, which possesses a high work function (such as Pt). The difference between the work function of the metal electrode (ϕ_M) and the electron affinity of the metal oxide semiconductor layer (χ_S) is expressed as Schottky barrier height (ϕ_B) [103], and the relation is written as:

$$\phi_B = \phi_M - \chi_S. \tag{2.9}$$

Schottky barrier results in high contact resistance (Figure 2.8(a)) due to the depletion of major charge carriers at the interface between the metal electrode and active layer [60]. The Schottky barrier's height and width (W) can be determined by the concentration of the dopants at the interface region [60]. In the case of metal oxide semiconductors (most are working as n-type semiconductors), oxygen vacancies (V_o) behave as dopants. Therefore, the electrical field-triggered migration of V_o within the active layer will result in resistive switching. Figure 2.8 shows the change of Schottky barrier height and width corresponding to the concentration of V_o at the interface, which is attributed to the resistive switching phenomena in an n-type metal oxide semiconductor-based memristive cell. When

the metal electrode is applied with a negative bias, the positively charged V_o will be attracted towards the electrode and accumulate at the interface. Consequently, the Schottky barrier height and width at the electrode/active layer interface are reduced due to the increasing concentration of the dopants (Figure 2.8(b)). The cell changes from a low to a high conductive state. Moreover, since the width of the ϕ_B at the interface is narrowed as well when the concentration of V_o is increased [60], the electron tunneling is facilitated, which enhances the conductive state of the cell. On the contrary, when the metal electrode is biased with a positive voltage, the V_o will be repelled away from the electrode/active layer interface back to the bulk of the active layer, by which the height and the width of Schottky barrier will recover to the low conductive state. In this way, the resistance of the cell can be modulated by the applied voltage. Compared to the abrupt resistance change in the filamentary devices, the ion migration-based memristive cells show a gradual change in conductance. This unique property resembles the plasticity of the biological synapse and thus is of high interest to mimic synaptical behavior. It is worth noting here that when the external electrical field is removed, the accumulated V_o at the interface is prone to diffuse spontaneously back to the bulk of the active layer due to the concentration gradient. This explains the short retention time of this type of memristive device. Interestingly, this volatility can be utilized to emulate the forgetting behavior of humans, which is crucial for information processing [30, 60, 104]. In an ion migration device based on a p-type semiconductor, the V_o works oppositely at the electrode and active layer interface, where the high concentration of V_o will lead to the increase of the barrier height and width.

Phase Transition

The crystalline and amorphous phases of a chalcogenide phase change material, such as $Ge_2Sb_2Te_5$ (GST), generally exhibit two different conductive states. The transition between the two phases can be reversibly triggered by controlling the critical temperature, consequently alternating the conductivity of the phase change material. This phase-dependent conductance property is intensively and also

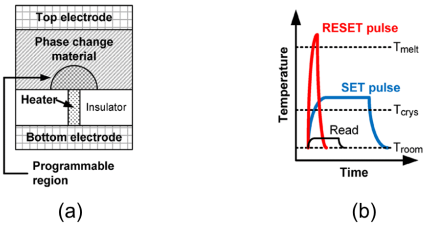


Figure 2.9: Device structure and operation pulses. **(a)** Cross-sectional schematics of a typical PCM cell consisting of a top electrode, phase-change materials, and a pillar-like bottom electrode. The phase-change region exhibits a hemispherical shape. **(b)** Voltage pulses of different amplitude and duration elevate the temperature of phase-change material to different levels, through which the ratio of the crystalline phase in the phase-change layer is tunable. © [2010] IEEE. Reprinted with permission from [105].

well-studied for a class of memory devices, phase change memory (PCM) [105]. A PCM cell generally consists of a top electrode, a phase change material in the middle, and a pillar-like bottom electrode (Figure 2.9(a)). Starting from the amorphous phase, Joule heating induced by a relatively low-voltage pulse increases the temperature, exceeding the crystallization temperature (i.e., $T > T_{crystal}$). The crystalline phase is thus formed, and the cell switches to a low resistive state (SET) [105]. On the contrary, RESET operation is achieved through the crystalline phase melting and quenching into the amorphous phase when applied with a higher voltage pulse, which raises the temperature above the melting point ($T > T_{melt}$) [30]. With respect to the time duration, the process of crystallization requires a longer time than the melting. The relation between the temperature and time of SET and RESET pulse is shown in Figure 2.9(b). The resistance of the cell is read by applying a smaller voltage, which will not trigger phase transition. A PCM cell typically has a mushroom shape in the phase change area in the middle layer (Figure 2.9(a)) since the pillar-like bottom electrode confines the heat and current, thus resulting in a hemispherical shape of the molten region [48]. The large concentration of carriers in the crystalline phase is regarded as the reason for the high conductivity, while the high resistance of the amorphous phase is due to its intrinsic semiconductor nature originating from Fermi-level pinning at the mid gap [48]. In a PCM cell, different volume ratios of the crystalline phase to the amorphous phase are possible by controlling the amplitude of the voltage pulse.

Therefore, an analog resistance change of a PCM cell can be achieved. This is a preferred property for neuromorphic applications [30].

Electron Trapping/de-trapping

In solid-state physics, traps within a semiconductor or insulator refer to new energy levers within the energy gap that are induced by the defects or impurities in the materials [106, 107]. The traps are energy-preferred locations for charge carriers (lower energy lever in conduction band for electrons and higher energy level in valence band for holes) and thus tend to immobilize charge carriers [49]. The charge carriers injected from the electrode under the electrical field, for instance, electrons, can be trapped within the material (Figure 2.10(a)). This phenomenon will modify the band structure or the interface properties, which may change the electron transport properties and thus result in a change in the resistance. The material can be recovered to its original resistive state upon the release of the trapped electrons [49]. The retention time of the electron-trapped resistive states depends on the barrier height of the trap, which implies the energy that electrons need to de-trap. This electronic effect-induced resistive switching behavior is used to design another non-filamentary type of memristive cells. These pure electronic effect-based devices are generally in a MIM stack or in a junction structure involving metal oxide materials, such as TiO_x [108], WO_x [109], $Ba_{0.7}Sr_{0.3}TiO_3$ [108], $NbO_x/TiO_x/NbO_x$ [110], and $Ta_2O_5/Nb_2O_{5-x}/Al_2O_{3-y}$ [111]. Depending on the position of the conduction-limited trap sites, this class of electron-based memristive devices is categorized into two types: electrode-limited and bulk-limited. The resistive switching behavior of the electrode-limited cells is ascribed to the change in the height and width of the Schottky barrier between the active layer and the electrode, which is induced by trapped electrons at the interface [60]. For the bulk-limited type, the resistance transition between different states is well described with the trap-controlled space-charge-limited conduction (SCLC) model [106]. This model attributes the low conductive state to trap-unfilled SCLC, while the trap-filled SCLC accounts for the high conductive state of the active layer [106].

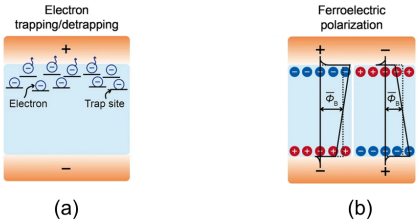


Figure 2.10: Schematics of working mechanisms. **(a)** Electron trapping/de-trapping. The trap site is a lower energy level spot in the active layer that can trap electrons. The filling state of the electron in the trap determines the conductance of the cell [60]. **(b)** Ferroelectric effect. The polarization direction determines the electron transport characteristics at the interface [60]. Reproduced under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

Ferroelectric Effect

Ferroelectric materials, such as lead zirconate titanate (PZT) [112] and $Hf_{0.5}Zr_{0.5}O_2$ [113], possess multiple spontaneous polarizations without an external electric field. The polarization can be changed in a nonvolatile manner upon application of a sufficient high external electrical field. The nonvolatility and tunability render a class of ferroelectric materials applied in transistor-based memory devices, such as ferroelectric random access memory (FeRAM) and ferroelectric field-effect transistor (FeFET). Recently, this class of materials has been studied as the active layer in a two-terminal resistive switching memory device, ferroelectric tunnel junction (FTJ). This class of resistive switching devices is classified as electronic-effect-based devices under the non-filamentary group. In general, an FTJ consists of two electrodes separated by a layer of ferroelectric material. The electron transport properties at the electrode/ferroelectric layer interface depend on the polarization direction. The Schottky barrier width is reduced (increased) when the polarization in the space-charge region is parallel (anti-parallel) to the internal electric field [49, 60]. These phenomena are illustrated in Figure 2.10(b). Therefore, the resistive switching can be ascribed to the change in the Schottky barrier width induced by the abrupt reversal of the polarization coercive field [49, 60].

2.5 Printing Technologies

Various printing techniques are applied to fabricate electronic devices and circuits and are mainly categorized into two families, e.g., contact and non-contact type. The contact type refers to the printing process in which the ink carrier directly interacts with the substrate to complete the pattern transfer. This type of printing technique includes screen printing, gravure printing, and flexography printing [6, 114]. In contrast, a certain distance exists between the printer's nozzle and the substrate for the non-contact type. In this case, the ink is generated as droplets and is deposited onto the substrate through a nozzle. Inkjet printing, electrohydrodynamic (EHD) jet printing, and aerosol jet printing belong to this printing category [6, 114]. Overall, the contact types are more production-efficient and more tolerant to ink viscosity but prone to errors in printing small patterns, whereas the non-contact types are more advantageous in printing small structures (can be down to sub μm) but rely largely on the property of the inks and substrates. Figure 2.11 compares these two types of printing categories with respect to the feature size of the printed object and the viscosity range of the available inks.
Regarding the application, contact printing techniques are commonly used in the industry for printing commercialized products, while non-contact printing techniques are preferred for research purposes in the institute. In recent years, laser printing based on two-photo absorption has been applied to PE. This technique was initiated for printing polymer 3D structures in the nm range and now is facilitating PE in the direction of smaller feature sizes and into the third dimension. Since the devices in this thesis are printed through inkjet and laser, only these two techniques will be introduced in detail in the next sections.

2.5.1 Inkjet Printing

Inkjet printing is a non-contacting printing technology in which the individual droplet of ink is ejected from the nozzle and dropped onto the substrate. The mechanisms of generating the ink droplet are classified into two types. They are thermal and piezoelectric effects-driven types [6, 115]. The nozzle is equipped

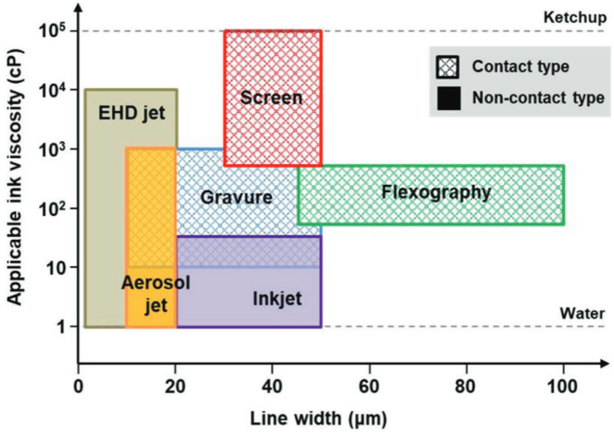


Figure 2.11: Comparison between different printing techniques in terms of applicable ink viscosity and the ranges of the printed line width. © 2019 WILEY-VCH Verlag GmbH & CO. KGaA, Weinheim. Reproduced with permission from [114].

with a piezoelectric transducer for the piezoelectric type, as shown in Figure 2.12. During operation, a series of square voltage pulses are applied to the piezoelectric transducer. Therefore, the deformation of the piezoelectric transducer will generate a pressure wave in the nozzle, and consequently, the ink will be repelled out of the nozzle and ejected onto the substrate [115]. The actuator is replaced with a micro-electrical heating element for the thermal effect-driven type. An electrical current will serve as input for the heating element, resulting in the vaporization of the ink inside the chamber (shown in Figure 2.12); consequently, a microbubble is generated, which increases the pressure to propel the ink out of the nozzle [115]. To execute a printing task, a pattern will first be designed composed of numbers of pixel dots. Each pixel dot represents a droplet of the ink that will be jetted. The designed pattern will be printed drop-by-drop by controlling the movement of the nozzle or the printing target.

Inkjet printing is a versatile printing technology that can be used to print various materials spanning from polymers, metals, and metal oxides to novel 2D and 1D

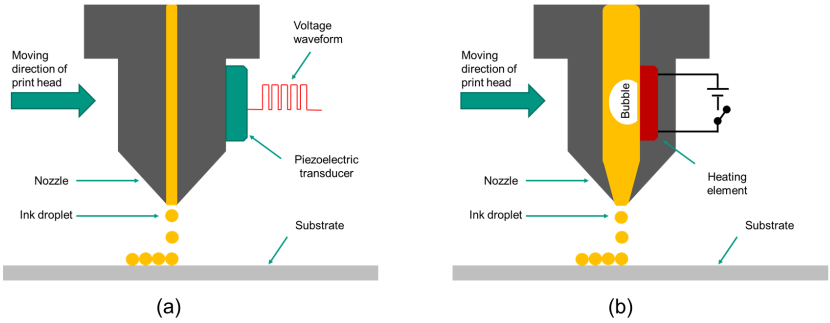


Figure 2.12: Working mechanism of inkjet printing. **(a)** Schematic of piezoelectric effect driven inkjet printing. **(b)** Schematic of thermal effect-based inkjet printing.

materials [2, 116, 117, 118]. In principle, as long as one material can be formulated into an ink that meets the requirements for inkjet printing, it can be printed. The key requirements of the ink include low viscosity, low particle size, and low volatility to avoid nozzle clogging [6]. Therefore, there is a vast material option for conductors, semiconductors, and insulators, which are crucial materials for building electronic devices.

Thanks to the diversity of the inkjet-printable materials, almost all electronic components can be inkjet-printed, included but not limited to field-effect transistor [10], sensors [9], solar cells [11], diodes [12], displays [13], memristors [116], capacitors [14], and antennas [15]. The minimum feature size and resolution that can be achieved by inkjet printing are in the tens of μm [115].

2.5.2 Laser Printing

Multi-photo 3D laser printing, also referred to as 3D laser photolithography or 3D direct laser printing, is an additive manufacturing technique that is powerful in fabricating 3D micro-nano structures. During the printing process, the focused laser induces multi-photo absorption in the photoresist (ink), which triggers a chemical reaction resulting in a transition from liquid to solid phase. Scanning the laser focus within the photoresist in all three dimensions will print a designed

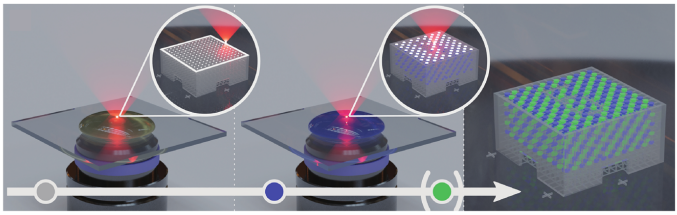


Figure 2.13: 3D multi-material printing with multi-photon laser printing. On a transparent substrate, different photoresists are drop-casted and exposed to the laser writing focus sequentially. By repeating the steps of "photoresist drop-casting - exposure to laser - washing residual photoresist," multi-materials are printed in 3D microstructure. The printed structures do not need to be 3D but also 2D, meaning 500 nm to 10 µm laterally, and a few 10s to 100 nm in thickness are possible (thin films) [119]. Reproduced under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

3D structure, and the part of the ink that is not solidified will be washed away after printing. Depending on the utilized photoresist, the underlying chemical reactions differ greatly. For instance, laser induces local cross-linking in monomers to achieve polymerization. In the case of metal salts, the laser leads to the reduction of the metals and leaves metal nanoparticles behind the movement of the focus in the solution [119, 120]. Figure 2.13 presents the general setup and printing process of the multi-material with multi-photon 3D laser printing. Compared to the other printing techniques, multi-photo laser printing possesses the smallest feature size of the sub-micrometer [119].

3D laser printing has been utilized to print various materials, including polymers, metals, glasses, etc. [119]. The printed objects are mainly applied in optical, mechanical, and biological research fields. Since the printing of electronically active semiconductor materials with laser printing is rarely reported, this advanced micro- and nanometer additive manufacturing technique has not been used for microelectronics before and is one of the main focuses of this thesis [121]. In this work, metals (Ag and Pt) and a semiconductor (ZnO) are laser printed to fabricate several electronic components (including diode, memristor, and transistor). In Chapter 3 and Chapter 6, the details of the laser-printed electronics will be introduced.

3 Methods

3.1 Fabrication

3.1.1 Inkjet Printing

The general fabrication processes of inkjet-printed memristors, as they are printed within this thesis, are illustrated in Figure 3.1. The inkjet-printed devices within this thesis are classified into two types, e.g., fully and partially printed, depending on whether the bottom electrode is printed. Both device variants are fabricated on a glass substrate but differ in the BE preparation process. For the fully printed one, prior to printing the BE, the glass substrate was cleaned by ultra-sonication for $20\,\mathrm{min}$ with a mixture of acetone and isopropanol (ratio of 1:1). Next, the BE was printed onto the cleaned glass substrate and followed by a sintering process in ambient condition to eliminate the residual solvent. For partially printed devices, a conductive material-coated glass was patterned with laser ablation, after which the designed BE was cleaned using the same procedure. After the BE was prepared, the active layer material was inkjet printed onto the BE. Depending on the material used as the active layer and BE, sintering with different conditions was performed for post-treatment of the active layer. Finally, TE was inkjet-printed onto the active layer perpendicular to the BE, forming a crossing point with the BE. The effective size of the inkjet-printed memristor is defined by the width of the TE and BE. The parameters of the printing and post-treatment of used inks are listed in Table 3.1. The detailed information on ink formulation is described in the Appendix.

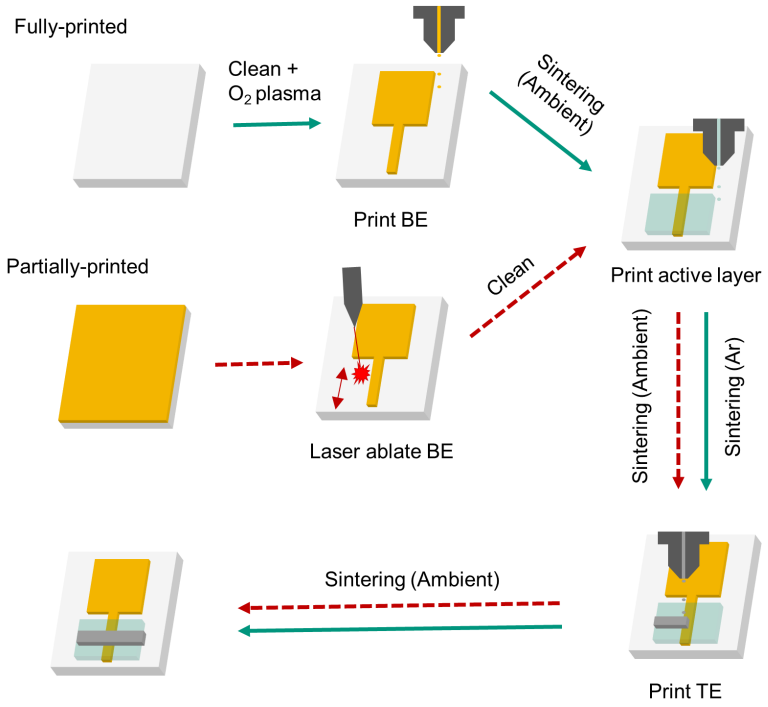


Figure 3.1: Schematics of the fabrication processes of fully- and partially-printed memristors.

Table 3.1: Treatment conditions of inks in and after printing. ROOM TEMPERATURE = "RT". *Active layer in the partially-printed device. +Active layer in the fully-printed device.

Ink	In printing	After printing
Ag	Printer stage temperature (50 °C)	Sintering in oven (100 °C, 1 h, Ambient)
$Zn(NO_3)_2^*$	Printer stage temperature (RT)	Sintering in oven (400 °C, 2 h, Ambient)
$Zn(NO_3)_2^+$	Printer stage temperature (RT)	Sintering in oven (400 °C, 2 h, Ar)
WO_{3-x}^*	Printer stage temperature (RT)	Sintering in oven (120 °C, 1 h, Ambient)

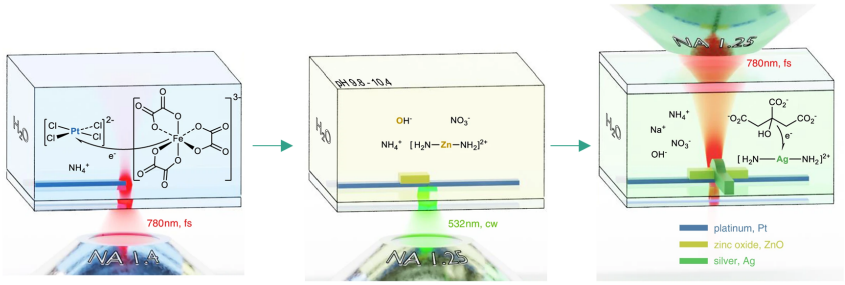


Figure 3.2: Process of laser printing of a memristor. From left to right: Laser-induced reduction of Pt in the Pt ink; Laser-induced local photothermal synthesis of ZnO on the surface of Pt; Laser-induced reduction of Ag on the surface of ZnO. Adapted from [121] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

3.1.2 Laser Printing

The laser-printed memristors were printed on a cover glass. The cover glass was treated with oxygen-plasma for $10\,\mathrm{min}$, after which the cover glass was immersed in a solution of (3-aminopropyl) Triethoxysilane dissolved in toluene (0.2% vol.) for $60\,\mathrm{min}$ for the purpose of silanization. The silanized glass surface improves the adhesion of the platinum particles during the laser printing. A PDMS frame was placed onto the silanized cover glass to confine the ink, which will be drop-casted afterward. In addition, a second piece of PDMS was put onto the PDMS frame with the ink, preventing solvent evaporation during printing. This setup is illustrated in Figure 3.2.

The printing follows a sequence of Pt, ZnO, and Ag, as shown in Figure 3.2. Three different inks were used, and the laser parameters were adjusted to guarantee an appropriate printing quality. Table 3.2 lists the inks and utilized laser parameters. After printing the Pt, the samples were washed in de-ionized water for $5\,\mathrm{min}$ and dried by blowing nitrogen on the glass substrate. After printing the ZnO, the samples were first washed in de-ionized water for $5\,\mathrm{min}$ and then in ethanol for another $5\,\mathrm{min}$. The samples were blown with nitrogen gas for drying. The detailed information on inks and laser setup is described in the Appendix.

Table 3.2: Laser printing parameters of the inks. NUMERICAL APERTURE = "NA". FETOSECOND = "fs". CONTINUOUS-WAVE = "cw".

Ink	Lens NA	Laser parameters			
		Type	Wavelength (nm)	Power (mW)	Speed ($\mu\mathrm{m/s}$)
Pt ink	1.4	fs	780	0.5 - 1.2	5 - 10
ZnO ink	1.25	cw	532	21.5	20
Ag ink	1.25	fs	780	0.35 - 0.7	10 - 20

3.2 Electrical Characterization

3.2.1 Quasi-static Measurements

The basic electrical characteristics of the printed memristors were determined from the current-voltage ($I - V$) curves, which are obtained from quasi-static measurements. Quasi-static measurements are also referred to as quasi-DC measurements. In this thesis, the meaning of quasi-static measurements lies in slowly ramping voltage over the device under test (DUT) while monitoring the current that flows through the device. The measured current-voltage relations were used to determine the resistive switching mode of the studied devices (e.g., digital or analog, bipolar or unipolar), switching parameters (e.g., SET and RESET voltage, $R_{\mathrm{off}}/R_{\mathrm{on}}$ values) and the appropriate compliance current level. Moreover, the $I - V$ cures are plotted on a logarithmic scale [28, 106] to investigate the possible conduction mechanism through the linear fitting of the curves. In this thesis, the quasi-static measurements were conducted with a semiconductor parameter analyzer (4200A-SCS, Keithley). The DUTs were probed with a probe station (MPS 150, Cascade). The connection is illustrated in the diagram shown in Figure 3.3(a). Figure 3.3(b) is the equivalent circuit diagram. The electrical measurements were carried out at room temperature and in ambient atmosphere. If there is no specific notation, the BE is always grounded while the voltage is applied to the TE. Voltage multi-segment sweeping mode is used to perform the

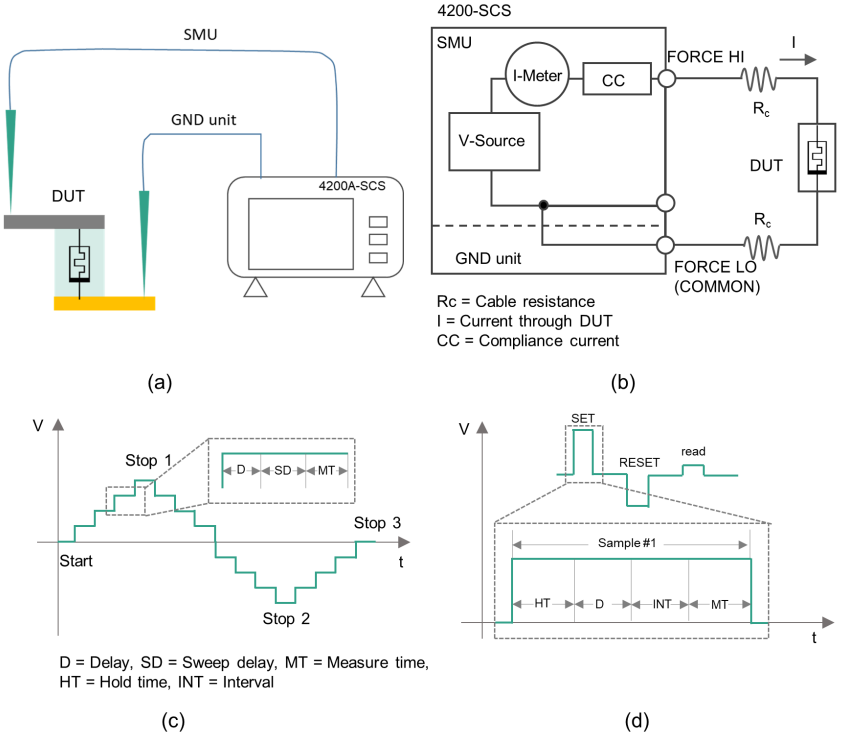


Figure 3.3: Schematics of quasit-static measurements. **(a)** The memristor under test is probed with the tungsten needle of the probestation. The TE is generally sourced with voltage while the BE is grounded, connecting to the semiconductor parameters analyzer in this thesis. **(b)** Equivalent circuit diagram of the connection between the DUT and semiconductor parameters analyzer. **(c)** Waveform of the quasi-DC voltage sweeping. **(d)** Waveform of sampling mode performed with the semiconductor parameters analyzer.

quasi-DC measurement, where the waveform is shown in Figure 3.3(c). The voltage is increased/decreased in a linear staircase form. Each voltage step increment consists of three timing elements, e.g., delay, sweep delay, and measurement time. In quasi-DC sweeping, the normal speed mode was selected, which is translated into the time duration of each step as ca. $60\,\mathrm{ms}$. The voltage amplitude increase is defined as a sweep rate (V/step). In addition, the sampling mode (waveform see Figure 3.3(d)) of the source measure unit (SMU) was used to apply a pulse. Due to the limitation of the four-time elements shown in the waveform, e.g., hold time, delay, interval, and measure time, the minimum time duration of the generated pulse is ca. $100\,\mathrm{ms}$. The sampling mode was used to program SET-RESET-read cycles to perform endurance tests. The timing of the sampling is not ideal for endurance tests (hundreds of ms versus $\mu\mathrm{s}$ of application standards). However, CC is available in the sampling mode, which is crucial for reducing switching failures during the endurance test. For fast pulse measurement, an additional CC device, such as FET or resistor, is required to limit the current since the Keithley PMU does not support CC.

3.2.2 Dynamic Pulsed Measurements

The study of the dynamic characteristics of the memristive devices, such as the switching time or the transient current response upon the application of the voltage, demands short pulse stimuli (ranging from $\mu\mathrm{s}$ to ns). The setup shown in Figure 3.4(a) was used to perform the dynamic pulse measurements. A pulse measurement unit (4225-PMU, Keithly) embedded in 4200A-SCS was used to generate a short voltage pulse. The output signal was transferred to the TE of the memristor under test through a remote preamplifier module (4225-RPM), which works as a current preamplifier for the 4225-PMU, providing additional high-speed, low-current measurement ranges. The BE of the memristor under test was connected to the ground unit of the semiconductor parameters analyzer. To capture the transient change of the current flowing through the memristor, a load resistor (R_{load}) was connected in series to the memristor. The current is calculated by dividing the voltage drop on the R_{load} by its known resistance. The voltage

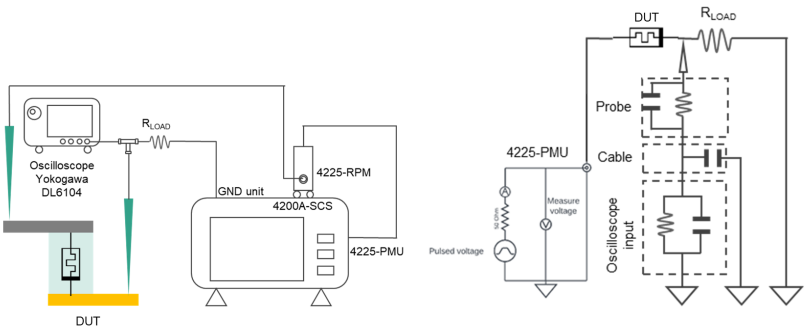


Figure 3.4: Schematics of setup used in dynamic pulsed measurements. **(a)** Connection of the memristor under test to the pulse measurement setup consisting of a pulse management unit, a remote preamplifier module, a ground unit, and an oscilloscope. **(b)** Equivalent circuit diagram of the setup connection.

was measured with an oscilloscope (DL6104, Yokogawa) that has a passive 10:1 attenuated probe (701939, Yokogawa). The equivalent circuit diagram of the measurement setup is shown in Figure 3.4(b).

4 Printed Memristors for Non-volatile Memory

4.1 Introduction to Printed Non-volatile Memory

Non-volatile memory refers to the class of information storage technologies in which the written data can be retained for a long period of time, even after the removal of the power supply. Non-volatility is desirable for printed electronic systems since it reduces system complexity by eliminating the peripheral circuitry, which is required in volatile memories to refresh the stored data periodically. Moreover, the ability to maintain data without a constant power input reduces the performance requirements of the power supply unit. These two factors work synergistically to mitigate the challenges of achieving fully printed electronic systems. For CMOS-based electronics, as briefly introduced in Chapter 2, Flash memory dominates the non-volatile memory market. Alternatively, emerging non-volatile memory technologies, including phase change memory (PCM), magnetic random access memory (MRAM), resistive random access memory (RRAM), and ferroelectric memory, have also gained tremendous momentum in research and are expected to improve the performance of non-volatile memories. However, the situation for printed non-volatile memory is different. Considering the manufacturing compatibility, PCM and MRAM are rarely reported for printed non-volatile memory. This is due to the strict requirements that are exposed on the active layer materials, such as surface property, low defect density, and crystallization, which require vacuum-based deposition methods (e.g., sputtering or atomic layer

deposition (ALD)) [122]. Printed transistor-based non-volatile memories, including floating gate FET [123], charge trap FET [124], and ferroelectric FET [125], have been reported. However, none of the transistor-based non-volatile memory has shown explosive growth in the field of PE. There are two main reasons: (a) the material selection of transistor-based non-volatile memory is still limited to polymers; (b) the relatively short retention and high operating voltage are the main obstacles to the development of printed transistor-based non-volatile memory.
In contrast, research in solution-processed RRAM has been particularly prosperous in recent years. Many publications of solution-processed memristors were circulated, spanning from stand-alone devices to applications [41, 126]. Memristors dominate the niche of solution-processed non-volatile memory and hold the biggest potential in real applications. Memristors surpass the other storage devices in solution-processed non-volatile memory due to: (a) Diversity in material selections. The reported active layer materials in solution-processed memristors cover almost all categories, including metal oxides, perovskites, polymers, 2D materials and their derivates, metal-organic frameworks (MOFs), covalent organic frameworks (COFs), biomaterials (e.g., silk fibroin) [126, 127], to name a few. The wide range of material choices allows device engineers to develop better memristors with a high degree of freedom. (b) Simple device structure. The capacitor-like three-layer architecture is relatively fabrication-friendly compared to the other more complex three-terminal devices. In particular, for solution-based fabrication technologies, such as printing, precise alignment of multiple components during fabrication is a huge challenge. The simple sandwich structure fosters the development of solution-processed memristors for large-scale applications. (c) Last but not least, performance. Due to the relatively low quality of solution-processed materials, the performance of transistor-based non-volatile memories lags behind that of vacuum-processed devices. On the contrary, the reported critical figures of merit of solution-processed memristors, such as endurance, retention, $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio, switching speed, and operation voltage, are on a par with their vacuum-processed counterparts. Table 4.1 compares the state-of-the-art performance between solution- and vacuum-processed memristors as non-volatile memory (disregarding material and fabrication technology). The

Table 4.1: Comparison of state-of-the-art performance between vacuum- and solution-processed memristors.

Categories	Endurance	Retention (s)	$R_{\mathrm{off}}/R_{\mathrm{on}}$	Speed (ns)	Operation voltage (V)
Vacuum -processed	10^{12} [128]	10^{7} [129] (150 °C)	10^{6} [130]	0.3 [131]	0.5 [132]
Solution -processed	10^{12} [133]	10^{6} [134] (165 °C)	10^{9} [135]	0.3 [133]	0.1 [136]

comparable performance between the solution- and vacuum-processed memristors may stem from the determined factor in the underlying mechanism, i.e., the defect density in the active material. Theoretically, higher defect density benefits the performance of a memristor, such as lower operation voltage [38]. Interestingly, the enrichment of defects in solution-processed materials is the point that is often cited as the cause for poor performance in other charge-based electronic devices (e.g., transistors) [10].

Solution-processed memristors have been validated as promising non-volatile memory, manifesting excellent electrical performance [126]. These two-terminal resistive switching devices are envisioned to be widely applied as memory units in emerging fields, including large-scale sensing, the Internet of Things (IoT), wearable electronics, intelligent packaging, and so forth. However, most of the reported memristive devices fabricated by solution methods have a common BE (shown in Figure 4.1(a)). Although this structure largely simplifies the fabrication process and facilitates the research of the device, it is unlikely to be used in a real application. To function as a memory unit, a certain number of memristive cells are required to be interconnected in a cross-bar architecture, as shown in Figure 4.1(c). Each device within the cross-bar is formed by a cross-point defined by the perpendicular TE and BE (Figure 4.1(b)). Therefore, a cross-point structure is ideal for investigating the device's characteristics. As introduced in Chapter 2, solution-based manufacturing methods, such as various printing technologies, are powerful in achieving patterning structures in a cost-efficient, mask-free, and

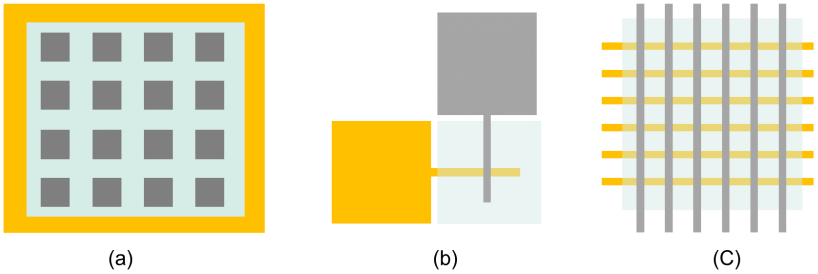


Figure 4.1: Schematics of the typical form of the memristor in research. **(a)** Common bottom electrode. **(b)** Cross-point form. **(c)** Cross-bar architecture.

bottom-up manner. Printing technologies are promising in fostering the development of solution-processed memristors for various applicable applications. Nevertheless, the research of printed memristors is still in an early stage and is evolving gradually. In particular, fully printed memristors are rarely reported. Under this circumstance, three types of metal oxide memristors developed with inkjet printing are presented in this chapter. The inkjet-printed memristive cells are systematically characterized, showing excellent electrical performance that is promising for non-volatile memory in PE. The results presented in this chapter are also published in [137, 138, 139].

4.2 Inkjet-printed Memristors Based on Metal Oxide Precursor Inks

The results in this section were also reported in [137, 138].

In this Section, two types of inkjet-printed memristors based on metal oxide precursor inks are presented. Zinc oxide (ZnO) is selected as the active layer material in both cases, and an aqueous zinc nitrate-based salt precursor ink was developed for printing (details of the ink see Appendix). The reasons that ZnO is selected as the active layer material in printed memristors for non-volatile memory applications include: (a) ZnO is a wide band gap metal oxide semiconductor ($3.3\,\mathrm{eV}$) and has a high redox potential, as well as good physical and chemical stability. These properties synergistically make the ZnO-based devices promising for non-volatile memory since they show excellent performance, including large memory window, high retention time, and the existence of unipolar and bipolar resistive switching behavior [39, 140, 141]. (b) ZnO is easily obtained from multiple salt-based precursor solutions through the sol-gel chemistry method. These zinc salt-based precursor solutions are ideal for ink preparation.
The two inkjet-printed memristors presented in this Section differ in terms of electrode materials, e.g., one is an asymmetric structure consisting of Ag/ZnO/Au (named AZAu in the later discussion), and the other is a symmetric structure consisting of Ag/ZnO/Ag (named AZAg in the later discussion). AZAu was partially inkjet-printed while the AZAg was fully printed (fabrication processes see in Chapter 3). The different material stacks and fabrication procedures render two devices with different working principles. In the following, the device structure, device performance, mechanism analysis, and advanced dynamic characteristics are presented.

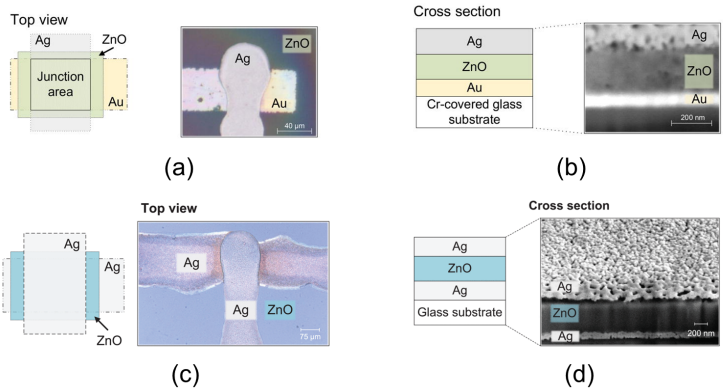
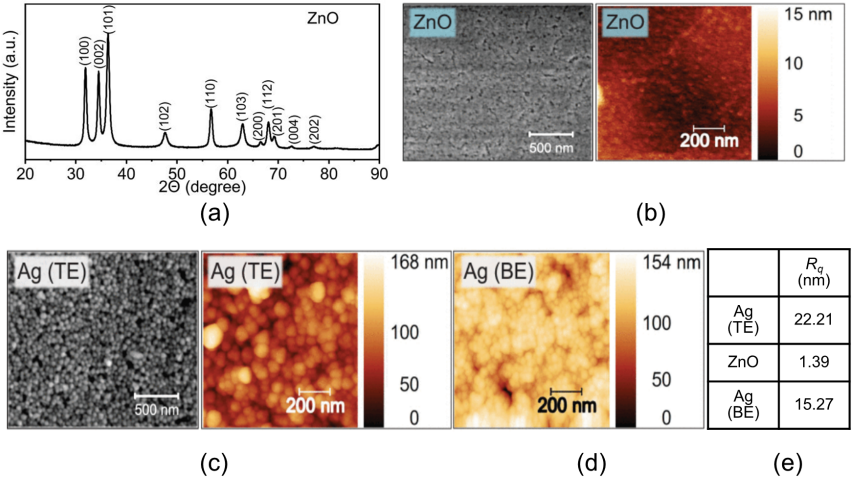


Figure 4.2: Device Structure of two inkjet-printed memristors based on ZnO precursor ink. Top view and microscopic image of AZAu **(a)** and AZAg **(c)**. Schematic cross-section of the device with corresponding SEM cross-sectional micrograph of AZAu **(b)** and AZAg **(d)**. (a) and (b) are adapted from [137], © 2021 AOP Publishing. (c) and (d) are adapted from [138] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

4.2.1 Device Structure

AZAu device is composed of a laser-ablated Au BE, an inkjet-printed ZnO layer, and an inkjet-printed Ag TE. Figure 4.2(a) displays the layout of the Ag/ZnO/Au memristor from the top view. The size of the effective device area, also labeled as the junction area, depends on the width of the top and bottom electrodes, which form the crossing junction of the sandwiched ZnO storage layer. The inkjet-printed memristor junction area is $\approx 50\,\mu\text{m} \times 50\,\mu\text{m}$ for the fabricated devices, as shown in the microscopic image on the right-hand side of Figure 4.2(a). The vertical structure of AZAu is schematically and optically illustrated in Figure 4.2(b) using SEM. The thickness of the material stack can be determined as Ag $\approx 80\,\text{nm}$, ZnO $\approx 200\,\text{nm}$, and Au $\approx 45\,\text{nm}$. For the structure of the AZAg device, the BE was replaced with inkjet-printed Ag. Therefore, a fully printed memristor was achieved. Figure 4.2(c) shows a schematic and an optical image of the fabricated memristor. The effective area of the fully inkjet-printed device is ca. $150\,\mu\text{m} \times 150\,\mu\text{m}$ and is formed at the cross-point of the top and bottom



	R_q (nm)
Ag (TE)	22.21
ZnO	1.39
Ag (BE)	15.27

Figure 4.3: Material characterization of printed thin film. **(a)** XRD patterns of the ZnO active layer transformed from zinc nitrate aqueous precursor ink. **(b)** SEM and AFM micrograph of the surface morphology of inkjet-printed ZnO layer. **(c)** SEM and AFM micrograph of the surface of inkjet-printed Ag as TE. **(d)** AFM micrograph of the inkjet-printed Ag as BE. **(e)** Table lists the surface roughness values R_q calculated from the AFM measurements. (a) is adapted from [137], © 2021 AIP Publishing. (b), (c), (d), and (e) are adapted from [138] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

electrodes. The sandwich-like structure of the device is illustrated with a cross-sectional schematic in Figure 4.2(d), along with an SEM micrograph, which shows the morphology and thickness of each inkjet-printed layer. The top- and bottom electrodes have a thickness of $\approx 100\,\mathrm{nm}$, and the ZnO layer is $\approx 500\,\mathrm{nm}$ thick. At the top Ag/ZnO interface, the focused ion beam cut inflicted damage, which is visible through the hole in the film and is a common effect. The undamaged top Ag electrode surface morphology can be seen in the upper part of the image, where a dense Ag nanoparticle-based thin film is observed.

The critical material properties of printed layers were characterized by X-ray diffraction (XRD), SEM, and AFM. Firstly, the structure and chemical composition of the printed ZnO were analyzed using XRD analysis. It reveals a clear transformation to zinc oxide from the zinc nitrate-based, inkjet-printed precursor.

The XRD results are shown in Figure 4.3(a), and no observable peaks, except for ZnO, are visible. The storage layer is formed in a poly-crystalline hexagonal wurtzite ZnO structure (compared with JCPDS card 36-1451). Furthermore, we investigate the inkjet-printed thin-film surface properties as shown in Figure 4.3. SEM micrographs show the dense Ag and ZnO thin-film surfaces. For surface roughness investigation, root mean square roughness (R_q) values of the Ag and ZnO layers are obtained with atomic force microscopy (AFM) in tapping mode over a scanning area of $1\,\mu\mathrm{m} \times 1\,\mu\mathrm{m}$ and the results are analyzed with an open source software Gwyddion [142]. The top and bottom electrode surfaces were compared for the Ag electrodes. The Ag BE is also subject to an annealing step, which is required to form the ZnO layer. The obtained roughness value for the Ag TE is $R_q = 22.21\,\mathrm{nm}$, the ZnO has an $R_q = 1.39\,\mathrm{nm}$, and the Ag BE surface roughness is $R_q = 15.27\,\mathrm{nm}$. The nanoparticle-based Ag thin films show an expected increased R_q when compared to the precursor-based ZnO thin film. For the Ag BE, the roughness values are reduced due to the annealing for ZnO thin-film formation, leading to Ag nanoparticles' agglomeration into bigger clusters and, hence, a denser film. The obtained value for the ZnO is comparable with reported values from dc magnetron sputtered ZnO thin-films [143]. Detailed information on all material characterization can be found in the Appendix.

4.2.2 Device Performance

Inkjet-printed AZAu and AZAg memristors resemble in terms of device structure but differ in the BE material. The selection of the BE material determines whether annealing of ZnO in an inert gas atmosphere is required (see fabrication details in Chapter 3). The device structure is symmetric or asymmetric, and the difference in the fabrication process results in two different resistive switching behavior: asymmetric AZAu devices exhibit bipolar, while symmetric AZAg devices show unipolar resistive switching. Accordingly, the figures of merit (endurance and $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio) turned out to be feasible for non-volatile memory applications. In the following, the Current-voltage $(I-V)$ characteristics and device performance,

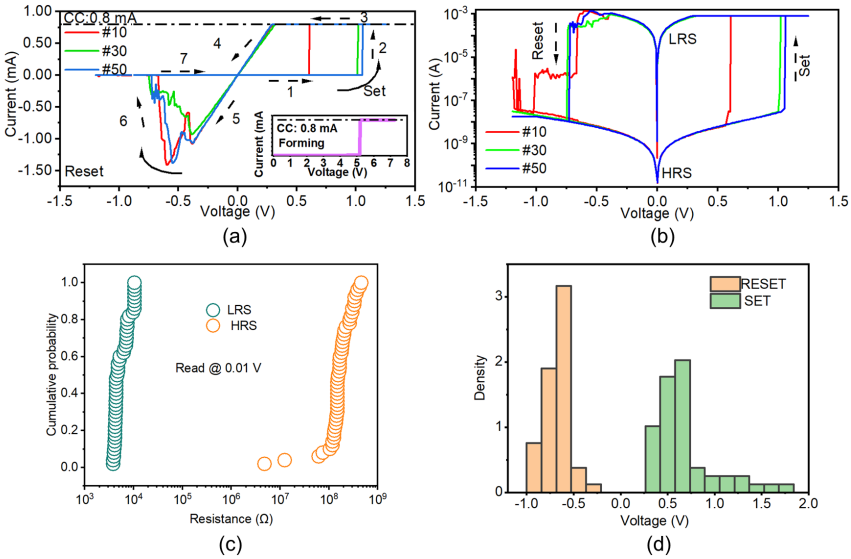


Figure 4.4: $I-V$ curves of inkjet-printed AZAu memristor. **(a)** $I-V$ curves are plotted on a linear scale showing the bipolar RS. The dashed arrows and labeled numbers depict the sequence of the sweeping. The solid, curved arrows indicate the resistive switching. A compliance current of $0.8\,\mathrm{mA}$ is set in the SET process. The small inset highlights the device-forming process. **(b)** $I-V$ curves plotted on a semi-logarithmic scale. **(c)** HRS and LRS distributions of one device over 50 RS cycles, which were measured with a read voltage pulse of $0.01\,\mathrm{V}$ after each voltage sweeping cycle in **(a)**. **(d)** SET and RESET voltage distribution analysis extracted from 50 RS cycles of **(a)**. Adapted from [137], © 2021 AIP Publishing.

including endurance, retention, $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio, and analysis on variability, are respectively presented and discussed.

Inkjet-printed Memristor: Ag/ZnO/Au

The resistive switching (RS) behavior of AZAu devices was primarily investigated by current-voltage ($I-V$) analysis, as shown in Figure 4.4(a). The quasi-static measurement was executed at a fixed sweeping rate of $0.01\,\mathrm{V/step}$. For the set process, which switches the device from a high resistive state (HRS) to a low

resistive state (LRS), the voltage was swept from $0\,\mathrm{V}$ to $1.5\,\mathrm{V}$ and back to $0\,\mathrm{V}$. For the reset process, in order to switch the device from LRS to HRS, the voltage was swept from $0\,\mathrm{V}$ to $-1.2\,\mathrm{V}$ and back to $0\,\mathrm{V}$. To prevent the memristor from breaking down, a compliance current (CC) of $0.8\,\mathrm{mA}$ was chosen to limit the maximum current during the set process. This value was selected after multiple experiments to ensure the best RS performance since the CC level could impact RS during the electrical measurements. This phenomenon was also observed and studied in literature [144]. The bias voltage was applied to the top electrode throughout $I-V$ characterization while the bottom electrode was grounded. A typical bipolar resistive switching behavior can be observed from the obtained curves since the set and reset processes were completed at opposite voltage polarities. In addition, the $I-V$ curves reveal that the RS mechanism of the investigated device is based on an electrochemical mechanism (ECM), as shown by Zhang et al. [145]. The small inset in Figure 4.4(a) depicts that the forming process is completed at around $5\,\mathrm{V}$, which is described as the first RS for a pristine device from initial HRS to LRS. For the SET process, an abrupt increase of current can be observed at $0.5\,\mathrm{V}$ for the tenth loop and at around $1\,\mathrm{V}$ for the thirtieth and fiftieth loop, which indicates a transition from HRS to LRS. The voltage at which the RS happens is labeled as the set voltage. The reduced set voltage of the tenth loop may be related to a smaller number of conductive filaments formed at the beginning. For the reset process, the device was switched back to HRS at around $-0.7\,\mathrm{V}$. The current peaks of the RESET process indicate multiple conductive filaments, which can not be ruptured at once.

The $I-V$ characteristics are plotted on a semi-logarithmic scale in Figure 4.4(b) to reveal more detail of the resistive switching. During RS, the curves exhibit steep slopes, which represent rapid set and reset processes. From the current level at the HRS and LRS, a maximum $R_{\mathrm{off}}/R_{\mathrm{off}}$ ratio of ca. 10^7 can be read at a voltage of $0.1\,\mathrm{V}$.

After the memristor was successfully set to LRS or reset back to HRS, a read voltage pulse of $0.01\,\mathrm{V}$ determined the device's resistance. The distribution of HRS and LRS over the 50 RS cycles are plotted in Figure 4.4(c) as a cumulative distribution function against two resistive states. The resistance distribution reveals that HRS shows more fluctuation than LRS. Figure 4.4(d) is the distribution

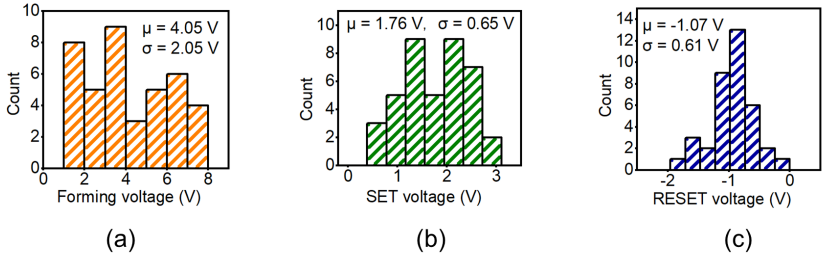


Figure 4.5: Device-to-device variability in terms of the operation voltage is analyzed by histograms of **(a)** Forming, **(b)** SET, and **(c)** RESET voltages. Data are collected from 40 devices. Adapted from [137], © 2021 AIP Publishing.

of the SET and RESET voltages within 50 RS cycles, from which a cycle-to-cycle homogeneity in terms of operation voltages is presented through the histogram. It is worth noting that the device can be set at an average value $\overline{x} = 0.68\,\mathrm{V}$ with a standard deviation $s = 0.33\,\mathrm{V}$ and be reset at an average value $\overline{x} = -0.68\,\mathrm{V}$ with $s = 0.12\,\mathrm{V}$ (Figure 4.4(d)), which is extremely competitive for low operation voltage among reported solution-processed metal oxide resistive switching devices [41].

To investigate the device-to-device variation of the inkjet-printed memristors, the Forming, SET, and RESET voltages of 40 devices were measured and visualized as histograms in Figure 4.5. The average Forming voltage is $\mu = 4.05\,\mathrm{V}$ with a standard variation $\sigma = 2.05\,\mathrm{V}$, which makes it difficult to forecast the voltage that is required to enable the first resistive switching in a pristine memristor (Figure 4.5(a)). The SET and RESET voltages are consistent once the conductive filaments exist steadily throughout the ZnO layer. The SET and RESET voltages exhibit a relatively narrow distribution. The mean values of SET and RESET voltages are respectively $1.76\,\mathrm{V}$ and $0.65\,\mathrm{V}$. The standard deviation of these two parameters resembles, respectively, in value of $0.65\,\mathrm{V}$ and $0.61\,\mathrm{V}$ (Figure 4.5(b) and (c)).

The switching endurance of the inkjet-printed memristor was investigated under pulsed voltage mode, where the device was switched between HRS and LRS in over 500 cycles. The resistance values of HRS and LRS are plotted in Figure4.6(a).

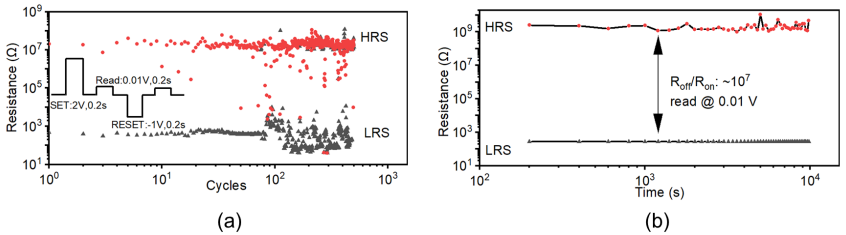


Figure 4.6: Key device performance of AZAu memristor for non-volatile memory. **(a)** Endurance of AZAu memristor under the short pulse voltage mode within 500 cycles. The small inset in (a) is the used voltage waveform. **(b)** Retention performance of both resistive states within 10^4 s. Adapted from [137], © 2021 AIP Publishing.

For the resistive state readout of the memristor, a readout voltage of $0.01\,\mathrm{V}$, which is too low to affect the conductive filaments, was employed after each RS operation. Under the pulse voltage mode (results see Figure 4.6(a)), a SET pulse of $2\,\mathrm{V}$ was applied over a duration of $0.2\,\mathrm{s}$ and the reset pulse of $-1\,\mathrm{V}$, was applied with a duration of $0.2\,\mathrm{s}$. Both voltages were applied to stimulate the device sequentially, and each voltage stimulation was followed by a resistance-read pulse voltage. The corresponding waveform is shown in the small inset of Figure 4.6(a) and was executed automatically by the semiconductor analyzer. As Figure 4.6(a) shows, within the first 100 cycles, the device can be switched reliably between HRS and LRS with a high on/off ratio exceeding 10^4. After 100 switching cycles, the window between two resistance levels is broadened by shrinking the resistance in the LRS. As a side effect, the resistive state of the device cannot be fully switched by pulse stimuli. This phenomenon is due to the increase in conduction filaments during continuous switching operations. However, it is worth noting that there is no obvious degradation of two resistive states after 500 switching cycles under pulse testing modes. This highlights the high reliability of the inkjet-printed device for memory applications.

The retention of the device in this work was also studied and is presented in Figure 4.6(b). There is no obvious tendency for the resistances of both resistive states to get close to each other within 10^4 s. No indication of degradation appears at the end of the retention test. The excellent retention performance enables the device to be a promising candidate for non-volatile memory. Besides, the very

high $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio of 10^7 was measured for the memristor used for the retention test.

Inkjet-printed Memristor: Ag/ZnO/Ag

In the case of inkjet-printed AZAg memristor, the forming process is achieved by a voltage sweep from $0\,\mathrm{V}$ to $3\,\mathrm{V}$. The observed current increases sharply and reaches the CC of $0.8\,\mathrm{mA}$ at $\approx 1.5\,\mathrm{V}$, as black curve shown in Figure 4.7(a). After the forming process, the resistive state of the device can be repeatedly switched from LRS to HRS and from HRS to LRS. After the forming process, the device is RESET and SET over 50 times by sweeping the voltage. The corresponding $I-V$ curves of the 10th, 30th, and 50th cycles are visualized in Figure 4.7(a). The SET process is achieved through a voltage sweep ($0 \rightarrow 2 \rightarrow 0\,\mathrm{V}$) with a CC of $0.8\,\mathrm{mA}$ and the $I-V$ characteristics are depicted by the red curves in Figure 4.7. For the RESET process, the voltage sweep spans over a smaller positive voltage range ($0 \rightarrow 1 \rightarrow 0\,\mathrm{V}$) without CC. The obtained $I-V$ curves for the RESET process are visualized as blue lines in Figure 4.7(a). The device exhibits a typical unipolar resistive switching behavior, where the SET and RESET processes happen with the same voltage polarity. The sudden increase and decrease of current at SET and RESET, which are observed from the $I-V$ characteristics in Figure 4.7, imply the formation and rupture of conducting filaments within the active layer of the device. The filament rupture in the RESET process is probably dominated by Joule heating[146].
The voltages extracted over 50 RESET and SET cycles are plotted in a histogram (Figure 4.7(c)). The RESET voltages exhibit a mean value of $\overline{x} = 0.38\,\mathrm{V}$ with a standard deviation of $s = 0.13\,\mathrm{V}$. The SET voltages show a mean value of $\overline{x} = 1.52\,\mathrm{V}$ with a standard deviation of $s = 0.27\,\mathrm{V}$. The distributions of the SET and RESET voltage levels indicate an overall low operation voltage and small temporal variation, which are crucial parameters for further application development. The cumulative probabilities of the device resistance at LRS and HRS, which are measured after SET and RESET using a small read voltage pulse of $0.01\,\mathrm{V}$, are plotted in Figure 4.7(d). For both resistance states, the variation

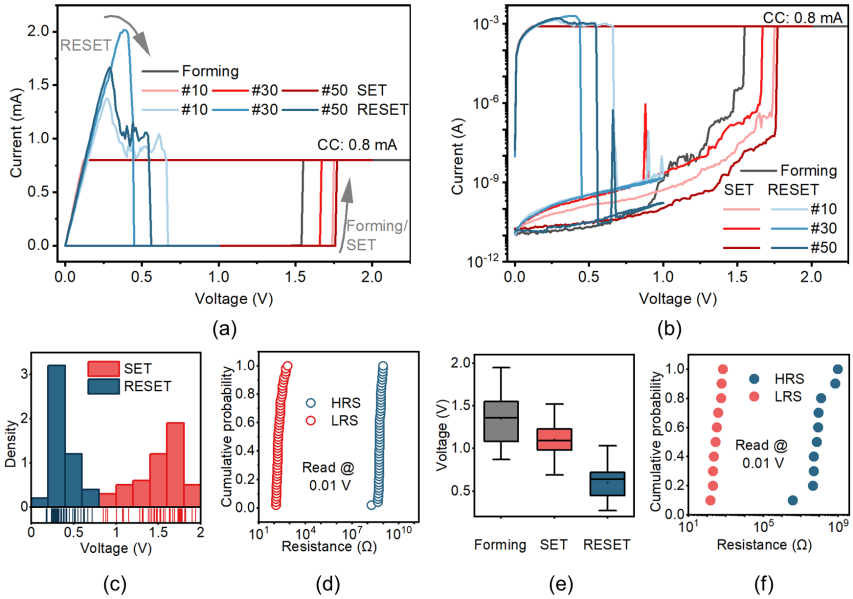


Figure 4.7: $I-V$ curves and performance variation of inkjet-printed AZAg memristors. **(a)** $I-V$ curves in the linear scale. **(b)** $I-V$ curves shown on the semi-logarithmic scale. Note: The Forming, 10th, 30th, and 50th cycles are shown. The curve of Forming is plotted with a dark-gray line. The red lines correspond to the SET processes, while the blue lines show the RESET processes. **(c)** SET and RESET voltage distribution of one device over all 50 RS cycles. **(d)** LRS and HRS distribution of one device over 50 RS cycles. **(e)** Box plot of forming, SET, and RESET voltages measured from 10 different devices. **(f)** Cumulative probability of HRS and LRS read from 10 different devices. Adapted from [138] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

over continuous cycling remains uniform and stable.

To examine the spatial variation, 10 devices from the same batch are electrically characterized under identical conditions. The voltages required for forming, SET, and RESET of 10 memristors are plotted in Figure 4.7(e) as box plot. The low forming voltage characteristics of the fully inkjet-printed memristor are shown among different devices through the small discrepancy between forming and SET voltages in Figure 4.7(e). This is an advantage in real applications since the redundant Forming process can be eliminated. The resistances of the 10 studied devices under HRS and LRS are plotted in Figure 4.7(f) in the form of cumulative

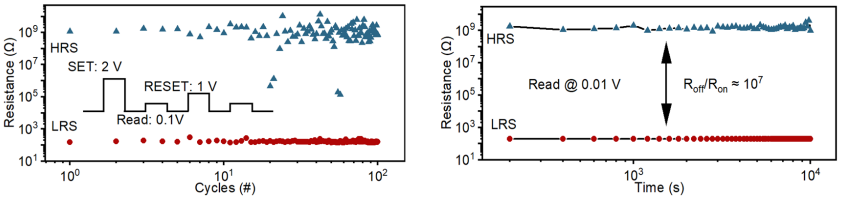


Figure 4.8: Key device performance of AZAg memristor for non-volatile memory. **(a)** Endurance performance of the device stimulated by the pulsed voltage. The inset in (a) is the pulsed voltage waveform. **(b)** Retention performance of the device at HRS and LRS over 10^4 s. Adapted from [138] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

probability over the resistance. Both LRS (at around $10^2\,\Omega$) and HRS (mostly distributed between $10^8\,\Omega$ and $10^9\,\Omega$) of different devices distributed in a narrow range proving a good device-to-device reproducibility in terms of resistive states.

To investigate the dynamic resistive switching (RS) behavior of the device, voltage pulses are applied to SET and RESET the device. The corresponding waveform is depicted in Figure 4.8(a). The pulse width used for SET and RESET is $0.2\,\mathrm{s}$. To SET the device, a $2\,\mathrm{V}$ pulse is used with a CC of $0.8\,\mathrm{mA}$. A $1\,\mathrm{V}$ pulse is applied without CC for the RESET process. After each applied voltage pulse and corresponding RS, the resistance of the memristor is read with a small voltage pulse of $0.1\,\mathrm{V}$ over $0.2\,\mathrm{s}$. The SET and RESET pulses are alternately applied to the device. The RS results are plotted in Figure 4.8(a), which show the resistance evolution of HRS (blue solid triangles) and LRS (red solid circles) after each RS cycle. The fully inkjet-printed memristor is successfully switched between HRS and LRS for $100\times$ and exhibits a large $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio of 10^7.
To investigate the retention, the device is set to a defined resistance state (LRS or HRS) and read out at one resistive state over an extended time period. For each resistive state, the resistance is read with a small voltage pulse with a width of $0.2\,\mathrm{s}$ and a height of $0.01\,\mathrm{V}$ every $200\,\mathrm{s}$ over $10^4\,\mathrm{s}$ at room temperature. Both HRS and LRS remain extremely stable over the full-time scale with a $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio of 10^7 as visualized in Figure 4.8(b). Furthermore, there is no detectable

degradation of any resistive state at the end of the measurements. This indicates the excellent retention performance of the device [36].

4.2.3 Mechanism Analysis

The two presented inkjet-printed memristors are different in device structure (Figure 4.9(a) and (d)) and operate under different modes in terms of voltage polarity. The AZAu works in bipolar RS mode, while the AZAg works in unipolar mode. Disregarding the discrepancy in the voltage polarity, both devices exhibit an abrupt binary RS behavior, a large ratio between HRS and LRS, and the non-volatility of two resistive states. The following discussion on the mechanisms of the RS behavior for each device will disclose the cause of differences and similarities in the characteristics of the two devices. Based on the criterion for designing the devices and the introduced RS mechanism widely accepted in the community (Chapter 2), both devices are postulated as filamentary type. The printed Ag TE works as Ag^+ source that ejects Ag^+ into the ZnO layer during the Forming process. The continuous redox reaction at TE and BE (Equation 2.4 and 2.5 in Chapter 2) eventually triggers the growth of Ag filaments in the ZnO matrix. The Ag filaments continuously connecting and disconnecting TE and BE are ascribed to the LRS and HRS, respectively. The conduction mechanisms of HRS and LRS are generally analyzed to prove the hypothesis. Different states of conductive filaments (CF) under HRS and LRS provide two dissimilar conduction paths for the charge carriers, which are represented by the current conduction mechanisms. To gain insight into the current conduction, the typical approach [28] is to linear fit the $I-V$ curves and compare the fitting results with the existing conduction mechanism. Here, the $I-V$ curves of the SET process in the two investigated memristors are plotted on a double-logarithmic scale, and the slopes of the manifold voltage region are extracted by linear fitting, as shown in Figure 4.9(b) and (e).

In the case of AZAu, the $I-V$ characteristics of LRS are in good agreement with Ohmic conduction, with a slope of around 1.00, which is in accordance with the work of Chiu et al. [147]. In addition, the high current level of LRS contributes

to the high conductivity, which indicates the formation of silver-conducting filaments in the ZnO layer. The conduction mechanism of LRS is illustrated by a schematic on the right side of Figure 4.9(c). In contrast to the LRS, governed by a single mechanism, the fitting results of HRS with multiple slope values can be linked to trap-controlled space charge limited conduction (TCSCLC) [72]. The conduction behavior of HRS occurs at the ZnO gap between the tip of the ruptured silver filament and the silver electrode (left side of Figure 4.9(c)); therefore, the conduction mechanism in this case is more complicated and needs to be discussed within different voltage regions. For the low voltage region, in the SET process, the $I-V$ curve follows Ohm's law, as the slope of the fitting curve is around 1.06. For this low voltage regime, the current can be attributed to the minuscule amount of the thermally excited charge carriers in the active layer [148]. Consequently, an extremely small magnitude of current compared with that of LRS can be observed in Figure 4.9(b).

As the applied voltage increases, the electrons from the metallic electrode can be injected into the ZnO layer and partially fill traps, which leads to a slight growth in the conductance, showing a larger slope of 1.77. This $I-V$ relationship is classified as trap-unfilled space charge limited conduction (SCLC), obeying Child's square law, with $I \propto V^2$, as discussed by Zhu et al. [28]. As the external electrical field is further increased, the electrons originating from the electrode fill the traps in the active layer, resulting in an exponential increase of the current with a slope of 2.94, which means a transition from trap-unfilled to trap-filled SCLC. The $I-V$ relationships of the HRS conform to the three stages of SCLC, which is summarized in [28].

In the case of AZAg devices, the obtained $I-V$ curve of one SET process is also plotted on a double-logarithmic scale in Figure 4.9(e). By applying a linear fit to the $I-V$ curves of the device at HRS, different slopes are obtained over different voltage regions, which are highlighted as blue lines with their corresponding slope values in Figure 4.9(e). The slopes increase from 1.04 over 2.07 further to 10.87 as the applied voltage at the top electrode increases from $0.1\,\mathrm{V}$ to $1.6\,\mathrm{V}$, at which the resistive switching happens. The increasing slopes over increasing voltages agree with trap-controlled space charge limited conduction. In TCSCLC, the current

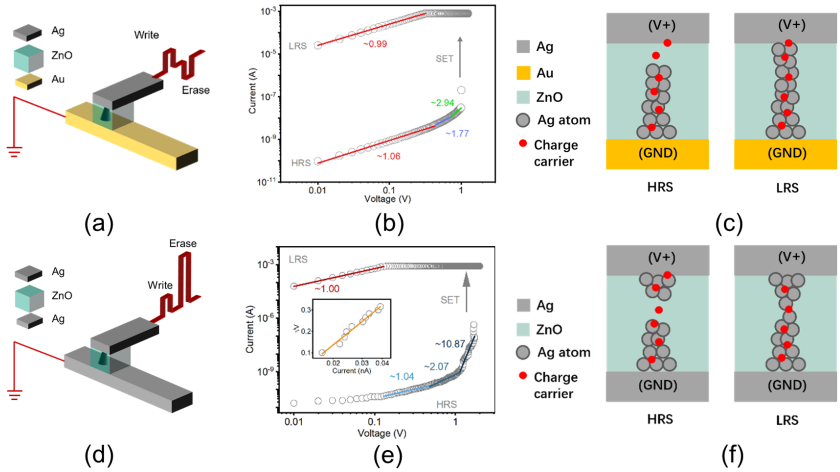


Figure 4.9: Mechanism analysis on non-volatile inkjet printed memristors. **(a)** and **(d)** Schematic of device structure and operation mode as non-volatile memory. **(b)** and **(e)** $I - V$ curve of the SET process plotted on a double logarithmic scale is analyzed by linear fitting to extract the slopes. **(c)** and **(f)** Schematics elucidate the CF states with respect to HRS and LRS, corresponding to the slope analysis in (b). AZAu memristors: (a), (b), and (c). AZAg memristor: (d), (e), and (f). (b) is adapted from [137], © 2021 AIP Publishing. (e) and (f) are adapted from [138] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

conduction behaves in three different ways when subjected to different voltage regions. For TCSCLC, in the low voltage region, Ohmic conduction occurs, where $I \propto V$. At medium voltage levels, the trap-unfilled SCLC corresponds to Child's square law, with $I \propto V^2$. When further increasing the voltage, the conduction is related to the trap-filled SCLC, with a current proportional to a voltage of higher exponent ($I \propto V^n$, with $n \geq 2$) [28]. This matches with the reported slopes as shown in Figure 4.9(e).

However, compared to the case of AZAu, the observed $I - V$ characteristics of AZAg in HRS at a very low voltage of $< 0.1\,\mathrm{V}$ do not correlate with TCSCLC. Therefore, the conduction mechanism in this region needs to be discussed separately. As the inset in Figure 4.9(e) depicts, the current-voltage dependence shows a good linear fit when plotting $\sqrt{V}$ over the logarithmic current, which indicates Schottky emission between the metal and metal oxide layer [149]. The Schottky

emission, which occurs at a low electrical field in the device, can be attributed to a small Schottky barrier, which is formed between the tip of Ag conducting filaments and the ZnO active layer. The transition of the conductance mechanism in HRS is explained in the cross-sectional schematic of the device at HRS in Figure 4.9(f). Here, the conducting Ag filaments in the ZnO layer are ruptured when the device is in HRS. As the applied voltage at the top electrode increases gradually, the thermally activated charge carriers from the tip of the Ag CF will be activated over the Schottky barrier, which is formed between the Ag CF and ZnO. This allows electrons to enter the conduction band of ZnO, which results in Schottky emission-like conduction behavior in the very low voltage region of the device. However, due to the unknown distance between both parts of the CF within the ZnO layer, the electric field cannot be predicted properly. As the applied voltage increases, the free charge carriers in ZnO are activated, which leads to Ohmic conduction. With a continuous increase of the applied voltage, more charge carriers are injected into the ZnO layer from the tip of the Ag CF, which partly fills the traps in the ZnO thin film. At this stage, the conduction behavior obeys Child's law. When the voltage at the top electrode is further increased, more charge carriers, which originate from the Ag CF, continuously fill the traps in the ZnO and lead to an exponential increase in the current, respectively.
At the LRS, a highly conductive Ag-based path in the ZnO layer, which bridges the top and bottom electrodes (right schematic in Figure 4.9(f)), is formed. In this case, the device is supposed to exhibit Ohmic conduction with a high conductivity. This behavior is well reflected in our fully inkjet-printed memristor with a slope of 1.00, as shown in Figure 4.9(e).
The above discussion on the RS mechanism reveals that the binary digital-type RS phenomena observed in inkjet-printed AZAu and AZAg memristors are attributed to the formation and rupture of the Ag filaments. Since the Ag-related electrochemical reactions are the main cause of manipulating the states of the Ag filaments, both devices are classified into electrochemical mechanism (ECM) type memristors in a broad sense. However, these two devices show a couple of dissimilar characteristics: (a) The asymmetric AZAu memristors show bipolar RS, while the symmetric AZAg memristors work in unipolar mode. (b) AZAu memristors have a moderated $R_{\mathrm{off}}/R_{\mathrm{on}}$ of 10^4 but show a larger number of RS

cycles (500). In contrast, a large $R_{\mathrm{off}}/R_{\mathrm{on}}$ comes out from AZAg memristors, and both HRS and LRS exhibit excellent uniformity. However, the uniform RS of a large memory window in AZAg devices is compromised by a reduced operating cycle (100). (c) AZAg memristors are electroformed at a low voltage of ca. $1.4\,\mathrm{V}$, which is close to the SET voltage of ca. $1.2\,\mathrm{V}$. In the case of the AZAu, a Forming process above $4\,\mathrm{V}$ is indispensable prior to the regular RS.

The answer to the dissimilar characteristics of these two devices can be found in the comparison of the way the Ag CF connects and ruptures during the RS. As sketched in Figure 4.9(c) and (f), the RS in the AZAu device is postulated to occur between the TE and the residual Ag CF remaining from the RESET. This is because the Ag^+ ejected from the TE is reduced at the Au BE, leading to the growth of the CF towards the TE. In this case, the CF adjacent to the TE is the weakest part and is vulnerable to rupture when reversing the voltage's polarity. Electrochemical reactions dominate the RESET process. Reflected in the RS, the AZAu devices show bipolar mode since the resistance transition in these devices relies on voltage-polarity-dependent redox reactions. When the BE is replaced by an inkjet-printed Ag electrode, the Ag from the BE can diffuse into the ZnO layer during the thermal annealing. This process will pre-incorporate Ag in the ZnO, which facilitates the process of forming the CF in a pristine device. This might be the reason for the low-forming voltage phenomena in AZAg devices. Similar strategies are reported in developing and forming free VCM memristors by generating oxygen vacancies in the active layer during the fabrication [38]. The size of the CF in the ECM device is correlated to the Forming process. An easier Forming process (e.g., lower voltage or CC) produces generally smaller CF with respect to the diameter [70]. Back to the case of the AZAg memristor, a smaller CF is formed under a lower Forming voltage, which is prone to rupture in the middle caused by Joule heating. The RS is postulated to happen between the two tips of the residual Ag CF in the ZnO. The thinner CF in AZAg devices contributes to the large $R_{\mathrm{off}}/R_{\mathrm{on}}$ but also confronts the problem of permanent breakdown. As introduced in Chapter 2, AZAg devices can be more specifically categorized into TCM memristors, in which the rupture of the CF relies more on Joule heating during RESET.

4.3 Inkjet-printed Memristors Based on Metal Oxide Nanoparticle Inks

The results in this section were also reported in [139].

The two aforementioned inkjet-printed memristors show excellent performance in terms of application for non-volatile memory in PE. However, the metal salt-based precursor ink requires a thermal annealing treatment of $400\,^{\circ}\mathrm{C}$. This thermal process has denied the chance to apply the devices to a large variety of polymer substrates, which are the main class of materials used as substrates in flexible electronics. To weaken the dependency of printed memristive technology on the materials of the substrates, one straightforward strategy is to use nanoparticulate dispersion ink to deposit the active layer. In the following, a nanoparticulate WO_{3-x} dispersion ink is used to replace the zinc nitrate precursor ink in AZAu devices, and a new memristive device with a structure of Ag/WO_{3-x}/Au (named AWAu) was developed under a lower temperature (max. $120\,^{\circ}\mathrm{C}$). The details of the device structure, material characterization, and electrical performance are presented in this section.

4.3.1 Device Structure

AWAu memristor is based on a three-material stack consisting of a laser-patterned gold (Au) bottom electrode, an inkjet-printed tungsten oxide (WO_{3-x}) active layer, and an inkjet-printed silver (Ag) top electrode. As shown in Figure 4.10(a), the effective area of the device is formed at the intersection of the two overlapping electrodes and is therefore defined by the overlapping area of the upper Ag top electrode (ca. $50\,\mu\mathrm{m}$ in width) and the lower Au electrode ($30\,\mu\mathrm{m}$ in width). The microscopic morphology of a pristine device is visualized in the cross-section depicted in the inset of Figure 4.10a with a high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM), from which the thickness of each layer can be approximated (Au bottom electrode has a thickness of $100\,\mathrm{nm}$,

inkjet-printed WO_{3-x} active layer with a thickness of ca. $600\,\mathrm{nm}$ and an inkjet-printed Ag top electrode of ca. $70\,\mathrm{nm}$). The elemental distribution of each layer is revealed by energy-dispersive X-ray spectroscopy (EDS) over the red highlighted area, in which Ag, W, and Au are clearly traced in the corresponding layers. The Pt layer above the Ag top electrode protects the device structure during the lamella preparation.
Furthermore, the surface roughness of the inkjet-printed WO_{3-x} active layer was investigated by atomic force microscopy (AFM) over an area of $1\,\mu\mathrm{m} \times 1\,\mu\mathrm{m}$. The AFM micrographs shown in Figure 4.10(b) reveal that the surface morphology of WO_{3-x} layer consists of granular nanoparticles. The root mean square surface roughness is $R_q = 28.90\,\mathrm{nm}$.
To reveal the crystal phase composition of the inkjet-printed tungsten oxide, the films were investigated with X-ray diffraction (XRD). From the obtained spectrum in Figure 4.10(c), a good agreement of the peaks in the measured XRD pattern with the data of the calculated WO_{3-x} (ICSD84139) at the 2θ positions of $18.1°$ (002), $18.9°$ (110), $22.1°$ ($10\overline{2}$), $22.7°$ (012), and $26.0°$ ($11\overline{2}$) can be seen. The (110) and ($10\overline{2}$) planes of the WO_{3-x} crystalline can be clearly seen in the high-resolution transmission electron microscopic (HRTEM) image in Figure 4.10(d) with a lattice spacing of $3.65\,\text{Å}$ and $3.14\,\text{Å}$, respectively. The micromorphology of the inkjet-printed WO_{3-x} is presented in Figure 4.10(e) from the top-view with SEM. Figure 4.10(f) is an SEM micrograph of the top-view of the inkjet-printed nanoparticulate Ag, in which the spherical Ag particles of ca. $30\,\mathrm{nm}$ - $50\,\mathrm{nm}$ in diameter are clearly shown. Detailed information on material characterization methods is described in the Appendix.

4.3.2 Device Performance

The Forming process of AWAu memristor was performed through an initial voltage sweep $(0\,\mathrm{V} \rightarrow 5\,\mathrm{V})$, to build the initial conducting filaments within the WO_{3-x} layer (Figure 4.11(a)). At $4\,\mathrm{V}$, the measured current abruptly reaches the CC of $0.8\,\mathrm{mA}$, which indicates the initial electroforming voltage of AWAu memristor. After the initial electroforming process, the device is switched between its LRS

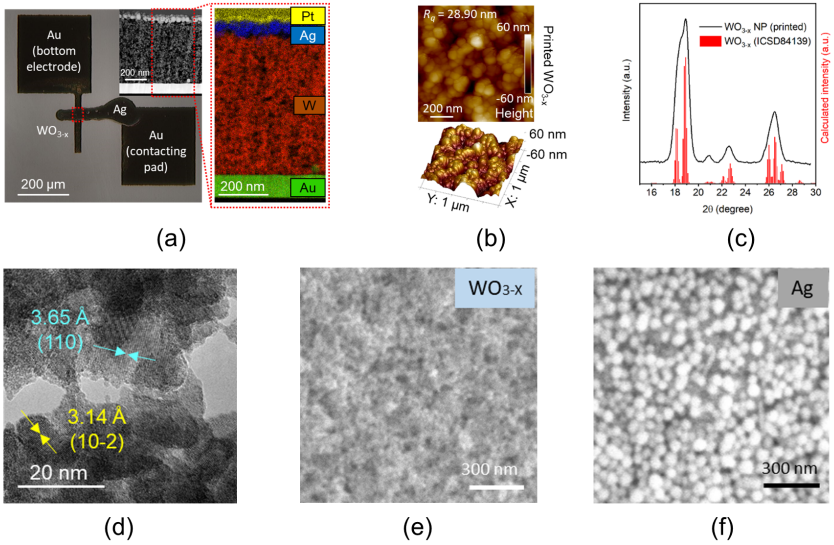


Figure 4.10: Device structure and material characterization of inkjet-printed memristor based on nanoparticle dispersion ink. **(a)** Optical image of the inkjet-printed AWAu memristor from a top view. The effective area of the device is formed at the overlapping area of the top and bottom- electrodes, which is marked with a red dashed rectangle with a size of $50\,\mu\text{m} \times 30\,\mu\text{m}$. Inset: cross-sectional STEM HAADF micrograph of the inkjet-printed AWAu memristor. An EDS elemental map of the selected area in STEM is shown in the zoom-in box. **(b)** 2D and 3D AFM image of the inkjet-printed WO_{3-x} layer. **(c)** XRD pattern of WO_{3-x}, inkjet-printed on Si wafer. For comparison, the calculated intensity of WO_{3-x} (ICSD84139) is plotted as red columns over 2θ. **(d)** HRTEM image of WO_{3-x} layer. The planes indicated by the arrows are assigned to WO_{3-x}. **(e)** Top view SEM image of the nanoparticle-based WO_{3-x} layer. **(f)** Top view SEM image of the nanoparticle-based Ag top electrode. Adapted from [139] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

and HRS by consecutive positive and negative voltage sweeps. It is noted that the SET voltage is much lower than the initial electroforming voltage due to the residual conducting filaments, which were previously formed in the WO_{3-x} layer. For the SET process, a voltage sweep $(0\,\mathrm{V} \rightarrow 2\,\mathrm{V} \rightarrow 0\,\mathrm{V})$, is applied over the device, with a CC of $0.8\,\mathrm{mV}$. To RESET the memristor, a voltage sweep $(0\,\mathrm{V} \rightarrow -1\,\mathrm{V} \rightarrow 0\,\mathrm{V})$ without CC is used. Figure 4.11(a) and Figure 4.11(b) show 11 representative *I-V* curves from 100 consecutive sweeping cycles. Based on the $I - V$ characteristics and the material stack of the AWAu memristor, the underlying RS mechanism is ascribed to filamentary ECM, similar to that of the AZAu device discussed earlier in this chapter.

For cycle-to-cycle device investigation, the distributions of the obtained 100 SET and RESET voltages are depicted as histograms in Figure 4.11(c). The obtained memristor SET voltage shows a low mean value of $\overline{x} = 1.05\,\mathrm{V}$, with a standard deviation of $s = 0.29\,\mathrm{V}$. The RESET voltage is centered around a mean value of $\overline{x} = -0.45\,\mathrm{V}$ with a standard deviation of $s = 0.11\,\mathrm{V}$. The resistance value of the device after each SET and RESET voltage sweeping cycle was measured by a voltage pulse of $0.1\,\mathrm{V}$. To analyze the cycle-to-cycle variations in terms of the LRS and HRS, the measured resistance values are plotted together with the cumulative probability in Figure 4.11. HRS shows a slightly wider distribution range than LRS, while SET to LRS failed occasionally over the 100 RS cycles (the outlier green circles). Nevertheless, a minimum $R_{\mathrm{off}}/R_{\mathrm{on}}$ of over 10 was guaranteed over the RS cycles, which is regarded as an adequate metric for read operation in non-volatile memory.

To investigate the performance of the memristor as a non-volatile memory device, voltage pulses are applied to the device for $200\,\mathrm{ms}$ to switch between the resistive states. For the "write" operation, which sets the device to LRS, a voltage pulse of $3\,\mathrm{V}$ and a CC of $0.8\,\mathrm{mA}$ is used, while a voltage pulse of $-1.5\,\mathrm{V}$ is used for the "erase" operation, which resets the device to HRS, without the need for CC. After each "write" and "erase" cycle, the resistance is read out through a small voltage pulse of $0.01\,\mathrm{V}$. Figure 4.12(a) shows the results after "writing" (blue dots) and "erasing" (red dots) the device over 12672 cycles. Only a few switching events fail, and a resistance $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio of 10^2 is obtained. In Figure 4.12(a), the endurance cycle-to-cycle variability of the HRS and LRS is

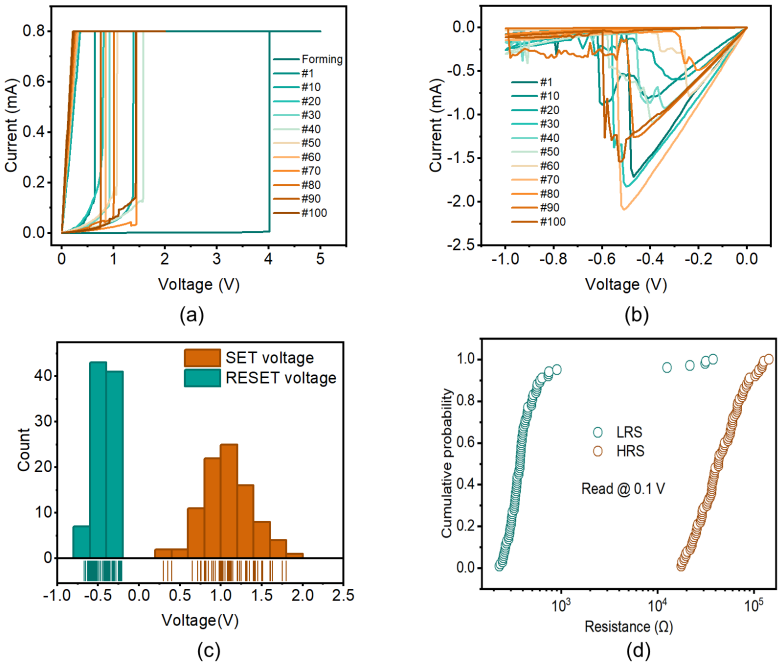


Figure 4.11: $I-V$ curves and performance variation of inkjet-printed AWAu memristors. **(a)** $I-V$ curves of the electroforming voltage sweep and 11 SET processes (out of 100) with a compliance current of $0.8\,\mathrm{mA}$. **(b)** $I-V$ curves of 11 RESET processes. **(c)** Distribution of SET and RESET voltage values extracted over 100 switching cycles, visualized as histograms. **(d)** LRS and HRS distribution of one device over 100 RS cycles. The read voltage was $0.1\,\mathrm{V}$. Adapted from [139] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

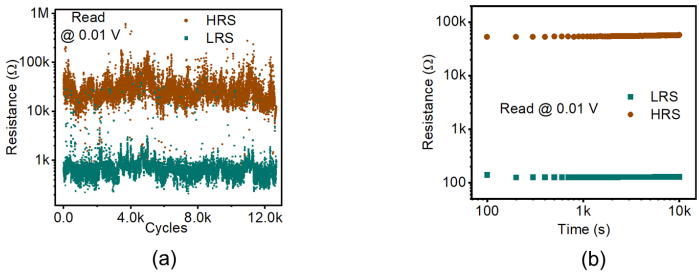


Figure 4.12: Key device performance of AWAu memristor for non-volatile memory. **(a)** Endurance performance of the device stimulated by the pulsed voltage. **(b)** Retention performance of the device at HRS and LRS over 10^4 s. Adapted from [139] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

observable, which is a common effect in ECM-based memristors due to their intrinsic stochastic properties [59]. If necessary, the endurance uniformity can be optimized by suitable circuit architectures, such as 1-transistor 1-memristor (1T1R) and feedback algorithms with adaptive current compliance measures [150, 151].

To investigate the retention performance of the device, the resistances of both resistive states are plotted in Figure 4.12(b) over 10^4 s. Therefore, the device is set to a defined resistive state (HRS or LRS), and its resistive state is continuously obtained by a read voltage, with a pulse height of 0.01 V and width of 200 ms. As visualized, both resistive states remain stable over the investigated time, and no signs of obvious degradation can be observed. The retention performance of the device further highlights its potential as a non-volatile memory element.

4.4 Conclusion

In this chapter, three types of inkjet-printed memristors of different material stacks were presented, including Ag/ZnO/Au, Ag/ZnO/Ag, and Ag/WO_{3-x}/Au. The devices were systematically characterized from a material and electrical perspective. Accordingly, resistive switching mechanisms are postulated based on an analysis of current conductions concerning HRS and LRS. Here, an overall conclusion is

drawn based on the above discussions.
Ag was selected as the TE for all printed memristive cells due to its chemical stability during the printing and the high migration speed of its ionic state in metal oxides. These two features render Ag an ideal material for active electrodes in printed cation-based resistive switching devices. The resistive switching behavior is attributed to the formation and rupture of the Ag conducting filaments. The three printed memristors presented in this chapter exhibit similar digital-type resistive switching. The distinct conducting mechanism of LRS and HRS indicates two different current pathways under these two resistive states. The results of the analysis of the resistive switching mechanism in the three printed memristors having Ag TE are in good accordance with the widely accepted ECM theory. The Ag filaments formed under a proper CC of $0.8\,\mathrm{mA}$ are regarded to account for the non-volatile resistive switching behavior in the printed memristor ($10^4\,\mathrm{s}$).
However, these three printed ECM devices exhibit different performance measures, mainly ascribed to the distinct material properties of the active layer. For the comparison between AZAu and AZAg pairs, although the active layer materials are both ZnO, the different materials selections on BE, e.g., Au and Ag, determined the distinct thermal sintering process of the zinc nitrate precursor ink. The printed Ag BE is assumed to diffuse into the ZnO layer during the thermal sintering process, which is analogous to doping ZnO with Ag during fabrication. Consequently, the symmetric AZAg devices show unipolar resistive switching and an almost forming free property. On the contrary, the asymmetric AZAu devices exhibit bipolar resistive switching, and an electroforming process is required. These different characteristics are also reflected in the endurance and the $R_{\mathrm{on}}/R_{\mathrm{off}}$ ratio measured under dynamic pulsed voltage mode. The AZAu has more cycle number (500) but with a smaller memory window (10^4), while AZAg has the biggest $R_{\mathrm{on}}/R_{\mathrm{off}}$ of 10^7 and is vulnerable to being stuck in HRS during the endurance test (100 cycles were measured). The Ag doping induced by the sintering of ZnO is postulated as the cause of the tradeoff between memory window and endurance observed in the two different device types. This required further advanced materials characterization in future studies.

The bandgap of the active layer material is the other factor that can determine the device performance, in particular, the $R_{\mathrm{on}}/R_{\mathrm{off}}$ and the endurance. The AWAu devices show a smaller memory window of 10^2, about three orders of magnitude less than the AZAu device. These two device types have the same electrode materials but differ in the active layer. ZnO has a larger bandgap ($3.3\,\mathrm{eV}$) than WO_{3-x} ($2.1\,\mathrm{eV}$), which renders HRS of ZnO devices a higher resistance. The higher resistance level of HRS determines the larger memory window since the two types of devices exhibit similar LRS. However, the tradeoff between memory window and endurance appears again. The best endurance cycle of 12672 was measured from the smaller $R_{\mathrm{on}}/R_{\mathrm{off}}$ AWAu device. The endurance cycle number of the AWAu device is also the highest among all reported printed digital-type memristors, as shown in Table 4.2. The tradeoff between memory window and endurance is a common phenomenon for memristive technology [36, 59]. This implies the direction of future memristive device engineering for non-volatile memory: excellent endurance and a large memory window within one device.

Table 4.2: Performance comparison of digital-type memristors for non-volatile memory. Comparison between presented devices in this thesis and other printed memristors. Abbreviations used: Electrohydrodynamic = "EHD", Absence of parameter = "-". $^{+}$ Endurance reported through $I-V$ sweeping. Cross-point = "CP", common-bottom = "CB" device architecture. Adapted from [139] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

Material stack	Printing method	Device architecture	Device area	Max. processing temperature ($^{\circ}$C)	$R_{\mathrm{off}}/R_{\mathrm{on}}$	Retention (s)	Endurance (Pulse cycles)	Reference	Year
Ag/$ZnSnO_3$/ITO	EHD jet	CB	$2\,\mathrm{mm} \times 100\,\mu\mathrm{m}$	130	300	1.2×10^4	200^{+}	[152]	2016
Ag/PMMA+MEH:PPV/Ag	EHD+Screen printing	CP	$200\,\mu\mathrm{m} \times 200\,\mu\mathrm{m}$	120	5	-	45^{+}	[153]	2017
Ag/HfO_2/Au	Inkjet	CB	$320\,\mu\mathrm{m} \times 320\,\mu\mathrm{m}$	240	10^3	-	128^{+}	[154]	2017
Ag/SOG/PEDOT:PSS	Inkjet	CP	$100\,\mu\mathrm{m} \times 100\,\mu\mathrm{m}$	425	10^4	1.6×10^4	1000^{+}	[155]	2017
Ag/HfO_2/Pt	Inkjet	CB	$320\,\mu\mathrm{m} \times 320\,\mu\mathrm{m}$	240	10^9	-	450^{+}	[156]	2019
Ag/WSe_2/Ag	Aerosol jet	CP	$70\,\mu\mathrm{m} \times 70\,\mu\mathrm{m}$	150	10^3	$< 10^4$	90^{+}	[157]	2019
Ag/Graphene+V_2O_5/Ag	Inkjet	CP	$40\,\mu\mathrm{m} \times 40\,\mu\mathrm{m}$	150	10^9	-	1300	[158]	2019
Ag/WSe_2/Ag	Aerosol jet	CP	$70\,\mu\mathrm{m} \times 70\,\mu\mathrm{m}$	Room temperature	10^2	-	-	[159]	2020
Ag/AlO_x/ITO	Inkjet	CB	$250\,\mu\mathrm{m} \times 250\,\mu\mathrm{m}$	150	40	10^5	100^{+}	[160]	2021
Al/BFO/FTO	Inkjet	CB	$200\,\mu\mathrm{m}$ (Diameter)	550	4	-	90	[161]	2021
PEDOT:PSS/WO_3/PEDOT:PSS	Inkjet	CP	$200\,\mu\mathrm{m}$	60	5	8×10^4	6000	[162]	2021
Ag/Cr-N-doped TiO_2/Ag	EHD jet	CP	-	110	2.5×10^3	5×10^3	500^{+}	[163]	2022
PEDOT:PSS/ZnO/PEDOT:PSS	Inkjet	CP	$200\,\mu\mathrm{m} \times 200\,\mu\mathrm{m}$	80	5	10^5	10^4	[164]	2022
Ag/ZnO/Au	Inkjet	CP	$50\,\mu\mathrm{m} \times 50\,\mu\mathrm{m}$	400	10^7	10^4	500	**In this thesis** [137]	2021
Ag/ZnO/Ag	Inkjet	CP	$150\,\mu\mathrm{m} \times 150\,\mu\mathrm{m}$	400	10^7	10^4	100	**In this thesis** [138]	2023
Ag/WO_{3-x}/Au	Inkjet	CP	$50\,\mu\mathrm{m} \times 30\,\mu\mathrm{m}$	120	10^2	10^4	12,672	**In this thesis** [139]	2023

5 Printed Memristors for Neuromorphic Computing

5.1 Introduction to Neuromorphic Computing in Printed Electronics

The goal of printed electronics is not to replace state-of-the-art silicon CMOS electronics but rather to complement it in some applications, such as large-scale applications (e.g., sensing or display), flexible substrate (e.g., wearable electronics for health monitoring), or disposable products (e.g., smart packaging) [4], to name a few. The Internet of Things (IoT) connects daily devices to ease humans' lives in certain areas [165]. The core computing tasks will be centrally performed by high-performance Si-based electronics devices, while the aforementioned PE-based devices are placed at the edge node where they are directly in contact with the physical world. Massive data are generated by the real physical world. Thus, the PE-based systems at the edge node are expected to process the in-time data quickly and to make rational decisions on the data that is significant to be sent to the central processing units. In this regard, the PE-based system is expected to process and store the data [165]. However, as discussed earlier, the information processing and storage units in a PE system rely on thinned Si-based chips, where a transition solution for a PE-based system is carried out, termed hybrid printed electronics (HPE).

To achieve a fully printed electronics system serving at the edge node in IoT, tremendous efforts have been put into developing printed devices for information storage and processing. For printed memory, as discussed in the previous chapter, memristive devices emerge as non-volatile memory. For information processing

units, conventional computing architecture based on Boolean logic may confront multiple challenges posed by printed electronics: (a) in the conventional von Neumann architecture, the processing unit and memory unit are separated. Therefore, data is frequently transported between these two units [28], which results in massive power consumption and eventually imposes technical issues on the power supply unit and related auxiliary circuitry in the PE system. (b) The cornerstone devices for the printed Boolean logic, the printed transistors, are suffering from moderated performance [10]. The printed transistors are either slow in switching speed (electrolyte-gated field effect transistors) or require high operation voltage (FET with dielectric gating materials). These limited performances render printed transistor-based Boolean logic unable to process massive in-time data generated at the edge. Even for mature and high-performance Si-based processors, novel computing paradigms are sought to process massive parallel data in a more efficient manner. These challenges imply that the conventional computing paradigm is not the optimal solution for information processing in a fully printed electronic system.

In fact, our brain is a biological computer that is proficient in performing specific computing tasks, including unstructured data classification and pattern classification, in a more energy-efficient manner compared to conventional central process units (CPU). This is because the human brain processes data parallelly while computing tasks are sequentially performed in a conventional CPU [30]. Moreover, self-learning is another unique human brain advantage, enabling the biological processor to perform similar tasks with growing speed but reducing power consumption [165]. This highly efficient intelligent system has inspired enormous research in developing novel computing paradigms by mimicking the human brain, which is referred to as neuromorphic computing [28, 29, 30]. The new information processing paradigm will also advance the development of printed information processing units. The properties, including but not limited to low-power consumption, parallel information processing, and self-learning, will have advantages for printed processors that must work with the limited conditions of a PE system. Moreover, the ability of analog computing of a neuromorphic network enables the PE device at the edge to direct interface with analog signals, which can further alleviate the difficulties in achieving a full PE system by eliminating

analog-to-digital or digital-to-analog (ADC/DAC) converters [166]. Therefore, solution-processed neuromorphic devices and networks have attracted significant attention in the research [31, 32, 33]

The human brain is a biological network composed of 10^{11} neurons and 10^{15} synapses [167]. Neurons are a class of cells consisting of dendrites, somas, and axons that handle information processing. A synapse is a connection between two neurons that transmit and integrate signals between neurons; in addition, synapses are also regarded as the main elements participating in memorizing and learning, which are achieved by modifying their connection strength. The tunable strength of a synapse is also termed plasticity [30]. The main idea of neuromorphic computing is to mimic neuronal behavior and synaptic plasticity. In the early stage of the research in neuromorphic computing, neuronal behavior and synaptic plasticity are emulated by the algorithm, which is eventually implemented with traditional integrated circuits based on CMOS technology [168]. Although artificial neurons and synapses have been functionally achieved through conventional CMOS technology, the computing efficiency and structure simplicity are still incomparable to that of the real neuronal network. To mimic the signal accumulation of a neuron with CMOS, a digital adder and accumulator are required [169]. For CMOS implementation of weight update in a synapse, the memory unit is frequently accessed and refreshed with updated weights [28]. This requires a high power consumption, and redundant circuitry is needed when implementing artificial neuronal networks with CMOS; in this regard, novel electronic devices are emerging to implement artificial neurons and synapses more energy-efficiently with fewer devices. Since a neuromorphic system is able to perform memory and calculation simultaneously, most of the neuromorphic devices have evolved from memory devices, such as PCM, FeRAM, MRAM, Flash, and ReRAM [28].

Memristor is cutting-edge research among all other novel neuromorphic devices. The memristors possess several unique advantages that are naturally ideal for the implementation of neuromorphic devices, including: (a) The mechanisms of resistance change in most memristors are attributed to ion migration. This resembles Ca^{+} flow between the neurons that are regarded as the fundamental neuronal behavior [166]. The two terminal structures of memristors are similar to the appearance of biological synapses and neurons. These two features render

memristors able to emulate both neurons and synapses. In the implementation of an artificial neuron, the TE and BE can be assigned as dendrite and axon (or vice versa), and the active layer can play the role of the cell body [30]. In the case of emulating a biological synapse, the TE and the BE are regarded as pre- and postsynaptic neurons, and the active layer works as the synaptic cleft where the plasticity is represented [30]. In addition, the realization of a complete memristive artificial neuromorphic system is a crossbar involving a memristor at each node. This format highly resembles the structure of the human cortex neural networks [30]. (b) When implementing a neuromorphic system with a memristive crossbar, the current sensing can be done simultaneously, disregarding the crossbar's size. This property exhibits huge potential in parallel computing [166]. Considering the advantages of memristive devices among the other novel memory devices in terms of technical realization with printing technologies, as discussed earlier in the chapter on printed non-volatile memory, this class of two-terminal resistive devices is regarded as one of the most feasible solutions for printed neuromorphic system and has attracted interests from the PE community [31, 32, 33]. In the following sections, the inkjet-printed AWAu memristor is introduced to implement multiple synaptical behavior, including paired-pulse facilitation (PPF), short-term plasticity, metaplasticity, as well as information integration and filtering ability.

5.2 Analog Resistive Switching Devices and Their Characteristics

The results in this section were also reported in [139].

The inkjet-printed Ag/WO_{3-x}/Au memristor can operate either in digital or analog resistive switching mode, depending on the activation procedure. In the case of emulating synaptic behavior, analog resistive switching is employed. To enable analog resistive switching, no electroforming is required over a pristine device, and only negative voltages are applied to the device (Figure 5.1). Applying a

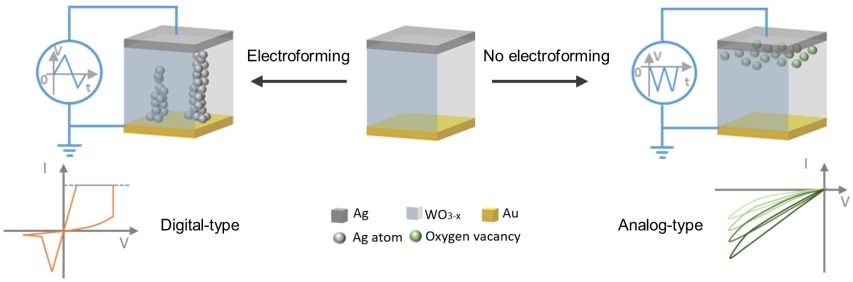


Figure 5.1: Schematics of two resistive switching behavior in inkjet-printed AWAu memristor. The functionality is based on applying or not applying a prior electroforming voltage to a pristine device. A positive electroforming voltage sweep is applied to obtain a digital-type memristor. This leads to the formation of silver conducting filaments in the WO_{3-x} layer. If the device is intended to be used as an analog-type memristor, no electroforming voltage is applied to the pristine device, and only negative voltages are used to modulate the oxygen vacancies at the Ag/WO_{3-x} interface. Adapted from [139] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

negative voltage to the Ag-based top electrode leads to the accumulation of oxygen vacancies (V_o) at the Ag/WO_{3-x} interface (Figure 5.1). The accumulated V_o is used to modulate the height of the Schottky barrier and gradually change the conductivity of the device as shown in Figure 5.1. To exploit the interface-based, analog resistive switching of the device, no initial electroforming voltage and only negative voltage sweeps and pulses are used to avoid Ag filament formation within the active layer. The gradual increase in conductivity of the memristor is shown in Figure 5.2(a), by applying five consecutive negative voltage sweeps ($0\,V \rightarrow -3\,V \rightarrow 0\,V$).

To visualize the dynamic incremental conductivity change with multiple successive negative voltage sweeps, the voltage and current are plotted over time in Figure 5.2(b). The peaks observed in the current measurements increase steadily with each voltage spike, which is similar to the increase in efficacy of a biological synapse exposed to a continuous stimulus. This analog resistive switching can be exploited to develop artificial memristive synapses [170].

The gradual increase in conductivity of the inkjet-printed memristor is due to the continuous accumulation of oxygen vacancies at the Ag/WO_{3-x} interface, as tungsten oxide is an n-type transition metal oxide-based semiconductor, where

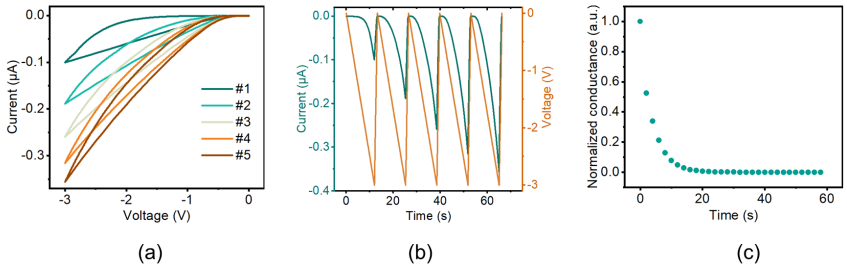


Figure 5.2: Analog resistive switching characteristics. **(a)** $I-V$ curves of five consecutive DC voltage sweeps following the protocol of $0 \rightarrow 3 \rightarrow 0\,\mathrm{V}$. A gradual increase in conductivity is shown. **(b)** Plot of voltage and measured current over time. **(c)** Exponential decay of the device's normalized conductance over time, measured after the fifth voltage sweep. This indicates the volatility of the conductance when the applied voltage is removed. Adapted from [139] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

V_o act as a dopant that increases the overall conductivity. The metal/semiconductor interface properties can be dynamically adjusted by changing the number of oxygen or V_o [38, 99, 100, 171, 172]. Therefore, gradually tunable resistive switching can be achieved by applying an external electrical field to the device, which helps to manipulate the amounts of V_o in the tungsten oxide.

For the analog-type memristor, the conductance decreases over time due to the volatility of the migrated oxygen vacancies. As shown in Figure 5.2(c), an exponential decay of the normalized conductance is observed after the device experienced 5 consecutive voltage sweeps. This can be attributed to the restoration of the Schottky-like contact at the Ag/WO_{3-x} interface, caused by spontaneous diffusion of the oxygen vacancies away from the metal/semiconductor interface. This conductance decay also explains the overlapping hysteresis loops in Figure 5.2(a). The phenomenon of volatile resistive switching in the reported inkjet-printed memristor can be used to emulate synaptic plasticity, which refers to the modification of the strength of synaptic transmission between two neurons [173].

5.3 Analysis of Working Mechanism

The results in this section were also reported in [139].

The following experiments were performed to study the mechanism leading to the memristor's volatile analog resistive switching behavior. Firstly, a DC voltage sweep from $-1\,\mathrm{V}$ to $1\,\mathrm{V}$ is employed to disclose the interface properties of the two metal/semiconductor interfaces in the pristine device, i.e., Ag/WO_{3-X} and WO_{3-X}/Au. The voltage sweep was added to the top electrode while the bottom electrode was grounded. The non-linear $I-V$ curve of the pristine device with current rectification is shown in Figure 5.3(a) as a green line, which indicates a Schottky contact at the Ag/WO_{3-X} interface while an Ohmic contact at the WO_{3-X}/Au interface [99].
Secondly, the DC bias sweep measurement is repeated five times at the top electrode (the bottom electrode is grounded). Then, an increasing tendency of the current that is allowed to flow through the device is captured (Figure 5.3(b). To analyze the way in which the oxygen vacancies modify the metal/semiconductor interface property, the voltage is swept from $-1\,\mathrm{V}$ to $1\,\mathrm{V}$ at the post-modified device (Figure 5.3(d)). Compared with the pristine device(green line in Figure 5.3(d)), a weakened current blocking effect is observed in the negative voltage region, and a strengthened conductivity occurs at the positive part after five cycles. Furthermore, cycles are increased up to ten (groups of $I-V$ curves see Figure 5.3(c)), after which the $I-V$ characteristic of the device deviates from the pristine Schottky rectifying curves as shown in Figure 5.3(d). An anomalous negative differential resistance (NDR) [174] becomes more obvious at around $0.5\,\mathrm{V}$ after ten cycles in Figure 5.3(d). It is postulated that the N-shaped NDR observed in the forward bias is attributed to the conductance decay induced by diffusion of oxygen vacancy towards the bulk in the tungsten oxide layer. Spontaneously diffusion of oxygen vacancy endows the volatility of the reconfiguration at the Ag/WO_{3-X} interface, which is supported by a comparison between Figure 5.3(a) and (d). In Figure 5.3(a), the other two $I-V$ curves are obtained from the modified device after $15\,\mathrm{min}$, before which the device experienced five and ten

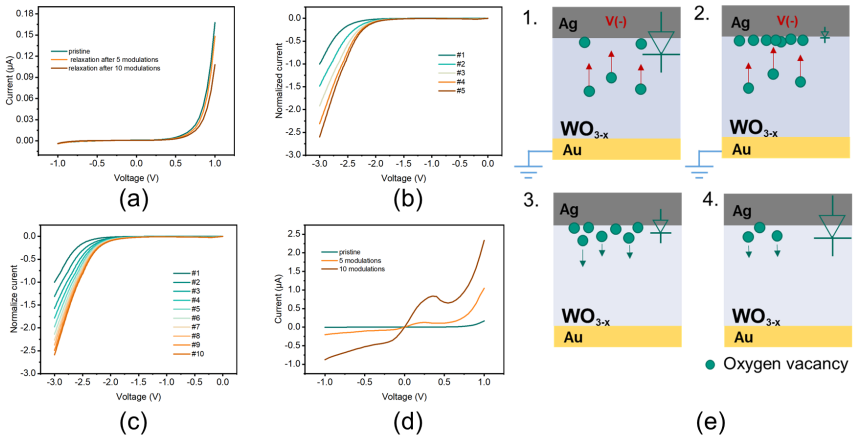


Figure 5.3: Experiments and corresponding discussion about mechanisms underlying the volatile analog resistive switching device behavior. **(a)** Current rectifying $I - V$ characteristic curves measured through voltage sweeps ranging from $-1\,\mathrm{V}$ to $1\,\mathrm{V}$, respectively, from pristine device and relaxed device after 5 and 10 times of modification. **(b)** and **(c)** Normalized I-V curves exhibit the enhanced conductivity of the device during modification employing 5 and 10 consecutive voltage sweeps in the range of 0 to $-3\,\mathrm{V}$. **(d)** $I - V$ curves measured thorough voltage sweeps ($-1\,\mathrm{V} \rightarrow 1\,\mathrm{V}$) on the pristine device and right after the last modification. **(e)** Schematic of the volatile analog resistive switching device behavior, which is ascribed to oxygen vacancy induced modification at the $\mathrm{Ag/WO_{3-X}}$ interface. Adapted from [139] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

consecutive voltage sweeps, respectively. After relaxation time, the property of the $\mathrm{Ag/WO_{3-X}}$ interface recovers to the Schottky-like contact as the overlapping of the three curves in Figure 5.3(a) suggests. To elucidate the dynamic process depending on the oxygen vacancy migration, the graphical representation of the process is shown in Figure 5.3(e). Once a negative voltage is applied to the top electrode, with the bottom electrode grounded, positively charged oxygen vacancies will be attracted towards the $\mathrm{Ag/WO_{3-X}}$ interface, where the continuous accumulation of n-type dopants will decrease the height of the Schottky barrier. As a consequence, the interface will behave like an Ohmic-like contact. As long as the applied voltage is disconnected, the spontaneous diffusion of oxygen vacancies will occur and lead to gradual recovery of the Schottky-like contact.

5.4 Emulation of Synaptic Functions

The results in this section were also reported in [139].

5.4.1 Artificial Memristive Synapse: Paired-pulse Facilitation

In a biological synapse (Figure 5.4(a), upper part), when two action potentials in rapid succession depolarize the pre-synaptic neuron, the second action potential can release more neurotransmitters than the first one, resulting in multiple times higher post-synaptic current (PSC) [175]. This biological phenomenon is called paired-pulse facilitation (PPF) [173, 175, 176, 177], and is described for biological synapses by the residual calcium (Ca^{2+}) theory [177]. Facilitation in biological synapses can persist for tens to hundreds of milliseconds and is considered an important factor in the encoding of temporal information [178].
The PPF is emulated with the presented inkjet-printed artificial memristive synapse by applying two identical voltage pulses and measuring the output current induced by these two successive voltage pulses within a short time interval (Figure 5.4(a)). The corresponding results for the artificial memristive synapse are shown in Figure 5.4(b), where successive voltage pulses of $-5\,\mathrm{V}$ are applied to the device over $10\,\mathrm{ms}$. The interpulse interval (Δt), which is the duration of the pulse-off time, is $30\,\mathrm{ms}$. It is observed that the second evoked current (I_2) exceeds the first (I_1), which is similar to the facilitation observed in biological synapses. As discussed earlier, this effect can be explained by oxygen vacancies in the tungsten oxide active layer, which migrate along the electrical field and accumulate near the Ag top electrode. This reduces the height of the Schottky barrier between the silver top electrode and the tungsten oxide, which leads to increased conductivity of the device. This effect has been observed also in other material systems (Pt/WO_{3-x}) [179] and other semiconductors [38, 171, 180]. Analogous to the residual Ca^{2+} theory, the migration and accumulation of the oxygen vacancies, triggered by the first input voltage pulse, contribute to the increase in the

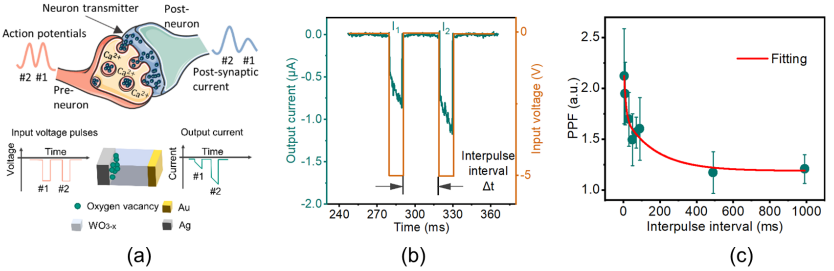


Figure 5.4: PPF of artificial memristive synapses. **(a)** Schematic of PPF in a biological synapse and emulation of PPF using printed AWAu memristor. **(b)** Experimental result of PPF measured from the printed AWAu memristor by applying two consecutive identical pulsed voltage. The amplitude of the second evoked current I_2 is higher than the first current I_1. **(c)** Decay of PPF measured in printed memristor with increasing interpulse interval. The green dots indicate the mean values and the error bar indicates the standard deviation. The fit of the exponential decay curve was performed using Equation (5.2). The schematic of the synapse in Figure 5.4(a) was modified based on the template from Servier Medical Art by Servier, which is licensed under a Creative Commons Attribution 3.0 unported license. Adapted from [139] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

conductivity produced by the second stimulus. Therefore, the interpulse interval needs to be shorter than the spontaneous diffusion time of the oxygen vacancies, which would counteract the accumulation and lead to an increase in conductivity. The synapse-like current enhancement observed in the memristor is quantified by the following equation [176]:

$$\mathrm{PPF} = \frac{I_2}{I_1}, \tag{5.1}$$

where I_1 and I_2 represent the PSC measured in the memristor and are caused by the first and the second voltage pulse, respectively.

Based on the residual Ca^{2+} theory, the magnitude of the PPF is supposed to decrease with increasing interpulse interval Δt [177, 181]. To emulate this interpulse-dependent decay in PPF for the artificial memristive synapse, paired pulses with identical height ($-5\,\mathrm{V}$) and width ($10\,\mathrm{ms}$), with varying interpulse interval, are utilized to stimulate the device. The interpulse intervals are set to $\Delta t = \{5, 10, 30, 50, 70, 90, 490, 990\}$ ms, respectively. The paired pulses of each interpulse interval are applied five times over the same memristor. The PPF

is calculated using Equation (5.1) for each interpulse interval and plotted as the mean values in Figure 5.4(c), including error bars, which indicate the standard deviation of the sample.
To describe the decreasing trend of the PPF with increasing interpulse interval, observed in the memristor, a double exponential decay function [176, 182] is modified in the following form:

$$\mathrm{PPF} = A + C_1 e^{(-\Delta t/\tau_1)} + C_2 e^{(-\Delta t/\tau_2)}, \tag{5.2}$$

where Δt is the interpulse interval, C_1 and C_2 are the enhancement magnitudes of the rapid and slow facilitation phases, whilst τ_1 and τ_2 represent the characteristic relaxation time of the two facilitation periods [176]. The parameter A is utilized to adjust the fitting results.
PPF over the interpulse interval is fitted as a red curve over the measured mean values and plotted in Figure 5.4(c), corresponding to a double exponential decay function from Equation (5.2). The red curve in Figure 5.4(c) shows facilitation with two components. It includes a fast decaying phase with τ_1 = 10 ms and C_1 = 0.68, as well as a slow decaying phase with τ_2 = 177 ms and C_2 = 0.54. The characteristic relaxation time constant of the two decaying phases is similar to the time scale of many biological synapses [176]. According to the fitting result, the parameter A in the modified double decay function Equation (5.2) is 1.19, which slightly deviates from the value of 1 in biological synapses [176]. From the PPF results, it is observable that the inkjet-printed artificial synapse is capable of emulating biological synapses.

5.4.2 Artificial Memristive Synapse: Short-term Plasticity with Enhanced Relaxation Time for Memory Formation

In the following, longer-lasting forms, such as potentiation, of synaptic plasticity are discussed. This is achieved by repeated, prolonged application of input stimuli trains between 200 ms - 5 s [176]. Potentiation is referred to as activity-evoked

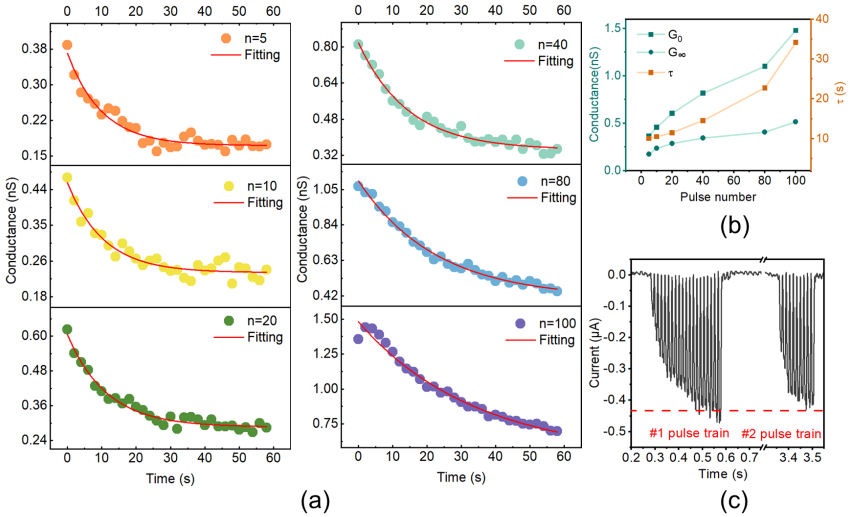


Figure 5.5: Memory formation process of the artificial memristive synapse. **(a)** Conductance decay after stimulation by various numbers of the voltage pulse, ($n = \{5, 10, 20, 40, 60, 100\}$). The conductance decay is fitted using Equation (5.3). **(b)** Extracted time constants (τ) and conductance enhancement (G_0, G_∞) from Equation (5.3). **(c)** Current responses of two voltage pulse trains. The first voltage pulse train requires 20 pulses to reach the threshold value (red dashed line), whereas for the second voltage pulse train, only 10 pulses are needed to reach the threshold value. The measured results indicate a faster learning process of the memristor after training. Adapted from [139] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

enhancement for a synaptic connection that can maintain synaptic efficacy over an extended period of time. Typical time spans are in the range of tens of seconds or even several minutes [183]. In addition to potentiation, another form of synaptic plasticity exists. If the activity-induced synaptic enhancement decays within a few seconds, it is referred to as augmentation [184].

The following experiments are designed to reconstruct the dynamic process that occurs at a post-synaptic neuron after the pre-synaptic counterpart is exposed to different numbers of repetitive stimulation. Through these experiments, different forms of synaptic short-term plasticity and memory formation in a biological synapse are emulated by the inkjet-printed memristors. Therefore, the device is

repeatedly stimulated with different negative voltage pulses (n = {5, 10, 20, 40, 80, 100}), with identical width ($20\,\mathrm{ms}$), height ($-5\,\mathrm{V}$), and interpulse intervals ($20\,\mathrm{ms}$).

After the last input voltage pulse, the device's conductivity is read out by measuring its resistance. This is performed every $2\,\mathrm{s}$ with a small voltage pulse of $0.01\,\mathrm{V}$ over $200\,\mathrm{ms}$. The change in conductance is visualized over time in Figure 5.5(a) to reveal various relaxation characteristics after different numbers of stimuli. The following equation is used to gain insight into the conductance decay and fit the obtained results. The form of the equation is derived from an exponential function used to describe the relaxation phenomena in biological synapses and in oxide materials. The modified equation is written as:

$$G(t) = (G_0 - G_\infty) \cdot e^{-(t/\tau)^\beta} + G_\infty, \tag{5.3}$$

where t is the recorded time after the last voltage pulse is applied to the memristor, $G(t)$ is the conductance at t, G_0 is the transient conductance immediately after the last input voltage pulse. Furthermore, G_∞ describes the stabilized conductance at infinite time, τ is the characteristic relaxation time constant, indicating how fast the conductance declines to $1/e$ of G_0, and β, ranging from 0 to 1, is considered as the stretching index to adjust the curve for a better fit [185]. In the case of the inkjet-printed memristor reported in this thesis, the conductance relaxation is adequately described when β is set to 1 in Equation (5.3) (red solid line in Figure 5.5(a)). Since the exponent β is related to the degree of correlation of the ion transport, the value of 1 indicates random Debye-like hopping of oxygen vacancies away from the silver electrode when the voltage applied to the memristor is removed [186].

As mentioned earlier, synaptic short-term plasticity of different forms can be distinguished by the relaxation time constant. When τ is extracted from the fitted curves in Figure 5.5(a) and plotted over the corresponding pulse number in Figure 5.5(b), an increase in the time constant from $10\,\mathrm{s}$ to $35\,\mathrm{s}$ with increasing pulse number is obtained. The extracted time constants in the inkjet-printed memristor coincide with reported values for augmentation (ca. $7\,\mathrm{s}$) and potentiation (ca. $30\,\mathrm{s}$) in biological synapses [187]. From a neurobiological point of view, prolonged

stimulation (increased stimuli when the pulse width and frequency are fixed) leads to an augmented release of Ca^{2+}, resulting in a longer time that is required to remove the residual Ca^{2+}. In the case of the memristor, oxygen vacancies behave similarly to Ca^{2+}. As more oxygen vacancies are forced to migrate to the top electrode with increasing numbers of input voltage pulses, the increased conductivity at the metal/semiconductor interface will decay slower.

As introduced previously, G_0 and G_∞ represent the transient conductive state and equilibrium conductive state, at $t = 0$ and $t = \infty$, respectively. Both values can be extracted from Equation 5.3, when fitted over the obtained measurement results, as shown in Figure 5.5(a). The obtained values are plotted over the pulse numbers in Figure 5.5(b). By increasing the number of input pulses, G_0 increases to larger values than G_∞. This leads to a higher activated amplitude $G_0 - G_\infty$, which accounts for the longer relaxation time constant (τ), shown in the same figure. The level of G_∞ in Figure 5.5(b) is consistently elevated by increasing the number of voltage pulses, which reveals a permanent increase of the conductivity in the memristor. The permanent conductance enhancement of the device is due to the stoichiometric changes of oxygen in the tungsten oxide active layer near the top electrode caused by the trapped oxygen vacancies. In neuroscience, a similar concept has been proposed to explain memory formation in the brain, which states structural changes in the synaptic morphology, known as "engram," underlying newly formed memory [188, 189].

Inspired by neuroscience, we can observe a "memory" effect at the tungsten oxide layer near the top electrode after repeated stimulation of voltage pulses due to reduced oxygen concentration in this area. This induced "memory" results from structural changes and residual oxygen vacancies right after the release of the voltage pulse train, which can jointly modulate the behavior of the device as shown in Figure 5.5(c). Primarily, a train of 20 voltage pulses of identical width, height, and time interval is applied to the Ag top electrode of an unformed memristor, and the induced current is measured.

After the memristor rests for several seconds, it's stimulated again with a pulse train incorporating the same parameters as the primary one but only using ten consecutive pulses. As visualized in Figure 5.5(c), the current evoked by each voltage pulse of the second stimulation train is largely increased, in comparison

to the primary pulse train, which indicates a faster and easier enhancement of the second group of repetitive stimuli. In this case, the subsequent plasticity of the memristor is modulated by the previous "activity-experience," which is labeled in neuroscience as metaplasticity [190]. Metaplasticity is regarded as a key property of a biological synapse that can address catastrophic forgetting, which means the previous learning contents are rapidly overwhelmed during the training of a new task [191]. By mimicking the metaplasticity of a synapse, several reported artificial networks can perform learning tasks faster [191, 192, 193]. From the measurement results obtained from our artificial memristor synapse, we observe plasticity as well as metaplasticity with excellent time scales close to biological synapses. The reported characteristics suggest the device's capabilities for neuromorphic computing.

5.4.3 Artificial Memristive Synapse: Frequency-dependent Input Signal Filtering and Integration

The earlier introduced experiments showed that the printed memristors could resemble important synaptic short-term plasticity properties regarding information storage and memory formation. Next to the reported figures of merit, further synaptic properties are accessible in biological synapses, such as signal filtering and integration [173, 194, 195, 196]. These synaptic signal processing capabilities can provide an important building block for artificial neural network circuits in order to increase the accuracy [195].
In the following, the capabilities of the inkjet-printed memristor to emulate synaptic short-term plasticity-related signal processing features, such as filtering and integration with respect to facilitation, are investigated. For the experiments, ten consecutive, identical voltage pulses, as shown in Figure 5.6(a), are applied to the memristor to mimic the input signal burst at a biological synapse. The output voltages are obtained over an additional resistor. The measurement setup is described in Chapter 3. The height of the input voltage pulse waveform is $-5\,\mathrm{V}$ and is applied over $10\,\mathrm{ms}$, while the interpulse time interval is varied to achieve

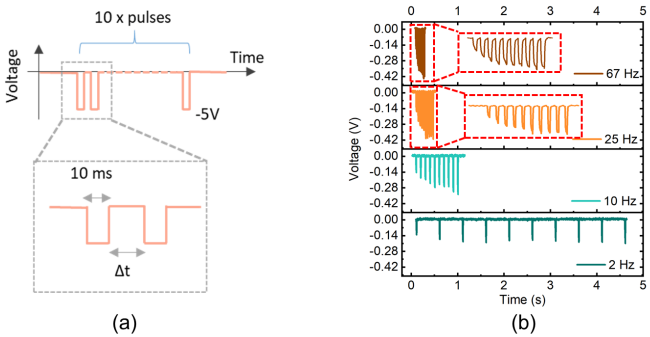


Figure 5.6: Frequency-dependent integration of input signals. **(a)** Waveform of the applied voltage pulse as input signals. The voltage amplitude and pulse-on time of a single voltage pulse are $-5\,\mathrm{V}$ and $10\,\mathrm{ms}$. Varying interpulse intervals can produce different frequencies, ranging over $2\,\mathrm{Hz}$, $10\,\mathrm{Hz}$, $25\,\mathrm{Hz}$, and $67\,\mathrm{Hz}$. **(b)** Output voltage of the memristor as a response to the input voltage pulse train for different frequencies.Adapted from [139] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

several frequencies of $2\,\mathrm{Hz}$, $10\,\mathrm{Hz}$, $25\,\mathrm{Hz}$, and $67\,\mathrm{Hz}$.
Figure 5.6(b) displays the output voltage response with respect to the input voltage pulse train over different frequencies. From the obtained measurements, the high-pass filtering and the integration behavior in the inkjet-printed device are observed. Although the pulse potential and pulse duration were kept the same, differences in the output potential are observable, which is similar to biological synapses with a low initial release function [173].

The experiments show that increased output potential can be measured with increasing input pulse frequency. The non-linear integration tendency is observable at input frequencies of $10\,\mathrm{Hz}$, $25\,\mathrm{Hz}$, and $67\,\mathrm{Hz}$ (see Figure 5.6). From $25\,\mathrm{Hz}$ and beyond, the voltage levels saturate at a plateau of $\approx 0.42\,\mathrm{V}$ due to oxygen vacancy saturation at the metal/semiconductor interface. At a low input signal frequency of $2\,\mathrm{Hz}$, no increase in voltage is seen. Here, the artificial synapse does not integrate the voltage levels, which resembles the behavior of a biological synapse with a low initial probability of release function [173]. The observed filtering and integration capability are explained by the electrical attraction of the positively charged V_o towards the Ag top electrode when applying negative

voltage pulses. This reduces the device's resistance due to the lowering of the Schottky barrier. As a result, the voltage drop on the voltage measurement resistor will gradually increase. However, after a certain number of successive voltage pulses, the conductivity at the Ag/WO_{3-x} interface cannot increase further, which results in a saturation of the voltage level. This can be explained by a change in the V_o gradient at the metal/semiconductor interface during operation. Therefore, the first voltage pulses can shift the V_o concentration easier than the later ones, which accounts for the saturated output voltage, shown in Figure 5.6(b). Furthermore, since the movement of V_o is defined by the on-and-off period of the input voltage pulse train, the cumulative enhancement of the conductivity is frequency-dependent. The higher the frequency of the input signals, the less time will be left for the device to "relax" between two voltage pulses, which leads to higher integration of the output voltage within a certain number of consecutive input voltage pulses.
The reported artificial synapse is capable of filtering unnecessary, low-frequency information of 2 Hz and shows frequency-dependent, non-linear integration capabilities at frequencies of 10 Hz, 25 Hz, and 67 Hz. This synaptic signal processing feature of the printed memristor is beneficial in artificial neural network circuits. The effect of non-linear efficacy increase and filtering was demonstrated using artificial dendrites [197].

5.5 Conclusions

This chapter exploits inkjet-printed $Ag/WO_{3-x}/Au$ memristor as an artificial synapse. First, the volatile analog resistive switching characteristics were studied in the AWAu cells that have not experienced the electroforming process. Only a negative voltage was applied to the Ag electrode while the Au electrode was grounded. The conductance of the memristive cell increases gradually upon the application of the negative voltage to the Ag electrode while decays exponentially after the release of the applied voltage. This analog resistive switching phenomenon of volatility observed in non-formed AWAu devices is attributed to

the Schottky barrier modulation at the Ag/WO_{3-x} interface. Upon application of a negative voltage to Ag electrodes, positively charged V_o is attracted to the Ag/WO_{3-x} interface and accumulates there, resulting in a reduction in Schottky barrier height and width. After the removal of the applied voltage, the accumulated V_o diffuses spontaneously back towards the WO_{3-x} layer, and the barrier structure at the interface recovers to its initial state. This volatile and analog resistive switching property of AWAu devices resembles the plasticity of biological synapses.

Next, the printed AWAu memristors were used to implement artificial synapses. The most fundamental synaptic function, paired-pulse facilitation (PPF), was emulated with the printed AWAu memristor. When increasing the time interval of the paired-pulse stimuli, the PPF measured from the printed memristor shows a two-phase exponential decay with time constants of $10\,\mathrm{ms}$ and $177\,\mathrm{ms}$, which is similar to biological synapses. This time interval-dependent signal-facilitating feature was further exploited to emulate the synapse's frequency-dependent input signal integration property. The results show that input signals of $2\,\mathrm{Hz}$ can not be integrated at the output terminal of the printed memristor, and only when the signals are above $10\,\mathrm{Hz}$ are non-linearly integrated. This property is beneficial to implement high-pass filters, where the low frequency (below $10\,\mathrm{Hz}$) signals are filtered out.

Furthermore, multiple forms of synaptic short-term plasticity were mimicked by the printed memristor. The measured timescales are close to that of a biological synapse, including facilitation (10-$177\,\mathrm{ms}$), augmentation ($10\,\mathrm{s}$), and potentiation ($35\,\mathrm{s}$). These biological-similar timescales are rarely reported in other artificial synaptic devices. In addition, a higher order of short-term synaptic plasticity, i.e., metaplasticity, is also emulated with the printed memristor. The short-term plasticity results indicate that the printed AWAu memristors can work as artificial synapses and implement working memory functions, which rely on multiple forms of short-term plasticity. The results in emulating synaptic behavior with printed memristors show great potential in implementing neuromorphic computing.

6 Printed memristor for Hardware Security

6.1 Introduction of Hardware Security Based on Memristors

Information security is one of the main topics in the digital era. The demands for information security are ubiquitous, including but not limited to anticounterfeiting, identification, authentication, and key generation [198]. The common measures for security are categorized into software- and hardware-based methodologies. Software-based security solutions rely on algorithms, possessing advantages like low cost and straightforward implementation, but are vulnerable to bugs, Trojans, and hacking [199]. Hardware-based security primitives leverage instance-specific and process-induced variations in physical devices as the entropy sources for proper security implementation [200]. Hardware-based security solutions are generally believed to provide superior security than their software-based counterparts. True random number generators (TRNG) and physical unclonable functions (PUF) are the two promising hardware security primitives. TRNG is used to efficiently generate unpredictable random bitstreams that are the cornerstone of an encryption algorithm. PUF is a physical entity (can be a device or an interconnected system) that is able to generate a unique "fingerprint" or trust anchor, which is used for identification, authentication, and cryptographic key generation [198, 201].

Both TRNG and PUF were first implemented using CMOS technology. The former mainly exploits the noise properties of metal oxide semiconductor field-effect

transistors (MOSFETs), while the latter utilizes the intrinsic performance variations of MOSFETs introduced during the manufacturing process, such as dopant variations, defects, and geometrical dimensions. Although the CMOS technology is mature for fabricating integrated circuits, it was proven not optimal for hardware security primitives due to the high cost in manufacturing, poor energy efficiency in implementing security functions, and, most importantly, limitation in entropy quality [202]. Alternatively, emerging memory technologies include phase change memory (PCM) [203], magnetic random access memory (MRAM) [204], ferroelectric random access memory (FeRAM) [205], and resistive random access memory (ReRAM) [200, 206, 207], are promising for novel hardware security primitives due to their technical advantages, such as energy efficiency, relatively high operating speed, and moderate manufacturing costs[35]. Among them, ReRAM, based on memristive cells, is at the cutting edge of both TRNG and PUF research. Random telegraph noise (RTN), which is commonly observed in filamentary memristors stemming from the charge trapping/de-trapping at the defect site, is commonly exploited to implement TRNG. Thanks to the large amplitude of the RTN in memristors, the preamplifier circuit can be eliminated in memristive TRNGs [199]. In addition, cycle-to-cycle variation in memristive cells is exploited to perform high-frequency and low-energy consumption TRNGs [208]. As introduced earlier, PUF leverages the intrinsic randomness of a physical system to produce a unique output. This intrinsic randomness is introduced during manufacturing, which is an analogy to a “fingerprint” or a “retina” of humans and is impossible to be physically cloned. Compared to other micro/nanoelectronics devices relying on manufacturing randomness, memristive PUF possesses an additional entropy source that originates from the inherent stochastic ion migration [199]. In other words, apart from the device-to-device variation, the cycle-to-cycle variation of memristive cells is also an excellent entropy source for implementing PUFs. This unique feature renders memristor-based PUFs reconfigurable and reduces the cost.

One of the primary motivations for developing novel hardware security primitives is to seek a robust, lightweight, and low-cost solution for IoT applications, which envisions a highly interconnected world bearing massive data generation and transmission. Printed electronics (PE) is widely accepted as one of the promising

technologies fostering the development of IoT. As introduced previously, various electronic components have been achieved with PE or are being the hot topic of PE. However, research in printed hardware security is still in its infancy. Some research on inkjet-printed PUFs based on electrolyte-gated field effect transistor (EGT) [201, 209, 210] are reported and have demonstrated enormous potential in lightweight security applications; one work reported the implementation of TRNGs with inkjet-printed h-BN memristor [69]. Only solution-processed memristive PUFs [211] have been reported. Laser-printed memristive PUF array in this chapter is the first printed memristive PUF.
In the following, the device characteristics of a laser-printed memristor consisting of an Ag/ZnO/Pt (termed AZP in the later discussion) structure are first presented. Next, a laser-printed 6×6 memristive crossbar is demonstrated as a PUF core. By exploiting the device-to-device variations, a unique and random 36-bit string was generated, which is promising for identification purposes.

6.2 Device Characteristics of Laser-printed Memristor

The results in this section were also reported in [121].

The studied memristor is fully laser-printed consisting of an Ag TE ($0.72\,\mu\mathrm{m}$ in linewidth), a ZnO active layer ($1.80\,\mu\mathrm{m}$ in linewidth), and a Pt BE ($0.60\,\mu\mathrm{m}$ in linewidth), as shown in Figure 6.1(a). The crossing of the Ag top electrode and the orthogonal Pt bottom electrode, with the ZnO sandwiched in-between, leads to an effective device area that is estimated to be ca. $0.43\,\mu\mathrm{m}^2$. Quasi-static voltage sweeping was performed to capture the resistive switching characteristics of the laser-printed memristor, and the obtained $I - V$ curves are plotted on a semi-logarithmic scale in Figure 6.1(b). The characterization protocol is as follows: A positive potential is applied to the top Ag electrode while the Pt electrode is grounded. To enable the initial resistive switching in a pristine device, a forming voltage sweep ($0\,\mathrm{V} \rightarrow 8\,\mathrm{V} \rightarrow 0\,\mathrm{V}$) was applied. The black current-voltage curve

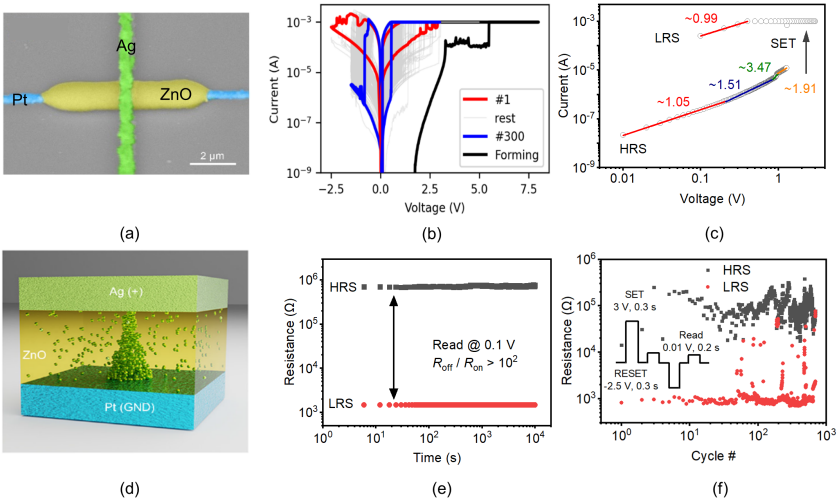


Figure 6.1: Laser-printed memristors and typical device characteristics. **(a)** Colored SEM micrograph of a fully laser-printed memristor in a structure of Ag/ZnO/Pt, **(b)** $I - V$ curves of a single memristor captured from 300 consecutive voltage sweeping cycles. The curves of Forming (black), the first cycle (red), and the cycle number 300 (blue) are emphasized by color. The other cycles are plotted in light gray curves. The curves are plotted on a semi-logarithmic scale. **(c)** A curve of SET plotted on a double-logarithmic scale. Linear fitting was performed to calculate the slopes of multiple voltage regions for conduction mechanism analysis. **(d)** A schematics of postulated filamentary resistive switching mechanism based on conduction mechanism discussion in (c). **(e)** Retention performance of the characterized memristor carried out by monitoring the LRS and HRS over 10^4 s. **d** Endurance performance of the characterized memristor under pulsed voltage mode over 700 cycles. The used voltage waveform is shown in the inset. Adapted from [121] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

in Figure 6.1(b) shows a pronounced current increase at around $5.5\,\mathrm{V}$, where it reaches the compliance current of $1\,\mathrm{mA}$.

RESET was realized by a voltage sweep at the TE from $0\,\mathrm{V}$ to $-1.5\,\mathrm{V}$ and back to $0\,\mathrm{V}$. The $I - V$ characteristics during the RESET process are visualized in Figure 6.1(b). SET was carried out by sweeping the voltage from $0\,\mathrm{V}$ to $3\,\mathrm{V}$ and back to $0\,\mathrm{V}$ at the TE. By alternatingly repeating the set and reset operations, the device is switched between HRS and LRS over 300 cycles. The 300 $I - V$ curves of the SET and RESET processes are shown in Figure 6.1(b) on a semi-logarithmic scale, from which an $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio of about 10^2 can be seen.

To study the resistive switching mechanism, following the previously introduced methods in Chapter 4, one of the SET curves from Figure 6.1(b) is plotted on a double-logarithmic scale in Figure 6.1(c). Linear fitting is performed on the curve of LRS and HRS to calculate the respective slopes. The fitting results indicate that the LRS is dominated by Ohmic conduction (with a slope of ca. 0.99), while the HRS exhibits a good accordance with trap-controlled space-charge-limited conduction (TCSCLC). With increasing voltage amplitude but prior to the resistive switching being triggered, the slope value of HRS shows a three-phase rise from 1.05 over 1.51 to 3.47. The fitting results imply that the TCSCLC has different charge-filling states, which is similar to the process described in the case of the AZAu device. One dissimilarity is that the period with a slope of 1.91 follows an exponential increase. This indicates a trap-free SCLC at a high electrical field before the device is switched to LRS [212]. This is observed in TCSCLC at a high-electrical field after the traps within the active layer are fully filled with charge carriers. In the case of inkjet-printed AZAu, this phase is missing since the SET voltage is lower. AZAu devices are switched to LRS before experiencing a trap-free SCLC phase. This difference in mechanism between the two types of printed memristor can be ascribed to the porosity of the ZnO layer. This needs further investigation of material-electrical correlated issues in future studies.

The material stack of this memristor is designed for cation-based resistive switching, in which the active Ag atoms form conducting filaments within the active layer by applying an appropriate voltage to the electrodes. The resistive switching mechanism is postulated to resemble the inkjet-printed AZAu device, as discussed earlier. Through manipulation of the formation and rupture of the Ag conducting filaments in the ZnO active layer (Figure 6.1(d)), by applying a proper voltage to the electrodes, a typical bipolar resistive switching is observed for the laser-printed devices.

To evaluate the retention performance, the memristor was switched to HRS and LRS, respectively, and the resistance of the device was measured every $6\,\mathrm{s}$ by applying a voltage pulse with a width of $0.2\,\mathrm{s}$ and a height of $0.1\,\mathrm{V}$ to the TE over a total timespan of $10^4\,\mathrm{s}$. As can be seen from Figure 6.1(e), both states are stable over the entire time period, with no sign of degradation. To examine the

dynamic performance of the device when subject to voltage pulses for programming, a waveform shown in the inset of Figure 6.1(f) was used. This waveform consists of a SET voltage pulse and a RESET voltage pulse with the indicated widths and heights. After each voltage pulse operation, the resistance state of the device is read out by a small voltage pulse (width $0.2\,\mathrm{s}$, height $0.01\,\mathrm{V}$) while it was repeatedly switched between HRS and LRS over 700 times (Figure 6.1(f)). Only a few set operations have failed during the 700 switching cycles.

6.3 Laser-printed Memristive Crossbar as Physical Unclonable Function (PUF)

The results in this section were also reported in [121].

As proof of concept, the first reported laser-printed memristor presented in this chapter has the smallest area ($0.43\,\mu\mathrm{m}^2$) among all the reported solution-processed memristors based on cross-point form [126], and has shown promising resistive switching characteristics. Nevertheless, the laser-printed memristor also shows the common drawback of high cycle-to-cycle variability stemming from the inherent resistive switching mechanism. This natural stochastic device behavior can be largely improved by optimizing the device structure in the future. Considering the excellent resistive state retention property of laser-printed memristors (Figure 6.1(c)) and leveraging the superior fabrication ability of laser direct printing in integrated microelectronics, it's worth exploiting circuit-level applications involving multiple memristors. As introduced earlier, the intrinsic variability of memristive cells is promising for hardware security, in particular as an entropy source for physical unclonable function (PUF). Prior to optimizing the laser-printed memristor to meet the strict requirements of logic or memory applications, the stochastic nature of the laser-printed memristors was exploited for a PUF.

First, a 6×6 crossbar architecture shown in Figure 6.2(a). The whole memristive

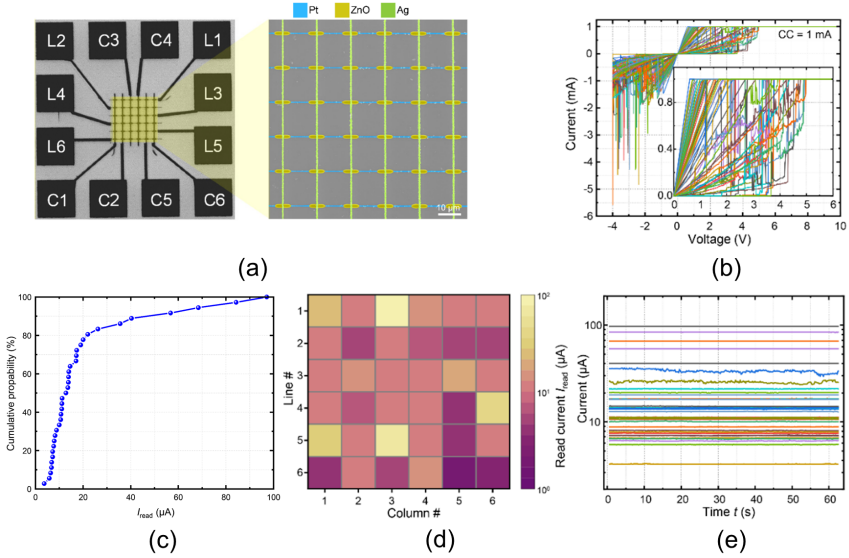


Figure 6.2: Characteristics of a 6×6 laser-printed memristive crossbar. **a** Left-hand side: Optical micrograph of the memristive crossbar with contacting pad. Right-hand side: Zoom-in of the crossbar captured by an SEM micrograph. The Pt BE, ZnO, and Ag TE are colored blue, yellow, and green, respectively. **(b)** $I - V$ curves showing the activation of 36 memristive cells are plotted in one figure but in different colors. The activation of every single cell followed a voltage sweeping protocol: $0\,\mathrm{V} \rightarrow 10\,\mathrm{V} \rightarrow -4\,\mathrm{V} \rightarrow 0\,\mathrm{V}$. The inset shows the zoom-in of the curves on the positive voltage regime with a CC of $1\,\mathrm{mA}$. **(c)** Distribution of the I_{read} collected from the 36 memristive cells in the crossbar. I_{read} was measured under $0.1\,\mathrm{V}$. **(d)** False-color representation of the I_{read} from the memristive crossbar. **(e)** Retention performance of 36 memristive cells within the crossbar by monitoring the I_{read} over $60\,\mathrm{s}$. Adapted from [121] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

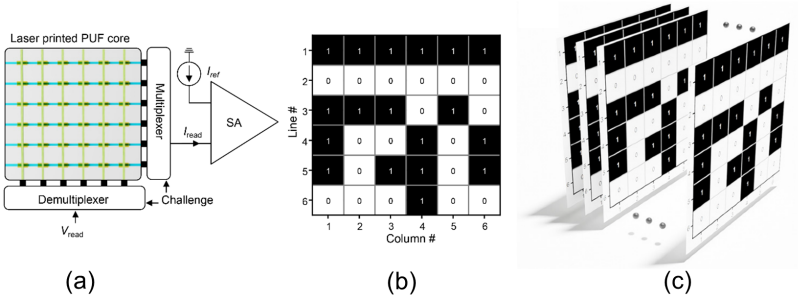


Figure 6.3: Performance of the laser-printed PUF based on a 6×6 memristive crossbar. **(a)** Schematics of the circuit architecture around the memristive PUF core. **(b)** Bit-array distribution corresponding to the 6×6 crossbar array. **(c)** Schematics of the evaluation bit errors over 300 cycles. Adapted from [121] under CC BY 4.0 license, `http://creativecommons.org/licenses/by/4.0/`.

crossbar circuit, including the surrounding Ag contacting pads (shown as the optical micrograph in the left-hand side of Figure 6.2(a)) and the memristive crossbar in the middle part (zoom in captured by SEM shown in the right-hand side of Figure 6.2(a)), were realized by laser-printing. At each node of the vertical Ag lines and the horizontal Pt lines exists a memristive cell involving a ZnO active layer of $1.8\,\mu\text{m}$ in linewidth. The details of laser printing are referred to in Chapter 3. This circuit is utilized as a physically unclonable function (PUF), a hardware-based security primitive. The PUF generates a unique response upon stimulation by a challenge comparable to a human fingerprint [198]. Herein, the variability of the memristor due to stochastic formation and rupture of conducting filament paths is the key [35, 213, 214]. For the initialization of the laser-printed memristor-based crossbar PUF, each device in the array is initially formed and then RESET, using a floating bias scheme. The initial Forming and RESET processes of the 36 memristor cells are shown as the $I - V$ curves in Figure 6.2(b). The inset in Figure 6.2(b) captures the current variations among 36 formed cells under the application of a positive voltage. This is the key factor for implementing a memristive PUF. After the initialization, the crossbar forms an interconnected resistive network, with varying resistances of the corresponding memristor cells and the laser-printed interconnects.

After the initialization of the crossbar, each memristor cell is addressed by applying a read-out voltage of $0.1\,\mathrm{V}$ and measuring the corresponding read-out current I_{read} in a floating bias scheme. The readout current is composed of the parts flowing through the selected devices and all sneak-path current from all unselected devices [215]. The cumulative distribution function of the I_{read} values is shown in Figure 6.2(c). Figure 6.2(d) shows the obtained I_{read} values corresponding to the device location in the crossbar in a false-color representation. To investigate the noise effects on the response stability, read-out operation in 200 ms time intervals over 300 cycles was performed on each device, and Figure 6.2(e) shows the temporal stability of the selected cells. The laser-printed memristive crossbar shows an excellent entropy source ascribed to the large device-to-device variation and temporal reliability validated by the retention measurements. These two features are ideal for building up a PUF core. Next, the performance of the memristive crossbar array as a PUF core is discussed.

For the complete architecture around the core of the physically unclonable function, a control logic as illustrated in Figure 6.3(a) is required. The control logic of the PUF was emulated by employing a multiplexer (MUX) and demultiplexer (DEMUX) for signal routing. By applying the challenge, which holds the DEMUX and MUX addresses for line and column selection, each memristor cell was selected by applying V_{read} and routing I_{read} to the input of the sensing amplifier. The iteration started at the uppermost line, went over all columns, and then moved to the next line. This was continued until all cells were addressed and the full challenge-response pair (CRP) was obtained, which led to a 36-bit wide response. The selected cell's I_{read} was compared to a reference current, I_{ref}, by a sense amplifier (SA), as shown in Figure 6.3(a). Based on which current exceeds the other, the sense amplifier generated an output (r_k) logic "0" or logic "1", according to Equation 6.1.

$$r_{\mathrm{k}} = \{1 \text{ if} I_{\mathrm{read}} > I_{\mathrm{ref}}, 0 \text{ if} I_{\mathrm{read}} < I_{\mathrm{ref}}\} \tag{6.1}$$

With this method, a $L_{\max} = M$ long PUF response was generated, where $L_{\max}$ was the maximum obtainable response length of the PUF, and M the amount of incorporated memristor cells. As a suitable value for the reference current I_{ref}, the median of the experimentally obtained I_{read} values was used, which yielded

$13.21\,\mu\mathrm{A}$ for the laser-printed crossbar structure shown in Figure 6.2(a). For the sense amplifier, the minimal current difference that can be sensed was assumed to be $100\,\mathrm{nA}$. Lower differences between currents were not distinguished but could potentially lead to a bias in the PUF response. The obtained bit-distribution across the array and the obtained 36-bit wide response $R = (r_1, r_2, r_3, ..., r_\mathrm{k}) = (111111000000111010100101101101000100)$ and the extracted bit patterns are illustrated in Figure 6.3(b), demonstrating that the laser-printed 6×6 array shown in Figure 6.2(a) represents a fully functional security circuit based on a physically unclonable function. Furthermore, no bit errors (BE= 0 %) occurred over 300 iterations for the investigated crossbar, as shown in Figure 6.3(c). The bit error calculation is schematically shown in Figure 6.3(c). The details of the calculation of the bit error are referred to in the Appendix.

6.4 Conclusions

In this chapter, a memristor consisting of an Ag TE, a ZnO active layer, and a Pt BE are presented. The whole material stack was fully laser-printed based on multi-photon absorption, with the patterning and sintering of the materials accomplished simultaneously. Moreover, the laser-printed Ag and Pt lines have a linewidth of $0.72\,\mu\mathrm{m}$ and $0.60\,\mu\mathrm{m}$, thus determining the smallest device area of $0.43\,\mu\mathrm{m}^2$, which is the record amongst all printed memristive devices.
The laser-printed memristor operates in a bipolar resistive switching mode with a $R_\mathrm{off}/R_\mathrm{on}$ ratio of 10^2. Under dynamic pulsed voltage mode, the laser-printed memristor shows good endurance over 700 cycles. The retention performance of the laser-printed cells was tested, and the results show no perceptible degradation of the memory window throughout a test time period of $10^4\,\mathrm{s}$. The electrical characterization implies the potential of laser-printed memristors for nonvolatile digital applications.
Next, a memristive crossbar consisting of 6×6 Ag/ZnO/Pt memristors was fully laser printed. All memristive cells were electroformed and RESET in HRS. The variations of HRS from device to device were exploited to implement a PUF,

which generated a random bit string consisting of 36 binary numbers. The bit string is stable among 300 iteration cycles, and it shows no bit error. The results show the potential of laser-printed memristive arrays in circuit-level applications for hardware security.

Multi-material based on multi-photon absorption laser printing was first used to fabricate microelectronic circuits. This technology shows extraordinary advantages in terms of device feature size and integration ability. This opens up a new application field in additive manufacturing technology.

7 Summary and Outlook

7.1 Summary

Printed electronics is a technological complementary to CMOS, showing unique advantages in specific application scenarios, including large-scale sensing in environmental, industrial, and agricultural monitoring, flexible electronics for wearable health monitoring, as well as lightweight and low-cost electronics products for the Internet of Things (IoT). However, the current achievements of printed electronics are still limited to direct components (e.g., sensors, diodes, transistors, and so forth) and simple circuits. The reasons behind that are ascribed to the lack of high-performance printed components for information storage and processing. Memristors, also referred to as resistive switching devices, have been proven as vacuum-processed devices that are promising for non-volatile memory and novel computing paradigms. Nevertheless, research on printed memristors is still in its infancy. This thesis explored the potential of solution-processable metal oxides in printing resistive switching devices and exploited their resistive switching characteristics in applications such as non-volatile memory, neuromorphic computing, and hardware security. Solution processable ZnO and WO_{3-x} were studied as the active layer of the resistive switching devices; inkjet printing and laser printing were used as the fabrication techniques.

Chapter 4 presents three types of inkjet-printed memristors of different materials stacks, including Ag/ZnO/Au, Ag/ZnO/Ag, and Ag/WO_{3-x}/Au. Ag is selected as the active electrode material, serving as both an excellent current conductor and cation supplier. The formation and rupture of the Ag-based conductive path within the active layer account for the digital-type resistive switching phenomenon observed in these three printed memristors. This is supported by distinct current

conduction mechanisms derived from the linear fitting discussion on $I-V$ curves of LRS and HRS. Thus, the three inkjet-printed memristors are categorized into electrochemical mechanism (ECM) type regarding the working mechanism.
Depending on the properties of the solution-processed metal oxides, the inkjet-printed memristors exhibit different device characteristics. Although both are based on ZnO transformed from an in-house developed zinc nitrate aqueous precursor ink, asymmetric Ag/ZnO/Au cells work in bipolar resistive switching mode, while the symmetric Ag/ZnO/Ag exhibit unipolar resistive switching behavior. The different BE materials are the main cause for the dissimilar device characteristics. In the case of Ag BE, Ag diffuses into the ZnO layer during the thermal sintering of the precursor ink, which is analogous to doping the ZnO with Ag during the fabrication. Consequently, the forming voltage in Ag/ZnO/Ag devices is as low as the SET voltage, enabling the devices to work in an almost forming-free mode. In addition, the fully inkjet-printed Ag/ZnO/Ag devices possess a particularly large $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio of 10^7 under dynamic pulsed voltage endurance test, which is even higher than most of the vacuum-processed memristive devices. In the case of the Ag/ZnO/Au devices, although a forming process is required to trigger the first resistive switching, an average forming voltage value of $4.05\,\mathrm{V}$ is still relatively low compared to the commonly reported vacuum-processed devices. The Ag/ZnO/Au devices show a balanced $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio (10^4) and endurance (500 cycles).
When the active layer is replaced with a nanoparticulate metal oxide dispersion ink, i.e., WO_{3-x}, a printed memristor with a structure of Ag/WO_3-x/Au can be fabricated at a low temperature of $120\,^{\circ}\mathrm{C}$. The Ag/WO_3-x/Au cells resemble the Ag/ZnO/Au devices regarding the electrode materials and the resistive switching mode. The lower bandgap of WO_{3-x} determines a smaller memory window of 10^2 but compensates with an excellent endurance above 12672 cycles, the record amongst reported printed memristors.
All three presented printed memristors can be operated at a low voltage $< 2\,\mathrm{V}$, and the RESET voltages are lower than $0.5\,\mathrm{V}$ in Ag/ZnO/Ag and Ag/WO_{3-x}/Au memristors. All studied printed memristors exhibit excellent retention above $10^4\,\mathrm{seconds}$ within the test period and no degradation of the memory window was observed. These remarkable device performances indicate the potential of

the printed memristors in the application of printed non-volatile memory.
Chapter 5 investigates the inkjet-printed Ag/WO_{3-x}/Au memristive devices that work without the formation of the Ag filaments. By eliminating the electroforming process in pristine memristors and applying a merely negative voltage to Ag TE, the printed Ag/WO_{3-X}/Au memristors show a gradual increase in conductance, which is volatile and decays spontaneously after the removal of the voltage. These volatile and analog resistive switching behavior are attributed to the Schottky barrier modulation at the Ag/WO_{3-x} interface due to a change in oxygen vacancy concentration. The volatile and analog resistive switching properties of the inkjet-printed Ag/WO_{3-x}/Au memristors are exploited to mimic synaptic functions. The fundamental synaptic function, paired-pulse facilitation, was remarkably emulated by the printed memristors, in particular, the two-phase exponential decay of PPF versus time interval with biological-similar time constants of $10\,\mathrm{ms}$ and $177\,\mathrm{ms}$. This property is further used for emulating frequency-dependent input signal integration and filtering. The results show that the printed memristors can serve as high-pass filters, allowing signal above $10\,\mathrm{Hz}$ to be integrated non-linearly. In addition, multiple forms of short-plasticity were achieved with the printed memristor, including facilitation (with a timescale of 10-$177\,\mathrm{ms}$), augmentation (with a timescale of $10\,\mathrm{s}$), and potentiation (with a timescale of $35\,\mathrm{s}$). Besides, a higher order of short-term plasticity, i.e., metaplasticity, is also emulated with the printed memristor. Short-term plasticity results indicate that the printed AWAu memristors can work as artificial synapses and implement the working memory function, which relies on multiple forms of short-term plasticity. The obtained results show great potential for implementations in neuromorphic computing. Last but not least, both filamentary and interfacial types of resistive switching behaviors are achievable with identical material stack, depending on the activation process applied to devices as fabricated, These multimodal features can be utilized to enable novel circuit design paradigms in printed electronics for near-sensor computing and wearable electronics.
Chapter 6 presents a fully laser-printed memristive device in a structure of Ag/ZnO/Pt and a circuit-level application for hardware security. This is the first time that advanced multi-material laser printing technology based on multi-photon absorption has been applied to microelectronics manufacturing. Due to

the superior structuring ability of laser printing, tiny Ag lines and Pt lines, respectively, with a linewidth of $0.72\,\mu m$ and $0.60\,\mu m$ were achieved. These feature sizes of the electrode materials defined the smallest device area ($0.43\,\mu m^2$) among all reported printed memristors. The laser-printed memristors show an endurance over 700 cycles, a memory window of 10^2, and a retention time over $10^4\,s$. These device performance parameters have proven adequate for later implementing a circuit-level hardware security application. A memristive crossbar of 6×6 Ag/ZnO/Pt memristors was fully laser-printed and successfully implemented as a PUF. The laser-printed memristive PUF generated a random bit string of 36 binary numbers. The bit string is stable over 300 iterations, showing no bit error (bit error = 0%), which can be used for identification. The results demonstrate the potential of laser-printed memristive arrays in circuit-level applications for hardware security.
In summary, printed resistive switching devices based on solution-processable metal oxides can show excellent performance, which is promising for applications, including non-volatile memory, neuromorphic computing, and hardware security. These novel printed devices will undoubtedly broaden the application spectrum of printed electronics.

7.2 Outlook

The presented results have driven a solid statement that printed resistive switching devices based on solution-processable metal oxides will advance the development of printed electronics. However, the research of printed memristors is still in the early stage, and future research is suggested from the following perspectives.
To understand the resistive switching mechanism, the current study remains in the imaginary scene of conducting filaments. The visualization of filaments within the thick solution-processed metal oxide layer (generally with a thickness of hundreds of nm) is still absent. Advanced imaging technologies, including in-situ and ex-situ electron microscopy (e.g., SEM and TEM), are highly recommended

for capturing the conductive filaments on a nanometer scale. The dynamic process of resistive switching in printed memristors is worthy of investigation, which will disclose the details of multiple chemical processes underlying the resistive switching, e.g., ion migration and nucleation. The above-mentioned results will facilitate the development of physical and behavioral models for printed memristors, which will eventually foster large-scale applications of printed memristors.
From the perspective of device engineering, the biggest challenge for memristor technology is the device-to-device and cycle-to-cycle variations, which is also true for printed memristors. The former variation stems from the manufacturing process and turns out to be even more severe in printed memristors. Therefore, improvements in the reliability of the printing process are highly demanded for realizing circuit-level applications with printed memristors. The later variation originates from random ion movements during resistive switching. This is an intrinsic property of memristive devices and can be improved by material and structural engineering of the device stack. The existing device engineering strategies are reported based on vacuum-processed technology and thus are incompatible with solution-based processes. Under this circumstance, a new device engineering concept is expected to mitigate the challenge of cycle-to-cycle variability in printed memristors.
From the view of large-size applications, the sneak-path problem will also be an obstacle to implementing crossbar memristive circuits. An appropriate printed selector, e.g., printed diode, transistor, or threshold-type memristor, must be fabricated together with the printed memristor. Concerning the limitation of the current printing technology in achieving complex structures, printed memristors with self-rectifying properties are promising for the realization of a 1R crossbar structure.

A Appendix

A.1 Ink Preparation for Inkjet Printing

$Zn(NO_3)_2$ aqueous precursor ink: zinc nitrate hexahydrate ($Zn(NO_3)_2 \cdot 6\,H_2O$, 98%, from Aldrich) was weighted and dissolved in a mixed solution of de-ionized water and glycerin (from Merck), which is in a volume ratio of 4:1. The concentration of the $Zn(NO_3)_2 \cdot 6\,H_2O$ is 0.1 M. The prepared precursor ink was stirred at room temperature for $2\,\mathrm{h}$ until turned fully transparent. The ink was filtered with a $0.2\,\mu\mathrm{m}$ PVDF membrane filter before use.

Ag nanoparticle dispersion ink: Commercially available silver nanoparticle dispersion ink from Sigma Aldrich (Silverjet, DGP). The solvent is triethylene glycol monoethyl ether and the concentration of silver nanoparticle is 30 - 35 wt. %. The particle size of silver is $\leq 50\,\mathrm{nm}$. The ink was used as received, without additional treatments.

WO_{3-x} nanoparticle dispersion ink: Commercially available tungsten oxide nanoparticle dispersion ink from Sigma Aldrich. The WO_{3-x} nanoparticles of a size $< 50\,\mathrm{nm}$ are dispersed in 2-propanol in a concentration of 2.5 wt. %. Prior to use, the ink was filtered firstly with a $0.7\,\mu\mathrm{m}$ glass fiber membrane.

Inkjet printer: Drop-on-demand piezoelectric inkjet printer from Fujifilm (DMP2831) was used for printing. Cartridges with $10\,\mathrm{pL}$ nozzle print heads were used to print materials.

A.2 Preparation of Non-printed Electrode

Au coated glass: Commercial available Au-coated slide glass (aluminosilicate glass) from Sigma Aldrich. A thin layer of Titanium is used to provide better adhesion of gold to glass. The gold layer is polycrystalline and has a thickness of 1000 Å.
Laser ablation: Au electrodes were ablated by Trumpf TruMicro 5000 ps laser.

A.3 Ink Preparation for Laser Printing

Pt ink: A 0.500 M stock solution of ammonium iron oxalate trihydrate ($(NH_4)_3[Fe(C_2O_4)_3] \cdot 3\,H_2O$, Alfa Aesar, 98%), and a 0.070 M stock solution of ammonium tetrachloroplatinate ((NH4)2[PtCl4], Alfa Aesar, 99.9% metal basis) in deionized water (conductivity 16-18 MΩ) were prepared and stored in the dark at 4 °C. The Platinum-based ink (1:1 by volume $(NH_4)_3[Fe(C_2O_4)_3]$: $(NH_4)_2[PtCl_4]$) was always freshly prepared prior to the laser printing experiments.
Ag ink:An aqueous solution of 0.083 M silver nitrate ($AgNO_3$, Alfa Aesar, 99.9+% metal basis) and 0.062 M trisodium citrate (Carl Roth, 99% p.a. ACS) was prepared. 14.000 M aqueous ammonia solution (28-30%, Merck, ACS Reag. Ph. Eur.) was added dropwise under stirring until the intermittently formed precipitate redissolved and a homogeneous solution was obtained.
ZnO ink: To obtain a ZnO ink with both a precise pH and Zn^{2+} concentration, the addition of ammonia must be conducted while monitoring the pH and the temperature. The pH values were determined using a Mettler-Toledo Seven Easy pH meter equipped with a Mettler-Toledo InLAB Science Pro-ISM electrode (inside/outside electrolyte 3.000 M KCl) equipped with a built-in temperature sensor (NTC). The built-in temperature compensation was used to arrive at the errors quoted in the main text. The electrode was calibrated by three-point calibration using pH 4.00, 7.00, and 10.00 calibrants (Roti®Calipure, Carl Roth).
Zink nitrate hexahydrate $Zn(NO_3)_2 \cdot 6\,H_2O$, Alfa Aesar, >98%) was dissolved

in deionized water (conductivity 16-18 MΩ, pH = 6.30) at room temperature. 14.000 M aqueous ammonia (28-30%, Merck, ACS Reag. Ph. Eur.) was added dropwise until the intermittently formed white precipitate was almost completely redissolved. Subsequently, the solution was stirred at 20 °C for 15 min. Additional ammonia was added dropwise until the desired pH value was reached. Afterward, the solution was filled into a volumetric flask, and deionized water was added. The pH was measured again and eventually adjusted by adding a few drops of ammonia. Thereby, the concentration of Zn^{2+} was fixed to 0.4 M, and the pH value was adjusted to 9.86 ± 0.01, 10.00 ± 0.02 and 10.39 ± 0.02, respectively. Finally, the ink was passed through a Satorius Minisart syringe filter (hydrophilic, 0.2 µm).

Laser printing instrumentation: A Ti:Sa femtosecond laser (Coherent, Chameleon Ultra II) was used for multi-photon printing of Pt and Ag. A 532 nm continuous-wave laser (Coherent, Verdi-V5) was used for the photothermal synthesis of ZnO. The power of the two lasers was controlled with two acoustic-optic modulators (AA Opto Electronic, MTS40-A3–750.850, and MT80-A1,5-VIS, respectively). The two laser beams were combined by means of a dichroic mirror and focused onto the ink-substrate interface by using an oil-immersion microscope objective lens (Zeiss, Plan-APOCHROMAT $100 \times /1.4$ Oil) for Pt, and a water-immersion microscope objective lens (Zeiss, LD C-APOCHROMAT $100 \times /1.25$ W) for ZnO and Ag. The objectives were mounted on a piezoelectric stage (Physik Instrumente, P-733.ZCL) with "100 µm" travel to translate the focus along the optical axis. The sample was translated horizontally using a combination of a piezo stage (Physik Instrumente, P-734.2CL, "100 µm × 100 µm" travel) and a motorized stage (Physik Instrumente, P-M-686, "25 mm × 25 mm" travel). It is important to find the correct position of the ink-substrate interface during the writing procedure, which was realized with high accuracy via a confocal detection scheme. In this interface-finding process, we scanned a focused probe laser (at 675 nm wavelength) with respect to the glass substrate along the z-direction in a range of a few micrometers. The position of the maximum of the reflected light power versus the z-position was taken as the interface position. To monitor the printing process in situ, we used a camera and light illumination in transmission

by a red light-emitting diode.

A.4 Material Characterization Methods

Different material characterization methods were used to gain insight information on printed memristors:
X-ray diffraction (XRD): XRD was used to investigate the crystalline information of the active layer materials. Instruments used in this thesis: (a) STOE Stadi P diffraction equipped with a Ga=jet X-ray source (Ga-Kα radiation, $1.2079\,$Å). (b) Bruker D8 Advanced Powder Diffraction.
Atomic Force Microscopy (AFM): AFM was used to characterize the surface properties of printed films, e.g., surface roughness. The measurements were performed in the tapping mode in the air condition using a silicon cantilever (HQ: NSC15/AL BS, MikroMasch). Instruments used in this thesis: Bruker Dimension Icon Atomic Force Microscope.
Scanning Electron Microscopy (SEM):
Transmition Electron Microscopy (TEM)/ Scanning TEM (STEM): TEM imaging, selected area electron diffraction (SAED) as well as STEM imaging and spectroscopy were performed on a FEI Osiris operated at $200\,\mathrm{kV}$ and equipped with a Super-X energy dispersive X-ray spectroscopy (EDS) detector. TEM bright-field images and SAED diffraction patterns have been recorded with a Gatan US1000, STEM BF and high-angle annular dark-field imaging was performed at a semi-convergence angle of $10.7\,\mathrm{mrad}$ and a camera length of $115\,\mathrm{mm}$, corresponding to an acceptance angle of $55\,\mathrm{mrad}$ to $200\,\mathrm{mrad}$ for HAADF. EDS data was evaluated with Bruker Esprit 2.3.
Device cross-section preparation: To prepare the cross-sectional sample, the Memristor structure on glass was first sputtered with $5\,\mathrm{nm}$ Pt, using a Leica ACE600 sputtercoater. The device of interest was localized using SEM in a FEI Strata 12672S DualBeam FIB-SEM. To protect the thin film during lamella preparation, a protective platinum layer of $20\,\mu\mathrm{m} \times 2\,\mu\mathrm{m} \times 0.1\,\mu\mathrm{m}$ was deposited

by electron beam induced deposition (EBID) and subsequently a slightly larger patch with height of $4\,\mu\mathrm{m}$ was deposited by ion beam induced deposition (IBID). Trenches close to the protective Pt patch were milled by $30\,\mathrm{kV}$ Ga-ions on both sides of the tentative lamella. Then, the pre-thinned lamella was cut free, welded to the tip of an Omniprobe manipulator, and attached to an Omniprobe copper grid. In a final step the lamella was thinned from the initial thickness of ca. $3\,\mu\mathrm{m}$ down to electron transparency ($< 100\,\mathrm{nm}$ thickness) by Ga-ions with energies of $30\,\mathrm{kV}$, $16\,\mathrm{kV}$, and $5\,\mathrm{kV}$. The final lamella was used for investigation in TEM.

A.5 PUF Calculation

With the obtained read currents over time, the PUF core's bit errors were calculated, according to equation A.1, where $R_{\mathrm{ref},n}$ being the n-th (here, $n = 1$), L-bit long reference response and $R'_{n,w}$, the W-times ($W = 300$) regenerated response.

$$\mathrm{BE}_n = \frac{1}{W} \sum_{w=1}^{W} \frac{\mathrm{HD}(R_{\mathrm{ref},n}, R'_{n,w})}{L} \cdot 100\% \tag{A.1}$$

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Acronyms and symbols

Acronyms

AE	Active Electrode
AFM	Atomic Force Microscopy
BT	Bottom Electrode
BE	Bit Error
CMOS	Complementary Metal-oxide Semiconductors
CC	Compliance Current
CF	Conductive filament
CE	Counter Electrode
CBRAM	Conductive Bridging Random Access Memory
CPU	Central Process Unit
CRP	Challenge Response Pair
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
DC	Direct Current
DEMUX	Demultiplexer

ECM	Electrochemical Mechanism
EDX	Energy Dispersive X-ray spectroscopy
EHD	Electrohydrodynamic
EGT	Electrolyte-gated Transistor
FET	Field-effect Transistor
FeRAM	Ferroelectric Random Access Memory
FeFET	Ferroelectric Field Effect Transistor
FTJ	Ferroelectric tunnel junction
GND	Ground
HRS	High Resistive State
HAADF − STEM	High-angle Annular Dark-field Scanning Transmission Electron Microscopy
HRTEM	High-resolution Transmission Electron Microscopy
HPE	Hybrid Printed Electronics
IRS	Intermediate Resistive State
IoT	Internet of Things
LED	Light-emitting Diode
LRS	Low Resistive State
MIM	Metal-Insulator-Metal
MRAM	Magnetic Random Access Memory
MOSFET	Metal Oxide Semiconductor Field-effect Transistor

MUX	Multiplexer
NDR	Negative Differential Resistance
OE	Ohmic Electrode
PE	Printed Electronics
PUF	Physical Unclonable Function
PCM	Phase Change Memory
PPF	Paired Pulse Facilitation
PSC	Post-synaptic Current
ReRAM	Resistive Random Access Memory
RRAM	Resistive Random Access Memory
RT	Room Temperature
RS	Resistive Switching
RTN	Random Telegraph Noise
SRAM	Static Random Access Memory
SEM	Scanning Electron Microscopy
SE	Schottky Electrode
SCLC	Space-charge-limited Conduction
SMU	Source Measure Unit
SA	Sense Amplifier
TEM	Transmission Electron Microscopy
TE	Top Electrode
TCM	Thermalchemical Mechanism

TRNG	True Random Number Generator
TCSCLC	Trap-controlled Space-charge-limited Conduction
VCM	Valence Change Mechanism
XRD	X-ray Diffraction
3D	Three dimension

Latin symbols and variables

Ag	silver
Au	gold
C	capacitance
Ca^{+}	calsium ion
$e^{'}$	electron with single negative charge
f	frequency
G	conductance
i	current
L	inductance
M	memristance
$\mathrm{Me}^{\mathrm{z}+}$	metal ion with z positive charge
$\mathrm{O_o}^{\mathrm{x}}$	lattice oxygen ion with neutral charge
Pt	platium
q	charge
$R_{\mathrm{off}}/R_{\mathrm{on}}$	ratio between high- and low-resistance

R	resistance
R_q	root mean square roughness
s	standard deviation of the sample
t	time
v	voltage
$\mathrm{V_o^{\cdot\cdot}}$	oxygen vacancy with double positive charge
$\mathrm{V_o}$	oxygen vacancy in simplified form
$\mathrm{WO_{3-x}}$	tungsten oxide
ZnO	zinc oxide
w	state variables determine the resistance of the memristor
W	the width of the Schottky barrier
$\overline{x}$	mean of the sample

Greek symbols and variables

β	stretching index
Δt	interpulse time interval
φ	magnetic flux
ϕ_B	Schottky barrier height
ϕ_M	work function of metal
μ	mean of the population
σ	standard deviation of the population
τ	characteristic relaxation time

χ_S	electron affinity of semiconductor

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