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A Stage-Gate Framework for Upscaling of Single-Junction Perovskite Photovoltaics

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To address the challenge of upscaling single-junction perovskite photovoltaics (PV) toward market-relevant performance in a structured and efficient manner, a stage-gate approach that divides the process into stages according to technology readiness levels (TRLs) is proposed. Whereas the first stage contains only material research, the later stages are concerned with the development from lab-scale devices to large-area modules, and properties such as device size as well as processing methods are adapted step-by-step toward commercializable techniques. The stages are connected by gates that specify the criteria that must be met for a material or process to be transferred to the next stage. In addition, a literature survey for the keywords "perovskite" and "module" is performed. This analysis shows that most of the reported modules have an area between 10 cm^2 and 20 cm^2, corresponding to stage 3 or TRL 5 in the scheme, and operational stability is often incompletely reported. These findings analysis indicate a significant gap in the research focus on large-area modules and elevated stress and field tests, which are essential for transitioning to commercial applications. It is suggested to use the proposed stage-gate process as an efficient and structured guideline toward commercializing perovskite PV.

1. Introduction

Perovskite PV has experienced a rapid increase in certified record values for the power-conversion efficiency (PCE) of solar cells as well as modules. The certified record PCE for single-junction perovskite solar cells (PSCs) has reached 26.1%.[1] This value is frequently compared to that of the best silicon (Si) solar cells (27.1%[1]) and used as evidence for the relevance and potential of perovskite PV. While halide perovskites have undeniably closed the efficiency gap to the decades older Si technology, the comparison has an obvious caveat: the area of the PSC is 0.05 cm^2 and the area of the Si solar cell is 243 cm^2. The corresponding value for perovskite modules is 20.6%, obtained for an area of 215.5 cm^2[2] which compares to a Si module record of 24.9% for an area of 1.77 m^2.[2] Thus,

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from the perspective of perovskite photovoltaics, there are still significant gaps to close. There is an efficiency gap for equal device area, a significant cell-to-module gap, and an additional (more difficult to quantify) device-stability gap that suggests that there are still scientific and technological challenges to push the technology toward commercialization.[3–5]

One of the critical challenges in scaling up perovskite PV is the transferability of perovskite film deposition from inert conditions to a controlled environment when using printing techniques.[6] In laboratory settings, perovskite films are often deposited under inert conditions to obtain high-quality films enabling excellent PCEs.[7] Printing techniques, such as inkjet printing and slot-die coating, require precise control over environmental conditions to ensure uniform film formation. Maintaining the same film quality and morphology in a controlled environment involves addressing issues such as moisture and oxygen sensitivity, solvent evaporation rates, and film crystallization dynamics. Additionally, ensuring the reproducibility of film deposition across large areas is challenging due to the increased susceptibility to environmental fluctuations.[8]

Finally, device stability is a significant challenge, especially for perovskite modules. Compared to small-area cells, there are additional failure mechanisms, for instance, due to the damage caused by laser patterning, the interaction between the materials in the device and the encapsulation material, or reverse bias caused by partial shading of series-connected modules in operation.[9]

Module fabrication poses a challenge with regard to cost effectiveness because of the higher material consumption and larger investment for the fabrication equipment. Therefore, we propose a so-called stage-gate process as a systematic approach to guide the development of single-junction perovskite PV in accordance with the Technology Readiness Level (TRL). The term stage-gate refers to an approach in which the development of a certain process or product is divided into defined steps (so-called stages) and in which a certain number of criteria (so-called gates) are required to progress from one stage to the next.

We believe that these clear guidelines will provide significant benefits to the community by accelerating progress, reducing costs, and enhancing comparability between different research institutes. For instance, the fabrication of large modules with materials that are inherently unstable or incapable of achieving high PCE due to high recombination rates or poor transport properties is not meaningful. TRLs are a method for assessing the maturity of a particular technology, ranging from early research stages (TRL 1) to fully operational systems (TRL 9). NASA introduced TRLs in the 1970s to assess the maturity of space technologies.[10] Over the years, TRLs have been adopted by various organizations and industries, including the European Commission for Horizon 2020.[11] For perovskite PV, TRLs became pivotal around the early 2010s, as the technology showed promise in lab-scale efficiencies. The term stage-gate process originally refers to a project management technique in which the development of a complex project is divided into several phases or stages, and the decision to move from one stage to the next is based on a list of objective criteria that have to be fulfilled.[12] In our proposed scheme, all gate criteria must be fulfilled simultaneously to take into account their possible interdependence.

After introducing the general concept and the details of this approach, we conducted a literature survey to analyze the extent to which research groups adhere to these guidelines, and at which TRLs the current academic research is conducted. Out of the large number of parameters that are relevant for the stage-gate process, we focus this analysis on the PCE and active area because these parameters are reported in every manuscript and are easy to extract. The analysis shows that the majority of the research is performed on modules with an active area smaller than 200 cm^2, corresponding to stage 3 and TRL5 in our definition.

We hope that our proposed stage-gate process will encourage the community to follow a more structured approach for perovskite upscaling and conduct more research in advanced stages at higher TRL levels.

1.1. Description of the Approach

To systematize the scale-up of single-junction perovskite PV, we propose a stage-gate process adapted from a similar scheme developed for the upscaling of organic photovoltaics[13] and adapt it to perovskite PV. An overview of the different stages and gates is shown in **Figure 1**, with the relevant properties shown in rows and the different stages or gates shown as columns. The definition of TRLs according to the European Commission[14] and the adaptation for perovskite PV is shown in Table S1 (Supporting Information). The highest TRL that we consider is TRL 7, because we want to focus on the research and development performed in academic institutions. Stage 1 is restricted to material investigation without any device fabrication, and stages 2–5 are related to device fabrication at different levels of upscaling.

The general concept is that, to progress from lower to higher TRLs, the various parameters and processing conditions are adapted toward higher TRL step by step. The most easily understandable quantity in this respect is the device area: in our scheme, stages 1 and 2 require no specification, stage 3 requires cells or minimodules with a size of at least 1 cm^2, stage 4 requires submodules with at least 200 cm^2, and stage 5 requires small modules with at least 800 cm^2. These criteria follow the definitions in the NREL efficiency chart.[2]

Because, as mentioned above, stage 1 is only related to materials and not to devices, it has some distinct differences concerning the properties that are investigated during the stage and that need to be met for the gate. Most importantly, a material

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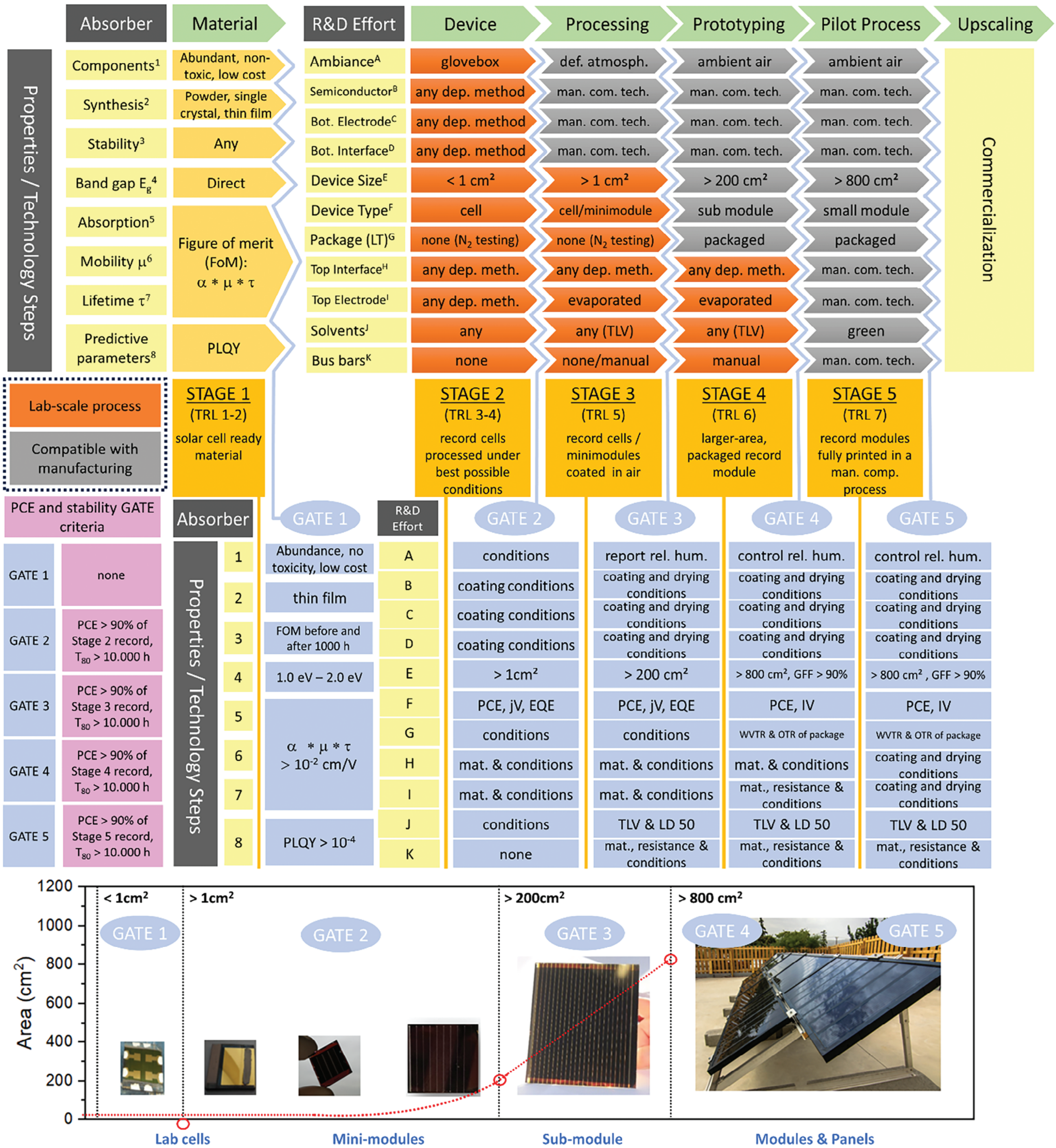

Figure 1. Overview of the proposed stage-gate process with the requirements for each stage and each gate stated in the respective fields. Conditions related to lab-scale fabrication are colored orange, whereas conditions related to large-area processing are colored gray. If not specified otherwise, a certain term such as "coating and drying conditions" means that these conditions should be reported without any explicit requirement that has to be fulfilled. The additional specifications for gate 1 are listed in **Table 1**, and the specific gate criteria for PCE and operational stability are listed in **Table 2**. The figure was created using some material from.[19]

Table 1. Specification of criteria for gate 1.

Property	Definition/measurement methods
abundance	Amount of material to fabricate $1TW_p$ has to exist
Low cost	$<10c/W_p$
toxicity	According to the guidelines of the European Union
Absorption coefficient α	Transmission measurements in the UV and visible region
Carrier mobilities μ	Terahertz pump-probe spectroscopy,[20] transient microwave conductivity,[20] Hall measurement[21]
Carrier lifetime τ	Transient photoluminescence,[22] Terahertz pump-probe spectroscopy, transient microwave conductivity

should exhibit a high absorption coefficient α, good charge carrier mobility μ, and a high lifetime τ to ensure good charge generation, good transport, and low recombination in a solar cell.[15] These criteria are summarized in a figure of merit defined as the product of α, μ, and τ that should be close to 1 for an ideal solar cell material.[16] Other important parameters are the photoluminescence quantum yield (PLQY) of the single film as another evidence for low non-radiative recombination, the band gap E_g, the stability of the pure material, the morphology (where the possibility to deposit the material as a thin film will be essential to move to the next stages of solar cell fabrication), and finally the abundance, non-toxicity, and low cost as a prerequisite for economic viability.

The subsequent stages 2–5 are related to the upscaling of devices and therefore enforce additional constraints on the processing conditions and device architecture. Lab-scale coating methods such as spin-coating are replaced by manufacturing-compatible technologies such as slot die coating between stages 2 and 3 for the absorber, bottom electrode, and bottom interface, and between stages 4 and 5 for the top interface and top electrode. While slot-die coating is usually considered the most suitable technology for up-scaling due to its high throughput of up to several 100 m/min, we have chosen the more general term "manufacturing-compatible" as companies might choose other methods based on technological and financial criteria.

The further parameters and conditions that are addressed in the stage-gate process are the environmental conditions (inert atmosphere in a glove box in the earlier stages, ambient air in the later stages), packaging (only required at later stages), solvents used for the whole process, including cleaning and waste (no requirements in the early stages, green solvents at the last stage), and bus bars (none at the earliest stage, manual fabrication in the intermediate stages, and manufacturing-compatible technology at the last stage). For a certain process to transition from one stage to the next, certain gate criteria must be met for every parameter. The gates are the latest point at which a certain challenge needs to be solved – for instance, it is already meaningful to work on green solvents in stages 2 and 3, but it is not a requirement for gates 2 and 3. In most cases, the gate criteria are equivalent to reporting the conditions that were used in a certain stage to verify that they meet the criteria, such as environmental conditions, coating and drying conditions, or area. As quantitative indicators, we propose minimum values for the PCE and stability: at each gate, the achieved PCE should be within 90% of the record value reported in the literature for this particular stage. Light management structures can be used to achieve these PCE values, but they must be specified along with the other gate criteria.

In addition to PCE, operational stability needs to be considered at the different gates, as it is an equally important prerequisite for commercialization. Our recommendation is to record the PCE both under one sun and under 85 °C in the dark over time as absolute values and that the required time after which the PCE has decreased to 80% of its initial value (T_{80}) should be larger than 10.000 h. If it is not practical to measure for 10.000 h, this value can be obtained from extrapolation after the initial burn-in period is over.[17] Alternatively, higher light intensities[18] can be used to achieve the equivalent photon dose of one sun after 10.000 h. For gate 4, we propose to add outdoor measurements according to ISOS-O as a requirement[17] to fulfill the definition of TRL 6 as "Technology demonstrated in a relevant environment", and for gate 5, we recommend to perform these outdoor measurements with a string of ≈20 modules of the required size (corresponding to a total area of at least 1.6 m^2) connected to an inverter, to fulfill the definition of TRL 7 as "System prototype demonstrated in a relevant environment". All the reports concerning PCE and stability should contain the statistics of the respective experiment.

Additional criteria for gate 1 that are not contained in Figure 1 are summarized in Table 1 , and Table S1 (Supporting Information) summarizes the abbreviations that were used in Figure 1.

Table 2. Gate criteria for device properties and stability. All these reports should contain the statistics of the respective experiments.

Gate	Requirements
1	Report FoM before and after 1000 h under one sun & in the dark at 85 °C
2	Report PCE, jV, and EQE before and after 1000 h under one sun & in the dark at 85 °C
3	Report PCE, jV, and EQE before and after 1000 h under one sun & in the dark at 85 °C
4	Report PCE and IV before and after 1000 h under one sun, in the dark at 85 °C & outdoor
5	Report PCE and IV before and after 1000 h under one sun, in the dark at 85 °C & outdoor

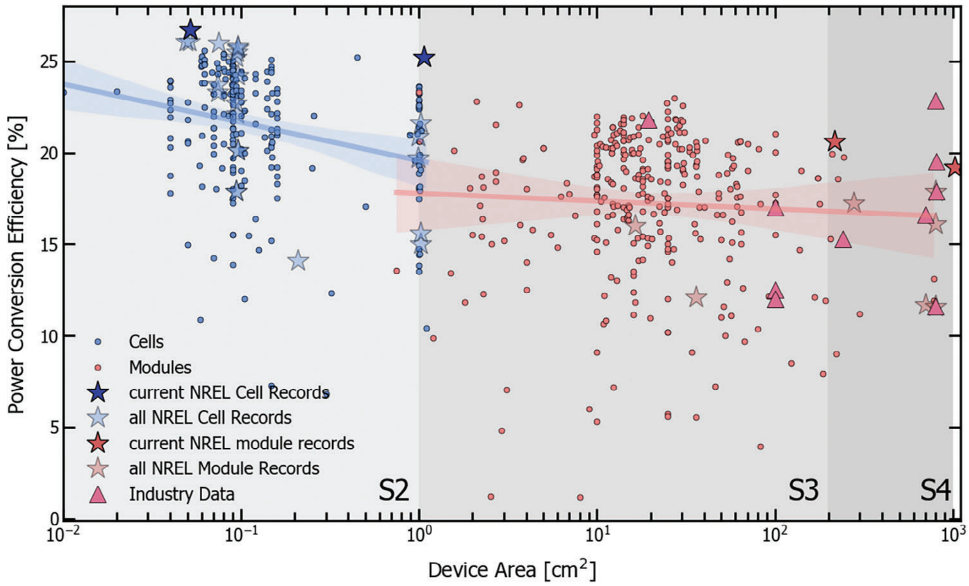

Figure 2. PCE versus area as the result of a literature search based on the keywords "perovskite" and "module". The data labeled as "cells" refers to small-area reference devices fabricated with the same recipe. The stages defined in Figure 1 are indicated versus the area where applicable. A regression is shown as a colored line with the uncertainty (99% confidence interval) as the shaded area. NREL records and additional industry data[9] are also indicated in the plot.

1.2. Discussion/Literature Review

To analyze to which extent current research is aligned with our proposed stage-gate process, we have conducted a keyword search for "module" and "perovskite" in the Scopus database, limited to publication years 2022 – 2024. As of July 2024, this search resulted in 798 hits. Out of these 798 publications, 287 presented new experimental data of single-junction perovskite modules and were analyzed for this study. The other articles are review papers and theoretical studies, present tandem devices or lack some information about the area.

For the 287 publications, PCE and device area were manually extracted for all devices, resulting in 317 different value pairs for module PCE and area. Furthermore, stability data was extracted if the PCE under one sun illumination was measured for at least 1000 h, which was the case for 116 out of the 317 value pairs. With this definition of stability, we follow the requirements outlined in[23] and the ISOS-L-1 standard. Even though the stage-gate process involves many more parameters, we limited our analysis to the ones just mentioned, because they are consistently reported. Parameters such as PCE and active area are often included in the abstract, allowing us to complete the manual search relatively quickly. For comparison, the equivalent Scopus search for the single keyword "perovskite" yielded 36.439 hits on July 12th, 2024. This number is no longer suitable for manual analysis and would require an automated analysis, for instance with Large Language Models (LLMs). We did not perform additional filtering for properties such as E_g or top electrode, since we wanted to provide a picture with as little bias as possible. The results of this analysis are shown in **Figures 2** and **3** and Figures S1 and S2 (Supporting Information). Most publications contain two or even three data points of small-area reference cells on the one and modules with larger areas on the other hand, differentiated by color in the plots. The data for small-area cells was included with the goal of achieving the best comparability between the cell and module levels. Figure 2 displays the PCE over the device area with the NREL record values indicated as a reference, revealing that cells were most commonly fabricated with an area of 0.1 cm^2, whereas the most common module area is ≈10–20 cm^2. This means that a large majority of the modules can be classified as stage 3 if the area is considered as the sole criterion. Figure 2 also reveals a substantial number of publications with PCE values below 10%, most of these corresponding to non-standard absorbers (for instance high E_g or lead-free perovskites).

The linear regression performed on the data points gives an indication of different upscaling losses: the rate of PCE decrease with increasing area is less pronounced for modules (≈1% per scaling factor of 100) than for the cells (≈4% per scaling factor of 100).

Whereas more than 300 data points correspond to areas below 200 cm^2, corresponding to stage 3, only eight publications report areas larger than 200 cm^2, corresponding to stage 4, and there are no publications corresponding to stage 5, i.e. for module areas larger than 800 cm^2. There is only one publication that approaches stage 4 with module areas of 780 cm^2 equal to the gate value of 800 cm^2, showing that most perovskite research published in academic journals is still at low TRL levels. Another insight from Figure 2 is the PCE drop that is observed when moving from the cell to the module and with increased area. This overall PCE drop is quantified in Figure S1 (Supporting Information), where we have compared the reported modules with the corresponding reference cells by plotting the ratio of module PCE to cell PCE versus the factor with which the area was increased. This panel shows that the most common factor for area upscaling is ≈100, and that most modules have 80–90% of the single-cell PCE. Furthermore, we observed a slight correlation

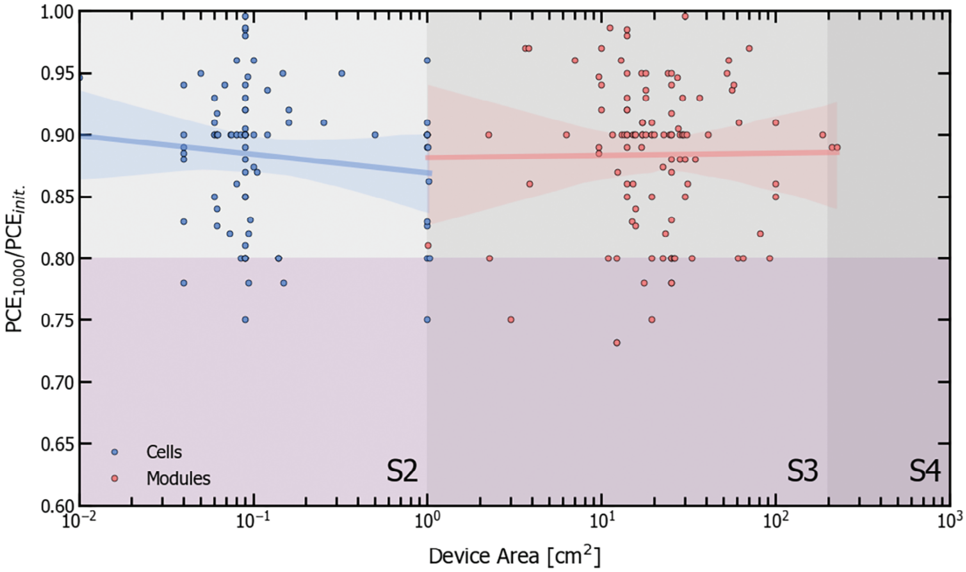

Figure 3. PCE loss (PCE after 1 h divided by initial PCE) versus device area as the result of a literature search based on the keywords "perovskite" and "module". The data labeled as "cells" refers to small-area reference devices fabricated with the same recipe. The stages defined in Figure 1 are indicated versus the device area, and values for which $PCE_{initial}/PCE_{1000}$ is smaller than 0.8 are indicated by darker shading to indicate the criterion of T_{80}. A regression is given as a colored line with the uncertainty (99% confidence interval) as the shaded area.

between the increase in area and the decrease in PCE. However, the spread in the data is again very large, and many outliers can be found.

In Figure 2, we have also included data from companies working on perovskite upscaling (based on the analysis in,[9] data summarized in Table S3, Supporting Information). These values are based on information available from the companies themselves (press releases etc.), not from peer-reviewed publications.

The analysis shows that, unlike the data points coming from academic institutions, modules are fabricated with areas between 100 and 1000cm^2, but also show a large spread of PCE between 12% and 21.8% at 1000cm^2. Two of the values, namely a PCE of 19.5% for an area of 810.1 cm^2 claimed by Wuxi Utmolight Technology, and a PCE of 22.66% for an area of 800.9 cm^2 claimed by Mellow Energy, are even higher than the corresponding NREL record (19.2% PCE for an area of 1027.1cm^2 by SolaEon). In addition, there is the claim of 19.04% PCE for a 2 m^2 module by Kunshan GCL Optoelectronic Material that is not shown in the figure, because it is outside of the area range that is found in our literature search.

Next, we analyzed the reported stability by plotting the remaining PCE after 1000 h (PCE_{1000}) divided by the initial PCE ($PCE_{initial}$) versus area (Figure 2) for both modules and reference cells. We have added a purple area at a T_{80} of 1000 h to indicate the stability requirements for all TRLs. We find many data points for the S2-3 regions, but none for S4, and we see a large spread of data, such that the uncertainty of the fitted trend (indicated by the shaded areas) is high. We find a slight negative correlation of device stability with the device area in small-scale devices and no trend in the module area. The former trend might be a consequence of sampling bias because the number of cells per substrate and batch is typically much larger for smaller cells, and only the most stable cells are reported. In Figure S2 (Supporting Information), we plotted the stability over the initial PCE. Both of these plots show a relatively large variation of the relative remaining PCE between 1.0 and 0.75, and find a positive correlation for both cells and modules – however again with a large spread.

After the analysis of the whole data set with respect to the most accessible criteria of PCE, active area, and stability, we examine a few exemplary data points to analyze the extent to which literature reports meet the remaining requirements of the stage-gate process. There is only one report of modules with areas close to 800 cm^2 corresponding to gate 4.[24] The reported PCE value of 13.1% is significantly below the record value of 19.2% given in the NREL charts. In addition, even though a T_{80} of ≈5000 h is reported for degradation in the dark under 85 °C, there is no data for the exposure to one sun or for outdoor degradation and no information about encapsulation. A similar consideration for gate 3 shows that there are a few publications with an area above or slightly below 200 cm^2 and a PCE approaching the reported record value of 20.6%.[25–27] Out of these, ref. [25] comes closest to the proposed stability requirements, reporting a T_{80} of more than 1000 h for one-sun illumination, whereas[26] reports only unsealed modules in ambient air with a T_{80} of ≈1200 h, and ref. [27] reports no stability data at all.

Finally, considering gate 2 with a required area of 1 cm^2 and a record efficiency of 26.39%,[28] several publications have reported values close to the gate criteria. For instance, ref. [29] presents a PCE of 22.6%, an active area of 3.63 cm^2, and a remaining PCE of 97% after 1000 h after one sun; ref. [30] reports a certified PCE of 22.72% for an active area of almost 24 cm^2 and a remaining PCE of 90% after 1500 h under one sun; ref. [31] presents a PCE of 22.97% for an active area of 27.22 cm^2 and a remaining PCE of 94.66% after 1000 h under one sun. This brief analysis reveals that although a substantial amount of research has been conducted up to stage 3, resulting in good performance in terms of PCE and stability, the number of published papers and the values reported significantly decrease in the higher stages.

To compare the above findings with similar information that is already available in the community, we extracted similar data from the Perovskite Database[32] and the Emerging PV Database,[33] as shown in Figures S3–6 (Supporting Information). These two databases have a slightly different scope compared to our analysis shown in Figure 2: The Perovskite Database aims to include data from all peer-reviewed publications, including processing conditions, whereas the Emerging PV database aims at publications showing "record" performance, where "record" is not limited to PCE but can also be related to other important performance parameters of Emerging PV devices, such as transparency, flexibility, or energy yield. As a result, the Perovskite Database contains significantly more data points than the Emerging PV database, which is clearly visible in the plot in Figure S3 (Supporting Information). At the moment, neither the Perovskite Database nor the Emerging PV database is designed to incorporate module data, meaning that they do not contain any information about parameters such as number of cells, specific details of the interconnect, etc. As a result, the plots generated from the Perovskite Database only contain very few data points for modules, whereas the plots generated from the Emerging PV database contain no data points for modules at all. For that reason, the statistical analysis for this data is restricted to cells and does not contain modules. The analysis of PCE versus area based on the Perovskite Database as well as the Emerging PV data suggests an almost constant PCE, but this is most likely because a larger range of PCE values are reported for small areas, whereas the values reported at 1cm^2 show a preselection for higher PCE values. Despite these limitations, the data generally supports our previous conclusion that there is a slight drop in PCE over area and that there is no obvious correlation between stability and initial PCE. With respect to the correlation between stability and active area, the plot from the Perovskite Database (Figure S4, Supporting Information) seems to suggest that stability increases with area, but this might be due to the small number and preselection of data points with a large area. Stability data from the Emerging PV database is not shown here because of the small number of datapoints.

These results indicate that while existing databases already serve the community, adding more publications and properties would allow a more comprehensive analysis. Currently, the extent of these databases is limited by the requirement for manual data entry. However, LLMs may soon be capable of directly extracting data from PDFs and structuring it for automatic uploads.

1.3. Conclusions and Recommendations

We proposed a stage-gate process as a structured approach for upscaling single-junction perovskite photovoltaics. With this contribution, we intend to start a discussion on a best practice stage-gate process that can be improved and adapted by the community for better alignment of the global research effort on perovskite photovoltaics.

This stage-gate process consists of five different stages, representing TRL levels from 1 to 7 and encompassing research performed in academia. Whereas stage 1 is restricted to investigating the properties of the absorber without any device fabrication, stages 2–5 are related to the upscaling of the technology from small-area cells to large-area modules. Between each stage, we propose a gate consisting of a number of properties that the device has to fulfill in order to make it suitable for the next stage. We believe that it is important to fulfill the complete list of criteria for a certain gate to account for their interdependency. For instance, it does not make sense to fabricate an 800 cm^2 module on a process that is inherently unstable. Another example would be to make a very robust encapsulation technique that, however, only works on small area cells.

To verify the extent to which our proposed approach corresponds to the research performed in academic institutions, we have performed a literature survey for the keywords "perovskite" and "module" and manually extracted the values for PCE, active area, and, if included, stability from 287 publications. This analysis shows that the vast majority of peer-reviewed publications were fabricated with an active area corresponding to stage 3, and only one publication was at the gate between stage 3 and stage 4. Stability data is only reported for a minority of the publications. We therefore, encourage the community to extend their research toward higher TRLs to enable the commercialization of perovskite PV and use the suggested stage-gate approach as a guideline and address all the issues that are relevant in addition to PCE. In this context, we believe that solving challenges related to upscaling should receive more recognition in high-impact factor journals.

We further encourage the community to record all relevant data in databases, thereby providing accurate tools to track the progress of the technology.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

commercialization, large-area, module, perovskites, upscaling

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