Compact and Power-Efficient RF Front-End Components for Beamforming Networks

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Zusammenfassung

Die neuesten Forschungsanstrengungen zur Gewährleistung der globalen Konnektivität sehen die Integration von terrestrischen, luftgestützten und satellitengestützten Kommunikationssystemen mit nahtloser Interoperabilität auf allen Ebenen vor. Phased Arrays, eine Schlüsseltechnologie für die elektronische Strahlsteuerung, kommen in jedem dieser Systeme zum Einsatz. Moderne Anforderungen treiben die Standards der nächsten Generation von Kommunikationssystemen zu höheren Betriebsfrequenzen. Der begrenzte verfügbare Abstand zwischen den Antennenelementen in einem Array führt zu strengen Flächenbeschränkungen für die elektronischen Komponenten des Strahlformungsnetzwerks. Zusätzlich wird bei Phased Arrays mit einer großen Anzahl von Elementen der hohe Stromverbrauch der IC-Komponenten aufgrund der damit verbundenen thermischen Herausforderungen zu einer weiteren kritischen Einschränkung. In dieser Arbeit werden Designtechniken zur Reduzierung des Flächen- und Stromverbrauchs untersucht, um eine kostengünstige und leichte industrielle Implementierung in hochintegrierten mm-Wellen-Systemen zu ermöglichen.

Es werden Miniaturisierungsstrategien diskutiert, beginnend mit passiven Strukturen, da diese in der Regel am meisten zum Gesamtflächenverbrauch der Schaltung beitragen. Es werden mehrere kompakte Geometrien für I/Q-Splitter vorgeschlagen, darunter ein differentieller 3D-Lange-Koppler und ein differentieller Spiralkoppler. Letzterer veranschaulicht auch die Performanzkompromisse, die mit einer engeren miniaturisierten Geometrie verbunden sind. Darüber hinaus werden gute Layout-Praktiken für andere Komponenten, wie z. B. mehrschichtige Induktivitäten und transformatorbasierte Impedanzanpassungsnetzwerke, erforscht und eingesetzt.

Als nächster Schritt wird in dieser Forschungsarbeit der Miniaturisierungsaufwand auf der Topologieebene des kompletten Phasenschiebers erweitert und vorgestellt. Es werden drei Designs im W-Band vorgestellt, die auf industrielle Spezifikationen für zukünftige terrestrische 6G-Systeme abzielen.

Alle Phasenschieber nutzen die Vektorsummierung als Phasenkontrollmechanismus, der eine hohe Phasenauflösung bei kompakter Bauweise bietet. Das erste Design basiert auf einer konventionellen Gilbert-Zelle, enthält aber einen zuvor vorgestellten kompakten differentiellen Lange-Koppler als I/Q-Splitter, ein LC-basiertes Ausgangsanpassungsnetzwerk und zwei Marchand-Baluns für die Single-Ended-Version. Die Integration dieser kompakten passiven Strukturen führt zu einer Chipfläche von 0,053 mm^2, die im Vergleich zu früheren akademischen Forschungspublikationen für dieselbe Betriebsfrequenz und Phasenauflösung deutlich kleiner ist. Die nächste Design-Iteration führt eine grundlegende änderung der Topologie der Gilbert-Zelle ein, die von der Blixer-Schaltung inspiriert ist. Bei diesem Ansatz wird die klassische Transkonduktanzstufe der Emitterschaltung g_m modifiziert, um einen integrierten aktiven Balun auf der Eingangsseite zu bilden. Gleichzeitig werden das Ausgangsanpassungsnetzwerk und die Balun-Funktionalität in einem Transformator kombiniert. Durch diese Modifikationen und die zuvor angewandten kompakten Layout-Strategien wird die belegte Fläche weiter auf 0,026 mm^2 reduziert. Der dritte Entwurf schließt das Kapitel ab, indem er verschiedene Ansätze für den bidirektionalen Betrieb erweitert und einige der besten Eigenschaften von aktiven und passiven Phasenschiebern in einem einzigen schalterlosen Block kombiniert. Dies wird erreicht, indem der Koppler und die Transformatoren für beide Signalrichtungen wiederverwendet werden und nur der Transistorkern verdoppelt wird. Alle Entwürfe wurden auf dem Wafer charakterisiert, und ihre Funktionalität wurde erfolgreich bestätigt.

Das nächste Kapitel befasst sich mit der Satellitenkommunikation als einem der Elemente der zukünftigen Beyond-5G-Infrastruktur. Die Spezifikationen und Entwurfsziele spiegeln die globalen Forschungstrends in diesem Bereich wider, einschließlich der Q- und V-Band Frequenzbereiche. Es wurde ein Subsystem für selbstkalibrierende Satellitenkommunikationssysteme entwickelt, wobei der Schwerpunkt auf einer großen Bandbreite und einem großen Dynamikbereich liegt. Da die belegte Fläche in der Raumfahrtanwendung ein noch größeres Problem darstellt, wurden die Miniaturisierungsbemühungen auf der Kettenebene durch Überdenken der Rollen und zusätzlichen Funktionen der Bausteine fortgesetzt. Als Ergebnis wird ein Blixer-basierter Phasenschieber für eine quasi-unabhängige Phasen- und Verstärkungsteuerung verwendet, der einen Übergang vom single-ended zum differentiellen Signal zwischen dem LNA und den folgenden VGA-Stufen bereitstellt. Darüber hinaus ermöglicht eine VGA-Stufe mit einem Resonator zwischen dem positiven und dem ne-

gativen Pfad sowohl die Verstärkungsteuerung als auch die Anpassung der Verstärkungssteigung. Durch die Integration mehrerer Funktionen kann daher die Gesamtzahl der erforderlichen Komponenten minimiert werden.

Das letzte Kapitel befasst sich mit Low-Power-Designs und den damit verbundenen Performanzkompromissen. Zur Beurteilung der akzeptablen Leistungsreduzierung werden zwei zweistufige *W*-Band-LNAs – ein Design mit optimaler Leistung und ein Design mit geringem Stromverbrauch – vorgestellt und quantitativ verglichen. Eine weitere Komponente des *W*-Band-Empfängers, die in diesem Kapitel vorgestellt wird, ist ein Mischer mit integriertem Spiegelfrequenzunterdrückungsfilter. Abhängig von den Anforderungen an die Spiegelfrequenzunterdrückung und dem Strahlformungsschema kann dieses Design als stromsparende, kompaktere Alternative zu den üblicherweise verwendeten Quadraturmischern dienen. Alle drei Schaltungen wurden charakterisiert, und die erzielten experimentellen Ergebnisse bestätigen die Gültigkeit der vorgestellten Ideen und Überlegungen.

Abstract

The latest research efforts to ensure global connectivity envision the integration of terrestrial, airborne, and satellite communication systems, with seamless interoperability across all layers. Phased arrays, a key technology for electronic beam steering, are utilized in each of these systems. Modern demands push the standards of next-generation communication systems to higher operational frequencies. Consequently, the limited available spacing between antenna elements in an array imposes strict area constraints on the electronic components of the beamforming network. Additionally, in phased arrays with a large number of elements, high power dissipation of IC components becomes another critical limitation due to the associated thermal challenges. This thesis investigates design techniques for area and power reduction to enable potential low-cost and lightweight industrial implementation and feasibility in highly integrated mm-wave systems.

Miniaturization strategies are discussed, beginning with passive structures since they typically contribute the most to overall circuit area consumption. Several compact geometries for I/Q splitters are proposed, including a 3D differential Lange coupler and a differential spiral coupler. The latter also exemplifies performance trade-offs associated with tighter miniaturized geometry. Additionally, good layout practices for other components, such as multi-layer inductors and transformer-based impedance matching networks, are explored and employed.

As the next step, this research work expands and presents the miniaturization effort on the topology level of the complete phase shifter. Three designs are presented in the *W*-band, targeting industrial specifications for future terrestrial 6G systems. All phase shifters utilize vector summation as the phase control mechanism, which offers high phase resolution within a compact footprint. The first design is based on a conventional Gilbert cell but incorporates a previously presented compact differential Lange coupler as an I/Q splitter, an LC-based output matching network, and two Marchand baluns for the single-ended versi-

on. The integration of these compact passive structures results in a die area of 0.053 mm^2, significantly smaller compared to prior academic research publications for the same operating frequency and phase resolution. The next design iteration introduces a fundamental modification to the Gilbert cell topology, inspired by the Blixer circuit. In this approach, the conventional CE g_m-stage is modified to form an integrated active balun on the input side. Simultaneously, the output matching network and the differential-to-single-ended conversion are combined in one transformer. These modifications, along with previously employed compact layout strategies, further reduce the occupied area to 0.026 mm^2. The third design concludes the chapter by expanding various approaches to bidirectional operation, combining some of the best properties of active and passive phase shifters into a single switchless block. This is achieved by re-using the coupler and transformers for both signal directions and only doubling the transistor core. All designs have been characterized on-wafer, and their functionality has been successfully confirmed.

The next chapter focuses on satellite communication as one of the elements in future beyond-5G infrastructure. Specifications and design goals reflect global research trends in this field, including frequency range of interest in the *Q*- and *V*- band. A subsystem for self-calibrating satellite communication systems has been developed with the focus on broad bandwidth and large dynamic range. As occupied area imposes even larger concern in space application, miniaturization efforts on the chain level, have been made by reconsidering the roles and additional functions of the building blocks. As a result, a Blixer-based phase shifter is used for quasi-independent phase and gain control, providing a single-ended to differential transition between the LNA and the following VGA stages. Additionally, a VGA stage with a resonator between the positive and negative branches enables both gain control and gain slope adjustment. Integrating multiple functions, therefore, allows for minimizing the total number of required components.

The final chapter explores low-power designs and the associated performance compromises. To assess acceptable levels of power reduction, two two-stage *W*-band LNAs – an optimum-performance design and a low-power design – are presented and quantitatively compared. Another *W*-band receiver component discussed in this chapter is a down-conversion mixer with an integrated image-reject filter. Depending on image rejection requirements and the beamforming scheme, this design can serve as a low-power, more compact alternative to

commonly-used quadrature mixers. All three circuits have been characterized, and the experimental results obtained confirm the validity of the presented ideas and considerations.

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Kateryna Smirnova

Contents

Acronyms and Symbols

Acronyms

BEOL	back end of line
BiCMOS	bipolar CMOS
CB	common-base
CE	common-emitter
EM	electromagnetic
FoM	figure of merit
HBT	heterojunction bipolar transistor
IHE	Institute of Radio Frequency Engineering and Electronics
IHP	Leibniz Institute for High Performance Microelectronics
IRR	image rejection ratio
KIT	Karlsruhe Institute of Technology
LNA	low-noise amplifier
NF	noise figure
PA	power amplifier
PS	phase shifter
Rx	receiver

SiGe	silicon germanium
Tx	transmitter
VGA	variable gain amplifier

Constants

$\pi = 3.14159..$	Pi
$c = 299\,792\,458$ m/s	Speed of light in vacuum

Latin Symbols

f	Frequency
IP3	Third-order intercept point
IMD3	Third-order intermodulation distortion
$P_{1\mathrm{dB}}$	1 dB compression point
P_{DC}	Power consumption

Greek Symbols

λ	Wavelength
φ	Phase
θ	Phase control setting; beam direction
ω	Angular frequency

1 Introduction

1.1 Phased Arrays in Advanced Wireless Communication

The fifth generation (5G) and future beyond-5G mobile communication networks in contrast to previous generations move higher in operating frequencies utilizing mm-wave bands. The large number of unlicensed and therefore less crowded bands as well as their larger absolute available bandwidth leading to higher achievable data rates are some of the most attractive features. Whereas 5G bands assigned in some countries include K_a (27−40 GHz), Q (33−50 GHz), and E-band (60−90 GHz) frequencies [HJY+21], the ongoing research in 6G systems development foresees the use of higher frequencies, such as W-band (75−110 GHz) and even reaching the sub-THz frequency range. Some of the foreseen 6G applications include autonomous unmanned vehicles, smart cities and massive Internet of Things.

Phased arrays are integral to modern communication systems, driving critical advancements in high-frequency wireless technologies. By enabling electronic beam steering, phased array technology provides precise and efficient directional communication. This capability is particularly valuable in environments with high user density and complex signal propagation, such as urban areas and satellite networks. The ability to dynamically form and steer beams, combined with techniques such as spatial diversity and spatial multiplexing [Mas17], is a key enabler of 5G and likely future generations of communication systems.

1.1.1 Principle of Operation

The use of phased arrays in mm-wave communication systems offers significant advantages compared to single antenna systems. Increasing with frequency

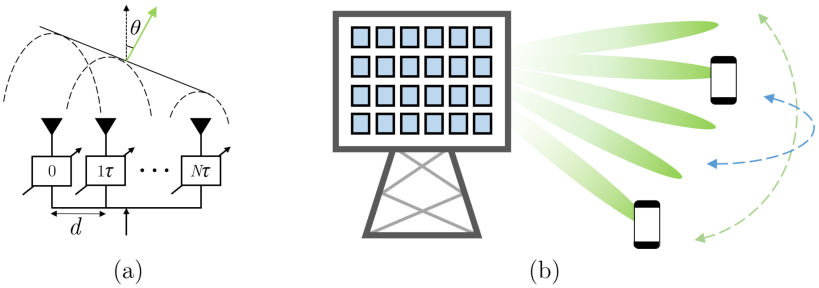


Figure 1.1: Uniform linear phased array (a) and 2D beam steering example (b).

propagation loss requires higher transmitter output power. Instead of a single high-power power amplifier (PA), a set of relatively low-power PAs in an array configuration exhibits improved energy efficiency by distributing the power requirements across the system [CA20]. The power usage is further optimized by focusing the radiated energy in narrower beams. For example, for a uniform N-element linear array (Fig. 1.1a) with a distance d between the elements, the 3-dB beamwidth θ_B vs. the beam steering angle θ is approximated as $\theta_B = \frac{0.886\lambda}{Nd\cos\theta}$ [Mai94]. Hence, more elements will narrow the radiated beam.

At the receiver side, the use of phased arrays leads to improved signal-to-noise ratio, due to coherent signal combining and the uncorrelated nature of noise [GHH04] [Ma16].

One key property of phased arrays is their beam steering capability. In essence, it means the ability to adjust the radiation pattern of an array, in other words, to electronically steer the beam. Variable time-delay control compensates for path length differences between each antenna element and the target direction and thus ensures a coherent signal combining at the desired angle. Additional amplitude control (tapering) can be applied to further adjust the radiation pattern shape, e.g. to reduce the side lobes. Therefore, phased arrays are capable of forming the main beam in the direction of the desired signal with reduced side lobes and providing eventually the null-steering (zero-forcing) in other directions, especially the direction of a known interferer.

For a single signal frequency, the required time delay difference $\tau = \frac{d\sin\theta}{c}$ translates into a phase shift difference of $\varphi = \omega\tau = \frac{2\pi d\sin\theta}{\lambda}$ (hence "phased"

array). For narrow-band systems the phase shift over the band can be assumed to be the same as for the center frequency of the band. For wide-band systems, an error occurs resulting in beam squint. To overcome this effect, one must use a true-time-delay functionality. This thesis focuses on phase-controlled phased arrays. More details on this choice are discussed in Chapter 3.

A beam steering example is schematically shown in Fig. 1.1b. Applying the same approach to a 2D array (e.g., on a base station) enables the beam steering in both vertical and horizontal planes.

1.1.2 Beamforming Architectures

Depending on the implementation, the beamforming can be categorized into three types: analog, digital, and hybrid (Fig. 1.2).

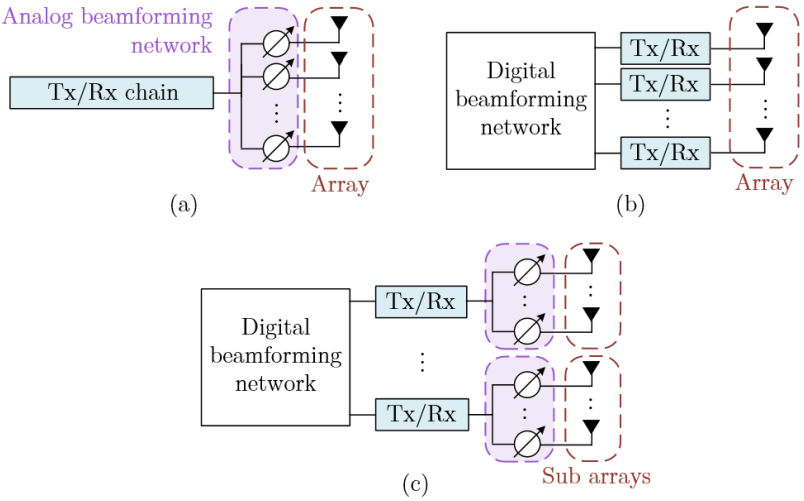


Figure 1.2: Analog (a), digital (b), and hybrid (c) beamforming.

Analog Beamforming

In systems using analog beamforming, the weighting and delay functionality is added to the signal in the analog domain. In most cases, this is done per antenna element to obtain maximum flexibility. However, column and/or row driven antenna panels are also in use, the weighting and delay functionality is then implemented for a group of antennas. Analog beamforming is a low-cost solution with low power consumption and lower complexity because after the signal summation operation or before the signal-split operation is completed, the remaining hardware is shared for all antenna elements (Tx/Rx chain in Fig. 1.2a). At the same time, this architecture suffers from several disadvantages. Signal combining in the analog domain excludes any additional data manipulations in the digital domain and thus limits the beamforming flexibility compared to the fully digital alternative. Limited bandwidth of analog phase shifters as key components for beam steering, in this case, results in reduced system's operational bandwidth. In addition, a conventional single array cannot generate multiple beams without employing complex techniques, such as splitting the array into sub-arrays based on the desired number of beams, which significantly increases overall hardware complexity. Moreover, mitigating the effects of undesired interaction between the beams may pose more challenges compared to digital beamforming, which can employ advanced algorithms for this purpose. However, analog beamforming is still the leading technique in communication systems, being cellular infrastructure or mobile handheld. A recent example is a joint concept for a sub-THz 6G system developed by Ericsson and Intel in 2023, where analog beamforming is anticipated to be the most likely scheme for a final implementation [PBE+23].

Digital Beamforming

In digital beamforming, each antenna has an individual dedicated RF chain, whereas the phase control is performed by digital baseband processing. In this case, mathematical algorithms can be used with maximum flexibility. This architecture can be used in both single- and multi-user scenarios, due to the ability to not only create multiple spatial streams simultaneously but also to reconfigure their number immediately if needed. However, such an attractive performance comes at the expense of increased cost and power consumption because of an increased number of components. Moreover, in receive mode, there is no early spatial filtering since the null-steering is performed in the digital domain. This means that all front-end components and ADCs are exposed

Table 1.1: Analog vs. Digital Beamforming

	Cost	P_{DC}	Simultaneous beams	Bandwidth	Accuracy
Analog					
Digital					

to potentially strong interferers from different directions [Sah]. This implies stricter linearity requirements to prevent signal distortion and therefore results in even higher power consumption. Required computational resources contribute to it as well, since the data that needs to be processed is proportional to the number of elements, number of beams, and instantaneous bandwidth of the signal. Digital beamforming has been used in conventional MIMO systems but may become too complex and expensive for both manufacturing and operation in massive MIMO systems, especially those using hundreds or more antenna elements.

Table 1.1 schematically summarizes the above-mentioned advantages and disagvantages of analog and digital beamforming.

Hybrid Beamforming

In essence, hybrid beamforming is an extension of the analog architecture to the multi-stream scenario. The main idea is to use a two-step procedure: analog signal processing within smaller sub-arrays (Fig. 1.2c) and digital signal processing with reduced dimensions (due to the reduced number of RF chains). Alternatively, analog and digital beamforming schemes can be applied to different scanning planes of an array − analog in the azimuth plane and digital for a coarser scan in the elevation plane. By combining the best features of analog and digital architectures, hybrid beamforming can be considered a promising trade-off solution. Some of the related research activities can be found in [MRH+17] and [IE19].

1.1.3 Analog Phase Shifting Configurations

Phase shifters are used in both analog and hybrid beamforming schemes and their position in a chain determines the corresponding phase shifting configuration. Fig. 1.3 explains three configurations, namely RF (a), IF (b), and LO (c) phase shifting. Such naming corresponds to the phase shifter location relative to a frequency conversion stage (mixer). In the following discussion, a receiver array is used as an example.

RF Phase Shifting

In the RF configuration, the phase shifting takes normally place after the received signal is amplified by a low-noise amplifier (LNA), but not down-converted in frequency yet. The phase shifting operation takes place on RF signals. This approach has multiple advantages, such as simplified LO distribution, overall reduced complexity and therefore the lowest area and power consumption. This is due to the phase-shifted signal combining implemented before the down-conversion, therefore, only one mixer and a corresponding LO source are required for the entire array. Disadvantages of this architecture include challenging phase shifter design at higher frequencies and a strong influence of its performance on the array functionality.

IF Phase Shifting

The use of a phase shifter after down-conversion at the intermediate frequency (IF) simplifies its design process in general but requires a separate mixer per antenna element and a complex LO distribution. In addition, another mixer is needed after such phase shifting for frequency conversion from IF to baseband, thus increasing the die area and power dissipation. The large footprint of passive

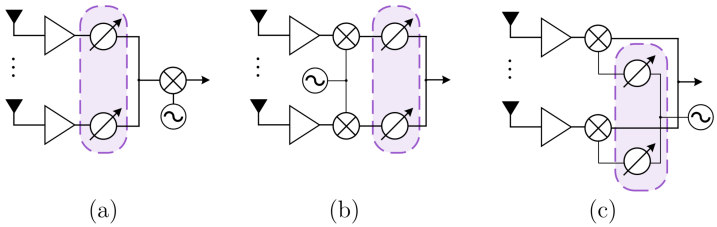


Figure 1.3: RF (a), IF (b) and LO (c) phase shifting as categories of analog beamforming.

Table 1.2: Phase Shifting Schemes Comparison

Phase shifting	Area/Cost	P_{DC}	Phase shifter design	LO distribution
RF				
IF				
LO				

power combiners (e.g., the Wilkinson combiner) at lower frequencies further increases the total area.

LO Phase Shifting

LO phase shifting architecture also suffers from a complex LO distribution network, especially challenging because of certain phase coherency that it has to guarantee. On the other hand, some of the requirements for the phase shifter performance are relatively relaxed, since the loss, non-linearity, and noise performance do not directly translate to the receiver performance [Fak].

Table 1.2 compares the RF, IF and LO phase shifting schemes by illustrating some of the above-mentioned aspects. In the available literature, rather few examples of mm-wave phased arrays utilizing IF phase shifting can be found, such as a *D*-band 8Tx-8Rx phased array [LR22] and a *V*-band 4-element receiver [KP15]. On the other hand, LO phase shifting implementations are more frequently reported in recent studies, including a 94-GHz 4Tx-4Rx phased array IC [TST+17], a 94-GHz 16Tx-1Rx chip [ZXL+24], and an *E*-band 16-TRx module [ESB20]. In most cases, enhanced SNR is highlighted as the primary motivation for adopting LO phase shifting, as the phase shifter's insertion loss does not affect the signal propagation path. However, due to its numerous advantages, RF phase shifting remains the most widely used scheme for high-frequency phased arrays. Several examples in *W*-band include [LPO+18], [LCH+22], [NVGS+15], [MMM+24] and many others. As shown in Table 1.2, the primary limitation of the RF phase shifting scheme is the challenging design of high-frequency phase shifters. Addressing this challenge is one of the key motivations of this thesis.

1.2 Satellite Communication in Beyond-5G Infrastructure

Nowadays, the latest technological advancements still have not resulted in meeting the demanded ubiquity, i.e., availability in remote areas. Ensuring a full coverage for various scenarios, including mobility use cases on land, sea, or air, requires a more complex multi-dimensional network with heterogeneous elements. Satellite constellations will complement 5G/6G terrestrial coverage and provide connectivity across the globe. European Space Agency (ESA) is actively carrying out various activities to integrate satellite technologies into communication networks as part of the ”Space for 5G/6G” program. More details can be found in [Age].

These activities include the design and implementation of a three-layer network architecture, comprised of the terrestrial, airborne, and space layers, schematically illustrated in Fig. 1.4.

Multi-beam phased arrays using analog beamforming scheme are widely used in modern satellite communication. The most recent examples include:

- **Starlink**, launched in 2018 by SpaceX into LEO (low Earth orbit). The constellation of thousands of satellites operates at the K_u-band

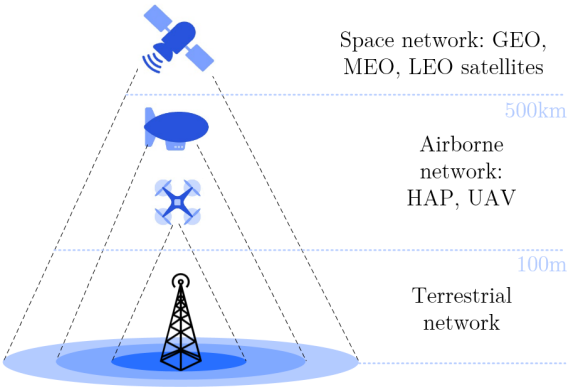


Figure 1.4: Multi-layer network architecture for 5G/6G.

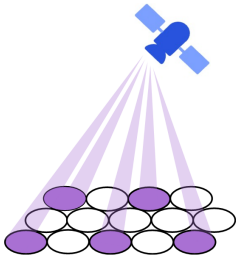


Figure 1.5: Beam hopping technology.

(12−18 GHz) and uses beam hopping (illustrated in Fig. 1.5) as the beam coverage method. The phase shifters are one of the main components of the 8-channel beamforming chip [MKAY+21].

- **Eutelsat Quantum**, developed by ESA, Eutelsat, and Airbus, and launched in 2021 into GEO (geostationary orbit). The satellite uses the same coverage method and frequency in receive mode as Starlink. Further details and more examples can be found in work [YWZ+23].

The increasing number of launched K_u- and K_a-band satellites seemingly pushes the research focus to Q- (33−50 GHz) and V- (50−75 GHz) frequency bands, which promise extensive spectrum resources. Companies like Boeing, SpaceX, and Telesat plan to explore these bands for the next generation of LEO Internet constellation systems [YWZ+23].

According to the overview [YWZ+23], analog beamforming plays a dominant role in modern satellite communication systems when a limited number of beams is sufficient. In such systems, the phase shifter remains a key component of the beamforming network, efficiently enabling the beam hopping technique for flexible coverage.

1.3 SiGe BiCMOS Technologies in Next-Generation Communication Systems

SiGe BiCMOS technologies made a new turn in the history of IC manufacturing and nowadays are continuously under development. This mixed-device semiconductor process offers simultaneously a superior high-frequency performance of SiGe HBT devices with f_t and f_{max} exceeding 300 GHz, as well as integration of a CMOS-based digital logic on a single substrate. The back end of line (BEOL) with large number of available metal layers additionally contributes to highly integrated compact electronic components by allowing a denser routing. Some SiGe BiCMOS technologies provide an option to use slower bipolar transistors with higher breakdown voltage, enhancing power amplifiers' performance. These properties enable a scalable phased array implementation on a single chip. Fully integrated SiGe BiCMOS *W*-band phased arrays were presented for instance in [LPO+18] and [SHSB19] from IBM and Nokia Bell Labs, respectively, and in [MMM+24] from NXP Semiconductors.

As an alternative, an array performance can be additionally optimized by combining the main advantages of several technologies in one multi-chip system. The main idea is explained in work [RP17]. The SiGe-based beamformer IC is combined with GaAs PA and LNA. Due to the higher breakdown voltage and low-loss substrate, such use of GaAs results in higher output power and lower noise figure (NF), respectively. The authors also present several examples of K_u and K_a phased arrays for satellite communication manufactured by Rockwell Collins and Boeing. If the advantages of such multi-chip implementations remain prominent enough at *W*-band and higher frequencies in the future, considering related packaging challenges, cost, mass volume production and continuous technological developments, is difficult to foresee.

The circuits presented in this thesis are implemented in:

- NXP's high volume 140-nm SiGe BiCMOS process with 6-layer BEOL and f_t/f_{max} of 280 GHz for high-speed devices (Chapter 2, 3);
- IHP's 130-nm SiGe BiCMOS SG13G2 process with 7-layer aluminum BEOL and f_t/f_{max} of 300/500 GHz (Chapter 5);
- IHP's 130-nm SiGe BiCMOS SG13G3Cu process with 6 copper and 2 aluminum BEOL layers and f_t/f_{max} of 470/650 GHz (Chapter 4).

1.4 Structure and Goals of the Thesis

In essence, many weak points in analog beamforming architecture come from the degrading performance of analog circuits at higher frequencies and their challenging design. This is especially relevant for phase shifters, as they are responsible for the complete beamforming functionality of analog and partially of hybrid schemes. Die area consumption is another critical point, as its reduction not only enables a higher level of integration but also directly influences the manufacturing costs, especially noticeable in volume production.

In addition, the antenna elements are normally placed proportionally closer to each other when the operating frequency increases. The spacing of $\lambda/2$ is often preferred to minimize grating lobes, which at 100 GHz would mean a grid of 1.5 mm. In this space, a full Tx and Rx RF chain (between the power combiner and the antenna), including digital control circuits, memory, etc., should be placed. Therefore, moving forward to sub-THz frequencies, the area consumption of a component becomes a defining factor, since a larger chain might simply not fit between the antenna elements.

This thesis investigates area- and power-reduction strategies for building blocks of phased arrays potentially used in beyond-5G systems both on land and in space.

In Chapter 2, various passive structures are presented with a focus on area reduction. Different implementations of quadrature signal splitters are discussed in detail and several designs are presented. The structures from this chapter are later used as building blocks for the circuits presented in the remaining chapters.

Chapter 3 presents three *W*-band active phase shifters designs. The first design is based on a conventional Gilbert cell and uses a compact vertical differential Lange coupler as an I/Q splitter. The second circuit uses one topology modification to integrate a balun-functionality directly to the core without additional components, thus further contributing to the circuit's miniaturization. The third design concludes the chapter by considering the use of phase shifters in a transceiver, i.e. operating in two directions. This circuit still uses a compact active topology and in addition, adapts one of the main advantages of passive phase shifters, namely their bidirectional operation.

Q- and *V*-band broadband components for space electronics are demonstrated in Chapter 4. This chapter discusses considerations for an efficient chain design with a focus on high dynamic range. In addition, an effort has been made to reduce the number of circuits in the chain by integrating several functions into one component. Presented designs include a phase shifter that can be simultaneously used as a variable gain amplifier (VGA) and a VGA with an additional equalization function.

Chapter 5 discusses design aspects for low-power operation, especially important for large phased arrays. Two *W*-band LNAs with standard and reduced power consumption are presented to investigate related compromise between performance metrics. A down-converting mixer design with additional image signal suppression is discussed as a low-power and compact alternative to conventional I/Q mixers.

2 Miniaturization of Passive Components

The size and number of passive components in a circuit directly impact the overall area consumption. This makes them the first candidate and the lowest hierarchical design level to develop miniaturization strategies. Inductors, couplers, transformers, baluns, power combiners, and other components are typically implemented using conventional geometries based on established design guidelines. However, the availability of multiple metal layers in modern technologies provides flexibility, enabling experimenting with different shapes and orientations.

2.1 I/Q Splitters Overview

One of the key steps in the phase shifter design is an in-phase and quadrature phase (I/Q) signal generation, required for many topologies. Some conventional passive I/Q splitter implementations are shown in Fig. 2.1.

Branch-line coupler shown in Fig. 2.1a achieves very low insertion loss and is easy to implement. The main disadvantages are the narrow-band response and its physically large geometry. Improved bandwidth and smaller footprint are possible to achieve using a coupled-line coupler, schematically shown in Fig. 2.1b. In this case, to obtain the power splitting with a 90° degrees phase difference two quadrature-wave lines are placed close to each other horizontally thus achieving an edge coupling. Vertical placement of the two lines provides a broadside coupling. By changing the distance between the two lines, one can control the proportion of the power splitting over the two output ports ”through” and ”coupled”. It is common to target a slight over-coupling instead of an ideal 3-dB splitting to enhance the frequency bandwidth. The concept is illustrated in Fig. 2.2.

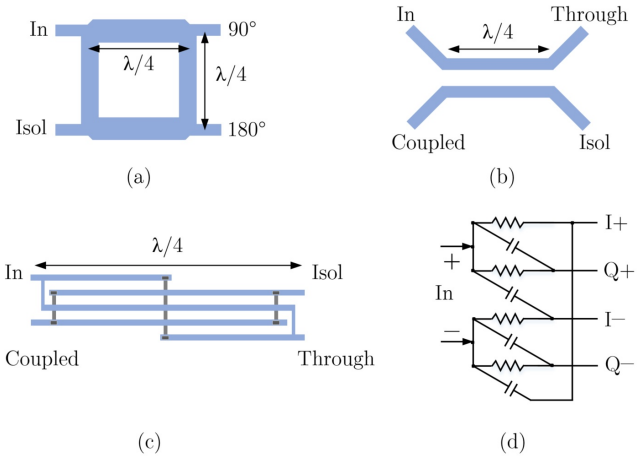


Figure 2.1: Quadrature signal generation: branch-line coupler (a), coupled-lines coupler (b), Lange coupler (c), polyphase filter (d).

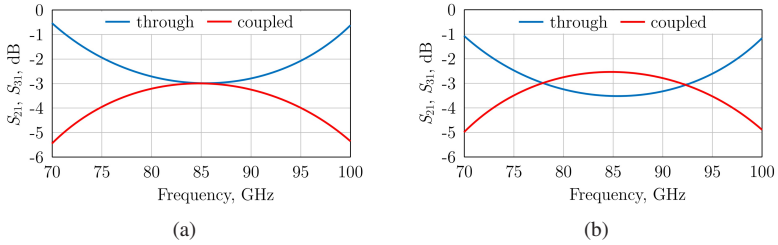


Figure 2.2: Simplified demonstration of an ideal 3-dB splitting (a) and over-coupling (b).

One common difficulty in coupled-line couplers is when for a desired coupling coefficient the lines have to be placed closer than allowed by the design rules of the technology used. This is especially true at mm-wave frequencies. To overcome this limitation, Julius Lange invented in 1969 a coupler as shown in Fig. 2.1c and by now known as the Lange coupler. In essence, the used interdigitated geometry is an evolution of a coupled-line coupler.

The simplified mathematical derivations to describe the Lange coupler function can be found in [KPP78]. They are based on the analysis of the even- and odd-

mode capacitances of the 4-conductor line, starting from a 2-conductor line (or 2-coupled lines). The analysis can be further expanded to an N-conductor line configuration, resulting in the change of the odd-mode capacitance:

$$C_{oN} \approx \frac{C_1}{2} + (N-1)(C_{0o} - C_{0e}), \tag{2.1}$$

where C_{0o} and C_{0e} are odd- and even-mode capacitances of a 2-conductor line, respectively, and C_1 is a total capacitance to ground of an equivalent single microstrip line. For simplicity, the rest of the analysis is left out here. The results show that for the same coupling coefficient in the Lange coupler the lines have to be placed wider apart than in the conventional coupled-line coupler, which solves the forementioned problem with design rules. The Lange coupler exhibits an additional advantage of a wideband frequency performance.

Another passive technique to provide an I/Q signal is to use an RC polyphase filter (PPF). The simplest schematic, namely a one-stage PPF is shown in Fig. 2.1d. One advantage of this topology is its very compact implementation form in silicon. When using multiple stages, it is possible to minimize the gain and phase errors over a large bandwidth, otherwise the performance can only be optimized at a single frequency point. At mm-wave frequencies, the PPFs are not frequently used as an I/Q splitter. Their main disadvantage is the significantly higher insertion loss in comparison with quadrature couplers. In most cases, an additional amplifying stage is required to compensate these losses at the drawback of increased power dissipation and area consumption. Some PPF examples include a wideband ring-shaped two-stage PPF proposed in [MHHP16] operating at 20–50 GHz and a type II two-stage PPF as an I/Q splitter at the input of a 26-GHz vector modulator from [KBKG19]. The above-mentioned designs exhibit an insertion loss of 19 dB and 12 dB, respectively. Moving towards higher operating frequencies, the advantage of reduced die area consumption becomes less and less pronounced, since the couplers also become proportionally smaller with increasing frequency while having much smaller insertion loss than PPF.

Other types of I/Q splitters, such as a 90° delay line and a rat-race coupler, were not considered in this overview.

2.2 Proposed Quadrature Couplers

Parts of this section include material previously published in [2] and [3].

From the previous overview, both Lange and coupled-line couplers were chosen as the most promising implementations of the I/Q splitter for a *W*-band phase shifter, as they demonstrate a compromise between the area consumption and insertion loss.

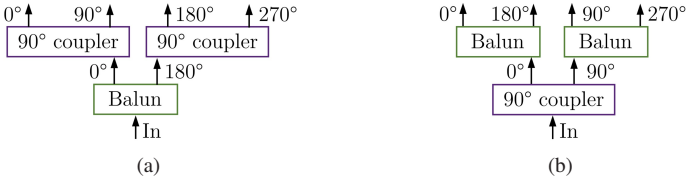


Figure 2.3: Differential I/Q signal generation using quadrature couplers.

Differential vector-sum phase shifters require differential I/Q splitters. To build one using quadrature couplers, two conventional approaches can be employed: using a balun for single-ended to differential conversion followed by two quadrature couplers (see Fig. 2.3a) or using one coupler followed by two baluns (see Fig. 2.3b). Both approaches result in the same set of output phases. However, the first approach allows flexible adjustment from single-ended to differential input by removing the balun. For this reason, this option was ultimately chosen for the proposed designs.

2.2.1 Differential Lange Coupler

For many topologies, an I/Q splitter, in any form, is essential for analog phase-shifting functionality and cannot be omitted. In many cases, the coupler occupies more than half of the IC area of an active phase shifter. Therefore, exploring more compact solutions remains crucial. From the discussion above, the first candidate chosen for our compact I/Q splitter is the Lange coupler due to its good compromise between insertion loss, chip area, and bandwidth. To build the complete differential I/Q splitter from Fig. 2.3a, the straightforward implementation would include two couplers placed next to each other, meaning

double area and a complicated connection with the succeeding hardware, due to the long shape of the Lange coupler in one direction. However, this thesis explores another approach, shown in Fig. 2.4.

The proposed differential coupler is built in essence by placing the first coupler vertically under the second one, obtaining differential operation for the same footprint. As a first step, couplers 1 and 2 were designed and optimized separately in a 6-metal layer technology. The line width and spacing in coupler 1 is 3 µm, following design rules for the upper thick metal layer. Since the thickness of metal layers m1 and m6 is unequal, two stacked thin metal layers (m1 and m2) are used for coupler 2 to partially compensate for the imbalance in ohmic losses and to achieve comparable performance.

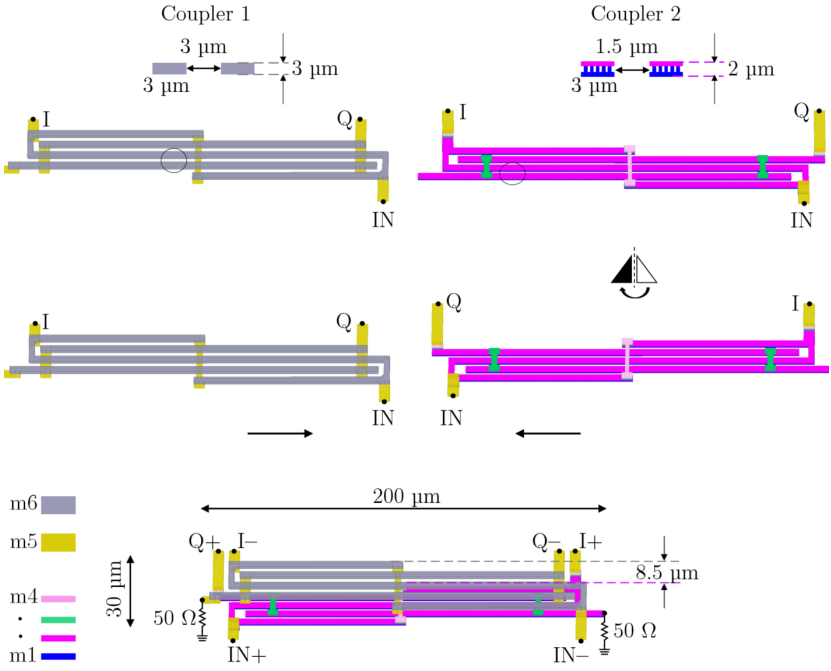


Figure 2.4: Differential Lange coupler.

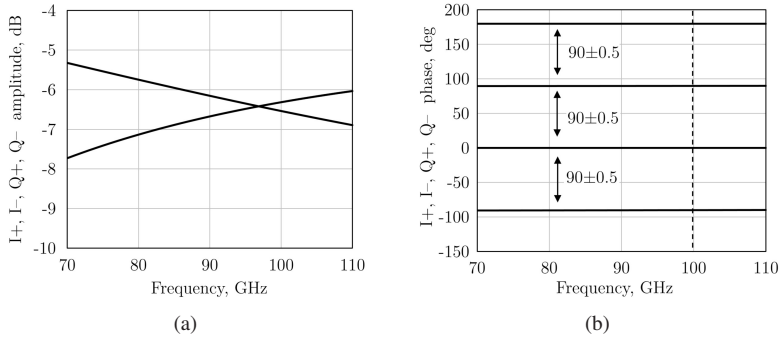


Figure 2.5: Simulated performance of two identical couplers placed next to each other: amplitude (a) and phase (b) response.

As the next design step, the two couplers were placed together and optimized as one differential structure. The main challenge in the layout optimization of such a combined structure is an unwanted broadside coupling between the two couplers. To reduce this interaction, coupler 2 was horizontally flipped relative to coupler 1. For the same reason, only two layers are used for coupler 2. Additionally, a horizontal offset of 8.5 µm was introduced to further increase the separation and reduce capacitive coupling between the two couplers. The offset was selected so that most of the lines in coupler 2 were positioned horizontally between the lines of coupler 1, rather than directly aligned underneath them.

Fig. 2.5 shows the simulated performance of a differential coupler formed by two identical Lange couplers (coupler 1), conventionally placed next to each other. This simulation uses an ideal balun, therefore, in Fig. 2.5a, 6 dB is the splitting loss, and an additional 0.4 dB (at 97 GHz) is the actual added (resistive) loss from the coupler layout. The ideal balun and a separate EM simulation of the identical couplers are also the reasons for four curves overlapping and appearing as two in the plot. Fig. 2.5b shows the relative phase response of the obtained phase states, as well as the maximum phase error between them within 70−100 GHz.

Fig. 2.6, in turn, presents the simulated performance of the proposed differential Lange coupler in its compact vertical implementation. Compared to the results of the conventional implementation, one can observe only 0.1 dB higher

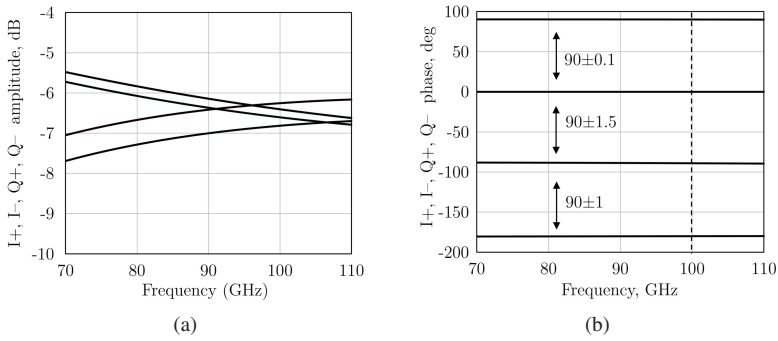


Figure 2.6: Simulated performance of the proposed vertical differential Lange coupler: amplitude (a) and phase (b) response.

insertion loss and a $0.5-1^\circ$ larger phase error. However, this is an expected and acceptable sacrifice for such a significant area reduction of almost 50%.

2.2.2 Differential Coupler Based on Spiral Edge-Coupled Lines

If broadband operation is not required and the design rules allow placing metal lines on the chosen layer close enough to each other, the use of a conventional coupled-line can offer more flexibility in terms of chosen geometry than the Lange coupler. Practically speaking, two coupled lines are easier to bend into various shapes to reduce the overall footprint than several interdigitated conductors with multiple connections.

In the next design iteration of a compact differential I/Q splitter, two single-ended couplers based on edge-coupled lines are used and turned into spiral geometries. They are implemented on different metal layers following the above-presented approach, i.e. placed vertically under each another. Coupler 2 is flipped relative to coupler 1 and uses the m1 and m2 layers, as in the previous design. The final geometry is presented in Fig. 2.7. The resulting structure, similar to the previous case, occupies only half the area normally required for two couplers placed side by side. Additionally, the square geometry

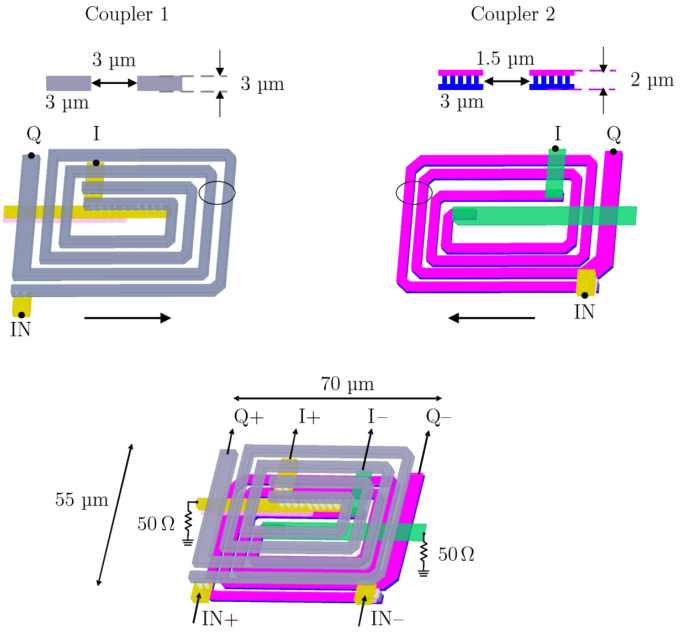


Figure 2.7: Differential spiral coupler.

is another beneficial property, as it often enables more convenient integration with other parts of the layout.

Fig. 2.8 shows the simulated performance of the differential spiral coupler. The structure exhibits 0.5 dB higher insertion loss compared to the differential Lange coupler, presumably caused by folding the lines several times to form a spiral. In addition, amplitude and phase imbalances deteriorate more within the same frequency range. However, such a narrow-band response was expected from the coupled-line coupler.

This example also demonstrates the difficult optimization process with increasing geometry complexity and related performance sacrifices. Nevertheless, these geometrical experiments can lead to effective miniaturization benefits.

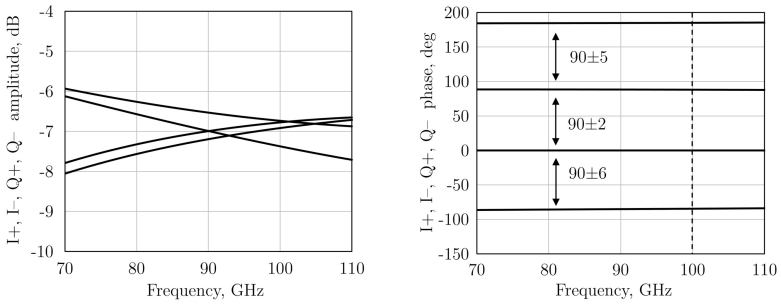


Figure 2.8: Simulated performance of the proposed vertical differential spiral coupler: amplitude (a) and phase (b) response.

2.3 Inductors and Baluns

Miniaturization techniques can be applied to other passive components as well. If a high Q-factor of an inductor is not critical, a multi-layer solution was used to reduce area consumption, as in [TIK+22] and [HTAH08]. An example of such an inductor is shown in Fig. 2.9a and was designed for the phase shifter which will be presented in Section 3.3.

The inductor uses two top layers and two thin layers stacked together to reduce the resistive loss of the final turn. An EM-simulated inductance of 130 pH is

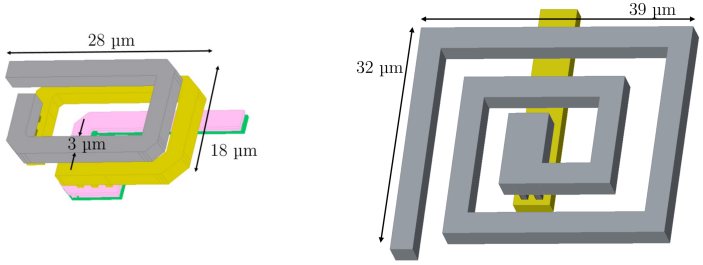


Figure 2.9: Multi-layer inductor (a) and conventional inductor (b).

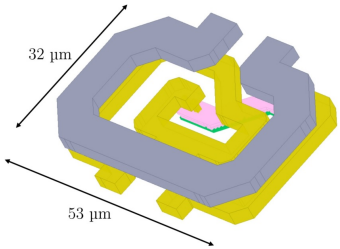


Figure 2.10: Transformer

achieved, with a Q-factor of 9.8 at 100 GHz. Adding more turns using lower thin metal layers is possible, allowing for a more compact design. However, increased resistive losses and reduced distance to the substrate lead to a Q-factor drop from nearly 10 to 8. Additionally, since the smallest turn on the highest metal layers is constrained by design rules, the area reduction achieved with a fourth turn would be minimal and not justify the trade-offs. Consequently, the final design uses three turns. An essential design consideration is maintaining the same signal propagation direction for each turn when transitioning between layers to enhance the structure's inductive behavior. Introducing a horizontal offset between turns can further improve performance by reducing undesired parasitic capacitance.

Fig. 2.9b illustrates an example of a conventional inductor geometry for size comparison. This structure achieves the same inductance of 130 pH with a Q-factor of 12 at 100 GHz. To summarize, the Q-factor drop from 12 to 9.8 corresponds to approximately a 40% reduction in area. It is important to note that this example provides a rough comparison and does not cover all possible geometries, implementations, or technological advancements available in various BEOL processes.

The use of transformers frequently contributes to the area efficiency of a circuit by combining impedance matching and a single-ended to differential conversion in one component. Fig. 2.10 shows one of the transformers used for the circuit to be discussed in Section 3.4. Two turns were used on one of the coils to further reduce the transformer size.

Normally the coupling coefficient degrades with increasing frequency. The coupling can be slightly improved for higher frequencies by, e.g., using sandwich-

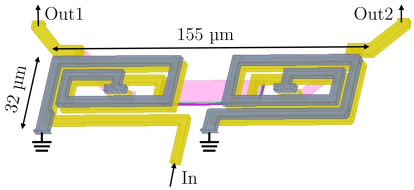


Figure 2.11: Marchand balun.

coupled transformers [HMM22], whereas the bandwidth remains rather limited. A broadband alternative for the single-ended to differential conversion among passive structures is a Marchand balun. The balun in Fig. 2.11 was designed for the single-ended version of the phase shifter presented in Section 3.2. It uses the broadside coupling between the lines turned into spirals for a more compact footprint than a conventional straight geometry of the Marchand balun.

2.4 Conclusion

This chapter presents miniaturization approaches applied to the layout design of I/Q splitters, a critical building block commonly used in phase shifters. Several conventional topologies are discussed in the context of mm-wave operation. The Lange coupler and coupled-line coupler are selected as baseline designs, as at *W*-band frequencies, they offer a smaller footprint than the branch-line coupler and lower insertion loss than polyphase filters. The objective of this chapter is to reduce the required area for these couplers by utilizing multiple metal layers and the available vertical volume. As a result, the proposed 3D differential Lange coupler achieves a 50% reduction in area with negligible performance degradation compared to two separate single-ended Lange couplers. An alternative design, the 3D spiral-shaped coupled-line coupler, occupies slightly less than 50% of the area of the previous design but at the expense of more significant phase and amplitude imbalances. The chapter also briefly discusses other passive structures, such as inductors, transformers, and baluns, and their role in area reduction.

3 W-Band Vector-Sum Phase Shifters for Phased Arrays

W-band phased arrays employing RF beamforming are in focus for the future terrestrial 6G systems development, as discussed in Chapter 1. The beam steering functionality of such arrays is critically dependent on the phase shifter design, which is the primary focus of this chapter.

3.1 Architectures and Definitions

3.1.1 Beam Squint in Phase-Based Beam Steering

To better understand the necessary hardware for a beam steering functionality, it is important to consider a more general principle of operation of phased arrays in terms of the instantaneous (or signal) bandwidth. Using the same example of the uniform linear array from Section 1.1.1, its array factor can be expressed as [Hau19]:

$$AF = \sum_{n=1}^{N} e^{j2\pi(n-1)\frac{d}{c}(f\sin\theta - f_c\sin\theta_s)}, \tag{3.1}$$

where f_c denotes the center frequency, d – the distance between two antenna elements, N – total number of antenna elements, θ – the angle of the wavefront and θ_s – desired beam direction.

In case $f = f_c$, the phase difference of $\Delta\varphi = \frac{2\pi f_c}{c} d\sin\theta_s$ applied to the neighboring elements will make the beam point to θ_s. If $f \neq f_c$, then with the same phase settings, the beam will deviate or squint from the target direction θ_s to $\theta_q(f) = \sin^{-1}(\frac{f_c}{f}\sin\theta_s)$. This mechanism is illustrated in Fig. 3.1 [Mai94].

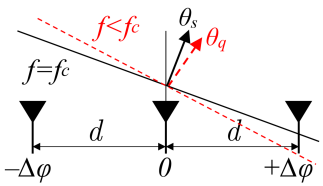


Figure 3.1: Beam squint during the phased array operation not at the central frequency f_c.

The acceptable level of beam squint for a system defines what signal bandwidth can be approximated as "narrow" or quasi-monochromatic. One commonly used criterion is derived from the concept of an array "fill time" [Mai94] at its largest scan angle. The array is minimally "filled", if a leading edge of a short pulse τ_{min} arrives at the last antenna element, while a trailing edge hits the first antenna element. Therefore,

$$B_s = \frac{1}{\tau} \leq \frac{c}{Nd\sin\theta_s}, \tag{3.2}$$

where B_s is the signal bandwidth, τ is the corresponding pulse duration and other variables are the same as in (3.1).

If the condition above is not satisfied, a pulse dispersion occurs leading to an increased bit error rate of digitally modulated signals.

Apart from the instantaneous signal bandwidth, the system or operational bandwidth is influenced by many other factors, such as mutual coupling between the elements, the bandwidth of each antenna and the remaining hardware [Hau17].

To mitigate the beam squint and ensure the broadband operation of a phased array without losing its beamsteering precision, a general solution is the use of true-time delay units (TTD). The phase shift is exactly proportional to the frequency and translates to a perfectly flat frequency response of the group delay.

One of the conventional implementations of a TTD includes time delay elements, e.g., multiple transmission lines of different lengths, with switches in between and additional equalizers to compensate for increasing insertion loss over frequency. High complexity and significant area consumption are the main drawbacks fundamentally inherent to TTD. In the literature, no publicly

available examples of *W*-band TTDs were found. The only available design in the *D*-band with sufficient maximum delay is presented in [KEKM20]. The circuit covers the 3-dB bandwidth of 60 GHz and provides 16 delay settings, which is equivalent to a phase shifter with a 4-bit phase resolution. Let us consider the work [RGB+21] for a very approximate size comparison. It presents a *D*-band active phase shifter design with a 5-bit phase resolution and 20 GHz of bandwidth. The first and latter circuits occupy 1.16 mm^2 and 0.05 mm^2, respectively. This example demonstrates a very high price for wideband operation, namely in this case, about a 23 times area penalty. On the other hand, the discussed TTD is based on the conventional topology with a separate delay stage per bit. An alternative approach was presented for a lower operating frequency range but resulted in a more compact footprint. Work [MLM14] demonstrated continuous delay control by separating stages for coarse switching and analog fine-tuning, resulting in an area of only 0.22 mm^2. Although significant miniaturization is achieved, the area of 0.22 mm^2 does not include a potentially required amplification stage to compensate for the 15-dB insertion loss of this circuit, as reported at 30 GHz.

For many integrated systems the use of such a bulky component at every antenna element is not an option. The use of the phase shifters is therefore frequently a preferred solution for the majority of narrow-band phased arrays with analog or hybrid beamforming schemes. An alternative solution to reach a compromise between wider bandwidth and a relatively compact system is shown in Fig. 3.2. Such hybrid phased array uses TTD only for the coarse delay control at the common legs of the sub-arrays, whereas a finer phase tuning is

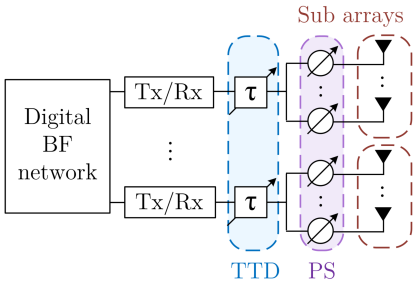


Figure 3.2: An example of a hybrid phased array as a compromise between time-delay-based and phase-shift-based arrays.

done by the phase shifters within each sub-array. The beam squint is also less critical for the individual sub-arrays due to their wider beamwidth. However, the final architecture choice and the feasibility of such trade-offs are defined by the application requirements.

This research work focuses on phase-shifter-based beamforming networks, whereas more information on TTD can be found in [Ma16].

3.1.2 Phase Shifter Topologies

Phase shifter as a building block allows for a large variety of possible implementations that exhibit different limitations depending on e.g. operating frequency, phase control range and resolution, area and linearity requirements. Several examples are presented in Fig. 3.3.

Switched-line and loaded-line topologies (shown in Fig. 3.3a,b) belong to well-known passive switchable solutions. They are easy to implement and use a straightforward principle of operation. However, in a single stage implementation, these topologies cannot provide the entire 360° phase shift range. Multiple stages combined could potentially do this, but achieving high phase resolution requires a large number of various passive structures and switches in between. Such solutions present therefore the highest area consumption and insertion loss.

Reflection-type phase shifters (RTPS) (shown in Fig. 3.3c) use a different principle of operation and provide continuous phase control by using two tunable loads connected to the conventional output ports of a 90° coupler. The output signal in this case is taken from the isolated port of the coupler. The main challenge of an RTPS is achieving the wide phase shift range which requires a more complex reflective load, such as in [GN17] or the use of additional phase shifting stages. This topology is especially popular in K and K_a frequency bands, where passive structures are more compact than at lower frequencies. At higher frequencies the RTPS exhibits higher insertion loss than other implementation forms, however, a few examples can be found for V-band, e.g., [LW18].

As a 1-bit phase-shifting stage, various switched-filter networks can be employed. One of the many possible implementations is illustrated in Fig. 3.3d.

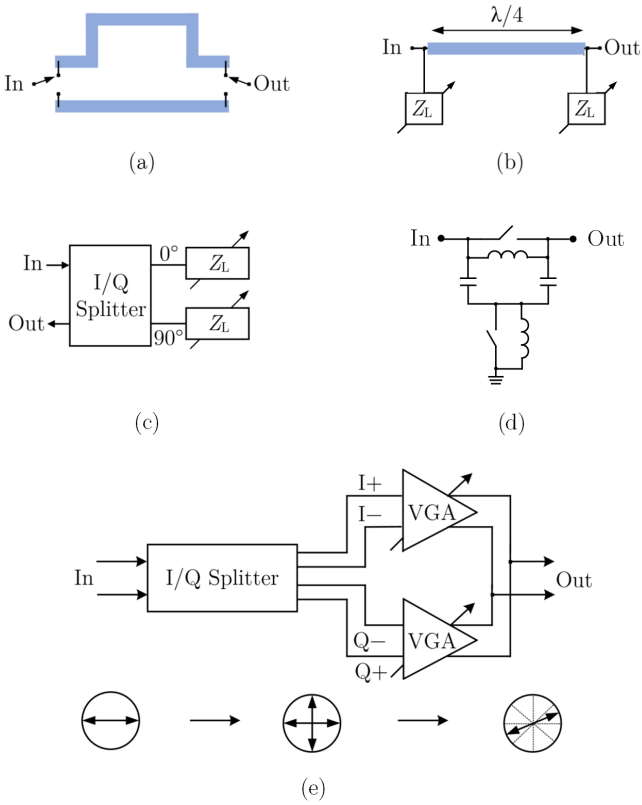


Figure 3.3: Phase shifter architectures: switched-line (a), loaded-line (b), reflection-type (c), switched-filter, and vector-sum (e) topologies.

This type of phase shifters, similar to switched-line and loaded-line topologies, suffers from an increased insertion loss when aiming for a high phase resolution but offers a larger bandwidth.

Finally, the vector-sum architecture is an active topology, which is frequently used in beamforming networks of phased arrays. The block-diagram as shown in Fig. 3.3e explains the principle of operation. After providing the differential input signal to the I/Q splitter, a differential I/Q signal is obtained, achieving four critical phase points, namely 0°, 90°, 180° and 270°. These points are

necessary to potentially reach a 360° phase range through the vector summation in all four quadrants. The VGAs in the I- and Q-path ensure the required amplitude weights for the desired signal at the output. The implementation of the VGAs, especially their gain control circuitry and its tunability, defines the maximum achievable phase resolution. The vector-sum architecture can also be adapted as a passive phase shifter by replacing the VGAs with attenuators, as proposed in [ZYG+23].

When moving to *W*-band frequencies, the implementation of a phase shifter becomes considerably challenging. Both passive and active solutions exhibit various limitations thus making the choice between them not obvious. Active implementations introduce either some gain or significantly lower loss compared to passive alternatives while having the most compact layouts ([LCHH20], [ZWL+23]). Passive phase shifters become smaller as the frequency increases and provide inherently high linearity, but their losses also increase, especially for high resolution, and require additional amplification. This in turn limits the linearity compared to a fully passive implementation, increases the overall die size and eliminates the attractive feature of reduced power consumption. As an example, the passive phase shifter in [WYW+22], based on switched networks, has an 18-dB average loss for a 6 bits phase resolution. Another recent work [GYA+24], proposes a *W*-band passive phase shifter with a combined architecture that incorporates two filter-based phase shift stages, an RTPS and a delay line. This implementation achieves an average insertion loss of 14.61 dB at 96 GHz and occupies an area of 0.22 mm^2. Another alternative could be a hybrid approach as a trade-off between linearity, phase-shift range, and phase-shifter loss. An example is demonstrated in [NVGS+15] and named a "cascaded active-passive phase-shift approach".

Apart from the overall fabrication costs increasing with the IC area consumption, limited spacing between antenna elements in arrays makes the area constraint non-negotiable in many cases. Because of the above-mentioned reasons, various hybrid implementations as well as fully active phase shifters become dominant in *W*-band. Instead of diving into a wide variety of component combinations and building a complex multi-stage phase shifting system, in this thesis, the preference is to explore the full potential of a single active phase shifter.

3.1.3 Performance Metrics

In this thesis, a phase shifter with a phase resolution of 6 bits in the 90–100 GHz frequency range was specified as design goal. These requirements were derived from a 6G mm-wave infrastructure communication system. The most critical performance metrics for this particular phase shifter include:

- Discreet phase control with a finite **resolution** N is a simpler and cheaper approximation of a desired continuous linear phase gradient. Reducing the phase shifter resolution leads to an increased pointing error

$$\frac{\Delta\theta}{\theta_{3dB}} = \frac{\pi}{4}\frac{1}{2^N} \tag{3.3}$$

  and causes quantization sidelobes with $P_{QL} = -6N$ dB [Mai94]. Various research activities aim to reduce these effects, e.g. using a two-dimensional quantization algorithm proposed by [HMB14]. As stated, 6 bit resolution is the requirement leading to 5.625° phase resolution.

- **Amplitude RMS error** – represents the undesired amplitude variation across different phase states. The metric is calculated as a root-mean-square of the amplitude deviation for each state from the average amplitude.

- **Phase RMS error** – has two definitions commonly used as the industrial standards in the field of mm-wave 6G systems. An integral nonlinearity (INL) definition defines the error in comparison to an ideal set of phase values. INL RMS phase error eventually represents full accumulated phase error across all states and is conventionally used as the phase RMS error definition in the literature. Another definition namely differential nonlinearity (DNL) RMS phase error is calculated as an average error between each state and the previous one and describes the phase shifting monotonicity.

Derived from the 6G system, the target amplitude RMS error and phase INL RMS error are in the range of 1 dB and 2°, respectively, across the frequency band.

The importance of amplitude and phase error assessment is caused by the overall performance degradation of the full array in the presence of such errors. Several examples include angle estimation degradation [Esc22], array gain reduction, as well as a negative impact for the null-steering of adaptive arrays leading to the worse interference rejection [BJ09] independent of the number of antenna elements.

The next performance characteristics are not specific to the phase shifters but are rather standard for most of the IC components. In this work, the aim was to generally optimize the designs to achieve a trade-off between the below-mentioned metrics.

- **Power consumption** of the individual phase shifter is less critical, compared to a PA that dominates in the chain in this regard. However, in an array, it is multiplied by the number of elements and thus every milliwatt can grow into a significant power dissipation if this number is very large. The most obvious practical disadvantages from the user perspective are stricter requirements for a power supply and increased operating expenses [MOM+20]. From a system design point of view, high power consumption creates significant challenges for heat dissipation components. An overheating affects the performance of electronic components and thus the entire system. Mechanical damage, i.e. bending the antenna plane due to thermal issues, will negatively influence the array beam steering capabilities [CHFX09].
- **Noise figure** (NF) of the vector-sum phase shifters is inherently increased by the splitting loss at the input and the insertion loss of the I/Q splitter. This is less problematic for an RF-beamforming receiver, as the phase shifter is located directly after the LNA and therefore presents a reduced noise contribution to the chain, if the preceding gain is high enough. The NF specifications on the transmitter side, in turn, imply stricter requirements for the phase shifter, even though the acceptable Tx NF is higher. The signal amplification by the PA occurs at the output, therefore the preceding components do not suppress the phase shifter noise presented to the chain. This is especially evident if the phase shifter or the remaining components additionally provide a gain control (attenuation), which is mostly the case in practice. This aspect is further discussed in Chapter 4.

- **Linearity** of a system defines the upper limit of its dynamic range and is often expressed in terms of the third-order intermodulation distortion (IMD3) or third-order intercept point (IP3) that eventually translates into an error vector magnitude (EVM) constraint. Considering linearity from a compression point of view, described by the 1-dB compression point ($IP_{1\text{dB}}$ or $OP_{1\text{dB}}$), helps to understand the fundamentally different requirements for the phase shifter operating in Rx and Tx direction. The input signal amplified by the LNA can compress the phase shifter as the next component in the Rx chain. In the Tx chain, the signal amplification occurs after the phase shifter, therefore, the $IP_{1\text{dB}}$ requirements can be more relaxed. In this chapter, the target OIP3 is set to 7 dBm.

3.2 Gilbert-Cell Based Phase Shifter

Parts of this section include material previously published in [3].

Based on the previously presented topology overview, the the vector-sum architecture is selected as the most suitable candidate for a compact implementation of a 6-bit phase shifter in one stage. In this topology, the gain of the VGAs in I- and Q-branches is set proportionally to $\cos\theta$ and $\sin\theta$, respectively, where θ is the desired phase of the output signal. Theoretically, this ensures a constant amplitude across all settings as the resulting amplitude after the vector summation is proportional to $\sqrt{\cos^2\theta + \sin^2\theta} = 1$, i.e. independent of the phase, whereas the resulting phase is equal to the desired phase: $\varphi = \tan^{-1}\left(\frac{\sin\theta}{\cos\theta}\right) = \tan^{-1}(\tan\theta) = \theta$.

The VGAs needed in the vector-sum phase shifter architecture can use various topologies, such as the Gilbert cell topology [GKR13a], [ZGKR+16], and a current-steering cascode topology [PZ17], [WGMKB18]. In this thesis, the Gilbert cell topology has been used as baseline. Several promising modifications will be introduced, starting from the miniaturization of passive structures and moving to more pronounced topology adjustments. The corresponding designs are presented in detail in the following sections.

3.2.1 Circuit Description

In the first vector modulator implementation, two Gilbert cells are formed by transistors Q_{01-04} and Q_{1-8}, as shown in Fig. 3.4. Decoupling capacitors are not shown in the schematic for simplicity but are included at the supply voltage Vcc and bias voltage V_3. Besides, available spacing on the die between DC pads is used for extra decoupling.

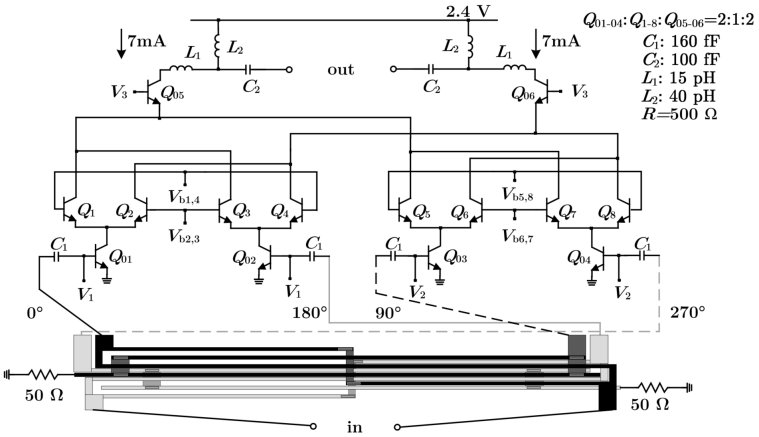


Figure 3.4: Simplified schematic. [3] ©IEEE

Phase Control

The circuit operation is based on a current-steering architecture. By varying V_{b1-8}, one can control current steering between all Q_{1-8} transistors and thus ensure that the required portions of each input signal (for vector summation) reach the output.

The phase shifter uses the differential Lange coupler discussed in Chapter 2 (Fig. 2.4) as an I/Q splitter. This leads to an overall area reduction compared to conventionally used two single-ended couplers placed next to each other.

Currents flowing through the Q_{1-8} transistors must satisfy cos- and sin- functions in a differential way as discussed previously. The design goal is achieving

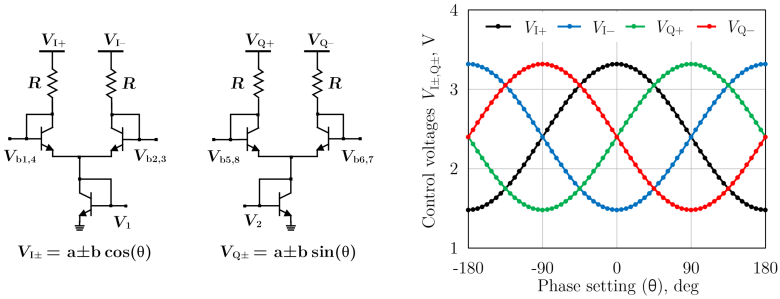


Figure 3.5: Bias networks (a) and phase control voltages (b).

a perfect 360° circle in the I-Q plane with constant amplitude for all phase states in an ideal case. The final implementation involves an integration of digital-to-analog converters (DAC) for the phase control, leading to the 6 bit resolution as discussed in section 3.1.3. As the digital part of the design is rather straightforward, this was not the objective of this work and therefore not implemented. In addition, certain measurement flexibility was needed for the prototype testing and potential troubleshooting.

As a temporary solution, the bias networks shown in Fig. 3.5a have been used for the analog control. The networks use a current mirror topology to copy the control currents to transistors Q_{1-8}. At a later stage, the ideal current sources on the schematic level were replaced by a combination of control voltages $V_{I,Q\pm}$ and resistors R. Such transition from current to voltage control helps to simplify chip characterization by allowing the use of a programmable source measure unit (SMU) for automated measurements. Fig. 3.5b shows the above-mentioned control voltages for every phase setting in the 360° range assuming the 6-bit resolution.

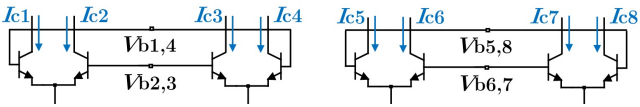


Figure 3.6: Quad transistors Q_{1-8} from Fig. 3.4 and the used notations for the current steering simulation.

Fig. 3.6 explains the used notations in the current steering simulation. The temporary bias networks translate voltages to the Q_{1-8} base voltages V_{b1-8} (Fig. 3.7) to obtain the collector currents I_{c1-8} as shown in Fig. 3.8.

As mentioned above, in a practical scenario, the currently used bias network will be replaced by DACs, therefore the DAC has to be able to supply bias voltages directly at V_{b1-8}, according to Fig. 3.7. The phase resolution limitation, in this case, comes from the regions where the points are located more densely, e.g., as shown in the same figure. ΔV_{min} sets thus the resolution requirement on the DAC. From this simulation, for the 6-bit phase shifter, the required range of voltages is from 1.44 V to 1.62 V with the smallest step of 1 mV. This can be achieved for example by a DAC supplying from 0 to 2.5 V with 12-bit resolution, being a common specification for a static DAC.

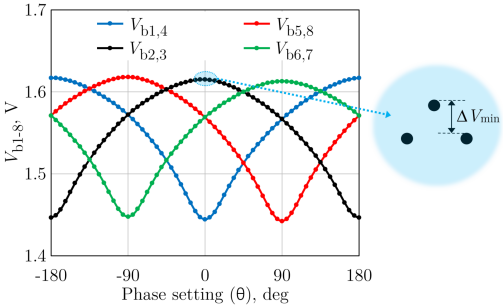


Figure 3.7: Base voltages of Q_{1-8} and phase resolution limitation.

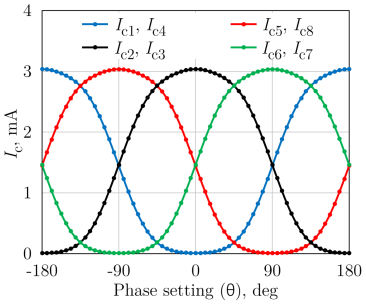


Figure 3.8: Collector currents of Q_{1-8}.

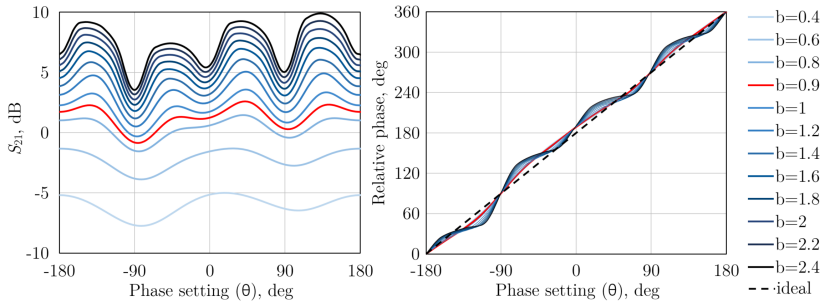


Figure 3.9: Choosing b coefficient in phase control equations.

The coefficients a and b used in the phase control equations (Fig. 3.5a) are chosen as 2.4 and 0.9, respectively. The value choice of b is one of the critical design decisions and is explained in Fig. 3.9. In an ideal case, the amplitude (expressed as absolute value of S_{21}) versus phase settings would be a flat horizontal line, meaning constant amplitude over all settings while the relative phase would have a linear response, corresponding to the dashed line (Fig. 3.9b). Smaller b leads to reduced amplitude variations and phase errors, however at the cost of absolute gain. In this scenario, the difference between base voltages $V_{\mathrm{b1-8}}$ becomes smaller, resulting in higher attenuation due to the destructive summation of the signals with opposite polarities, since all the paths are switched on simultaneously. This approach is frequently used in VGA design for attenuation. The results in the figure include the final EM simulation, therefore the response is not perfect for any of the b values. On the other hand, increasing b increases the average gain by the cost of higher amplitude and phase error. Due to these trends, $b = 0.9$ was chosen as a compromise.

The implemented analog phase control gives one fixed set of 64 (6 bits) states that, in the ideal case, results in one perfect circle in a S_{21} constellation diagram, demonstrating zero amplitude and phase errors. In practice, one can always observe certain deviations, mainly explained by a combination of two factors. The I/Q splitter in the architecture inserts phase and amplitude imbalances affecting the overall performance. However, a non-linear behavior of the Gilbert cell exhibits prevailing contribution. This behavior is studied analytically in

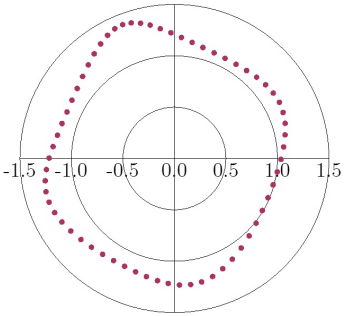


Figure 3.10: Measured non-calibrated S_{21} constellation diagram as an example of circle deformation.

[MJNPR20] showing that the parasitic base-emitter junction capacitance C_π, especially at higher frequencies contributes the most to this effect.

$$I_1'^{+} \propto (1 - X)(J_0(x) + 2\omega C_\pi V_\mathrm{T} J_1(x))\sin\,\omega t, \tag{3.4}$$

$$x = \frac{I_\mathrm{m}}{2\omega C_\pi V_\mathrm{T}}, \tag{3.5}$$

where J_0, J_1 denote the Bessel functions of the zeroth and first order, respectively, x – the argument of the Bessel function. I_m comes from RF tail current in the form of $I_\mathrm{RF} = I_m(1 + \cos\,\omega t)$. X ranges from 0 to 1 and is referred to as the control-to-phase-shift coefficient. Further details can be found in the complete analysis provided in the aforementioned work.

The multiplier including Bessel functions J_0, J_1 causes rotation and expansion of the constellation diagram. This effect is normally included in device modelling and is observed in the measurement results. Fig. 3.10 shows the measured constellation diagram for one set of voltages as an example.

By characterizing the phase shifter with a higher gain and phase resolution, one can manually choose the best settings to minimize this variation. This procedure has not been explored for this circuit but will be demonstrated in the last design of this chapter. In this design, the main interest is in obtaining the agreement between simulated and measured amplitude and phase RMS errors.

Common-Base Buffer

Transistors Q_{05-06} in Fig. 3.4 are used as a common-base buffer to reduce the load-sensitivity of the circuit. Besides, this buffer improves impedance matching and adds gain to the circuit. The corresponding simulation procedure to optimize the Q_{05-06} device size is explained in Fig. 3.11. Due to a large number of parallel connections, the output impedance of two Gilbert cells (reflected by S_{22}) is low and difficult to match. At the same time, the input impedance of a common-base transistor (S_{33}) is also low, while the output impedance (S_{44}) is higher, which aligns perfectly with this design. As can be seen from the figure, increasing Q_{05-06} brings $\mathrm{Re}(S_{33})$ closer to $\mathrm{Re}(S_{22})$, while $\mathrm{Re}(S_{44})$ moves further away from the 50-Ohm circle. Simultaneously, $\mathrm{Im}(S_{33})$ moves away from the complex conjugate S_{22}^*. This can potentially increase the phase error, as vector summation occurs at this connection in the circuit, making it the most sensitive point to mismatches. Consequently, the results do not demonstrate one clear "winning"Q_{05-06}:Q_{1-8} ratio. Instead, optimum options seem to lie in the middle range, with a size ratio of 1 or 2. A larger transistor size is better for the current combining, which is why a ratio of 2 was selected for the final design. Components L_1, L_2, and C_2 form an output matching network.

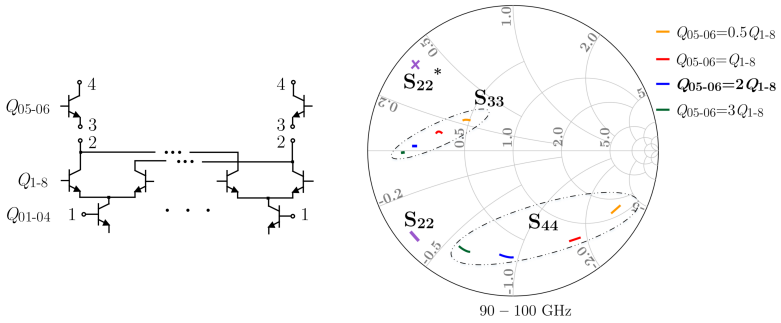


Figure 3.11: Simulation procedure to choose Q_{05-06}: port setup (a) and simulation results (b).

Linearity

The supply voltage available for this design was 2.4 V. When splitting 2.4 V between three stacks of transistors, achieving high linearity and high compression points can be challenging due to the limited voltage headroom. That is why, the quasi-differential topology is used to avoid a further voltage drop across the current source used in fully-differential circuits. The transistor size ratio is chosen as $Q_{01-04} : Q_{1-8} : Q_{05-06} = 2 : 1 : 2$. In this circuit, the linearity is dominated by the transconductance devices Q_{01-04}, therefore they are dimensioned accordingly. Fig. 3.12 shows the simulated output 1-dB compression point ($OP_{1\text{dB}}$) for each phase setting at 95 GHz, corresponding to maximum gain. The phase shifter achieves the average $OP_{1\text{dB}}$ of 0.6 dBm.

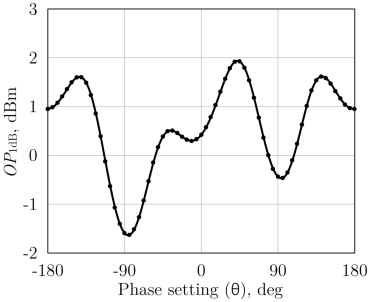


Figure 3.12: Simulated $OP_{1\text{dB}}$ for all phase settings.

3.2.2 Experimental Results

The die microphotograph with RF and DC pads is shown in Fig. 3.13. The active circuit core occupies 0.027 mm^2 of the IC area. The control voltages were obtained from the SMU.

The small signal measurements have been carried out using a broadband on-wafer system with Keysight N5290A VNA in a 4-port mixed mode configuration. The designed phase shifter consumes 49 mW of power including the control bias circuitry, from which the Gilbert cells use 34 mW, all from a 2.4 V supply. Fig. 3.14a presents measured gain for all phase states and provides a

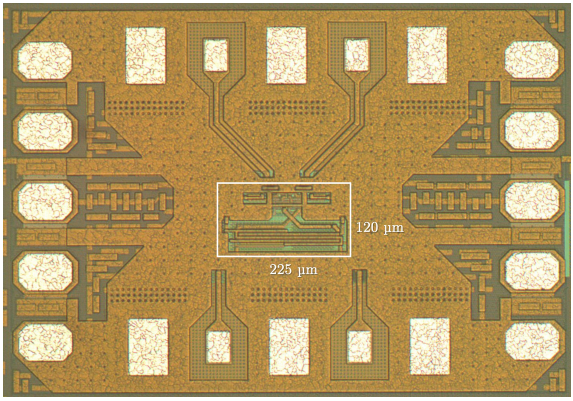


Figure 3.13: Chip photograph. [3] ©IEEE

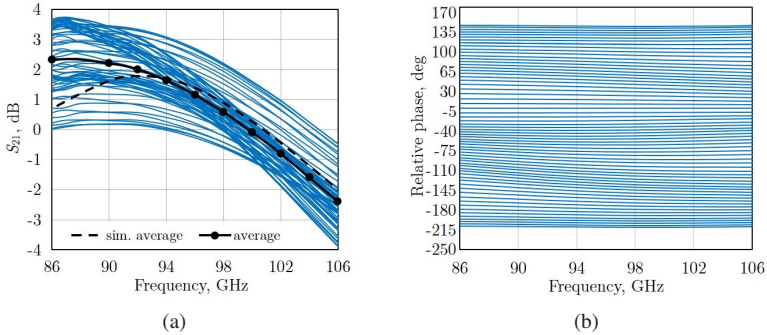


Figure 3.14: Measured gain (a) and relative phase for all phase settings (b).

comparison between simulated and measured average gain versus frequency. The maximum average gain is 2.3 dB. The average measured gain is in good agreement with simulated data, especially in the 92−106 GHz span. The relative phase shown in Fig. 3.14b is obtained by normalizing all 64 measured states to one of the states to remove frequency effects not directly related to the phase-shifting functionality of the circuit.

The measured frequency behavior of the amplitude and phase RMS error is shown in Fig. 3.15. The minimum amplitude RMS error is 0.67 dB at 98 GHz

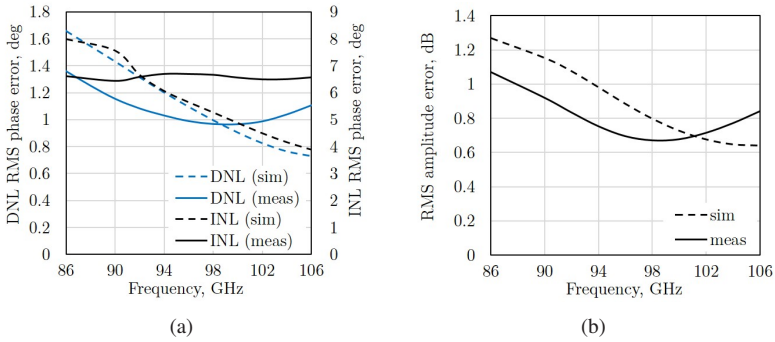


Figure 3.15: Measured and simulated phase (a) and amplitude (b) RMS error. [3] ©IEEE

and for the frequency range 86−106 GHz, remains below 1 dB. Measured values are in good agreement with the simulation, with only a slight shift towards lower frequencies.

The presented phase shifter exhibits 6.4° of INL RMSE, which remains below 6.6° at 86−106 GHz. The phase shifter has a minimum DNL RMSE of 0.98°, which remaining better than 1.35° across the same frequency range. The measured phase DNL and INL RMSE remain within the same range as the simulated values. However, accurately capturing the frequency behavior of these performance metrics proved more challenging due to their sensitivity to the EM simulation setup, particularly the pin placement.

The final performance satisfies the design goals in terms of the frequency range (92−100 GHz), phase resolution (6 bits), amplitude RMS error (≤1 dB), and OIP3 (≥7 dBm). The current INL RMS phase error of 6.4° needs further calibration with additional digital bits to bring it to the desired 2°. This procedure belongs to the standard characterization steps and is demonstrated in Section 3.4.2 for the last design in this chapter.

3.3 Blixer-Based Phase Shifter

Parts of this section include material that will be published in [4].

For a single-ended chain, the above-presented phase shifter requires input and output baluns. Following a straightforward approach, a phase shifter with two Marchand baluns from Chapter 2 (Fig. 2.11) can be realized. These two additional structures result in almost doubling the total IC area, i.e. 0.053 mm^2 instead of 0.027 mm^2. Consequently, any effort put into the miniaturization of the phase shifter seems unproductive only because of the area needed for the single-ended to-differential conversion. Therefore, this subchapter focuses on a compact implementation of this function.

3.3.1 Circuit Description

For the next design iteration shown in Fig. 3.16, the transconductance stage of the Gilbert cell was modified following the Blixer approach, proposed in [BKLN08]. Transistors $Q_{01,03}$ and $Q_{02,04}$ are connected in the common-base (CB) and common-emitter (CE) configuration respectively, to ensure 180° phase differences between branches and thus serve as an active balun directly integrated into the core. In this case, no passive balun is needed at the input, and also no additional transistors are needed to implement the single-to-differential function making this circuit different from adding an active balun as a separate stage at the input.

It should be noted that this phase shifter was not designed for a direct comparison with the previous design, but rather separately optimized to test several miniaturization ideas. Overall much smaller transistors were used to somewhat reduce the power consumption. The size ratio between the devices is $Q_{01-04} : Q_{1-8} : Q_{05-06} = 1 : 1.2 : 2.1$. The ratio between Q_{1-8} and Q_{05-06} is chosen following the considerations from the previous subchapter.

Inductors L_1 provide a DC path to ground in the branches with the CB transconductance stage. Simultaneously, the chosen inductance value ensures an RF choke at this node, allowing further RF signal propagation to the CE transistors $Q_{02,04}$. A common-base stage, Q_{05-06}, for current combining at the output

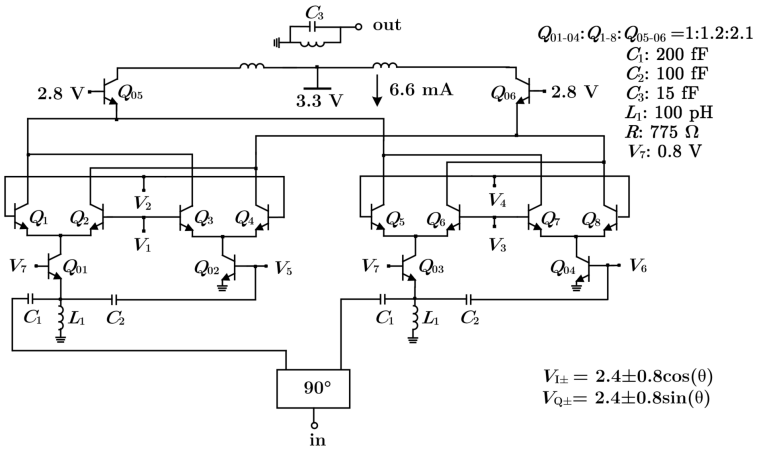


Figure 3.16: Simplified schematic. [4] ©IEEE

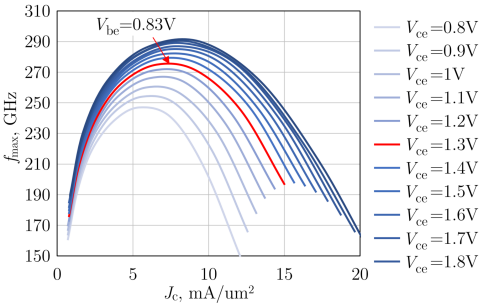


Figure 3.17: Simulated $f_{\max}$ to choose $V_{5,6}$.

is followed by a transformer as a compact solution, combining a matching network with a balun functionality.

An important aspect after modifying the g_m-stage is to make sure that it provides the differential signal to Q_{1-8}. Fig. 3.18a,b show simulated amplitude and phase difference between two outputs (2 and 3) of such a g_m-stage using a separate test-bench Fig. 3.18c. $V_{5,6}$ has a fixed value chosen to maximize $f_{\max}$ (Fig. 3.17), while V_7 is swept to optimize Q_{01-04} balun functionality.

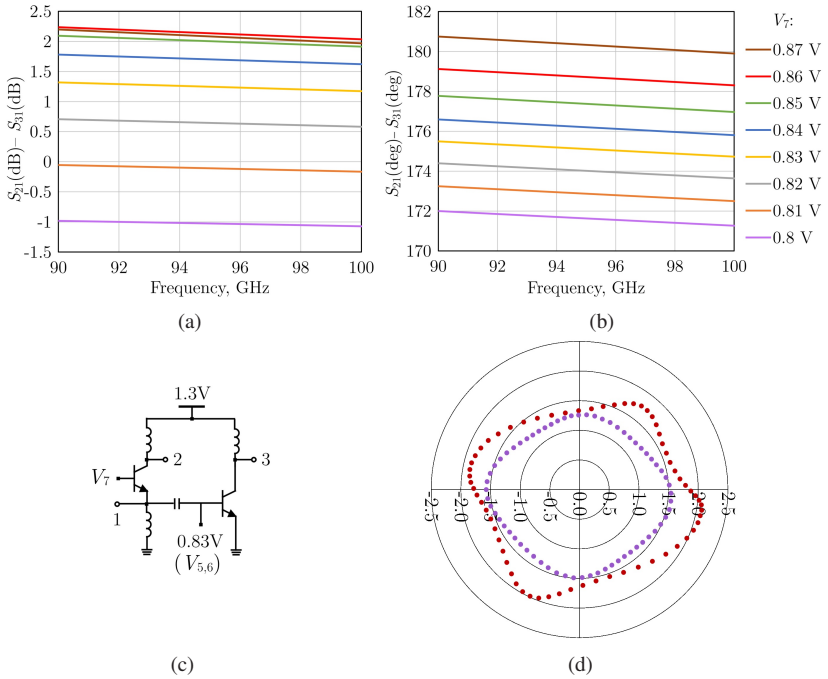


Figure 3.18: Choosing V_7: simulated amplitude imbalance (a) and phase difference (b) at the output of g_m-stage for different V_7; simplified simulation test bench (c) and S_{21} constellation diagram of complete phase shifter after tuning V_7 (d).

Changing V_7 impacts the transistors' transconductance, leading to variations in amplitude imbalance. Simultaneously, the phase response at port 2 also changes, presumably due to the influence of V_7 on C_{cb}. The simulation results demonstrate challenging simultaneous amplitude and phase imbalance reduction. The original design used $V_7 = 0.87$ V, as it provides the best phase response, i.e., the closest to 180°. However, the layout also introduces certain imperfections, such as amplitude and phase imbalances from the coupler, possible asymmetry, and additional parasitics. Together with previously discussed distorted S_{21} constellation diagram from the Gilbert cell, this contributes to the accumulated phase-amplitude error. Fig. 3.18d shows S_{21} behavior after the EM simulation (brown response, $V_7 = 0.87$ V). To decrease the amplitude

deviation V_7 was adjusted back to 0.8 V, resulting in the purple, improved, constellation in Fig. 3.18d.

The bias network provides the circuit with voltages V_{1-6} operating similarly to the previous phase shifter. Separate networks for $V_{5,6}$ and V_7 have the advantage of an additional possible tuning of currents flowing through different branches after the circuit is fabricated. The phase shifter including bias networks consumes 37 mW of DC power, from which the Gilbert cells use 22 mW from a 3.3 V supply voltage.

3.3.2 Experimental Results

The chip microphotograph is shown in Fig. 3.19. The active circuit core occupies 0.026 mm^2 of the die area and is shown in detail in the zoomed-in photograph.

The transistor core in Fig. 3.19d has been designed targeting a trade-off between a simple connection with the coupler, layout symmetry to avoid the phase error increase, and avoiding output lines being too close to each other because of the opposite polarity of the signal.

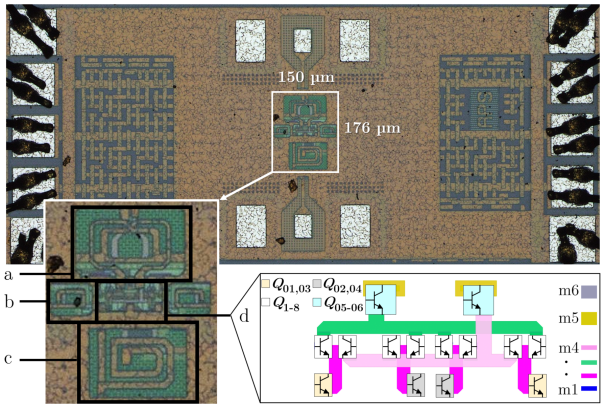


Figure 3.19: Chip photograph: (a) transformer, (b) multi-layer inductor, (c) quadrature coupler, (d) core. [4] ©IEEE

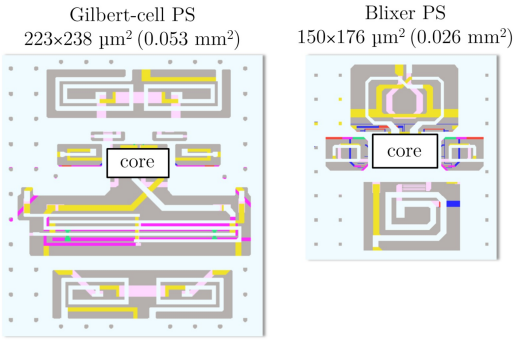


Figure 3.20: Comparison of phase shifters using Gilbert cell and Blixer topologies.

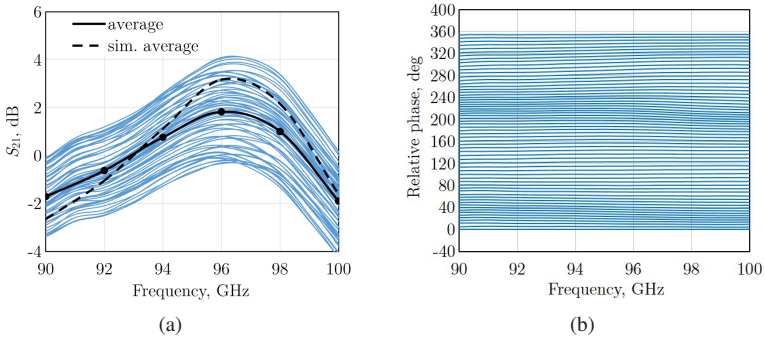
To assess the achieved area reduction let us compare the single-ended version of the previous phase shifter (section 4.2) that uses the original Gilbert cell topology with the Blixer-based version. Fig. 3.20 demonstrates the die area reduction by half mainly because of input- and output balun function integration into the Blixer-like transconductance stage and the transformer, respectively.

The circuit has been characterized using the Agilent N5251A broadband system using an N5247B PNA-X in a 2-port configuration. In addition to on-wafer calibration, RF pads open/short de-embedding has been performed using fixturing operations of the PNA.

The measured gain for every phase setting is presented in Fig. 3.21a. A solid black line represents the average measured gain that achieves 1.8 dB at 96 GHz, whereas a dashed line shows a simulated average gain for comparison. The relative phase response is presented in Fig. 3.21b.

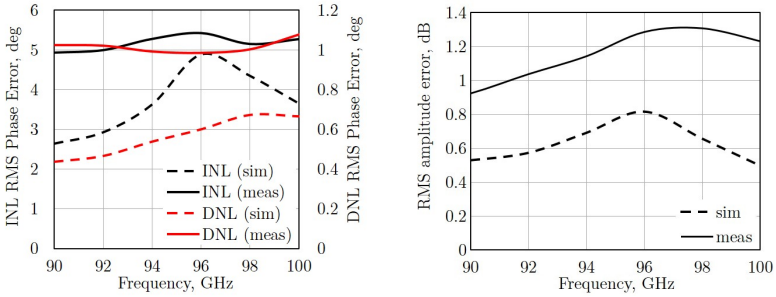
Fig. 3.22 shows the amplitude and phase RMS errors calculated from simulated and measured responses. At 90−100 GHz amplitude RMS error remains lower than 1.3 dB. The circuit demonstrates phase errors lower than 5.4° and 1° in INL RMS and DNL RMS definitions, respectively, without additional digital calibration.

Simulated OP_{1dB} for all phase settings is shown in Fig. 3.23. According to these results, the original design with $V_7 = 0.87$ V with equal currents flowing through $Q_{01,03}$ and $Q_{02,04}$ exhibits the average OP_{1dB} of −5.4 dBm. It drops



(a) (b)

Figure 3.21: Measured gain (a) and relative phase for all phase settings (b). [4] ©IEEE



(a) (b)

Figure 3.22: Measured phase (a) and amplitude (b) RMS error. [4] ©IEEE

to −9.8 dBm with $V_7 = 0.8$ V that was previously chosen to reduce the amplitude variation across phase settings. The main reason for the compression point deterioration is the current reduction through $Q_{01,03}$ due to this change. This could be potentially improved by creating the same difference between $Q_{01,03}$ and $Q_{02,04}$ collector currents (for amplitude RMSE reduction) without changing the total current through all branches. The compression point measurement was performed only at the most critical phase points, i.e., those with the largest expected difference in $OP_{1\text{dB}}$. For $V_7 = 0.8$ V, the results showed the average $OP_{1\text{dB}}$ of −8 dBm.

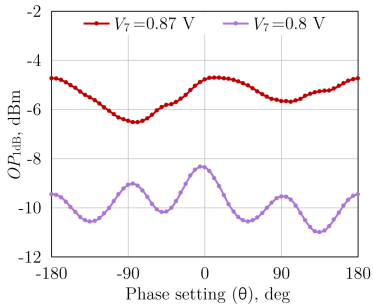


Figure 3.23: Simulated OP_{1dB} for all phase settings.

Overall, this prototype exhibits a narrower bandwidth compared to the previous version due to the transformer-based impedance matching and the narrow-band coupled-line coupler instead of the Lange coupler. However, the achieved bandwidth and phase resolution meet the requirements. Uncalibrated amplitude and phase RMS error of 1.3 dB and 5.4°, respectively, remain in a similar range as for the first circuit. This phase shifter was not optimized in terms of linearity. Instead, the goal for this prototype was to reach the similar phase control performance, while applying the above-explained area-reduction strategies. The achieved reduction of 50% is considerable noting that the performance degradation is minimal.

3.4 Bidirectional Active Phase Shifter

Parts of this section include material previously published in [2].

3.4.1 Circuit Description

For many systems, the use of passive phase shifters is commonly considered advantageous because of their reciprocity. In other words, when operating in two directions, i.e. transmitting and receiving, one passive phase shifter is equivalent to two active ones, separately used for each direction. This has to

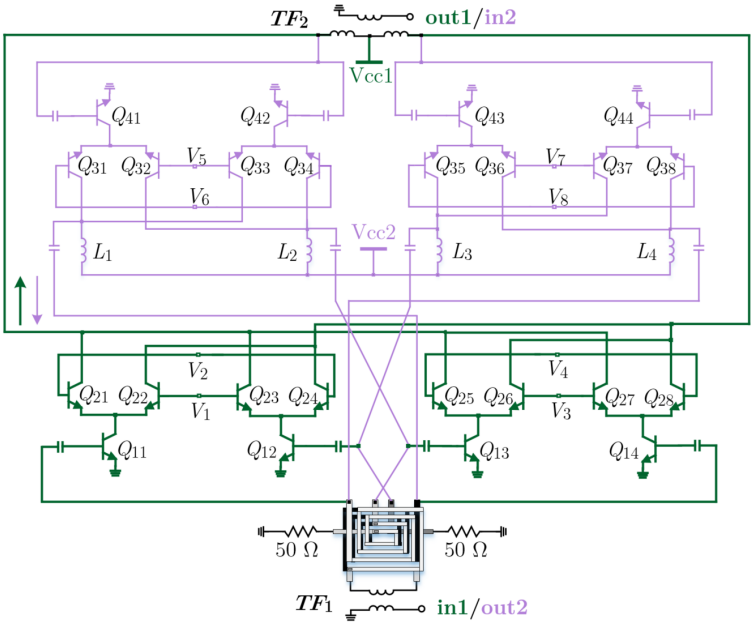


Figure 3.24: Simplified schematic. [2] ©IEEE

be taken into account for a fair comparison, especially when considering the miniaturization aspect.

This section discusses a different approach, aiming to combine the advantages of both passive and active phase shifters and mimic the reciprocity functionality in an active phase shifter. The idea is based on work [GCSC18] that presents a bidirectional one-stage differential amplifier. Instead of placing the whole circuit twice, the authors double only the core and re-use the input and output matching networks for both directions.

The proposal is to adapt and expand this approach to the active Gilbert-cell-based phase shifter. A simplified schematic is shown in Fig. 3.24. The circuit includes two cores connected in a way that a differential coupler and transformers TF_1, TF_2 are re-used.

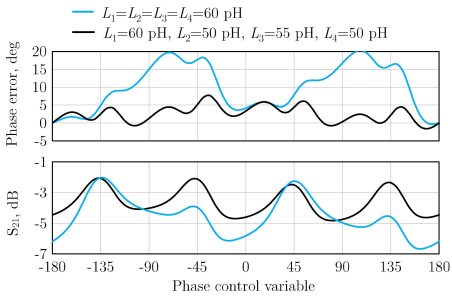


Figure 3.25: Simulated effect of unequal L_{1-4} on phase and amplitude variations at 95 GHz. [2] ©IEEE

- **Direction 1** (green-colored) uses a conventional topology with a differential I/Q splitter (discussed in Chapter 2, Fig. 2.7) at the input, TF_1 and TF_2 used for input and output matching, respectively, and additionally providing single-ended to differential conversion. The supply voltage Vcc1 is supplied through the center tap of TF_2.

- **Direction 2** (purple-colored) would ideally be a flipped version of direction 1. However, since the coupler is placed at the output between the core and TF_1, voltage Vcc2 has to be supplied conventionally by using shunt inductors L_{1-4}. This location of the coupler demonstrated an inherent performance degradation in comparison to the previous case, causing larger amplitude and phase errors, when controlling the phase. This effect is presumably caused by the coupler imbalances introduced at the output of Q_{31-38}, thus affecting their output impedance. To compensate for these imbalances, inductors L_{1-4} are made intentionally slightly unequal. Fig. 3.25 demonstrates the simulated achieved improvement i.e. reduced amplitude variations and phase error compared to ideal phase states at 95 GHz.

Bias voltages for transistors $Q_{11-14,21-28}$ and $Q_{31-38,41-44}$ are provided through two separate bias networks following the same approach as in the above-presented designs. Since there are no switches introduced in the RF path, the two cores can not be used simultaneously. The direction of operation is defined by the bias network that is currently activated. In practice, this is not a limitation as mm-wave communication systems are mostly time-duplexed systems.

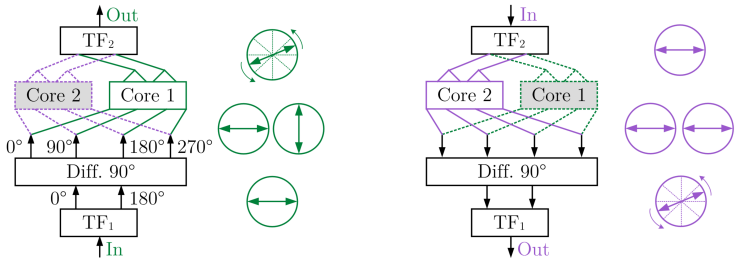


Figure 3.26: Circuit's block diagram: (a) direction 1, (b) direction 2. White and grey represent activated and not activated components.

For the presented prototype, all transistors use the smallest one-finger device, thus leaving room for further optimization. The main challenge is a simultaneous change of on- and off-state impedance when changing device size. Therefore, an optimized active core for operating in one direction can introduce certain off-state impedance, influencing the performance of the phase shifter in the opposite direction. However, since the specifications for components in transmit- and receive chains are commonly not identical, this bidirectional phase shifter can be optimized to have intentionally different performance in the forward and reverse directions of operation.

In contrast to the previous prototypes, no common-base buffer is included for any direction of operation. Since such a current combining is only possible for the direction 1, it was decided not to further increase the circuit's asymmetry by adding the buffer only to half of the circuit. However, depending on the Rx and Tx specifications such asymmetry can be introduced on purpose. The principle of operation is illustrated separately for each direction in Fig. 3.26. The block diagrams shows the fundamental difference between two directions and the reason why the outputs of core 2 can not be combined in a similar way like direction 1. Since the 90° phase difference is introduced by the differential coupler, the outputs of the core 2 are simply two differential signals. Therefore all 4 outputs have to reach the coupler separately to reach all four quadrants of the 360° circle. The situation for the direction 1 is different because the 90° phase shift is introduced at the input of the core 1 and combining the outputs performs the vector summation.

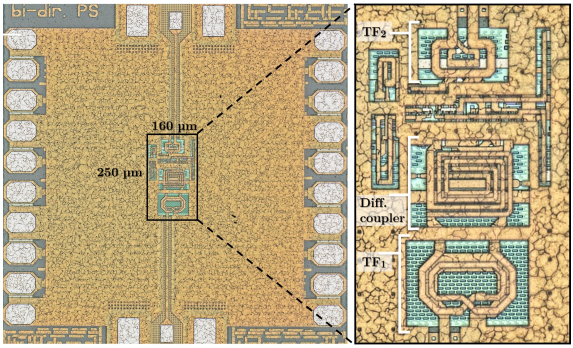


Figure 3.27: Chip photograph. [2] ©IEEE

The power consumption of the circuit without and with phase control bias networks is 38 mW and 62 mW, respectively, from a 3.3 V supply voltage. Fig. 3.27 shows the chip microphotograph with a zoomed-in core part of the circuit that occupies 0.04 mm^2 of the die area.

3.4.2 Experimental Results

Fig. 3.28 shows the frequency behavior of the measured gain for all phase settings in both directions, as well as measured and simulated average gain. In both directions, the phase shifter exhibits comparable performance, only with a slight frequency shift, when operating in the reverse direction. The maximum measured average gain is −7.4 dB (direction 1) and −8.2 dB (direction 2).

In both directions, the circuit exhibits higher insertion loss compared to the simulation, especially visible at the center frequency due to the flatter response of the measured average S_{21}. Such frequency behavior can be an indication of an additional resistive loss not accounted for in the simulation. To investigate this effect, both simulated a measured input and output impedance have been compared, as shown in Fig. 3.29, for two cases: 1) the phase shifter is active in one direction, 2) not active, both cores are deactivated. The idea behind this comparison is to see if a non-active core presents in parallel to an active one an impedance that deviates from the model. The results indicate a larger change

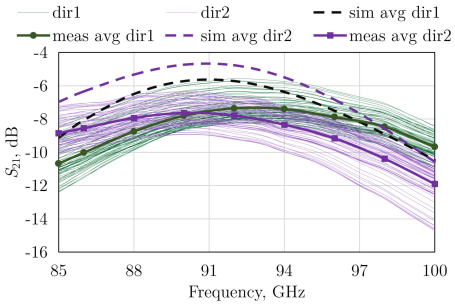


Figure 3.28: Measured gain for all phase settings. [2] ©IEEE

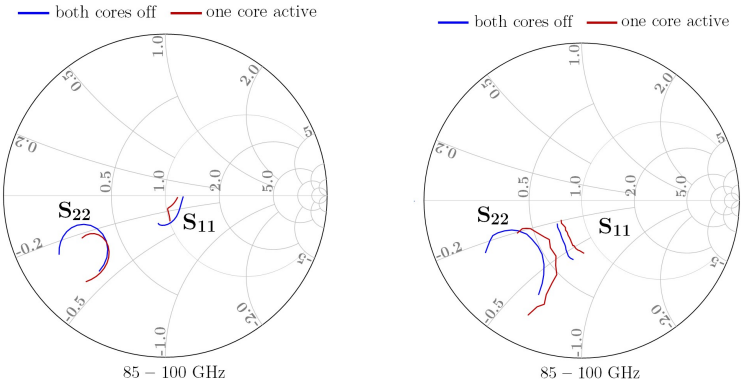


Figure 3.29: Simulated (a) and measured (b) return losses.

in the measured active part of both S_{11} and S_{22} compared to the simulation, therefore presumably causing a change in the insertion loss.

To perform the amplitude and phase calibration of the phase shifter, i.e., to obtain one set of points (per direction) with minimized errors, the measurement with 4-bit gain control and 8-bit phase control was performed. The results at 92 GHz and chosen points for 6-bit phase operation are presented in Fig. 3.30. This procedure ensures the use of the circuit with its best possible performance.

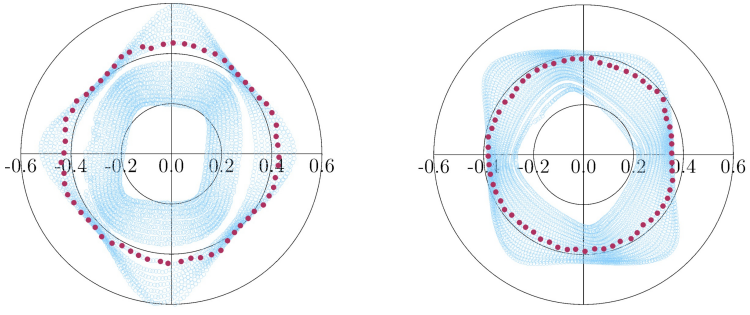


Figure 3.30: S_{21} constellation diagram with 4-bit gain and 8-bit phase control at 92 GHz in directions 1 (a) and 2 (b). [2] ©IEEE

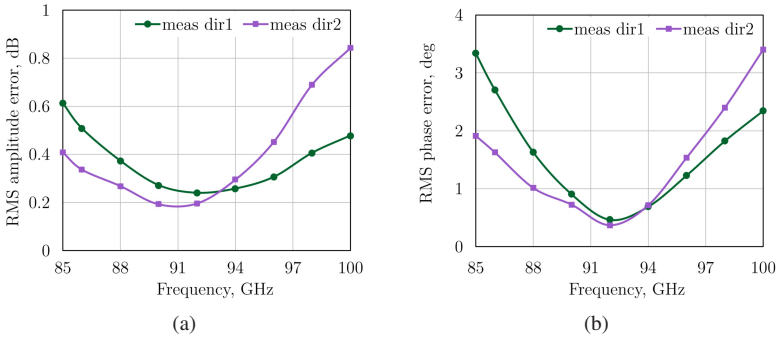


Figure 3.31: Calibrated measured amplitude (a) and phase (b) RMS error. [2] ©IEEE

Fig. 3.31a shows the corresponding amplitude RMS error for 4-bit amplitude resolution. The best achieved values after calibration are 0.24 dB and 0.19 dB, while the RMS error does not exceed 0.61 dB and 0.8 dB within 85−100 GHz in the first and second directions, respectively. The performance can be improved further using a higher bit resolution, however not explored due to exploding measurement time. Fig. 3.31b presents the frequency dependence of the phase RMS (INL) error. The calibrated phase response achieves the minimum values of 0.46° and 0.37° of the RMS error, while within 85−100 GHz it does not exceed 3.4°.

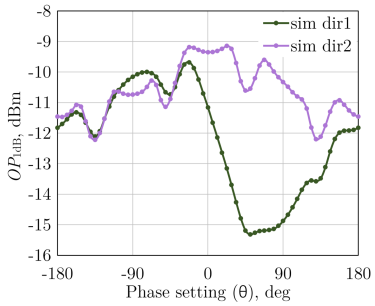


Figure 3.32: Simulated OP_{1dB} for all phase settings.

Simulated OP_{1dB} for two directions and all phase settings are shown in Fig. 3.32. As previously mentioned, in a real system, linearity specifications for Tx and Rx paths are fundamentally different. Therefore, this phase shifter was not optimized in terms of linearity and compression point. Instead, the focus was on achieving comparable phase performance in two directions, namely amplitude and phase RMS error.

The presented bidirectional phase shifter covers the desired frequency range with the required phase resolution in two directions. After additional digital calibration, the amplitude and phase RMS errors are reduced. At 100 GHz the phase RMS error of 3.4° slightly exceeds the required 2°, but it can be corrected by shifting the calibration frequency from 92 GHz, e.g., closer to 96 GHz. The original 92 GHz was only chosen because it is the center frequency of the achieved 3-dB bandwidth. The amplitude RMS error meets the requirements. Compared to the previous circuits, the gain was the main sacrifice, whereas the reduced die area for the TRx operation is the main advantage. However, as this circuit combines features of both active and passive phase shifters, such performance trade-offs are rather expected.

3.5 Conclusion

This chapter presents three active phase shifters, designed for a beamforming network of *W*-band phased arrays. All designs have been fabricated in the same IC technology and successfully characterized. The phase control in all cases

is based on vector summation and implemented using the current steering mechanism. The main purpose of this chapter is to present several effective topology modifications and techniques applied to the conventional Gilbert cell for the circuit's miniaturization without sacrificing its functionality. Interestingly, many techniques have already been present in the literature, but were previously utilized either in other building blocks (e.g. Blixer) or in simpler structures (one-stage bidirectional amplifier) and have not become widely used since then. The potential improvement seemed promising, therefore the ideas were successfully adapted resulting in the most compact phase shifters among those available in the literature. However, as the functionality is confirmed, there is room for further optimization for the final practical implementation. Performance summary is included in Table 3.1, where Version 1, 2, and 3 correspond to sections 3.2, 3.3 and 3.4, respectively.

Table 3.1: Phase Shifter Performance Summary

	Tech.	Type	Bi-dir.	Freq, GHz	Phase resol., bits	Avg. gain, dB	Gain RMSE, dB	Phase RMSE, deg	IP_{1dB}, dBm	P_{DC}, mW	Area, mm^2
[LCHH20]	130-nm SiGe	active	–	72–82	6	7	0.76	3.5	–10	60	0.31
[KH23]	28-nm CMOS	active	–	80–100	6	–9	0.24	2.2	–1	7.7	0.11
[AK18]	130-nm SiGe	hybrid	–	92–100	5	9.5	1.8	5	–13.6	31	0.82[3]
[NVGS+15]	120-nm SiGe	hybrid	+ –	88–96	5	–3.5	2.4	12	–13[2]	–	0.25[4]
[LW15]	130-nm SiGe	passive	+	58–64	cont.	–10	0.7[1]	–	13.8	0	0.16
[WYW+22]	65-nm CMOS	passive	+	90–100	6	–18	2.4[1]	10.5	–	0	0.193
Version 1	SiGe	active	–	86–106	6	2.3	1	6.6	–1.7	49	0.027[5]
Version 2	SiGe	active	–	90–100	6	1.8	1.3	5.4	–10.8	37	0.026
Version 3	SiGe	active	+	85–100	6	–7.4/ –8.2	0.6/ 0.84	3.4	–3.8	62	0.04

[1] max variation [2] for inverting amplifier [3] incuding LNA [4] estimated from chip photo [5] w/o baluns

4 Q- and V-Band Building Blocks for Space Electronics

4.1 Q- and V-Band Frequencies in Satellite Communication

The new generation of LEO satellite constellations with Q/V-band user up- and downlinks is anticipated, as discussed in Section 1.2. While this transition to higher frequencies is being explored, Q- and V-bands have already been adopted for feeder links, i.e., communication links between satellites and ground stations (gateways) to relay data that is later distributed to users. However, current systems employ mechanical steering, which necessitates a complex ground infrastructure. An alternative implementation based on electronic beam steering using phased arrays is currently under research. In 2024, ESA announced a tender to develop an integrated broadband Q- and V-band beamforming network for feeder links in Very High Throughput Satellites (VHTS) [esa]. The aforementioned activities and growing scientific interest indicate that future developments in satellite communication will likely focus on these frequency bands.

This chapter presents the design and integration of components developed as part of a research project with the German Aerospace Center (DLR). A complete broadband system is planned to implement self-calibrating functionality (built-in self-test) in space. The following sections discuss a part of this system, specifically a so-called Channel RFIC, which is essentially a highly linear chain providing phase and gain correction in Q- and V-band. In the receiver, this subsystem is positioned after an external LNA. An identical CRFIC is implemented on the transmitter side as one of the driver stages before the microwave power module based on a traveling wave tube.

4.2 Definitions and Specifications

In this chapter, the focus was on the following performance metrics.

- **Bandwidth** of the channel RFIC should cover part of the Q-band and possibly extend to the V-band, specified here as 37.5−42.5 GHz and 54.2−58.2 GHz, respectively.
- **Dynamic range**: The chain is required to cover an input power range between −20 dBm and −60 dBm. This requirement implies that the compression point $IP_{1\text{dB}}$ should be better than −19 dBm.
- **Gain range**: 40 dB. The power gain should be sufficient to ensure an output power in the range between −20 dBm and −32 dBm. This specification is illustrated in Fig. 4.1. P_{out} of −20 dBm is preferred.
- **Linearity** is one of the main design challenges, expressed in terms of IMD3 with a target value of 40 dBc with the tone spacing of 100 MHz for all gain settings.
- **Noise figure** (NF) is preliminary specified within 8−18 dB, where 8 dB and 18 dB correspond to the highest and lowest gain of the chain. This requirement presents a significant design challenge as well considering several attenuation stages required.
- **Phase control** with a 20° step is specified within a 360° phase shift range.

A straightforward implementation to cover the required bandwidth would involve two chains optimized separately for the specified Q- and V-bands and

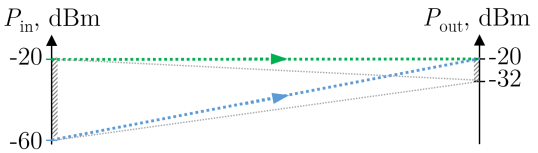


Figure 4.1: Specified dynamic range of channel RFIC. Blue and green lines correspond to preferred P_{out} of −20 dBm. Grey lines are an example of an alternative design goal within the specifications.

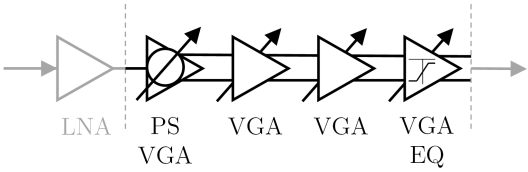


Figure 4.2: Block diagram of the proposed channel RFIC. Components between the dashed lines are discussed in this thesis.

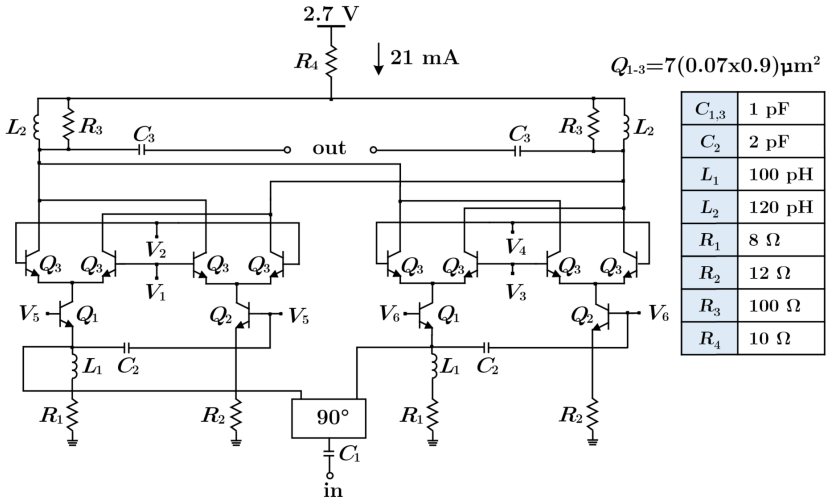
connected into one switchable block. In this thesis, another approach is explored to achieve facilitated area efficiency and reduced overall system complexity. The idea is to develop a single chain operating over a broad frequency range of 37−60 GHz instead of switching between two chains.

Fig. 4.2 presents the block diagram of the proposed channel RFIC. This chapter expands the miniaturization strategies discussed in Chapters 2 and 3 to the subsystem level by reusing components for multiple functions simultaneously. The symbols, which slightly deviate from conventional notations, illustrate these functions. The phase shifter performs the required phase correction and contributes to the gain control range provided by the following VGA stages. One VGA was designed to integrate an additional gain equalization function. The following sections discuss these two building blocks in detail. The order of components is selected to optimize the worst-case noise performance of the chain, which will be discussed in the next subsection.

4.3 Active Phase Shifter for Broadband Phase and Gain Control

4.3.1 Circuit Description

An important aspect to mention is that when discussing broadband phase shift, the term does not refer to instantaneous bandwidth, as this would contradict the discussion on the bandwidth limitations of phase shifters in Section 3.1.1. Instead, in this chapter, the term 'broadband' indicates the ability to support operation separately in two narrow frequency bands, as specified above.



$C_{1,3}$	1 pF
C_2	2 pF
L_1	100 pH
L_2	120 pH
R_1	8 Ω
R_2	12 Ω
R_3	100 Ω
R_4	10 Ω

Figure 4.3: Simplified schematic.

Fig. 4.3 shows the simplified schematic of the phase shifter. The circuit uses the Blixer-based topology, similar to that presented in Section 3.3. The main differences from the previous design include device size optimization and resistive emitter degeneration to enhance the circuit's linearity.

Instead of the narrowband transformer-based output matching network used in the previous design, this circuit employs an LC network with an additional parallel resistance, R_3, for bandwidth extension. Since the output is kept differential, the Blixer topology provides a natural transformation from a single-ended LNA to the following differential VGA stages in the chain. This offers additional flexibility in choosing the VGAs' gain control mechanism.

The phase control is implemented as discussed in Chapter 3, i.e., by changing V_{1-4} using the control voltages $V_{\mathrm{I,Q}\pm}$ through the bias network from Section 3.2.1. The impact of the chosen b coefficient in the control equations $V_{\mathrm{I}\pm} = a \pm b\cos(\theta)$ and $V_{\mathrm{Q}\pm} = a \pm b\sin(\theta)$ was previously presented in Fig. 3.9. In Chapter 3, b was chosen as a trade-off to avoid increased amplitude and phase errors (when b is large) while not introducing significant insertion loss (when b is small). However, for this chain, the latter mechanism can be beneficial, as

it allows one building block to independently control phase and attenuation by changing θ and/or b. This means that such a phase shifter additionally covers part of the required gain range, potentially reducing the number of VGA stages in the chain.

In the low-gain setting, the phase shifter, used simultaneously as an attenuator, is expected to inherently present a higher NF compared to a VGA stage in the same attenuation setting due to the additional I/Q splitting loss at the input. Since no amplification stages, other than the LNA, are used in the low-gain scenario, the phase shifter is placed directly after the LNA. In the proposed channel RFIC, the noise contribution of the attenuating phase shifter experiences the best suppression in the chain.

The chip photograph, magnified core layout (a) and coupler layout (b) are presented in Fig. 4.4. The layout was designed following the miniaturization approaches and good practices previously discussed in Chapter 3, such as the use of multi-layer inductors and design symmetry. The I/Q splitter is implemented as a twice-folded Lange coupler to achieve an optimum compromise between area and bandwidth. This solution is more compact than the conventional Lange coupler while still offering greater bandwidth than the tightly wound

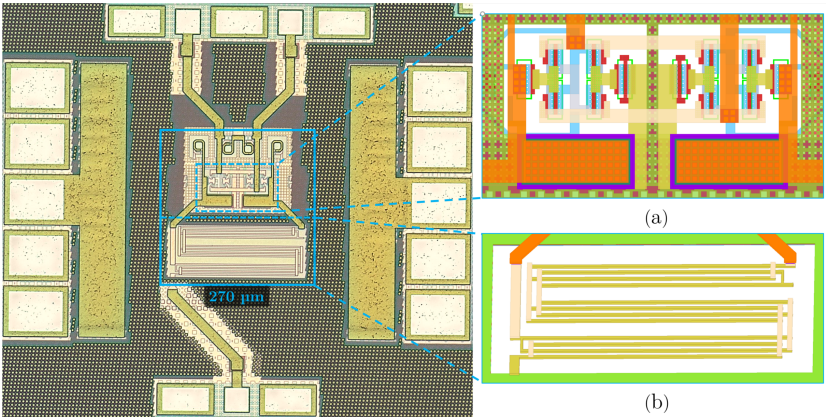


Figure 4.4: Chip photograph of the phase shifter; core layout (a) and folded Lange coupler layout (b).

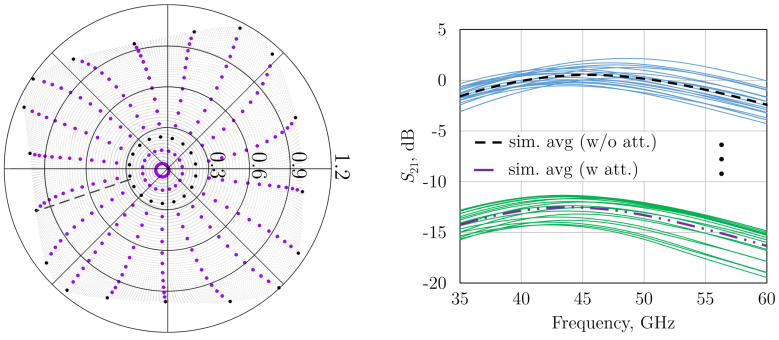
spiral coupler, both of which were presented in Section 2.2. The functional core area of the phase shifter is approximately 0.073 mm^2.

4.3.2 Simulation Results

In this section, the final full-layout EM simulation results for the presented phase shifter are discussed. The concept of fully independent phase and gain control is valid only in an ideal theoretical scenario. Fig. 4.5a shows the simulated S_{21} for various settings at 40 GHz. Each circle with bold dots corresponds to a fixed value of the b coefficient, with θ swept from $-180°$ to 180° in 20° increments. Multiple circles represent different b values in the range of 0.01 V to 0.28 V, with an arbitrarily chosen step for demonstration purposes only.

The smallest displayed circle (b = 0.01 V) illustrates one of the main limitations of integrating VGA functionality into the phase shifter. The amplitude imbalances in the circuit, typically acceptable for standard phase shifter operation (i.e., in the high-gain setting) and evaluated using the RMS error definition, can become critical in low-gain settings. In this example, the smallest circle is no longer centered around 0, but is almost completely shifted to the left half of the polar plot. This indicates that although attenuation is achieved, the phase shifter's performance is disrupted, as the circuit cannot reach half of the settings for the full 360° range. For this reason, the b range was preliminary chosen between 0.05 V and 0.28 V, corresponding to the highest chosen attenuation state and no attenuation, respectively. These two sets of dots are shown in black.

The second problem is phase drift across different gain settings, evident from the curved shapes formed by the dots with fixed θ (from the edge towards the center), rather than forming straight lines. However, the ambiguity of the grey dots in the figure – simulated with higher gain and phase resolution – demonstrates the potential to address both problems to some extent. This can be achieved by manually selecting the optimal points, such as those along the dashed line, rather than the adjacent raw purple curve, for a fixed θ. Similarly, for a fixed b, the points forming the "better" circle (as previously shown in Fig. 3.30 for the bidirectional phase shifter) can be selected. Such adjustments to the settings are more reasonable when using measured data. Therefore, for



(a) (b)

Figure 4.5: Simulated S_{21} for different phase and gain settings (a). Black dots represent preliminary chosen settings without and with maximum attenuation at 40 GHz. Corresponding simulated frequency dependence for these two sets (b).

further simulations, the attenuated and non-attenuated sets mentioned above are selected and displayed in Fig. 4.5b, represented in green and blue, respectively. Multiple curves correspond to different phase settings ($\theta = -180° : 20° : 180°$) for each value of b. In both cases, the 3-dB bandwidth of the average gain covers the combined frequency range of interest, i.e. 35–60 GHz.

Fig. 4.6 presents the simulated IMD3 at 40 GHz and 56 GHz (the center frequencies of the specified Q- and V-bands) using the tone spacing of 100 MHz for the same sets of points. A distinctive and advantageous feature of the employed gain control scheme is the relatively small variation in IMD3, as indicated by the nearly overlapping green and blue lines. However, the linearity varies across different phase settings. This effect may be slightly reduced by selecting points with smaller amplitude error during phase control, as discussed earlier.

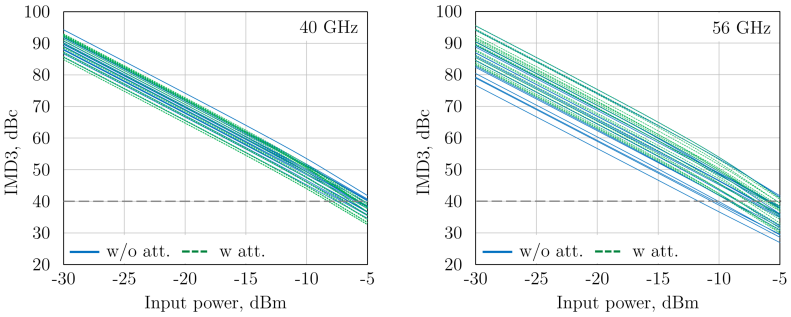


Figure 4.6: Simulated IMD3 at 40 GHz (a) and 56 GHz (b) for different phase settings without and with attenuation.

4.3.3 Experimental Results

The results of the small-signal characterization are presented in Fig. 4.7. Fig. 4.7a compares the measured and simulated gain for one raw reference set of phase settings, without additional attenuation applied. The simulation results were previously shown in Fig. 4.5b plotted in blue (marked as w/o attenuation). The measured S_{21} constellation diagram in Fig. 4.7b demonstrates phase-shifting functionality combined with attenuation control. Red dots illustrate achievable settings for 20° phase control with minimized amplitude error. This procedure can similarly be repeated for intentionally attenuated gain states. Moreover, the characterization can be expanded to provide higher phase and gain resolution.

Two-tone characterization was conducted using the Swept IMD measurement class on the PNA-X network analyzer. Fundamental tones and third-order intermodulation products were recorded across varying input power levels. The measurement results for previously mentioned reference set of states are displayed in Fig. 4.8 at center frequencies of 40 GHz and 56 GHz, with a tone spacing of 100 MHz. To reduce the measurement duration, the results were obtained for the settings corresponding to 45° phase control steps. At lower input power levels, intermodulation products fall below the sensitivity threshold of the PNA-X, resulting in a deviation from the expected slope.

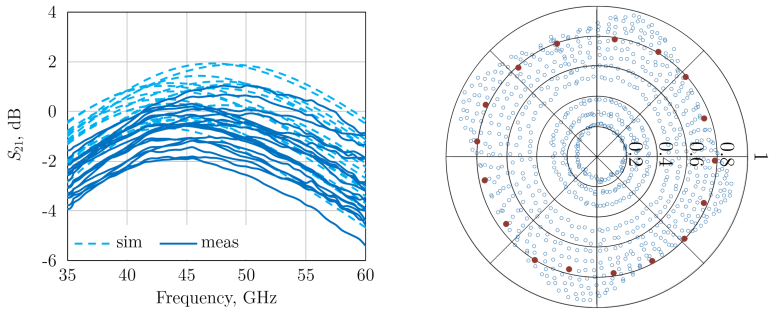


Figure 4.7: Measured gain for one set of phase states without attenuation (a); measured S_{21} constellation diagram at 40 GHz (b).

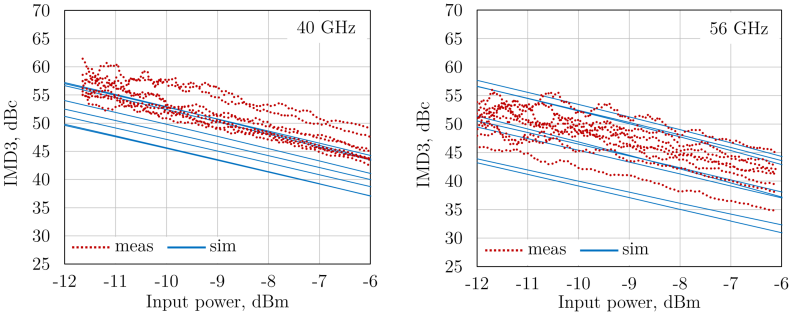


Figure 4.8: Measured IMD3 at 40 GHz (a) and 56 GHz (b) for several phase settings without attenuation.

Generally, larger discrepancies between measurement and simulation results at 40 GHz align with the small-signal performance trends, which demonstrate closer agreement with simulations at 56 GHz than at 40 GHz.

The measured data enables linearity assessment in terms of IIP3, calculated as follows:

$$\mathrm{IIP3} = \frac{\mathrm{IMD3(dBc)}}{2} + (P_{\mathrm{in}}(\mathrm{dBm}) - 3). \tag{4.1}$$

Here, $P_{in} - 3$ represents the input power level of each individual tone, while the input power in Fig. 4.8 denotes the combined input power of the two tones. Based on this data, the circuit demonstrates a minimum IIP3 of 12 dBm at 40 GHz and 8 dBm at 56 GHz.

4.4 Broadband Variable Gain Amplifier with Gain Equalization

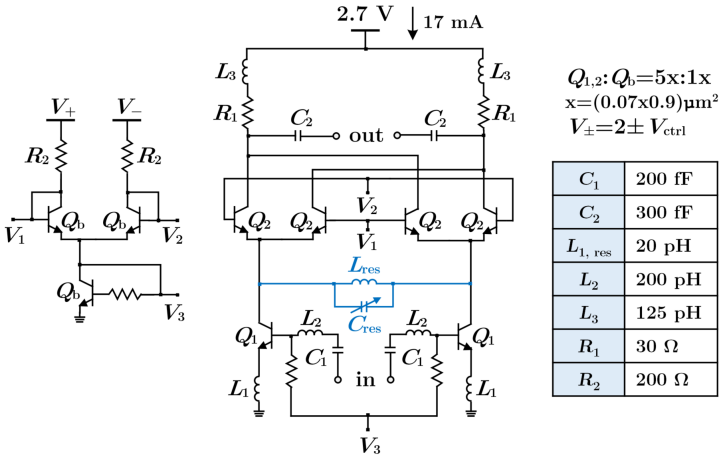
4.4.1 Circuit Description

The schematic of the subsequent building block in the chain, the VGA, is shown in Fig. 4.9. The topology is based on the same gain control mechanism discussed in the previous section, which promises almost constant linearity across settings.

The VGA is placed after the phase shifter that in the attenuation regime will lead to not suppressed noise contribution of the VGA. Therefore, additional efforts have been made to improve the NF by employing conventional strategies for simultaneous noise and power matching. This is achieved through the choice of transistor size and the use of emitter degeneration L_1. Further details on such optimization are discussed in the following chapter, in the context of LNA design.

The original goal was to develop a VGA with a flat frequency response and reduced NF. This initial design phase was implemented using the components marked in black in the schematic. The gain is controlled by V_{ctrl}, which influences $V_{\pm}$ and, consequently, $V_{1,2}$ through the bias network. As previously discussed, reducing V_{ctrl} activates the branches with opposite signal polarities simultaneously, thereby providing attenuation.

In a conventional scenario, one or several equalizers would be developed as separate building blocks to adjust the resulting slope of the chain's frequency response. Instead, this thesis explores the compact and efficient integration of the equalization function into the VGA. Consequently, a resonator consisting of L_{res} and variable C_{res}, both marked in blue, was added between the differential branches. In this case, the equalizer operation is also based on destructive signal



C_1	200 fF
C_2	300 fF
$L_{1,\,res}$	20 pH
L_2	200 pH
L_3	125 pH
R_1	30 Ω
R_2	200 Ω

Figure 4.9: Simplified schematic.

summation, but at specific frequencies. The resonator is tuned to the frequency where no attenuation is required, meaning it effectively presents an ”open” state, and therefore no signal passes between the branches. Consequently, the slope is created between frequency points with and without additional attenuation.

The EM-simulated layout view of the proposed equalizing VGA is shown in Fig. 4.10. The right side includes the magnified transistor connections and the aforementioned resonator. The main functional part of the circuit occupies 0.017 mm^2 of die area.

4.4.2 Simulation Results

Fig. 4.11 illustrates the S_{21} frequency response for several gain settings of the VGA without the resonator. The gain control range between the highest-gain state and the preliminary chosen maximum attenuation is approximately 30 dB. However, larger attenuation is achievable if required.

The simulated equalizer settings, obtained by sweeping the control voltage V_{var} of C_{res} while the VGA remains at a fixed high-gain setting, are presented in

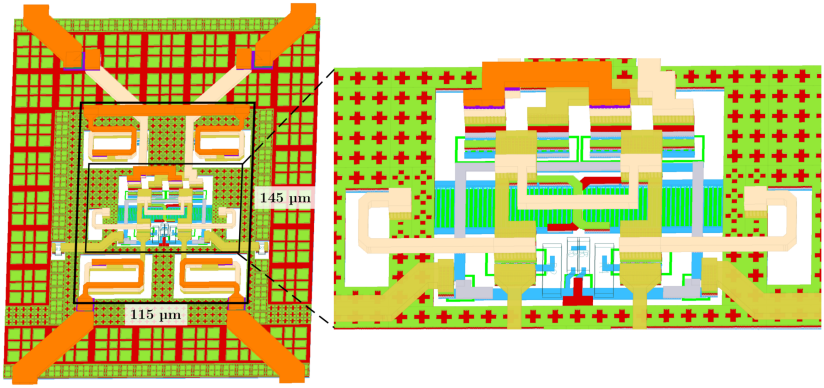


Figure 4.10: Final EM simulated layout of the VGA with magnified core.

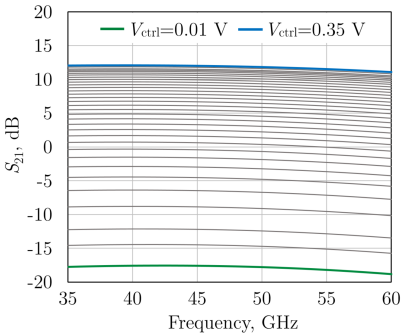


Figure 4.11: Simulated frequency response for different gain settings without the resonator. Blue and green correspond to the maximum gain setting and chosen maximum attenuation, respectively.

Fig. 4.12a. The combination of factors, such as the poor quality factor of the available varactor and layout parasitics, limited the gain slope and operational frequency range (as visible, for example, from the rounded positive slope green curve in the *V*-band). As the *Q*-band was prioritized in this project, the intercept point of maximum positive and negative slopes was intentionally shifted towards 40 GHz to ensure the best flexibility in the *Q*-band. The gain slope control added to the VGA using the presented approach requires no

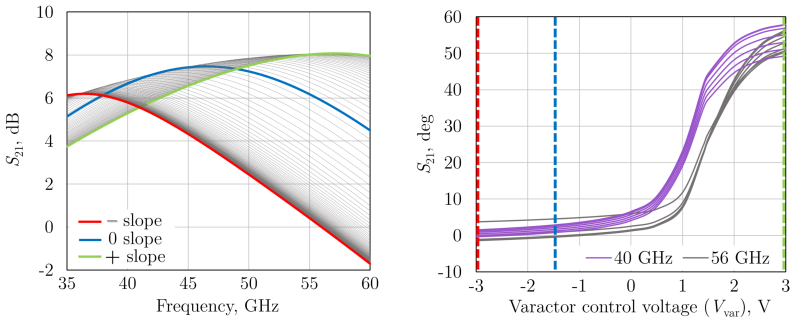


Figure 4.12: Simulated equalization settings in high-gain state of VGA with the resonator (a). S_{21} phase for different VGA gain states versus varactor control voltage for equalization control (b).

additional DC power and occupies a negligibly small additional area. However, the trade-off for this functionality can be observed when comparing the zero slope of the equalizing VGA with the highest gain setting of the conventional VGA (i.e., blue lines in Fig. 4.12 and Fig. 4.11). The equalizing VGA lost 4.6 dB of gain and exhibits 3 dB gain flatness within 35−60 GHz, compared to the 1 dB gain flatness achieved by the VGA without the resonator.

Fig. 4.12b illustrates an undesired effect of the presented gain slope control − additional phase rotation. The three vertical dotted lines correspond to the control voltage values V_{var} for the same three slopes shown in Fig. 4.12a. The curves of the same color represent the simulated S_{21} phase for a fixed frequency across different gain settings. Gain control without equalization exhibits noticeably less phase variation compared to when the equalization function is used. In general, phase variation introduced by components other than the phase shifter complicates phase control within the overall chain. In this particular case, the narrow-band LNA is specifically tuned for the Q-band, which implies that, in most cases, the positive slope will primarily be used to compensate for reduced gain in the V-band. Moreover, the full 360° phase coverage provided by the phase shifter allows for manual phase adjustments to counter this phase rotation. Since the channel RFIC is a single chain, rather than part of a phased array beamforming network, this adjustment becomes more manageable.

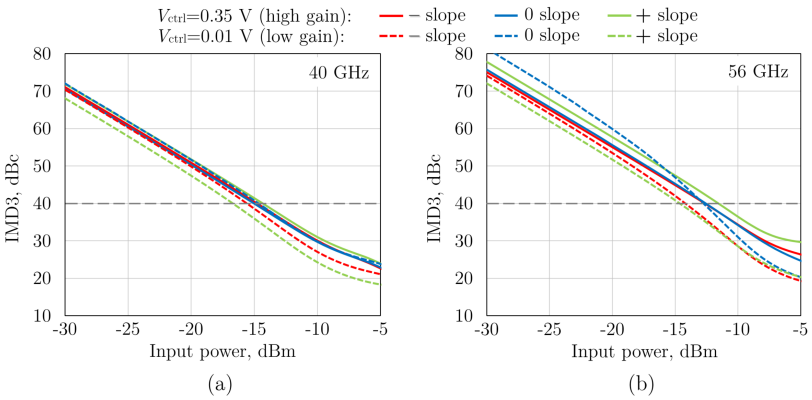


Figure 4.13: Simulated IMD3 at 40 GHz (a) and 56 GHz (b) for three main slope in high- and low-gain VGA states.

Fig. 4.13 shows the simulated IMD3 at 40 GHz (a) and 56 GHz (b) for the three above-highlighted gain slopes: negative, positive, and zero slope. Each slope is presented for both high- and low-gain VGA settings. The expected maximum input power range at this phase of the chain design was between −20 dBm and −15 dBm, depending on the attenuation distribution among the components. Except for one setting, the 40 dBc IMD3 requirement is primarily satisfied in the simulation. The largest variations in IMD3 occured between high- and low-gain settings. The gain slope control, in turn, introduced almost no change in the IMD3, an advantageous property presumably due to the resonator's placement. The resonator is well-isolated from both the input and output of the circuit and is not located directly in the RF path.

4.5 Channel RFIC Simulation Results

The layout of the developed channel RFIC is presented in Fig. 4.14. As previously discussed, the chain is designed to target a 40 dB gain control range with P_{out} of −20 dBm, corresponding to an S_{21} range of 0−40 dB for power-matched interfaces. An alternative design, which includes one less VGA stage (i.e., four components instead of five), is also sufficient for an output power

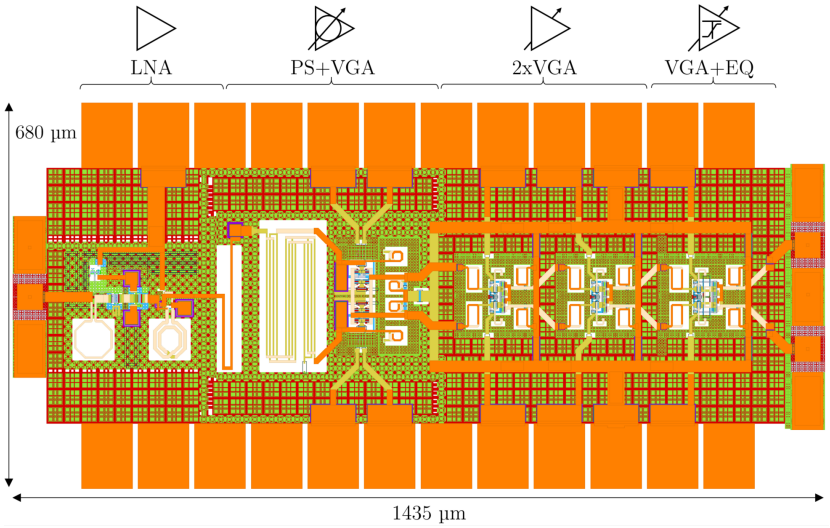


Figure 4.14: CRFIC layout. LNA was developed by other project partner and is not part of this thesis.

of −32 dBm. This configuration would provide gain control in the range of −12 dB to 28 dB. The presented building blocks are capable of additional attenuation without design modifications, while the maximum gain is constrained by the number of stages. Although this alternative chain design is an attractive option due to reduced area and power consumption, the resulting NF was considerably higher due to increased attenuation. Consequently, the final decision was made in favor of the first option with $P_{\text{out}} = -20$ dBm. The chain dissipates 270 mW of DC power and occupies 0.4 mm^2 of die area, excluding the pads and 0.98 mm^2 with pads.

The corresponding results of the piece-wise EM simulation including the LNA are presented in Fig. 4.15. The parameters S_{21}, NF, and IMD3 are shown for two primary gain settings, referred to as the high-gain and low-gain states. These correspond to the following edge cases: 1) $P_{\text{in}} = -60$ dBm, $P_{\text{out}} = -20$ dBm; and 2) $P_{\text{in}} = -20$ dBm, $P_{\text{out}} = -20$ dBm. The minimum NF for these states is 4.5 dB and 18 dB, respectively, which meets and partially outperforms the original requirements of 8−18 dB. However, due to the narrowband LNA

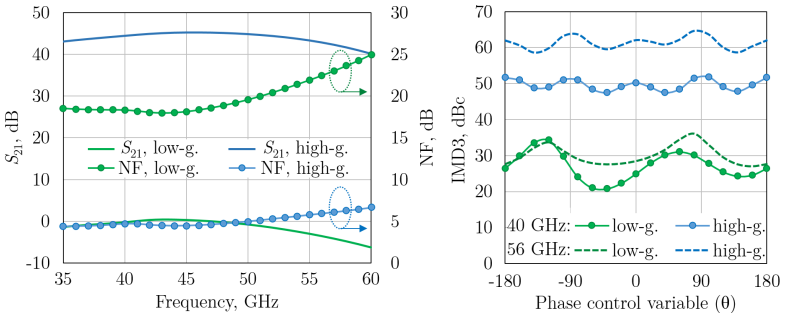


Figure 4.15: Simulated frequency response of CRFIC high- and low-gain settings and corresponding NF (a). Simulated IMD3 for the same gain settings versus phase control settings (b).

design, these NF values are not sustained across the entire operating frequency range.

The IMD3 in Fig. 4.15b was simulated at 40 GHz for different phase settings of the phase shifter. Overall, the individual blocks were optimized for bandwidth, IMD3, and area, with the component order in the chain prioritized for NF improvement. While this may not be the ideal configuration for IMD3, particularly in the low-gain setting, it allows for further optimization opportunities.

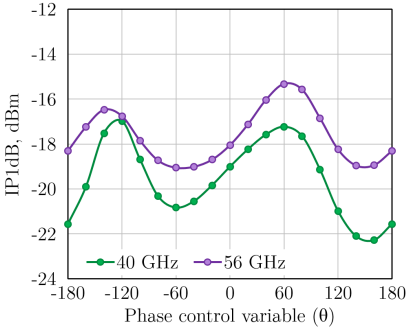


Figure 4.16: Simulated IP_{1dB} of CRFIC for different phase settings at 40 GHz and 56 GHz.

Fig. 4.16 presents the simulated IP_{1dB} for various phase settings of the phase shifter. At 56 GHz, the results meet the minimum IP_{1dB} requirement of −19 dBm. However, at 40 GHz, approximately half of the settings do not achieve this value. Since the maximum input power corresponds to the low-gain operation of the channel RFIC, several decibels of gain can still be recovered at the final stage (equalizer) to compensate for the compressed gain and to maintain the desired output power of −20 dBm.

4.6 Conclusion

This chapter presents a subsystem prototype for phase and gain control in the Q- and V-bands for self-calibrating satellite communication systems. The proposed design approaches for individual blocks focus on utilizing less conventional features of standard topologies to integrate multiple functions into a single component, enhancing system efficiency. Examples include the use of an active Blixer-based phase shifter as a variable attenuator, a low-noise VGA, and additional gain equalization achieved through a small modification of the VGA stage.

The resulting chain offers over 40 dB of gain control and 360° phase control, covering both frequency bands simultaneously, thereby eliminating the need for switchable alternatives. Potential future improvements include IMD3 optimization at the system level, linearization of gain control, exploration of phase-invariant VGA design options and the use of a broadband LNA.

All results presented in this chapter, except for the phase shifter, are based on EM modeling. Due to the project timeline, some prototypes have not yet arrived, and the complete chain has not been fabricated at the time of writing. Consequently, some characterization results are not yet available.

5 W-Band Low-Power Components

5.1 Effects Caused by High Power Dissipation

Power dissipation, as mentioned in Chapter 3, affects the performance of electronic components by increasing the die temperature of the IC. With higher operating frequencies and the miniaturization of electronics, smaller transistors are often densely packed into small areas, resulting in higher power density. Thermal effects limit a circuit's reliability by accelerating electronic failure mechanisms, thus reducing Mean Time To Failure (MTTF). This MTTF reduction was modeled and investigated in [LS14]. The authors discuss electromigration, high-temperature stress migration, thermal fatigue, drift of device parameters, ionic effects, increase in leakage current, and other effects. These effects become a major concern when aiming for long-term, reliable operation in harsh environmental conditions like, e.g. desert, and space.

In [NDS+20], NASA presented plans and activities to employ phased arrays in both space and aeronautics communication systems. It envisions a transition from large geostationary satellites to a distributed architecture consisting of many small satellites (CubeSats/SmallSats). In this scenario, the demand for so-called low SWaP-C (Size, Weight, Power, and Cost) becomes more critical. The complexity of thermal control in the dense packaging of SmallSats is discussed in detail in the SoA Small Satellite Technology Report [nas]. The smaller external surface of such satellites limits the radiator area, thereby deteriorating heat emission capability. Due to the limited volume and thus increased power density, some components lack a direct thermal path to the radiators, making heat dissipation more challenging. Apart from the generated heat, the satellite is exposed to various external effects, such as solar heating and heat reflection from the planet.

Reducing the power consumption of electronic components is therefore essential to maintain this complex thermal balance. Many cooling systems are

bulky and heavy and require their own power supply. They also occupy payload capacity that would otherwise be used for critical instruments and other components. Additionally, as satellites rely on solar panels and batteries, providing a high-power supply poses an additional design challenge. Considering these factors, high power consumption increases every SWaP-C element, which directly translates into reduced operational efficiency of the satellite.

In summary, high-power electronic components in phased arrays pose significant challenges for each layer of a potential 5G/6G network (as discussed in Section 1.2), namely terrestrial, airborne, and space. In space and airborne scenarios, the associated consequences can threaten the entire operation, whereas on land, they mainly increase costs and complexity. However, every factor becomes crucial when targeting volume production and global deployment.

The research trend of moving to higher operating frequencies is observed across all dimensions of the future multi-layer network, though at different paces. Therefore, similarly to Chapter 3, this chapter focuses on *W*-band frequencies, envisioned for future 6G systems. The goal of this chapter is to explore the possibility of reducing the power dissipation of components for a 100-GHz phased array receiver and the corresponding performance compromises.

5.2 Low-Power Low-Noise Amplifier

Parts of this section include material previously published in [1].

5.2.1 Performance Metrics

Two 100-GHz LNAs were fabricated to provide a quantitative performance comparison. The first circuit employs the optimal-performance design (here referred to as the standard design), whereas the second circuit represents the low-power variant.

During the design phase, the most relevant performance metrics were evaluated:

- **Noise Figure** (NF) of an LNA primarily impacts the total noise performance and, consequently, the dynamic range of a receiver.
- **Gain**, in this context, defines the suppression of noise added by the subsequent component, according to the Friis' formula. The higher the gain of the LNA, the less the noise contribution to the system.
- **Input impedance** is ideally matched to a 50-Ω antenna interface for a complete reflectionless power transfer. For many applications, however, $|S_{11}| \leq -10$ dB is considered an acceptable level of reflection.
- **Linearity** of the LNA, in this section, is discussed in terms of the compression behavior and is mainly expressed by $IP_{1\text{dB}}$.
- **Power dissipation** (P_{DC})

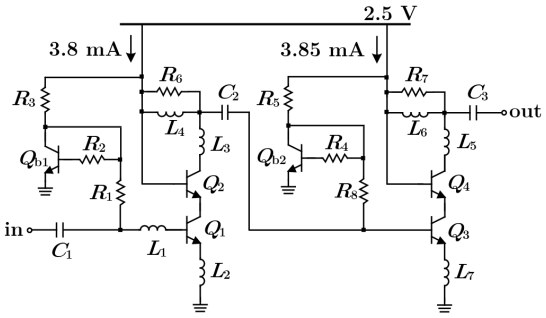
Both circuits were designed using the same technology and overall design procedure to ensure a fair comparison. The LNAs are based on a cascode topology to enhance the circuit's stability by minimizing the Miller effect. A two-stage design was chosen to increase the gain.

5.2.2 Optimal-Performance Design Description

Fig. 5.1 presents the schematic of the baseline LNA with a certain P_{DC} for optimal performance. For clarity, the figure does not include decoupling capacitors at the Vcc node. The circuit uses well-established methodologies to achieve simultaneous noise and power matching. Thus, the chosen emitter area for Q_1 corresponds to the real part of the optimum noise impedance S_{opt} approaching 50 Ω. S_{opt}, when presented at the input of an LNA, ensures the minimum noise figure NF_{min}. At the same time, the emitter-degeneration inductor L_2 is used to increase the real part of S_{11} to meet the requirement $S_{11} = S^*_{\text{opt}}$.

Components $L_{3,4}$, R_6, and C_2 form an inter-stage matching network, whereas the output matching network uses $L_{5,6}$, R_7, and C_3. Resistors $R_{6,7}$ provide additional stabilization and broaden the bandwidth by reducing the Q factor of the matching networks.

The bias network in the first stage consists of R_{1-3} and Q_{b1}, which form a current mirror. Resistors $R_{1,2}$ are scaled to accommodate different base



Q_1:$Q_{2\text{-}4}$:$Q_{b1,b2}$=4x:5x:1x
x=(0.07x0.9)µm²

C_1	1 pF	$C_{2,3}$	200 fF
L_1	120 pH	$R_{1,8}$	5 kΩ
$L_{2,7}$	25 pH	R_2	25 kΩ
L_3	60 pH	R_3	1.7 kΩ
L_4	40 pH	R_4	20 kΩ
L_5	100 pH	R_5	1.85 kΩ
L_6	15 pH	$R_{6,7}$	1 kΩ

Figure 5.1: Standard LNA schematic. [1] ©IEEE

currents, since the Q_{b1} and Q_1 transistors have different sizes. Similarly, the current mirror built with $R_{4,5,8}$ and Q_{b2} biases Q_3 transistor in the second stage.

This LNA consumes in total 23.5 mW of DC power from a 2.5 V supply.

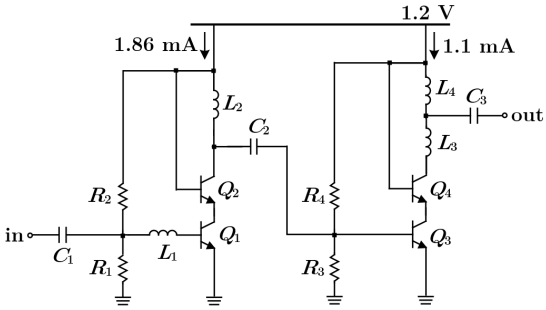
5.2.3 Low-Power Design Description

The second circuit is designed with an additional effort to minimize the power dissipation, while maintaining a comparable performance. The schematic is shown in Fig. 5.2.

The power dissipation reduction is achieved by following three main steps: 1) using smaller CE transistors; 2) reducing the supply voltage; and 3) using voltage dividers as a bias network.

The design procedure requires a trade-off between NF, P_{DC} and compression point. Fig. 5.3 presents the impact of the size of Q_1 and Q_3 stages on NF_{min} and OP_{1dB}. This analysis considers OP_{1dB} instead of IP_{1dB} to take gain into account. Green and red dots represent the baseline design discussed in the previous section and the low-power variant, respectively.

From step 1, as the CE transistors Q_1 and Q_3 define the current consumption, smaller emitter areas were selected for these devices. Q_1 is chosen to be twice as large as the smallest available option (2 emitter fingers) as a compromise



$Q_1{:}Q_2{:}Q_3{:}Q_4$=2x:7x:1x:4x
x=(0.07x0.9)µm^2

C_1	1 pF	$R_{1,3}$	10 kΩ
C_2	50 fF	R_2	3.5 kΩ
C_3	45 fF	R_4	3.4 kΩ
L_1	150 pH	L_3	55 pH
L_2	70 pH	L_4	40 pH

Figure 5.2: Low-power LNA schematic. [1] ©IEEE

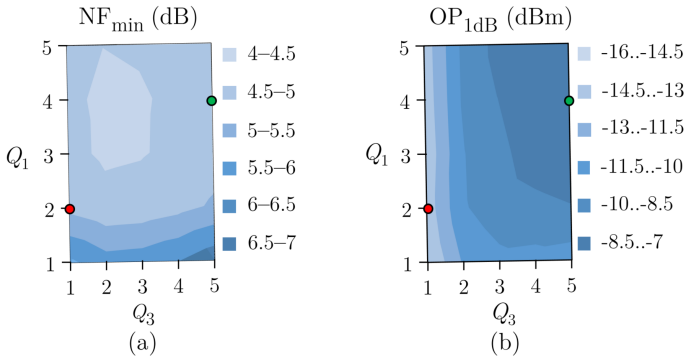


Figure 5.3: Impact of common-emitter transistors size on NF_{min} (a) and OP_{1dB} (b) at 100 GHz. Green and red dots are standard and low-power designs, respectively. [1] ©IEEE

between P_{DC} and NF. Fig. 5.3a shows an immediate increase in NF_{min} by 1−1.5 dB when using the one-finger option for Q_1, due to higher base resistance and, consequently, increased thermal noise. Increasing further Q_1 emitter area in comparison to the chosen option does not improve NF_{min}, unless larger Q_3 is used, as can be observed from the 4 – 4.5 dB zone shape. The deviation of the pattern in this area from the horizontal zones could be due to the noise contribution from the second stage.

Low power dissipation eventually negatively impacts linearity. Applying step 2, a reduced supply voltage limits the available voltage headroom, while lower collector current decreases the signal current swing and shifts the operating

point closer to the non-linear region of the transistor's transfer characteristics. Together, these factors reduce the maximum signal power level that a circuit can handle without distortion.

In the presented low-power LNA, the main contributor to the circuit's non-linearity is the output stage, as Q_3 compresses the signal previously amplified by the first stage. The almost vertical pattern of OP_{1dB} for small Q_3 in Fig. 5.3b supports this observation. Meanwhile, the power consumption of the second stage has a negligible impact on the NF compared to the first stage. This is evident from the horizontal behavior of different NF_{min} zones for small Q_1 (see Fig. 5.3a). For this circuit, maintaining a comparable NF with lower P_{DC} was prioritized, hence the P_{DC} of the second stage was significantly reduced by choosing the smallest Q_3. Overall, this study does not propose a single ideal solution but rather helps to visualize the trade-offs and make reasonable design decisions based on specific requirements.

The impact of decreased supply voltage Vcc on input impedance is explained in Fig. 5.4. For the chosen size of Q_1, Vcc reduction from 2.5 V to 1.2 V leads to S_{11} shift towards 50 Ω-circle. This corresponds to 4 fF increase in C_{in}, mainly due to the reduced V_{cb} and therefore larger C_{cb}. This effect makes the emitter degeneration unnecessary in contrast to the standard version. In addition, the Vcc reduction leads to a slight improvement in S_{opt} by decreasing its real part, probably because reduced collector current corresponds to smaller R_{opt}. The

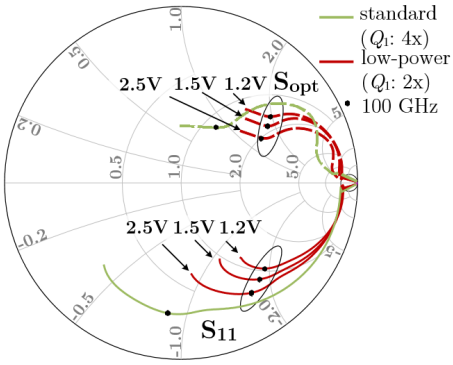


Figure 5.4: Impact of Vcc on input impedance. [1] ©IEEE

figure also explains more complicated simultaneous noise and input impedance matching, when the smaller Q_1 is used. This is due to the increased real part of S_{opt} (approximately 100 Ω) in the low-power variant compared to the standard design (red versus green). Vcc was not reduced below 1.2 V, as the maximum available gain (G_{max}) of a two-stage design would approach G_{max} of a single cascode stage with optimal P_{DC}. Using two stages in this case would no longer be practical, and comparing the baseline two-stage circuit with single-stage low-power variant would be inappropriate.

The size selection of Q_2 and Q_4 is partly based on simplifying impedance matching. Using a larger Q_2 increases its C_{cb} which contributes to the interstage matching and allows for smaller L_2 and C_2. The size of Q_4 helps to bring the high real part of S_{22} to the 50-Ω circle and makes the output matching easier.

Due to the chosen operating point and reduced emitter area of CE transistors, lower g_m and total gain are expected. To maximize the gain at the center frequency under such conditions, the design goal was to achieve the highest possible Q factor of the matching networks, while consciously sacrificing the bandwidth. Therefore, in contrast to the presented standard LNA, this circuit excludes resistors parallel to shunt inductors ($L_{2,4}$ in this case) in the inter-stage and output matching networks.

After incorporating the aforementioned power-saving considerations into the low-power design, the total P_{DC} was reduced to 3.8 mW from the 1.2 V supply. This corresponds to an approximately six times reduction compared to the previously presented standard design (23.5 mW).

5.2.4 Experimental Results

The chip photographs are shown in Fig. 5.5. The active circuit core of the standard and low-power LNA occupies 0.018 mm^2 and 0.014 mm^2 of the IC area, respectively. The compact layout is achieved by adjusting the shape and orientation of spiral inductors and by CB device sizing as previously described.

The small-signal characterization has been performed with the Agilent N5251A broadband system using an N5247B PNA-X in a 2-port configuration. Fig. 5.6a presents simulated and measured S-parameters of the standard LNA. The

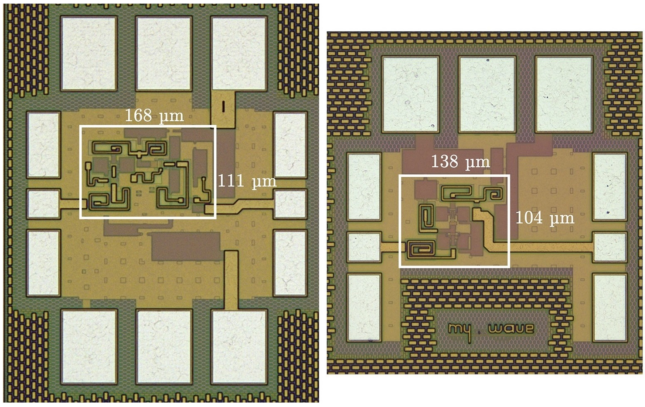


Figure 5.5: Chip photographs. [1] ©IEEE

measured gain at 100 GHz is 22.2 dB with a 3-dB bandwidth of 24 GHz (86−110 GHz).

Measured and simulated S-parameters for the low-power LNA are shown in Fig. 5.6b. The measured S_{21} curve shows a frequency shift relative to the simulation of less than 5% from the central frequency. According to [SPT+11], during modeling, transistors are often characterized for the forward-active regime, whereas in the low-power LNA, the transistors operate closer to saturation. This assumption, combined with the overall higher susceptibility of this design to process variations, can possibly explain the discrepancies between measured and simulated results. In addition, voltage dividers used as bias networks are generally less reliable compared to current mirrors used in the standard LNA. The measured 3-dB frequency range starts at 93.8 GHz and extends beyond 110 GHz, which exceeds the coverage of available frequency extension modules. Therefore, the 3-dB bandwidth of the low-power version can only be reported as greater than 16 GHz. A gain of 16 dB was measured at 100 GHz.

Fig. 5.6 also presents the simulated and measured NF for both circuits. The measurements were performed using the broadband setup (see Fig. 5.7) at MilliLab in the VTT Technical Research Center of Finland. The setup consists of a noise source and a noise receiver. The noise receiver includes a mixer,

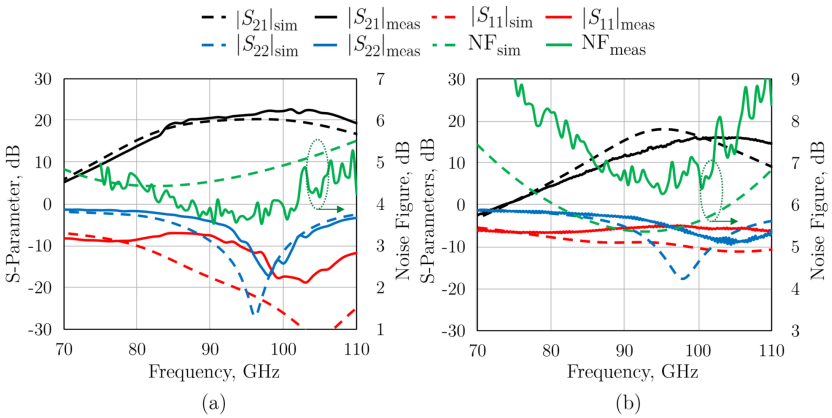


Figure 5.6: Measured and simulated S-parameter and NF for standard (a) and low-power (b) LNAs. [1] ©IEEE

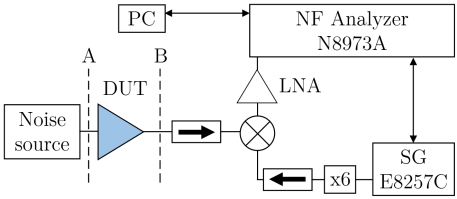


Figure 5.7: *W*-band NF measurement setup at MilliLab.

LO chain, and NF analyzer. The Y-factor method was used to derive the NF of the DUT. First, the noise receiver NF was determined by connecting the noise source, presenting two known power levels (hot and cold), to the calibration plane (B). The receiver NF and gain factor were calculated from the respective power measurements. Then, the device under test (DUT) was connected between the noise source and the noise receiver. The NF and gain factor of the cascaded DUT and noise receiver were determined as during the receiver calibration. The final calculations were made using Friis' formula. More details on the test setup are available in [VHLK+02]. Measured NF values at 100 GHz for the standard and low-power versions are 4 dB and 6.3 dB, respectively. The standard LNA exhibits flatter NF frequency response compared to the low-power variant. The deviations in the measured NF from

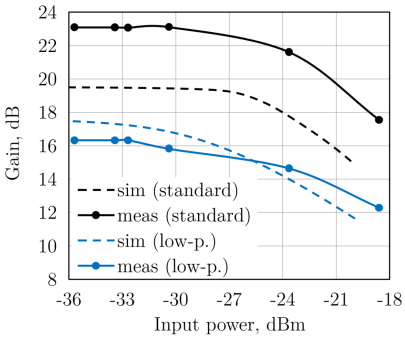


Figure 5.8: Measured large-signal performance at 100 GHz. [1] ©IEEE

the simulated values could be due to a shifted input impedance, as indicated by e.g. the deteriorated input matching of the low-power LNA compared to the simulation.

The large-signal performance was characterized using the same setup as for the small-signal measurements, but with the PNA in spectrum analyzer mode. The input power was controlled by an attenuator of the frequency extension module. Simulated and measured results at 100 GHz for the two circuits are presented in Fig. 5.8. The standard and low-power LNAs exhibit the measured $IP_{1\mathrm{dB}}$ of −24.5 dBm and −26.5 dBm, respectively. Curve imperfections may be caused by the manual control of the attenuator, which inherently introduces some measurement inaccuracy.

The performance of the presented LNAs, along with other examples from the literature, is summarized in Table 5.1. The presented study demonstrates that after a reduction of 84% in P_{DC}, the LNA experienced a 45% loss in the Figure of Merit (FoM) compared to the baseline circuit.

Table 5.1: LNA Performance Summary

	Tech.	P_{DC}, mW	S_{21}, dB	Freq, GHz	BW, GHz	NF, dB	IP_{1dB}, dBm	Area, mm^2	FoM
[GWR20]	22-nm CMOS	16	18.2	92	31	5.8	–22.8	0.435	5.7
[ZWT+22]	40-nm CMOS	23.4	18.5	84	16.1	5.7	–19	0.174	10.2
[USK+15]	130-nm SiGe	12	27.5	125	35’	5.5	–33	0.39	6.6
[YK19]	90-nm CMOS	6.8	21.5	90	5+	8.3	–30	0.1	3
Standard	130-nm	23.5	22.2	100	24	4	–24.5	0.018	10
Low-power	SiGe	3.8	16	100	>16	6.3	–26.5	0.014	5.5

’BW with gain >20 dB; 3dB-BW estimated from the plot is 15 GHz
FoM = $1000 \cdot \frac{G \cdot IP_{1dB}[mW]}{(F-1) \cdot P_{DC}[mW]}$, $G = S_{21}$ (linear), $F-$noise factor (linear)
+estimated from the plot

5.3 Down-Conversion Mixer with Image Rejection

Parts of this section include material previously published in [5].

This section will focus on the design considerations for a down-conversion mixer, another crucial component in a *W*-band receiver.

5.3.1 Performance Metrics

The focus will be on the following performance indicators for the down-conversion mixer:

- **Conversion gain** (CG) of a down-converting mixer quantifies the efficiency of translating the input RF signal to the output IF signal, i.e.

CG = P_{IF}(dBm) − P_{RF}(dBm). Higher conversion gain can enhance the system's signal-to-noise ratio and eliminate the need for additional amplification stages in the IF path.

- **LO power** (P_{LO}) required to maximize the mixer's CG influences design decisions for the LO chain components. High output power demands from a voltage-controlled oscillator result in increased power dissipation and can pose other challenges, particularly at higher frequencies. For instance, a performance trade-off may arise between P_{out} and frequency tuning range, or between P_{out} and linearity.
- **Image rejection ratio** (IRR) describes the ability of a receiver to suppress the image signal, i.e. IRR = $P_{desired}$(dBm) − P_{image}(dBm) at the IF. As shown in Fig. 5.9, the image frequency is symmetrically offset from the LO frequency and is down-converted to $f_{IM} - f_{LO} = -f_{IF}$, which mathematically is identical to f_{IF}. An RF signal at the image frequency, i.e., the image signal, after down-conversion, is indistinguishable from the desired signal.

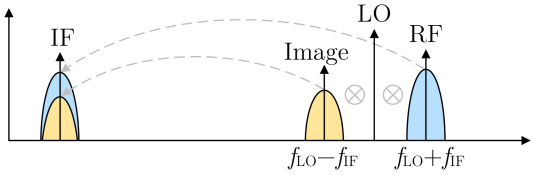


Figure 5.9: Image signal problem.

- **Linearity** of the mixer, in this section, is discussed in terms of the compression behavior and is expressed by IP_{1dB}. The target IP_{1dB} of higher than −11.5 dBm was derived from the measured OP_{1dB} of the previously presented low-power LNA.
- **Power dissipation** (P_{DC})

5.3.2 Image Rejection Approaches

Figure 5.10 presents several well-known topologies designed to suppress the image signal. The Hartley image reject architecture operates by introducing a quadrature phase shift between two mixing branches and then combining the down-converted signals. In this configuration, the desired signal components are combined in-phase, while the image frequency components, being 180° out-of-phase, are effectively canceled out. The phase shift can be introduced in either the LO path or the RF path, as shown in Fig. 5.10a,b, respectively.

Overall, this approach based on the quadrature phase shift is frequently used today because it can theoretically provide infinite IRR in an ideal case. However, in practice, the phase and amplitude imbalances introduced by the 90° splitter decrease the IRR, which is expressed by the formula [Raz11]:

$$\mathrm{IRR} = 10\log\left(\frac{(1+a)^2 + 2(1+a)\cos\Delta\theta + 1}{(1+a)^2 - 2(1+a)\cos\Delta\theta + 1}\right), \tag{5.1}$$

where a is the relative gain error and $\Delta\theta$ is the phase error in radians. The main disadvantages include doubled power and area consumption compared

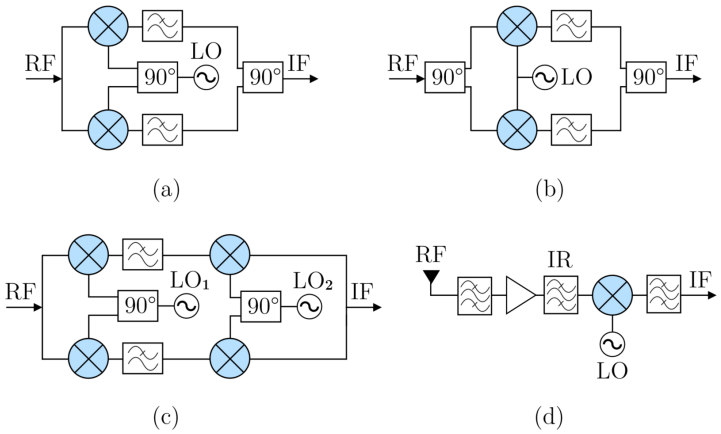


Figure 5.10: Examples of image-reject topologies: Hartley architecture with phase shift in LO- (a) and RF-path (b); Weaver architecture (c); filter-based architecture (d).

to a filter-based architecture, and in the case of the Hartley topology, the use of a bulky 90° splitter at the IF.

A popular variation of the Hartley topology is the quadrature mixer (or I/Q mixer) [LKK+18, HK20, KWBP21]. It operates on the same principle, but instead of combining the IF outputs, the I and Q branches are kept separate until they reach the digital processing stage. This separation allows for advanced digital signal processing, providing additional flexibility.

The Weaver architecture, shown in Fig. 5.10c, reduces sensitivity to quadrature mismatches compared to the Hartley topology. This approach uses an additional mixing stage and does not require a broadband phase shift at IF to achieve high IRR. However, the use of four mixers and two quadrature LO sources significantly increases power dissipation and overall complexity, and can negatively affect the NF. More complex variations of the Weaver topology, incorporating a double-quadrature second down-converting stage, can be found in the literature (e.g., [WMLH17]).

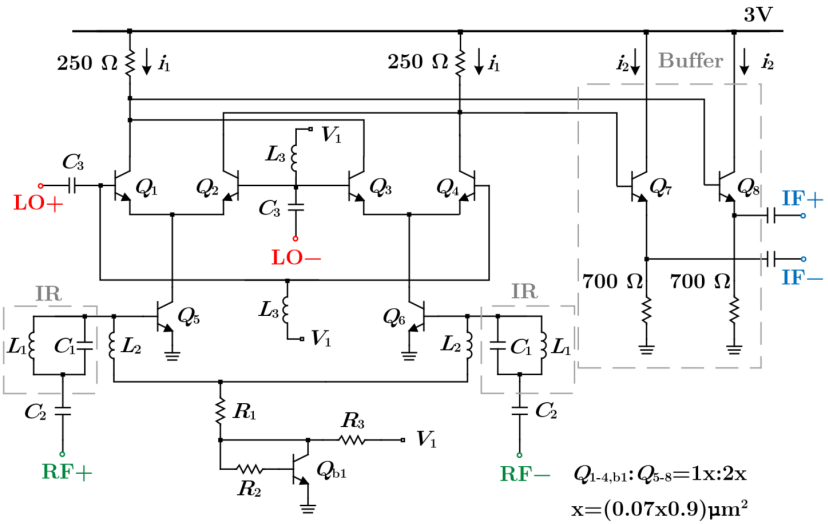
The use of image rejection filters (see Fig. 5.10d) offers a straightforward and power-efficient alternative to the previously discussed topologies. However, this approach is limited to high-IF systems, as effective image filtering without distorting the desired signal is possible only when the RF and image frequencies are sufficiently spaced apart. The specific frequency separation depends on the required IRR and the filter implementation.

Nevertheless, in all configurations the mixer is a key component. This section presents a compact, low-power 100-to-20 GHz down-conversion Gilbert-cell mixer with an integrated band-stop filter for image suppression at 60 GHz for an LO at 80 GHz.

5.3.3 Circuit Description

The schematic of the down-converting mixer is shown in Fig. 5.11. According to the design goals, f_{RF} = 100 GHz, f_{LO} = 80 GHz, and hence f_{IF} = 20 GHz.

Some of the considerations for the P_{DC} reduction discussed in Section 5.2.3 were applied to this design. The primary strategy involves reducing current consumption by using smaller $Q_{5,6}$ transistors in the g_m-stage. The goal for



L_1, pH	L_2, pH	L_3, pH	C_1, fF	C_2, fF	C_3, fF	R_1, kΩ	R_2, kΩ	R_3, kΩ	i_1, mA	i_2, mA	V_1, V
70	60	105	100	60	25	1	2	2.46	1.13	2.57	2.075

Figure 5.11: Mixer schematic. [5] ©IEEE

the presented circuit is to maintain a compromise between P_{DC}, $IP_{1\mathrm{dB}}$, and the occupied area. Therefore, $Q_{5,6}$ transistors with two emitter fingers were chosen, as using the smallest available size (one finger) would further degrade the mixer's linearity.

In contrast to the LNA design, the supply voltage was not reduced to allow the use of resistive load instead of inductive load. This approach balances P_{DC} and area consumption. A physically larger but more power-efficient alternative would include a lower Vcc and the use of inductors, which at the IF output would significantly increase the occupied area. The chosen resistor value of 250 Ω provides sufficient gain and necessary voltage at the collector node of the switching stage devices.

The current mirror formed by R_{1-3} and Q_{b1} is used as the bias network for the CE transistors $Q_{5,6}$, as discussed in Section 5.2.2.

Transistors Q_{1-4} use the smallest available emitter area. Due to the low DC currents provided by $Q_{5,6}$ and the relatively high impedance of Q_{1-4}, the required LO signal power was reduced as part of the design optimization process. A low P_{LO} of -10 dBm is sufficient to ensure full switching of the quad devices, thereby maximizing the conversion gain. As discussed above, this presents the advantage of partially relaxed requirements for LO distribution, which is especially beneficial in multi-channel integration.

The image-rejection functionality is achieved through a band-stop filter composed of L_1 and C_1. These components form a parallel resonator tuned to a center frequency of 60 GHz, which corresponds to the expected image frequency. The resonator, placed at the RF input, forms an L-type matching network at 100 GHz in combination with C_2 and L_2.

Fig. 5.12 presents the preliminary schematic simulation of the CG frequency response with and without the IR filter. At the start of the design, achieving high CG at 100 GHz was prioritized. This simulation includes only ideal components, i.e., layout effects are not considered at this stage. Although the comparison shows a clear IRR improvement of 14.2 dB, the total IRR of 22.5 dB remains significantly lower than that exhibited by most state-of-the-art I/Q mixers. Additionally, during the layout design phase, when transitioning to more realistic component modeling, the challenge of achieving both high CG at 100 GHz and high IRR became more pronounced. In the final design, a higher IRR was eventually prioritized, under the condition that the mixer did

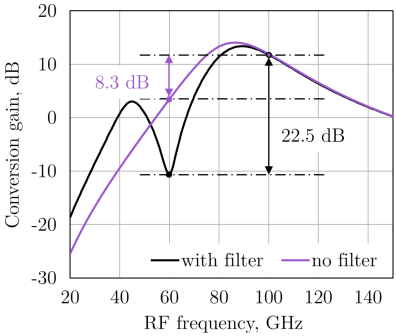


Figure 5.12: Preliminary ideal schematic simulation with a focus on high conversion gain. Two curves represent simulations with and without image-rejection filter.

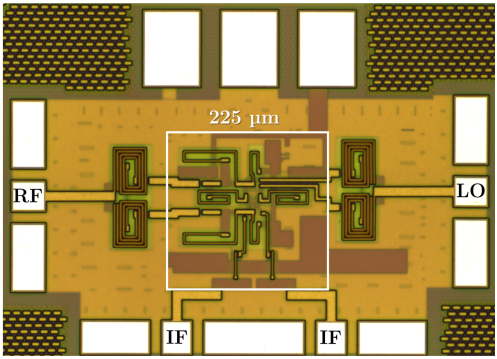


Figure 5.13: Chip photograph. [5] ©IEEE

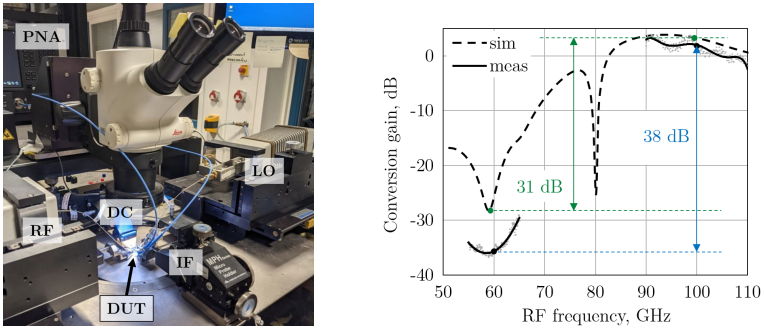
not exhibit conversion loss. The final full-EM simulation of the mixer design, focusing on IRR, showed approximately 31 dB of peak IRR, as will be further presented along with the measured data.

The Gilbert cell is followed by a common-collector (CC) buffer ($Q_{7,8}$) to match the low output impedance to the 50-Ω measurement environment. For $Q_{7,8}$, the smallest device size that ensures appropriate output matching ($|S_{22}| \leq -10\,\text{dB}$) and linearity was chosen. The impedance matching for the LO port at 80 GHz is done similarly to the RF port, using a shunt inductor L_3 and a series capacitor C_3.

The designed Gilbert cell consumes 8 mW of power from a 3 V supply voltage and the active circuit core occupies 0.048 mm^2. The chip photograph is shown in Fig. 5.13. Two Marchand baluns at RF and LO inputs are included for the measurement purposes. The total power consumption of the circuit including the CC buffer is 23 mW from the 3 V supply. The simulated single-sideband noise figure is 15 dB in the center of the band.

5.3.4 Experimental Results

Conversion gain measurement was performed using a 3-port scalar mixer/converter (SMC) mode of the PNA-X, instead of the spectrum analyzer mode. The test setup is shown in Fig. 5.14a. The RF signal was provided by



(a) (b)

Figure 5.14: Test setup (a) and measured conversion gain (b). [5] ©IEEE

port 1 of the PNA, followed by the *W*-band frequency extension module. The differential IF output was connected to the PNA's ports 3 and 4. An external signal generator was used as the source for the LO signal. The CG was tested by sweeping f_{RF}, while keeping $f_{LO} = 80$ GHz fixed with $P_{LO} = -10$ dBm. The results are presented in Fig. 5.14b. The solid lines are fitting curves for the measured points, caused by calibration imperfections. Due to equipment limitations and complex calibration, the characterization was performed for the limited RF frequency ranges of 90–110 GHz and 55–65 GHz to confirm the image rejection functionality. The measured IRR at 100 GHz is 38 dB and remains better than 35 dB for the RF range of 90–105 GHz. The 7-dB difference in IRR_{max} is presumably due partially to measurement (calibration) inaccuracies but primarily to an imprecise EM modeling of the RF matching network and the IR filter. Additionally, the piecewise simulation of the mixer and baluns could contribute to this accumulated error. Apart from the absolute value, the change in the CG shape at 60 GHz likely indicates an underestimated parasitic resistance of the resonator components in the EM simulation.

Fig. 5.15a presents a CG dependence on the RF power at $f_{RF} = 100$ GHz, $f_{LO} = 80$ GHz, and $P_{LO} = -10$ dBm. The input power was swept by the manual attenuator of the frequency extension module. The simulated and measured IP_{1dB} are −11.5 dBm and −12.3 dBm, respectively.

Fig. 5.15b shows the simulated and measured CG versus LO power at $f_{RF} = 100$ GHz, $f_{LO} = 80$ GHz, and $P_{RF} = -30$ dBm. The LO signal with

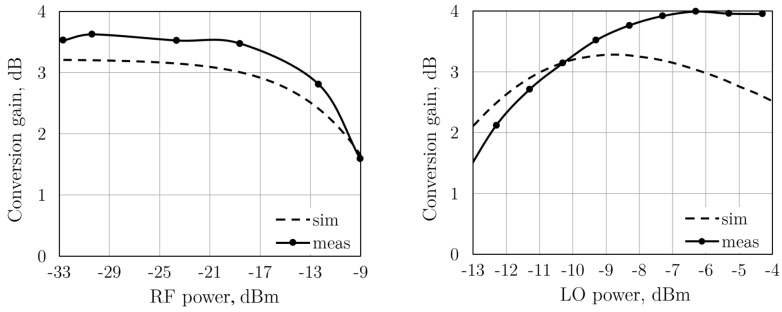


Figure 5.15: Measured conversion gain versus RF power (a) ($P_{LO} = -10$ dBm) and LO power (b) ($P_{RF} = -30$ dBm). [5] ©IEEE

$P_{LO} = -10$ dBm was originally chosen according to simulated data, as further power increases did not result in significant CG improvement. However, the measured curve demonstrated slightly different behavior, with CG_{max} shifted to approximately 2.5 dBm higher P_{LO}.

The measured performance of the mixer is summarized in Table 5.2.

5.4 Conclusion

This chapter investigates the impact of power dissipation, beginning with system-level constraints and then focusing on specific building blocks.

Two 100-GHz low-noise amplifiers have been developed, characterized, and compared for the quantitative analysis of performance compromises associated with reduced P_{DC}. In the LNA design, these compromises include mainly NF, linearity and partially input impedance matching. Both circuits are based on the same topology and are fabricated in the same IC technology to keep the comparison consistent. The low-power version employs rather conventional methods to achieve lower P_{DC}. However, this study identifies specific points in the circuit where power reduction critically affects different performance metrics such as NF, gain, and linearity.

Table 5.2: Mixer Performance Summary

	Tech.	f_{RF}, GHz	f_{IF}	CG, dB	P_{LO}, dBm	IP_{1dB}, dBm	IRR, dB; Type	P_{DC}, mW	Area, mm^2
[LYT+13]	65-nm CMOS	65	1.25 MHz	0±1	2	n/a	>40 (I/Q)	40.8	0.861’
[CKKJ20]	100-nm GaAs pHEMT	93	50 MHz	–8.7	10	n/a	19.2–47.9 (I/Q)	–	2.72’
[MPK+21]	130-nm SiGe	135	5 GHz	32	0	–41	no IR	65	0.2
[LW19]	90-nm CMOS	94	0.1 GHz	14.6	1	–8.7	no IR	5	0.358
[AHMW21]	22-nm FD-SOI CMOS	70	3.8 GHz	12–15	n/a	–5.6.. –8	17–32 (I/Q)	36	1.68+
[TSJE21]	22-nm FDSOI	60	1 MHz	21	–3	–16.2	no IR	5.25	0.065
Section 5.3.3	130-nm SiGe	100	20 GHz	3.7	–10	–12.3	38 (filter)	23	0.048

’including pads + complete receiver

The *W*-band down-conversion mixer is introduced to analyze the impact of topology choice on achieving compact and power-efficient design. The feasibility of the presented filter-based image-rejection mixer is discussed as a simpler alternative to I/Q mixers. Additionally, the trade-offs between P_{DC}, linearity, and occupied area are explored.

The presented ideas and considerations offer practical insights into reducing total power dissipation when specifications are more relaxed. For example, achieving moderate IRR may be adequately addressed with a simple additional IR filter, which is more practical than employing two mixers, a quadrature

LO source, and an IF coupler. Similarly, if meeting linearity criteria, reducing P_{DC} in the second LNA stage can be achieved without significantly compromising noise performance. Conversely, in systems with stricter requirements, sometimes none of the discussed approaches may be applicable.

6 Conclusions and Outlook

This thesis explores RF front-end building blocks for analog beamforming networks in future beyond-5G terrestrial and satellite communication systems. Phase shifters, as a key component of phased arrays for analog beamforming, are the core of this research. Iteratively developed mm-wave phase shifters helped to identify and systematize the miniaturization approaches and their limitations. The results reveal that miniaturization in phase shifters can be achieved at various hierarchical design levels. The lowest is the miniaturization of passive components of the circuit, particularly of the passive I/Q splitters. Geometry optimization in the vertical direction rather than in the traditional horizontal way leads to significant area reduction. The 3D implementation of the Lange coupler exhibits negligibly small performance degradation with a 50% area reduction. To further reduce the occupied area, another type of I/Q splitter was chosen as a baseline, namely a coupled-line coupler. This 3D spiral coupler implementation achieves approximately 75% area reduction but suffers from more pronounced degradation in gain and phase errors that also deteriorate more within the same frequency range. Due to the narrow-band nature of phase-shifter-based phased arrays, the achieved performance can still be acceptable for some systems. These results demonstrate a fundamental trade-off between the area and performance of passive components.

The next miniaturization level can be reached by re-evaluating the topology choices of the circuit. The active vector-sum topology proved to be a suitable choice for compact phase shifters providing large phase resolution. The presented W-band Blixer-based implementation advances the miniaturization aspect by using the g_{m}-stage of the Gilbert cell as an active balun and a transformer-based output matching network that also serves as a balun on the output side. These ideas, combined with a compact quadrature coupler implementation, represent a combination of two miniaturization levels and result in a 50% area reduction compared to the conventional Gilbert cell with an LC-based matching network.

The highest level of miniaturization requires considering the circuit's role within a complete system. As a first step, considering the phase-shifting functionality required in receive and transmit modes, a hybrid solution, namely a bidirectional active phase shifter, was proposed. This building block is a promising compromise combining the bidirectional operation of passive phase shifters with the compact footprint of active topologies. The main principle is based on reusing passive components of the phase shifter in two signal directions, resulting in an additional 20% area reduction compared to two separate Blixer-based designs. As a second step, an extension of the presented miniaturization approaches to multiple building blocks was investigated for a satellite communication system. The research results show that one of the keys to a compact system is the functions distribution and integration of several functions into one component. In this thesis, this integration includes the Blixer-based phase shifter, simultaneously used as a VGA, and a VGA with a gain equalization function. The simulation results also reveal a downside to this approach, namely the degradation of some of the functions that must be taken into account. For instance, the integrated equalizer offers more flexible gain control over frequency, but the maximum gain is reduced compared to a traditional VGA, and the slope is not as "sharp" as it could potentially be with a separate equalizer. As a result, the presented research demonstrates that despite the limitations of each miniaturization level, their combination promises significant area reduction for the complete system.

Power dissipation reduction, as a separate crucial aspect, was investigated based on other building blocks, such as the LNA and down-conversion mixer. The comparison of performance-optimized and power-optimized LNA designs shows and quantifies the negative effect of reduced power consumption on the noise figure (mainly from the first stage), gain, linearity (mainly from the second stage), and bandwidth. The proposed mixer design with an integrated image-rejection filter can be a compact and low-power alternative to conventional I/Q mixers, depending on the required image-rejection ratio and beamforming scheme.

Future work can potentially include several aspects:

- Characterization of the remaining designs, including a complete channel RFIC from Chapter 4, as a first step.
- Radiation tests at Tesat-Spacecom are planned as part of the research project. These experiments will be valuable for observing the behavior of IHP's new SG13G3Cu technology and identifying potential weak spots in the designed circuits in terms of radiation hardness.
- The reliability aspect can be explored using Monte Carlo simulations to assess the sensitivity of the designs to process variations, including evaluations over a broader temperature range.
- While simple temporary bias networks for phase control of the phase shifters were sufficient for research purposes and straightforward characterization, they will need to be replaced with a proper DAC alternative for a more realistic design in the future.
- Several concepts, such as miniaturization at different design levels and P_{DC} optimization, can be combined. For example, a single chain could be developed using the integration of multiple functions within the same component, as in the channel RFIC, potentially incorporating the bidirectional phase shifter with a separate linearity optimization. This approach could be expanded to a complete phased array, which would serve as a fitting conclusion to this work.

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Own Publications

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Other Contributions

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