A Compact 238–278-GHz Frequency Sextupler Based on a Single Bootstrapped Gilbert Cell

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***Abstract*— We present an integrated frequency multiplier-by-six (sextupler) for signal generation at *J*-band (220–325 GHz) frequencies. Typically, multiplication-by-six in state-of-the-art designs is achieved by cascading frequency tripler and doubler circuits. In contrast, we propose to accomplish the multiplication-by-six in a single bootstrapped Gilbert cell (BGC) by leveraging odd-harmonic generation in the transconductance stage and self-mixing in the switching quad. A circuit analysis of the harmonic generation and mixing mechanisms is presented and verified through simulations. The sextupler is combined with a balance-compensated transformer (TF) balun at the input and a cascode amplification stage to increase the output power. As proof-of-concept, a prototype is fabricated in an advanced 130-nm SiGe BiCMOS technology with a core area of only 0.06 mm^2. The circuit demonstrates a measured peak conversion gain (CG) of 7 dB and output power of up to 4.3 dBm at 257 GHz with a dc power consumption of 119 mW, resulting in a leading-edge dc-to-RF efficiency of 2.2%. All undesired harmonics are suppressed by more than 20 dBc over the entire 3-dB bandwidth, ranging from 238–278 GHz. Compared to recently published silicon-based frequency sextuplers operating at similar frequencies, our proposed single-stage approach results in a significant reduction of dc power and silicon area, while maintaining a superior dc-to-RF efficiency and competitive output power.**

***Index Terms*— Efficiency, frequency multiplier, harmonic suppression, *J*-band, millimeter-wave (mm-wave), multichannel, self-mixing, SiGe BICMOS, signal generation.**

I. Introduction

SILICON technologies offer low cost, high-level integration, and have become the dominant choice to exploit the large bandwidth and small wavelength available at millimeter-wave (mm-wave) frequencies. Recent technological advances have pushed the transit frequency (f_T) and maximum oscillation frequency (f_{MAX}) of silicon-based transistors beyond 500 and 700 GHz, respectively [1], driving research toward higher frequency bands such as *J*-band (220–325 GHz). Single-channel *J*-band transceivers have already been demonstrated for various radar applications using silicon [2], [3], [4]. Current research focuses on multichannel systems, such as phased array [5] and multiple-input-multiple-output (MIMO) architectures [6], which offer improved angular resolution, beamforming, and spatial diversity. A multichannel architecture is also advantageous for high-power signal generation, where combining transmit (TX) channels increases effective isotropic radiated power (EIRP) [7]. In the project underlying this work, the goal is to develop a transmitter operating at 260 GHz, employing at least 2 × 2 parallel TX channels for use in a nuclear magnetic resonance experiment.

A major challenge in *J*-band systems is to provide a signal source with low phase noise and a wide tuning range. Fundamental operation of voltage-controlled oscillators (VCOs) or phase-locked loops (PLLs) at *J*-band is difficult due to low quality factors, increasing impact of parasitics [8], and limited operating speed of silicon-based dividers [9]. As a result, VCOs or PLLs are often operated at lower frequencies, with frequency multipliers used to generate the *J*-band signal [2], [3], [4], [5], [6], [7]. The planned transmitter foresees a multiplication factor (MF) of six, leading to an operating frequency of the signal source below 50 GHz, allowing either on-chip realization or the use of a laboratory signal generator.

Another obstacle in multichannel chips is that they usually feature a central local oscillator (LO) distribution network. LO distribution after the multiplier and operating directly at *J*-band is not feasible due to multiple reasons. First, transmission line lengths become comparable to the wavelength, thus exhibiting excessive loss and sensitivity to impedance transformation. Second, additional amplification to compensate for the passive loss is inefficient at *J*-band due to limited device gain at these frequencies. Therefore, the preferred approach is to distribute signals at lower frequencies and use a frequency multiplier in each channel [3], [4], [5], [6], [7]. However, this increases the importance of a compact form factor and high efficiency of the multiplier to minimize footprint, power consumption, and heat generation in solid-state implementations.

We introduce a *J*-band frequency multiplier-by-six (sextupler) aiming to address the stringent requirements in multichannel systems. In Section II, we present a comprehensive state-of-the-art review of mm-wave multipliers, highlighting that frequency sextuplers mainly rely on the robust but area- and power-inefficient approach of cascading triplers and doublers. In this work, we propose to replace the cascaded approach by a single-stage solution to perform the

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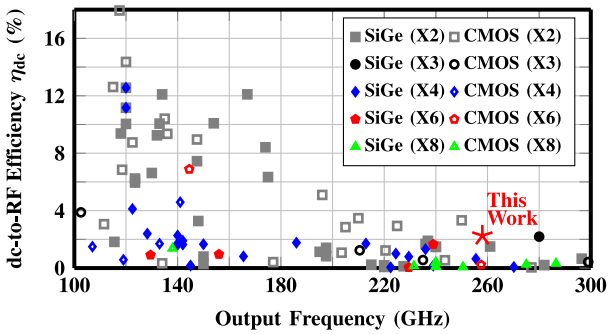

Fig. 1. State-of-the-art summary of silicon-based millimeter-wave frequency multipliers above 100 GHz.

multiplication-by-six on a significantly smaller form factor and with a superior efficiency than prior art. A detailed circuit analysis of our proposed single-stage sextupler follows in Section III, and the experimental results of our fabricated prototype are discussed in Section IV of this work.

II. Review: Millimeter-Wave Multipliers

In general, frequency multipliers generate higher order harmonics $n \cdot f_0$ ($n = 2, 3, \ldots$) of input frequency f_0 by leveraging device nonlinearity or waveform clipping, with a filter or injection-locked oscillator selecting the target harmonic. Injection-locked multipliers require only low power of the injected signal near the oscillator's self-oscillation frequency, but they usually suffer from a narrow locking range [10], [11], [12] and are not considered in this work, which focuses on non-injection-locked approaches. Key performance metrics of mm-wave multipliers are output power, conversion gain (CG), harmonic rejection ratio (HRR), and dc-to-RF efficiency

$$\eta_{dc} = P_{out}/P_{dc} \tag{1}$$

where P_{out} is the output power at the desired harmonic and P_{dc} the applied dc power. Fig. 1 summarizes state-of-the-art silicon-based multipliers above 100 GHz, showing a clear trend of decreasing η_{dc} with rising frequency. We next review common circuit topologies and recent strategies for miniaturization and efficiency enhancement.

A. Frequency Doublers and Triplers

There are two main categories of doublers. The first is push-push (PP) doublers, including a pair of transistors combining even-order harmonics, while odd-order harmonics ideally cancel each other out. PP doublers are widely used at mm-wave frequencies [13], [14], [15], [16], [17], [18], [19], [20], [21], but provide only single-ended output. The second group leverages the Gilbert cell (GC) as a four-quadrant multiplier to generate the second harmonic by self-mixing of the input frequency. In [22], a modified version, the so-called bootstrapped Gilbert cell (BGC), has been proposed. Unlike the standard GC, where the input signal directly drives the switching quad, the BGC's quad is fed from the transconductance (g_m) stage's output. This bootstrapping technique enhances input impedance, CG, and output signal balance [22], [23].

Frequency triplers are commonly implemented as overdriven differential amplifiers [24], [25], [26], or they leverage the enhanced second-order nonlinearity by using a doubler followed by a mixer [27], [28] to produce a $3f_0$ output signal by mixing the input signal with the output signal of the doubler.

B. Higher Order Multipliers

Higher MFs > 3 are usually achieved by cascading doublers (X2) and triplers (X3). Fig. 2 shows popular cascaded approaches for quadruplers (X4) and sextuplers (X6) in the left column. The X4 in [29] employs two cascaded PP doublers with interstage balun and bandpass filter for enhanced HRR, but needs an amplifier to compensate for interstage loss. In [30], the interstage balun is eliminated by using BGC-based doublers with differential output. The f_0 input signal is applied to the g_m stage, and its output current feeds the quad stage generating the second harmonic through self-mixing. However, each BGC requires long transmission lines to shift the phase (φ) between RF and LO inputs to optimize CG and suppress dc self-mixing components [23]. Similar limitations are seen in prior-art sextuplers. The X6 in [31] combines a tripler with multiple amplifiers to feed a final doubler stage, using two-way power combining to counter the single-ended PP output, though at the expense of increased power and silicon area. Comparable architectures are used in [32], [33], [34], [35], [36], [37], and [38]. Higher factors (MF = 8 [39], [40], [41], MF = 9 [42], [43], [44], and beyond [27], [45], [46], [47], [48], [49]) are achieved using similar cascaded methods but typically at the cost of power and area efficiency, limiting their use in multichannel systems.

To address this issue, several studies have proposed higher order multiplication in a single stage, as shown in the right column of Fig. 2. Wang et al. [50] suggest replacing the PP doubler cascade with a phase-controlled PP cascode to extract the fourth harmonic, reducing form factor and improving η_{dc} but retaining single-ended output. In [51], X4 multiplication is demonstrated in a single GC by using the g_m stage as third harmonic generator (3HG), which mix with the f_0 input signal in the quad (see concept in Fig. 2). While the available single-stage studies are mostly limited to MF = 4, only few examples are available for higher MF. In [52], waveform clipping in a cascode amplifier is proposed to achieve X4, X6, or X8 multiplication, but output power and efficiency remain low at 180 GHz ($P_{out} = -6$ dBm, $\eta_{dc} = 0.32\%$).

In summary, prior art mainly relies on robust but inefficient cascaded approaches for higher order multipliers, while no promising single-stage solutions are yet available for the target MF = 6. This work proposes to combine the advantages of the bootstrapping technique with the self-mixing concept to demonstrate a highly compact and power-efficient X6 multiplication in a single BGC. As illustrated in Fig. 2 (bottom right), the g_m stage is used as 3HG stage, and the bootstrapped topology enables efficient self-mixing of the third harmonic in the quad, producing the sixth harmonic without extra cascaded multiplication stages. Compared to a PP doubler, which typically requires an additional driver stage at these

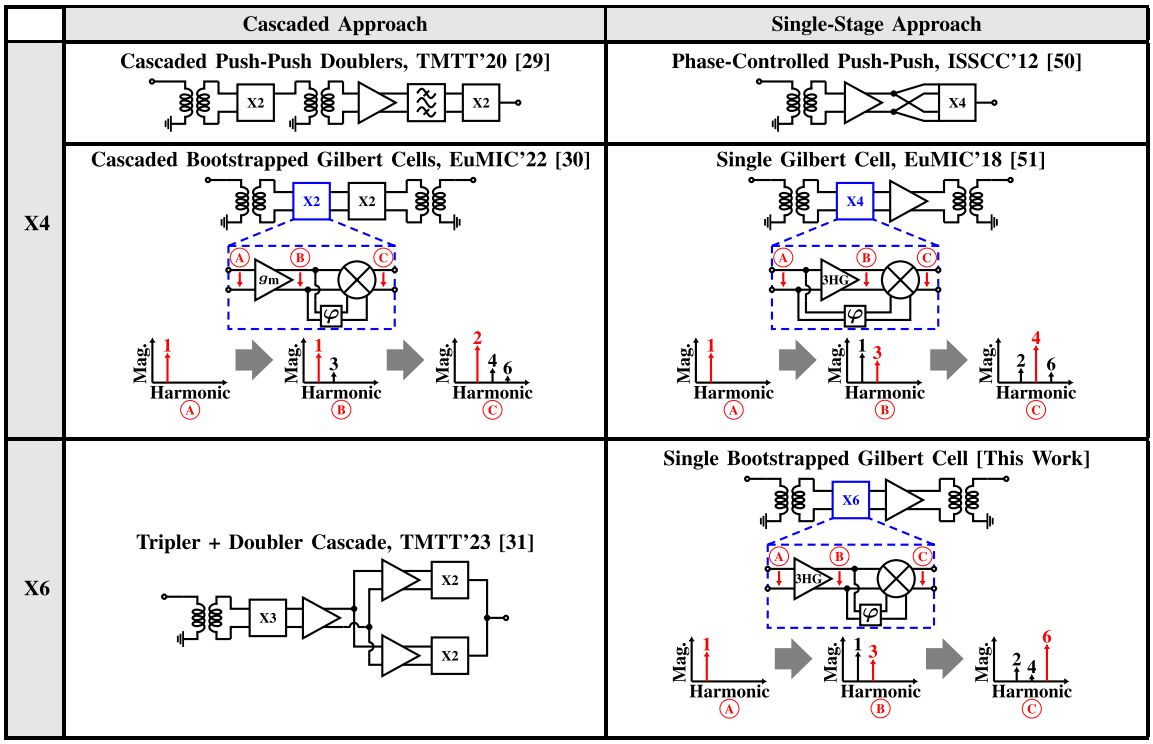

Fig. 2. Evolution from conventional cascaded to single-stage approach for prior-art frequency quadruplers and proposed frequency sextupler.

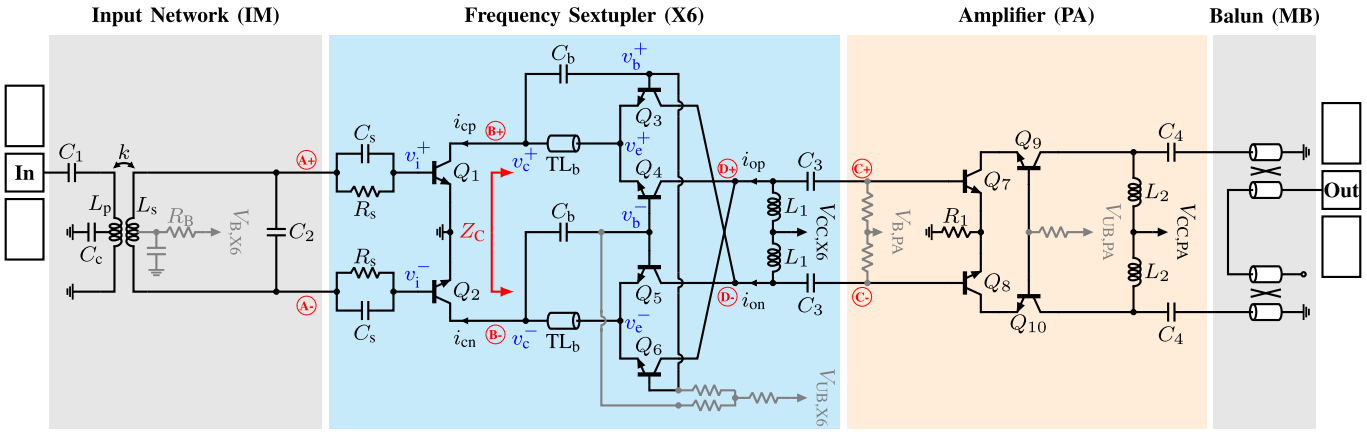

Fig. 3. Circuit schematic of the frequency sextupler.

frequencies [17], [18], [19], [20], [21], the BGC quad benefits from enhanced CG and can be driven directly by the output current of the 3HG stage. To our knowledge, this is the first use of a single bootstrapped GC for higher order multiplication. Our design achieves a measured output power of 4.3 dBm at 257 GHz with the smallest core area of 0.06 mm^2 and highest reported dc-to-RF efficiency of 2.2% for silicon-based sextuplers at J-Band frequencies up to date.

III. Circuit Design

The prototype circuit is designed in IHP's advanced 130-nm SiGe BiCMOS technology SG13G3. This technology features heterojunction bipolar transistors (HBTs) with f_T/f_{MAX} = 470/650 GHz, which are scalable in discrete values via the finger count N_x, each having a size of 70 × 900 nm. The collector–emitter (BV_{CEO}) and collector–base (BV_{CBO}) breakdown voltages are specified with BV_{CEO} = 1.5 V and BV_{CBO} = 3.8 V, respectively. The process offers an eight-layer metal stack from X-FAB including four thin (M1–M4) and two 3.2 μm-thick (ThCu1, ThCu2) copper layers, as well as one thin (ThinAl) and one 2.8 μm-thick (ThickAl) aluminum top layer. Metal–insulator–metal (MIM) capacitors with 2 fF/μm^2 are available between both aluminum layers. Further, salicided and unsalicided polysilicon resistors as well as MOS varactors can be used. The complete circuit diagram of our proposed frequency sextupler is given in Fig. 3. The circuit is divided into four main parts (IM, X6, PA, MB), which are analyzed in detail in the sections below.

A. Single-Stage Bootstrapped Frequency Sextupler

The following circuit analysis of our proposed frequency sextupler concept refers to Fig. 3. The sextupler topology is

a BGC. Transistors Q_{1-2} form a transconductance (g_m) stage and their collector currents (i_{cp}, i_{cn}) become emitter currents of the quad devices Q_{3-6}. The R_s-C_s high-pass network at the input is added to reduce gain at low frequencies, while a cut-off frequency well below the desired input frequency range avoids undesired performance degradation. To explain the working principle of the proposed sextupler, we begin to analyze the g_m stage separately first.

In prior-art BGC-based doublers, the main purpose of the g_m stage is to present a relatively high input impedance and to convert the differential input voltage ($v_i = v_i^+ - v_i^-$) at frequency f_0 into a collector current ($i_c = i_{cp} - i_{cn}$) of the same frequency. Since higher harmonic generation is undesired, a small-signal analysis is often carried out [23]. However, unlike prior art, we wish to use the g_m stage as 3HG (from now on referred to as the 3HG stage) and leverage a strong third-harmonic component at nodes Ⓑ for self-mixing in the switching quad. We therefore have to rely on a nonlinear analysis to assess the 3HG stage operation. In general, higher order harmonics are generated by the inherently exponential I–V characteristics of the HBTs or by waveform clipping. To analyze the nonlinearities caused by the device I–V characteristics, let us assume a monotone input signal

$$v_i^+ = V_i \cdot \cos(\omega_0 t) \tag{2}$$

being applied at the base of Q_1. When V_i reaches a level sufficient to forward-bias the base–emitter diode, a collector current i_{cp} is flowing through the device, and its maximum value is controlled by V_i. As V_i decreases and the base–emitter diode is turned off, i_{cp} is truncated. We can therefore model i_{cp} as a clipped cosine pulse [53] and the interval t_0 of nonzero current divided by the period T of the input signal is referred to as conduction angle. Since the cosine pulses are periodic, we can express i_{cp} (and similarly i_{cn}) as a Fourier series with the amplitude of the nth harmonic given by [53]

$$I_n = I_{max} \frac{2}{\pi} \frac{\sin(n\delta)\cos(\delta) - n\sin(\delta)\cos(n\delta)}{n\left(n^2-1\right)} \tag{3}$$

where I_{max} is the peak collector current and $\delta = \pi t_0/T$. Fig. 4(a) shows the harmonic content calculated from (3) and normalized to I_{max}. It can be seen that the third harmonic features two maxima at $t_0/T \approx 0.33$ and $t_0/T \approx 0.67$. However, since (3) does not account for device parasitics and the effect of waveform clipping, precise large-signal models of the HBTs are required to predict the actual nonlinear behavior.

We therefore rely on the simulated harmonic amplitudes of the collector current, which are given in Fig. 4(b) as a function of the base–emitter voltage V_{be} for a fixed collector–emitter voltage of $V_{ce} = 1.1$ V and a 43-GHz input signal with amplitude of $V_i \approx 300$ mV (≈0 dBm in a 50 Ω system), which is a realistic value for oscillators at this frequency and can be generated by a signal generator without any problems. As predicted by (3), the simulated third harmonic also exhibits two maxima, the first at $V_{be1} \approx 0.66$ V and the second at $V_{be2} \approx 0.87$ V. A closer look at the simulated waveforms of i_{cp} and i_{cn} at $V_{be1} = 0.66$ V in Fig. 4(c) justifies our previous modeling as truncated cosine pulses for small V_{be}. However, the second maximum at $V_{be2} = 0.87$ V features

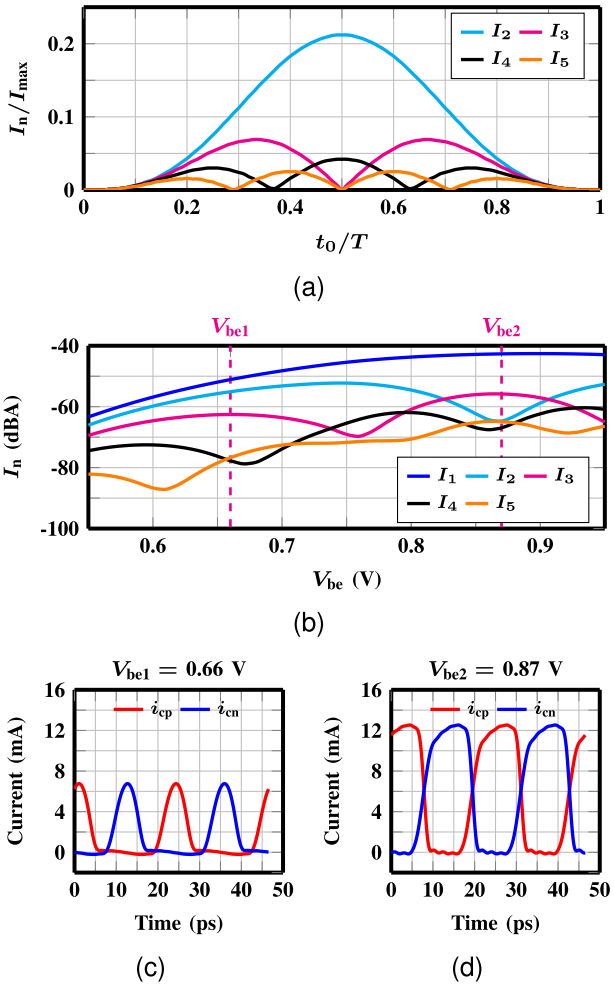

Fig. 4. Analysis of 3HG stage current harmonics at nodes Ⓑ. (a) Calculated harmonics based on clipped cosine model. (b) Simulated harmonics of collector current i_{cp} versus V_{be}. Simulated time-domain waveforms of i_{cp} and i_{cn} for (c) $V_{be1} = 0.66$ V and (d) $V_{be2} = 0.87$ V.

a larger third harmonic than the first maximum. As shown in Fig. 4(d), this is because the upper half-waves of the collector currents are clipped as well. As a result, the current waveforms have a square-wave shape and are therefore rich in odd harmonics. Also, the third harmonic component in Fig. 4(b) is larger than the second harmonic, as even harmonics exhibit a local minimum at $V_{be2} \approx 0.87$ V. Even though we expect the even harmonics to cancel out due to differential operation, this reduces undesired mixing products that may arise from a common-mode excitation at the input, for example caused by amplitude and phase imbalance of the transformer (TF) balun. It should be noted that the optimum bias point depends on the conduction angle and thus varies with the applied input power and the size of the HBTs. A larger device size (N_x) increases the current amplitudes, but larger input power is required to clip the upper half-wave of i_c due to a reduced input impedance. We therefore choose a moderate device size of $N_x = 3$ and bias the 3HG stage devices at $V_{be} = 0.87$ V and $V_{ce} = 1.1$ V. The 3HG stage devices are voltage-biased over series resistor $R_B = 1$ kΩ at the center tap of the input TF's secondary winding to inherently reduce V_{be} when the input power (and thus the base current

over the biasing resistor) increases. This ensures the efficient generation of higher harmonics even for larger input power levels [29]. Alternatively, a current-biasing scheme with a tail current source at the virtual ground node between Q_{1-2} emitters is also an effective way to generate square-wave current waveforms, but was omitted here due to an increased voltage headroom and its parasitic output capacitance, which gives rise to common-mode excitation at high frequencies.

We now turn back to Fig. 3 and continue our analysis with the switching quad. If Z_c denotes the impedance seen at the collectors of Q_{1-2}, further assuming $v_b = v_c$ are ideally ac-shorted over C_b, we notice that

$$v_b = v_b^+ - v_b^- = \underbrace{v_c^+ - v_c^-}_{v_c} = \left(\underbrace{i_{cp} - i_{cn}}_{i_c}\right) \cdot Z_c. \tag{4}$$

From Fig. 4, we know that i_c in our design has strong first and third harmonic components and can be expressed as

$$i_c = I_0 + I_1 \cdot \cos(\omega_0 t) + I_3 \cdot \cos(3\omega_0 t) \tag{5}$$

assuming that the fifth and higher odd-order harmonics can be neglected for facilitated derivations and using the fact that even harmonics are inherently suppressed under ideal differential excitation. As analyzed in [23], the impedance

$$Z_c = f(\omega, Z_0, \theta, C_b, g_m) \tag{6}$$

is a frequency-dependent function, mainly depending on the impedance presented by Q_{3-6} emitters and bases, capacitance C_b, as well as characteristic impedance Z_0 and electrical length θ of the transmission line TL_b. Using (5) and (6), we can write the first and third harmonic components of v_b separately

$$v_{b1} = v_{c1} = V_{b1} \cdot \cos(\omega_0 t) \tag{7}$$

$$v_{b3} = v_{c3} = V_{b3} \cdot \cos(3\omega_0 t) \tag{8}$$

where $V_{b1} = I_1 \cdot Z_c(\omega_0)$ and $V_{b3} = I_3 \cdot Z_c(3\omega_0)$. Similarly, we can express the harmonic components of v_e as

$$v_{e1} = V_{e1} \cdot \cos(\omega_0 t + \varphi_1) \tag{9}$$

$$v_{e3} = V_{e3} \cdot \cos(3\omega_0 t + \varphi_3) \tag{10}$$

noting that the network formed by C_b and TL_b introduces a frequency-dependent phase shift $\varphi(\omega)$ between base and emitter. Using (7)–(10) and assuming ideal four-quadrant multiplication in the switching quad [54], we are now able to formulate the mixing processes in the quad

$$v_{b1} \cdot v_{e1} = \frac{V_{b1} V_{e1}}{2}[\cos(\varphi_1) + \cos(2\omega_0 t + \varphi_1)] \tag{11}$$

$$v_{b1} \cdot v_{e3} = \frac{V_{b1} V_{e3}}{2}[\cos(2\omega_0 t + \varphi_3) + \cos(4\omega_0 t + \varphi_3)] \tag{12}$$

$$v_{b3} \cdot v_{e1} = \frac{V_{b3} V_{e1}}{2}[\cos(2\omega_0 t - \varphi_1) + \cos(4\omega_0 t + \varphi_1)] \tag{13}$$

$$v_{b3} \cdot v_{e3} = \frac{V_{b3} V_{e3}}{2}[\cos(\varphi_3) + \cos(6\omega_0 t + \varphi_3)]. \tag{14}$$

Equations (11)–(14) present important results. First, we note that (14) is the desired self-mixing process, which is why we wish to maximize the third harmonic voltage amplitudes (v_{b3}, v_{e3}) to generate a strong sixth harmonic component at the output. Second, from (11)–(13), we see other mixing products at $2f_0$ and $4f_0$, which need to be suppressed.[1] At last, we see from (11) and (14) that the dc components from the self-mixing processes can be eliminated for $\varphi_1, \varphi_3 = m \cdot 90°$ ($m = \pm 1, \pm 3, \ldots$). If we assume an ideal linear frequency dependence of $\varphi(\omega)$, this condition is fulfilled by

$$\varphi_1 = \frac{\varphi_3}{3} = \pm 90°. \tag{15}$$

Inserting (15) into (12) and (13), we realize that in this case the $4f_0$ terms possess opposite phases and (given that the amplitudes of both mixing products are equal) cancel each other out. This is a remarkable result because it means that an optimized phase shift between Q_{3-6} base and emitter ideally eliminates both the dc and $4f_0$ terms simultaneously. We conclude from our derivations that the network formed by C_b and TL_b needs to be optimized carefully since it controls the amplitude and phase relations of the switching quad and thus the harmonic components at the output of the BGC.

We first analyze the harmonics at the quad output nodes Ⓓ without any filtering network included. Fig. 5(a) shows the sixth harmonic component of the output current ($i_{out} = i_{op} - i_{on}$) versus C_b and the electrical length θ (specified at $f_0 = 43$ GHz) of transmission line TL_b. Since device and layout parasitics affect the optimum θ [23], the quad layout is simulated until the metals connecting to C_b and TL_b to consider the parasitic effects in the simulation. We see that the influence of C_b is minor above ≈40 fF, which allows us to choose our design point (DP) at $C_b = 65$ fF for easy implementation as a MIM capacitor. When moving along the (red dashed) line of constant $C_b = 65$ fF, the current contour shows its global maximum at $\theta \approx 65°$. Simulations confirm that V_{b3} exhibits a maximum at the same θ value, as expected from (14). To continue our analysis, we inspect the first eight simulated harmonics of i_{out} versus θ at constant $C_b = 65$ fF in Fig. 5(b). In accordance with our derivations, the even-order harmonics dominate over the odd-order ones. Also, the global maxima of the $2f_0$ and $6f_0$ components are both located around $\theta \approx 65°$. At the same value of θ, the $4f_0$ component exhibits its global minimum and is suppressed by more than 20 dB compared to the desired $6f_0$ component. Time-domain simulations show that v_b is ahead of v_e by 90°, which confirms that (15) holds and $\theta \approx 65°$ is the optimum electrical length of TL_b for our sextupler. TL_b is realized as a microstrip line with $Z_0 = 70\ \Omega$ using the top-most thick copper layer (ThCu2) for lowest loss and M3 ground layer to allow shielded supply routing below M3. Fig. 5(c) shows the simulated harmonics of i_{out} over different input frequencies, indicating that the inherent suppression of the fourth harmonic is maintained over a wide frequency range.

At last, the output matching network (OMN) is analyzed for high sixth harmonic output power and suppression of undesired harmonics. The simulations from Fig. 5(b) and (c) indicate that the closest even-order harmonics ($4f_0$, $8f_0$) are

[1] Note that we have neglected the $5\omega_0$ and higher terms in (5) and have assumed ideal four-quadrant multiplication in our derivation. In reality, there exist mixing terms at all harmonics of f_0, from which the ones close to $6f_0$ are most critical, while the others can be filtered out effectively.

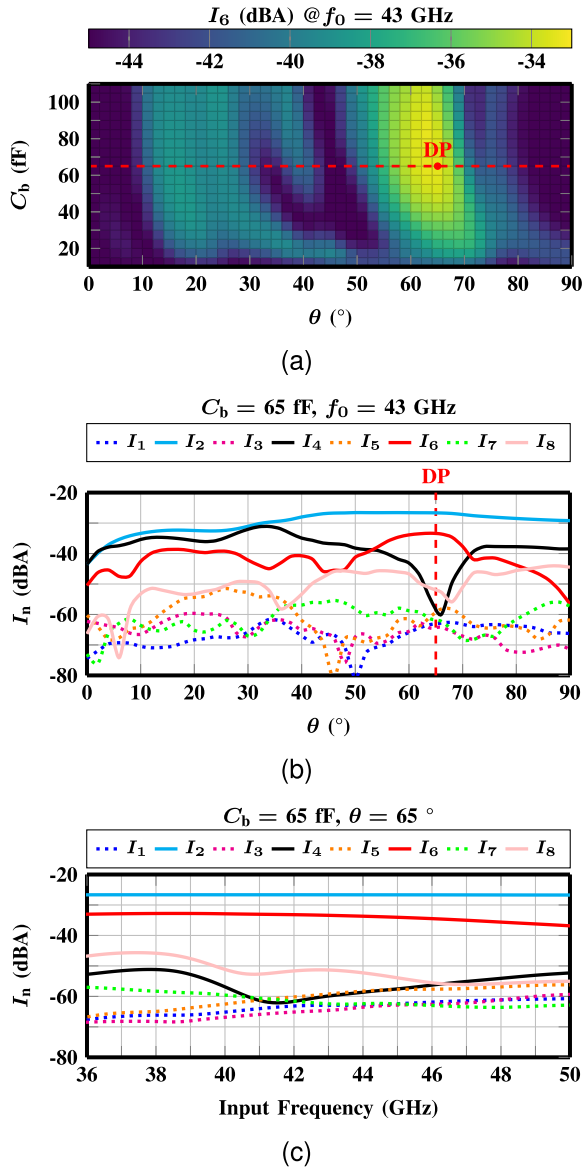

Fig. 5. Quad stage optimization at $f_0 = 43$ GHz through simulated output current ($i_{out} = i_{op} - i_{on}$) into nodes Ⓓ. (a) Sixth harmonic current versus C_b and electrical length θ of TL_b. (b) First–eighth harmonic versus θ at $C_b = 65$ fF. (c) Harmonic performance over input frequency at $C_b = 65$ fF, $\theta = 65°$.

suppressed below $6f_0$ thanks to the phase optimization in the quad. Since $2f_0$ remains the most critical undesired harmonic, a simple two-element high-pass network composed of L_1 and C_3 is chosen to filter out $2f_0$ components effectively while providing optimal load impedance at $6f_0$. Inductance L_1 is realized with a short metal line and C_3 is a metal–oxide–metal (MOM) capacitor formed between M3 and M4 due to their close proximity. The OMN is optimized through electromagnetic (EM) simulations, and its filtering effectiveness is assessed in Fig. 6. This is done by simulating the harmonic power levels at nodes Ⓓ (before OMN) and Ⓒ (after OMN) at the sextupler's output, with an input frequency of $f_0 = 43$ GHz and input power $P_{in} = 0$ dBm. The results confirm that the OMN's high-pass characteristics significantly enhance suppression of all harmonics below $6f_0$. At the design

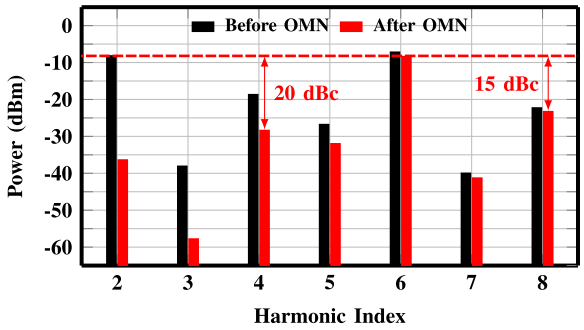

Fig. 6. Simulated harmonic power levels at sextupler output before OMN (at nodes Ⓓ) and after OMN (at nodes Ⓒ) for input frequency/power of 43 GHz/0 dBm.

frequency of $6f_0 = 258$ GHz, the OMN's insertion loss is 1.2 dB. The minimum HRR after the OMN is 15 dBc for the eighth harmonic, with all other harmonics being suppressed by at least 20 dBc with respect to the desired sixth harmonic. Given that the resonant amplification in the PA stage further improves the suppression of undesired harmonics, we have refrained from implementing higher order bandpass [29] or bandstop filters [55] in this work. For applications with more stringent HRR requirements than in our case, the harmonic suppression can be further improved by choosing a network with enhanced frequency selectivity around $6f_0$ at the expense of increased passive loss and silicon area.

B. Balance-Compensated Input TF

The input network (IM) in Fig. 3 is used to convert the single-ended input signal into a balanced signal at nodes Ⓐ, and for impedance matching. Both tasks can be combined effectively by using a TF-based balun, featuring a smaller form factor compared to Marchand baluns (MBs) with LC-based matching network. Our optimized input TF layout is shown in Fig. 7(a). We use the top-most thick copper layer (ThCu2) for the TF's primary coil and the secondary coil is formed by stacking both aluminum layers for reduced ohmic loss. The TF exhibits simulated primary inductance $L_p = 144$ pH with quality factor $Q_p = 22$, secondary inductance $L_s = 189$ pH with $Q_s = 14$, and coupling factor $k = 0.61$ (see Fig. 3) at the design frequency of 43 GHz. MOM capacitor $C_2 = 28$ fF between the balanced outputs and series MIM capacitor $C_1 = 75$ fF [not shown in Fig. 7(a)] at the input are added for matching purposes.

Even though primary and secondary coils do not fully overlap in our design, mutual parasitic capacitance between TF windings poses a challenge at mm-wave frequencies, since it results in undesired common-mode excitation [56]. The common-mode portion in turn causes amplitude and phase imbalance between nodes Ⓐ, which need to be minimized to avoid unwanted even-harmonic generation in the 3HG stage of our proposed sextupler. It has been shown that the common-mode excitation can be reduced by grounding the center tap of the TF's secondary coil and connecting an additional susceptance to the center tap of the primary winding [56] or vice versa [34]. In our design, the center tap of the secondary coil is ac-grounded through MIM capacitors

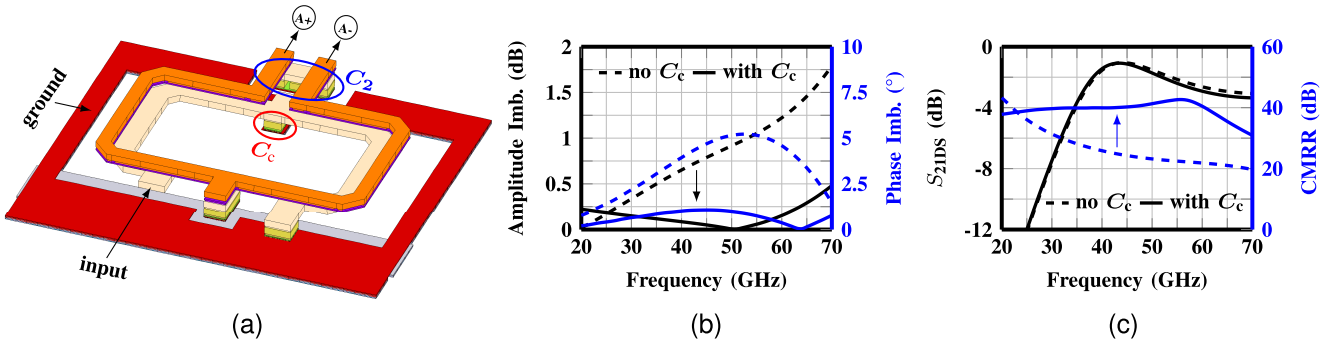

Fig. 7. Input TF design. (a) Layout view with balance-compensation capacitance C_c and matching capacitance C_2, (b) simulated amplitude/phase imbalance of the output signals, and (c) simulated single-ended-to-differential transmission S_{21DS} and CMRR.

[not shown in Fig. 7(a)] in close proximity to the TF area. Also, we have added a small balance-compensation capacitance $C_c = 11$ fF at the primary coil's center tap, which is realized as a MOM capacitor between metal layers M4 and ThCu1. The optimum value of C_c is found through EM simulations to also account for the parasitic on-chip ground plane inductance. To assess the effect of C_c on the balun performance, the TF is simulated with (solid lines) and without (dashed lines) the balance-compensation capacitance. Fig. 7(b) shows the amplitude and phase imbalance over a wide range of input frequencies. It can be seen that inserting C_c minimizes the imbalance at the design frequency of 43 GHz by 0.7 dB and 3.4°, respectively. Without balance-compensation, imbalances of up to 1.8 dB/5.2° are observed in the displayed frequency range. After adding C_c, the imbalance can be reduced to values below 0.5 dB/1.1°, indicating that the balance-compensation works effectively over a wide frequency range. As shown in Fig. 7(c), the reduced imbalance also reflects in an improved common-mode rejection ratio (CMRR), while the single-ended to differential transmission (S_{21DS}) is not affected by C_c.

C. J-Band Cascode Amplifier and Output Balun

As shown in Fig. 3, the sextupler is followed by a fully differential cascode amplifier (PA) optimized around $6f_0$ to further enhance output power and harmonic suppression. A fully differential topology with $R_1 = 8.3\ \Omega$ is opted to achieve high CMRR and hence robustness against any imbalance at the PA input. A conservative device size of $N_x = 4$ is selected for Q_{7-10} based on the available input power from the sextupler. Transistors Q_{7-10} are biased at peak f_T/f_{MAX} current density and draw 24 mA from a 2.6 V supply. The output network formed by $L_2 = 11$ pH and $C_4 = 20$ fF is optimized to transform a balanced impedance of 100 Ω into the PA's optimum load impedance. The simulated small-signal performance of the PA is summarized in Fig. 8(a), indicating a peak differential gain (S_{21DD}) of 12.2 dB with a 3-dB bandwidth of 226–282 GHz (22.1%). At the design frequency of 258 GHz, a CMRR of 19 dB is achieved. The large-signal simulations in Fig. 8(b) are carried out at 258 GHz, showing an input-referred 1-dB compression point around −6 dBm, which coincides with the maximum power delivered from the sextupler.

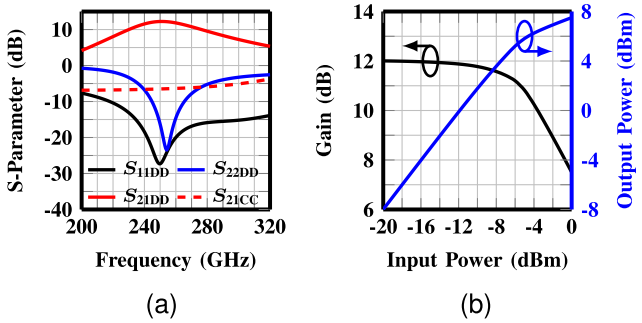

Fig. 8. Simulated performance of the J-band amplifier. (a) S-parameters versus frequency. (b) Gain and output power versus input power at 258 GHz.

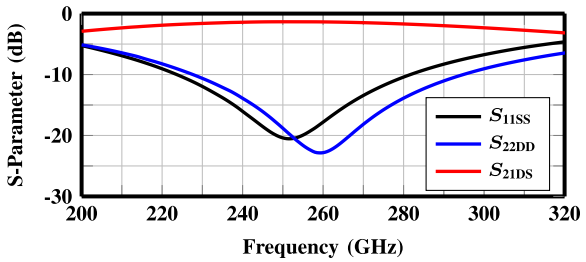

Fig. 9. Simulated mixed-mode S-parameters of the J-band MB including the output pad's parasitic capacitance.

The PA's balanced output signal is converted into a single-ended signal through a MB, which is added solely for measurement purposes. The simulated S-parameters of the MB including the effect of the output pad's parasitic capacitance are given in Fig. 9, demonstrating an insertion loss of $S_{21DS} = 1.35$ dB at 258 GHz. Both single-ended (S_{11SS}) and balanced (S_{22DD}) ports are well matched over a wide frequency range centered around 258 GHz.

IV. Experimental Results

The chip micrograph of the proposed frequency sextupler is given in Fig. 10. The total chip area including pads is 0.4 mm^2. The core area, which comprises the complete RF path except the output MB, measures only 0.06 mm^2.

Small-signal measurements covering the complete frequency range from 10 MHz up to 330 GHz are performed using a Keysight N5291A vector network analyzer (VNA) in two different setups. The frequency range below 220 GHz is covered in a single measurement with the broadband

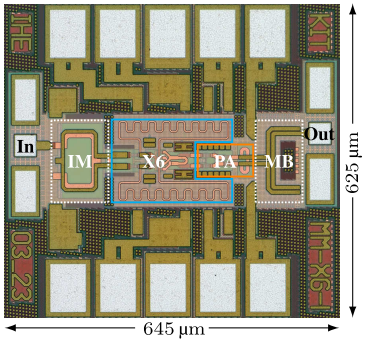

Fig. 10. Chip micrograph of the fabricated frequency sextupler.

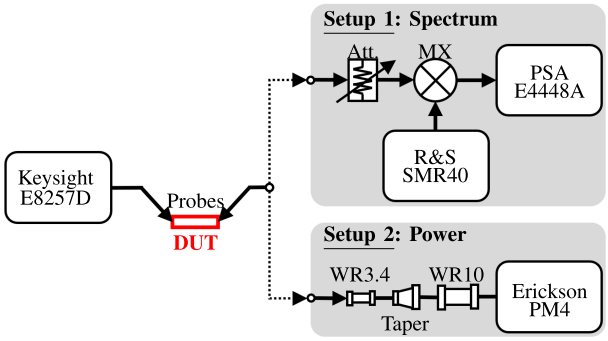

Fig. 12. Large-signal measurement setup.

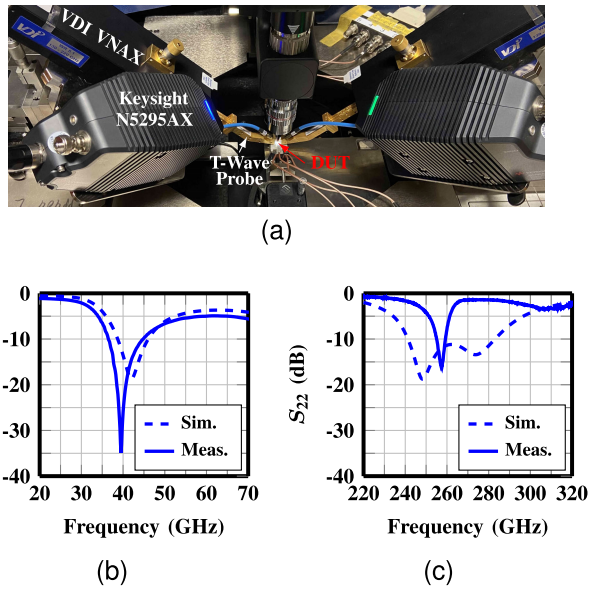

Fig. 11. Small-signal characterization. (a) 220 GHz broadband measurement setup. (b) Input reflection coefficient. (c) Output reflection coefficient.

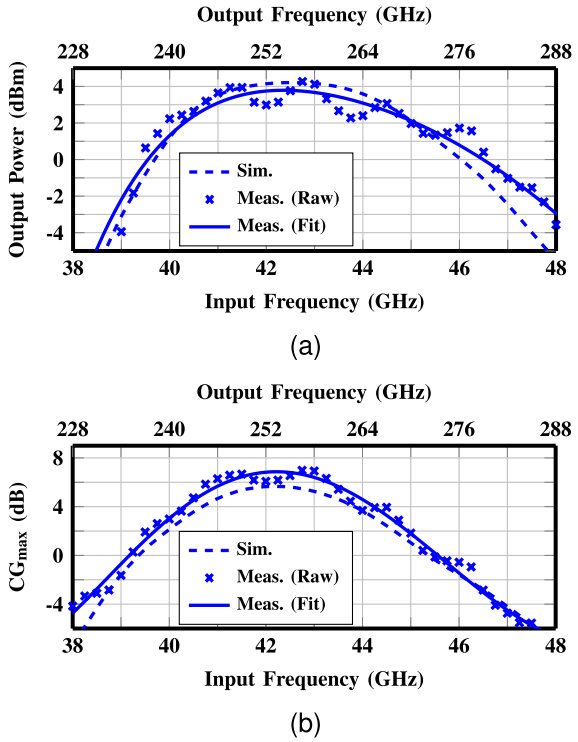

Fig. 13. Measured and simulated large-signal performance. (a) Sixth harmonic output power at fixed input power level of $P_{in} = 5$ dBm. (b) CG_{max} versus frequency.

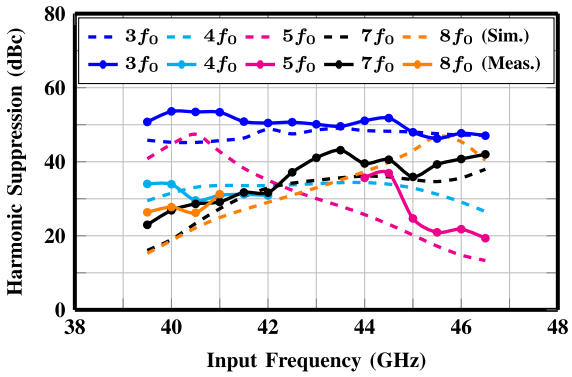

Fig. 14. Measured and simulated harmonic suppression within the 3-dB bandwidth at fixed input power level of $P_{in} = 5$ dBm.

measurement setup shown in Fig. 11(a) including a Form-Factor dual-band T-wave probe with integrated diplexer and two parallel VNA extenders at each port for the 0.01–130 GHz (Keysight N5295AX) and 130–220 GHz frequency range (VDI WR5.1-VNAX), respectively. The input reflection coefficient in Fig. 11(b) shows a good agreement between measurement and simulation and remains below −10 dB between 36–45 GHz (22.2%). For the frequency range from 220–330 GHz (WR3.4), VNA extenders from OML are used. Measured and simulated output reflection coefficients are given in Fig. 11(c).

The on-wafer measurement setup used for large-signal characterization of the frequency multiplier is shown in Fig. 12. The first harmonic input signal is generated by a Keysight E8257D signal generator. At the output side, spectrum measurements including the third to eighth harmonic power levels are performed by using an Agilent E4448A spectrum analyzer and different down-conversion mixers (MX) for the frequency ranges of 220–330 GHz (VDI WR3.4MixAMC-I) as well as 110–170 GHz (VDI WR6.5MixAMC-I). A variable waveguide attenuator precedes the mixer to avoid gain compression during down-conversion. An additional power measurement in the WR3.4 frequency range is conducted with an Erickson PM4 calorimetric power meter to verify the sixth harmonic output power. The measured and simulated sixth harmonic output

TABLE I
STATE-OF-THE-ART SILICON-BASED HIGHER ORDER FREQUENCY MULTIPLIERS AT J-BAND FREQUENCIES

Ref.	Technology (f_T/f_{MAX})	MF	Topology	f_c (GHz)	BW_{3dB} (%)	P_{out} (dBm)	Ways	P_{in} † (dBm)	CG_{max} (dB)	P_{dc} † (mW)	η_{dc} (%)	HRR (dBc)	Area§ (mm^2)
[57]	45 nm SOI (−/−)	4	PPX2–PPX2	280	3.6	-7	1	12	-19	93.5	0.21[a]	17[b]	0.13[c]
[58]	130 nm SiGe (300/450)	4	PPX4	255.5	5.0	-8.4	1	3.5	-10.4	22.4	0.65[a]	10	0.24
[59]	130 nm SiGe (300/500)	4	PPX2–PA–PPX2	236	20.3	5.5	2	0	7[c]	270	1.4	>20[b]	0.19[c]
[32]	40 nm CMOS (−/−)	6	PA–X3–PA–PPX2	257.5	6.6	3	4	-10	13[a]	890	0.22[a]	–	6.11[c]
[33]	130 nm SiGe (300/500)	6	X3–GCX2	229.5	6.5	-4	2	0	-1[c]	900	0.04[a]	>14	0.19[c]
[31]	130 nm SiGe (300/500)	6	X3–PA–PPX2	239	28.5	9	2	2	16	480	1.92	>15	0.2
This	130 nm SiGe (470/650)	6	BGCX6–PA	258	15.5	4.3	2	5	7	119	2.2	>20	0.06
This*	130 nm SiGe (470/650)	6	BGCX6–PA	258	15.5	5.6	2	5	8.3	119	3.1	>20	0.06

* excluding output balun † at peak P_{out} § core area [a] calculated from table data [b] simulated [c] estimated

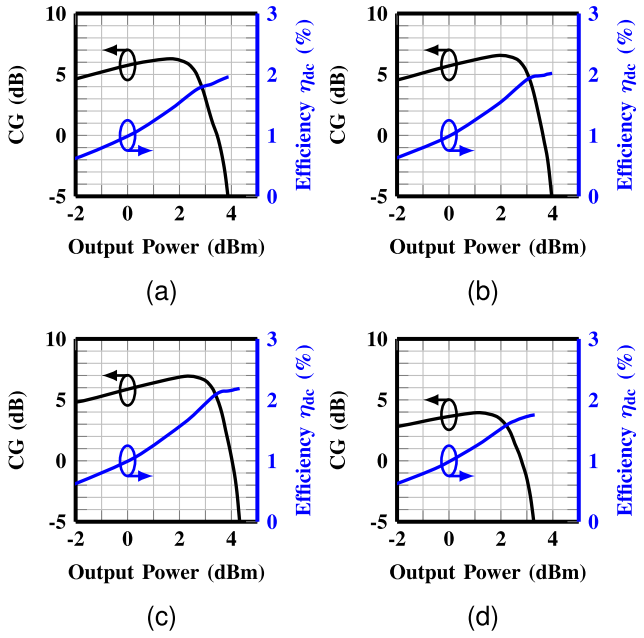

Fig. 15. Measured CG and dc-to-RF efficiency at input/output frequency of (a) 41/246 GHz, (b) 42.5/255 GHz, (c) 43/258 GHz, and (d) 44.5/267 GHz.

power and the maximum conversion gain (CG_{max}) are plotted in Fig. 13. The results show excellent agreement between measurement and simulation, with peak measured values of 4.3 dBm for output power and 7 dB for CG_{max} at 256.5 GHz. The measured results also indicate a 40 GHz wide output power 3-dB bandwidth (BW_{3dB}) ranging from 238–278 GHz (15.5%). Within this bandwidth, all other harmonics are suppressed by more than 20 dBc, as shown in Fig. 14. Around the center frequency, a minimum harmonic suppression of more than 30 dBc is achieved. At the peak output power of 4.3 dBm, the sextupler and output amplifier draw 23.5 mA / 24 mA from their 2.4 V / 2.6 V supplies, respectively. This results in a total dc power consumption of 118.8 mW. The measurement results of CG and dc-to-RF efficiency are plotted in Fig. 15 versus output power at various frequencies. A peak efficiency of $\eta_{dc} = 2.2\%$ is demonstrated at 258 GHz. Consistent results are achieved by repeating measurements on different samples.

V. CONCLUSION

We have introduced a single-stage sextupler based on a BGC, implemented in a 130-nm SiGe BiCMOS technology with $f_T/f_{MAX} = 470$ GHz/650 GHz. Our analysis of the harmonic generation and mixing mechanisms in the BGC has revealed that it is possible to simultaneously maximize the desired sixth harmonic and inherently suppress the most critical mixing products at the fourth and eighth harmonic frequencies by carefully optimizing the phase relations in the switching quad. Thanks to this inherent suppression mechanism, the requirements on the filter network are greatly relaxed. A single cascode amplification stage is included, helping us to achieve a peak output power of 4.3 dBm and a minimum harmonic suppression of $>$ 30 dBc at 257 GHz. Further, we have shown the effectiveness of adding a small balance-compensation capacitance at the primary coil's center tap in a TF-based balun to improve amplitude and phase imbalance over a wide frequency range.

In Table I, we provide a comparison of silicon-based higher order frequency multipliers at J-band frequencies. Among the listed studies, our design stands out by achieving the highest dc-to-RF efficiency and by occupying the smallest silicon core area. By replacing the traditional tripler-doubler cascade used in prior-art sextuplers with our proposed single-stage approach, approximately 70% of core area and more than 75% of dc power can be saved when compared to state-of-the-art sextuplers at similar frequencies and output power levels. The compilation in Table I also indicates that our proposed design is favored by an enhanced suppression of undesired harmonics and a competitive 3-dB bandwidth. Given these results, the

presented single-stage frequency sextupler is highly attractive for realizing compact and power-efficient LO paths in phased arrays or any other multichannel systems.

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