A Cryogenic Gallium Nitride Full Bridge for Use in a Thermally Insulating Dual Active Bridge

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***Abstract*—In this paper, a Liquid Nitrogen (LN_2) cooled Gallium Nitride (GaN) Cryogenic Full Bridge (CFB) is presented as part of a Dual Active Bridge (DAB) for use in a hybrid Liquid Hydrogen (LH_2) High Temperature Superconductor (HTS) transmission line. The concept of a 20 kW DAB with cryogenic parts is outlined and the design of the CFB as one of the cryogenic parts is presented. Furthermore, the construction of a cryogenic test bench is described which is used to validate the functionality of the CFB and to characterize it. Finally, the first measurements of the prototype down to 82 Kelvin are presented, which confirm the increased efficiency of the GaN semiconductors at cryogenic temperatures.**

***Index Terms*—Wide-Bandgap, GaN, Cryogenic, Dual Active Bridge (DAB), Measurements**

I. Motivation

Due to the increasing number of superconducting applications, such as superconducting drives for electric aviation [1], [2], generators for energy production [3], [4] or cables for energy transmission [5], [6], the operation of power electronics in combination with superconducting applications is becoming an increasingly important research topic.

Nowadays, power electronics work at much higher ambient temperatures than the cryogenic system and the connection between these two parts is made with copper-based current supplies, which leads to a high heat input into the cryogenic area. This in turn increases the necessary cooling power and thus reduces the overall efficiency of the system. One way of reducing the heat input is to replace the copper-based current supplies with a galvanically isolated converter, whereby the galvanic isolation also serves as a thermal barrier to separate the cryogenic area from the environment.

Therefore, one part of the power electronics operates in the cryogenic temperature range which, depending on the used semiconductor material and component technology, leads to lower conduction and switching losses and thus even further increases the system efficiency [7]. This paper will investigate the opportunity to improve efficiency by using semi-cryogenic converters instead of copper feeders. For this purpose, a widely used galvanically isolated converter topology, the DAB, is examined.

This work is motivated by an LH_2 project, in which a hybrid LH_2-HTS transmission line, similar to the idea pointed out in [8], is developed and constructed. Due to the cryogenic boiling temperature of the hydrogen of $21.15\,\mathrm{K}$ [9] the system intrinsically provides the low temperatures necessary for superconductor operation, which additionally can be used for cooling the power electronics as well.

The paper is structured into six sections. In the following section II, the concept of a DAB with cryogenic converter parts is outlined. One of the cryogenic parts, the CFB is described in detail in section III. The construction of a cryogenic test bench, with which the functionality of the CFB is validated, is pointed out in section IV. First measurements are presented in section V. Finally, in section VI a summary and an outlook is given.

II. Cryogenic Gallium Nitride based Dual Active Bridge

A possible topology with an intrinsic galvanic isolation is the DAB [10]. This circuit basically consists of two full bridge circuits, connected to a Medium Frequency (MF) or High Frequency (HF) transformer, allowing a magnetically coupled energy transmission. Both, the input and output port are DC ports, making this topology suitable for the interface connection of an HTS. In the following, the design of such a DAB operating at the transition between the cryogenic and the ambient temperature system parts is described. The topology is depicted in Fig. 1.

One of the two full bridges, the CFB, and one of the transformer windings work at cryogenic temperatures. The second full bridge, second winding and the transformer core operate at ambient temperature. Hence, the thermal insulation is between both transformer windings which is challenging

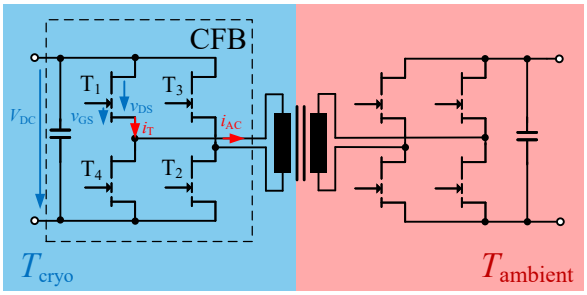


Fig. 1: DAB with CFB and thermally insulating transformer

for the transformer design. The idea is similar to the setup published in [11], but instead of silicon semiconductors GaN-HEMTs are used, allowing higher switching frequencies and therefore a more compact transformer design.

Due to the promising cryogenic behavior of GaN-HEMTs [12]–[15], the *GS66516T* transistors [16] from *Infineon/GaN Systems* are used in this work. These are 650 V, 60 A rated devices resulting in a DC link voltage V_{DC} of 400 V and a desired rated power P_{N} of 20 kW. When operating the DAB in Single Phase Shift (SPS) mode, the transmitted power is controlled by the phase shift φ between the voltages of the two full bridges. With the equations given in [10] the transmitted power can be calculated for a $1:1$ transformer ratio to

$$P = \frac{V_{\mathrm{DC1}} \cdot V_{\mathrm{DC2}} \cdot \varphi}{2 \cdot \pi \cdot L_\sigma \cdot f_{\mathrm{sw}}} \cdot \left(1 - \frac{|\,\varphi\,|}{\pi}\right). \tag{1}$$

The maximum power is transmitted for $\varphi = \frac{\pi}{2}$. It is proportional to the DC voltages V_{DC1}, V_{DC2} and inversely proportional to the stray inductance L_σ of the transformer and the switching frequency f_{sw}. To keep the design simple, the two DC link voltages are chosen $V_{\mathrm{DC1}} = V_{\mathrm{DC2}} = V_{\mathrm{DC}}$ equal. To reach the desired power of $P_{\mathrm{N}} = 20\,\mathrm{kW}$ with the given DC link voltage V_{DC}, the product of $L_\sigma \cdot f_{\mathrm{s}}$ must not exceed $1\,\mathrm{H\,s^{-1}}$. Hence, the maximum switching frequency is limited by the stray inductance of the transformer.

The detailed transformer design will be published in a subsequent paper. However, first analytic calculations and Finite Element Method (FEM) simulations showed an expected value of the stray inductance L_σ in the range of 2.5..7 µH, highly dependent on the gap between the ambient primary and cryogenic secondary winding. Here, an optimum is to be found to ensure thermal insulation on the one hand and to reduce the stray inductance of the transformer for reaching the rated power of 20 kW on the other hand. With the simulated values for the stray inductance, the rated switching frequency was set to $f_{\mathrm{sw}} = 100\,\mathrm{kHz}$. The design characteristics of the DAB are summarized in Tab. I.

To increase the transmitted power, several GaN-DAB cells can be connected in series and parallel. Furthermore, due to the positive temperature coefficient of the on-resistance $R_{\mathrm{DS,on}}$ and the negative temperature coefficient of the transconductance g_{m} over the full temperature range down to 93 K, as shown in [12], [14], a direct parallelization of GaN-HEMTs even at cryogenic temperatures is suitable and promising.

TABLE I: Design characteristics of the proposed cryogenic DAB

Semiconductors	*GaN Systems GS66516T*
Rated power P_{N}	20 kW
DC link voltage V_{DC}	400 V
Switching frequency f_{sw}	100 kHz
Stray inductance transformer L_σ	2.5..7 µH

The power electronics design of both full bridges, the cryogenic and the conventional one, is identical, offering a direct comparison of the circuits. The difference only lies in the cooling. While the "warm" full bridge is cooled using conventional water cooling, the cryogenic one is $\mathrm{LN_2}$ cooled. $\mathrm{LN_2}$ is used because of its low boiling point at 77.15 K [9], its good availability and for safety reasons. The detailed design of the full bridge is outlined in the next section.

III. Design of the Cryogenic Full Bridge

The challenge in designing the CFB is to ensure a safe operation of all components at cryogenic temperatures. While the GaN-HEMTs itself are suitable for temperatures down to 77 K, care must be taken into a proper selection of the other necessary components such as the DC link capacitors, the gate-drivers and their power supplies.

A split DC link is used, consisting of six 100 nF NPO ceramic capacitors as primary link and a single 210 µF Polypropylene (PP) secondary capacitor. According to [7] both capacitor types are suitable for cryogenic temperatures. As gate driver two *SI8275AB-IS1* isolated half-bridge ICs from *Skyworks* are used. Several cryogenic measurements with this driver family are reported in [17] and [18], showing a successful operation at temperatures down to 77 K. The isolated power supply of the drivers at cryogenic temperatures is challenging. An overview of several DC/DC converters exposed to 77 K is given in [18], showing that none of the investigated devices performs well at cryogenic temperatures. For that reason, the proposed design positions the power supplies spatially separated from the gate drivers and the GaN-HEMTs, offering a thermal insulation. The thermal conductivity between the cold power section and the "warm" signal processing section on the Printed Circuit Board (PCB) is further reduced by board cut-outs. Note that the complete gate loop itself, consisting of the GaN-HEMT, the gate driver, the gate resistors and buffer capacitors is located in the cold section and therefore stays as small as possible. Furthermore, the power supplies can be heated by optional heating resistors if necessary. To measure the on-resistance of the GaN devices, the clamping circuit presented in [19] is used. The measurement principle is described in detail in section V.

The PCB design and the results of a thermal steady state simulation are shown in Fig. 2. The simulation was performed

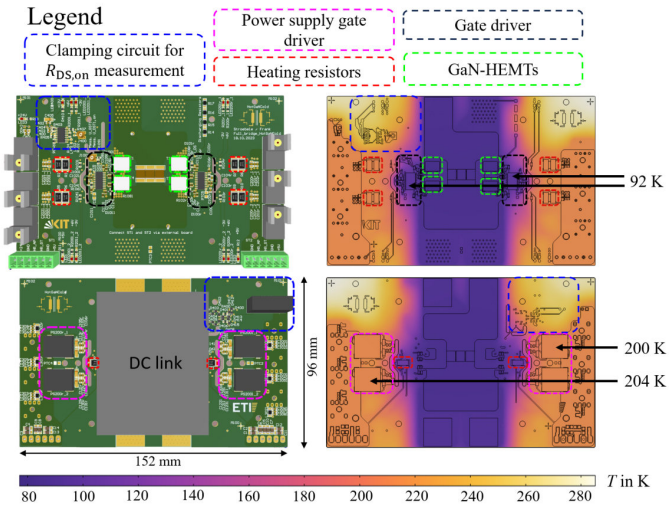


Fig. 2: PCB and thermal simulation of the developed GaN CFB

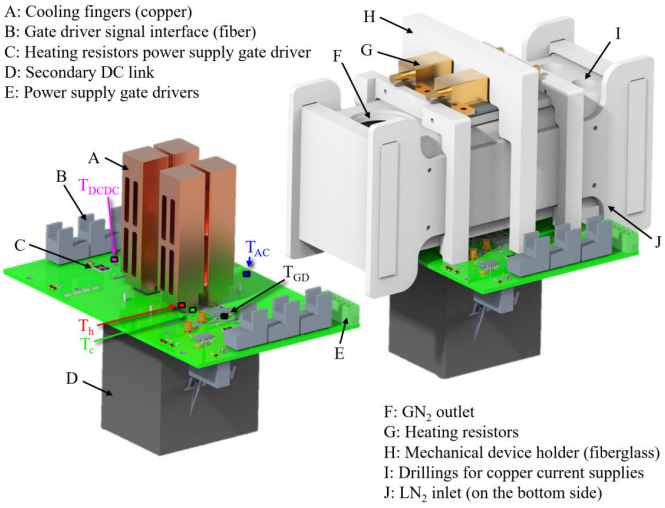


Fig. 3: LN_2 heatsink for cryogenic cooling of the full bridge

with *COMSOL Multiphysics*, using the heat transfer and thermal radiation module. As the entire PCB is later located in a vacuum, no convection is considered. Several simplifications are made. All electronic components are defined as solid copper bodies, the case temperature of the GaN-HEMTs is set to constant 77 K and the ambient temperature, which is relevant for the thermal radiation calculation, is set to 300 K. The aim of the simulation is to validate the thermal insulation between the power part in the middle of the PCB and the signal processing part on the left and right side. This separation is clearly visible in Fig. 2. While the temperatures of the GaN-HEMTs, DC capacitors and gate drivers remain below 100 K, the power supply for the gate drivers, consisting of four *MGN1D050603MC-R13* DC/DC converters, reaches temperatures equal or greater than 200 K.

IV. Design of the Cryogenic Power Electronics Test Bench

Instead of putting the whole setup into LN_2, an indirect cooling with finger-shaped copper heat sinks is used to ensure that only the GaN-HEMTs are cooled. This concept is pictured in Fig. 3. One end of the cooling fingers is placed on the top-side cooled transistors. As Thermal Interface Material (TIM) indium foil is used since indium has a high thermal conductivity of $\lambda_{\mathrm{Indium}} = 81.6\,\mathrm{W\,K^{-1}\,m^{-1}}$ and shows good formability [9], leading to smaller thermal contact resistances. The thermal resistance of the TIM layer is calculated using

$$R_{\mathrm{th,TIM}} = \frac{1}{\lambda_{\mathrm{Indium}}} \cdot \frac{d_{\mathrm{TIM}}}{A_{\mathrm{HEMT}}}. \tag{2}$$

With a thickness d_{TIM} of 200 µm and a cooling pad area A_{HEMT} of $8.27\,\mathrm{mm} \cdot 5.64\,\mathrm{mm}$ [16] the thermal resistance $R_{\mathrm{th,TIM}}$ of the TIM layer is about $\approx 0.05\,\mathrm{K\,W^{-1}}$. Similarly, the thermal resistance of one copper finger can be estimated to $R_{\mathrm{th,h}} \approx 0.26\,\mathrm{K\,W^{-1}}$. The fingers are glued into a rectangular fiberglass pipe, using *Stycast1266*. Before operation, LN_2 is fed into the pipe. During operation, the heat dissipating into the LN_2 causes it to evaporate at the cooling fingers. Assuming maximum semiconductor losses $P_{\mathrm{loss,HEMT}}$ of 25 W for a single transistor leads to a maximum case temperature T_{c} of

$$T_{\mathrm{c}} = P_{\mathrm{loss,HEMT}} \cdot (R_{\mathrm{th,TIM}} + R_{\mathrm{th,h}}) + T_{\mathrm{LN2}} \approx 85\,\mathrm{K} \tag{3}$$

For simplification, the thermal contact resistance from copper to LN_2 is neglected and the constant LN_2 boiling temperature is assumed at the contact surface of the copper fingers with the liquid. To keep the thermal contact resistance as small as possible, several cut-outs increase the surface area.

A siphon design as shown in Fig. 4 lets the emerging Gaseous Nitrogen (GN_2) only escape via an outlet pipe. By measuring the evaporation rate, the heat flow into LN_2 and hence the occurring losses of the power converter can be determined. For dimensioning the whole LN_2 piping, the evaporation rate for a continuous CFB operation is taken. As the worst-case scenario semiconductor losses $P_{\mathrm{loss,tot}}$ of 100 W are considered. These can be converted into the evaporation rate of the nitrogen using

$$\dot{V}_{\mathrm{LN2}} = 2 \cdot M_{\mathrm{N}} \cdot P_{\mathrm{loss,tot}} \cdot \frac{1}{\rho_{\mathrm{LN2}} \cdot \Delta H_{\mathrm{vap,N}}}. \tag{4}$$

With the molar mass $M_{\mathrm{N}} \approx 14.007\,\mathrm{g\,mol^{-1}}$, the mass density $\rho_{\mathrm{LN2}} \approx 0.81\,\mathrm{kg\,L^{-1}}$ and the evaporation enthalpy of $\Delta H_{\mathrm{vap,N}} \approx 5.58\,\mathrm{kJ\,mol^{-1}}$ of LN_2 as given in [9], follows a volume flow rate of $\dot{V}_{\mathrm{LN2}} \approx 0.62\,\mathrm{mL\,s^{-1}}$ for the liquid. With its much lower mass density $\rho_{\mathrm{GN2}} \approx 1.25\,\mathrm{g\,L^{-1}}$ the volume flow rate of the vaporizing nitrogen is $\dot{V}_{\mathrm{GN2}} \approx 402\,\mathrm{mL\,s^{-1}}$. For the GN_2, pipes with 26 mm inner diameter are taken, resulting in flow rates smaller than $v_{\mathrm{max,GN2}} = 0.757\,\mathrm{m\,s^{-1}}$. The pipes for LN_2 have an inner diameter of 17 mm which is chosen to simplify and accelerate the LN_2 filling. Smaller di-

ameters make filling more difficult due to evaporation through contact with the warm pipe wall.

To enable measurements at a defined temperature above the boiling temperature of nitrogen, heating resistors are mounted on the other side of the cooling fingers (cf. Fig. 3). The temperatures at different locations (cf. Fig. 3 and Fig. 4) are measured and supervised using PT1000 temperature sensors. For galvanic isolation, the *AMC3336* Analog Digital Converter (ADC) is used, enabling e.g. a measurement directly between the cooling fingers and the case of the GaN-HEMT. The same sensor type is used to measure the LN_2 level inside the LN_2 tank.

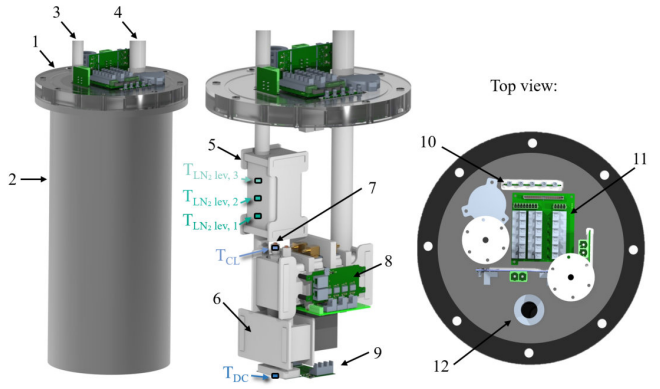


Fig. 4: Cryogenic test bench for CFB characterization

To prevent icing of the CFB, the whole setup operates in a hermetic chamber, that can be either flooded with GN_2 or dry compressed air. Alternatively, it can be evacuated. In the intended DAB operation, an evacuated chamber is desired to prevent any convective flow of heat. To monitor the pressure, a *PVC4100* vacuum transducer based on a Pirani sensor is used. However, the results presented in this paper are measured with dry air at ambient pressure, due to microcracks at several adhesive joints detected after the first cryogenic measurements, caused by different expansion coefficients of various fiberglass materials and copper. However, further cryogenic measurements are still possible since the leakage rates through the microcracks are small enough.

The DC port, AC port, the gate signals and all measurement signals are routed outside using in-house developed vacuum feedthroughs, consisting of several PCBs that are glued into the vacuum chambers cover.

V. Measurements

This section presents cryogenic measurements of the developed CFB. First, the correct function of the circuit is validated at cryogenic temperatures by applying single pulses to the circuit. The recorded traces are used to determine the on-resistance $R_{\mathrm{DS,on}}$ over the full temperature range of the case temperature T_{c} from Room Temperature (RT) down to $82\,\mathrm{K}$. Furthermore, the temperature distribution in the test setup and on the power PCB is examined in more detail. Eventually, the continuous operation of the circuit is investigated.

A. Functional Testing at Cryogenic Temperatures

For the functional test, an ohmic load with a parasitic inductive component is connected to the AC terminals of the CFB and single pulses are applied at different DC link voltages. The waveforms of v_{GS}, v_{DS} and $v_{\mathrm{DS,on}}$ of transistor T1 (cf. Fig. 1) as well as of the load current i_{AC} are recorded. The voltage $v_{\mathrm{DS,on}}$ is measured using the clamping circuit shown in Fig. 8 and corresponds to the drain-to-source voltage of T1 during on-state.

For all voltage measurements, optically isolated probes are deployed, Tab. II shows a list of the measuring devices used. The constructed test bench during the cooling phase is shown in Fig. 5. Before every cryogenic measurement, the chamber is flooded with dry air. A *Sensirion SHT21* humidity sensor monitors the humidity inside to prevent icing. After ensuring a relative humidity smaller than $10\,\%$, the cooling starts by pouring LN_2 into the fiberglass pipe. The case temperature can be adjusted via the filling rate. To reduce the mechanical stress on the cooled parts, the rate should be moderate, resulting in a test duration of $\approx 3\,\mathrm{h}$ for the entire series of measurements.

TABLE II: Measurement setup on-resistance measurements

Oscilloscope	*LeCroy Wavesurfer 4104HD,* 12 bit, 1 GHz
Probe for v_{GS} measurement	*PMK Firefly FF-1500* with *FF-MMCX-25V* tip
Probe for v_{DS} measurement	*Micsig MOIP02P* with OP500-2 tip
Probe for $v_{\mathrm{DS,on}}$ measurement	*Micsig MOIP02P* with OP10-2 tip
Probe for i_{AC} measurement	CWT *CWTUM/1/B* Rogowski coil 300 A, 9 Hz – 30 MHz

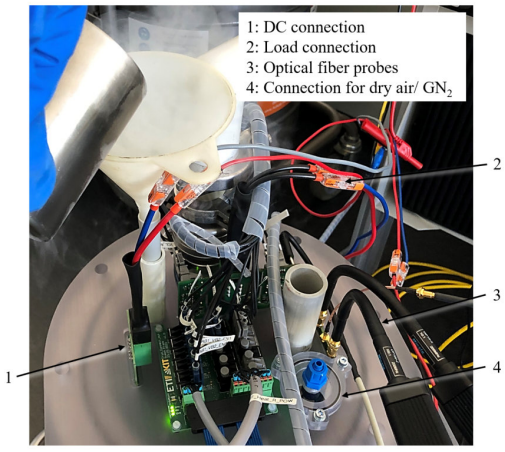


Fig. 5: Test bench for cryogenic measurements

The results for a DC link voltage V_{DC} of $400\,\mathrm{V}$ and a load resistor R_{load} of $7.5\,\Omega$ at case temperature T_{c} of $99\,\mathrm{K}$ are shown in Fig. 6 for a complete switching period, Fig. 7 focuses

on the turn-on and turn-off event. In the latter, the fall time $t_{\mathrm{fall,cryo}} = 8.8\,\mathrm{ns}$ and rise time $t_{\mathrm{rise,cryo}} = 7.2\,\mathrm{ns}$ of the drain-to-source voltage v_{DS} are marked. The values $t_{\mathrm{fall,rt}} = 9.6\,\mathrm{ns}$ and $t_{\mathrm{rise,rt}} = 6\,\mathrm{ns}$ at RT are similar.

At the turn-off event a high overvoltage resulting in a maximum drain-to-source voltage $v_{\mathrm{DS,max}}$ of $\approx 667\,\mathrm{V}$ occurs (cf. Fig. 7b). However, it could be proven that this overvoltage is caused by the developed feedthrough PCB of the measurement signals and does not correspond to the real voltage across the semiconductor. Measurements at RT with and without the feedthrough show that the voltage directly at the GaN HEMT is only $\approx 513\,\mathrm{V}$. Hence, the transients measured at cryogenic temperatures with the feedthrough are not reliable. Nevertheless, the stationary end values used e.g. for the $R_{\mathrm{DS,on}}$ calculation are not significantly influenced.

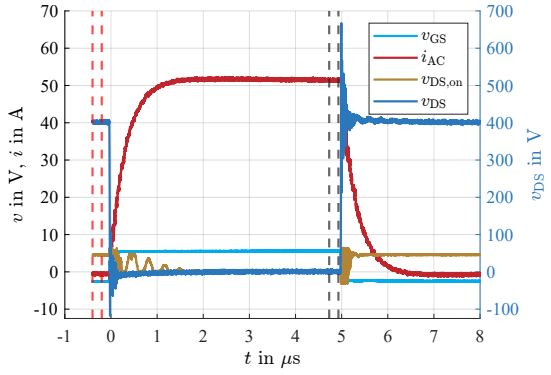
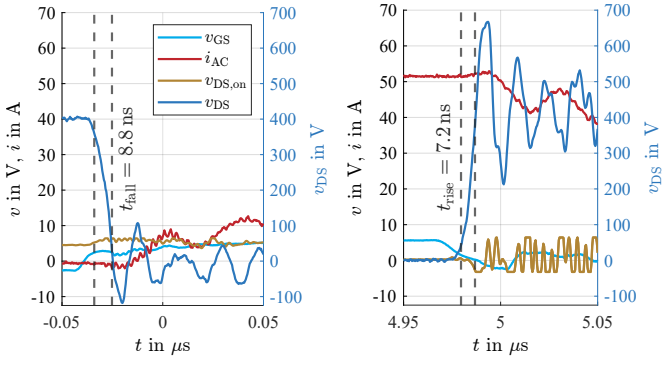


Fig. 6: Waveforms for one switching period at $T_{\mathrm{c}} = 99\,\mathrm{K}$, $V_{\mathrm{DC}} = 400\,\mathrm{V}$ and $R_{\mathrm{load}} = 7.5\,\Omega$

When looking at the gate voltage v_{GS}, a reduction of the absolute values of the positive and negative driver voltage supplied by the *MGN1D050603MC-R13* DC/DC converter is observed. During operation at RT, the positive and negative voltages $v_{\mathrm{GS,pos}}$ and $v_{\mathrm{GS,neg}}$ are $5.85\,\mathrm{V}$ and $-2.81\,\mathrm{V}$, respectively. These voltages drop to $5.6\,\mathrm{V}$ or $-2.56\,\mathrm{V}$ during the cooling process down to the DC/DC converter temperature T_{DCDC} of $\approx 150\,\mathrm{K}$. To compensate for this drop, the integrated heating resistors can be used to increase the temperature T_{DCDC} up to $\approx 180\,\mathrm{K}$ and thus the voltages to $5.68\,\mathrm{V}$ and $-2.72\,\mathrm{V}$.



(a) Turn-on (b) Turn-off

Fig. 7: (a) Turn-on and (b) turn-off events at $T_{\mathrm{c}} = 99\,\mathrm{K}$, $V_{\mathrm{DC}} = 400\,\mathrm{V}$ and $R_{\mathrm{load}} = 7.5\,\Omega$

In total, the functionality of the CFB is validated over the complete investigated temperature range down to $T_{\mathrm{c}} \approx 82\,\mathrm{K}$. Even at the minimum measured temperature $T_{\mathrm{DCDC}} \approx 150\,\mathrm{K}$ that corresponds to $T_{\mathrm{c}} = 82\,\mathrm{K}$ (cf. Fig. 12a) and without using the optional heating resistors, the DC/DC converter voltages are high enough to ensure safe switching.

B. Wide Temperature Range On-Resistance Measurement

The traces shown in Fig. 6 are used for determining the on-resistance $R_{\mathrm{DS,on}}$. In the interval between the two red dotted lines, the offset of i_{AC} is measured and between the two black dotted lines, the values of i_{AC} and $v_{\mathrm{DS,on}}$ are averaged for the $R_{\mathrm{DS,on}}$ calculation. Hence, these traces are recorded for each operation temperature. The temperature range of the case temperature T_{c} for the measurement is from RT down to $\approx 82\,\mathrm{K}$ in $\approx 25\,\mathrm{K}$ steps. At each temperature, calibration of the clamping circuit and variation of different DC link voltages V_{DC} from $40\,\mathrm{V}$ to $400\,\mathrm{V}$ are performed. Three measurements with a constant ohmic load are recorded for all operating points. The procedure is shown in Fig. 8.

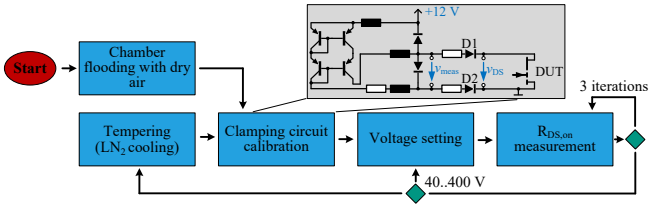


Fig. 8: Procedure of the cryogenic $R_{\mathrm{DS,on}}$ measurement

As mentioned in section III, the clamping circuit described in [19] is used for measuring the voltage V_{DS} during on-state. The circuit is pictured in Fig. 8. It is based on a current mirror and several clamping diodes. The diodes D_1 and D_2 are within the measurement path. Hence, both diodes must show identical behavior to ensure that the forward voltage across both diodes during the on-state of the transistor is identical. Further, they must operate at the same temperature. Temperature sensors are attached to both diodes to monitor their temperatures T_{D1} and T_{D2} during the measurement series.

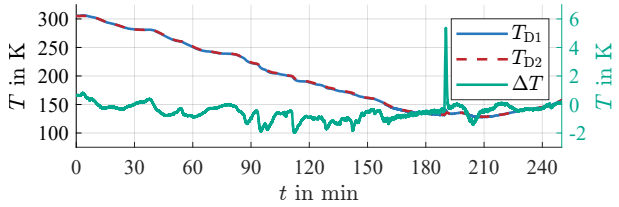


Fig. 9: Temperatures of the clamping diodes during the entire cryogenic experiment

The results are depicted in Fig. 9. As shown, the difference between both temperatures ΔT stays smaller than $2\,\mathrm{K}$ for

the whole measurement series until $t = 180\,\text{min}$. However, when measuring the voltage v_{meas} (cf. Fig. 8) without any load, but turned on transistor at different temperatures, the temperature-dependent offset-voltage v_{offset} depicted in Fig. 10 ($T_{\text{clamping}} = (T_{\text{D1}} + T_{\text{D2}})/2$) can be observed. For this reason, the aforementioned calibration of the clamping circuit is carried out for every operation temperature.

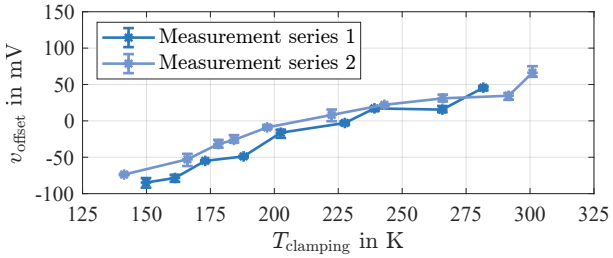
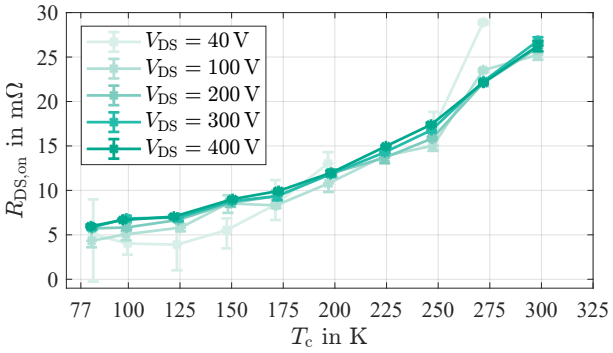
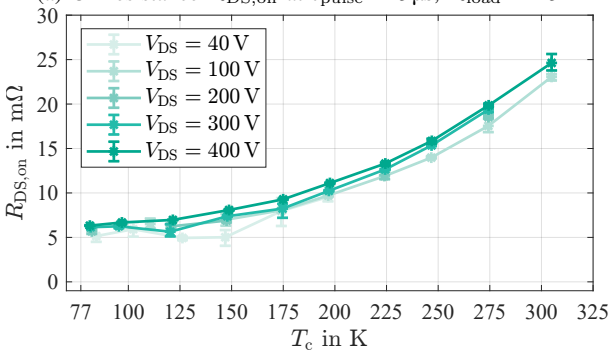


Fig. 10: Offset voltage of the clamping circuit

In Fig. 10 and the following graphs, the asterisks mark the measured mean values and the bars are the minimum and maximum values. The measured on-resistance values $R_{\text{DS,on}}$ for a constant ohmic load R_{load} of $15\,\Omega$ or $7.5\,\Omega$ and various DC link voltages V_{DC} are depicted over the entire temperature range in Fig.11a and Fig. 11b. Note, that the CFB is rated for a DC link voltage V_{DC} of $400\,\text{V}$.



(a) On-resistance $R_{\text{DS,on}}$ at $t_{\text{pulse}} = 5\,\mu\text{s}$, $R_{\text{load}} = 15\,\Omega$



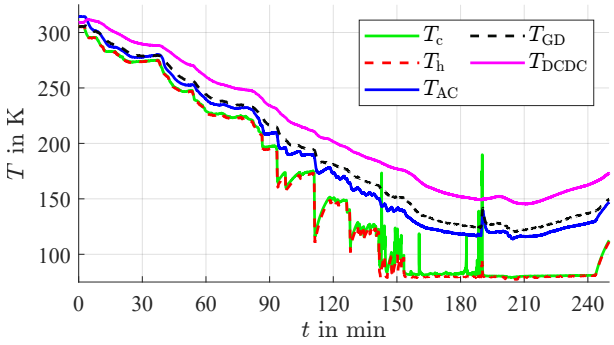
(b) On-resistance $R_{\text{DS,on}}$ at $t_{\text{pulse}} = 5\,\mu\text{s}$, $R_{\text{load}} = 7.5\,\Omega$

Fig. 11: On-resistance $R_{\text{DS,on}}$ measurements

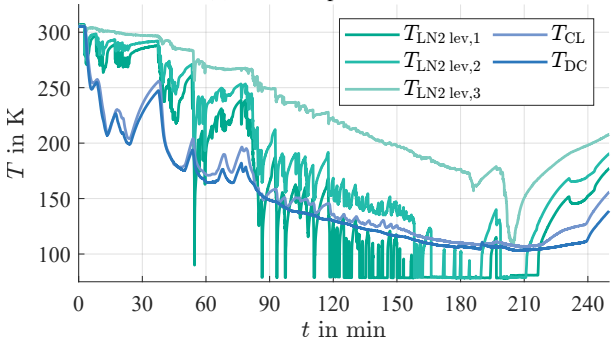
Compared to RT, a reduction in resistance by a factor of ≈ 5 can be achieved for a case temperature T_{c} of $\approx 82\,\text{K}$. Particularly at low voltages and $R_{\text{load}} = 15\,\Omega$, a large fluctuation in the measured values is observed. This can be explained by the low voltages $v_{\text{DS,on}}$ in the order of a few $10\,\text{mV}$ for these operation points.

C. Cryogenic Temperature Distribution

To monitor the temperature at various points of the CFB during a complete cryogenic measurement, the temperature sensors shown in Fig. 3 and Fig. 4 are used. Their results are depicted in Fig. 12.



(a) PCB temperatures



(b) Temperatures of the test bench

Fig. 12: Temperatures during the entire cryogenic experiment

Over the first $\approx 160\,\text{min}$ the $R_{\text{DS,on}}$ measurement is carried out. The plateaus with constant T_{c} are recognizable. Further, it is visible, that until $\approx 140\,\text{min}$ the temperatures of the cooling finger T_{h} and directly above the case T_{c} are almost identical. Afterwards, there are deviations for around $20\,\text{min}$, until they are almost identical again. It can be assumed that the proper thermal contact between the cooling finger and the transistor is no longer present at the beginning of this interval. This leads to a significantly increased thermal resistance which in turn limits the maximum coolable power dissipation of the transistor. During the time range from $\approx 180\,\text{min}$ to $\approx 195\,\text{min}$ measurements with continuous switching are conducted. From $t \approx 210\,\text{min}$, the system heats up again.

The sensors $T_{\text{LN2lev,1}}$, $T_{\text{LN2lev,2}}$ and $T_{\text{LN2lev,3}}$ are for monitoring the LN_2 level. Immersed in LN_2, they show $77\,\text{K}$, otherwise the value is significantly higher. Their measured values can be used to determine the evaporation rate during the warm-up process of the setup. The sensors are each $4\,\text{cm}$ apart

which corresponds to a volume of $\approx 120\,\mathrm{mL}$ enclosed by the sensors in this setup. When comparing $T_{\mathrm{LN2lev,1}}$ and $T_{\mathrm{LN2lev,2}}$ after $t = 210\,\mathrm{min}$, the time between $T_{\mathrm{LN2lev,1}}$ leaving $\mathrm{LN_2}$ and $T_{\mathrm{LN2lev,2}}$ leaving $\mathrm{LN_2}$ is determined to $\approx 5.5\,\mathrm{min}$, resulting in an evaporation rate $\dot{V}_{\mathrm{LN2}}$ of $\approx 0.36\,\mathrm{mL\,s^{-1}}$. With (4) this can be translated into a heat input of $\approx 58\,\mathrm{W}$ with the power electronics turned off. Note, that this is only a rough estimation for the heat input without any load. In the final setup, this heat input offset is expected to be much less, due to the convection prevented by the vacuum. In addition to the method described below with the power meter, the calorimetric approach described here using the evaporation rate of the $\mathrm{LN_2}$ can also be used to measure the efficiency.

D. Continuous Operation

In this section the continuous operation of the CFB at cryogenic temperatures is analyzed. The circuit operates in buck mode as shown in Fig. 13. A constant ohmic load R_{load} of $15\,\Omega$ and an open loop control with a switching frequency f_{sw} of $100\,\mathrm{kHz}$ and a duty cycle d of 0.5 are applied. The choke has an inductance L of $1\,\mathrm{mH}$.

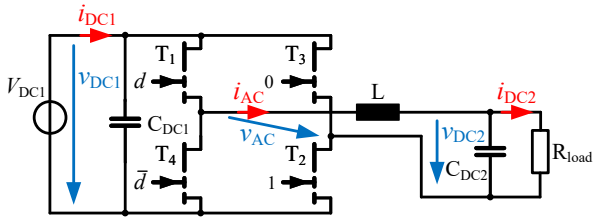


Fig. 13: Continuous operation of the CFB in buck mode

During operation the input voltage v_{DC1}, the input current i_{DC1}, the output voltage v_{DC2}, the output current i_{DC2} and the AC voltage v_{AC} and current i_{AC} are measured with a *DEWETRON DEWE3-PA8-RM* power meter. For current measurement, *Signaltec CT100* current transducers are used. The voltages are measured directly with *DEWETRON's TRION3 1810M-PA* module.

The continuous operation is performed after the $R_{\mathrm{DS,on}}$ measurement described in subsection V-B, when the CFB is cooled down to case temperature Tc of 82 K. The first measurement is performed for around 5 s with a DC link voltage V_{DC} of 40 V. Figure 14 shows the recorded traces for a time interval of 100 µs.

The efficiency calculated from the measured traces in this operation point $\eta_{\mathrm{meas,cryo}}$ is $\approx 97.65\,\%$. A *PLECS* simulation with the circuit parameters and the semiconductor model from *GaN Systems* with extrapolated losses for the cryogenic region gives for RT an efficiency $\eta_{\mathrm{sim,rt}}$ of $\approx 97.13\,\%$. For a case temperature Tc of 82 K an efficiency $\eta_{\mathrm{sim,cryo}}$ of $\approx 98.02\,\%$ is simulated. Therefore, the measured efficiency at cryogenic temperature is higher than the simulated efficiency at RT.

The efficiency values pointed out are quite low, due to the low DC link voltage V_{DC} of 40 V, which is only one-tenth of the rated voltage. Further, the limited accuracy of

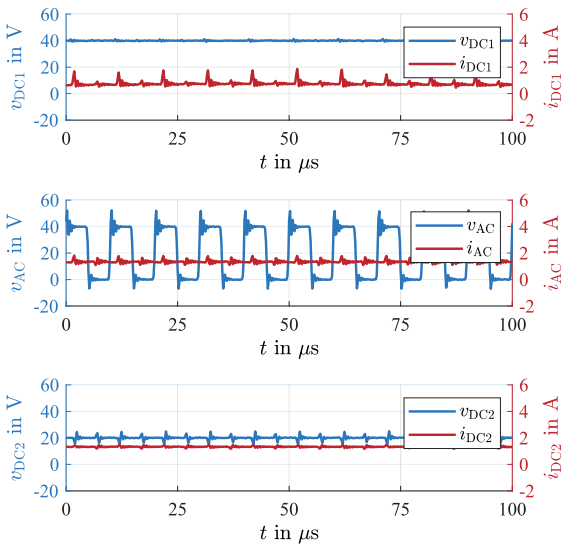


Fig. 14: Voltage and current traces for buck-mode continuous operation (cf. Fig. 13 for the current and voltage definitions)

the power meter, especially for low current and voltage values has to be considered. However, it is not possible with the current test bench to reach stable continuous operation for higher voltages, due to the loss of the proper thermal connection between the semiconductor and the cooling finger, as assumed in subsection V-C. This is investigated further in detail. Figure 15 therefore shows the zoomed time interval from Fig. 12a for the period of the continuous measurement. At $t \approx 35\,\mathrm{s}$, the measurement with the DC link voltage V_{DC} of 40 V is performed. When evaluating the case temperature T_{c}, an increase ΔT_{meas} of about 0.6 K during switching can be detected. Comparing this measured value with the simulated temperature increase ΔT_{sim} of only 20 mK, it can be assumed that the theoretically calculated thermal resistance $R_{\mathrm{th,TIM}}$ from section IV is significantly lower than the real effective resistance.

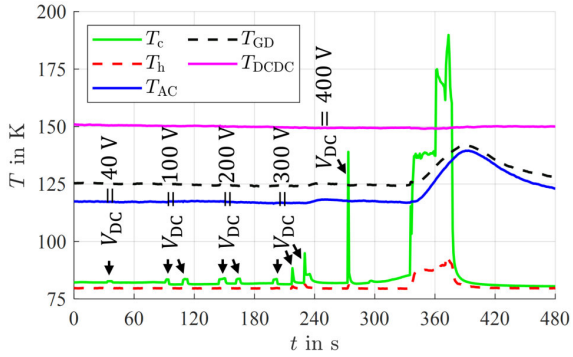


Fig. 15: Temperatures for buck-mode continuous operation

Further tests with higher DC voltages are shown in Fig. 15. A power limitation of the power supply unit was activated for these measurements, which limits the output power P_{DC1} to

100 W after a few milliseconds. The peaks in the case temperature T_c, visible from the 300 V measurements onwards, result from this limitation and the insufficient thermal connection of the semiconductors. With the 400 V measurement, the increased thermal resistance leads to a temperature increase in the case temperature T_c of more than 100 K which ultimately leads to the destruction of the semiconductor at around 335 s.

For that reason, in a future design care must be taken to a better thermal connection between the heatsink and the case of the transistor. This can be realized, for example, by increasing the contact pressure with spring screws. With those, the thermal contraction of the copper finger, which is around 250 µm in the current design, can be compensated.

VI. Summary and Outlook

This paper introduces a LN_2 cooled full bridge circuit, based on GaN-HEMTs for the use within a thermally insulating DAB, rated with $P_N = 20\,kW$, $V_{DC} = 400\,V$. The dimensioning and design of the power PCB and the whole cryogenic test bench are outlined. First measurements show a successful single pulse operation over the complete current-voltage-temperature operation range up to $V_{DC} = 400\,V$, $I_T \approx 50\,A$ and down to $T_c = 82\,K$. The on-resistance is reduced by a factor of five at $T_c = 82\,K$ compared to operation at RT. The cryogenic behavior of the gate driver and measurement circuit are described in detail. All circuits operate successfully over the whole temperature range. In addition, various temperature sensors allow the temperature distribution throughout the converter to be monitored. This information can be used e.g. to monitor the thermal connection of the semiconductors or to calculate the heat input into the system. The continuous operation of the circuit in buck mode at cryogenic temperatures was demonstrated for a DC link voltage of 40 V. An improved efficiency was measured for this operation point compared to operation at RT, which still has to be proven for higher DC link voltages and currents.

Therefore, future work includes appropriate improvements in the thermal connection of the semiconductors, which will allow continuous operation at rated power and rated voltage. To solve the problem of microcracks described in section IV, the fiberglass/copper combination will be replaced by all-metal heat sinks. This will allow the operation under a vacuum. Moreover, the development and construction of the thermally insulated transformer will be finished. Finally, the complete system, consisting of two back-to-back connected DABs, will be realized and characterized.

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