Lithium trapping induced memory effect of Gr/SiO_x blend anodes in lithium-ion batteries subjected to repeated partial cycling

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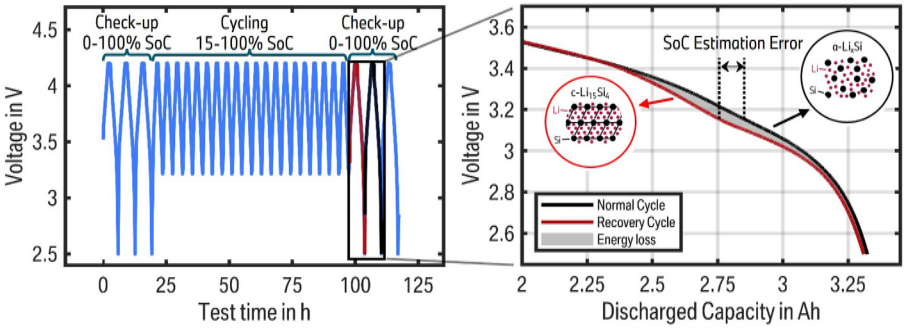
GRAPHICAL ABSTRACT



ABSTRACT

The use of silicon-based secondary anode materials in blend anodes alongside graphite is becoming increasingly prevalent in commercial lithium-ion batteries also used more and more in automotive applications. In addition to the accelerated degradation of silicon due to its significant volume expansion, the crystalline phase transition of fully lithiated silicon results in alterations to the voltage profile during discharging. This study examines the impact of this phase transition on the operation and state estimation of battery cells using such silicon-containing graphite/SiO_x blend anodes. A memory effect of trapping lithium in the crystalline phase occurs when the cell is subjected to partial cycling without being fully discharged. However, this effect can be cancelled out by a single deep discharge. To gain further insights, a variation in cycle numbers, state of charge range during cycling, charge and discharge current, and the operation temperature is conducted. In order to validate the findings, a variety of commercial and automotive cells and blend anode half-cells are analyzed.

Keywords:
Lithium-ion battery
Gr/SiOx blend anode
Memory effect
Lithium trapping
Capacity recovery

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1. Introduction

The market share of battery electric vehicles (BEVs) has exhibited a notable increase in recent years, with a substantial rise in the number of BEVs sold from 2.1 million in 2018 to 13.7 million in 2023 [1]. In order to extend the range of BEVs, new materials are investigated to enhance the energy density of lithium-ion batteries (LIBs). Among the active materials for the negative electrode, silicon (Si) is the most promising candidate, exhibiting a specific capacity of 3579 mAh/g at room temperature, which is about ten times higher than that of today's state-of-the-art material graphite (Gr) [2–4]. Moreover, silicon has a considerably low working potential, ranging from 0.2 to 0.6 V, which is essential for achieving a high energy density [5–7]. However, silicon experiences a significant volume expansion upon (de-)lithiation of ~280 % at full lithiation [8–10]. This results in the loss of active material and loss of lithium (Li) inventory, due to pulverization of Si-particles [7,11], particle cracking [4,12], loss of electrical contact [5,13], solid electrolyte interface (SEI) growth [14], and an overall unstable solid electrolyte interface [10,15,16]. The consequence of this degradation is a rather fast reduction of the available capacity, which counteracts the primary advantage of Si. A number of methods have been developed to avoid the adverse effects associated with volume expansion. Increasing the surface area to volume ratio by the implementation of nanoparticles reduces the strain during lithiation but results in a lower volumetric energy density [17]. Nevertheless, it has been demonstrated that such nanoparticles can withstand pulverization and cracking below a certain diameter [5,9,15].

The use of silicon oxide (SiO_x) or silicon embedded in a carbon matrix (SiC) instead of pure silicon particles presents an alternative with an intrinsically lower specific capacity, but with marked benefits in view of volume expansion [6,10,15,18]. The formation of Li-silicates and Li_2O as irreversible side products of SiO_x [19,20] results in an effective reversible specific capacity of ~1400 mAh/g [12,21,22]. To ensure longevity while still providing a capacity boost, commercially available cylindrical LIBs often employ a blend anode with SiO_x as a secondary active anode material in addition to graphite. This approach combines the high specific capacity of SiO_x with the high conductivity and structural stability of graphite which can further buffer the volume expansion of silicon [21,23–25].

The differences in the working potential between SiO_x and graphite in combination with the intrinsic hysteresis of SiO_x between lithiation and delithiation has an influence on the interplay between the two active materials. Cycling a LIB with a Gr/Si blend anode without fully charging or discharging the cell can result in disparate cell voltages at the same state of charge (SoC) due to the hysteresis of silicon [3,26]. In our previous research, we demonstrated that the SiO_x in Gr/SiO_x blend anodes undergoes preferential lithiation at increased C-rates at room temperature [27,28]. This leads to a different state of lithiation (SoL) of SiO_x and graphite at the same cell SoC, which remains even after prolonged relaxation periods due to the hysteresis of SiO_x [27]. Richter et al. [14] showed the inverse effect at extremely low temperatures of 20 °C in cells with Gr/Si anodes. However, the voltage discrepancies can occur even at a similar SoL for silicon. This phenomenon, which has been reported in numerous studies on silicon half-cells, typically occurs following the phase transition from fully lithiated amorphous (a) silicon to crystalline (c) $Li_{15}Si_4$ [2,11,13,17,29–39]. In general, silicon is in an amorphous state after formation while undergoing (de-)lithiation [34]. Two amorphous phase transitions occur during the lithiation process. Initially, fully delithiated a-Si forms a-Li_2Si [29,30] at a potential range of 250–200 mV vs. Li/Li^+ [29]. Upon further lithiation, the second phase transition to a-$Li_{3.5}Si$ occurs at approximately 100 mV vs. Li/Li^+ [29]. As the SoL is increased further, it is kinetically more preferable to rapidly [34,39] form the metastable [29,33] crystalline phase c-$Li_{3.75}Si$, often referred to as c-$Li_{15}Si_4$, rather than to increase the amount of Li in the amorphous state [17,29]. The formation of c-$Li_{15}Si_4$ is more likely to occur in regions with isolated silicon anions, which are created during lithiation by breaking the Si-Si bonds of larger silicon clusters with extended networks [29]. This crystalline phase transition occurs below a potential of 60 mV [33,38] to 50 mV vs. Li/Li^+ [2,29,31,32].

Ogata et al. [29,30] reported the formation of an overlithiated crystalline phase c-$Li_{3.75+\delta}Si$ with $\delta = 0.2–0.3$, which occurs when the SoL is increased further, to potentials below 50 mV vs. Li/Li^+. The formation of this c-$Li_{3.75+\delta}Si$ phase was found to be more favorable than the process of breaking additional Si-Si bonds to create the phase c-$Li_{3.75}Si$ from a-$Li_{3.5}Si$ [29]. In the absence of a crystalline phase during lithiation, the delithiation process shows the characteristic symmetrical hysteresis of silicon at its higher potential [30].

The reduction of a-$Li_{3.5}Si$ to a-Li_2Si occurs within the range of 270–310 mV vs. Li/Li^+ [29,36], followed by a return to fully delithiated a-Si at approximately 500 mV vs. Li/Li^+ [29,36]. However, the Li stored in a crystalline phase is delithiated at different potentials, creating an additional asymmetric voltage hysteresis [30,34]. The overlithiated crystalline phase is reduced back to c-$Li_{3.75}Si$ in the range of 50–150 mV vs. Li/Li^+ before any other Li is delithiated from silicon [29,30]. The transition back to an amorphous state, occurs at a significantly higher potential of around 440 mV vs. Li/Li^+ [2,11,29,35,36], which is at a higher level than the transition from a-$Li_{3.5}Si$ to a-Li_2Si. In addition, this decrystallization does not result in the amorphous phase a-$Li_{3.5}Si$ from which it was originally formed, but rather in a less lithiated phase. Two different phases are reported, namely a-Li_2Si [36,37] and a-$Li_{1.1}Si$ [29]. Caused by this effect, fully lithiated silicon exists at potentials as high as 440 mV vs. Li/Li^+, despite almost half of the Li is delithiated from amorphous Si. It is highly likely that this crystalline phase is formed in blend anodes containing graphite and silicon, given that the phase transition LiC_{12} to LiC_6 occurs at a potential plateau around 80 mV vs. Li/Li^+ [40,41]. Even minor polarization and concentration gradients can reduce the potential to a level below the threshold of 50–60 mV vs. Li/Li^+ for the formation of c-$Li_{3.75}Si$ [29,30]. For the same reason, c-$Li_{3.75}Si$ may also exist at potentials slightly above 440 mV vs. Li/Li^+ [11,35]. The crystalline phase was confirmed by several analytical methods. Specific peaks in the X-ray diffraction (XRD) spectrum are observable [32,37], dark spots in scanning electron microscopy (SEM) images indicate the existence of the crystalline phase [31] and the overlithiated phase c-$Li_{3.75+\delta}Si$ is detectable by nuclear magnetic resonance (NMR) [30].

The influence of the aforementioned characteristic on the potential of Gr/SiO_x anodes, combined with the intrinsic hysteresis of silicon [3,26,42], presents a significant challenge to the battery management system (BMS). A specific open-circuit voltage (OCV) does not directly correlate to a specific SoC for these blend anodes. Unlike laboratory battery test stands with a high accuracy in current measurements, the operation in BEVs does not allow coulomb counting to estimate the SoC, without a significant cumulative error over time [43–45].

The available online methods for estimating the SoC employ the OCV in two possible ways. The first is through direct comparison with a OCV lookup table after relaxation [43,44,46]. The second is as a foundation of model-based approaches that represent the entire electrochemical processes within the battery [43–46]. Beside the known dependencies of cell degradation and ambient temperature [43,45,47], the presence of a crystalline silicon phase can influence the OCV-SoC characteristic and, consequently, the SoC estimation. Similar to the SoC, the state of health (SoH) estimation is sensitive on OCV changes as it depends directly on OCV comparison after relaxation [48] or on OCV based peak comparison in incremental capacity analysis [46,49]. It is therefore necessary to track changes of the OCV over time to achieve an accurate SoC and SoH estimation, with the goal of improving the lifetime, safety, and performance of BEVs [43,44,49].

The memory effect was first observed for batteries in nickel cadmium (NiCd) and nickel metal hydride (NiMH) cells [50–54]. In such cells, repeated partial cycling results in a transient reduction in available capacity, which recovers following a slow, deep discharge [50,53]. In contrast, LIBs were long considered memoryless. However, Sasaki et al. [55] observed a memory effect in the cathode material $LiFePO_4$ (LFP),

whereby a single cycle in a lower SoC range resulted in changes to the voltage profile. The recovery of the available capacity after a substantial rest period was recently reported by Solchenbach et al. [56], resulting from an in-plane $LiPF_6$ gradient in cylindrical cells with Gr/Si anodes and a high excess of electrolyte. A memory effect for LIBs half-cells with pure silicon was also observed by Ulldemolins et al. [39] and Wen et al. [11], which is caused by the previously described crystalline phase transition. Similar observations were made for Gr/Si blend anode in half-cells [57]. To the best of our knowledge, this has not been investigated yet for SiO_x and on full cell level.

This study examines the induced memory effect of trapped Li in the crystalline phase of silicon for commercial and automotive LIBs with Gr/SiO_x anodes. The influence of the OCV and the resulting effect on the SoC estimation, the capacity retention and energy losses are presented. A series of parameter variations are conducted, including variations in the SoC range during cycling, the number of consecutive cycles, the C-rate during charging and discharging, and the temperature during operation. Moreover, the study includes measurements on anode half-cells with Gr/SiO_x blend anodes, providing additional insights.

2. Experimental

2.1. Commercial and automotive cells

To preclude the possibility that the results are attributable to a cell-specific effect, a total of five different commercial or automotive cell types are analyzed. These cell types vary in format, area of application, and manufacturer, and contain >5 wt% of SiO_x or a comparable amount of pure Si. However, from an operational standpoint, the capacity share between silicon and graphite is of particular interest. The pseudo OCV during discharging can be used to determine the capacity share of Si. We showed in our previous work that graphite is delithiated prior to silicon [28]. Given that graphite exhibits a distinct voltage profile with multiple phase transitions [58], it is possible to determine the SoC range at which graphite is mainly delithiated. This allows for an estimation of the capacity share of SiO_x and graphite. A detailed description of this calculation is presented in the Supplementary Materials section S1. The relevant cell parameters for each of the five cells are provided in Table 1, including the cell format, the nominal capacity, the operating voltage, the calculated silicon capacity share, and the gravimetric and volumetric energy density.

MoliCel M35A cells with a high energy density are used as the primary cell type in this work (Cell A), due to its high amount of SiO_x in the range of 10–14 wt%, determined by SEM with energy dispersive X-ray (EDX) analysis. This is in accordance with the high calculated silicon capacity share of 26.0 ± 0.5 %. Cell A is used for the majority of the parameter variation, while the other cell types are employed to show that the effect exists not only for one cell type. The MoliCel P45B (Cell B) is produced by the same manufacturer as Cell A. However, its design is more oriented towards providing high power than high energy, with a slightly lower amount of SiO_x. Cell C is manufactured by Murata/Sony and bears the identification US18650VTC6, with SiO_x as a secondary active anode material and the same cylindrical 18650 format as Cell A. To ensure that this effect is not exclusive to SiO_x but also exists in blend electrodes using pure silicon besides graphite, the SDI 30Q is used as Cell D. According to Bazlen et al. [59], this cell contains nano-Si in addition to graphite. The fifth cylindrical cell is a large-format automotive cell, further referred to as Cell E. This cell is produced at a BMW in-house prototype line, with the sole purpose of research and development. Full disclosure of all specific cell parameters is not possible, due to confidentiality reasons. Therefore, the results of Cell E are either presented as approximate values or by normalization.

2.2. Anode half cells

Additionally to cells A-E, a Gr/SiO_x blend electrode consisting of 7.6 wt% SiO_x (d50 ~5 µm) and 87.4 wt% graphite (~20 µm), is utilized for the anode half-cell study. The lithium predoped SiO_x secondary particle contains nano-sized Si, SiO_2, silicates and is coated with a thin carbon layer to improve its electrical conductivity. The electrode coating mixture of 1 wt% conductive carbon, 0.5 wt% carboxymethyl cellulose (CMC), and 3.5 wt% polyacrylate-based binder has a mass loading of ~10 mg/cm^2 and is pressed to a thickness of ~60 µm.

Prior to cell assembly, the electrodes are dried in a vacuum oven at 120 °C for at least 12 h. Two types of separators are employed in this work, namely a tri-layer PP/PE/PP separator (17 mm diameter, Celgard 2325, Celgard LLC, USA) and a glass fiber separator (16.5 mm diameter, 260 µm, GF/A Whatman, USA). Both separators are dried under vacuum in a glass oven (B-585, BÜCHI Labortechnik GmbH, Germany) for at least 12 h. The drying temperature for the tri-layer separator is 60 °C and for the glass fiber 300 °C. The cells are prepared in a dry room with a dew point < -50 °C. One piece of each type of separator is sandwiched between a lithium metal (300 µm thick, 16 mm in diameter) and Gr/SiO_x blend electrode disc (15 mm in diameter) in a CR2032 coin cell configuration. The tri-layer separator is facing to the SiO_x-graphite electrode. A commercially available electrolyte containing ethylene carbonate (EC), dimethyl carbonate (DMC), ethyl methyl carbonate (EMC) and fluoroethylene carbonate (FEC) is added in an amount of 100 µl.

The SiO_x-graphite//Li cells are allowed to rest at OCV after cell assembly to ensure sufficient wetting of the electrodes. Formation is performed galvanostatically with two consecutive full cycles at a rate of C/10 between 0.03 and 1.0 V vs. Li/Li$^+$. A constant voltage (CV) step is incorporated at the end of the electrode lithiation (i.e., 0.03 V vs. Li/Li$^+$) until the C-rate drops below C/50. The formation and subsequent half-cell measurement is performed isothermally at 25 °C using a battery test system (SL1130A, Keysight Technologies, United States) in a climatic chamber (customized model, Angelantoni Test Technologies, Italy).

2.3. Test procedure

All tests conducted in this study proceed with a consistent methodology. First, the available begin-of-test (BoT) capacity is determined through a capacity check-up. Subsequently, a specific number of cycles is conducted within the designated SoC range. The test is concluded with a second capacity check-up to determine the available end-of-test (EoT) capacity and to calculate the capacity retention, which is analogous to the state of health (SoH) of the cell.

The capacity check-up consists of three consecutive full cycles with a

Table 1
Specific parameters of the five cylindrical cells with a blend anode, used in this work. The share of the silicon capacity is calculated based on the pseudo OCV and the anode potential. The remaining parameters are derived from the specification provided by the cell manufacturers.

Cell	Format	Nom. Capacity	Operation voltage	Silicon capacity share	Gravimetric energy density	Volumetric energy density
A	18650	3.45 Ah	2.5–4.2 V	26.0 ± 0.5 % (SiO_x)	250 Wh kg^{-1}	700 Wh l^{-1}
B	21700	4.5 Ah	2.5–4.2 V	20.7 ± 0.5 % (SiO_x)	242 Wh kg^{-1}	643 Wh l^{-1}
C	18650	3.12 Ah	2.5–4.2 V	18.3 ± 0.5 % (SiO_x)	241 Wh kg^{-1}	631 Wh l^{-1}
D	18650	3 Ah	2.5–4.2 V	14.8 ± 0.5 % (nano-Si)	238 Wh kg^{-1}	646 Wh l^{-1}
E	4695	~30 Ah	2.8–4.2 V	15–20 % (SiO_x)	~300 Wh kg^{-1}	~800 Wh l^{-1}

constant-current constant-voltage (CCCV) charge step and a constant-current (CC) discharge step until the maximum or minimum cell voltage is reached, respectively. The CV phase of the charge step is terminated when the C-rate drops below C/50. Both the charge and discharge step use a C-rate of C/3. The available capacity, Q_{ref}, is determined during the final discharge step, as the preceding two cycles should be sufficient to eliminate all potential side effects that may affect the capacity of the cell.

During cycling, the upper or lower SoC deviate from 100 or 0 %, respectively. CCCV charging or discharging with a cutoff C-rate of C/10 is employed to set SoCs between 0 and 100 %. The voltage for each specific SoC is derived from the C/10 pseudo-OCV in the corresponding direction. It is essential to distinguish between charge and discharge OCV, as LIBs containing silicon have no unique OCV, due to the voltage hysteresis of silicon.

The test procedure of the reference case is conducted with the following parameters during cycling. Twenty cycles are performed between 15 and 100 % SoC at an ambient temperature of 25 °C, controlled by a climate chamber. A C-rate of C/2 is selected for charging and discharging, respectively. The lower SoC is set to approximately the center of the Si-range for cell A, as defined in section S1 in the Supplementary Materials.

The base test for cell A repeats this reference case five consecutive times, with a capacity check-up performed after each set of 20 cycles. In this way, all possible changes during the degradation process of the cell can be observed. Subsequently, each parameter is subjected to further variations to analyze its effect. This contains a variation in the number of cycles, a variation in the SoC range, a variation in the C-rate, and a variation in the temperature. The reference case is repeated for cells B to E, to eliminate the possibility of a specific effect, attributed to cell A. Furthermore, an additional lower SoC variation is conducted for cell E. The comprehensive test matrix is presented in Table 2.

The aforementioned anode half-cells are subjected to a similar test procedure. Fifteen consecutive cycles are conducted at 25 °C between different upper and lower cutoff potentials with a C-rate of C/10. The reduced C-rate compared to the reference case is required because coin cells typically exhibit an increased polarization compared to full cells. This is due to the overall configuration of the half cells, including the increased separator thickness. The upper cutoff potential is selected either at 400 mV vs. Li/Li$^+$, which is slightly below the potential of 440 mV vs. Li/Li$^+$ at which the crystalline phase is reverted to amorphous silicon [35,46], or at 270 mV vs. Li/Li$^+$, which is slightly above the potential at which graphite is active [40,60]. The lower cutoff voltage is set to either 60 mV vs. Li/Li$^+$ or 10 mV vs. Li/Li$^+$. According to the literature, at 10 mV vs. Li/Li$^+$ the crystalline phase transition of silicon is highly expected while at 60 mV vs. Li/Li$^+$ this transition should not have occurred yet [29,39]. The exact test specification is also described in Table 2.

Table 2
Overview of all conducted test scenarios, including the utilized cell, the number of cycles in between the check-ups, the employed SoC range during cycling, the C-Rate for charging and discharging, and the ambient temperature.

	Cell	# Cycles	SoC Range	C-Rate (Charge - Discharge)	Temperature
Reference case	Cell A	20	15–100 %	C/2 – C/2	25 °C
Base test/Aging	Cell A	5x 20	15–100 %	C/2 – C/2	25 °C
Number of cycles	Cell A	5	15–100 %	C/2 – C/2	25 °C
		50	15–100 %	C/2 – C/2	25 °C
		100	15–100 %	C/2 – C/2	25 °C
		200	15–100 %	C/2 – C/2	25 °C
SoC variation	Cell A	20	0–100 %	C/2 – C/2	25 °C
		20	5–100 %	C/2 – C/2	25 °C
		20	10–100 %	C/2 – C/2	25 °C
		20	20–100 %	C/2 – C/2	25 °C
		20	25–100 %	C/2 – C/2	25 °C
		20	30–100 %	C/2 – C/2	25 °C
		20	50–100 %	C/2 – C/2	25 °C
		20	70–100 %	C/2 – C/2	25 °C
		20	15–80 %	C/2 – C/2	25 °C
		20	15–60 %	C/2 – C/2	25 °C
		20	15–40 %	C/2 – C/2	25 °C
		20	30–70 %	C/2 – C/2	25 °C
C-rate variation	Cell A	10	15–100 %	C/10 – C/10	25 °C
		20	15–100 %	C/5 – C/5	25 °C
		20	15–100 %	1C–1C	25 °C
		20	15–100 %	2C–2C	25 °C
Temperature variation	Cell A	20	15–100 %	C/2 – C/2	10 °C
		20	15–100 %	C/2 – C/2	40 °C
Cell variation	Cell B	20	15–100 %	C/2 – C/2	25 °C
	Cell C	20	15–100 %	C/2 – C/2	25 °C
	Cell D	20	15–100 %	C/2 – C/2	25 °C
Cell-variation + SoC variation	Cell E	20	5–100 %	C/2 – C/2	25 °C
		20	10–100 %	C/2 – C/2	25 °C
		20	15–100 %	C/2 – C/2	25 °C
		20	20–100 %	C/2 – C/2	25 °C
		20	30–100 %	C/2 – C/2	25 °C
		20	40–100 %	C/2 – C/2	25 °C
		20	50–100 %	C/2 – C/2	25 °C
Anode half cell	7.6 wt% SiO_x	15	10–400 mV vs. Li/Li$^+$	C/10 – C/10	25 °C
		15	10–270 mV vs. Li/Li$^+$	C/10 – C/10	25 °C
		15	60–270 mV vs. Li/Li$^+$	C/10 – C/10	25 °C

3. Results and discussion

3.1. Influence of lithium trapping on the cell behavior

The memory effect of LIBs containing silicon as a secondary active anode material is evident when examining the discharge capacity during cycling. Fig. 1 illustrates the discharge capacity for each of the five sets of 20 cycles between 15 and 100 % SoC, in comparison to the discharge capacity of the third check-up cycles. The latter is employed to determine the available capacity Q_{ref}. While the discharge capacities of the check-ups demonstrate a nearly linear decline (R^2 = 98.4 %), it is evident that the capacity of the partial cycles (15–100 % SoC) exhibits an accelerated decrease but subsequently recovers a majority of the capacity loss during the check-ups. The actual loss of capacity between the check-ups can be attributed to the general degradation processes inherent in LIBs. Given the significant volume expansion that SiOx undergoes upon lithiation, the most likely processes are additional SEI growth and loss of active material due to particle cracking [15,16]. As the temperature and C-rate of the check-ups and cycling are identical or comparable, it can be assumed that the complete discharge during the check-up has a sort of recovery effect on the battery, thereby reversing the significant capacity loss observed during cycling. This behavior of the discharged capacity is comparable to the results observed in pure silicon half-cells [11,39].

This impression solidifies upon closer examination of the voltage behavior during discharging. The greater deviation is evident between the initial and final 15–100 % SoC cycles and between the first and the second full cycles of the check-up after cycling at the EoT condition. Fig. 2 shows the four aforementioned voltage profiles, in addition to the last full discharge step of the BoT check-up. All profiles are displayed over the discharged capacity during each individual cycle. As previously stated, graphite is predominantly delithiated at higher SoCs and SiO_x at lower SoCs [28], here indicated as Gr-range and Si-range, respectively.

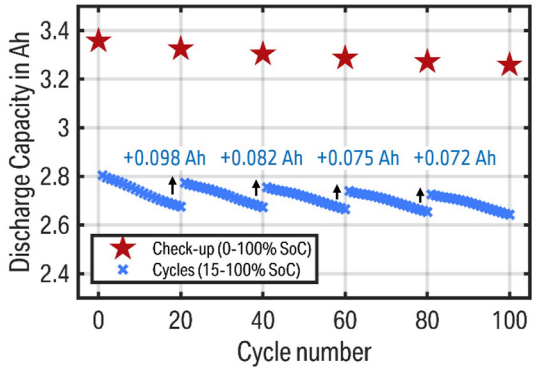

Fig. 1. Discharged capacity vs. cycle number in the base test with five sets of 20 cycles between 15 and 100 % SoC each and a check-up between each of the five sets. The discharged capacity of the third check-up cycle is indicated in red and represents the reference capacity of the cell at this specific point in time, which is used to calculate the SoH of a battery. The discharged capacity of all 100 cycles in blue illustrates the memory effect, exhibiting a rapid increase after each check-up before displaying a large decrease. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

In the Gr-range, neither the cycles nor the check-up exhibit any deviation. However, a reduction in voltage is observable in the Si-range with increasing cycle count. Therefore, this section is presented in more detail as a zoom plot in Fig. 2. The lower SoC of 15 % is set by a constant voltage phase at the corresponding voltage, resulting in a diminished discharge capacity for the last cycle. Similar voltage changes are present in the first cycle of the EoT check-up, which will henceforth be referred to as the recovery cycle. The voltage profile shows a decrease at the start of the Si-range, when being compared to the second cycle of the EoT check-up, further referred to as the normal cycle, or the BoT check-up. However, the steep decrease of the voltage reverses at approximately 3.1 V, reaching a near-plateau state, until it converges towards the profile of the normal cycle. Upon reaching a voltage below 2.9 V, only a minor deviation is observable between the recovery and normal cycle.

The described behavior presents a multifaceted influence on the battery operation. As previously stated, the first effect is a reduced cyclical capacity retention compared to the actual capacity retention ascertained during the check-ups. Secondly, a reduction in the voltage within the Si-range results in an error in the SoC estimation, when the SoC estimation is based solely on the cell voltage. As the same voltage is reached at a lower discharge capacity, the estimation results also in a lower value, given that high precision coulometry is only available for test stands. This is particularly crucial in BEVs, where reliable range estimation is a necessity. In the presented case, the remaining driving range will decline at a significantly accelerated rate during the first half of the Si-range and on the contrary will decline at a lower rate than the actual driving distance during the latter half. A third negative consequence is a minor energy loss between the recovery and normal cycle. This energy loss consists of two parts. Firstly, the lower voltage within the Si-range results in a decline in the energy. Secondly, the slightly reduced capacity of the recovery cycle compared to the normal cycle further reduces the discharged energy. Given the absence of a discernible distinction between the second and the third cycle of the EoT check-up, it can be reasonably inferred that this second energy loss can also be attributed to the partial cycling. It is either a secondary effect of the presented memory effect or might be explained by the diffusion of Li-ions into the anode overhang, which are only delithiated during consecutive discharge steps [61–63].

In general, batteries undergo an aging process upon repeated cycling [64,65]. Therefore, it is necessary to determine not only the capacity retention of the cycles between 15 and 100 % SoC, but also the capacity retention between the BoT and EoT check-up. It is essential to consider the overall degradation when evaluating the cyclical capacity retention, as this mitigates the severity to a certain extent. As previously stated, the third discharge cycle of the check-up is used for this determination. The capacity retention $rQ_{\text{Check–up}}$ describes the relation between Q_{ref} at EoT condition and Q_{ref} at BoT condition.

$$rQ_{\text{Check–up}} = \frac{Q_{\text{ref,EoT}}}{Q_{\text{ref,BoT}}} \tag{1}$$

A comparable calculation can be performed to determine the capacity retention during cycling rQ_{Cycling}, by comparing the discharged capacity of the first with the last partial cycle:

$$rQ_{\text{Cycling}} = \frac{Q_{\text{cycle,first}}}{Q_{\text{cycle,last}}} \tag{2}$$

$Q_{\text{cycle,first}}$ describes the discharge capacity of the first cycle, here between 15 and 100 % SoC and $Q_{\text{cycle,last}}$ describes the discharge capacity of the last, which is in this case the 20th, cycle. The maximum SoC error is described as:

$$SoC_{\text{Error,max}} = \frac{\max\limits_{x}\left(Q_{\text{EoT,normal}}(U=x) \quad Q_{\text{EoT,recovery}}(U=x)\right)}{Q_{\text{ref,EoT}}}, \tag{3}$$

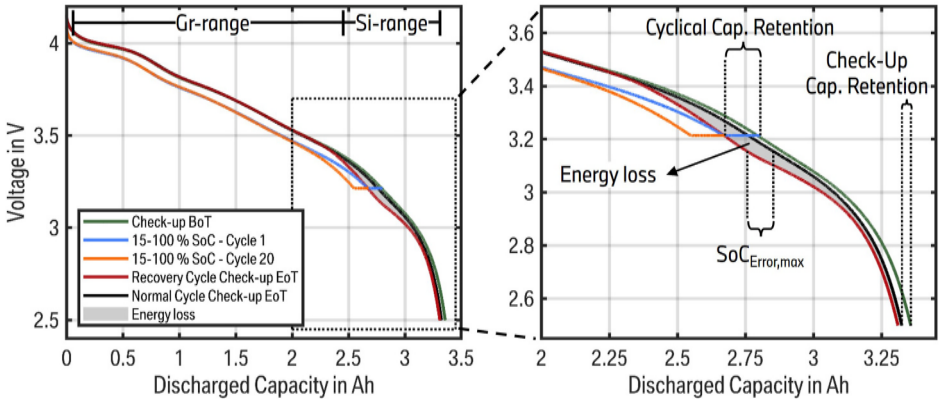

Fig. 2. Discharge voltage profile of all relevant cycles, influenced by the memory effect and displaying the recovery. A more detailed view is provided in a zoom plot on the right, in the range above 2 Ah, where notable deviations in voltage profiles are observed. The following cycles are presented in chronological order: Last cycle of the BoT Check-Up (grey), initial 15–100 % SoC cycle (blue), final 15–100 % SoC cycles (orange), first EoT check-up or recovery cycle (red), and second EoT check-up or normal cycle (red). Furthermore, the metrics used to assess the severity of the memory effect are visualized, including the check-up and cyclical capacity retention, the maximum SoC error, and the energy loss (red area). (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

where $Q_{EoT,normal}(U = x)$ describes the discharge capacity when the voltage U is equal to x during the normal cycle of the EoT check-up. Similarly, $Q_{EoT,recovery}(U = x)$ describes the discharge capacity of the recovery cycle of the EoT check-up. In the presented case in Fig. 2, the $SoC_{Error,max}$ is equal to 2.55 % at a voltage of 3.15 V. The energy loss E_{loss} of the recovery cycle in relation to the normal cycle is defined by the subtraction of the respective energies:

$$E_{loss} = E_{normal} \quad E_{recovery} \tag{4}$$

$$E = \int_{t_{start}}^{t_{end}} U \cdot |I| \, dt \tag{5}$$

Eq. (5) is used to calculate E_{normal} and $E_{recovery}$ in Eq. (4). The integral is calculated from start to end of the respective discharge step. Absolut value of the current I is necessary, as the current is usually defined negative during discharging. In Fig. 2 the energy loss accounts for 0.6 %, or 73 mWh. All the metrics described for quantifying the memory effect are also indicated in the zoom plot in Fig. 2.

3.2. Crystalline silicon phase transition

The memory effect can be explained by reference to the previously mentioned phase transition of silicon from amorphous to crystalline that occurs when reaching a state of full lithiation. To confirm that the origin is indeed the phase transition, a test scenario with a pure graphite anode similar to the base test is analyzed, which does not indicate the presence of a memory effect. The voltage profiles of the recovery and normal cycle are displayed in Fig. S2 in the Supplementary Materials. To the best of our knowledge, a memory effect attributed to pure graphite anodes has also never been reported in the literature. Moreover, a change in the OCV is responsible for the changes in the voltage profile during the recovery cycle, which is confirmed by repeating the reference case with a relaxation interval every 2 % SoC.

While the phase transition was investigated in detail for pure silicon anode half-cells [11,29,39], the consequences for a full cell with a blend anode have not been examined yet. The phase transition from a-$Li_{3.5}Si$ to c-$Li_{3.75}Si$ occurs at an anode potential below 60 mV vs. Li/Li^+ [11,29,33]. In a blend anode in a full cell, this potential is typically not reached for the open circuit potential (OCP), as an SoC of 100 % is typically located before reaching fully lithiated graphite [30]. Consequently, the charging process terminates during the last graphite plateau of the phase transition from LiC_{12} to fully lithiated LiC_6 with an OCP of ~80 mV vs. Li/Li^+ [40,41]. However, with only a small polarization, the actual potential is likely to fall below the threshold of 60 mV vs. Li/Li^+, which permits for the phase transition of silicon to its crystalline form [30]. Fig. 3 shows the pseudo OCP during C/20 (de-)lithiation of harvested electrodes from cell A. Even at this C-rate of C/20, the potential falls slightly below 60 mV vs. Li/Li^+ at a fully cell SoC of 100 %. This is determined through the fitting of harvested electrode potentials to a C/20 pseudo OCV of cell A. Discharging the cell to 15 % SoC has to terminate at a potential below 440 mV vs. Li/Li^+, otherwise the crystalline phase will be reverted back to a-$Li_{1.1}Si$ during each cycle [29] and no memory effect would occur. This is demonstrated in Fig. 3 for cell A, where the potential at 15 % full cell SoC is indeed slightly below the threshold. Given that the SoC is set using a CV phase until a cutoff C-rate of C/10, it is reasonable to conclude that the anode potential remains largely below the threshold. Therefore, with each cycle, more Li is trapped in the crystalline phase of Si, which is not converted back to the amorphous phase. However, even a slightly lower SoC might recover the trapped Li during each cycle for cell A.

It is important to note that the anode potential in half-cells is not identical to that in full cells. The reason is that the anode/cathode interaction and the voltage range are different in both cell types. Accordingly, the full cell SoC illustrated in Fig. 3 is merely an approximation.

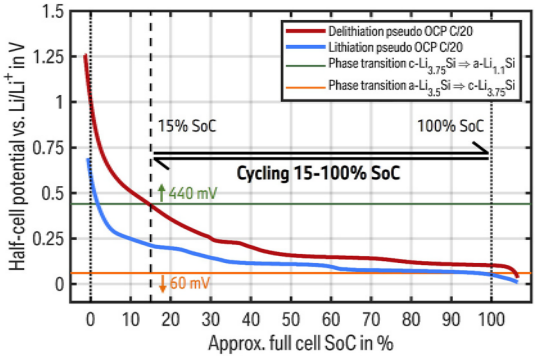

Fig. 3. Lithiation (blue) and delithiation (red) anode potential vs. Li/Li+ of harvested electrodes from cell A. The effective full cell SoC for both 0 and 100 % is indicated with dotted lines. The full cell SoC of 15 % is indicated with a dashed line, visualizing the potential range during the partial cycling in the reference case. The anode potential for the phase transition from a-$Li_{3.5}Si$ to c-$Li_{3.75}Si$ below 60 mV is indicated in orange, while the reverse transition from c-$Li_{3.75}Si$ to a-$Li_{1.1}Si$ above 440 mV is represented in green. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

During the first full discharge, which is in this test scenario the recovery cycle of the EoT check-up, the anode potential rises above 440 mV vs. Li/Li^+, resulting in the back transformation to the amorphous silicon phase. This typically results in a plateau at 440 mV vs. Li/Li^+ until the phase transformation is completed [11,35]. This plateau can also be observed at full cell level in Fig. 2 in the range of 2.75–3 Ah of discharged capacity. The comparatively small voltage decrease instead of an exact plateau within this range can be attributed to the decreasing cathode potential. The observed memory effect can thus be fully explained by the phase transition of silicon from crystalline to amorphous.

This is a comparable reason to the cause of the memory effect for NiCd and NiMH cells, which can be explained by the formation of the γ-NiOOH phase [50,52,54] or the amorphous phase HNi_2O_3 [53]. Both phases are reversed upon deep discharge, similar to the c-$Li_{3.75}Si$ phase. On the contrary, the origin of the memory effect in LFP cells can be attributed to the two-phase equilibrium potential of LFP, which results in the voltage deviations [55].

3.3. Parameter variation on full cell level

In order to investigate the impact of the memory effect on the operation of batteries, particularly in the context of BEVs, a parameter variation is presented in the following section. The impact on the operation is determined by evaluating the changes in capacity retention, maximum SoC error, and energy loss, as described in Eqs. (1)–(5), in comparison to the reference case. The parameter variation includes alterations in the impact over aging, the number of cycles prior to recovery, the SoC range during cycling, the used C-rate, and the ambient temperature.

3.3.1. Memory effect upon aging

During the base test, the reference case is repeated five times with a check-up conducted between each set of cycling. This permits an analysis of the extend of Li trapping throughout cell degradation. Fig. 4a–c illustrate the three defined metrics to measure Li trapping. Fig. 4a shows the capacity retention in percent for the check-ups and the cycles of all five sections, according to Eq. (1) and Eq. (2), respectively. The capacity retention of the check-up is included in the figure since it is important to evaluate the cyclical capacity retention correctly. A reduction in the capacity retention during the check-ups indicates a degradation of the cell. Accordingly, the difference between the cyclical and check-up capacity retention is relevant when evaluating Li trapping. Fig. 4b

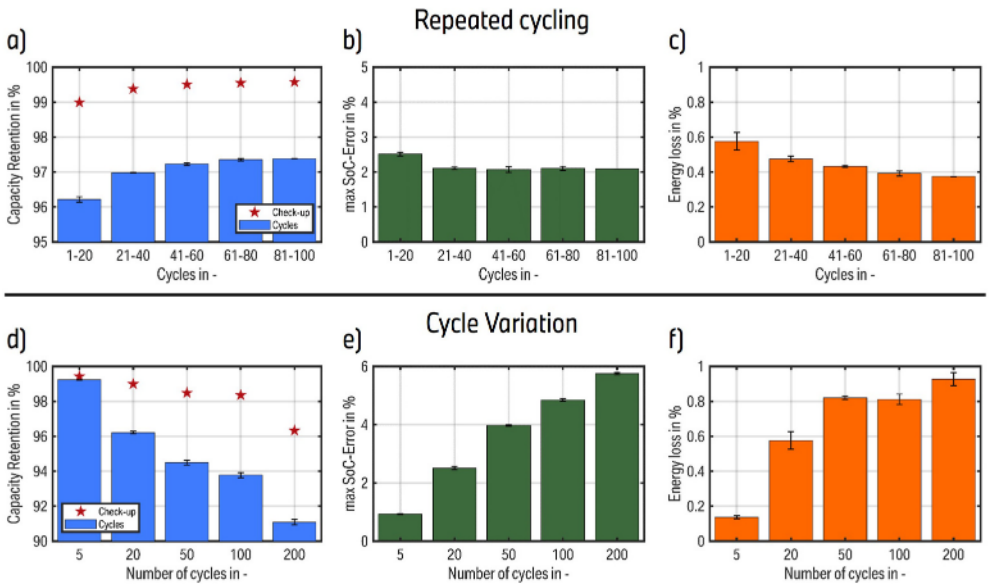

Fig. 4. Illustration of the metrics for quantifying Li trapping for the five sets of the reference case in the base test (a–c), as well as the variation in the number of cycles (d–f). (a) Capacity retention for the check-ups and the specific cycles in between the check-ups for each set of 20 cycles. (b) Maximum SoC-error between the recovery and normal cycle for each set of 20 cycles. (c) Energy loss of the recovery cycle, compared to the normal cycle, for each set of 20 cycles. (d) Capacity retention for the check-ups and the specific cycles in between the check-ups for each number of cycles in the cycle variation. (e) Maximum SoC-error between the recovery and normal cycle for each number of cycles in the cycle variation. (f) Energy loss of the recovery cycle, compared to the normal cycle, for each number of cycles in the cycle variation.

illustrates the maximum SoC error, as defined in Eq. (3), while Fig. 4c depicts the energy loss between the recovery and normal cycle during the EoT check-up according to Eq. (4). Similar plots to those presented in Fig. 4a–c are presented in subsequent sections for the remaining parameter variations.

The results of the repeated cycling demonstrate that aging has only a minor impact on the memory effect. A trend emerges, indicating that Li trapping has a progressively diminished impact with increasing lifetime. This trend is particularly evident between the first and the second set of 20 cycles. The first set exhibits the least capacity retention, the largest maximum SoC error, and the largest energy loss. Especially the maximum SoC error remains largely unchanged for the remaining sets, while the other metrics improve and appear to be converging with increasing set number. A comparable trend towards a reduction in the recovered capacity with increased aging is also evident in Fig. 1.

It can be inferred that there is a slight correlation between an improvement in the memory effect and increased aging, with the largest sensitivity observed during the initial cycles. It is unclear whether the number of cycles or the number of phase transitions from crystalline to amorphous during the recovery cycles is responsible for this effect. Similar results were also reported on pure silicon half-cell level, with a reduced memory effect with increased total cycle count [2,30,35].

3.3.2. *Variation in the number of cycles*

In this section, the number of repeated cycles before recovery is modified. All remaining test parameters are consistent with those of the reference case. The number of cycles varies from 5 to 200 cycles, as listed in Table 2. The results of the three metrics for this variation are visualized in Fig. 4d–f in a manner identical to that employed for the aging case in Fig. 4a–c. A clear dependency exists between the extend of Li trapping with the number of cycles. With increasing cycle number, all metrics indicate an increase in the amount of trapped Li. However, the amount of trapped Li appears to reach a maximum with increasing cycle count. The difference between capacity retention and check-up is approximately 4 % for the case 50, 100 and 200, with the energy loss exhibiting a slight increase. The SoC error is also not increasing in a linear fashion, with an additional error of 1 % for the case 200 cycles over the error of approximately 5 % during the initial 100 cycles. With a difference of 5 % between the capacity retention of the check-ups and the cycles and a maximum SoC error of approximately 6 % in the 200-cycle case, this cell appears to reach saturation between 5 and 6 % of trapped Li. The saturation is contingent upon the silicon capacity share, and thus will vary for cells with disparate silicon contents. Given a silicon capacity share of 25.5 % and a Si-range of 29.9 %, it can be assumed that approximately half of the silicon transitions to the crystalline phase, given that some of the remaining graphite will also be delithiated until 15 % SoC. Further details are presented in section S1 in the Supplementary Materials.

In summary, the impact of the memory effect increases with the number of cycles between the check-ups until reaching a saturation, which depends on the silicon content.

3.3.3. *Cell variation*

To ensure that the memory effect is not cell-specific for cell A, but rather a general occurrence of silicon in blend anodes, the reference case is repeated for all five cells listed in Table 1. Fig. 5 compares the resulting capacity retention, the maximum SoC error, and the energy loss. The maximum SoC error in Fig. 5b demonstrates that the memory effect occurs irrespective of the cell format, design, and silicon material. With the exception of cell C, the difference between the check-up and cyclical capacity retention in Fig. 5a is comparable for all remaining cells. The voltage profiles of cells B to E are presented in Fig. S3 of the Supplementary Materials. A comparable voltage deviation is observable during the recovery cycle, which indicates the presence of Li trapping. This suggests that the memory effect occurs in a similar manner in nano-Si as in SiO_x and independent of the cell format.

Cell C shows a significantly lower difference between the capacity retention of the check-up and cycles, yet also displays a strong cell degradation of ~2.5 % within the 20 cycles. Given that the crystalline phase transition is also associated with an increased cell degradation, it may be inferred that Cell C is less resistant to aging mechanisms as the remaining cells. As previously stated in Section 3.3.1, the memory effect is less pronounced in the presence of increased degradation, which also explains the reduced difference in the capacity retention. The largest

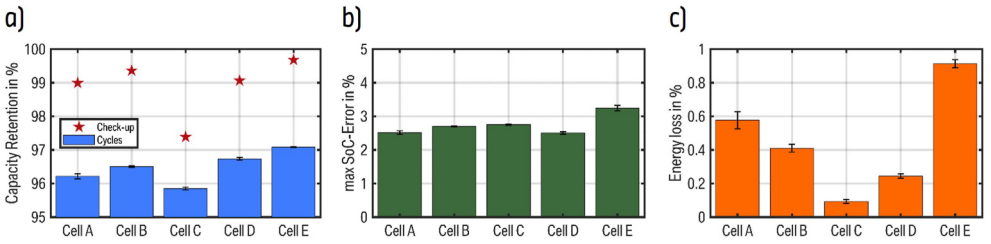

Fig. 5. Illustration of the metrics for quantifying Li trapping for the reference case of all cell types. (a) Capacity retention for the check-ups and the specific cycles in between the check-ups for each cell type. (b) Maximum SoC-error between the recovery and normal cycle for each cell type. (c) Energy loss of the recovery cycle, compared to the normal cycle, for each cell type.

deviation between the cells is observable in Fig. 5c for the energy loss. This can be primarily attributed to the discrepancy between the discharged capacity of the recovery and normal cycle. As aforementioned, the recovery cycle typically exhibits a slightly reduced discharged capacity than the normal cycle. The reason for this additional capacity regain between the recovery and normal cycle is yet to be elucidated and will be the subject to further investigation. The elevated cutoff voltage for Cell E is responsible for the observed increase in energy loss, as the recovery cycle is not yet fully completed. Moreover, the lower energy loss of cells C and D can be attributed to their discharge capacity, as evidenced by the recovery cycle exhibiting values closer to those of the normal cycle. The pronounced degradation of cell C, in particular, results in a discernible decline between the recovery and normal cycle in the EoT check-up. This further diminishes the energy loss, as the memory effect and the degradation cancel each other out.

3.3.4. SoC variation

Fig. 6 displays the three metrics for a variation in the SoC range during cycling for cells A and E, as listed in Table 2. The results demonstrate a pronounced dependence of this parameter. The most significant memory effect for cell A occurs at a lower SoC between 15 and 25 %, with an upper SoC of 100 %. All metrics show Li trapping in the cases 30–100 %, 15–80 %, and 30–70 %, however, to a lesser extent. For the remaining SoC ranges, little to no Li trapping is apparent in the displayed metrics in Fig. 6a–c, nor in an analysis of the voltage profiles.

The SoC variation for cell E exhibits a similar behavior, illustrated in Fig. 6d–f, with a shift towards lower SoCs of 10–20 % for the most severe cases. This can be attributed to the lower amount of silicon in the blend anode.

At a lower SoC of 10 % or less, no discernible indication of Li trapping is observable. Nevertheless, a small increase of the lower SoC to ~15 % results in a considerable amount of Li trapping. Fig. 3 shows that the anode potential at a full cell SoC of 15 % is only slightly below the threshold of 440 mV vs. Li/Li^+ at which the crystalline phase c-$Li_{3.75}Si$ reverses to amorphous a-Li_xSi phase [11,29,35,36]. Consequently, the anode potential rises above 440 mV vs. Li/Li^+ at a full cell SoC below ~15 %, thereby recovering the trapped Li during each cycle and no difference is observable in the EoT check-up. There still exists a small amount of trapped Li for each cycle when the SoC reaches 100 %. However, this quantity exists in any full cycle and is therefore undetectable through voltage analysis. The same relation applies to the case 5–100 % SoC for cell E. Due to the lower amount of Si, the anode potential of 440 mV vs. Li/Li^+ is not reached in the case of 10–100 % SoC, resulting in a significant amount of trapped Li for this cell.

Increasing the lower SoC above 30 % for cell A, or above 20 % for cell E, results in a reduction of the memory effect, compared to the aforementioned SoC ranges that exhibit a pronounced memory effect. Since the upper SoC is maintained at 100 % and therefore an anode potential drop below 50 mV vs. Li/Li^+, it is reasonable to anticipate the occurrence of Li trapping. However, compared to the reference case, silicon is

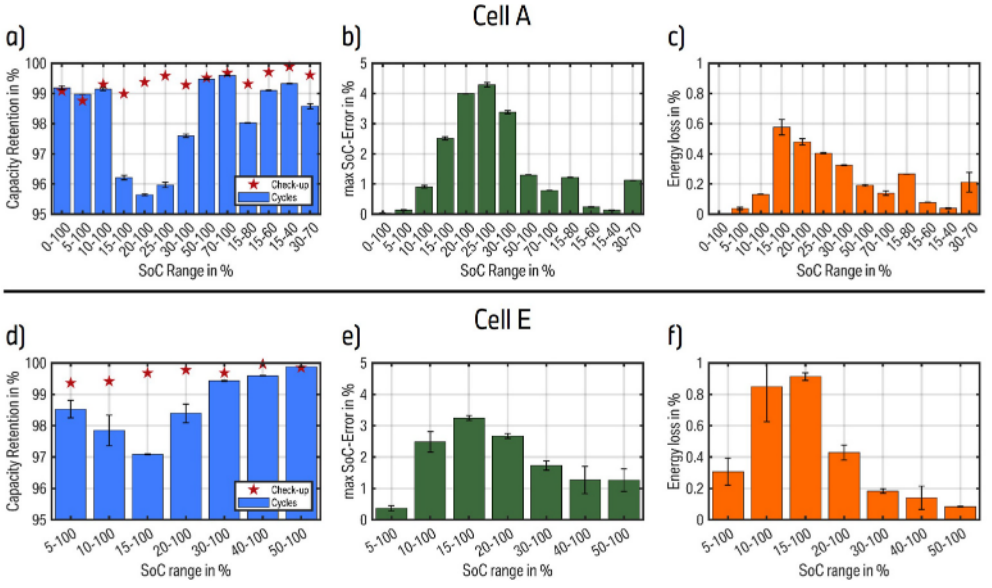

Fig. 6. Illustration of the metrics for quantifying Li trapping for the variation in the SoC range during cycling for Cell A (a–c) and cell E (d–f). (a) Capacity retention for the check-ups and the specific cycles in between the check-ups for each SoC range of cell A. (b) Maximum SoC-error between the recovery and normal cycle for each SoC range of cell A. (c) Energy loss of the recovery cycle, compared to the normal cycle, for each SoC range of cell A. (d) Capacity retention for the check-ups and the specific cycles in between the check-ups for each SoC range of cell E. (e) Maximum SoC-error between the recovery and normal cycle for each SoC range of cell E. (f) Energy loss of the recovery cycle, compared to the normal cycle, for each SoC range of cell E.

mostly not active during the cycling for these SoC ranges. As evidenced by the analysis of the pseudo OCV of cell A, only graphite is active during discharging to 30 % SoC. Therefore, silicon remains almost fully lithiated even at the higher rate of C/2 at a SoC higher than 30 %. This suggests that the silicon needs to be active to exhibit trapped Li. The certain reason for this relation cannot be given at this point and will be further investigated. One potential explanation is the breakage of Si-Si bonds in large silicon clusters to create isolated silicon anions. Ogata et al. [30] state that the formation of c-$Li_{3.75}Si$ is kinetically enhanced if isolated silicon anions exist. During lithiation, the larger Si-Si clusters are broken down into smaller clusters, which ultimately result in the formation of isolated silicon anions. In the case of a blend electrode, where silicon is not active above ~30 % SoC, these clusters are unable to be further broken down into smaller clusters, which hinders the transition to the crystalline phase. This also provides an explanation for the increase in the amount of trapped Li with each cycle in the critical scenarios, as an increased proportion of isolated anions is expected when the silicon is active.

The impact of varying the upper SoC on the memory effect is examined for cell A and displayed in Fig. 6a–c. At upper SoCs below 100 %, the effect initially decreases and then becomes nearly undetectable. At upper SoCs of 70 and 80 %, the three metrics show a discernible but reduced amount of trapped Li in comparison to the 100 % case with the same lower SoC. However, at upper SoCs below 70 %, the impact of the effect reduces to a similar degree as in the cases with lower SoCs below 15 %. This indicates that no memory effect exists. Given that the crystalline phase forms below an anode potential of 50 mV vs. Li/Li^+ [2,31,32], even with the polarization at a C-rate of C/2, the OCP needs to be near this value. For blend anodes containing silicon and graphite, the OCP reaches this threshold, even at SoCs below 100 %. This is attributed to the large voltage plateau of the graphite phase transition from LiC_{12} to LiC_6 at a potential of ~0.08 V at high lithiation [7]. Fig. 3 illustrates this plateau for cell A at a full cell SoC above 65 %. Therefore, when the charge step progresses to an SoC which is within this plateau, the anode potential with polarization drops below the threshold of 50 mV vs. Li/Li^+ to from crystalline Si. A charge step that terminates prior to this plateau, the anode potential does not decrease consistently below the threshold, resulting in the absence of Li trapping due to a lack of formation of the crystalline phase.

In summary, a critical SoC range for the upper and lower SoC exists, within which a pronounced memory effect occurs. The lower SoC must be sufficiently high to ensure that the anode potential remains below ~440 mV vs. Li/Li^+, while also being sufficiently low for silicon to be actively (de-)lithiated during each cycle. The upper SoC should be sufficiently high to terminate the charge process within the last graphite plateau. However, an increase in the upper SoC results in a more pronounced memory effect. Additionally, this critical SoC range depends on the silicon share of the blend anode.

3.3.5. *C-rate variation*

The variation of the C-rate, ranging from a low rate of C/10 to a high rate of 2C, demonstrates that there is nearly no rate dependency with regards to Li trapping. Fig. 7a–c shows the three metrics, which display no large deviation except in the case of a C-rate of C/10. However, this outlier, indicating a lower impact of Li trapping at this low rate, may be misleading due to the fact that only half the number of cycles are performed for this rate, due to limitations in the test duration. Projecting the 10 cycles of the C/10 case to the standard of 20 cycles would result in comparable values for all metrics to the remaining C-rates. This reinforces the strong dependency of the number of cycles. Since cell A is designed with a high energy density rather than providing a high power, the cells show increased degradation at higher rates, visible in Fig. 7a. This is most likely attributed to the deposition of metallic Li during charging, which occurs at anode potentials below 0 V vs. Li/Li^+ [66,67]. It is difficult to apply the common and simple Li deposition indication methods, due to the specific design of the cell tests. The use of CCCV charging hinders the analysis of discrepancies in the voltage relaxation [68–70]. Furthermore, the overall reduced capacity retention within each cycle, caused by the memory effect, precludes the use of the coulombic efficiency as an indicator [71,72]. However, under the assumption that Li deposition occurs, this ensures that the anode potential falls below the 50 mV threshold to form crystalline Si. Nevertheless, the results of the C-rate variation demonstrate that even at lower rates, the potential drops below this threshold, resulting in a comparable amount of trapped Li in the crystalline phase.

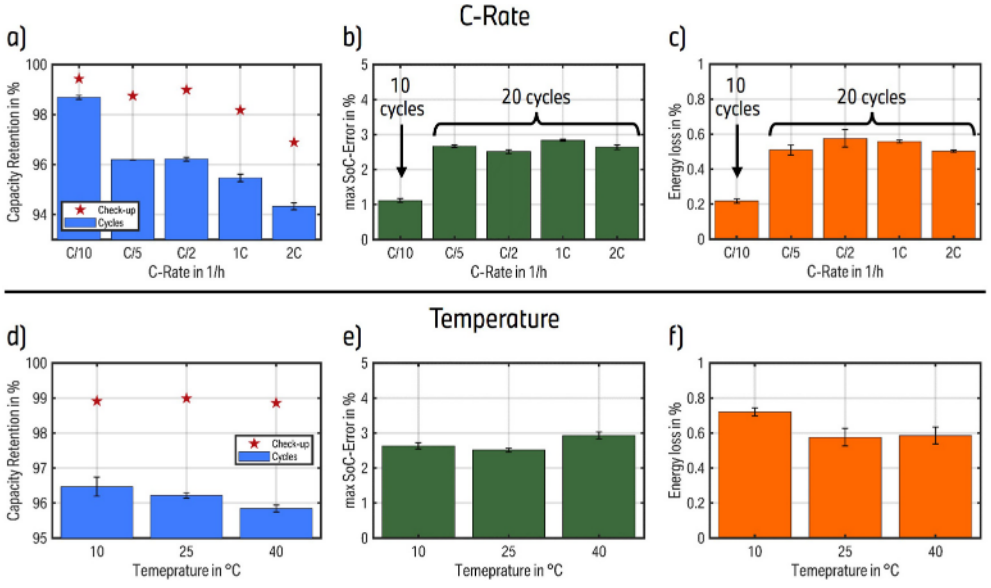

Fig. 7. Illustration of the metrics for quantifying Li trapping for the variation in the C-rate during (dis-)charging (a–c) and for the temperature variation (d–f). (a) Capacity retention for the check-ups and the specific cycles in between the check-ups for each C-rate. (b) Maximum SoC-error between the recovery and normal cycle for each C-rate. (c) Energy loss of the recovery cycle, compared to the normal cycle, for each C-rate. (d) Capacity retention for the check-ups and the specific cycles in between the check-ups for each ambient temperature. (e) Maximum SoC-error between the recovery and normal cycle for each ambient temperature. (f) Energy loss of the recovery cycle, compared to the normal cycle, for each ambient temperature.

3.3.6. Temperature variation

As with the C-rate variation, no large deviation is observable for cell A in the temperature variation between 10 and 40 °C. The capacity retention in Fig. 7d shows a small slight tendency towards an enhanced memory effect at higher temperatures, whereas the energy loss in Fig. 7f depicts the contrary tendency towards an increased effect at lower temperatures. The maximum SoC error in Fig. 7e shows no discernible trend with respect to temperature. Therefore, it can be concluded that nearly no temperature dependency exists. Both the C-rate and the temperature variation cause changes in the polarization, as a reduced temperature increases the internal resistance of the cell, similar to an increased C-rate [73]. Consequently, the polarization has most likely no effect on the amount of Li trapping.

3.4. Li trapping on anode half-cell level

The memory effect, caused by trapped Li in the fully lithiated crystalline phase, has been frequently reported and explained with pure silicon anode half-cells [11,29,39], but rarely with blend anode half-cells [57]. To demonstrate that the established SoC dependency also exist at half-cell level, a variation of the upper and lower cutoff potential is performed, as described in Table 2. Moreover, repeating the full cell tests in a comparable manner at the electrode level verifies that the observed memory effect can be attributed to the anode. The existence of the crystalline phase is additionally supported by the observation of a plateau at ~440 mV vs. Li/Li$^+$. The delithiation voltage profiles of the recovery and normal cycles during the EoT check-up are presented in Fig. 8. The first scenario outlines the anticipated worst case, with a lower cutoff potential of 10 mV vs. Li/Li$^+$ and an upper cutoff potential of 400 mV vs. Li/Li$^+$. A potential of 10 mV vs. Li/Li$^+$ is considerably below the threshold of 50 mV vs. Li/Li$^+$, whereas 400 mV vs. Li/Li$^+$ is only slightly below 440 mV vs. Li/Li$^+$, illustrated in Fig. 8a. Given the previous assumption of breaking the Si-Si clusters into isolated silicon anions, this potential range utilizes the majority of the Si-range without regaining the trapped Li. The results show increased amounts of all three metrics over any results of the cylindrical cells. The capacity retention between the first and fifteenth cycle account for 93.8 % with no appreciable degradation. Furthermore, the maximum SoC error and energy loss are found to be 5.8 % and 3.8 %, respectively. The maximum SoC error after 15 cycles of the half-cell is identical to that observed for 200 consecutive cycles of cell A. However, it should be noted that the energy loss cannot be calculated in a similar manner as presented in Eq. (4) due to the use of a pure Li metal counter electrode instead of an intercalation cathode. Therefore, the trapped Li increases the anode potential during the recovery cycle, rather than reducing the cell voltage. The overall lower voltage of an anode half-cell in comparison to a full cell, results in a significantly higher percentage of lost energy.

In the second scenario, illustrated in Fig. 8b, the upper cutoff potential is reduced to 270 mV vs. Li/Li$^+$, to utilize solely the graphite range, which is comparable to the case 30–100 % SoC for cell A. However, due to the visible degradation between the recovery and normal cycle, it is challenging to calculate a meaningful SoC error. Nevertheless, the voltage profile demonstrates a potential change in the recovery cycles with a clear but reduced characteristic, as anticipated from the results of the 30–100 % SoC case. However, the voltage profile exhibits a deviation from the expected plateau at approximately 440 mV vs. Li/Li$^+$. This plateau persists in a diminished form alongside an additional small plateau around 320 mV vs. Li/Li$^+$, which has not yet been reported.

The unexpected plateau observed at approximately 320 mV vs. Li/Li$^+$ also appears in the measurements of the third case, as shown in Fig. 8c, where the lower cutoff potential is increased to 60 mV vs. Li/Li$^+$. Given that the phase transition is known to occur below 50 mV vs. Li/Li$^+$ [2,29,31,32] or, in some cases below 60 mV vs. Li/Li$^+$ [33,38], limiting the cutoff potential to 60 mV vs. Li/Li$^+$ should not result in any crystalline silicon. This is supported by the observation that this test scenario

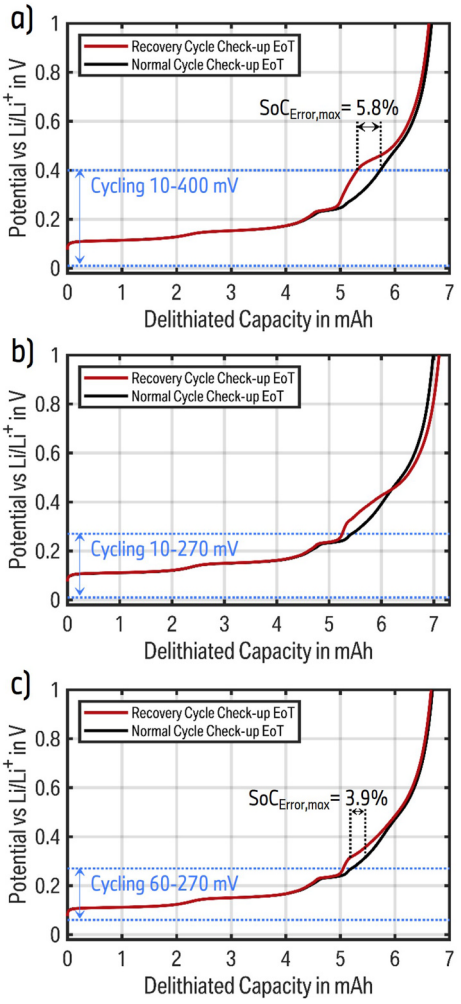

Fig. 8. Anode potential of the recovery cycle (red) and the normal cycle (black) in the EoT check-up for the cases (a) 10–400 mV vs. Li/Li + cycling, (b) 10–270 mV vs. Li/Li + cycling, and (c) 60–270 mV vs. Li/Li + cycling. The potential range during cycling is indicated in blue for each case. The maximum SoC error is visualized in (a) and (c). (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

exhibits no voltage plateau at 440 mV vs. Li/Li$^+$, where the crystalline phase is otherwise reverted to an amorphous phase. However, the discernible shift in the voltage profile, with a maximum SoC error of 3.9 %, suggests the possibility of another phase transition occurring above 60 mV vs. Li/Li$^+$. This intermediate phase appears to be reverted at approximately 320 mV vs. Li/Li$^+$, rather than at 440 mV vs. Li/Li$^+$. It is conceivable that this is a lower lithiated crystalline phase than c-Li$_{3.75}$Si, given the similarity in the general behavior of this phase transition. Nevertheless, it is not possible at this stage to make any definitive statements. Further experiments are required to prove these assumptions and evaluate under which test scenarios this behavior is reproducible.

4. Conclusion

This work analyzes the impact of the phase transition of fully lithiated silicon anode material from the amorphous to the crystalline state in LIB cells containing Gr/SiO$_x$ blend anodes at high SoC. It has been shown that:

- A crystalline phase transition at high states of lithiation is observable that impacts the operation of commercial and automotive batteries with Gr/SiO_x blend anodes.
- The phase transition is reversed only if the cells are discharged to SoC levels below 5–10 %, depending on the silicon content, leading to a memory effect for partial cycles.
- If unreversed, the crystalline phase changes the OCV characteristic, resulting in SoC and SoH estimation errors, a reduction in the discharge energy, and leads to a temporary loss of cyclable Li.
- The amount of trapped lithium shows a cumulative effect with the number of partial cycles and a dependency on their SoC range.
- If fully discharged, the phase transition is reversible, enabling an almost complete recovery of the trapped lithium.
- Partial cycling of Gr/SiO_x anode half-cells indicate an intermediate crystalline phase transition.

The anode potential repeatedly decreases below 60 mV during the cycling of Gr/SiO_x blend anodes, which results in the formation of the silicon crystalline phase c-$Li_{15}Si_4$. This changes the OCV in the lower SoC range, where silicon is predominantly active during discharging. These changes remain until the anode potential exceeds 440 mV, at which point the crystalline phase is reverted.

The results of electrochemical cell tests demonstrate that the described memory effect is present in all investigated cells containing different types of silicon alongside graphite. There is a notable correlation between the number of partial cycles before full discharge, with an increasing trend towards a higher cycle count. A critical SoC window for partial cycles is identified, wherein the lower SoC falls within the active Si-range but is not so low as to cause the recovery of the crystalline phase with each cycle. Furthermore, the upper SoC must be sufficiently high to facilitate the phase transition from amorphous to crystalline, thereby reaching a severe state of the memory effect. A slight correlation between battery degradation and the amount of trapped Li exists, with a lower SoH exhibiting less trapped Li. This suggests that the effect may decrease over the lifetime of the battery. The conducted experiments provide no evidence of a temperature- or C-rate-related dependency, both of which impact the polarization. The variations in the cutoff potentials observed in anode half-cells with blend electrodes suggest the potential existence of an intermediate crystalline phase, in addition to the well-documented c-$Li_{15}Si_4$. Further investigation is required to better comprehend the silicon lithiation behavior in blend electrodes.

In conclusion, the crystalline phase transition of silicon presents a significant challenge in the use of LIBs with Gr/SiO_x blend anodes in BEVs and other applications. The impact of the memory effect can be mitigated by limiting the upper SoC during charging, as this reduces the formation of crystalline silicon during each cycle. Moreover, it is advised that regular deep discharge cycles are conducted below the recovery threshold, to regain the trapped Li. If such operational adjustments are not feasible, it is essential that the BMS tracks the degree of lithiation of Si, especially at high SoCs. By adjusting the OCV accordingly, seamless operation as well as an accurate SoC and SoH estimation can be ensured.

CRediT authorship contribution statement

Julian Knorr: Writing – original draft, Visualization, Methodology, Investigation, Formal analysis, Conceptualization. **Hao-Chen Hsiao:** Writing – original draft, Methodology, Investigation, Formal analysis. **Alexander Adam:** Writing – review & editing, Formal analysis, Conceptualization. **Barbara Rödl:** Writing – review & editing, Supervision. **Thomas Waldmann:** Writing – review & editing, Supervision. **Markus Hölzle:** Writing – review & editing, Supervision. **Michael A. Danzer:** Writing – review & editing, Supervision.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Julian Knorr reports a relationship with BMW Group that includes: employment. Hao-Chen Hsiao reports a relationship with BMW Group that includes: employment. Alexander Adam reports a relationship with BMW Group that includes: employment. Barbara Roedl reports a relationship with BMW Group that includes: employment. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Table of abbreviations

a	Amorphous
BEV	Battery electric vehicle
BMS	Battery management system
BoT	Begin of test
c	Crystalline
CC	Constant-current
CCCV	Constant-current constant-voltage
EDX	Energy dispersive X-ray
EoT	End of test
Gr	Graphite
Li	Lithium
LIB	Lithium-ion battery
NMR	Nuclear magnetic resonance
OCP	(Half-cell) open-circuit potential
OCV	(Full-cell) open-circuit voltage
SEI	Solid electrolyte interface
SEM	Scanning electron microscopy
Si	Silicon
SiC	Silicon embedded in carbon matrix
SiO_x	Silicon oxide
SoC	State of charge
SoH	State of health
SoL	State of lithiation
XRD	X-ray diffraction

Data availability

Data will be made available on request.

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