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RESEARCH ARTICLE

Linear Active Disturbance Rejection Control-Based Voltage Controller for Buck and Boost DC/DC Converters in DC Distribution Grids

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ABSTRACT DC distribution grids have recently gained research attention for the efficient integration of converter-interfaced distributed energy resources (DER). This paper presents a voltage controller for the buck and boost DC/DC DER-interfacing converters that operate in voltage control mode, acting as DC grid-forming converters. A linear active disturbance rejection control (L-ADRC) model is proposed, consisting of an augmented Kalman filter for the state and disturbance estimation, an adaptive state reference trajectory generator and a linear quadratic regulator as feedback controller. This L-ADRC model is formulated according to the generalised ADRC concept, making the voltage controller applicable to converters of the non-minimum phase (NMP) class, like the boost DC/DC converters in voltage control mode, and suitable for matched and mismatched disturbances, opposite to the original ADRC, which exists mostly in literature of converter controllers. The formulation of the proposed L-ADRC model in the non-canonical form facilitates the employment of model-based estimation and feedback control methods, whose performance is determined through the design of several parameters. This provides more degrees-of-freedom in the design of the voltage controller, beyond the design of the common L-ADRC formulation based on the bandwidth of the linear extended state observer and the scaling factor of a proportional error feedback controller. In addition, the physical significance of the converter's states allows the integration of additional control functions, relying on the electrical quantities of the converter, for the enhancement of the performance of the voltage controller. For this, a virtual impedance-based current limiter is integrated in the L-ADRC model, which is necessary for preventing high currents at the converter's switches. Moreover, the formulation of the adaptive state reference trajectory of the L-ADRC model according to the estimated disturbance provides a smooth state reference to the state feedback controller and enhances the robustness of the voltage controller against disturbances. The L-ADRC is designed based on both frequency and time domain analyses, contrary to the design approaches of ADRC converter controllers in literature. It is validated in a hardware-in-the-loop implementation and the performance is analysed in simulation against a PID voltage controller.

INDEX TERMS DC/DC converters, voltage control, disturbance rejection, DC systems.

I. INTRODUCTION

Environmental and technical drivers motivate the increasing integration of distributed energy resources (DER) in the distribution grid, which are interfaced through power-electronics converters. Hence, DC power systems become

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attractive, offering efficient DER connection to the grid [1]. Various network topologies of DC power systems have been investigated, such as single-bus LVDC microgrids [1], one-terminal LVDC distribution grids [2], [3] and multi-terminal, MV or LV, DC distribution grids [4], [5]. The economically attractive grid connection of DER, as well as the requirements for stability and security of the DC power system, necessitate the participation of DER in the system regulation. The DER-interfacing converters can operate in voltage or power/current control mode, acting as DC grid-forming or grid-feeding converters [6]. This paper contributes to the field of voltage control design for the DC grid-forming converters in the DC power systems. Without loss of generality of the control approach, the developed voltage controller is designed for buck and boost DC/DC converters of LV MTDC distribution grids.

The voltage controller, designed based on the derived standalone nominal converter model, should achieve tight voltage control, i.e. to minimise the error between the output voltage and the desired voltage set-point, caused due to changes in the operating point [7]. The voltage control should be achieved in good dynamics, to ensure the stability of the DC power system, which presents fast dynamics due to lack of electromechanical inertia and the negative damping of the constant power loads (CPLs) [8], [9]. To exhibit the nominal stability and performance when implemented in the real converter plant, the voltage controller should reject the disturbances due to the discrepancies between the nominal model and the real plant, which perturb the output voltage from the desired set-point. These are internal disturbances, such as uncertainties of the nominal converter model, and external disturbances, like interactions of the converter with other components in the grid [10]. The robustness of the voltage controller against the external disturbances can support the plug-and-play capability of the converter: the converter presents the desired performance independently from the network topology of the DC power system where it is integrated, without ad hoc design of the voltage controller. This feature is important for the incremental deployment and expansion of future MTDC distribution grids. Moreover, the desired performance should be achieved, while respecting the current limits of the real converter plant, presenting low computation burden for facilitating the easy hardware implementation, without requiring large control input (duty cycle) close to saturation for avoiding the lost of controllability [7], [11].

The most common control technique in practice is the proportional-integral-derivative (PID) control, since it exhibits simple structure, easy implementation and functionality [12], [13]. However, the PID control presents poor performance in converters of the non-minimum-phase (NMP) class, such as the boost DC/DC converters in voltage control mode [14], [15]. In addition, the most common design methods for the PID control, based on the frequency response of the linearised nominal converter model, do not consider large-signal disturbances in the real converter plant. Hence, the PID voltage controller exhibits low robustness against disturbances, with oscillatory dynamic performance, while requiring large control input [15], [16], [17]. The low robustness cause also lack of plug-and-play capability: when the DC grid expands, i.e. in different operating point and under different interactions with other components, the PID controller cannot control successfully the output voltage without re-tuning. For the performance improvement of the PID control, automatic tuning methods have been proposed [16], [18], [19], [20], [21], [22], as well as the intelligent PID (i-PID) controller, where converter model uncertainties are estimated and rejected [23], [24], [25]. However, these solutions are computationally complex and have not yet managed to replace the simple frequency response-based tuning methods in the real-world practice of PID converter controllers, resulting in the poor control performance noted above [12], [16].

The continuing advances in digital signal processing and on-board computation capacity enabled the application of model-based feedback control methods for the voltage controller of the DC/DC converters [7], [9], [26], [27]. Thanks to their inherent properties, these modern control methods manage to compromise opposing performance requirements and operation restrictions more effectively than the error-based PID controller. To enhance the robustness against disturbances of the feedback control, adaptive and robust control methods have been proposed [28], [29], [30], [31], [32]. An alternative control solution is based on the disturbance/uncertainty estimation and attenuation (DUEA) technique [33], [34], [35]. Opposite to most adaptive and robust control techniques, the DUEA-based control manages a good balance between the nominal performance and the robustness against disturbances, through a non-complex structure, thanks to the estimation and rejection of the total disturbance [27], [36]. The active disturbance rejection control (ADRC) is the spearhead of the DUEA-based control techniques: an extended state observer (ESO) provides the estimated total disturbance, which is integrated in the state feedback controller as a feedforward compensation term for the disturbance rejection; the state reference trajectory of the feedback controller is provided by a tracking differentiator (TD) [37], [38], [39].

The application of the ADRC for the voltage control in DC/DC converters has gained increasing research interest [40], [41], [42]. These ADRC models are usually formulated according to the nominal converter model expressed in the canonical form, with its system order being the only available information. However, this original formulation of the ADRC exhibits degraded performance in converters of the NMP class, since the (right-half-plane) RHP zeros limit the bandwidth of the ESO and thus the feedback controller. To overcome this limitation, the model-assisted ADRC has been proposed, whose formulation considers partial information of the real converter included in its

nominal model, to cancel the disturbance stemming from the RHP zeros [43]. Reference [44] reviews the formulation and compares the control performance of such modified ADRC models, with different partial information in the nominal converter model used in the ADRC design, e.g. information about poles and/or (right-half-plane) zeros of the converter. Nevertheless, the nominal converter model for the design of these ADRC models is also expressed in the canonical form, similarly to the original ADRC formulation. Hence, the total disturbance is integrated in the nominal converter model always in the same dynamic equation as the control input, fulfilling the matching condition. As a result, the designed ADRC models are not suitable for handling mismatched disturbances. The expression of the nominal converter model in non-canonical form enables the formulation of a suitable feedforward control term of the ADRC to reject the exact type of disturbances (matched or mismatched) that are introduced in the converter model [45], [46]. Reference [47] proposes the generalised ADRC, which combines the two aforementioned modifications. Although its benefits are known in theory, there is no development of such ADRC model for the voltage control in DC/DC converters.

When partial information of the converter's dynamics is used in the ADRC formulation in the non-canonical form, the state reference trajectory is usually generated by a filter computed as the equilibrium point of the dynamic nominal converter model at the steady-state operation [44], [47], [48]. By avoiding the computation of the derivatives of the output reference signal in the TD of the ADRC, this approach makes the computation burden of the voltage controller smaller and thus its hardware implementation easier [39], [49]. However, this nominal state reference trajectory does not constitute a smooth state profile, since a step-wise change of the output set-point is reflected as a step-wise change of the states, opposite to the nominal state reference trajectory generated by the TD in the original ADRC.

The vast majority of the ADRC applications in converters refers to the original linear ADRC (L-ADRC), which is designed according to the bandwidth of a linear ESO (L-ESO) and the scaling factor of a proportional error feedback controller [40], [42], [50]. Although the idea of integrating advanced estimation and feedback control methods, such as Kalman filter and energy-based control, in the ADRC formulation is theoretically known for providing more degrees-of-freedom in the control design, there is limited work on such ADRC models for voltage control in converters [51], [52].

A limitation of the canonical form of the nominal converter model is the lack of physical significance of the states. This does not allow the employment of additional control functions, relying on the electrical quantities of the converter. Due to lack of work on ADRC converter controllers in the non-canonical form, there is also limited work on additional control functions integrated in the ADRC voltage controller for its performance enhancement, such as a current limiter [53].

Moreover, the design process of ADRC converter controllers in literature does not include performance analysis in both frequency and time domains, as well as restrictions of the hardware implementation. There are only a few theoretical works that relate the performance of the ADRC in time domain with the performance requirements expressed through the frequency response [54], [55]. The common design approach in literature considers only the effect of the ADRC parameters on the performance under small-signal disturbance in the frequency domain [49], [56], [57], [58], [59], while the performance under large-signal disturbance in the time domain is ignored.

This paper presents an L-ADRC model for the voltage control in buck and boost DC/DC converters. Leveraging the well-known linear quadratic Gaussian (LQG) controller [60], the developed L-ADRC model consists of three elements: an augmented Kalman filter (KF) as ESO, a linear quadratic regulator (LQR) as feedback controller and a reference trajectory generator (RTG); a virtual impedance-based current limiter is also integrated in this voltage controller. Building on the work of [52] and [53], which demonstrates the performance of this LQG-based voltage controller for buck DC/DC converters, this paper contributes by presenting the formulation properties and design of the L-ADRC model that enable the desired features of the voltage controller, missing from the existing ADRC applications in DC/DC converters:

- The L-ADRC voltage controller is applicable to converters of the NMP system class and capable of attenuating matched and mismatched disturbances introduced in the nominal converter model, thanks to its formulation according to the generalised ADRC.
- The developed L-ADRC model provides more degrees-of-freedom in the voltage control design than the original L-ADRC, offering flexibility in the design process for the fulfilment of opposing performance requirements. This is achieved through the employment of advanced model-based estimation and feedback control methods, whose performance is determined through the design of several parameters.
- The L-ADRC voltage controller integrates additional control functions, i.e. a current limiter here, relying on the electrical quantities of the DC/DC converter. This is enabled thanks to the formulation of the L-ADRC model based on converter states with their physical significance.
- In the developed L-ADRC model, the generated state reference trajectory constitutes a smooth state profile for the state feedback controller, avoiding step-wise changes. This is achieved through the formulation of the RTG as the online update of the nominal reference trajectory according to the estimated total disturbance.
- The parameters of the developed L-ADRC model are designed through performance analysis in both frequency and time domains, and this design is validated

through hardware-in-the-loop (HiL) tests. In this way, the analyses in both domains act supplementarily for the parameters design, which is taken into consideration for the first time in the ADRC literature in converter applications.

The outline of the paper is as follows: Section II presents the structure of the developed L-ADRC model and discusses its formulation properties. In Section III, the parameters of the L-ADRC model are designed, by analysing their effect on the performance of the voltage controller and validating them in hardware-in-the-loop (HiL) tests. Section V compares the performance of the proposed L-ADRC model with the PID voltage controller, in frequency and time domains, and Section VII concludes on the contributions of this work according to the presented model and results.

II. L-ADRC MODEL FOR VOLTAGE CONTROL IN BUCK AND BOOST DC/DC CONVERTERS

In this section, the developed L-ADRC model is presented. First, the nominal models of the buck and boost DC/DC converters are derived. Then the virtual state of the total disturbance is defined and introduced to these converter models. The elements of the L-ADRC structure are then formulated on the basis of these nominal converter models. Lastly, the beneficial formulation properties of this voltage controller are discussed.

A. NOMINAL CONVERTER MODELS

Figure 1 illustrates the circuit diagram of the standalone nominal model of a buck DC/DC converter, where V_{in} is the DC voltage of the ideal voltage source substituting the DER unit at the input port of the real DC grid-forming converter in the DC distribution grid, and R_{Ld} is the resistive load representing the nominal resistive output impedance of the real converter plant at the steady-state operation of the DC grid. In the circuit diagram, C is the filter capacitor and R_C is its parasitic resistance, L is the filter inductor and R_L is its parasitic resistance, v_o is the output voltage, i_L is the inductor current and u is the control input from the voltage controller (duty cycle). A similar circuit diagram can be drawn also for the standalone nominal model of the boost DC/DC converter.

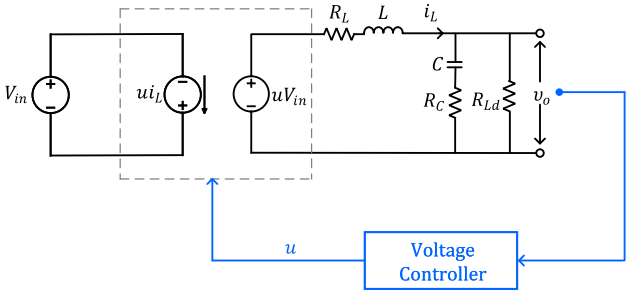

FIGURE 1. Circuit diagram of nominal model of buck DC/DC converter.

The nominal converter models are averaged continuous-time models in continuous conduction mode, which is considered in this work. The nominal model of the buck DC/DC converter is described by the second-order small-signal state-space model in (1), where the two states are the capacitor voltage v_C and the inductor current i_L, the measurement y is the output voltage v_o, the control input u is the duty cycle and $R_a = R_{Ld} + R_C$ and $R_b = R_{Ld} + R_L$. For simplicity, the variable notation of the diagram in Figure 1 is kept also for the perturbed variables of the small-signal model, omitting the notation of time-varying signals.

$$\begin{bmatrix} \dot{v_C} \\ \dot{i_L} \end{bmatrix} = \overbrace{\begin{bmatrix} -\frac{1}{CR_a} & \frac{R_{Ld}}{CR_a} \\ -\frac{R_{Ld}}{LR_a} & -\frac{R_L R_a + R_{Ld} R_C}{LR_a} \end{bmatrix}}^{\mathbf{A}_{buck}} \begin{bmatrix} v_C \\ i_L \end{bmatrix} + \overbrace{\begin{bmatrix} 0 \\ \frac{V_{in}}{L} \end{bmatrix}}^{\mathbf{B}_{buck}} u$$
$$y = \underbrace{\begin{bmatrix} \frac{R_{Ld}}{R_a} & \frac{R_{Ld} R_C}{R_a} \end{bmatrix}}_{\mathbf{C}_{buck}} \begin{bmatrix} v_C \\ i_L \end{bmatrix} \tag{1}$$

The averaged continuous-time model of the boost DC/DC converter is linearised around the equilibrium operating point (V_C^*, I_L^*, U^*) provided in (2) as function of the output voltage set-point V^*. This derives the small-signal state-space model in (3), where the same definition of states, measurement and control input and the same notation of the perturbed variables are kept, as for the buck DC/DC converter.

$$\begin{aligned} V_C^* &= \frac{R_a}{R_{Ld}} V^* - R_C I_L^* \\ I_L^* &= \frac{1}{R_{Ld}(1-U^*)} V_C^* \\ U^* &= \frac{V_{in} R_a}{2 V_C^* R_b} \\ &\quad \pm \frac{\sqrt{V_{in}^2 R_a^2 + 4 V_C^* R_b \frac{-V_C^* R_b R_{Ld} + V_{in} R_a R_{Ld} - R_L V_C^* R_b}{R}}}{2 V_C^* R_b} \end{aligned} \tag{2}$$

$$\begin{bmatrix} \dot{v_C} \\ \dot{i_L} \end{bmatrix} = \overbrace{\begin{bmatrix} -\frac{1}{CR_a} & \frac{(1-U^*)R_{Ld}}{CR_a} \\ -\frac{R_{Ld}(1-U^*)}{LR_a} & -\frac{R_L R_a + R_{Ld} R_C (1-U^*)}{LR_a} \end{bmatrix}}^{\mathbf{A}_{boost}} \begin{bmatrix} v_C \\ i_L \end{bmatrix}$$
$$+ \overbrace{\begin{bmatrix} -\frac{R_{Ld} I_L^*}{CR_a} \\ \frac{R_{Ld} V_C^* + 2 R_{Ld} R_C I_L^* (1-U^*)}{LR_a} \end{bmatrix}}^{\mathbf{B}_{boost}} u$$
$$y = \underbrace{\begin{bmatrix} \frac{R_{Ld}}{R_a} & \frac{R_{Ld} R_C}{R_a} \end{bmatrix}}_{\mathbf{C}_{boost}} \begin{bmatrix} v_C \\ i_L \end{bmatrix} \tag{3}$$

It can be noticed that the nominal model of both DC/DC converters include partial information of the real converter plants, in terms of first-order dynamics of the electrical quantities of the capacitor voltage and inductor current. In addition, the nominal converter models are expressed in the non-canonical form, and thus the states of the state-space models keep their physical significance.

The L-ADRC model is formulated based on this nominal converter models, which include partial information of the

real plants, expressed in the non-canonical form. Therefore, the formulation of the L-ADRC model follows the form of the generalised ADRC. For simplicity, the formulation of the elements of the L-ADRC model and its transfer functions in the following sections are expressed in terms of **A**, **B** and **C** matrices, corresponding to $\mathbf{A}_{buck}$, $\mathbf{B}_{buck}$ and $\mathbf{C}_{buck}$ of (1) in the case of the buck DC/DC converter, or $\mathbf{A}_{boost}$, $\mathbf{B}_{boost}$ and $\mathbf{C}_{boost}$ of (2) in the case of the boost DC/DC converter.

B. VIRTUAL STATE OF TOTAL DISTURBANCE

Considering that the external and internal disturbances perturb the output voltage of the DC/DC converter, they can be regarded physically as circulating currents, as in [61] and [62]. Therefore, the total disturbance is modelled as a virtual current source i_d, introduced in the nominal converter model, i.e. the model of the total disturbance presents a physical significance, following the physical significance of the states of the nominal model. This modelling approach of the total disturbance in the DC/DC converters leverages similar disturbance models used in motor systems [63]. Figure 2 presents this virtual current source in the circuit diagram of the buck DC/DC converter, illustrated in dotted line to be distinguished from the physical elements of the circuit. Similar circuit diagram with the virtual current source can be drawn also in the case of the boost DC/DC converter.

The circulating currents are unknown (unmeasurable) constants, changing occasionally step-wise with correlation time much larger than the time constants of the converter plants in the DC distribution grids [61], [64]. As a result, the total disturbance i_d can be considered as a bounded stochastic and non-white variable, which can present a countable number of discontinuity points [61], [65].

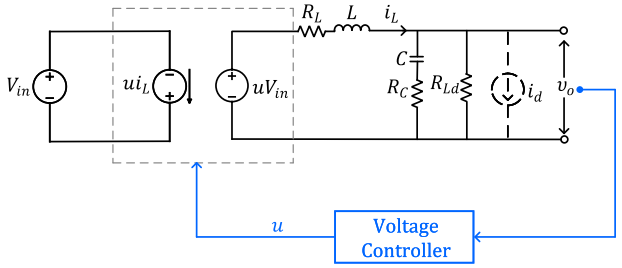

FIGURE 2. Circuit diagram of nominal model of buck DC/DC converter with virtual current source i_d.

The state-space model of the DC/DC converter with the virtual current source i_d is derived as

$$\begin{aligned} \dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \mathbf{B}u + \mathbf{B}_d i_d \\ y &= \mathbf{C}\mathbf{x} \end{aligned} \tag{4}$$

where the matrix $\mathbf{B}_d$ is the same for both DC/DC converters, given by (5), following the direction of the current of the virtual source as in the circuit diagram of Figure 2. Considering the formulation of $\mathbf{B}_{buck}$, $\mathbf{B}_{boost}$ and $\mathbf{B}_d$, following the non-canonical form of the nominal converter models with the introduced total disturbance, it can be concluded that the i_d is a mismatched disturbance in the case of the buck DC/DC converter, as it does not appear in the same dynamic equation with the control input, opposite to the case of the boost DC/DC converter, where it is a matched disturbance.

$$\mathbf{B}_d = \begin{bmatrix} -\frac{1}{C} \\ 0 \end{bmatrix} \tag{5}$$

In the context of the ADRC, the total disturbance is considered as an additional virtual state, which is now integrated in the state vector **x** of the nominal converter model, to form the augmented state vector $\mathbf{x}_{aug}$ in (6). It should be noticed that this virtual state here includes only the internal and external disturbances, but not the modelled first-order dynamics of the nominal converter model, opposite to the original ADRC formulation derived on the basis of the nominal converter model without any information of the real converter device. The dynamics of the nominal converter model is represented here by the dynamic equations of the states with their physical significance, and thus it is known (not part of the disturbance/uncertainty).

$$\mathbf{x}_{aug} = \begin{bmatrix} \mathbf{x} \\ i_d \end{bmatrix} \tag{6}$$

C. STRUCTURE OF L-ADRC MODEL

Figure 3 presents the structure of the developed L-ADRC model applied as voltage controller in the buck DC/DC converter, while the same structure of the L-ADRC model can be applied also in the case of the boost DC/DC converter. The next paragraphs describe the three elements with their properties, and derive the control input, i.e. the duty cycle provided by the L-ADRC voltage controller.

1) AUGMENTED KALMAN FILTER (KF)

The augmented KF is the ESO of the L-ADRC model, which provides the estimated states of the nominal model $\hat{\mathbf{x}}$ and the estimated virtual state $\hat{i}_d$. The state estimation allows for avoiding the usage of two measurement sensors; the input of the L-ADRC model is only the output voltage measurement. For applying the augmented KF, the non-white noise i_d is regarded as the transformation of a white noise input w with unit spectral density through a linear shaping filter [61], [66]. In this way, the system to be estimated by the augmented KF includes the nominal converter model and the shaping filter, with a white signal being the noise input to this system. The shaping filter is the same in the case of both DC/DC converters. The dynamics of the virtual state i_d is determined by the state-space model of the shaping filter [61], [66]

$$\begin{aligned} \dot{x}_f &= a_f x_f + b_f w \\ i_d &= x_f \end{aligned} \tag{7}$$

where x_f is the state of the shaping filter and a_f and b_f are parameters of the shaping filter given by (8), with τ_d being

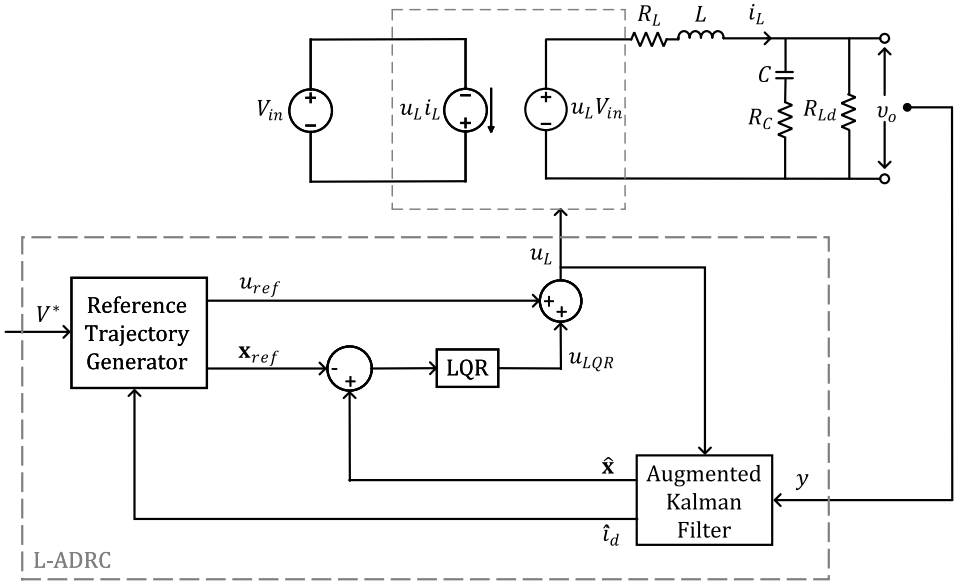

FIGURE 3. Structure of L-ADRC model applied in buck DC/DC converter.

the correlation time and σ_d^2 the variance of the disturbance i_d.

$$a_f = -\frac{1}{\tau_d}$$
$$b_f = \sqrt{2\sigma_d^2 a_f} \tag{8}$$

The augmented state-space model of the system of the nominal converter model and the shaping filter is derived by (9), where n is the white noise of the measurement y with variance σ_n^2. This augmented model is valid for both DC/DC converters with the corresponding matrices.

$$\begin{bmatrix} \dot{v}_C \\ \dot{i}_L \\ \dot{i}_d \end{bmatrix} = \overbrace{\begin{bmatrix} \mathbf{A} & \mathbf{B}_d \\ 0 & -a_f \end{bmatrix}}^{\mathbf{A}_{aug}^{KF}} \begin{bmatrix} v_C \\ i_L \\ i_d \end{bmatrix} + \overbrace{\begin{bmatrix} \mathbf{B} \\ 0 \end{bmatrix}}^{\mathbf{B}_{aug}^{KF}} u + \begin{bmatrix} \mathbf{0}_{2\times 1} \\ b_f \end{bmatrix} w$$
$$y = \underbrace{\begin{bmatrix} \mathbf{C} & 0 \end{bmatrix}}_{\mathbf{C}_{aug}^{KF}} \begin{bmatrix} v_C \\ i_L \\ i_d \end{bmatrix} + n(t) \tag{9}$$

For this system model, the augmented KF is derived as

$$\dot{\hat{\mathbf{x}}}_{aug} = \mathbf{A}_{aug}^{KF}\hat{\mathbf{x}}_{aug} + \mathbf{B}_{aug}^{KF}u + \mathbf{L}_{KF}(y - \mathbf{C}_{aug}^{KF}\hat{\mathbf{x}}_{aug}) \tag{10}$$

The Kalman gain $\mathbf{L}_{KF}$ is defined as

$$\mathbf{L}_{KF} = \mathbf{P}\mathbf{C}_{aug}^{KF\,T} R_n^{-1} \tag{11}$$

where $\mathbf{P}$ is the solution of the algebraic Riccati equation

$$\mathbf{A}_{aug}^{KF}\mathbf{P} + \mathbf{P}\mathbf{A}_{aug}^{KF\,T} - \mathbf{P}\mathbf{C}_{aug}^{KF\,T} R_n^{-1}\mathbf{C}_{aug}^{KF}\mathbf{P} + \mathbf{B}_w R_w \mathbf{B}_w^T = 0 \tag{12}$$

with R_n and R_w being the covariance of the measurement noise n and the covariance of the white noise w with unit spectral density, respectively, which are assumed to be uncorrelated. The parameters σ_d, τ_d and R_n in (11)-(12) determine the Kalman gain $\mathbf{L}_{KF}$, affecting thus the performance of the augmented KF, i.e. they constitute degrees-of-freedom for the design of the ESO of the L-ADRC model.

2) REFERENCE TRAJECTORY GENERATOR (RTG)

The RTG calculates online the state reference trajectory $\mathbf{x}_{ref}$ as the equilibrium point of the nominal converter model with the total disturbance i_d, which is determined by its estimated value $\hat{i}_d$, as appears in (13).

$$\begin{bmatrix} \mathbf{x}_{ref} \\ u_{ref} \end{bmatrix} = \overbrace{\begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & 0 \end{bmatrix}^{-1}}^{\mathbf{S}} \begin{bmatrix} \mathbf{0}_{2\times 1} \\ V^* \end{bmatrix} + \overbrace{\begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & 0 \end{bmatrix}^{-1}}^{\mathbf{L}_{adp}} \begin{bmatrix} -\mathbf{B}_d \\ 0 \end{bmatrix} \hat{i}_d$$
$$= \begin{bmatrix} \mathbf{x}_{nom} \\ u_{nom} \end{bmatrix} + \begin{bmatrix} \mathbf{x}_{adp} \\ u_{adp} \end{bmatrix} \tag{13}$$

The $\mathbf{x}_{ref}$ consists of two terms, $\mathbf{x}_{nom}$ and $\mathbf{x}_{adp}$. The nominal state reference trajectory $\mathbf{x}_{nom}$ is the state of the nominal converter model at the equilibrium operating point determined by the output reference V^* (voltage set-point). This corresponds to the reference filter used in the generalised ADRC in [47] and [48], which transforms the output reference to the state reference trajectory of the converter. This is equivalent to the state reference trajectory generation by the TD of the original ADRC through the derivatives of the output reference, considering that in the generalised ADRC the nominal model is expressed in the non-canonical form. The adaptation term $\mathbf{x}_{adp}$, computed online according to the estimated disturbance $\hat{i}_d$, conforms the $\mathbf{x}_{nom}$, to make the state reference trajectory $\mathbf{x}_{ref}$ a smooth state profile without step-wise changes, by following the dynamics of

the real converter plant. The objective of a smooth state profile is similar in the case of the TD in the original ADRC; however, in the L-ADRC model here this is achieved while avoiding the derivation of the output reference. As a result, the computation burden of the RTG is kept low, simplifying the implementation of the L-ADRC model in the hardware of the converter [39], [49]. Moreover, the adaptive state reference trajectory $\mathbf{x}_{ref}$ increases the robustness of the L-ADRC voltage controller against disturbances, as pointed out in similar ADRC formulation approaches [63].

3) LINEAR QUADRATIC REGULATOR (LQR)

The LQR, as the feedback controller of the L-ADRC model, minimises the error between the estimated states $\hat{\mathbf{x}}$ of the nominal converter model, provided by the augmented KF, and the state reference trajectory $\mathbf{x}_{ref}$, provided by the RTG. The gain $\mathbf{K}_{LQR}$ of the LQR is designed according to the nominal converter model, so that the control law achieves the desired nominal performance. This is expressed as the minimisation of the following cost function:

$$J = \int_0^\infty [(\mathbf{x} - \mathbf{x}_{nom})^T \mathbf{Q} (\mathbf{x} - \mathbf{x}_{nom}) + R(u - u_{nom})^2]\, dt \tag{14}$$

where R is a weighting factor to penalise the control effort and $\mathbf{Q} = q\mathbf{C}^T\mathbf{C}$ is a symmetric, positive semidefinite weighting matrix to penalise the error of the output voltage. The parameters q and R, determining the gain $\mathbf{K}_{LQR}$ of the LQR are the degrees-of-freedom for the design of the feedback controller of the L-ADRC model.

For different values of the parameters q and R, Figure 4 presents the deviations of the control input Δu_{LQR} around its equilibrium U^* for deviations of the capacitor voltage Δv_C and the inductor current Δi_L from their equilibrium V_C^* and I_L^*, respectively, in the case of the buck DC/DC converter with the nominal parameters of Table 14 in Section VIII. For smaller values of q and larger values of R, the LQR reacts more strongly to current deviations. In addition, the 3D plane becomes more flat, indicating a less sensitive control input to deviations of voltage or current, i.e. the LQR reacts to voltage/current deviations without requiring large control input. As the value of q increases and of R decreases, the LQR presents the opposite performance: the control input reacts more strongly to the deviations of the voltage and it reaches easily the saturation limits, becoming incapable for providing successful control. It can be concluded that there is a trade-off in the design of the q and R parameters of the LQR in the case of the buck DC/DC converter between the main control goal of tight voltage control and effective current control for the protection of the switches, without large control input.

Similarly, Figure 5 presents the deviations Δu_{LQR} for the deviations Δv_C and Δi_L for different values of q and R in the case of the boost DC/DC converter with the nominal parameters of Table 14 in Section VIII. For all values of q and R, the control input u_{LQR} does not change with the deviations of i_L. For small values of q and large values of R, the control input is less sensitive to the voltage deviations, achieving tight voltage control without large control input, but also without preventing large current deviations.

It should be mentioned that the aforementioned analysis of the effect of the LQR parameters on the deviations of voltage, current and duty cycle (electrical quantities of the DC/DC converter) is possible thanks to the expression of the nominal converter model in the non-canonical form and thus the physical significance of its states. This provides an insight in the performance of the feedback controller of the L-ADRC model, in terms of achieved voltage control and the requirements of control input and current injection from the converter.

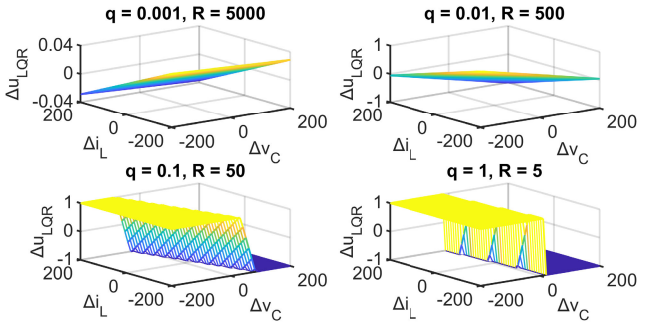

FIGURE 4. Deviations Δu_{LQR} for deviations Δv_C and Δi_L for different LQR parameters q and R in the buck DC/DC converter.

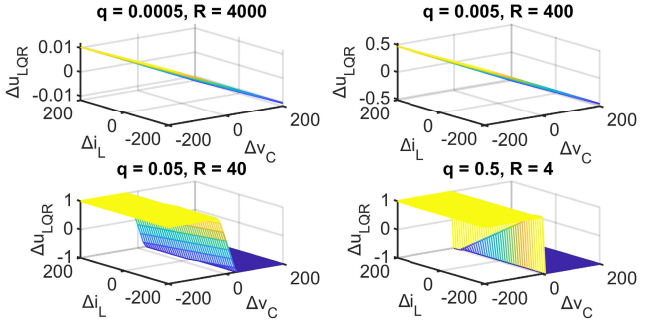

FIGURE 5. Deviations Δu_{LQR} for deviations Δv_C and Δi_L for different LQR parameters q and R in the boost DC/DC converter.

4) CONTROL INPUT

The control input u_L is determined by the feedback term u_{LQR} from the feedback controller LQR and the feedforward term u_{ref} from the RTG, i.e.,

$$\begin{aligned} u_L &= u_{LQR} + u_{ref} \\ &= -\mathbf{K}_{LQR}(\hat{\mathbf{x}} - \mathbf{x}_{ref}) + u_{ref} \\ &= -\mathbf{K}_{LQR}(\hat{\mathbf{x}} - (\mathbf{x}_{nom} + \mathbf{x}_{adp})) + u_{nom} + u_{adp} \end{aligned} \tag{15}$$

As it can be seen in (15), the control input consists of three terms. The first term determines the convergence of the estimated states $\hat{\mathbf{x}}$, and thus the states $\mathbf{x}$, to the online generated state reference trajectory $\mathbf{x}_{ref}$ according to the

dynamics of the feedback controller, which is designed according to the desired dynamic performance. The terms $\mathbf{K}_{LQR}\mathbf{x}_{nom}$ and u_{nom} include the information of the nominal dynamics and the nominal control input of the converter model, determining thus its nominal dynamic performance. The third term u_{adp}, a feedforward term of the estimated disturbance as denoted in (13), achieves the disturbance rejection.

D. INTEGRATED CURRENT LIMITER IN L-ADRC VOLTAGE CONTROLLER

As discussed above, the LQR cannot achieve effective voltage control while preventing large current at the switches with the same design of its parameters. The q and R parameters are designed to fulfil the requirements of the voltage control and a current limiter needs to be integrated in the L-ADRC voltage controller, to prevent large currents close to the operational limits of the DC/DC converter. For this, the approach of the virtual-impedance current limiter (VICL) is adopted. Figure 6 presents the integration of the VICL element to the structure of the L-ADRC model. The state reference trajectory $\mathbf{x}_{ref}$ from the RTG is decreased by the output $\mathbf{x}_{VI}$ of the VICL given in (16), representing the voltage drop across the virtual impedance of the current limiter, which is adaptive according to the output current i_o of the DC/DC converter.

$$\mathbf{x}_{VI} = \begin{bmatrix} (\max(k_p(i_o - I_{thres}), 0)) \cdot i_o \\ 0 \end{bmatrix} \tag{16}$$

The parameter k_p is

$$k_p = \frac{V^*}{I_{max}(I_{max} - I_{thres})} \tag{17}$$

where I_{thres} is the over-current threshold, beyond which the VICL is activated, and I_{max} is the maximum allowed output current of the DC/DC converter. When the output current i_o exceeds the over-current threshold I_{thres}, the adaptive virtual impedance becomes non-zero and thus the VICL is activated, to decrease the voltage reference of the LQR by the voltage drop $\mathbf{x}_{VI}$. In this way, the voltage control is relaxed, to avoid commanding large current injection from the DC/DC converter. It should be noticed that, to realise the concept of the virtual impedance-based current limiter, the formulation of $\mathbf{x}_{VI}$ in (16) relies on the definition of the states with their physical significance, as electrical quantities. This is not possible when the nominal converter model is expressed in the canonical form, where the second state is defined as the derivative of the first, i.e. as a relation of both states.

It should be noticed that theoretically the virtual impedance relates the output current i_o with the output voltage v_o. However, in this implementation it affects the state of the capacitor voltage v_C, under the valid assumption that the current though the filter capacitance is very small and v_o and v_C are thus almost equal.

The use of the output current i_o as input in the VICL indicates the need for a current sensor, additionally to the voltage measurement sensor that the L-ADRC voltage controller needs. The estimated inductor current i_L cannot be used as input to the VICL, even under the valid assumption of almost equal i_o and i_L. The L-ADRC structure does not constitute a state observer-based feedback controller, like the LQG, where the estimated states converge to the measurements. In the L-ADRC structure, there is a feedforward term of the control input, which shifts the output measurements compared to the estimated states for the disturbance rejection. Therefore, the peak current, which is important for the functionality of the VICL, is different for the i_o and $\hat{i_L}$. This is further explained in Section IV, where internal signals of the L-ADRC structure are presented to discuss the functionality of the developed voltage controller.

E. TRANSFER FUNCTIONS OF L-ADRC MODEL

The transfer functions of the L-ADRC model are derived in this section to provide an insight in the properties of its formulation. For this derivation, the VICL is not included in the structure of the L-ADRC voltage controller: the VICL is activated under large-signal disturbances, not analysed through the transfer functions, which are used for the small-signal performance analysis in the frequency domain. By following the process of [60], the structure of the elements of the L-ADRC model in Figure 3 can be transformed to the diagram of the L-ADRC model with transfer function blocks in Figure 7, where the reference signal $r(s)$ corresponds to the set-point V^* of the output voltage, $C_L^{PF}(s)$ is the transfer function of the pre-filter, $C_L^{FB}(s)$ is the transfer function of the feedback controller, $C_L^{FF}(s)$ is the transfer function of the feedforward term, and $P(s)$ is the transfer function of the nominal converter model, determined as

$$\begin{aligned} P(s) &= \mathbf{C}(sI - \mathbf{A})^{-1}\mathbf{B} \\ C_L^{PF}(s) &= \mathbf{C}_{aug}^{KF}\left[(\mathbf{S})_1\ (\mathbf{S})_2\ 0\right]^T \\ C_L^{FB}(s) &= \mathbf{K}_L(sI - \mathbf{A}_{aug}^{KF} \\ &\quad + \mathbf{L}_{KF}\mathbf{C}_{aug}^{KF} + \mathbf{B}_{aug}^{KF}\mathbf{K}_L)^{-1}\mathbf{L}_{KF} \\ C_L^{FF}(s) &= (\mathbf{S})_3 \end{aligned} \tag{18}$$

where the gain $\mathbf{K}_L$ is determined as the 1×3 vector

$$\mathbf{K}_L = \begin{bmatrix} (\mathbf{K}_{LQR})_1 \\ (\mathbf{K}_{LQR})_2 \\ [-(\mathbf{K}_{LQR})_1(\mathbf{L}_{adp})_1 \\ -(\mathbf{K}_{LQR})_2(\mathbf{L}_{adp})_2 - (\mathbf{L}_{adp})_3] \end{bmatrix}^T \tag{19}$$

with $(\mathbf{a})_i$ being the $i-$th element of the vector $\mathbf{a}$ or $\mathbf{a}^T$.

For the assessment of the L-ADRC performance in terms of disturbance rejection and noise attenuation, an input disturbance d and measurement noise n are introduced in the diagram of Figure 7. The input disturbance d represents all the internal and external disturbances that might occur in the real converter plant, except for the dynamics of the converter represented through the nominal model and the measurement

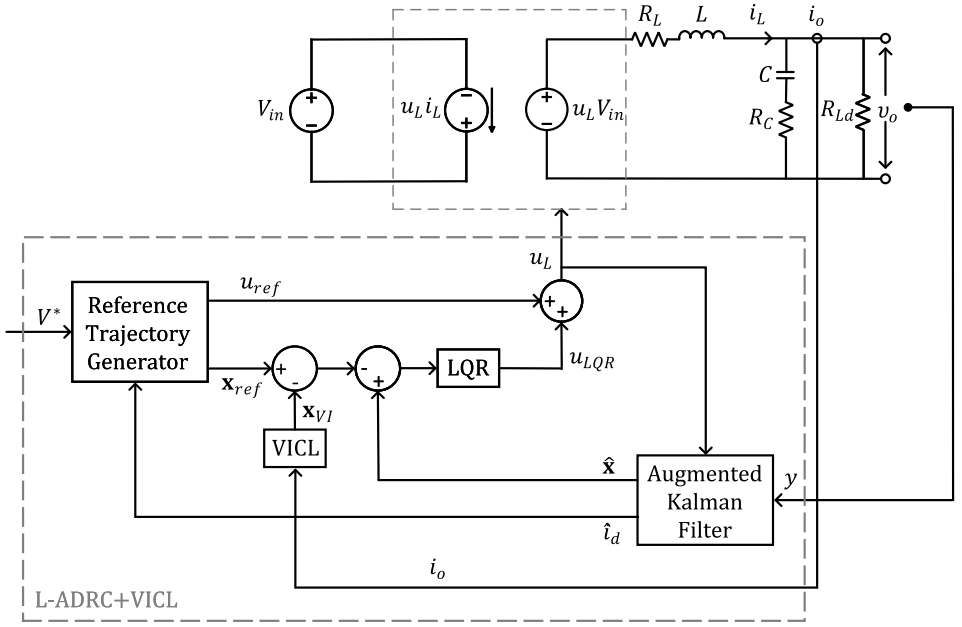

FIGURE 6. Structure of L-ADRC model with integrated VICL applied in buck DC/DC converter.

noise represented through n. The output $y(s)$ is expressed as

$$\begin{aligned} y(s) &= P(s)u_L(s) + P_d d(s) + n(s) \\ &= \mathbf{C}(sI - \mathbf{A})^{-1}\mathbf{B}u_L(s) \\ &\quad + \mathbf{C}(sI - \mathbf{A})^{-1}\mathbf{B}_d d(s) + n(s) \end{aligned} \tag{20}$$

since the input disturbance d is introduced in the nominal state-space model of the converter through the $\mathbf{B}_d$, similarly to the virtual current source i_d in (4). By substituting in (20) the control input from the block diagram of the L-ADRC model in Figure 7

$$u_L = C_L^{FB}(s)[C_L^{PF}(s)r(s) - y(s)] + C_L^{FF}(s)r(s) \tag{21}$$

the $y(s)$ is written

$$\begin{aligned} y(s) = &\underbrace{\frac{P(s)[C_L^{FB}(s)C_L^{PF}(s) + C_L^{FF}(s)]}{1 + P(s)C_L^{FB}(s)}}_{G_{yr}} r(s) \\ &+ \underbrace{\frac{P_d(s)}{1 + P(s)C_L^{FB}(s)}}_{G_{yd}} d(s) \\ &+ \underbrace{\frac{1}{1 + P(s)C_L^{FB}(s)}}_{G_{yn}} n(s) \end{aligned} \tag{22}$$

The three terms in (22) determine the three transfer functions of the closed-loop system (DC/DC converter controlled by the L-ADRC model), namely the reference-to-output $G_{yr}(s) = y(s)/r(s)$, the input disturbance-to-output $G_{yd}(s) = y(s)/d(s)$ and the measurement noise-to-output $G_{yn}(s) = y(s)/n(s)$ transfer functions.

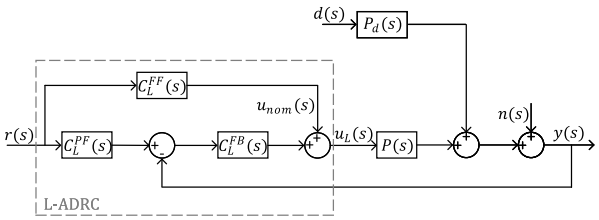

FIGURE 7. Diagram of L-ADRC model with transfer function blocks, included input disturbance $d(s)$ and measurement noise $n(s)$.

F. PROPERTIES OF THE FORMULATION OF THE L-ADRC MODEL

The developed L-ADRC model presents the following properties stemming from its formulation, which provide desired features to the voltage controller of the DC/DC converters.

1) SUITABILITY FOR CONVERTERS OF NMP SYSTEM CLASS

The proposed L-ADRC model is formulated based on a nominal converter model that includes partial knowledge about the real converter plant, as appears in (1) and (3). Due to this, the feedforward term u_{ref} of the control input in (13) does not consists only of the term u_{adp} for the online disturbance rejection, but also the fixed term of the nominal control input u_{nom}. As appears in Figure 7, the term u_{adp} is integrated in the transfer function $C_L^{FB}(s)$ of the feedback controller, since it is expressed in terms of the estimated virtual state $\hat{\imath}_d$. This approach follows the formulation of the original ADRC [38], [67]. The u_{nom} is the only term generated by the feedforward block $C_L^{FF}(s)$. This term rejects

the internal disturbances of the nominal converter model that includes partial information of the real converter plant. These known state-dependent disturbances include the instabilities due to RHP zeros in the case of nominal converter model of the NMP class, like the boost DC/DC converter in voltage control mode. Therefore, thanks to the feedforward term u_{nom}, the proposed L-ADRC model is suitable to converters of the NMP class, which need a feedforward control law to achieve dynamic performance with small settling time and undershoot [43], [68], [69].

2) ATTENUATION OF MATCHED AND MISMATCHED DISTURBANCES

According to (13) for the RTG of the L-ADRC model, the feedforward term u_{adp} for the online disturbance rejection consists of the estimated disturbance $\hat{i}_d$ multiplied with the compensation gain $(\mathbf{L}_{adp})_3$. This feedforward term is derived as the equilibrium steady-state operating point of the dynamic nominal converter model with partial information about the real converter plant, where the disturbance i_d is integrated. Hence, this term can reject this disturbance, as appears in the expression of the nominal converter model, i.e. matched or mismatched [45]. Thanks to the formulation of the feedforward term u_{adp}, the L-ADRC model is able to attenuate the right type of the disturbance integrated at the nominal model of each DC/DC converter. This and the previous features of the proposed L-ADRC model stem from its formulation according to the generalised ADRC concept.

3) REDUCED ESTIMATION BURDEN

The ESO of the proposed L-ADRC model is formulated based on the nominal converter model that includes partially known dynamics of the real converter plant, i.e. first order dynamics as appears in (1) and (3). Therefore, the ESO, i.e. the augmented KF, needs to estimate only the rest uncertainties of the nominal converter model, e.g. uncertainties of the filter parameters values, unmodelled higher-order dynamics and non-linearities, etc., additionally to the external disturbances. This reduces the estimation burden of the ESO, which can leave bandwidth margin for the estimation of unknown disturbance dynamics of larger frequency spectrum [68]. This is advantageous especially in the case of converters of the NMP class, which present RHP zeros, limiting the closed-loop bandwidth.

4) LARGE DEGREE-OF-FREEDOM IN CONTROL DESIGN

The L-ADRC model employs the augmented KF as ESO and the LQR as feedback controller, as presented in Section II-C. These elements of the L-ADRC model are designed by determining five parameters, i.e. R_d, τ_d, R_n of the augmented KF and R, q of the LQR. This offers large degree-of-freedom in the design of the voltage controller to fulfil opposing performance requirements.

5) INTEGRATION OF ADDITIONAL CONTROL FUNCTIONS IN VOLTAGE CONTROLLER

The physical significance of the states in the formulation of the nominal converter model in (1) and (3) enables the theoretical analysis of the effect of each element of the L-ADRC model directly on the electrical quantities of the DC/DC converter. Moreover, the formulation of the L-ADRC model based on the converter states with their physical significance as presented in Section II-C allows the integration of additional control functions in the voltage controller, whose concepts rely on the electrical quantities of the DC/DC converter. The VICL as described in Section II-D is integrated in the L-ADRC model thanks to this formulation of the nominal converter model, since its concept relies on the electrical quantities of voltage and current of the DC/DC converter.

6) ADAPTIVE STATE REFERENCE TRAJECTORY

The formulation of the state reference trajectory $\mathbf{x}_{ref}$ in (13) as the update of $\mathbf{x}_{nom}$ through $\mathbf{x}_{adp}$, which follows the dynamics of the real converter plant reflected in the estimated disturbance, provides a smooth state profile to the state feedback controller. This is achieved without the need for computing the derivatives of the output reference signal, as in the TD of the original ADRC, keeping the computation burden of the developed L-ADRC model low, facilitating thus its hardware implementation. Moreover, with this formulation, the state reference trajectory includes the information of the estimated disturbance $\hat{i}_d$, enhancing the robustness of the L-ADRC model against disturbances.

7) SMALL-SIGNAL STABILITY OF CLOSED-LOOP SYSTEM

As it can be seen in (13), the $\mathbf{S}$ and $\mathbf{L}_{adp}$ of the $[x_{ref}, u_{ref}]^T$ are formed through the inverse nominal converter model, which can be also expressed as the transfer function $P^{-1}(s)$, with $P(s) = N(s)/D(s)$. Although the inverse nominal converter model is unstable for converters of the NMP class, as the $N(s)$ is not Hurwitz in this case, the closed-loop system can be designed to be internally stable. This is achieved by designing the characteristic polynomial $D(s)D_L^{FB}(s)+N(s)N_L^{FB}(s)$ of the closed-loop system (22) to be Hurwitz, where $N_L^{FB}(s)$ and $D_L^{FB}(s)$ are the numerator and denominator of the feedback controller C_L^{FB}, respectively. Therefore, the parameters of the LQR and the augmented KF of the L-ADRC model, which are included in the characteristic polynomial, are designed to cancel the internal instability of the inverse nominal converter model of the NMP class. This design approach is similar to that of the disturbance observer-based control for systems of the NMP class [70].

8) LARGE-SIGNAL STABILITY OF CLOSED-LOOP SYSTEM AND PLUG-AND-PLAY CAPABILITY

The large-signal stability of the closed-loop system is proven by taking onto consideration the formulation of the L-ADRC model. The boundedness of the total disturbance and

dynamics of the nominal converter model, the formulation of the reference trajectory and the stability properties of the ESO (augmented KF) and the feedback controller (LQR) fulfil the assumptions for the asymptotic stability of the closed-loop system of the L-ADRC-controlled DC/DC converter [50], [71]. This establishes the theoretical proof of the plug-and-play capability offered by the L-ADRC voltage controller to the DC/DC converter: the closed-loop system is stable for any bounded disturbance, which includes the different disturbances (different operating point, different interactions with other components) in DC power systems of different network topology where the DC/DC converter is integrated, without ad hoc design of the L-ADRC model.

III. DESIGN OF PARAMETERS OF L-ADRC MODEL

This section presents the design of the parameters of the elements of the L-ADRC model. First, the effect of the parameters on the performance of the L-ADRC model under small-signal disturbance is analysed in the frequency domain, by applying it in the nominal models of the buck and boost DC/DC converters. This determines the range of the parameters values for a stable system of each DC/DC converter. Then, the effect of the parameters values, in the predetermined ranges, is investigated under large-signal disturbance in the time domain, by applying the continuous-time L-ADRC model in the switched models of the DC/DC converters in an MTDC distribution grid. The performance analysis in the time domain supplements the performance analysis in frequency domain, by revealing possible dependencies of the design on the model linearisation. By considering the effect of the L-ADRC parameters on the performance in both frequency and time domains, this design process determines their values. Lastly, this design of the L-ADRC model is validated in the hardware implementation, to determine design dependencies on the control digitalisation. The results of the performance analysis in the following sections are computed for the DC/DC converters with nominal parameters of Table 14 in Section VIII.

A. EFFECT OF L-ADRC PARAMETERS ON PERFORMANCE IN FREQUENCY DOMAIN

The performance of the closed-loop system of the nominal model of each DC/DC converter is analysed in cases where the value of one parameter of the L-ADRC model varies, while the rest parameters keep fixed values. The range of value variations of the parameter under study, as well as the fixed values of the rest parameters, are selected for a stable closed-loop system.

In the first case, the value of the covariance R_d of the non-white input disturbance i_d varies. This parameter determines the characteristics of the total disturbance that can be estimated by the augmented KF, and thus the desired disturbance rejection for which the L-ADRC model is designed. Figure 8 presents the magnitude Bode plot of the transfer function G_{yr} of the buck DC/DC converter for different values of R_d. By observing the 0 dB magnitude gain of G_{yr} at low frequencies for all R_d values, it can be concluded that the L-ADRC model achieves tight voltage control, preventing any static error at the steady-state operation of the buck DC/DC converter, thanks to the effective disturbance rejection. Table 1 presents the values of the achieved bandwidth of the closed-loop system, as well as the achieved stability margins (gain margin, phase margin) of the open-loop system, for the different values of R_d of Figure 8. It can be concluded that there is a trade-off in the design of R_d for achieving simultaneously high bandwidth and large stability margins. Moreover, larger values of R_d cause more effective estimation and rejection of the input disturbance d at the steady-state and dynamic operation of the buck DC/DC converter, as observed from the values of the magnitude gain of the transfer function G_{yd} in low and medium frequencies in Figure 9. On the contrary, smaller values of R_d cause lower impact of the measurement noise on the dynamic operation of the converter, as appears in the values of the magnitude gain of the transfer function G_{yn} in medium frequencies in Figure 10. Therefore, there is second trade-off in the design of the R_d parameter, for achieving accurate estimation and effective rejection of the input disturbance, while simultaneously suppressing the measurement noise. Same trade-off for the design of the R_d parameter is found also in the case of the boost DC/DC converter. Similar conclusions can be drawn for the design of the R_v and τ_d parameters that affect the performance of the augmented KF and thus of the L-ADRC model.

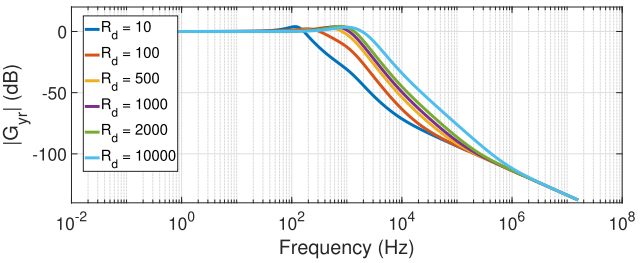

FIGURE 8. $|G_{yr}|$ Bode plot of closed-loop system of buck DC/DC converter for varying value of parameter R_d [A^2].

TABLE 1. Bandwidth and stability margins of buck DC/DC converter with L-ADRC voltage controller for varying value of parameter R_d.

R_d [A^2]	Bandwidth [Hz]	Gain Margin [dB]	Phase Margin [°]
10	191	158	100.10
100	439	11	64.12
500	1041	5	44.52
1000	1325	5	39.75
2000	1616	4	37.32
10000	2338	7	41.40

In the second case, the value variations are performed for the parameter R of the LQR feedback controller, which is

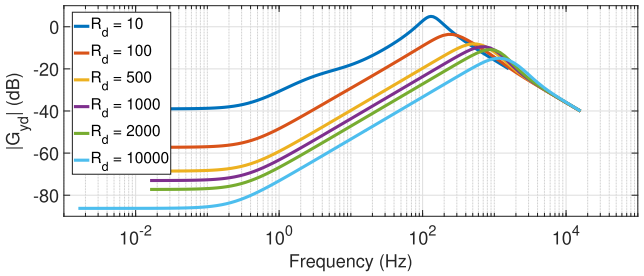

FIGURE 9. $|G_{yd}|$ Bode plot of closed-loop system of buck DC/DC converter for varying value of parameter R_d [A^2].

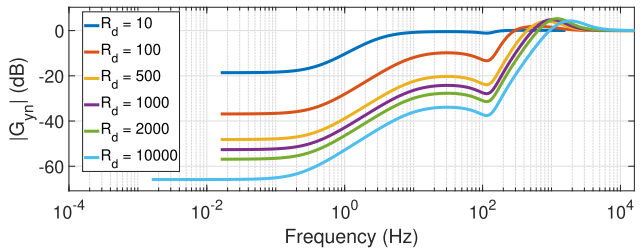

FIGURE 10. $|G_{yn}|$ Bode plot of closed-loop system of buck DC/DC converter for varying value of parameter R_d [A^2].

related to the dynamic performance of the L-ADRC model. Figure 11 presents the magnitude Bode plot of the transfer function G_{yr} of the boost DC/DC converter for different values of R. All values of R provide tight voltage control at the steady-state operation of the converter, as it can be concluded from the 0 dB magnitude gain of G_{yr} at low frequencies. Table 2 presents the achieved bandwidth and stability margins for the different values of R of Figure 11. It can be seen that an optimal value of R can be found with regard to the bandwidth, whereas the stability margins decrease with increasing R. On the other hand, larger values of R cause less effective rejection of the input disturbance in the low and medium frequencies, as it can be seen in Figure 12, and larger impact of the measurement noise on the dynamic performance, as observed in Figure 13. Hence, there is a trade-off also for the design of R, for achieving large stability margins with effective disturbance and noise rejection. However, it should be noticed that the different values of R do not change strongly the performance of the closed-loop system, implying that there is no need for excessive effort to compromise this design trade-off. Similar observations can be made also for the design of R in the case of the buck DC/DC converter, as well as for the design of the q parameter of the LQR feedback controller for both DC/DC converters.

B. EFFECT OF L-ADRC PARAMETERS ON PERFORMANCE IN TIME DOMAIN

In this section, the effect of the L-ADRC parameters on the performance of the switched converter model of the DC/DC converters is analysed in cases of values variations.

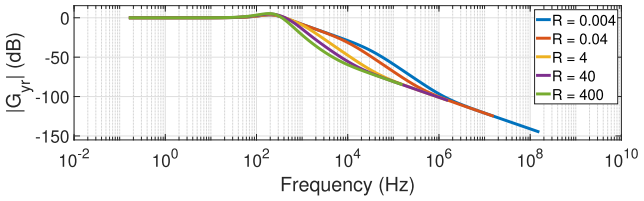

FIGURE 11. $|G_{yr}|$ Bode plot of closed-loop system of boost DC/DC converter for varying value of parameter R.

TABLE 2. Bandwidth and stability margins of boost DC/DC converter with L-ADRC voltage controller for varying value of parameter R.

R	Bandwidth [Hz]	Gain Margin [dB]	Phase Margin [°]
0.004	557	4	47.21
0.04	560	4	46.81
4	580	3	43.47
40	533	3	40.35
400	425	2	39.10

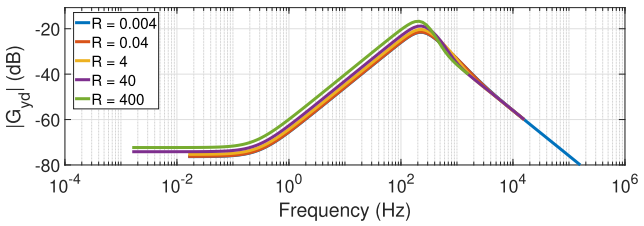

FIGURE 12. $|G_{yd}|$ Bode plot of closed-loop system of boost DC/DC converter for varying value of parameter R.

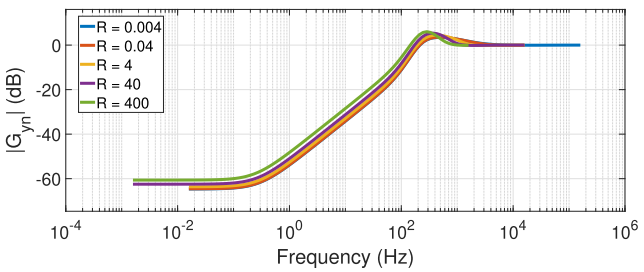

FIGURE 13. $|G_{yn}|$ Bode plot of closed-loop system of boost DC/DC converter for varying value of parameter R.

Figure 14 illustrates the LV three-terminal DC distribution grid simulated for the performance analysis in the time domain. The nominal voltage and the line parameters are mentioned in Table 3. The switched models of the three converters involve an IGBT+diode configuration and a PWM. The buck DC/DC converter at T_1 and the boost DC/DC converter at T_3 operate as DC grid-forming converters in the grid, employing the developed L-ADRC model for the voltage control. The filter parameters of the switched converter models are the same as for their nominal models, mentioned in Section II-A. The load-interfacing buck DC/DC converter at T_2 employs PID current controller, behaving thus as a CPL [72], [73], [74]. Table 4 presents the filter

parameters of the load-interfacing buck DC/DC converter and the second-order transfer function of its PID current control, designed for crossover frequency $f_{cr} = 1700$ Hz and phase margin 90° [75]. The voltage and power/current set-points of the aforementioned controllers are provided by a power flow algorithm.

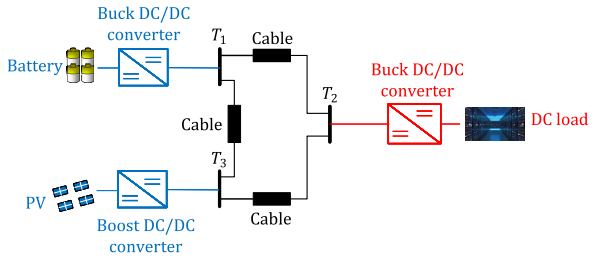

FIGURE 14. Three-terminal LVDC distribution grid.

TABLE 3. Parameters of three-terminal DC grid.

Parameter [Units]	Value
Nominal Voltage V_{grid} [V]	760
Line Resistance R_l [Ω/km]	0.12
Line Inductance L_l [H/km]	400e-6
Line Capacitance C_l [F/km]	0.5e-6
Length of line T_1-T_2 [km]	2.07
Length of line T_1-T_3 [km]	1.2
Length of line T_2-T_3 [km]	1

TABLE 4. Parameters of nominal buck DC/DC converter and PID current controller of CPL.

Parameter [Units]	Value
V_{in} [V]	900
L [H]	1.6e-3
R_L [Ω]	0.1
C [F]	850e-6
R_C [Ω]	0.05
R_{Ld} [Ω]	1
f_{sw} [kHz]	10
PID current controller	$\frac{3.2614e-06s^2+0.0022s+2.4566}{1.4429s^2+s}$

In the simulation scenario for the performance analysis, the load increases by 0.5 p.u. at time $t = 0.25$ s. In the first case, the value of the covariance R_d varies, whereas the rest parameters of the L-ADRC model keep fixed values, suitable for a stable system. Figure 15 presents the output voltage of the buck DC/DC converter at T_1 in this case of the simulation scenario. It can be observed that larger values of R_d cause smaller voltage undershoot and oscillations with smaller amplitude after the disturbance, leading to faster stabilisation with better dynamic performance. This conclusion of the performance analysis in the time domain agree with that in the frequency domain in Section III-A, since larger values of R_d offer better dynamic performance thanks to more effective disturbance rejection and larger bandwidth. However, to achieve this, larger control input (duty cycle) is required when R_d values increase, as it can be observed in Figure 16. As a result, there is a trade-off in the design of the parameter R_d to compromise good dynamic performance with the practical restrictions of the control input. This is an additional design trade-off to these mentioned in the analysis in the frequency domain in Section III-A. Therefore, the analysis in the time domain supports the analysis in the frequency domain revealing the effect of the parameters on the performance regarding different requirements indicators. Similar conclusions can be drawn for the design of R_d in the L-ADRC model of the boost DC/DC converter at T_3 of the simulated DC distribution grid, as well as for the design of R_v and τ_d of the augmented KF in the L-ADRC model of both buck and boost DC/DC converters.

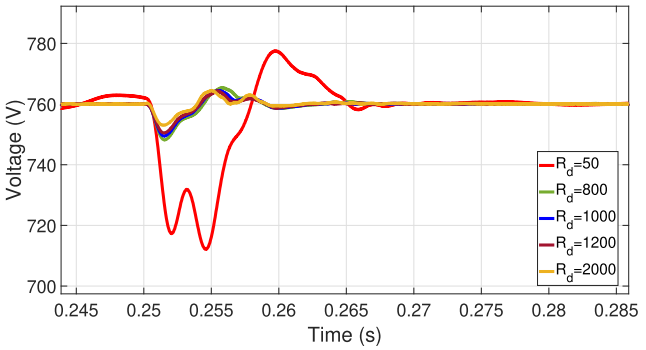

FIGURE 15. Output voltage of buck DC/DC converter in three-terminal DC distribution grid in scenario of load disturbance for varying value of parameter R_d [A^2].

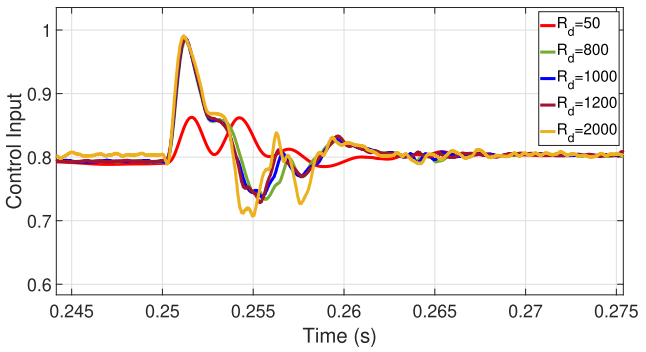

FIGURE 16. Control input of buck DC/DC converter in three-terminal DC distribution grid in scenario of load disturbance for varying value of parameter R_d [A^2].

In the second case of the simulation scenario, the values of the R and q parameters of the LQR feedback controller of the L-ADRC model vary simultaneously, while the rest parameters present fixed values. Figure 17 presents the output

voltage of the buck DC/DC converter at T_1 in this simulation case. It can be observed that, as q increases and R decreases, the output voltage presents better dynamic performance, with smaller undershoot, oscillations with smaller amplitude and shorter settling time. However, this is achieved with larger control input, which reaches almost the saturation limit of the duty cycle, as illustrated in Figure 18. Moreover, the peak of the output current after the disturbance increases, with increasing q and decreasing R values, as it can be observed in Figure 19. These observations agree with the analysis in Section II-C3. Therefore, the performance analysis in the time domain validates the theoretical analysis regarding the need for a current limiter, to keep the peak current low, when the LQR parameters are designed for effective voltage control. Similar conclusions about the effect of the LQR parameters on the performance of the L-ADRC model in the boost DC/DC converter at T_3 can be derived, matching the theoretical analysis in Section II-C3.

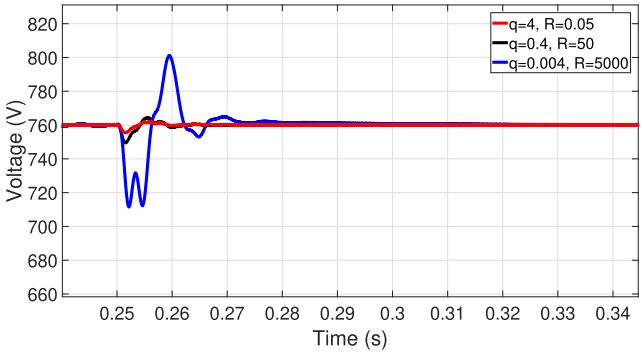

FIGURE 17. Output voltage of buck DC/DC converter in three-terminal DC distribution grid in scenario of load disturbance for varying value of parameters q and R.

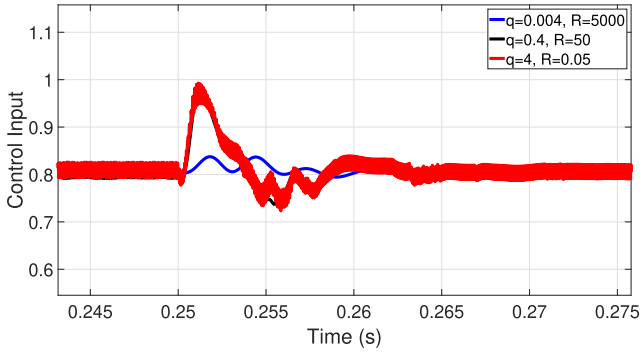

FIGURE 18. Control input of buck DC/DC converter in three-terminal DC distribution grid in scenario of load disturbance for varying value of parameters q and R.

C. EFFECT OF VICL PARAMETERS ON PERFORMANCE IN TIME DOMAIN

The effect of the parameter I_{thres} of the VICL integrated in the L-ADRC model is investigated under large-signal disturbance in time domain. The parameter I_{max} of the

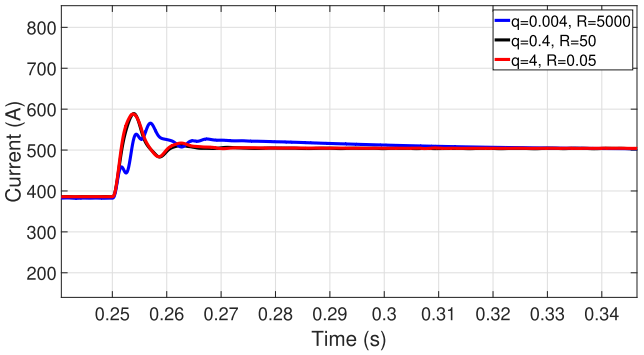

FIGURE 19. Output current of buck DC/DC converter in three-terminal DC distribution grid in scenario of load disturbance for varying value of parameters q and R.

VICL remains constant according to the size of the DC/DC converters in the MTDC grid, as it is not a control parameter, but rather a physical characteristic.

In the simulation scenario, the VICL is integrated to the L-ADRC model of the boost DC/DC converter at T_3 and the value of I_{thres} of the L-ADRC+VICL model varies, while the rest parameters keep fixed values. Figure 20 and Figure 21 present the output current and output voltage of the boost DC/DC converter with the L-ADRC model and the L-ADRC+VICL model for three different values of I_{thres} in the same simulation scenario. It can be observed that with the L-ADRC+VICL model with $I_{thres} = 620$ A the current peak decreases by 3.5%, while the voltage undershoot/overshoot increase by $3 - 4\%$, in comparison to the performance of the L-ADRC model. When the VICL parameter increases to $I_{thres} = 625$ A, the current peak decreases only by 0.3%, although the output voltage is already degraded by $1 - 2\%$ with regard to the performance of the L-ADRC model. When the VICL parameter decreases to $I_{thres} = 618$ A, the current peak decreases by 3.5%, but the voltage overshoot increases by 6% compared to the performance of the L-ADRC model. It can be concluded that there is a range of I_{thres} values, for which the VICL exhibits a advantageous relation between the benefit of the decrease of the current peak and the cost of the increase of the oscillations amplitude in the voltage. Beyond this range of the I_{thres} values, this behaviour is lost, with the cost of the degradation of the voltage control being larger than the benefit of the peak current limitation. It should be noticed that, for all values of the parameter I_{thres}, the VICL affects the performance of the L-ADRC+VICL model only at the transients after the load disturbance, to prevent high currents at the switches of the DC/DC converter. The stabilisation of the output voltage is not affected, presenting similar oscillatory behaviour (similar frequency and damping of oscillations) and the same settling time as with the L-ADRC model, which agrees with the conclusion in [53].

D. VALIDATION OF L-ADRC MODEL IN HARDWARE IMPLEMENTATION

The values of the parameters are determined, taking into account the aforementioned design trade-offs, the combined

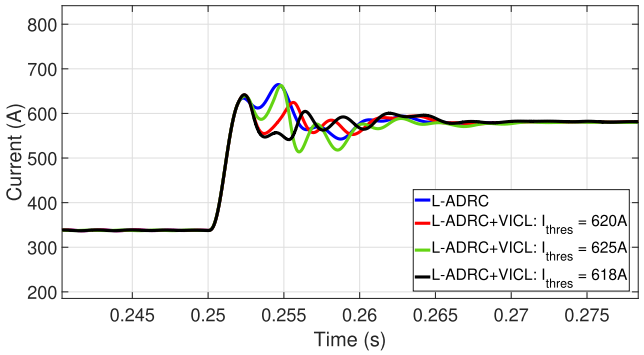

FIGURE 20. Output current of boost DC/DC converter in three-terminal DC distribution grid in scenario of load disturbance for L-ADRC and L-ADRC+VICL control models.

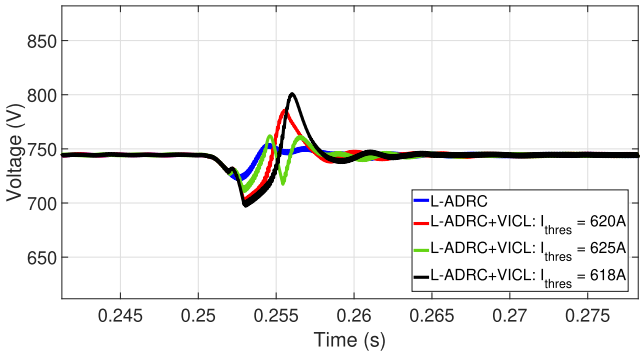

FIGURE 21. Output voltage of boost DC/DC converter in three-terminal DC distribution grid in scenario of load disturbance for L-ADRC and L-ADRC+VICL control models.

effect of all parameters on the performance of the controller and the mutually-affected design of certain parameters due to their relations. The values of the parameters of the L-ADRC model for buck and boost DC/DC converters are provided in Table 5.

TABLE 5. Parameters of L-ADRC model for buck and boost DC/DC converters.

L-ADRC Parameter [Units]	Buck Converter	Boost Converter
R_d [A^2]	1000	1000
τ_d [s]	0.4	0.5
R_v [V^2]	0.01	0.01
R	50	4
q	0.4	0.05

The design is validated through the hardware implementation of the L-ADRC model in the HiL set-up of Figure 22. The models of DC/DC converters, LC filters and lines in the three-terminal DC distribution grid of Section III-B are implemented in the field programmable gate array (FPGA) of the OPAL-RT OP5707 target and simulated through the electrical hardware solver (eHS) with simulation time step of $T_s = 215$ ns. The PWM of the CPL converter is also implemented in the FPGA of this OPAL-RT target, with single update of the duty cycle at each time step and symmetrical (triangular) carrier, whereas its PID current controller, discretised with time step $T_d = 50$ μs, is implemented in the central processing unit (CPU) of the OPAL-RT target. The PWM of the DC grid-forming buck and boost converters are implemented in the FPGA of the OPAL-RT OP4510 target, in the same modelling approach as the PWM of the buck DC/DC converter of the CPL, while their discrete-time L-ADRC voltage controllers are implemented in the CPU of this OPAL-RT target. For this, the discrete-time augmented KF and LQR are applied in the continuous-time converter models, with discretisation time step $T_d = 50$ μs, by using the parameters of the continuous-time L-ADRC model presented above. In addition, the nominal converter models are discretised with time step $T_d = 50$ μs following the ZOH discretisation method and solved at the steady-state operation to derive the discrete-time model of the RTG. The L-ADRC voltage controllers in OPAL-RT OP4510 target receive analog signals of voltage measurements from the DC grid-forming converters in the OPAL-RT OP5707 target. The PWM of the DC grid-forming converters in OPAL-RT OP4510 target provide back the digital signals of the switching pulses to the gates of these DC/DC converters in OPAL-RT OP5707 target. The measurement sampling and A/D conversion at the OPAL-RT OP4510 target are triggered at the beginning and middle time-points of the PWM period of the two DC/DC converters, synchronising thus the measurement sampling with the switching process, for obtaining more accurate average values without oscillations.

For a more realistic operation of the HiL set-up, a shift of 40 μs between the two PWMs of the DC/DC converters in the FPGA of the OPAL-RT OP4510 target is employed. In addition, the PWM sampling of these two converters in OPAL-RT OP4510 target is not aligned with the PWM sampling of the CPL converter in OPAL-RT OP5707 target, due to the random time instant when the execution of the two targets of the HiL set-up starts. In this way, the PWM pulses of the three DC/DC converters are not synchronised, as it occurs also in practice in the real-world operation between individual DC/DC converters in a DC grid.

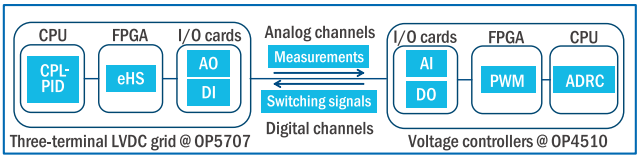

FIGURE 22. HiL set-up.

The HiL test simulates the operation of the three-terminal DC grid in a scenario of load increase by 50% at $t = 0.2$ s. Four different variants of the random shift between the PWM signals of the DC grid-forming converters and the CPL converter are simulated, by repeating the same simulation four times for a random start of the two targets. In this way, the design of the L-ADRC model is validated

in a realistic hardware implementation and execution. The results of the HiL simulations are compared with these of the offline time simulation with the discretised L-ADRC model, to analyse the discrepancies of the performance due to the hardware implementation. Figure 23 and Figure 24 present the output voltage of the buck and boost DC/DC converters in these simulations, respectively. It can be observed that the discrepancies between the HiL and the offline simulations are different for the different PWM shift variants. However, these discrepancies are very small for all variants, with the largest being 0.4% in the case of the buck DC/DC converter and 0.5% in the case of the boost DC/DC converter. Similar small discrepancies between the HiL and offline simulations are observed in the output current and duty cycle of both DC/DC converters. It can be concluded that the delays due to the control cycle execution in the hardware and the involved noise in the signal transfer do not affect the performance of the voltage controller. The performance of the L-ADRC model at the hardware implementation presents the same features as in the offline simulations, which validates its design.

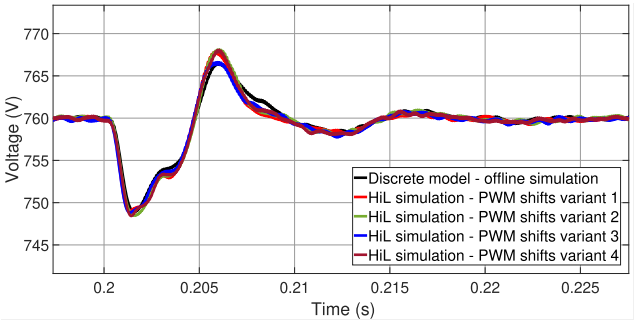

FIGURE 23. Output voltage of buck DC/DC converter in three-terminal DC distribution grid under four cases of HiL tests.

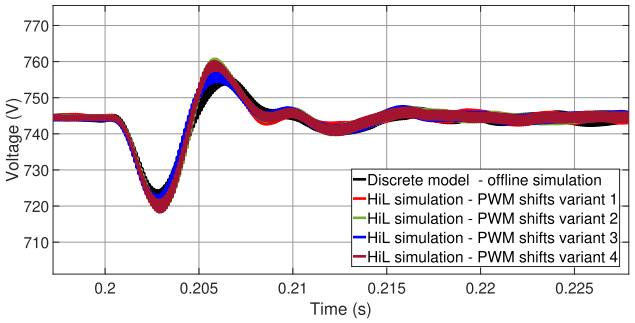

FIGURE 24. Output voltage of boost DC/DC converter in three-terminal DC distribution grid under four cases of HiL tests.

IV. FUNCTIONALITY OF L-ADRC MODEL

In this section, internal signals of the L-ADRC structure are presented to discuss the functionality of the developed voltage controller to estimate and reject the total disturbance. These quantities are presented for the L-ADRC model applied in the buck and boost DC/DC converters of the DC grid of Figure 14 with the control parameters of Table 5 under a load increase by 0.5 p.u. at time $t = 0.25$ s.

Figure 25 presents the estimated total disturbance $\hat{i}_d$ as output of the augmented KF of the L-ADRC model of the buck converter at T_1 of the DC grid and Figure 26 presents the adaptation term u_{adp} of the control input of the L-ADRC model. It can be observed that the u_{adp} follows the dynamics of the $\hat{i}_d$ as indicated in (13). Figure 27 presents the different terms of the control input of the L-ADRC model. It can be noticed that the u_{ref} generated by the RTG follows the dynamics of the u_{adp} around the u_{nom}, as appears in (13), i.e. the u_{adp} conforms the u_{nom} according the estimated total disturbance. The control input u_L follows the dynamics of the u_{LQR}, determining the dynamic performance of the L-ADRC model, shifted by the u_{ref} to reject the total disturbance, as appears in (15).

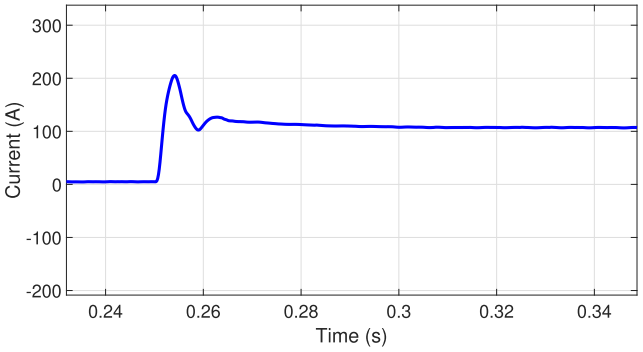

FIGURE 25. Estimated total disturbance $\hat{i}_d$ of buck DC/DC converter under load increase.

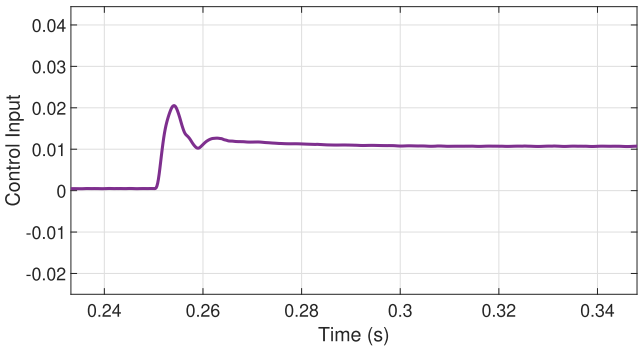

FIGURE 26. Adaptation term u_{adp} of control input of buck DC/DC converter under load increase.

Figure 28 presents the adaptation term $v_{C_{adp}}$ of the state of the capacitor voltage of the L-ADRC model, which follows the dynamics of the estimated total disturbance $\hat{i}_d$, according to (13). The $v_{C_{ref}}$ generated by the RTG follows the dynamics of the $v_{C_{adp}}$ around the $v_{C_{nom}}$ according to (13), as appears in Figure 29. It can be also seen that the $\hat{v}_C$ is regulated at the steady state to the $v_{C_{ref}}$ by the LQR feedback controller of the L-ADRC model. The dynamics of the $\hat{v}_C$ follow the dynamics of the v_o, assuming small voltage drop at the parasitic resistance of the filter capacitor, as it can be seen in

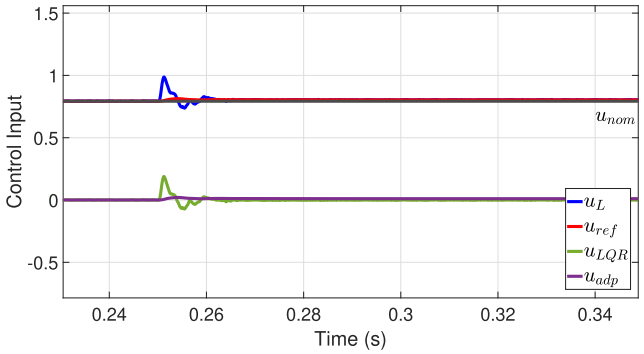

FIGURE 27. Terms of control input of buck DC/DC converter under load increase.

Figure 30. However, the $\hat{v}_C$ differs from the v_o at the steady state, because the v_o is controlled to the nominal voltage thanks to the feedforward term u_{ref} for the disturbance rejection.

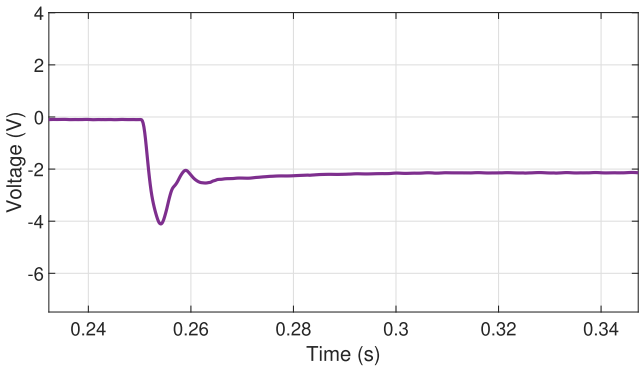

FIGURE 28. Adaptation term $v_{C_{adp}}$ of capacitor voltage state of buck DC/DC converter under load increase.

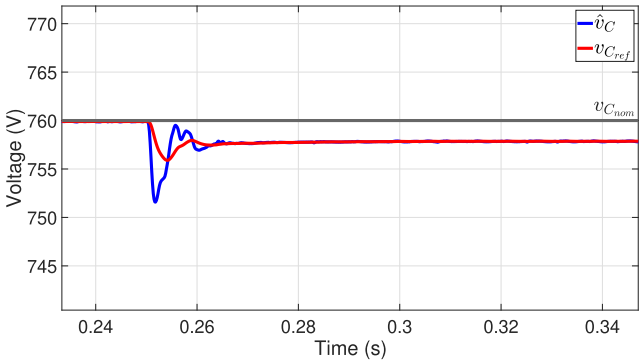

FIGURE 29. Terms of capacitor voltage state of buck DC/DC converter under load increase.

V. PERFORMANCE COMPARISON OF L-ADRC MODEL WITH PID CONTROL

In this section, the performance of the L-ADRC model is compared with this of the PID control, when both

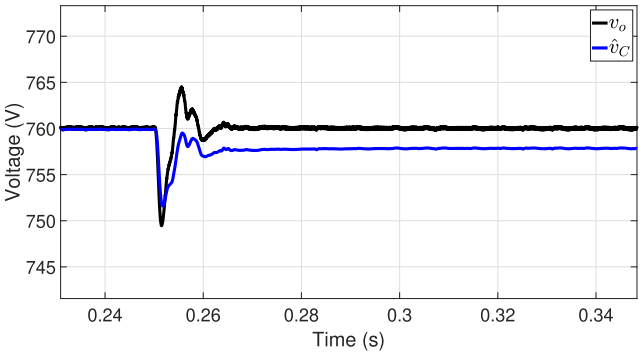

FIGURE 30. Estimated capacitor voltage state and measured output voltage of buck DC/DC converter under load increase.

TABLE 6. Gains of PID voltage controller for buck and boost DC/DC converters.

PID Gain	Buck DC/DC converter	Boost DC/DC converter
k_{p_v}	0.008	$5 \cdot e^{-4}$
k_{i_v}	9	0.5
k_{d_v}	$1.1 \cdot e^{-5}$	$7.5 \cdot e^{-6}$

are applied as voltage controllers in the buck and boost DC/DC converters with nominal parameters of Table 14 in Section VIII. The parameters of the L-ADRC model for both converters present the values mentioned in Section III. The gains of the PID voltage controller of the buck and boost DC/DC converters are provided in Table 6. Opposite to the design process for the L-ADRC model, where both frequency and time domains are considered supplementarily, for the design of the PID controller the frequency domain is not considered, as it provides PID gains that lead to unacceptable performance in the time domain. The discrepancies between small-signal analysis with the linearised closed-loop system and large-signal analysis with the non-linear model of the DC/DC converter applied in a multi-converter grid cannot be mitigated by the PID controller, as in the case of the L-ADRC model. Therefore, the PID gains are determined through tuning under large-signal disturbances in time simulations, when this control is applied to the buck and boost DC/DC converters of the three-terminal DC distribution grid of Section III-B. The PID gains are tuned to provide voltage control performance, in terms of under-/overshoot and settling time, that is similar to this of the L-ADRC model under the same load disturbance scenario in the three-terminal DC grid. For this design of the voltage controllers, their performance is then compared in frequency and time domains, to reveal the beneficial features of the L-ADRC model against the PID controller considering other performance indicators, such required current injection and duty cycle change to achieve the voltage control, or plug-and-play capability offered to the DC/DC converters.

A. COMPARISON IN FREQUENCY DOMAIN

1) OPEN-LOOP GAIN, STABILITY MARGINS, AND BANDWIDTH

Figure 31 presents the Bode plots of the open-loop system of the buck DC/DC converter with PID and L-ADRC voltage controllers. In comparison to the PID controller, the L-ADRC model presents larger positive loop gain at frequencies of $60 - 300$ Hz during the dynamic operation of the converter while dealing with disturbances, whereas its loop gain decreases drastically to negative values in frequencies larger than the bandwidth of the controller ($\sim$ 2000 Hz) for stronger disturbance/noise attenuation. The L-ADRC voltage controller provides the control effort in a more efficient way than the PID voltage controller, when this is needed to handle the disturbances [42]. This benefit is more clear in the case of the boost DC/DC converter, since the PID controller is not suitable for NMP systems, as mentioned in Section I. This is illustrated in Figure 32, which presents the Bode plots of the open-loop system of the boost DC/DC converter for the two voltage controllers. The open-loop gain of the PID controller decreases in medium frequencies, whereas the gain of the L-ADRC model remains large, indicating the suitability of the developed voltage controller to stabilise properly the voltage of the boost DC/DC converter.

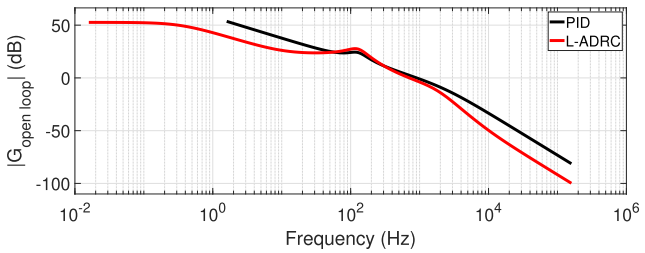

FIGURE 31. Magnitude Bode plot of open-loop system of buck DC/DC converter with L-ADRC and PID controllers.

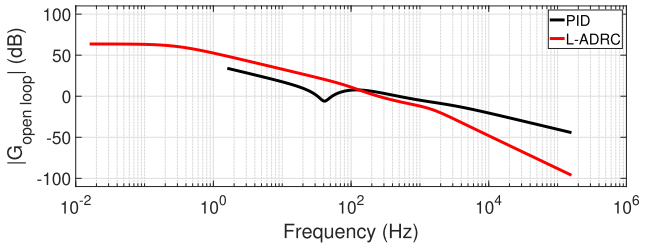

FIGURE 32. Magnitude Bode plot of open-loop system of boost DC/DC converter with L-ADRC and PID controllers.

Table 7 and Table 8 present the achieved bandwidth and stability margins of the buck and boost DC/DC converters, respectively, in the cases of the L-ADRC model and the PID controller. In the case of the buck DC/DC converter, the L-ADRC model achieves similar bandwidth as the PID controller, but with smaller stability margins. However, also in the case of the L-ADRC model, the phase margin, which is more crucial for the stability assessment [76], is still above the critical value of 30°, which can cause the closed-loop system to have substantial ringing when subjected to disturbances [76], [77]. On the other hand, in the case of the boost DC/DC converter, the L-ADRC model manages to compromise acceptable stability margins with good control bandwidth, opposite to the PID controller, which presents good stability margins but at the cost of very low bandwidth.

TABLE 7. Bandwidth and stability margins of buck DC/DC converter with L-ADRC and PID controllers.

Control	Bandwidth [Hz]	Gain Margin [dB]	Phase Margin [°]
L-ADRC	1325	5	39.75
PID	1637	∞	63.31

TABLE 8. Bandwidth and stability margins of boost DC/DC converter with L-ADRC and PID controllers.

Control	Bandwidth [Hz]	Gain Margin [dB]	Phase Margin [°]
L-ADRC	580	3	43.47
PID	33	3	72.39

2) ROBUSTNESS AGAINST CONVERTER MODEL UNCERTAINTIES

For assessing the capability of the two voltage controllers to handle converter model uncertainties, their performance is investigated for varying value of the filter capacitance of the buck DC/DC converter by 7.5 times, according to similar practice in [78]. The rest parameters of the nominal converter model and the control parameters keep the values mentioned above.

Table 9 and Table 10 present the changes in the gain and phase margins of the buck DC/DC converter due to the capacitance variations in the cases of the L-ADRC model and the PID controller, respectively. It can be seen that the gain margin varies strongly for both controllers. However, the phase margin remains almost the same in the case of the L-ADRC model, with maximum change of only around 2%, whereas it changes by around 60% in the case of the PID controller. Therefore, the L-ADRC model is more robust to the filter capacitance uncertainties than the PID controllers regarding the phase margin, which is more crucial for the stability assessment [76].

The changes in the capability of the L-ADRC model for disturbance rejection due to the variations of the filter capacitance are illustrated in Figure 33, which presents the magnitude Bode plots of G_{yd} of the closed-loop system of the buck DC/DC converter. The largest variation of the $|G_{yd}|$ is 23 dB occurring in medium frequencies around 1 kHz. This is regarded as small variation of $|G_{yd}|$, considering the variation of the filter capacitance by 7.5 times. Therefore, the L-ADRC maintains its capability for disturbance rejection despite the

TABLE 9. Stability margins of buck DC/DC converter with L-ADRC voltage controller for varying value of C_{buck}.

C_{buck} [F]	Gain Margin [dB]	Phase Margin [°]
0.0008	3	36.6
0.001	5	39.75
0.002	15	40.89
0.004	∞	36.55
0.006	∞	34.01

TABLE 10. Stability margins of buck DC/DC converter with PID voltage controller for varying value of C_{buck}.

C_{buck} [F]	Gain Margin [dB]	Phase Margin [°]
0.0008	∞	60.20
0.001	∞	63.31
0.002	∞	68.36
0.004	0.4	56.15
0.006	1	23.64

converter model uncertainties. The PID controller does not offer disturbance rejection in low and medium frequencies of the converter operation, as the input disturbance is not considered during its design. However, the way it deals with the disturbance is also affected strongly from the variations of the filter capacitance, as it appears in Figure 34. The most important effect is the change by 3 kHz of the frequency, at which it starts providing disturbance/noise rejection.

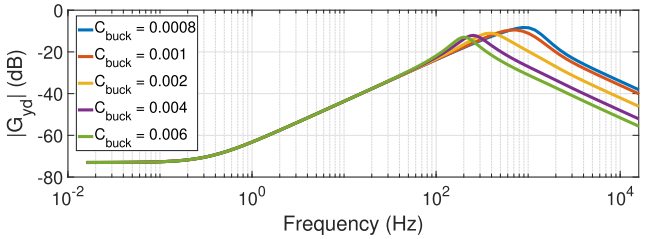

FIGURE 33. $|G_{yd}|$ of closed-loop system of buck DC/DC converter with L-ADRC voltage controller for varying value of filter capacitance C_{buck} [F].

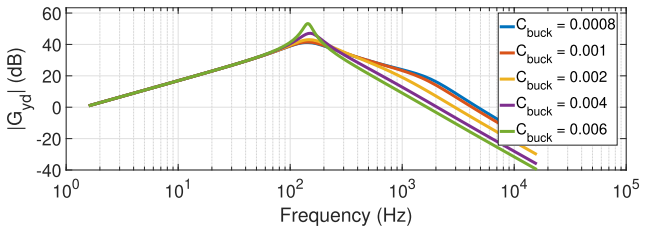

FIGURE 34. $|G_{yd}|$ of closed-loop system of buck DC/DC converter with PID voltage controller for varying value of filter capacitance C_{buck} [F].

The effect of the filter capacitance variations on the noise attenuation of the two voltage controllers is illustrated in Figure 35 and Figure 36, which present the magnitude Bode plots of G_{yn} of the closed-loop system of the buck DC/DC converter in the case of the L-ADRC model and the PID controller, respectively. It can be observed that the uncertainties of the filter capacitance affect the frequencies at which the noise amplification occurs for both controllers. However, this effect is smaller in the case of the L-ADRC model than in the case of the PID controller. As a result, the L-ADRC model presents higher insensitivity to filter capacitance variations for the attenuation of the measurement noise.

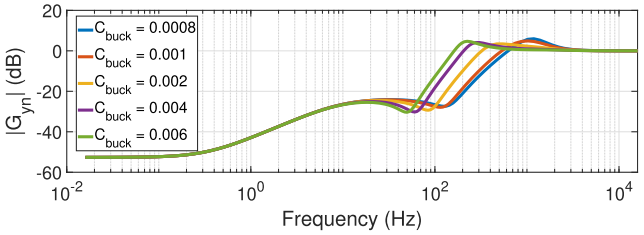

FIGURE 35. $|G_{yn}|$ of closed-loop system of buck DC/DC converter with L-ADRC voltage controller for varying value of filter capacitance C_{buck} [F].

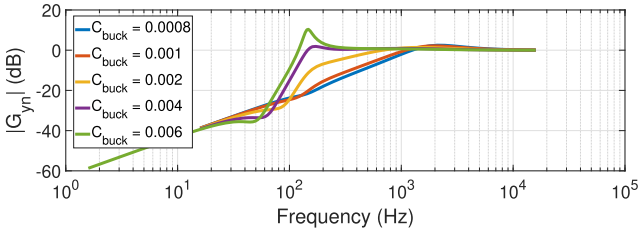

FIGURE 36. $|G_{yn}|$ of closed-loop system of buck DC/DC converter with PID voltage controller for varying value of filter capacitance C_{buck} [F].

B. COMPARISON IN TIME DOMAIN

1) REJECTION OF EXTERNAL DISTURBANCE

The scenario of the load increase by 0.5 p.u. at $t = 0.25$ s in the three-terminal DC distribution grid of Section III-B is simulated in the cases of the two voltage controllers. Figure 37 presents the output voltage of the buck DC/DC converter at T_1 of the grid for the two controllers. It can be observed that the dynamics of the voltage control for both controllers is comparable, requiring similar increase of the control input after the disturbance, as appears in Figure 38. Moreover, the control input signal is less noisy in the case of the L-ADRC model than in the case of the PID controller, which agrees with the analysis in the frequency domain in Section V-A1, according to which the open-loop gain of the L-ADRC model decreases drastically in high frequencies, achieving suppression of the noise in the provided control effort. In addition, in the case of the L-ADRC model the good performance of the voltage control is achieved by causing a current overshoot smaller by 20% than in the case of the PID controller, as illustrated in Figure 39. Similar conclusion for the comparable dynamic performance of the two controllers

can be also drawn in the case of the boost DC/DC converter at T_3 of the grid. This occurs due to the tuning of the parameters of both controllers according to their performance in the time domain, by implementing them in the converters of this three-terminal DC grid.

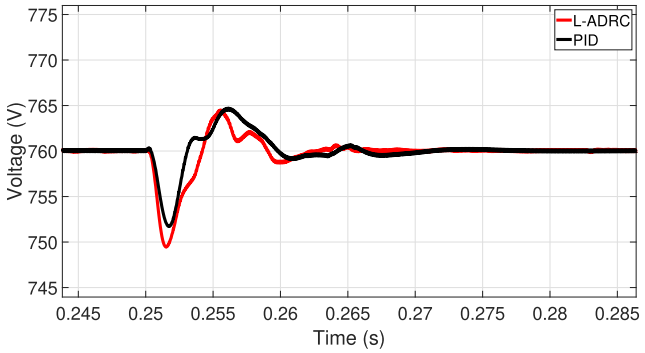

FIGURE 37. Output voltage of buck DC/DC converter in three-terminal DC distribution grid under load disturbance for L-ADRC and PID voltage controllers.

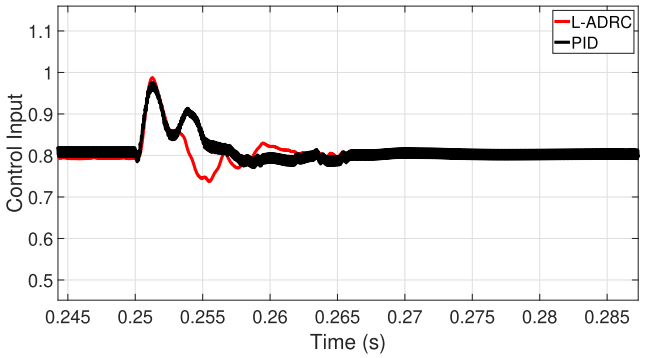

FIGURE 38. Control input of buck DC/DC converter in three-terminal DC distribution grid under load disturbance for L-ADRC and PID voltage controllers.

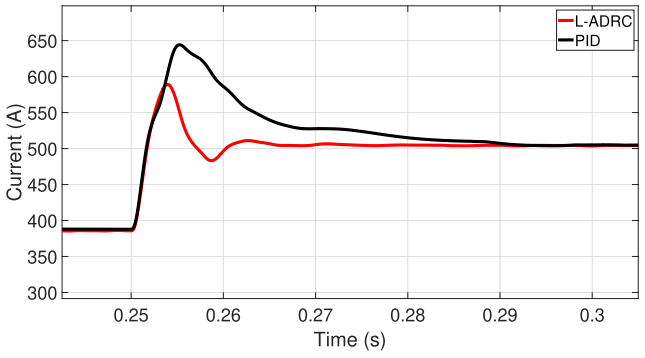

FIGURE 39. Output current of buck DC/DC converter in three-terminal DC distribution grid under load disturbance for L-ADRC and PID voltage controllers.

2) REJECTION OF DIFFERENT GRID INTERACTIONS AND PLUG-AND-PLAY CAPABILITY

For assessing their plug-and-play capability, the two voltage controllers are applied to the DC grid-forming converters of a five-terminal DC grid of the same nominal voltage as the DC grid in the previous sections, without any prior design modification. This assesses the ability of the controllers to handle the different external disturbances in the new grid, due to the different interactions between different number of converters integrated in a DC power system of a different topology.

Figure 40 presents the five-terminal DC grid. The line parameters are the same as in the three-terminal DC grid, whereas their lengths are mentioned in Table 11. The DC/DC converters are simulated through the same switched models as in the three-terminal DC distribution grid, with the same filter parameters. The DC grid-forming converters at terminals T_1, T_2, T_4 and T_5 employ the voltage controllers, whereas the load-interfacing DC/DC converter at T_3 operates as a CPL, with the same PID current controller as in the three-terminal DC grid. The voltage and power/current set-points of the converter controllers are provided by a power flow algorithm for the five-terminal DC grid.

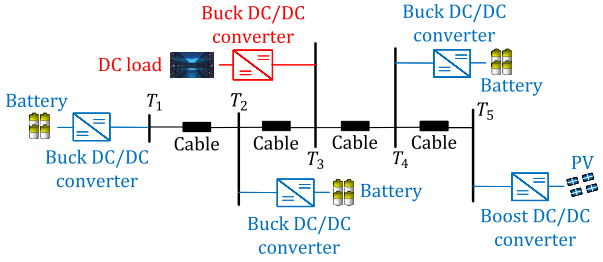

FIGURE 40. Five-terminal LVDC distribution grid.

TABLE 11. Length of lines in five-terminal DC grid.

Parameter	Value
Length of line T_1-T_2 [km]	1.25
Length of line T_2-T_3 [km]	1
Length of line T_3-T_4 [km]	1.2
Length of line T_4-T_5 [km]	0.6

The same scenario of load disturbance is simulated as in the three-terminal DC grid in the previous section. Figure 41 presents the output voltage of the buck DC/DC converter at T_2 of the grid in the cases of the two voltage controllers. Opposite to the PID voltage controller, the L-ADRC model exhibits in the five-terminal grid similar dynamic performance as in the three-terminal grid discussed in the previous section, without any design modification. Similarly, the L-ADRC model manages to control the output voltage of the boost DC/DC converter at T_5 of the five-terminal DC grid without any design modification, as appears in Figure 42. On the contrary, the PID controller does not achieve to control the output voltage of the boost DC/DC converter in the five-terminal grid: it requires large increase in the duty cycle, beyond the critical value, which

causes inversion of the conversion gain v_o/V_{in}, as appears in Figure 43 [79], [80].

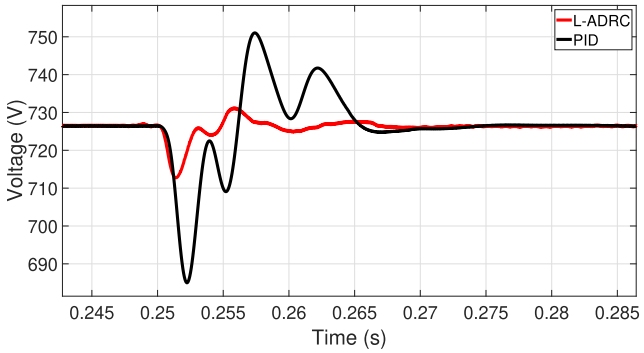

FIGURE 41. Output voltage of buck DC/DC converter in five-terminal DC distribution grid under load disturbance for L-ADRC and PID voltage controllers.

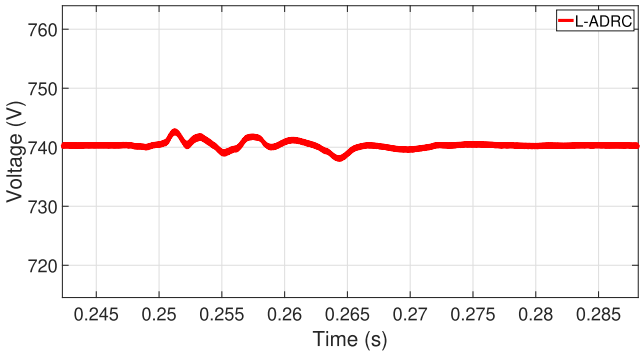

FIGURE 42. Output voltage of boost DC/DC converter in five-terminal DC distribution grid under load disturbance for L-ADRC voltage controller.

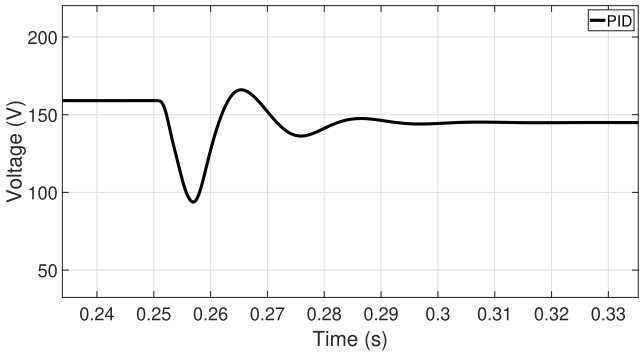

FIGURE 43. Output voltage of boost DC/DC converter in five-terminal DC distribution grid under load disturbance for PID voltage controller.

The L-ADRC model can provide plug-and-play capability to the DC/DC converters, thanks to the estimation and rejection of the total disturbance d, which includes the unknown external disturbances due to the components' interactions that are different in the two DC grids. This feature implies also that the DC power system used for the design of the parameters of the L-ADRC model in the time domain can be an exemplary network model of the same nominal voltage of the real grid. A detailed model of the grid with all components is not required. Opposite to this, the PID controller does not provide plug-and-play capability, since the total disturbance is not taken into account in its design. Therefore, its tuning should be performed for the real converter plant integrated in the real grid together with other components.

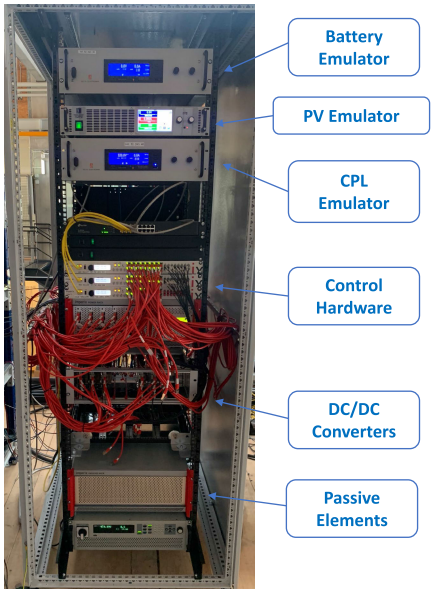

FIGURE 44. Lab set-up.

VI. PERFORMANCE VALIDATION OF L-ADRC MODEL IN A LAB SET-UP

In this section, the performance of the L-ADRC model is validated with the real DC/DC converters in a lab set-up within the Smart Energy System Control Laboratory [81]. The lab set-up consists of the elements presented in Figure 44 representing the three-terminal DC grid of Figure 14. The battery and the CPL, interfaced by a buck DC/DC converter in the three-terminal grid, are each emulated by a Delta Elektronika SM15000 voltage source. The PV, interfaced by a boost DC/DC converter, is emulated by an ITECH IT6012C-800-50 voltage source. The three DC/DC converters of the grid are realised through the Imperix PEB8038 modules and the controllers of the converters are uploaded in the control hardware of these modules. The parameters of the lab set-up and the PI current controller of the CPL are provided in Table 12, whereas the parameters of the L-ADRC model of the DER-interfacing buck and boost DC/DC converters are mentioned in Table 13.

Figure 45 presents the output voltage of the buck and boost DC/DC converters at T_1 and T_3 of the three-terminal DC grid of the lab set-up, respectively, for a test scenario of load increase from 1.5 kW to 3.5 kW. It can be observed that the output voltage presents an undershoot of 0.9845 p.u. and an overshoot of 1.0035 p.u. in the case of both converters.

TABLE 12. Parameters of lab set-up.

Parameter [Units]	Value
V_{grid} [V]	200
$V_{in_{buck}}$ [V]	240
$V_{in_{boost}}$ [V]	102
$V_{in_{CPL}}$ [V]	250
L [H]	2.5e-3
C [F]	500e-6
R_{Ld} [Ω]	53.3
k_{p_i}, k_{i_i}	0.03, 15
f_{sw} [kHz]	20
R_l [Ω]	0.1
L_l [H]	400e-6
C_l [F]	0.5e-6

TABLE 13. Parameters of L-ADRC model for buck and boost DC/DC converters in lab set-up.

L-ADRC Parameter [Units]	Buck Converter	Boost Converter
R_d [A^2]	$4e^4$	$4e^4$
τ_d [s]	12	12
R_v [V^2]	$4e^3$	$6e^3$
R	45	400
q	0.04	0.05

Figure 46 presents the control input of the two converters for the same test in the lab set-up. It can be seen that the control input presents around 1.01 p.u. overshoot and 0.99 p.u. undershoot at both converters. It can be concluded that the L-ADRC voltage controller achieves tight voltage control after the disturbance, without requiring large changes in the control input, when it is implemented in the control hardware of real power converters. The delays involved in the process (real actuators, control execution) and the noise of the hardware do not affect the performance of the L-ADRC model.

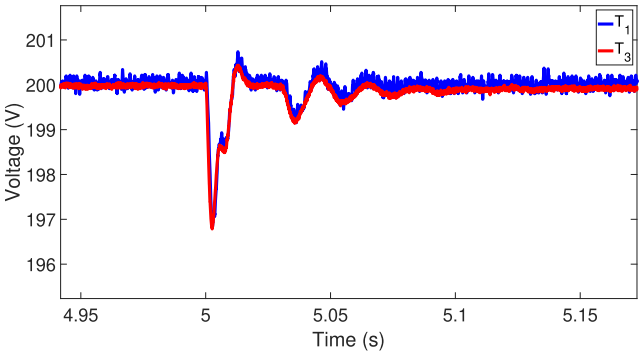

FIGURE 45. Output voltage of buck and boost DC/DC converters in lab set-up under load disturbance.

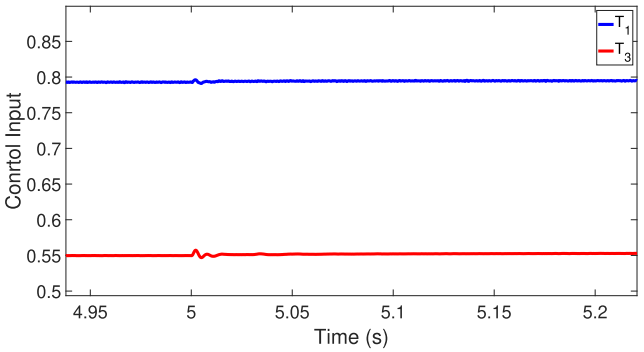

FIGURE 46. Control input of buck and boost DC/DC converters in lab set-up under load disturbance.

TABLE 14. Parameters of nominal model of buck and boost DC/DC converters.

Parameter [Units]	Value	Parameter [Units]	Value
$V_{in_{buck}}$ [V]	1000	$V_{in_{boost}}$ [V]	500
L_{buck} [H]	1.6e-3	L_{boost} [H]	1.0e-4
$R_{L_{buck}}$ [Ω]	0.1	$R_{L_{boost}}$ [Ω]	0.1
C_{buck} [F]	1e-3	C_{boost} [F]	10e-3
$R_{C_{buck}}$ [Ω]	20e-3	$R_{C_{boost}}$ [Ω]	0
$R_{Ld_{buck}}$ [Ω]	2.3	$R_{Ld_{boost}}$ [Ω]	2.3
$f_{sw_{buck}}$ [kHz]	10	$f_{sw_{boost}}$ [kHz]	10

VII. CONCLUSION

This paper presents a L-ADRC model for the voltage control in buck and boost DC/DC converters. Via its formulation properties, it is shown that the proposed L-ADRC model is suitable for converters of both MP and NMP classes and for dealing with both matched and mismatched disturbances as introduced in the nominal converter model. Thanks to the formulation of the nominal converter model with partially known dynamics, the estimation of disturbances in large frequency spectrum is enabled. Moreover, the use of states with their physical significance in the nominal converter model provides insight in the effect of the elements of the L-ADRC model on the electrical quantities of the DC/DC converters, revealing the need for the integration of the current limiter in the L-ADRC voltage controller for respecting the operation limits of the real converter plant. In addition, the formulation of the adaptive state reference trajectory provides a smooth state profile and enhances the robustness of the L-ADRC voltage controller against disturbances. The performance analysis of the L-ADRC model, in both frequency and time domains, demonstrates the large number of degrees-of-freedom for its design, stemming from the employment of model-based estimation and feedback control methods. The performance comparison against a PID voltage controller demonstrates the advantages of the L-ADRC model for the voltage control in buck and

boost DC/DC converters. The validation of the performance in the lab set-up proves its applicability in real converter devices.

APPENDIX

See Table 14.

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