Mixerless RFSoC Microwave Signal Generation for Superconducting Circuit Applications

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***Abstract*—In the realm of quantum computing and low-temperature detectors, precise signal conditioning is crucial for the effective readout and control of superconducting qubits and sensors. As these technologies evolve, the need for increasingly sophisticated and integrated systems becomes more apparent. This contribution presents the design of a mixer-less analog front-end board optimized for superconducting circuit interfacing. It leverages the capabilities of the Radio-Frequency System-on-Chip (RFSoC) from AMD Xilinx and utilizes software-selectable channel filtering stages, ultimately achieving wide-band signals without analog local oscillator leakage.**

***Index Terms*—RFSoC, Direct RF, Microwave Signals, Analog Front-End, Quantumcomputing, Quantum Circuits, Signal Conditioning**

I. Introduction

Low latency and data reduction requirements for superconducting qubit and quantum sensor applications yield FPGA-based signal processing as a promising approach. Our custom readout platform, the QiController, is based on a Xilinx ZCU216 Radio Frequency System-on-Chip (RFSoC) evaluation board. To facilitate its usage, we developed an analog front-end Printed Circuit board (PCB) for filtering and adjusting signals of interest (Figure 1). The board is fully configurable using the Quantum Interface Controller (QiController) [1] via the Radio Frequency Mezzanine Connectors (RFMCs) of the ZCU216. Digital mixing capabilities from the Xilinx Radio Frequency Data Converter (RFDC) stage on the RFSoC on the ZCU216 keep all frequency transforms transparent to the Programmable Logic (PL).

II. Design and Capabilities

The front-end board measures $311\,\mathrm{mm}$ by $252\,\mathrm{mm}$, fans out 16 Transmission (TX) channels, 8 Reception (RX) channels and 32 digital Input and Output (IO) lines. These IO lines, intended for trigger and marker signals, are required for syncing and interfacing with other lab equipment. Routing through level shifters ensures manually switchable $1.8\,\mathrm{V}$ or $3.3\,\mathrm{V}$ output Voltage levels and input protection.

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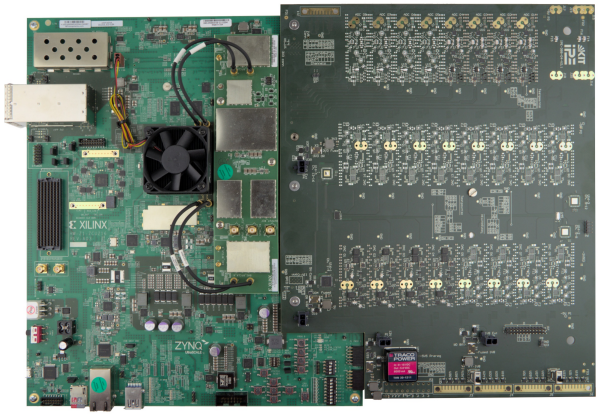

Fig. 1. Custom $311\,\mathrm{mm}$ by $252\,\mathrm{mm}$ Mixerless DirectRF Analog Front-End Board Mounted on the AMD Xilinx ZCU216 Evaluation Board.

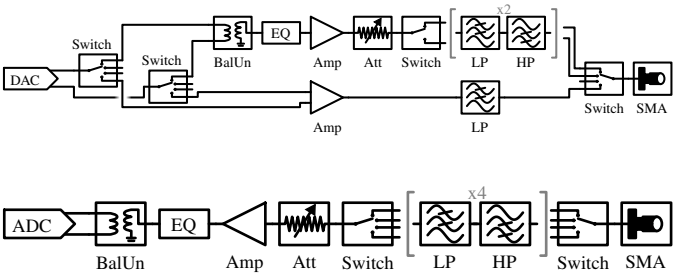

Fig. 2. Schematic of one DAC channel (top) and one ADC channel (bottom) showing the independent signal filtering sections.

The frequency range of interest from DC to $7\,\mathrm{GHz}$ given by the RFSoC is to be covered fully on the TX side, while RX features partial coverage.

As the Digital-to-Analog Converters (DACs) and Analog-to-Digital Converters (ADCs) have different maximum sampling frequency ($f_{dac} < 10\,\mathrm{GS\,s^{-1}}$, $f_{adc} < 2.5\,\mathrm{GS\,s^{-1}}$) per the manufacturer, the TX and RX channel designs thus feature different filters. The narrower ADC side Nyquist Zones (NZs), equivalent to bandwidth, also mounts to a greater number of filters required with $100\,\mathrm{MHz}$ - $2\,\mathrm{GHz}$ and 5 - $7\,\mathrm{GHz}$ coverage. Alternative pass bands can be selected through mounting different filters with compatible footprints.

The first stage of any DAC channel (fig. 2 top) consists of two *Menlo Micro* Micro Electromechanical System (MEMS)

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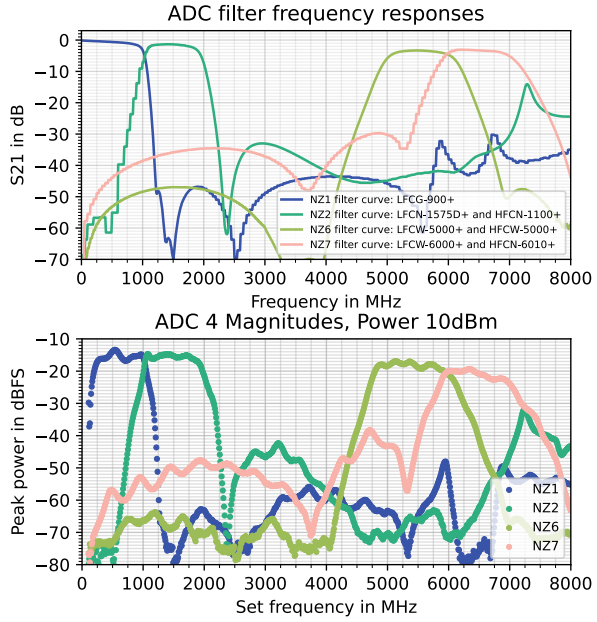

Fig. 3. Simulated (top) and measured (bottom) frequency response of ADC filters.

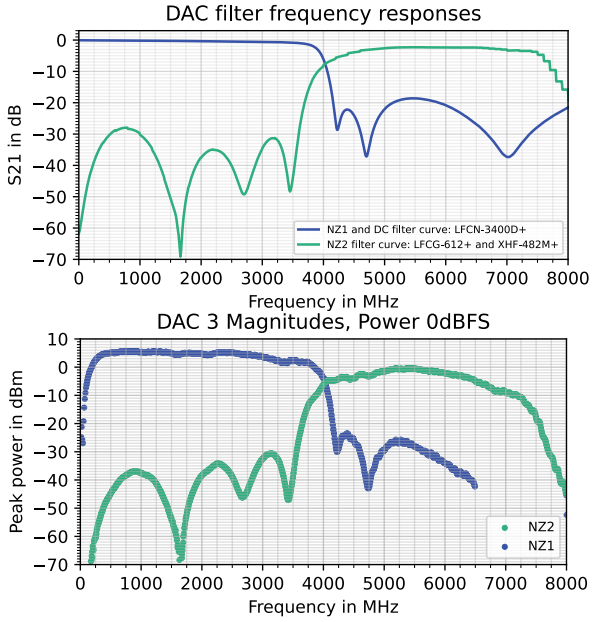

Fig. 4. Simulated (top) and measured (bottom) frequency response of DAC filters.

switches, which permit relay-like signal switching down to nonzero direct current levels (unlike, for example, PIN diode versions). This enables potential control of DC-coupled flux bias lines and maintains operability throughout wide tuning ranges. The DC-capable path consists of an Operational Amplifier (OPA), both removing the common mode voltage and providing differential to single ended conversion. The second signal path is AC coupled through a BalUn with both lossy elements on each port improving matching. Finally, another switch lets the user choose whether to filter for contents from the first or second DAC NZ (figure 4) combining either of the filtered signals and the DC path to a single output connector.

Any ADC channel (figure 2 bottom), starting at the SMA connector, first employs a four-throw switch to route the incoming signal onto different filter banks (figure 3). This is preferred over power splitting, as the latter would incur a higher insertion loss. Attenuator placement before the amplifier ensures a user selectable trade off between signal level and distortion from clipping at the cost of slightly higher SNR.

Equalization and 31.5 dB of analog dynamic range are provided at TX and RX to maintain a flat frequency response and compensate dielectric losses.

Digital slow control consists of a single Inter-Integrated Circuit (I2C) bus configuring seven PCA9506 General Purpose Input and Output (GPIO) port expanders. This enables runtime configuration of the filter banks, amplifiers and level shifters. The modular software architecture of the QiController utilizing the ServiceHub [2] facilitates easy remote user access via Python scripts through Google Remote Procedure Call (gRPC) based Ethernet channels.

III. Limitations

As the conversion of a discrete time-sampled signal is ambiguous in terms of NZs, a mirror image signal will always be produced when close to NZ border regions. Similarly, due to interpolation of the net data from the PL to the actual sampling frequency, several similar spurs appear throughout the whole frequency range when sweeping both the DA and AD. The finite slope of the filters employed means users will need to add additional suppression or tolerate the spurious emissions (compare figs. 3 & 4).

While the physical size of the PCB is substantial and individual coaxial line breakout as SMA connectors is not particularly tightly integrated, this approach is pursued for versatility and could easily be replaced by higher density connections for 1U chassis mounting.

At the time of writing, the DC channel features high loss at frequencies below 10 MHz, likely due to a misconfigured OPA feedback network.

IV. Conclusion

We have presented a uniquely convenient-to-use, compact, high-channel count signal conditioning front-end and a basic laboratory passband characterization. It will serve as the analog interface of the QiController for future multi qubit experimentation.

References

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