Super Heterodyne Mixer Front-End Module for Qubit Readout and Manipulation

Robert Gartmann†*, Oliver Krömer†, Richard Weller†, Nick Karcher†, Luis E. Ardila-Perez†, Oliver Sander†
Institute for Data Processing and Electronics (IPE)
Karlsruhe Institute of Technology (KIT), D-76133 Karlsruhe, Germany

***Abstract*—Superconducting quantum circuit interfacing frequently entails working with multi-GHz radio frequency signals. The quickly evolving field relies on FPGA-based software-defined radio systems, providing the required flexible low-latency signal synthesis and analysis capabilities. Consequently, there are many custom hardware developments and upcoming commercial systems with proprietary interfaces. In contrast, this contribution presents a compact, platform-agnostic frequency conversion and level matching analogue front-end for 800 MHz vector signal generation, which expands the covered frequency band for any SMA connectorised system from baseband frequencies below 400 MHz to 4-10 GHz. It is in active use for quantum bit characterisation and for quantum sensor readout.**

***Index Terms*—Quantum Circuit Interfacing, Qubit, Quantum-computing, Software-Defined Radio, Analogue Front-End Mixer**

I. Introduction

Microscopic superconducting circuits show many promising applications, from quantum annealing and computing [1] to various approaches of sensing technologies. The low temperature (mK to K) environment poses its own challenges. However, it guarantees low-noise operation, excellent shielding, and superb sensitivity. The absence of resistive loss in superconducting materials makes them an excellent choice to form electrical resonance circuits, which can be interfaced using frequency-multiplexed schemes. This means that many resonators can be manipulated or read out through a single coaxial line, with the ultimate number limited by channel speed, thus bandwidth, and signal generation limits.

II. Design Principle

Mixers are used for up and down conversion of signals on the Printed Circuit board (PCB) (compare figs. 2) and 1).

Complex (IQ) mixing ensures efficient use of the available band, it also doubles the band coverage with the same Baseband (BB) signal frequency (fig. 1 green). The BB interface contains anti-aliasing low-pass filters and is converted from the single-ended Subminiature Version A (SMA) connectors to a differential pair. SMA also enables platform-agnostic, fully transparent connection to any type of signal generation device.

The Intermediate Frequency (IF) is designed for 2 GHz to 4 GHz operation (fig. 1 orange). Baseband isolation is sufficient, so only a low-pass filter is required for harmonic rejection. There is a resistive combiner pad in the IF nodes with connections to monitoring ports as well as synthesisers. It also enables higher instantaneous bandwidth assemblies [2].

The signal is converted between IF and Radio Frequency (RF) through a real mixer, which generates both sidebands (fig. 1 blue). Another set of filters provides spectral clearance. Level adjustment is achieved through signal amplifiers and equalisers. Passive directional couplers enable monitoring of the signals without disconnecting from the main circuit. There is a Voltage Variable Attenuator (VVA) on the Transmission (TX) side. The RF ports are also SMA connectors, albeit with different solder pad geometry for higher frequency operation.

The Local Oscillators (LOs) are on board Texas Instruments Voltage Controller Oscillator (VCO) + Phase Locked Loop (PLL) Integrated Circuits (ICs). Their output is filtered to the respective IF or RF band through a low- and high-pass filter pair. This is necessary as the IC provides a rectangular output signal, containing harmonics of the fundamental, which would both divert power and clutter the spectrum.

The board works off of a single 12 V supply and exposes additional ports for reference clocking as well as IDC connectors for slow control. It has euro card format of 100 mm by 160 mm and is manufactured on an 8 layer stackup of Panasonic Megtron 6 low-loss material. Schematic capture and routing were performed on the Siemens Mentor PADS standard plus software suite.

III. Capabilities

The BB interface has a frequency limit of 400 MHz stemming from Mini Circuits LFCN-400+ filters, as the converters of the Institute for Data Processing and Electronics (IPE) Software Defined Radio (SDR), based on a Xilinx Radio Fre-

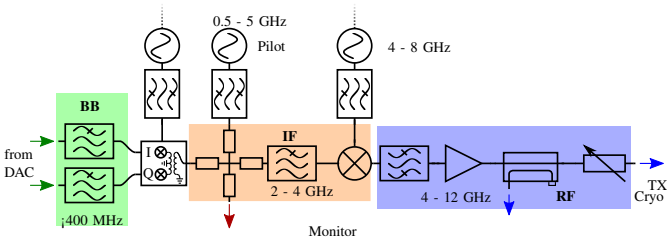

Fig. 1. Simplified schematic of the transmission signal path, upconverting from baseband to radio frequency.

The authors acknowledge the support by the Doctoral School "Karlsruhe School of Elementary and Astroparticle Physics: Science and Technology". The authors acknowledge the financial support by the German Federal Ministry of Education and Research in the framework of PtQube (FKZ:13N15015)

979-8-3315-4137-8/24/$31.00 ©2024 IEEE
DOI 10.1109/QCE60285.2024.10408

quency System-on-Chip (RFSoC), work at $1\,\mathrm{GS\,s^{-1}}$. This is also close to the $500\,\mathrm{MHz}$ maximum bandwidth of the conversion ICs. The TCM1-1-83X+ BalUn Alternating Current (AC) coupling limits the lower frequency to several MHz. Though the LTC5588 modulator does not provide meaningful configuration ability to alter the signal, the LTC5586 demodulator features variable attenuation, harmonic and intermodulation optimisation.

The LMX2594 LOs provides dual differential outputs of up to $15\,\mathrm{GHz}$. Fractional PLL operation allows for sub Hertz frequency accuracy. As all three bands - BB, IF, and RF - have a valid frequency range, there are many possible combinations to achieve any one output frequency (see IV). As the conversion utilises two local oscillators and aims for a large, beyond-octave output frequency bandwidth, the full band Spurious Free Dynamic Range (SFDR) can be worse than $20\,\mathrm{dB}$, of course dependent on per-user filtering and precise LO positioning. Whether this is a problem depends on the setup, as the resonators present a means of isolation. Similarly, if and where in the cold stages the superfluous power is dissipated hinges on the location of termination resistors.

The VVA allows easy alteration of the signal power, which is frequently performed when identifying ideal operating conditions or deliberately performing power sweeps. The equalisers show negative slope with increased frequency to compensate for the cable, the substrate, and device insertion loss, resulting in a flat response.

IV. Theory of Operation

As the PCB has no default power-up condition, the Inter-Integrated Circuit (I2C) and Serial Peripheral Interface (SPI) interfaces exposed through IDC connectors need to be fed with the configuration for the ICs. It consists of two register sets for the local oscillators, one for the demodulator, as well as voltage configuration for the Digital-to-Analog Converter (DAC) driven VVA. Establishing a connection to the Field-Programmable Gate Array (FPGA) platform or System-on-Chip (SoC) based computer allows for communication through LAN via the zeroRPC and Google Remote Procedure Call (gRPC) framework. User settings are processed locally in Python scripts, then handed over to the C++ based host application on the network-enabled device. Linux kernel drivers map the logical functions to the register and supply it through a multiplexed SPI bus.

Though the PLLs can achieve any frequency, ideal jitter performance is attained when driven in integer mode, meaning

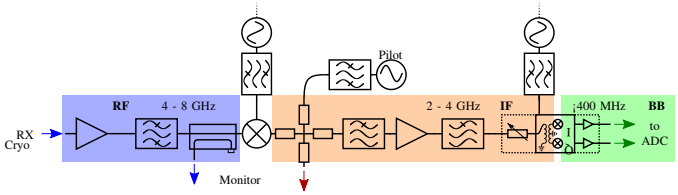

Fig. 2. Simplified schematic of the reception signal path, mixing the radio frequency signal back down to baseband.

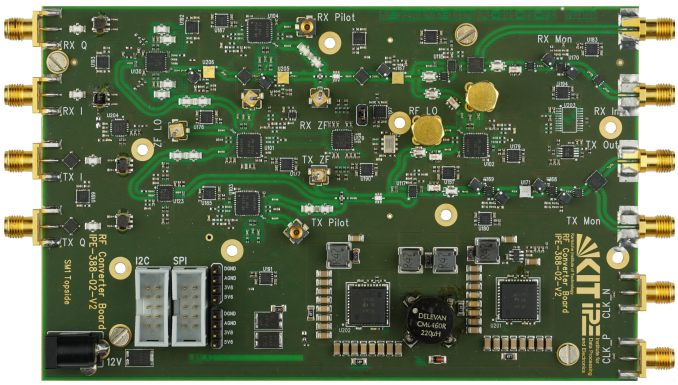

Fig. 3. Picture of the finished printed circuit board assembly. BB inputs are on the left with RF and clocks supplied on the right hand side.

the BB instrument adapts its synthesis. Similarly, pushing the LO and image frequency in RF to the filter rejection bands is achieved through a high IF. Consequently, the IF should be as high as possible. As there is currently no IF equaliser installed, this means the signal level is highest with low IF. For this reason, the output filtering can be configured as $4\,\mathrm{GHz}$ or $8\,\mathrm{GHz}$ high-pass and $8\,\mathrm{GHz}$, $10\,\mathrm{GHz}$ or $12\,\mathrm{GHz}$ low-pass.

The VVA shows per-part variation, requiring extensive two-dimensional calibration if precise levels are desired. However, as cryostat setups frequently change and both custom wires and bonds alter the attenuation and coupling efficiencies, power has to be determined through various means.

V. Phase Noise

The LO IC has very low nominal additive phase noise: $<70\,\mathrm{fs}$ rms from $10\,\mathrm{Hz}$ to $100\,\mathrm{MHz}$. The total jitter is slightly higher due to a clock fanout buffer and both LOs being used in tandem. High reference clock frequencies beyond $100\,\mathrm{MHz}$ ensure sufficient slew rate for this jitter number, while lower F_{PFD} mean finer integer stepping. Internal reference frequency dividers allow for both merits at the same time.

As neither the reference frequency nor the desired output frequency are fixed, the loop filter is as described in the data sheet. While no ground plane separation is employed between the VCO, charge pump, and digital ground, there are two separate supplies for the output driver stage and the rest of the IC. Each LO has half the differential pair terminated into a debug connector, while the other goes to mixers.

VI. Conclusion

This work demonstrates a compact, platform-agnostic radio frequency conversion front-end. It can operate stand-alone and provides a low-cost means for evaluating superconducting circuit systems.

References

[1] R. Gebauer, "A flexible fpga-based control platform for superconducting multi-qubit experiments," 2022, 47.12.01; LK 01.

[2] R. Gartmann, N. Karcher, R. Gebauer, O. Krömer, and O. Sander, "Progress of the ECHo SDR readout hardware for multiplexed MMCs," *J. Low Temp. Phys.*, Sep. 2022.