A Coupled Inductor Based SSCB With Reduced Components for DC Microgrid Protection

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***Abstract*—DC microgrids have gained importance for their high efficiency, no need for synchronization, high power quality, and potential to reduce greenhouse gas emissions. Ensuring reliable and fast protection against over current and shor-circuit faults is considered to be a challenge even to date. Solid-state circuit breakers offer a promising solution, providing rapid and arc-less fault clearing. However, SSCBs employing fully controlled devices lead to higher costs and conduction losses. This paper discusses a cost effective circuit breaker, using a semi-controlled switch based on a coupled inductor. The proposed SSCB has reduced overall components, a discharged capacitor and also allows the option to trip manually for maintenance. A detailed analysis and design methodology for component selection is presented in the later sections. The SSCB is experimentally validated by developing a laboratory prototype for a voltage rating of 400V and at a nominal current of 15A & 20A with a short circuit fault current of 60 A.**

***Index Terms*—Solid state circuit breakers (SSCBs), Greenhouse gas, Microgrids, DC distribution, fault protection, DC circuit breaker, Electric Vehicles, Energy storage systems.**

I. Introduction

THE growing impact of climate change, primarily driven by greenhouse gas (GHG) emissions, has strengthened the need to reduce fossil fuel dependence and shift to renewable energy sources [1]. One promising solution is the implementation of DC microgrids (MGs), which support renewable resources. Compared to AC systems, DC MGs exhibit several advantages: they have improved transmission capabilities and power quality and do not need synchronization, reactive power, phase, and frequency control [2].

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The necessity of DC MGs has become increasingly evident, as DC distribution is a key component in modern electrical systems such as Electric Vehicles (EVs), data centres, telecommunications, energy storage systems, renewable energy integration, and both residential and commercial buildings [3]. At the lower end of the LVDC range, applications include EVs, remote households, telecommunication and data centres [4]. As renewable energy infrastructure expands, the movement toward MVDC power distribution for energy delivery becomes inevitable, supported by power electronic converters. Meanwhile, HVDC technology now includes applications such as long-distance transmission, submarine and underground cables, and the interconnection of asynchronous systems [5], [6].

The primary goal of the DC system includes the efficient integration of various renewable energy resources and loads without compromising on reliability. Different zones, as illustrated in Fig. 1, require distinct protection mechanisms due to their respective safety or risk classifications, according to the overview presented in [7], [8]. The voltage levels range from $\leq$ 400 V at the consumer end to $\leq$ 1500 V for Low Voltage DC electrical installations. Thus, each zone demands a different protection device. However, designing an effective coordinated protection system for DC MGs remains a significant challenge [9]. Unlike AC systems, DC fault currents rise rapidly and lack a natural zero-crossing point, which can result in a persistent arc upon opening a DC circuit breaker [10], [11]. The fault current must be extinguished quickly and reliably to prevent damage, maintain microgrid stability, and reduce downtime.

DC circuit breakers (DCCBs) in the literature are classified into modified mechanical, hybrid, and SSCBs, each with distinct response time, efficiency, and complexity characteristics [12]. Modified mechanical circuit breakers (MCBs) offer the lowest possible conduction losses but respond more slowly and require extra arc-extinguishing mechanisms to force the current to zero, resulting in a more complicated and bulky design [13]. On the other hand, SSCBs provide rapid, arc-less fault interruption, offering the fastest response times but at the cost of increased conduction losses. Hybrid DC circuit breakers (HCBs) combine the advantages of both mechanical and SSCBs, achieving low conduction losses with an intermediate fault response time [14].

SSCB Topologies reported in [15]–[17], which employ capacitor commutation for the fault interruption, have gained significant attention as they offer faster switch commutation due to the absence of inductive elements, a simpler design with fewer auxiliary circuits and low conduction losses, making

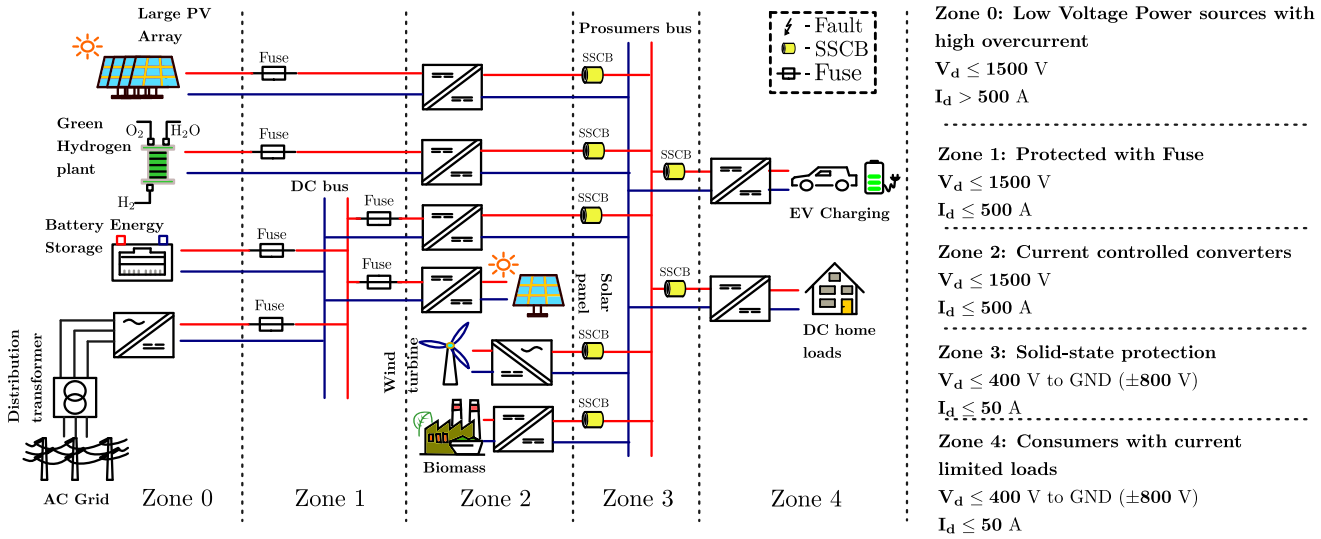


Fig. 1: Assessment of Safety Zones in DC microgrids in accordance with the standards overview presented in [7].

them efficient under normal operation. However, they cannot limit fault current since capacitors do not naturally restrict current [15]. They also cause high current overshoots during switching, requiring snubber circuits to mitigate the issue [16]. For high-power applications, these topologies require large capacitors, which further increases cost, size, and system stress [17].

Semi-controlled thyristor-based SSCBs are widely used for the protection of the DC MGs due to the availability of higher voltage and current-rated devices at a lower cost, high surge current withstand capability, and low conduction loss of the thyristor at high current [18], [19]. Among the various semi-controlled SSCBs, the Z-source circuit breakers (ZSCB) have gained prominence due to their autonomous fault interruption capability, which eliminates the need for sense and trip electronics [20]. A modified unidirectional series ZSCB topology has been presented in [21] to overcome several issues in the conventional series ZSCB topology, such as unwanted power flow to the load before commissioning the circuit breaker, and negative current flow through the load for a short period along with high peak current through the main thyristor during commissioning. Bidirectional ZSCB topologies have been presented in [22], [23], but require more active and passive components during both conduction and fault interruption. To offer adjustable fault current trip levels, several coupled inductor-based bi-directional ZSCBs have been introduced [24]–[27]. The main limitation of ZSCBs is their inability to trip for large impedance faults or over-current events. A method for implementing overload protection is presented in [28] and has the inherent advantage of high di/dt tripping. However, it cannot effectively distinguish high-impedance short circuit faults and requires additional power semiconductor switches, leading to increased control complexity. To overcome the drawbacks of ZSCBs, several thyristor-based SSCBs have been proposed that include a current sensor and use the mutual coupling between the coupled inductor coils to commutate the main thyristor [29], [30].

To overcome the existing issues of the SSCBs mentioned

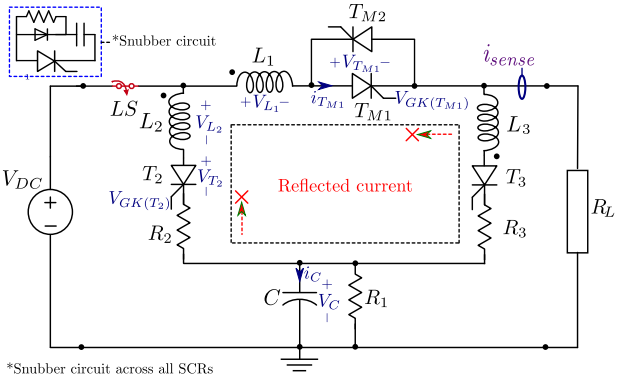


Fig. 2: Proposed SSCB topology.

above, this paper introduces a new bidirectional thyristor-based SSCB topology that finds its applications, as illustrated in Fig. 1, with a simplified circuit design. A single fault on a DC system can increase the current and simultaneously affect the renewable sources, ESSs, and interconnected loads. Thus, the SSCB protection, if not provided, may lead to system-level unrecoverable impacts.

The key features and contributions of the proposed SSCB topology are as follows:

1) The proposed SSCB utilizes a three-winding coupled-inductor design, enabling bidirectional power flow, unlike conventional coupled inductor based SSCB designs that typically use only two windings. [31]–[38].
2) The proposed design minimizes the number of components, requiring only one capacitor, no diodes in the conduction path, and a single coupled inductor, leading to lower cost and improved reliability.
3) A single thyristor switch and inductor winding in the main conduction path reduce conduction losses, enhancing efficiency. Additionally, the auxiliary inductor path is only activated during fault interruption and does not contribute to conduction losses.
4) The auxiliary capacitor remains uncharged under normal

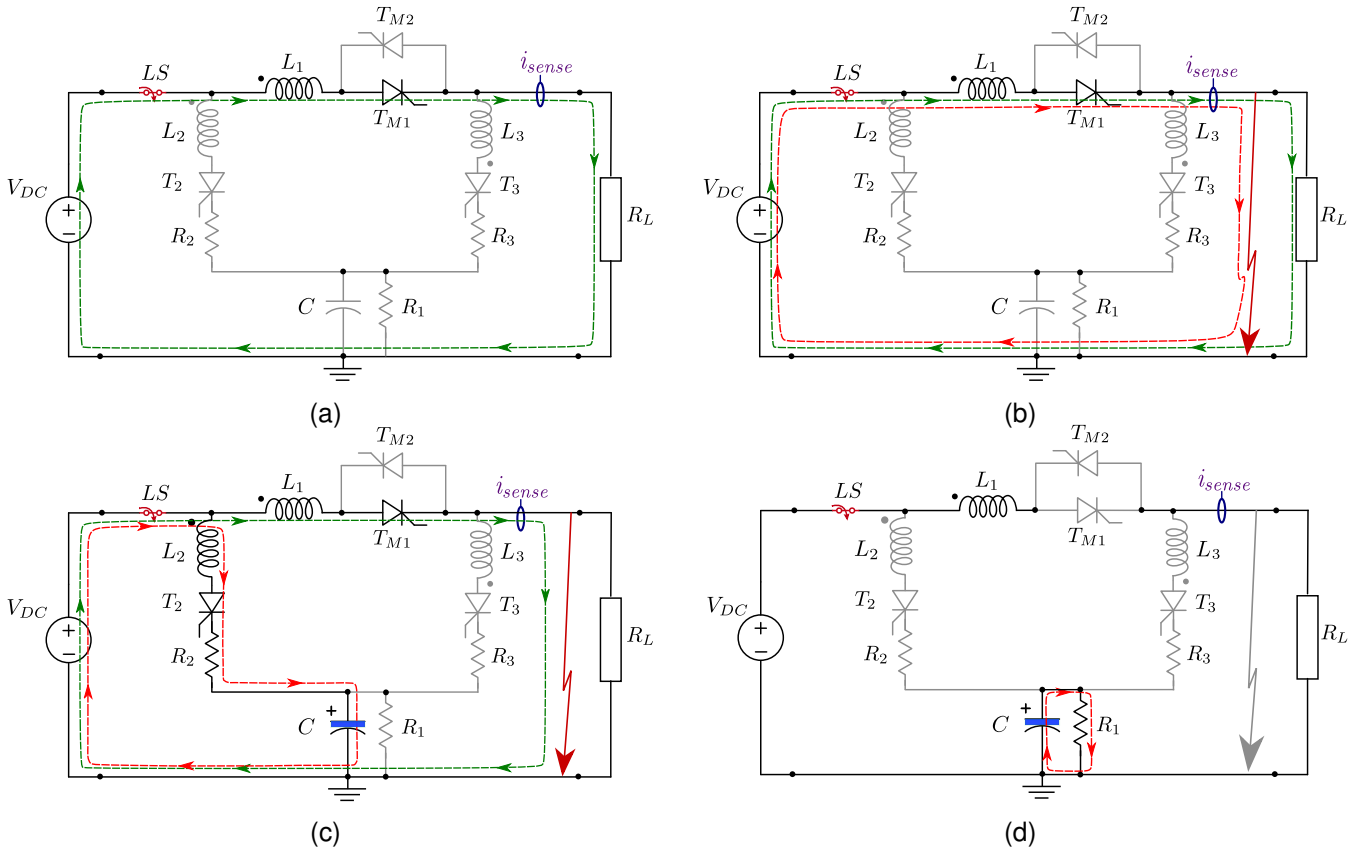


Fig. 3: Modes of operation for the proposed SSCB: (a) Steady state operation (*mode-1*), (b) Transient fault current interval (*mode-2*), (c) Fault current interruption (*mode-3*), and (d) Capacitor discharge interval (*mode-4*).

conditions and is only charged during fault interruption, unlike other SSCB designs that require capacitor pre-charging and periodic charge top-up [39].

5) Since the proposed topology does not require a precharged capacitor and periodic charging, it enhances the SSCB reliability during commissioning.
6) The SSCB provides reliable protection against both over-current events and short-circuit faults, ensuring a fast trip response, and also includes a manual tripping feature.
7) The auxiliary branch is designed as an energy-absorbing branch, ensuring that all the excess energy is handled by the auxiliary capacitor. However, an MOV and a snubber circuit are included as a backup for voltage clamping and additional protection of the SCRs during turn-off.
8) During a fault condition, the proposed SSCB does not experience the reflected current flowing back to the source, as the thyristors are inherently unidirectional.

The paper is organized as follows: Section II describes the proposed SSCB in detail. Section III discusses the circuit modeling of the SSCB topology. Experimental validation is provided in Section IV. Section V provides a detailed discussion and comparison of the proposed SSCB topology. The conclusions are drawn in Section VI.

II. Proposed SSCB Topology

This section discusses the operational modes of the proposed SSCB, illustrated with a schematic in Fig. 2. The design includes two primary thyristors, T_{M_1} and T_{M_2}, arranged in an anti-parallel configuration to enable bidirectional power flow, and these thyristors are the main conduction elements. The circuit breaker comprises inductors L_1, L_2, and L_3, with coupling between L_1 and L_2 when power flows from left side port to the right side port, and coupling between L_1 and L_3 when power flows in the opposite direction. The commutation circuit consists of an inductor, an auxiliary thyristor, a current limiting resistor, and a capacitor. A low-speed switch LS provides galvanic isolation between the DC bus and the load.

A. Operating Principle of the SSCB

Operational modes of the proposed SSCB are illustrated in Fig. 3. Since the proposed SSCB is symmetrical, operating modes showing power flow from the left port (V_{DC}) to the right port (load) are discussed. The conceptual voltage and current waveforms at different points in the topology are illustrated in Fig. 4.

1) *Mode-1 (t_1 to t_2)*: The circuit schematic associated with this mode is shown in Fig. 3(a). In this mode, the switch LS is closed, and the thyristor T_{M1} is triggered at the time instant t_1. As a result, current flows from source to the load through a path containing $V_{DC} \rightarrow L_1 \rightarrow T_{M1} \rightarrow R_L$. A voltage spike appears across the coupled inductor windings as the load current ramps up. The circuit enters into a steady state at time instant t_{1-b} with the voltage across the load (V_{R_L}) equal to V_{DC} if the drop across the switch T_{M1} and inductor

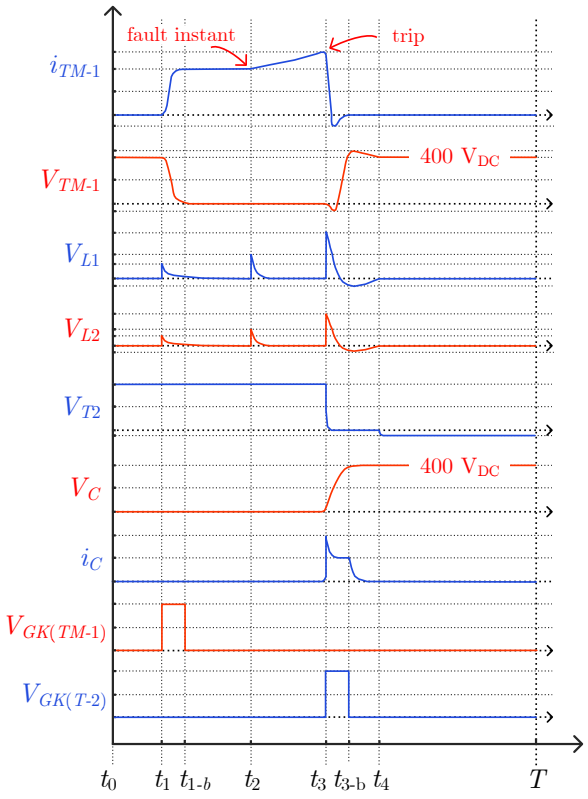


Fig. 4: Conceptual waveforms depicting modes of operation.

winding L_1 is neglected. The gate pulse to the thyristor T_{M1} is removed at time instant t_{1-b}, but the thyristor T_{M1} continues to remain in on-state and supply the load current. During the period from t_1 to t_2, the auxiliary path is kept off, and the capacitor remains uncharged.

2) *Mode-2 (t_2 to t_3)*: The circuit schematic during this mode is shown in Fig. 3(b). A short circuit or over-current fault is created at the load side at time instant t_2. As a result, the system current rises rapidly with the slope of fault current rise limited only by the inductance L_1. Since the topology employs a current sensor, the current rise is sensed and fed to the microcontroller.

3) *Mode-3 (t_3 to t_4)*: If the system current rises above the preset fault value, the auxiliary thyristor T_2 is turned on by providing a gate pulse to the switch at time instant t_3 as shown in Fig. 3(c). The auxiliary current path is through $V_{DC} \rightarrow L_2 \rightarrow T_2 \rightarrow R_2 \rightarrow C$. As a result, the fault current is diverted through the coupled inductor L_2 and charges the capacitor. The gate pulse to the auxiliary thyristor is removed after a short time interval at instant t_{3-b}, but the auxiliary thyristor continues to conduct until the capacitor is fully charged to the DC bus voltage.

Due to the mutual coupling action, the voltage across L_1 increases and opposes the source current. The thyristor T_{M1} turns off, once the current through it falls below the holding current, at t_{3-b}. The capacitor charges to DC bus voltage V_{DC}, after which the current in T_2 reduces to zero, resulting in the auxiliary path thyristor T_2 turning off naturally.

4) *Mode-4 (t_4 onwards)*: At time instant t_4, once the auxiliary thyristor T_2 has turned off, it blocks the voltage equal to the difference of the supply voltage V_{DC} and the capacitor voltage V_C, considering that the voltage across the inductor L_2 is zero. The capacitor which is now charged to V_{DC} will discharge through the resistor connected across to it. This mode of operation is described in Fig. 3(d). Once the auxiliary capacitor is discharged, the SSCB is ready for the next fault interruption process.

B. Analysis of the impedance network of the proposed SSCB

Under normal condition, the proposed SSCB becomes a simple RL circuit. During fault an additional branch with inductor L_2 and C comes into parallel with the RL branch as shown in Fig. 3c.

Applying KVL to both the branches:

$$V_{\text{in}} = (sL_1 + R_L)I_1(s) + sMI_2(s) \tag{1}$$

$$V_{\text{in}} = (sL_2 + \frac{1}{sC})I_2(s) + sMI_1(s) \tag{2}$$

where, V_{in} is the input voltage, R_L is the load resistance, C is the capacitance of the auxiliary branch, L_1, L_2 are the self inductances and M is the mutual inductance between the windings.

Writing the two equations (1) and (2) in matrix form:

$$\begin{bmatrix} sL_1 + R_L & sM \\ sM & sL_2 + \frac{1}{sC} \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix} = \begin{bmatrix} V_{\text{in}} \\ V_{\text{in}} \end{bmatrix} \tag{3}$$

Solving for $I_1(s)$ by using Cramer's Rule:

$$I_1(s) = \frac{(sL_2 + \frac{1}{sC})V_{\text{in}} - sMV_{\text{in}}}{(sL_1 + R_L)(sL_2 + \frac{1}{sC}) - (sM)^2} \tag{4}$$

Since the output voltage is taken across the resistor R,

$$V_{out} = R_L \cdot I_1(s) \tag{5}$$

Thus, the transfer function is:

$$H(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_L I_1(s)}{V_{\text{in}}} \tag{6}$$

Substituting $I_1(s)$ in (6), the transfer function during transient is:

$$H(s) = \frac{R_L(sL_2 + \frac{1}{sC} - sM)}{s^2(L_1L_2 - M^2) + s(R_LL_2 + \frac{L_1}{sC}) + \frac{R_L}{sC}} \tag{7}$$

As a special case by substituting C, L_2 and M as '0' in (7):

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{R_L}{s \cdot L_1 + R_L} \tag{8}$$

Equation (8) refers to the transfer function of the system during normal operation.

The bode plot during the normal and transient fault condition for their respective transfer function (8) and (7) is shown in Fig. 5 and 6 respectively.

Overall frequency response analysis of the proposed SSCB:

1) At low frequencies, the gain is approximately 1 (0 dB), meaning the circuit passes low-frequency signals with minimal attenuation. The phase shift is close to 0°, indicating that the output voltage remains in phase with the

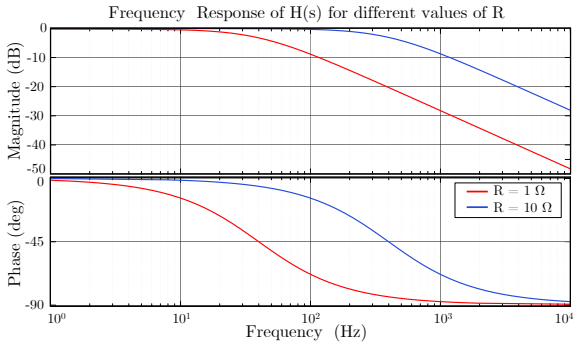


Fig. 5: Bode diagram of the input–output voltage transfer function before fault.

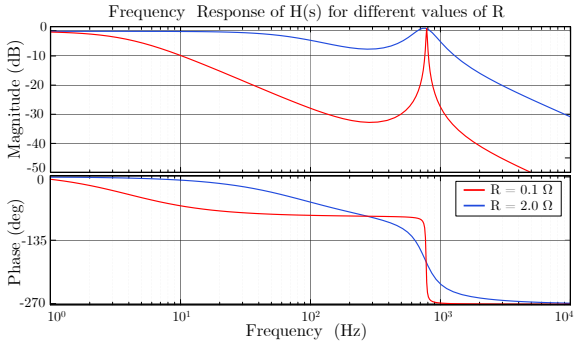


Fig. 6: Bode diagram of the input–output voltage transfer function during fault.

input, as shown in Fig. 5 and Fig. 6, which corresponds to normal operation.

2) At high frequencies, the gain decreases, and the phase shift approaches -90°, signifying the increasing dominance of the inductor's impedance, resembling that of a low-pass filter as shown in Fig. 5.
3) At high frequencies, the gain decreases, and the phase shift approaches -270°, signifying the increasing dominance of the capacitor's impedance, resembling that of a low-pass filter as shown in Fig. 6, which corresponds to a transient condition.

This filtering capability arises from the unique structure of the proposed topology, allowing the circuit breaker to function not only as a protection device but also as an effective filter.

III. Circuit Modeling of the Proposed SSCB

In this section, the equivalent circuit of the SSCB during fault interruption is modeled, and the governing equations for choosing the required inductance and capacitance are derived from the mathematical model. The selection criteria for thyristors and current limiting resistors are provided. To simplify the analysis, the on-state voltage drop of thyristors, the winding resistance of the coupled inductor, and the internal resistance of the capacitor are omitted.

A. Steady state

During the steady state, the main switch T_{M1} is in on-state. Considering the behaviour of inductor as a short circuit during steady state, current flowing through the thyristor is given as:

$$I_{T_{M1}} = \frac{V_{DC}}{R_L} \tag{9}$$

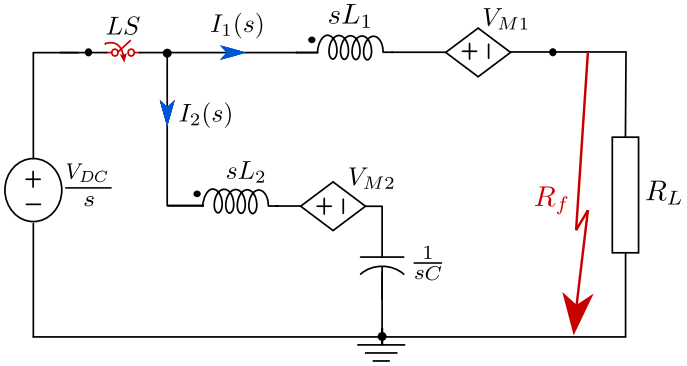


Fig. 7: Equivalent circuit of SSCB during transient fault state in s-domain.

B. Fault transient state

When a short circuit or over-current fault occurs, system current rises to a very high value. Fig. 3(b) shows the fault current path. An equivalent model of the circuit in Laplace domain during this operation is shown in Fig. 7. Thyristor in the auxiliary path is triggered once the load current reaches a preset value, which makes the capacitor begin charging. To simplify the analysis, voltage across the main thyristor T_{M1} and the fault resistance R_f are neglected.

Referring to Fig. 7, circuit equations in the Laplace domain can be written as,

$$\frac{V_{DC}}{s} = L_1 \cdot (s \cdot I_1(s) - I_{peak}) + V_{M1} \tag{10}$$

$$\frac{V_{DC}}{s} = L_2 \cdot (s \cdot I_2(s) - a \cdot I_{peak}) + V_{M2} + \frac{1}{s \cdot C} \cdot I_2(s) \tag{11}$$

$$Where, \begin{cases} L_{1,2} = L_{1s,2s} + L_{1l,2l}, L_l = L_s(1-k) \\ M = k\sqrt{L_1 L_2}, L_2 = \dfrac{L_1}{a^2} \\ I_M = I_{\text{peak}}, I_A = a \cdot I_{\text{peak}} \\ V_{M1} = M \cdot (s \cdot I_2(s) - a \cdot I_{peak}) \\ V_{M2} = M \cdot (s \cdot I_1(s) - I_{peak}) \end{cases} \tag{12}$$

In the above equations, $L_{1,2}$ is the total inductance, $L_{1s,2s}$ is the self-inductance and $L_{1l,2l}$ is the leakage inductance. Usually, $L_{1s,2s} >> L_{1l,2l}$. M refers to mutual inductance between the coils, 'k' is the coupling coefficient whose value lies between 0 and 1 ($0 < k < 1$), and the inductance value in auxiliary path is related to the primary path inductor according to the relation mentioned in (12) where 'a'=N_1/N_2 is the turns ratio of the two coupled windings. I_M and I_A are the initial current values in the primary and auxiliary paths, respectively. V_{M1} and V_{M2} are the voltage due to the mutual inductance present between the windings. I_{peak} is the maximum current flowing through the main thyristor during the fault instant.

By considering (12) and solving equations (10) and (11). The time domain equations for $i_1(t)$, and $i_2(t)$ are given as:

$$i_1(t) = I_{\text{peak}} \cdot (1+k) + \frac{V_{DC} \cdot t}{L_1} - \frac{V_{DC} \cdot k \cdot (k-a)\sqrt{C}}{a \cdot (k^2-1) \cdot \sqrt{L_1}} \sinh\left(\frac{a \cdot t}{\sqrt{C \cdot L_1 \cdot (k^2-1)}}\right) - I_{\text{peak}} \cdot k \cdot \cosh\left(\frac{a \cdot t}{\sqrt{C \cdot L_1 \cdot (k^2-1)}}\right) \tag{13}$$

$$i_2(t) = V_{DC} \cdot \frac{a \cdot \left(\frac{k}{a}-1\right) \cdot \sqrt{C}}{\sqrt{(k^2-1) \cdot L_1}} \sinh\left(\frac{a \cdot t}{\sqrt{C \cdot L_1 \cdot (k^2-1)}}\right) + I_{\text{peak}} \cdot a \cdot \cosh\left(\frac{a \cdot t}{\sqrt{C \cdot L_1 \cdot (k^2-1)}}\right) \tag{14}$$

$$where, \begin{cases} i_{TM1} = i_1(t) \\ i_{TA2} = i_2(t) \end{cases} \tag{15}$$

and, $\frac{a \cdot t}{\sqrt{C \cdot L_1 \cdot (k^2-1)}}$ is the damping frequency of the second order system, i_{TM1} and i_{TA2} are the thyristor current in the main path and auxiliary path respectively.

Simplifying the equations (13) and (14) by using Taylor series expansion, the thyristor currents become:

$$i_{TM1} = i_1(t) = I_{\text{peak}} + \frac{V_{DC} \cdot (k \cdot a - 1)}{L_1 \cdot (k^2-1)} \cdot t \tag{16}$$

$$i_{TA2} = i_2(t) = I_{\text{peak}} \cdot a + \frac{V \cdot a \cdot (k-a)}{L_1 \cdot (k^2-1)} \cdot t \tag{17}$$

The thyristor current i_{TM1} in (16) drops to zero only when:

$$a \cdot k > 1 \text{ for } t > 0 \tag{18}$$

Similarly, the current in the main path falls to zero once the above condition is satisfied.

C. Reverse Recovery State

The current in the main path becomes zero when the auxiliary path is turned on. Due to coupling between L_1 and L_2, the voltage across L_1 becomes $a \cdot V_{L2}$; thus, a negative voltage appears across the main thyristor (T_{M1}), initiating the reverse recovery process. During this period, stored charges are removed from the junction, leading to a complete turn-off of the thyristor and making it ready for the next interruption cycle. The auxiliary path, as a result, behaves as an LC circuit is excited with a voltage source V_{DC} as shown in Fig. 8.

The Voltage across the main thyristor is found as,

$$\begin{cases} V_{TM1} = V_{DC} - V_{L1} \\ V_{L1} = a \cdot V_2 \end{cases} \tag{19}$$

Applying KVL for the LC circuit in Laplace domain:

$$\frac{V_{DC}}{s} = L_2 \cdot (s \cdot I_2(s) - a \cdot I_{peak}) + \frac{I_2(s)}{s \cdot C} \tag{20}$$

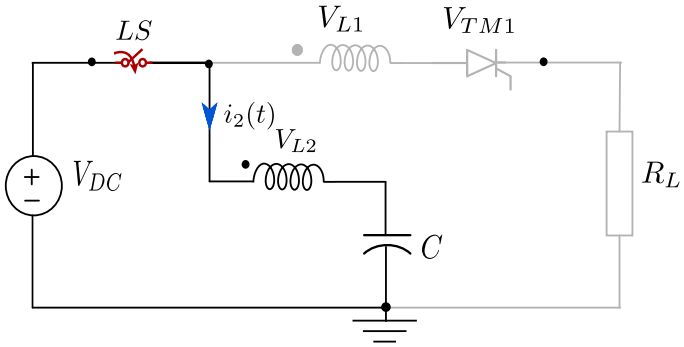


Fig. 8: Equivalent circuit of SSCB after current interruption.

Where $a \cdot I_{peak}$ is the initial condition of the auxiliary path. Upon solving this, the time domain equation is given by:

$$i_2(t) = \frac{V_{DC}}{\sqrt{L_2 \cdot C}} \sin\left(\frac{t}{\sqrt{L_2 \cdot C}}\right) + a \cdot I_{peak} \cos\left(\frac{t}{\sqrt{L_2 \cdot C}}\right) \tag{21}$$

The voltage across the inductor L_2 is given by:

$$V_{L2}(t) = V_{DC} \cdot \cos\left(\frac{t}{\sqrt{L_2 \cdot C}}\right) - a \cdot I_{peak} \cdot \sqrt{\frac{L_2}{C}} \cdot \sin\left(\frac{t}{\sqrt{L_2 \cdot C}}\right) \tag{22}$$

According to (19) the voltage across L_1 is given as:

$$V_{L1}(t) = a \cdot V_{DC} \cdot \cos\left(\frac{t}{\sqrt{L_2 \cdot C}}\right) - a^2 \cdot I_{peak} \cdot \sqrt{\frac{L_2}{C}} \sin\left(\frac{t}{\sqrt{L_2 \cdot C}}\right) \tag{23}$$

Simplifying (23) by using Taylor series expansion, we have:

$$V_{L1}(t) = a \cdot V_{DC} - a^2 \cdot I_{peak} \cdot \frac{t}{C} \tag{24}$$

The voltage across T_{M1} from (19) is given by:

$$V_{TM1}(t) = (1-a) \cdot V_{DC} + a^2 \cdot I_{\text{peak}} \frac{t}{C} \tag{25}$$

For successful commutation, it must be ensured that V_{TM1} in (25) is negative.

D. Selection of components (L_1 and C)

From (16) the condition for L_1 after the current through the main path has become zero is given by

$$L_1 = \frac{V_{DC} \cdot (1 - k \cdot a) \cdot t}{I_{\text{peak}} \cdot (k^2-1)} \tag{26}$$

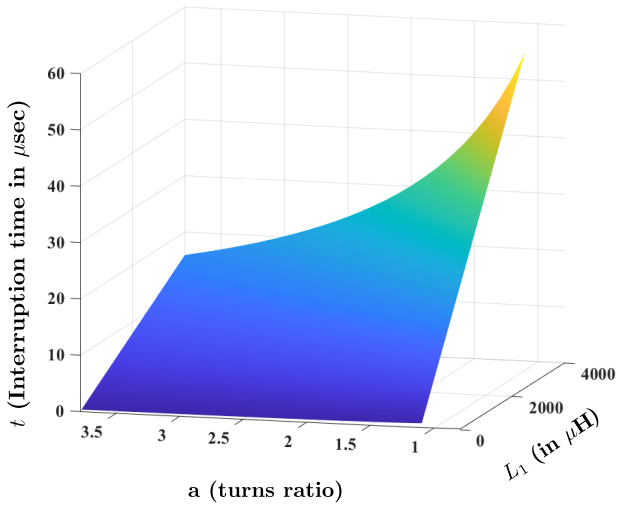
where t is the time taken for the current to drop to zero, a is the turns ratio, k is the coupling coefficient, and I_{peak} is the maximum fault current that reaches before dropping to zero.

The condition for C can be obtained from (25) for $V_{TM1} < 0$:

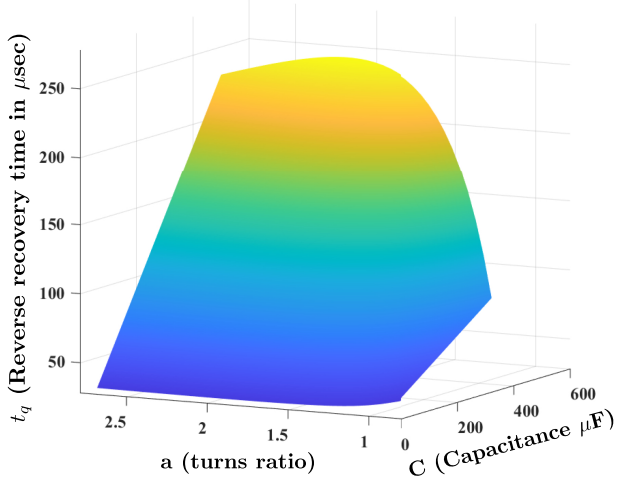
$$C > \frac{a^2 \cdot I_{peak} \cdot t}{V_{DC} \cdot (a-1)}, t = t_q \tag{27}$$

where t_q is the reverse recovery time.

A 3D plot for L_1 in (26) and C in (27) is shown in Fig. 9(a) and Fig. 9(b) respectively. L_2 is determined once



(a)



(b)

Fig. 9: 3D plot: (a) Inductor L_1 (*t vs* L_1 *and* a), (b) Capacitor C (t_q *vs* C *and* a).

a is calculated. Further, a higher k value should be selected; a magnetic core is more suitable when compared to an air core. The capacitance requirement is stated in (27). The rated voltage of this C should be higher than V_{DC}.

E. Design of Coupled inductor

The coupled inductor is designed using a powder-iron E80 core sourced from manufacturer 'Magnetics' with part number: '00X8020E040'. The main winding (L_1) inductance is obtained using (26). The turns ratio 'a' must have a value above '1' to ensure proper mutual coupling and induced voltage on the main winding during the fault condition.

The turns ratio, 'a' is given as :

$$a = \frac{N_1}{N_2} = \sqrt{\frac{L_1}{L_2}} \tag{28}$$

Two E80 powder iron cores are stacked together to double the core cross-sectional area and keep the core flux density within the maximum limit (B_{sat}) of 1.6T at the steady-state operating current. The effective core cross-sectional area becomes,

$$A_e = 2 \times A_{e(\text{single})} \tag{29}$$

where $A_{e(single)}$ is the cross-sectional area of a single core. The inductance of a winding can be expressed as:

$$L = \frac{N^2 \mu_0 A_e}{\frac{l_m}{\mu_r} + g} = \frac{N^2 \mu_0 A_e}{g} \quad (\text{considering } \frac{l_m}{\mu_r} \ll g) \tag{30}$$

The magnetic flux density can be expressed as:

$$B = \frac{\mu_0 N I}{g} \tag{31}$$

where, in (30) and (31), N represents the number of turns of the inductor winding, μ_0 is the permeability of free space, μ_r is the relative permeability of the core material, A_e is the effective core cross sectional area, l_m is the effective length of the magnetic path, and 'g' is the air gap between the cores. The air gap 'g' is obtained from (31) as

$$g = \frac{\mu_0 N I}{B} \tag{32}$$

by substituting (32) in (30), the number of turns in the main winding can be expressed as:

$$N_1 = \frac{L_1 I_1}{A_e B_{sat}} \tag{33}$$

The inductance L_2 and L_3 is can be calculated using (28). Then the number of turns in the auxiliary windings L_2, L_3 is calculated as:

$$N_2 = N_3 = \sqrt{\frac{L_2 g}{\mu_0 A_e}} \tag{34}$$

The mutual coupling between the main winding and auxiliary winding is $M = k\sqrt{L_1 L_2}$, where $0 < k < 1$ is the coupling coefficient. During fault condition, the main and auxiliary inductor windings are in parallel. The equivalent inductance with flux aiding can be obtained as:

$$L_{eq} = \frac{L_1 L_2 - M^2}{L_1 + L_2 - 2M} \tag{35}$$

The equivalent inductance during fault conditions reduces, which ensures that the core does not get saturated [40].

F. Selection of discharging resistor R_1

To determine the required resistance for fully discharging a capacitor, the standard capacitor discharge equation is used:

$$V(t) = V_0 e^{-\frac{t}{R_1 C}} \tag{36}$$

where V_0 represents the voltage to be discharged, R_1 is the resistance needed to dissipate capacitor energy, C denotes the capacitance in Farads, and t corresponds to the discharge time. A capacitor is considered fully discharged when its voltage drops to a negligible level. A common approximation is that it takes about five time constants for the voltage to decay close to zero. This gives the total discharge time as:

$$t_{\text{discharge}} = 5 R_1 C \tag{37}$$

The required resistance for the capacitor to discharge in a known specified time is:

$$R_1 = \frac{t_{\text{discharge}}}{5C} \tag{38}$$

G. Selection of Thyristors (SCRs)

Thyristors in the main path handle the fault current and block the DC bus voltage. The maximum current rating should exceed the preset current value set for transient fault conditions. The thyristor's maximum blocking voltage rating should be chosen to block twice the rated DC input voltage. The thyristors selected for the experiment are of high power capacity.

H. Selection of snubber circuit

To determine the required snubber capacitor, the energy stored in the network inductor (the coupled and the stray inductance energy) is equated to the energy stored in the capacitor. The energy stored in an inductor is given by:

$$E_l = \frac{1}{2} L I_{\text{peak}}^2 \tag{39}$$

Where, E_l is the energy stored in the inductor, I_{peak} is the peak current flowing through the inductor when the fault is interrupted.

The energy stored in a capacitor is given by:

$$E_c = \frac{1}{2} C V_0^2 \tag{40}$$

Where, E_c is the energy stored in the capacitor, V_0 is the voltage across the snubber capacitor (C) to be designed. Equating (39) and (40) results in:

$$C = \frac{L I_{\text{peak}}^2}{V_0^2} \tag{41}$$

This equation determines the required snubber capacitor based on the inductor peak current and DC voltage. The snubber resistor (R_s) is designed to dissipate the energy stored in the snubber capacitor during switch turn on. It helps in damping oscillations and reducing switching transients. For critical damping, the snubber resistor should match the characteristic impedance of the circuit:

$$R_s = \sqrt{\frac{L}{C}} \tag{42}$$

The diode is selected to withstand the peak voltage across the switch during turn-off while also being capable of conducting the charging current of the snubber capacitor.

The MOV connected across the switches is 'SVC 431D-20A', which has a nominal varistor voltage (Vnom) of 430V, and a clamping voltage of (Vclamp) of 710 V. The surge energy rating of the MOV is 140J.

I. Selection of current limiting resistors (R_2 and R_3)

The resistors are chosen to avoid any oscillatory response in the discharged capacitor in the auxiliary path, damping the energy so that the voltage remains within the allowed DC level. Resistors also ensure the peak current in the thyristors does not exceed their maximum permissible limit.

J. Component failure analysis

If the auxiliary path fails to turn on during the transient fault condition, the circuit becomes a simple RL circuit. The current flow path is through $V_{DC} \rightarrow L_1 \rightarrow T_{M1} \rightarrow R_f$ [31].

Minimum fault current ramp rate:

$$V_{DC} = L_1 \cdot \frac{di_1}{dt} + R_L \cdot i_1 \tag{43}$$

Solving the above equation (43) results in:

$$i_1 = \frac{V_{DC}}{R_L} \left(1 - e^{-\frac{R_L \cdot t}{L_1}}\right) \tag{44}$$

During the fault period :

$$\begin{cases} i_1 = I_{fault} \\ R_L = R_f \end{cases} \tag{45}$$

Substituting (45) in (44) and simplifying using Taylor series expansion results in:

$$\frac{I_{\text{fault}}}{V_{DC}} = \frac{t}{L_1} = G_f \tag{46}$$

Where G_f is the fault conductance, and t is the time the fault current takes to rise to a maximum value. From (46), it is evident that G_f is directly proportional to time and increases with time.

The fault current ramp rate (H) can be derived as:

$$H = \frac{G_{\text{f}}}{t} = \frac{I_{\text{fault}}}{V_{DC} \cdot t} = \frac{1}{L_1} \tag{47}$$

$$I_{\text{fault}} = V_0 \cdot G_f = V_0 \cdot H \cdot t \tag{48}$$

If the on-state voltage drop of the thyristor is neglected, then V_{DC}=V_0. Therefore, during any short-circuit fault, the fault current (I_{fault}) is given by (48).

IV. Experimental Validation

This section provides details of the hardware implementation and experimental validation, along with a detailed discussion of the results. The experimental setup and the prototype developed in the laboratory is shown in Fig. 10 and Fig. 11. The proposed SSCB topology is experimentally validated for a DC system with voltage and current ratings of 400 V and 15 A (60 A short circuit), respectively.

The components and equipment used for the proposed SSCB are summarized in the TABLE I.

A. Results and discussion for overcurrent event

This subsection presents experimental results to validate the performance of the proposed topology, as shown in Fig. 2 against over-current faults. Initially, the galvanic isolation switch LS is closed. The main thyristor T_{M_1} is then triggered to establish the power flow to the load. As shown in Fig. 12, a steady state current of 15 A flows through the load considering a system voltage of 400 V and load resistance of 26Ω. The

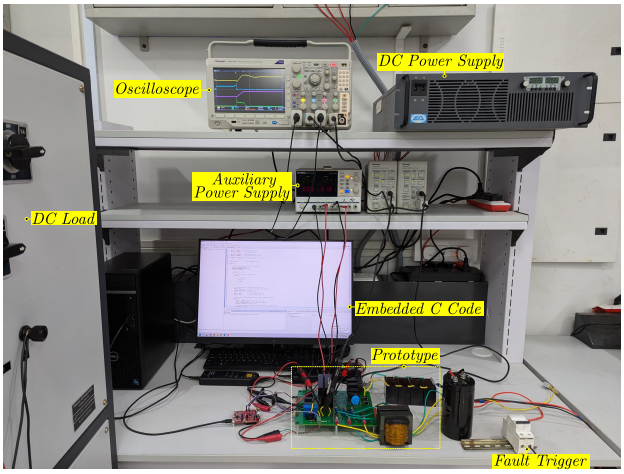


Fig. 10: Experimental setup designed in the laboratory.

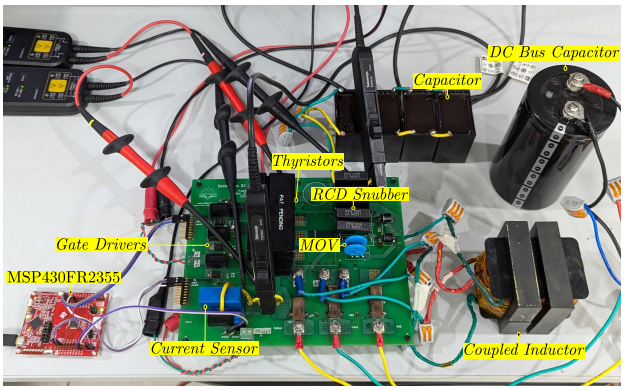


Fig. 11: Close up view of the experimental setup

capacitor (C) in the auxiliary circuit remains uncharged during regular operation, which is evident from Fig. 12, capacitor voltage waveform.

To check the circuit breaker response to an overcurrent event, a step change in load is initiated at the instant t_1 as shown in Fig. 12, and the current through the system increases exponentially. The current rise depends on the inductor L_1 and load resistance (R_L). The LEM LA55-P current sensor, which monitors the load current continuously, sends an analog output voltage signal to the microcontroller. When the load current exceeds the digital value set in the microcontroller corresponding to a preset fault current value of 20 A, a control signal is sent to trigger the commutation circuit thyristor T_2. After a short cumulative delay introduced by the gate driver, the thyristor T_2 turns on at the instant t_2 as shown in Fig. 12. As a result, the capacitor C in the auxiliary circuit starts charging through the coupled inductor L_2. During the capacitor charging process, there is an induced voltage in the auxiliary path inductor winding L_2 due to the mutual coupling. This further induces a voltage on the primary winding L_1 that opposes the DC bus voltage and aids in bringing the main thyristor T_{M1} current down to zero instantly. After a short reverse recovery process, the main thyristor T_{M1} blocks the DC bus voltage, and the fault current is cut off.

The capacitor further continues to charge. The presence of current limiting/charging resistance (R_2) of 2.5 Ω, ESR of

TABLE I: Components and Equipment.

Components / Equipment	Value / Rating	Type / Part No
DC-link voltage (V_{DC})	400 V	enArka 400V/25A
Coupled coils (L_1, L_2=L_3)	4 mH, 1.1 mH	Custom made
Capacitor (C)	200 µF / 450 V	EZPV60117MTC
Load resistance (R_L)	26 Ω	Generic
Charging Resistors (R_2, R_3)	2.5 Ω	Generic
SCRs (T_{M_1}, T_{M_2}, T_1-T_4)	1200 V, 40 A	40TPS12A, Vishay
Snubber Diode	1000 V, 6 A	FR607, EiC Semi
Snubber Capacitance	1 µF	ECW-FG2J105KA
Snubber Resistance	15 Ω, 15 W	Generic
MOV	V_{clamp} = 710 V	SVC 431D-20A

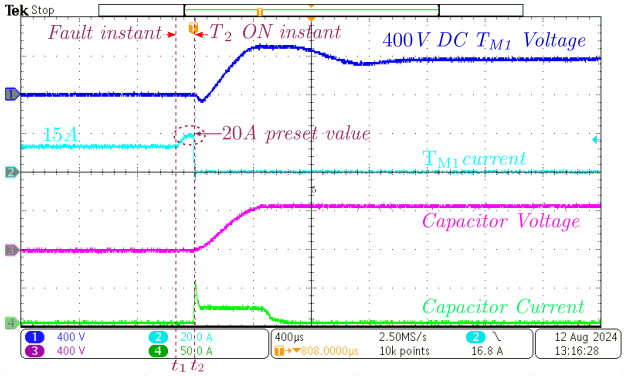


Fig. 12: Experimental result showing overcurrent interruption by the SSCB for a system rating of 400 V, 15 A.

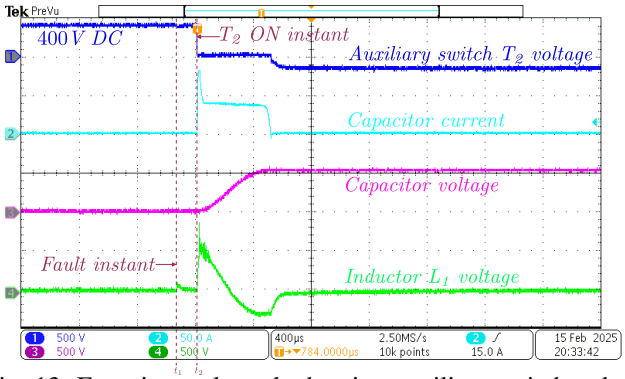


Fig. 13: Experimental result showing auxiliary switch voltage for overcurrent interruption by the SSCB for a system rating of 400 V, 15 A.

the capacitor, and inductor winding L_2 resistance limits the peak capacitor charging current to 22 A. The time taken by the capacitor to reach steady state voltage level is observed to be approximately 480μs. After the capacitor charges to the DC grid voltage, the thyristor T_2 turns off automatically as the current falls below the holding threshold value. Fig. 13 presents the experimental result showing the voltage across the auxiliary thyristor T_2, capacitor current and voltage, and main inductor winding voltage during overcurrent fault interruption.

B. Results and discussion for short-circuit fault

The performance of the SSCB is experimentally validated against short-circuit (low impedance) faults as shown in Fig. 14 for a system voltage of 400 V and a nominal load current of 20A. The short-circuit trip threshold is set to 55A for

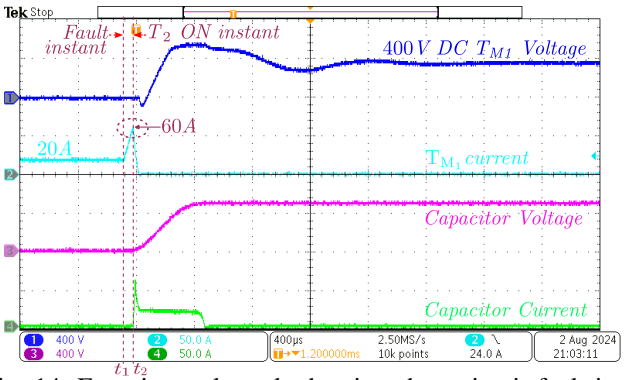


Fig. 14: Experimental result showing short circuit fault interruption by the SSCB at 20 A (nominal, 60 A short circuit).

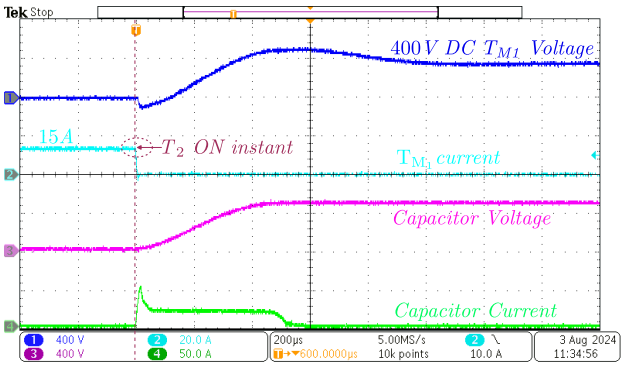


Fig. 15: Experimental result showing manual tripping of SSCB under steady state operation by triggering T_2 for 400 V, 15A.

validation. The circuit breaker operation remains the same, as explained in the discussion for an overcurrent event. A nominal current of 20A flows through the main thyristor by closing the galvanic isolation switch LS and triggering the main thyristor T_{M1}. A short-circuit fault is initiated at the load at time instant t_1, which causes the load current to rise rapidly at a rate determined by the inductance of the main winding L_1. When the current through the main thyristor T_{M1} exceeds the threshold of 55A, the controller sends a pulse at time instant t_2 to trigger the thyristor T_2 in the auxiliary path that charges capacitor C through inductor winding L_2. It may be noted that, after T_2 is triggered, the peak capacitor charging current reaches 60 A, and the capacitor charges to a steady state voltage after 480μs. T_2 in the auxiliary path turns off naturally once the capacitor is charged as the current falls below the thyristor's holding current.

A voltage is induced in inductor winding L_2 during the capacitor charging, resulting in a voltage being induced in the main path winding L_1 as the two coils are magnetically coupled. The induced voltage in L_1 opposes the main source voltage and reduces the current flowing through T_{M1} to zero. After a short reverse recovery process, the current through T_{M1} drops to zero and begins to block the DC bus voltage. It may be noted that the fault current reaches 60 A even though the trip threshold is 55 A; mainly because of the delays in the control, communication, and gate drive systems. The steady-state operation of the circuit breaker can be interrupted for maintenance activities by just triggering the thyristor T_2. This

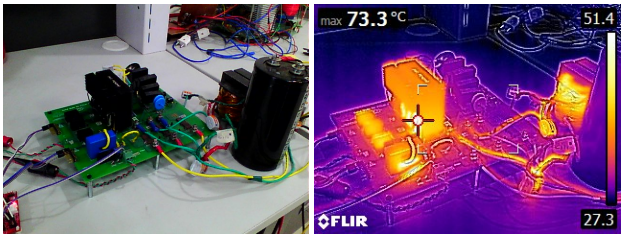


Fig. 16: Thermal image of the experimental setup under continuous operation for 60 minutes at a nominal current of 10A.

feature is validated experimentally, as shown in Fig. 15. The SSCB takes less than 50 μs for the fault interruption (to bring the fault current to zero).

C. Power Loss and Efficiency of the SSCB

Major contributors to power loss in the proposed circuit breaker are the thyristor and winding coil in the main current path, as they continuously carry the load current. The power loss in auxiliary components used in the commutation circuit is not considered since they come into action only during fault events, which occur for a short interval. In the proposed SSCB, only one thyristor T_{M1} and winding L_1 contribute to the power loss in a steady state. The prototype uses a thyristor from Vishay with a forward voltage drop of 0.9 V, and for a system current of 15 A, the conduction loss in SCR is estimated to be about 13.5 W. The power loss in winding L1 is due to its resistance dissipating as heat, affecting the circuit breaker's efficiency. The total winding resistance from the designed coil L_1 is found to be 85 mΩ, and the power loss calculated according to ${i_{L1}}^2 \cdot R_{L1}$ is 19.12 W. The total power loss incurred by the SSCB for a system rating of 400 V and 15 A is 32.75 W. Therefore, the efficiency of SSCB is estimated at 99.46%. The thermal image to assess the heat distribution and performance of the proposed SSCB under continuous operation for 60 minutes at a nominal current of 10A is provided in Fig. 16.

V. Discussion and Comparison

The proposed topology bench marked with the existing topologies as documented in the literature with parameters considered are shown in Table II. The comparison focuses on features that are critical for fault interruption in DC systems, with all power devices considered to their respective voltage and current ratings.

The comparison highlights critical attributes such as stresses and blocking voltages based on the experimental results. The total active and passive components have been calculated for bidirectional power flow and power loss is estimated based on semiconductor devices and coupled inductor windings in the main path. Some of the other comparison criteria are presented in Fig. 17 and Fig. 18, using a bar graph and a donut chart. The pictorial comparison include the number of semiconductor and passive devices and the commutation circuits required for each topology. Additionally, also highlighting advantageous features such as controlled or manual tripping, a discharged state of the capacitor before commissioning, the provision

TABLE II: Comparison of different bidirectional SCR-based SSCBs

Parameter	[31]	[32]	[33]	[34]	[35]	[36]	[37]	[38]	Proposed DCCB
Operating voltage level	<80V	<80 V	<60 V	<50 V	<80 V	<80 V	<300 V	<300 V	<400 V
Current stress level on the main thyristor	-2 A to 1.5 A	7 A	40 A	-1.5 A to 0.5 A	40 A	10.5 A	150 A	-4A to 27 A	<80 A
Switch blocking voltage during turn-off (stress)	30 V	75 V	600 V	25 V	40 V	20 V	300 V	400 V	600 V
Peak forward blocking voltage of thyristor	600 V	200 V	3.3 KV	400 V	200 V	400 V	1200 V	1200 V	1200 V
Number of devices in conduction path	6	7	5	5	6	6	5	6	4
Total number of active components (switches)	1	1	3	2	2	2	4	5	3
Total number of passive components	15	15	22	21	24	21	24	27	16
Power loss when conducting	***	***	*	*	**	**	*	**	*
Fault current reflected to source	×	✓	×	×	✓	✓	✓	×	×
Configurable fault current threshold	✓	✓	✓	✓	✓	×	✓	✓	✓
Common ground	✓	✓	✓	✓	✓	✓	✓	✓	✓

1) Peak forward voltage values are referenced from respective manuscripts.
2) Passive components include snubbers and MOVs across each switch for bidirectional power flow.

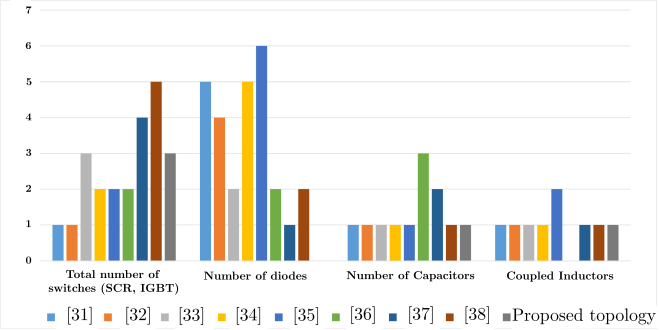


Fig. 17: Bargraph comparing various components of the proposed with other topologies.

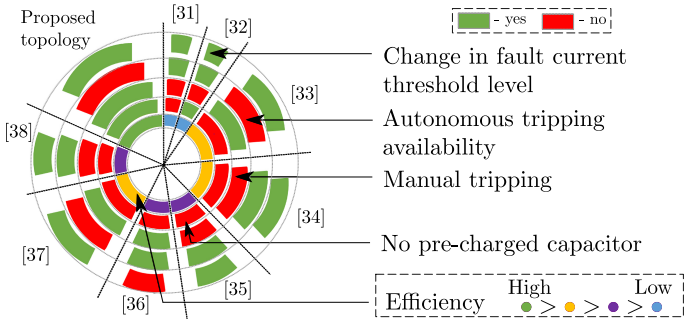


Fig. 18: Donut chart comparing various performance metrics of the proposed SSCB with other topologies.

for an adjustable fault current trip level, and SSCB on-state efficiency across different topologies.

Capacitor charging during both commissioning and recommissioning is a challenge in the design presented in [31], and the presence of two diodes in the main thyristor conduction path reduces efficiency compared to the proposed topology. In [32], the SSCB cannot provide manual tripping, requiring an additional switch for this functionality, which is a limitation compared to the proposed design. In addition, the efficiency is reduced as two diodes and one switch are in the primary conduction path. In [33], the capacitor continuously charges through the diode. There is a switch and diode in the primary conduction path, thus making the SSCB less efficient. In [34], the capacitor must be charged before every commissioning, and a diode is always present in the primary conduction path, leading to additional losses. Moreover, the design lacks the capability for manual tripping. The SCCB presented in [35] utilizes two coupled inductors, unlike the proposed topology, which employs only one three-winding inductor. Additionally, it incorporates three capacitors in the Bi-directional ZSCB, making the design significantly bulkier than the proposed topology.

A notable drawback of the SSCB presented in [36] is the complexity of the analysis. Additionally, the fault current threshold cannot be adjusted due to the lack of coupling between the inductors, a feature the proposed topology addresses effectively. Moreover, the number of components in the primary conduction path is higher, leading to higher on-state losses and thus reducing efficiency. The SSCB design presented in [37] is characterized by the presence of numerous switches and two capacitors. During manual fault clearing, both capacitors dissipate energy in the resonance state. Furthermore, both capacitors must be charged during commissioning and recommissioning, which is not required in the proposed topology. In [38], the circuit breaker does not support manual tripping, and proper capacitor charging is required during commissioning, making it less flexible in comparison to the proposed topology. The presence of two inductors, one diode, and a switch in the primary conduction path makes the design less efficient than the proposed topology.

Overall the three winding coupled inductor SSCB has bidirectional capability with minimal components and no diodes in the main conduction path. The additional winding is utilised

only during fault conditions, while the auxiliary capacitor operates without recharging. This topology also prevents reflected current. Unlike other designs, it does not require a dedicated snubber circuit. All these features provide significant advantage to the proposed topology in comparison to the other topologies.

VI. Conclusion

This article introduces a new coupled inductor-based SSCB topology with fewer components designed to protect the DC microgrid integrated with various renewable energy sources. The proposed topology includes a powder-iron core coupled inductor to reduce the inductor size and a discharged capacitor in the auxiliary path. Reliable current interruption during short-circuit and over-current faults is assured by charging the auxiliary path capacitor through a coupled inductor only during fault conditions. The mutual coupling between the inductor windings induces a reverse voltage across the coupled inductor in the main current-carrying path, which in turn opposes the source voltage, and reduces the fault current through the main thyristor to zero. A comprehensive overview of the operational modes of the proposed topology, followed by an analysis of the circuit during fault conditions to derive the governing equations for the coupled inductor and capacitor selection, is done. The proposed SSCB topology has been experimentally validated for fault interruption against overcurrent events, short-circuit faults as well as manual tripping at a system voltage of 400 V DC and a current of nominal 15 A, with fault current thresholds set at 20 A for overcurrent event and 60 A for short-circuit faults. In all the cases, the fault interruption times limited well below 50 μs.

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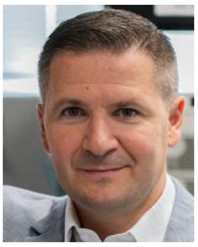

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