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High voltage monolithic pixel sensor in 55 nm technology

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Abstract: The Monolithic Active Pixel Sensors (MAPS) implemented in high-voltage CMOS (HVCMOS) technology are suitable for tracking of high-energy particles in particle physics experiments. To explore performance improvements in smaller technology nodes, a prototype of the next-generation HVCMOS sensor has been done using 55 nm high-voltage technology. This technology offers the benefits of smaller feature size and reduced power consumption.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Solid state detectors

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Contents

1 Introduction

Particle detectors made of silicon have been widely used in experimental particle physics for many years. The HVCMOS sensors employ commercial HV-CMOS chip production technologies and allow combining the sensors with readout electronics on the same chip [1]. HVCMOS pixel sensors are based on deep n-well in p-substrate diodes, with the readout electronics embedded in the deep n-well. The negative bias voltage applied to the p-substrate generates the depletion region and accelerates the charge collection by drift (~1 ns).

A lot of HVCMOS sensors [2–4] have been designed in 180 nm–130 nm processes. Exploration of a smaller technology node with improved performances, such as smaller feature size and reduced power consumption is required for future applications. In this article, an implementation of an HVCMOS sensor in a 55 nm HVCMOS technology has been presented. A prototype chip named CEPCPix1 has been implemented in 55 nm HVCMOS technology with low resistivity substrate (~10 Ω cm). The application can be one particle physics experiment, such as CEPC or LHCb.

This paper is organized into 5 sections. Section 2 describes the overall CEPCPix1 chip architecture. Section 3 describes the pixel structure including its components. Section 4 shows some measurement results. Section 5 gives the conclusion.

2 Chip architecture

The CEPCPix1 pixel detector is a system-on-chip which contains 26 × 26 pixels with size of 25 µm × 25 µm. The whole chip area is about 1.25 mm × 1.25 mm. Every pixel contains a deep n-well as sensor electrode. The size of the deep n-well is 16.7 µm × 16.4 µm. The digital readout part is spatially separated from the pixels and placed at the bottom of the chip. The approach of separating the digital part from the analog pixel electronics has several advantages: the noise caused by digital

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activity is confined to the chip periphery; the power consumption caused by clocked digital lines is smaller; the sensor electrode capacitance is smaller. However, the drawback of this approach are numerous lines which are needed to connect the pixels to their digitizers. To overcome such problems, we have implemented a novel address encoding method.

The pixel matrix is divided into two groups for testing of two different readout methods. Two columns for digital readout and 24 columns for analog readout. The digital periphery receives hit pulses from the digital columns of the pixel matrix and performs timestamp measurements and data uploading.

3 Pixel electronics

The pixel electronics, shown in figure 1, contains a charge sensitive amplifier (CSA), a high pass filter, a comparator, a threshold tune DAC and the output drivers. The pixel electronics are placed in the deep n-well, which is the charge signal collection electrode. The deep n-well is coupled via a capacitor to the amplifier. There is no isolation between PMOS transistors and the deep n-well as in some other HVCMOS designs.

Since the comparator uses PMOS transistor-load and has rail to rail output swing, there is a positive feedback to the collection electrode, which is considered in design.

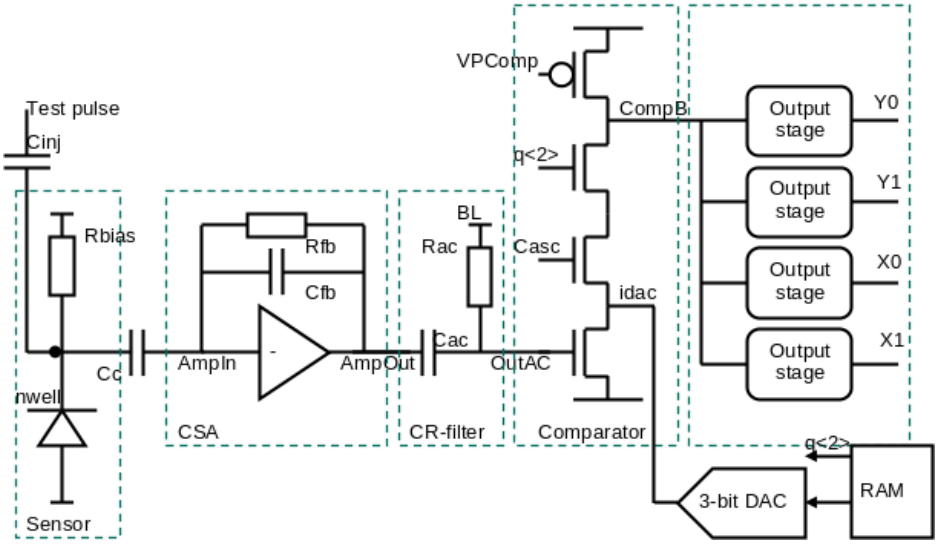

Figure 1. Pixel electronics of CEPCPix1.

3.1 Charge sensitive amplifier

The active part of the charge sensitive amplifier (CSA) is a folded cascode amplifier with source follower as the output stage. CSA receives a capacitively coupled signal (device Cc in figure 1) from the sensor diode. A PMOS transistor has been applied as the input transistor since it has low flicker noise.

To ensure a large amplification, a big transconductance and output resistance are required. Since the transconductance is proportional to the bias current while the output resistance is inversely proportional to the load current, the typical design value of the bias current is about 10 times larger than the load current.

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Each pixel also contains a capacitive injection circuit based on capacitor C_{inj} (figure 1) to generate test signals which allows fast testing and commissioning the sensor chip. The output of the CSA in one pixel per column is connected to the analog multiplexer and an analog output pad.

Compared to older designs in 180 nm technology, the simulated current consumption is very small. The current flow through CSA is 1 µA, and through comparator is ~500 nA. Therefore, the total power consumption per pixel is below 2 µW.

3.2 Comparator

The output signal from the high pass filter (CR-filter in figure 1) — OutAC — is fed into a simple comparator with tune DAC. The DC voltage at the comparator input is defined by the voltage BL. The AC-coupling between the CSA and the comparator prevents this base line variations at the amplifier output influence the threshold. These variations would contribute to the input referred threshold mismatch. The output of the 3-bit current steering DAC is applied for threshold tuning. By adding a programmable offset, we act against threshold variations. The tune-DAC current step can be adjusted using an 8-bit bias-DAC placed at the chip periphery. The signal q < 2 > (stored in a RAM cell) is used to disable the comparator.

3.3 Novel addressing scheme

To test and verify various readout techniques, two readout methods are designed in this chip. The left-most 2 columns use digital design (address is encoded digitally) while the other 24 columns use analog readout (address is encoded as amplitude).

Figure 2 shows the novel addressing scheme. The output of the comparator is connected to 4 output stages in each pixel. All four output stages are used in the case of digital readout and only two in the case of analog readout. The output stage generates a current, and the current is sent via address bus to the impedance amplifier. Therefore, the address line has a constant potential, there is no cross talk to the sensor n-well. The current of the output stage is programmable.

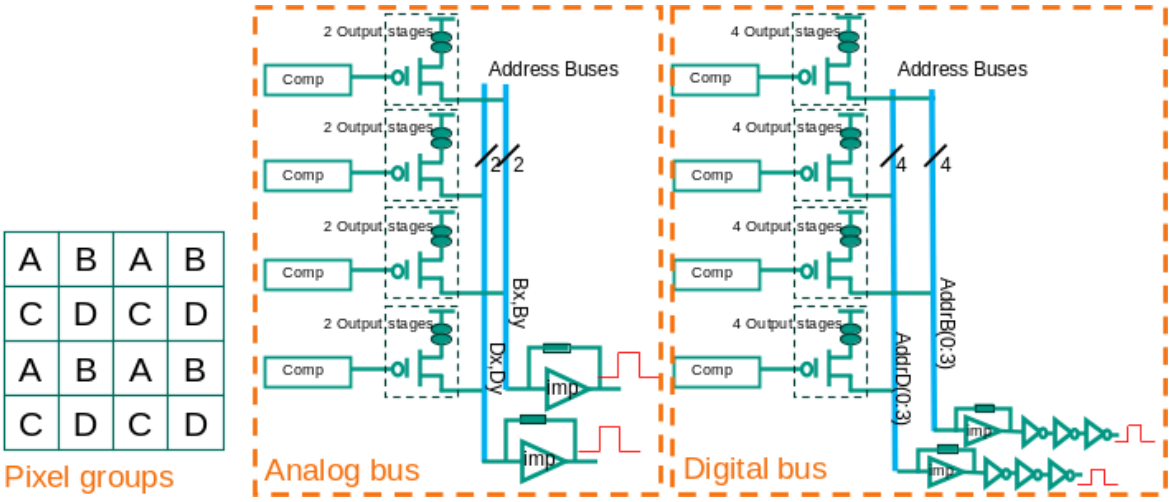

Figure 2. Novel addressing scheme.

3.4 Pixel groups

Since the pixel is very small (25 µm × 25 µm), we can expect that one particle hit causes signals in many pixels. The most probable cluster size (number of simultaneously hit pixels) is up to 4 pixels.

Therefore we divide the pixel matrix into 2 × 2 pixel groups. The pixels in a group are labeled as A, B, C and D. Every pixel in a group A, B, C and D has its own address output. In this way we avoid that address-signals mix if a particle causes signals in two or more pixels of one cluster.

In the case of analog columns, two output drivers per pixel are used. Since there are four pixel groups (A, B, C and D), there are in total eight output lines Ax, Bx, Cx, Dx and Ay, By, Cy, Dy. The outputs "x" of different columns have different amplitudes, the outputs "y" of different rows also have different amplitudes. By measuring the amplitudes of the ABCD-outputs, we can determine the row and column of hit pixel. In case of digital columns, 4 output drivers per pixel are used: Addr(0:3). These four digital signals encode the address. When a pixel gets hit, it generates its address code of a certain pulse length which depends on hit signal amplitude. The addresses are binary coded, code Addr(0:3) = 0000 is not used. Therefore, a hit is detected when at least one address output becomes logic 1. For readout of 15 pixels, 4 address lines are needed. As described above, the pixels of one group (A, B, C and D) have its own 4-bit address bus. The total number of digital address lines is 16: AddrA(0:3), AddrB(0:3), AddrC(0:3) and AddrD(0:3).

Processing of addresses. The analog column outputs are connected directly to pads and will be amplified through an impedance amplifier on the PCB and analyzed with an oscilloscope.

The 16 digital column outputs are connected to the impedance amplifiers placed on chip followed by level shifters. The digital part consists of 4 "time stamp (TS) groups" (time measurement modules), readout control unit (RCU), serializer and configuration block. The time measurement module receives the address, generates a hit pulse (as OR function of address bits) and measures the rising and trailing edge timestamps.

The drive voltages for output stages are generated by internal DACs. The output stage of each analog output group is driven by a certain voltage according to its position. The drive voltages are arranged in sequence order from the left to right in X dimension and bottom to top in Y dimension. In this case, each group is coded with a unique output amplitude to indicate its position.

A timestamp measurement unit detects the hit pulse and measures leading and trailing timestamps as well as captures address information. The timing is controlled by three parameters: capture_position, check_position and detect_max_length. When a pixel is hit, its address is sent to the address bus. When the counter reaches the capture_position, the address information is captured. When the counter reaches the check_position, the address is captured again in comparison with the previous. A mismatch triggers an error bit for overlapping hits. This check procedure only operates when the trailing edge is not detected. The check position value is set according to the pulse length and the rate of overlapping hits. And it should be bigger than capture_position.

4 Measurement results

We first used charge injections to calibrate the chip, with the analog output monitored via an oscilloscope. Capacitance C_{inj} can be estimated by using the parasitic capacitance extraction tool. The measurement result is shown in figure 3. The shows the analog output signal versus different injection amplitudes.

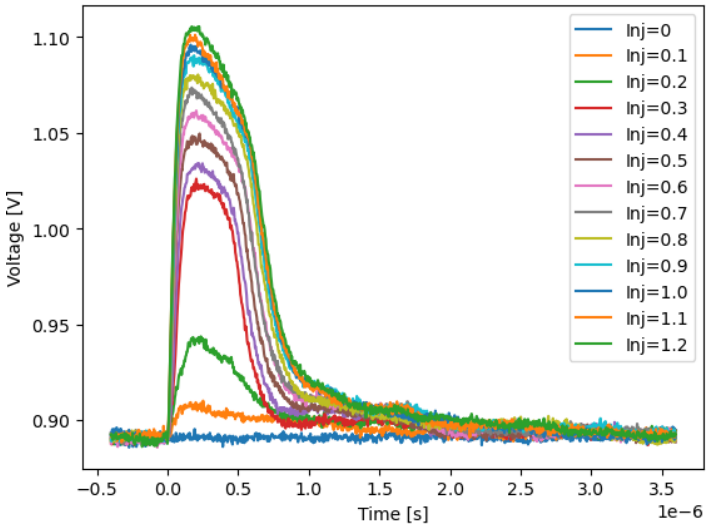

Figure 3. The analog output signal versus different injection amplitude.

To complement the tests with charge injections, the sensor was tested with ^{55}Fe and ^{90}Sr radioactive sources.

Figure 4 shows the histogram of analog output signals when the chip is irradiated with ^{55}Fe radioactive source. The larger peak corresponds to the photons from Kα emission with an energy of 5.9 keV, that generate in silicon about 1640 electron-hole pairs. The peak is at nearly 73 mV and the sigma of the Gaussian fit is 2.6 mV. The corresponding equivalent noise charge is 58 e.

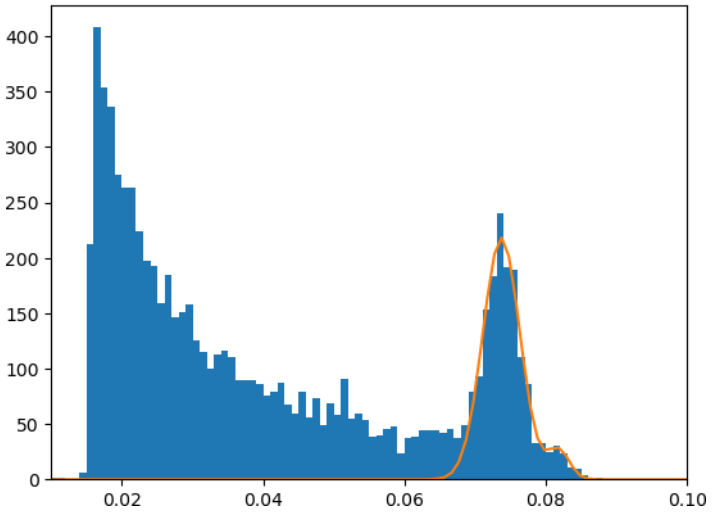

Figure 4. Histogram of analog output signals when the chip is irradiated with ^{55}Fe radioactive source.

A similar measurement has been done with a ^{90}Sr source emitting β-particles (electrons). The measurement result is shown in figure 5. A depletion voltage of 30 V has been applied. The most probable value (MPV) of the distribution is around 50 mV. Calibrated from the results of the ^{55}Fe, we obtain that the MPV is around 1100 e. The depletion depth is estimated to be about 10 µm.

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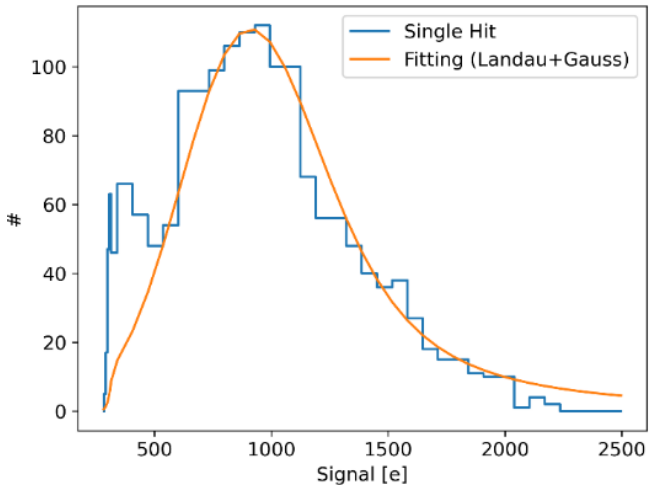

Figure 5. Spectrum of the β-particles irradiated by a ^{90}Sr radioactive source.

5 Conclusion and outlook

A monolithic active pixel detector named CEPCPix1 has been implemented with a 55 nm HVCMOS technology with low resistivity substrate (~10 Ωcm). This chip is designed as a prototype to evaluate suitability of the 55 nm technology for sensor design. The CEPCPix1 chip consists of a pixel matrix, a digital readout module and auxiliary blocks, such as bias DACs. The pixel matrix is composed of 26 × 26 pixels and each pixel size is 25 µm × 25 µm. Additionally, in this prototype, both analog and digital readout is designed. In analog readout, the pixel addresses are recognized by different amplitudes set by internal DACs. In digital readout, the pixel addresses are binary encoded. In both methods, the number of address lines is largely decreased compared to previous HVCMOS designs. The functionality tests have been performed. Equivalent noise charge of 58 e and a β-particle particle signal (most probable value, ^{90}Sr) of 1100 e have been measured. High resistivity substrates (>1 kΩcm) can be offered by the foundry as well. We expect higher signals with chips implemented on high resistivity substrates in the next design iterations.

Acknowledgments

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