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Implementation and Characterization of Monolithic Pixel Detectors in 65 nm CMOS Imaging Sensor Technology

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In the midst of winter, I found there
was, within me, an invincible summer.

Albert Camus, *Return to Tipasa*

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Silz, Mecklenburg-Vorpommern, Germany
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Abstract

This thesis presents the design of a low-power, low-noise front-end based on a transconductance amplifier, conceived for monolithic applications with an emphasis on detecting and amplifying minimum ionizing particle signals.
TPSCo 65 nm transistor technology is currently the leading candidate for developing new monolithic active-pixel detectors for the European Organization for Nuclear Research (CERN) experiments. Prior to the design phase, a comprehensive characterization of this technology node was conducted, focusing on two primary concerns for analog designers in the high-energy physics community: characterization under irradiation, and the study of its analog performance using the Enz-Krummenacher-Vittoz (EKV) model. In the irradiation characterization, several transistor test structures were fabricated and subjected to Total Ionizing Dose (TID) tests up to 1 Grad (SiO_2), followed by annealing at temperatures up to 100 °C. The resulting data were analyzed not only using traditional figures of merit but also employing a custom EKV extractor routine, enabling an in-depth investigation into how irradiation and variations in bulk bias affect the analog performance of transistors of this technology. Both studies confirmed radiation-induced degradation in this node, comparable to other 65 nm technologies. However, the EKV model demonstrated that normalization can mitigate these impacts on transconductance efficiency, making it a powerful tool for analog designers.
Leveraging the insights gathered from the characterization and employing a structured analog design approach, all the various front-end sub-blocks (Charge Sensitive Amplifier (CSA), discriminator, tuning digital-to-analog converter, and feedback) are modeled and implemented. Simulations at schematic and layout levels, successfully demonstrate the feasibility of a low-power, low-noise front-end design using TPSCo 65 nm technology, which can be applied to future applications such as the ALICE ITS3 upgrade.

Zusammenfassung

Diese Dissertation stellt den Entwurf eines stromsparenden, rauscharmen analogen Front-Ends für monolithische Anwendungen auf Basis eines Transkonduktanzverstärkers vor. Der Schwerpunkt liegt auf der Detektion und Verstärkung minimal-ionisierender Teilchensignale sowie geringem Energieverbrauch.
Die TPSCo 65 nm Transistortechnologie ist der derzeit führende Kandidat für die Entwicklung neuer monolithischer aktiver Pixeldetektoren für die Experimente der Europäischen Organisation für Kernforschung (CERN). Vor der Entwurfsphase wurde eine umfassende Charakterisierung dieses Technologieknotens durchgeführt, wobei der Fokus auf zwei primären Anliegen im Kontext der Hochenergiephysik lag: Charakterisierung unter radioaktiver Bestrahlung und Untersuchung der analogen Performanz mit dem Enz-Krummenacher-Vittoz (EKV) Modell. In der Bestrahlungscharakterisierung wurden mehrere Transistor-Teststrukturen gefertigt und Tests der Gesamtionisierungsdosis [engl. Total Ionizing Dose (TID)] bis zu 1 Grad (SiO_2) unterzogen, gefolgt von Wärmebehandlung bei bis zu 100 °C. Die resultierenden Daten wurden nicht nur mit Hilfe traditioneller Kennzahlen analysiert, sondern auch mit einer benutzerdefinierten EKV-Extraktionsroutine. Diese erlaubt eine eingehende Untersuchung, inwieweit Bestrahlung und Variationen in der Substratvorspannung die Performanz der Transistoren dieser Technologie beeinflussen. Beide Studien bestätigten eine strahlungsinduzierte Verschlechterung in diesem Knoten, vergleichbar mit anderen 65 nm Technologien. Das EKV-Modell zeigte jedoch, dass durch Normalisierung diese Auswirkungen auf die Transkonduktanzeffizienz gemindert werden können, was es zu einem mächtigen Entwurfswerkzeug macht.
Die Dissertation schließt mit dem Entwurf eines stromsparenden, rauscharmen Front-Ends basierend auf einem ladungsempfindlichen Verstärker (engl. Charge Sensitive Amplifier, CSA). Unter Nutzung der aus der Charakterisierung gewonnenen Erkenntnisse und eines strukturierten Ansatzes für den Entwurf analoger Schaltungen werden verschiedene Blöcke (CSA, Diskriminator, Digital-Analog-Wandler zur Abstimmung, sowie Rückkopplung) modelliert und implementiert. Simulationen des Front-Ends auf Schaltbild- und Layout-Ebene demonstrieren erfolgreich die Machbarkeit eines stromsparenden, rauscharmen Entwurfs unter Verwendung der TPSCo 65 nm Technologie, das in zukünftigen energiesparenden Anwendungen wie dem ALICE ITS3-Upgrade eingesetzt werden kann.

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List of Abbreviations

ALICE A Large Ion Collider Experiment

ASIC Application-Specific Integrated Circuit

ATLAS A Toroidal LHC ApparatuS

BSIM Berkeley Short-channel IGFET Model

CERN European Organization for Nuclear Research

CMOS Complementary Metal-Oxide-Semiconductor

CMS Compact Muon Solenoid

CSA Charge Sensitive Amplifier

CS Common Source

DAC Digital-to-Analog Converter

DNL Differential NonLinearity Error

DPTS Digital Pixel Test Structure

DRC Design Rule Check

EKV Enz-Krummenacher-Vittoz

ENC Equivalent Noise Charge

EPFL Swiss Federal Institute of Technology Lausanne

ER1 Engineering Run 1

FB Feedback

FE Front-End

FoMs Figures of Merit

GUI Graphic User Interface

H2M Hybrid-to-Monolithic

HEP High-Energy Physics

HL-LHC High Luminosity-Large Hadron Collider

IC Inversion Coefficient

I/O Input/Output

INL Integral NonLinearity Error

ITS Inner Tracking System

LHCb LHC beauty

LHC Large Hadron Collider

LSB Least Significant Bit

MALTA2 Monolithic from ALice To Atlas 2

MAPS Monolithic Active Pixel Sensor

MDC Minimum Detectable Charge

MIPs Minimum Ionizing Particles

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

MOSS Monolithic Stitched Sensor

MOST MOnolithic Stitched sensor with Timing

MOS Metal-Oxide-Semiconductor

NDA Non-Disclosure Agreement

OTA Operational Transconductance Amplifier

PDK Process Design Kit

PSD Power Spectral Density

PSRR Power Supply Rejection Ratio

R2R Rail-to-Rail

RINCEs Radiation-Induced Narrow Channel Effects

RISCEs Radiation-Induced Short Channel Effects

sEKV simplified charge-based EKV

SLVS Scalable Low Voltage Signaling

STI Shallow Trench Isolation

TDC Time to Digital Converter

TID Total Ionizing Dose

ToA Time-of-Arrival

ToT Time-over-Threshold

TTS Transistor Test Structure

List of Symbols

Voltages		
V_{in}	Input voltage	V
$V_{\text{out}}(s)$	Output voltage in the Laplace domain	V
V_{GS}	Gate-to-source voltage	V
V_{TH}	Threshold voltage	V
V_{DS}	Drain-to-source voltage	V
V_{dsat}	Saturation voltage	V
V_{OV}	Overdrive voltage	V
ΔV_{out}	Amplitude of the output pulse	V
V_{Drop}	Voltage drop across the pixel resistance	V
Currents		
$i_{\text{k}}(t)$	Instantaneous current generated on the k detector electrode	A
$I_{\text{in}}(s)$	Input current in the Laplace domain	A
I_{leak}	Leakage current at the detector	A
I_{D}	Drain current	A
$I_{\text{ON}}(\text{TID})$	Maximum drain current at irradiation step	A
$I_{\text{ON}}^{\text{lin}}$	Maximum drain current in linear region	A
$I_{\text{ON}}^{\text{sat}}$	Maximum drain current in saturation region	A
$I_{\text{OFF}}^{\text{sat}}$	Saturation leakage current	A
$I_{\text{D, max}}$	Maximum drain current in saturation	A
I_{SPEC}	Specific current	A
$I_{\text{spec}\square}$	Specific current per square	A
I_n^2	Noise power spectral density (PSD)	A^2/Hz
I_{LSB}	Least Significant Bit (LSB) current of the DAC	A
$\%I_{\text{ON}}$	Percentage of variation of the maximum drain current	1
Capacitances		
C_{FB}	Feedback capacitance	F
C_{L}	Load capacitance	F
C_{in}	Input capacitance	F
C_{DET}	Detector capacitance	F

C_{T}^2	Total capacitance, calculated as $C_{\mathrm{FB}}C_{\mathrm{in}} + C_{\mathrm{FB}}C_{\mathrm{L}} + C_{\mathrm{in}}C_{\mathrm{L}}$	F
C_{OX}	Gate oxide capacitance per unit area	$\mathrm{F/m^2}$
C_{OXU}	Unitary gate oxide capacitance per unit area	$\mathrm{F/m^2}$
C_{GS}	Gate-to-source capacitance	F
C_{GB}	Gate-to-bulk capacitance	F
C_{GD}	Gate-to-drain capacitance	F
C_{GSU}	Gate-to-source unitary capacitance	F
C_{GBU}	Gate-to-bulk unitary capacitance	F
Resistances		
R_{FB}	Feedback resistor	Ω
r_{ds}	Output resistance between drain and source	Ω
R_{pix}	Resistance of each pixel	Ω
$R_{\square}$	CMOS technology metal resistance	Ω/m
Time Constants		
τ_r	Rise time	s
τ_{f}	Falling time	s
Jitter	Jitter	s
Physical and Material Constants		
K	Constant	$\mathrm{MeV\,cm^2}$
m_e	Electron mass	kg
c	Speed of light	m/s
Z	Atomic number of absorption medium	1
A	Atomic mass of absorption medium	u
β	Velocity of the traversing particle	m/s
γ	Lorentz factor	1
W_{max}	Maximum kinetic energy transferable to an electron by a charged particle	MeV
I	Mean excitation energy	MeV
δ	Density-effect correction	1
z	Charge of the incident particle	$\mathrm{e^-}$
k	Boltzmann constant	J/K
T	Absolute temperature	K
ϵ_{OX}	Permittivity of the oxide layer	F/m
L_{sat}	Channel length where carrier drift velocity saturates	m
λ_{c}	Saturation velocity parameter	1
$f(\mathrm{IC})$	Function of Inversion Coefficient	1
q_{s}	Normalized drain current parameter	1
VS	Velocity of saturation effects	1
Q_{min}	Minimum Detectable Charge (MDC)	$\mathrm{e^-}$
Semiconductor Parameters		
D_n	Diffusion constant for electrons	$\mathrm{m^2/s}$

D_p	Diffusion constant for holes	m^2/s
v_n	Average drift velocity for electrons	m/s
v_p	Average drift velocity for holes	m/s
E	Electric field	V/m
μ_n	Mobility for electrons	$\mathrm{m}^2/(\mathrm{V\,s})$
μ_p	Mobility for holes	$\mathrm{m}^2/(\mathrm{V\,s})$
μ_0	Channel mobility	$\mathrm{m}^2/(\mathrm{V\,s})$
K_μ	Transconductance parameter	A/V^2
U_T	Thermal voltage	V
W	Transistor width	m
L	Transistor length	m
IC	Inversion Coefficient	1
VS	Velocity of saturation effects	1
n	Slope factor	1
$J_{n,\mathrm{diff}}$	Diffusion current density for electrons	A/m^2
$J_{p,\mathrm{diff}}$	Diffusion current density for holes	A/m^2
∇n	Concentration gradient of electrons	$1/\mathrm{m}^3$
∇p	Concentration gradient of holes	$1/\mathrm{m}^3$
G_FB	Transconductance of the feedback transistor	S
G_m	Transconductance of the input transistor	S
Noise Parameters		
$e_n(s)$	Noise source	V
$e_n(\omega)$	Noise spectrum	V
V^2_rmsOUT	Output noise power	V^2
Γ	Noise related parameter	1
σ_{eq}	Equivalent noise standard deviation	1
ENC	Equivalent Noise Charge	1
Other Parameters		
Q_in	Input charge	C
N	Number of pixels per column	1

1 Introduction

Pixel detectors, arrays of individual sensors, are powerful tools for both particle physics and imaging. In the context of High-Energy Physics (HEP) experiments, tracking detectors typically consist of multiple layers of pixel silicon sensors and are used to reconstruct the trajectories of particles. Each pixel on the detector collects the electric charges generated upon interaction with a particle and incorporates circuitry to process the signal. The processing electronics in the pixel sensor are influenced by environmental factors such as radiation or temperature, which in turn affects the overall operation of the pixel detector. Therefore, the readout electronics integrated into each pixel sensor must align with the performance requirements of the pixel detector. Additionally, the requirements imposed on each Application-Specific Integrated Circuit (ASIC) must take into account the peculiarities of integrated circuit design and the specific transistor technology used [1].

The detectors in operation at the Large Hadron Collider (LHC) of the European Organization for Nuclear Research (CERN) are examples of HEP experiments. The LHC accelerates particles to a center-of-mass energy of 14 TeV in two opposing rings with a circumference of 27 km through several accelerator stages. The particle beams are brought to collision at four interaction points, where the four largest experiments—A Toroidal LHC ApparatuS (ATLAS), Compact Muon Solenoid (CMS), A Large Ion Collider Experiment (ALICE), and LHC beauty (LHCb)—are positioned. New particles are created from the energy set free during the collisions and spread out in all directions from the collision point. A large magnet system bends the paths of charged particles. Different detecting subsystems, arranged in layers around the collision point, record positions, momenta, and energies, allowing for their individual identification [2]. Figure 1.1 shows, as an example, a transverse slice through CMS, with the vertex detector positioned closest to the beam pipe [3].

High-energy physics experiments aim to increase the energy of colliding particles and achieve higher collision rates. The TPSCo 65 nm monolithic Complementary Metal-

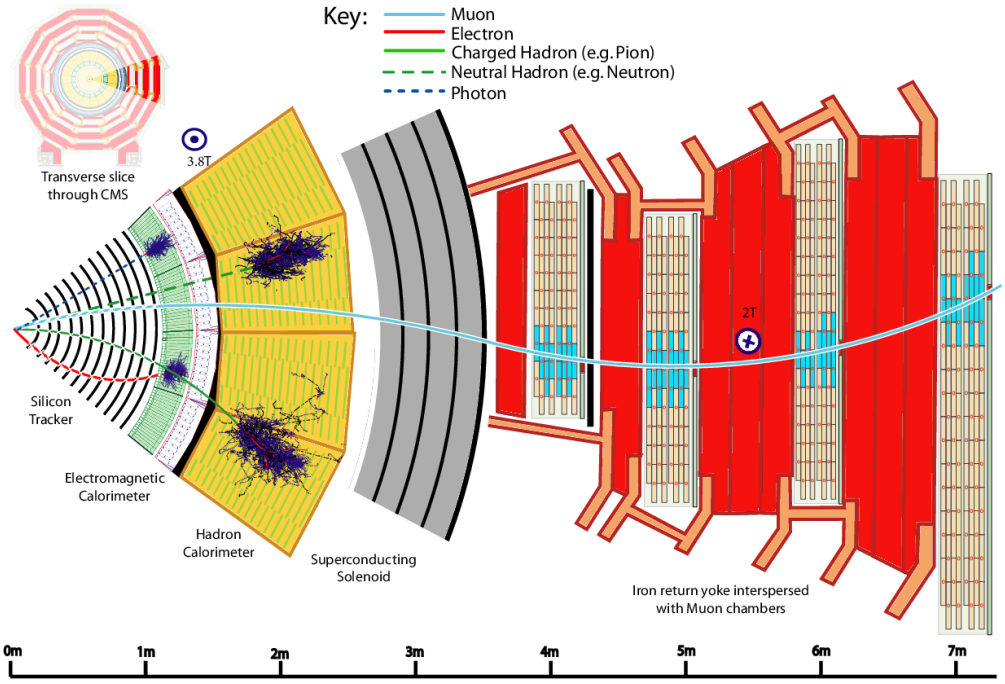

Figure 1.1: Transverse slice through CMS. The vertex detector, positioned closest to the beam pipe, is immersed in a magnetic field. This magnetic field bends the tracks of charged particles, enabling the measurement of their momenta [3].

Oxide-Semiconductor (CMOS) imaging process is the next candidate for developing new monolithic active CMOS pixel sensors for vertex measurements at a high rate and in hostile environments at the High Luminosity-Large Hadron Collider (HL-LHC) upgrade at CERN. The higher luminosity[I] will lead to a maximum expected Total Ionizing Dose (TID) of up to 1 Grad after ten years of operation. On the other hand, the move to more advanced nodes with smaller feature sizes should allow for reduced power consumption and more sophisticated signal processing.

Therefore, in the design of analog circuits for the HEP physics community, two steps are essential: understanding the experiment and future application of the pixel sensor, and understanding the peculiarities of the transistor technology in use. This thesis presents the development of analog readout electronics and their sub-blocks using the TPSCo 65 nm imaging process, while offering a preliminary characterization of this technology under radiation sources and an understanding of its analog performance using the Enz-Krummenacher-Vittoz (EKV) model. The design will focus on figures of merit like pixel size, noise, power consumption, response time, and radiation tolerance, using a structured analog CMOS design approach [5] that takes into account the advantages and drawbacks of the smaller nodes.

[I] Luminosity is the quantity that measures the ability of a particle accelerator to produce the required number of interactions [4].

1.1 Structure of the Thesis

The thesis is organized as follows:

- Chapter 2 offers an introduction to pixel detectors used in high-energy physics experiments. It covers foundational topics such as the PN junction, sensor and charge generation (Bethe-Bloch formula), signal formation (Ramo theorem), and signal processing. It then presents two recent front-end designs using the TPSCo 65 nm monolithic image sensor technology. Finally, it discusses considerations for designing front-ends based on a Charge Sensitive Amplifier (CSA), focusing on noise, stability, and time performance.

- Chapter 3 covers the characterization of the TPSCo 65 nm technology under radiation sources. It begins with an introduction to the theory underlying the main radiation-induced effects in transistors, depending on where the ionizing charges accumulate: gate oxide, shallow trench isolation, or spacers. The chapter then presents results at 1 Grad, followed by a detailed study of narrow channel and short channel effects. Given that two different transistor processes are available, a preliminary comparison of their behavior under irradiation is provided. Finally, the radiation response of thick oxide devices is discussed.

- Chapter 4 explores the impact of radiation-induced and back bias effects on the analog design parameters of the TPSCo 65 nm. It begins with an introduction to the theory related to the modeling of Metal-Oxide-Semiconductor (MOS) devices using the EKV model. This is followed by a proposal for an EKV parameters extractor implemented in Python. The chapter then examines the effects of radiation-induced effects on large-signal characteristics, and EKV model parameters. Furthermore, it addresses the impact of radiation on small-signal characteristics, covering effects on output conductance and transconductance efficiency. Finally, the chapter discusses the influence of back bias on analog performance.

- Chapter 5 covers the implementation of a novel low-power and low-noise front-end. It begins by outlining the specifications and objectives of the design. The chapter then explores the fundamental limits on designing low-power and low-noise front-ends. Following this, it details the design procedure, including the development of each of the front-end sub-circuits. Schematic simulations are discussed, along with post-layout extraction simulations that address layout considerations, such as the influence of parasitic capacitances on performance. The chapter concludes with a comparison of the new front-end with the H2M and MOSS front-ends.

- Chapter 6 finalizes the thesis, presenting general conclusions and outlook.

1.2 Thesis Contributions

The present thesis delves into the characterization of TPSCo 65 nm imaging process and the development of circuits using this node. To the best knowledge of the author, the thesis contains the following novel contributions:

- Characterization of the TPSCo 65 nm technology under irradiation. The results were previously published in [6].
- Measurements of nMOS transistors under different back-gate biases. This lead to the clarification of the unexpected behavior described in [7], where the gain of the presented analog circuit decreased with increasing reverse substrate bias voltage, contradicting simulation results.
- Proposal of a Python routine to extract EKV parameters at different irradiation levels and back biases (available at [8]). It is based on the SEKV-E extractor [9] developed at Swiss Federal Institute of Technology Lausanne (EPFL) but with three main differences: (i) the velocity of saturation effect is not taken into account until the final stage of the extraction (ii) the code avoids pre-filtering of the data to prevent missing information (iii) the overfitting issue due to the nonlinearity of the nonlinear least-squares is rectified by weighting the cost function.
- Study of the TID effects on the TPSCo 65 nm technology using the four main parameters of the simplified charge-based EKV (sEKV) model following the methodology previously applied to a 28 nm hybrid node [10–12].
- Study of limitations on the design for low-power and low-noise front-ends applied to a monolithic node, following the methodology presented in [13] on an hybrid node.
- Design of a low-noise low-power front-end based on a transconductance amplifier using the Inversion Coefficient (IC) design approach.
- Contribution to the development of the Hybrid-to-Monolithic (H2M) prototype chip and its analog periphery, which lead to the following publications [14–18]. Several sub-blocks of the analog periphery where used at the MOSS prototype chip, presented in [19].

In general terms, this thesis covers the main aspects of the design of analog blocks for the high-energy physics community, using a front-end as reference block. The thesis has been written such that it may serve as a comprehensive guide for newcomers to analog design, providing direction on where to begin their research and how to integrate the various aspects into a practical application.

2 Monolithic Active Pixel Detectors

During the past years pixel detectors have become a crucial tool for particle physics and imaging, enabling detailed detection of particle interactions. Each pixel in these detectors collects charges from particle interactions and processes the signal with integrated circuitry. The detection occurs at the sensor, while the analog readout electronics translate the current pulse into a voltage that can be processed by digital electronics, allowing not only photon counting but also time of arrival and energy measurements.

The performance of these pixel detectors significantly impacts the overall precision of tracking. As HEP experiments advance towards higher collision energies and rates, optimizing these pixel detectors and their sub-circuits for more precise position and momentum resolution becomes critical to meet the stringent requirements of these systems. For the effective development of these detectors it becomes essential the understanding of the physics underlying the detection process, and the study of the mathematical constraints involved in analog readout electronics.

This chapter delves deeper into pixel detectors used in the context of high-energy physics experiments. Section 2.1 offers an introduction to pixel detectors going from the PN junction forming the collection electrode to the processing chain covering the signal formation. Section 2.2 focuses on Monolithic Active Pixel Sensor (MAPS). Section 2.3 introduces two recent front-end designs using the TPSCo 65 nm monolithic image sensor technology which serves as a starting point for the design presented in Chapter 5. Finally, Section 2.4 introduces some considerations on the design of front-ends based on a CSA regarding noise, stability and time performance.

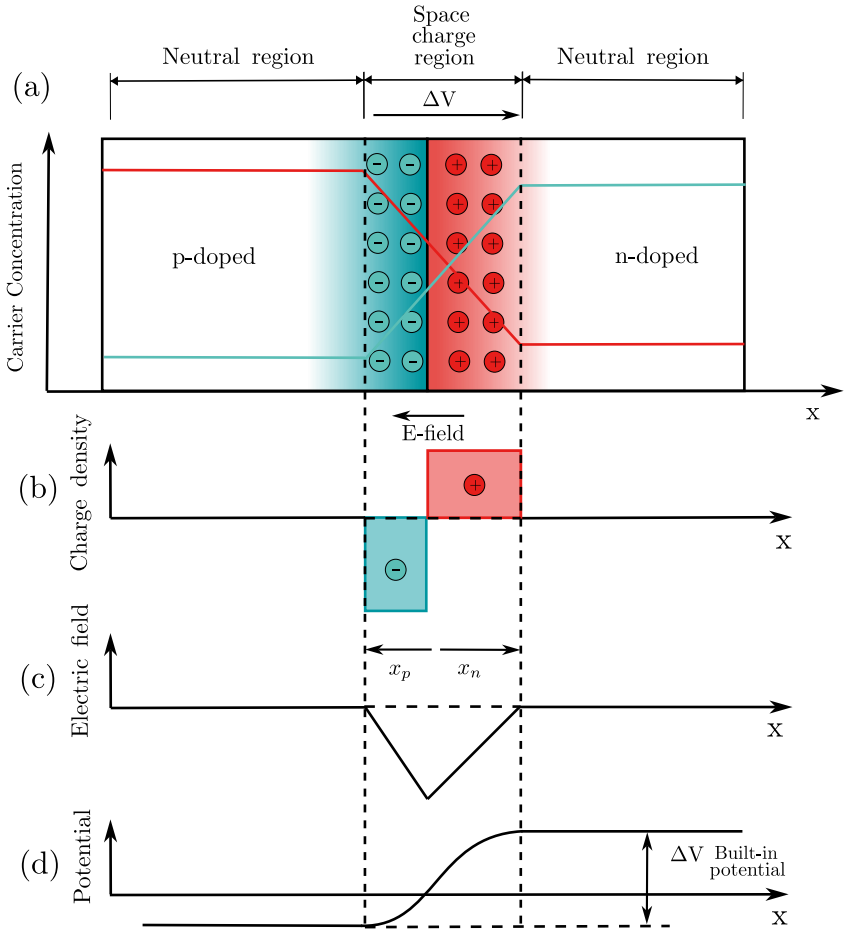

Figure 2.1: The PN junction: a) structure b) space charge density c) electric field distribution and d) potential distribution. Adapted from [20].

2.1 Foundations on Pixel Detectors

2.1.1 The PN Junction (Drifting and Diffusion)

Silicon is a chemical element with four electrons in its valence layer. Taking a crystal of silicon and doping it with an element that has one more electron in its valence layer, such as phosphorus (which has five electrons), results in an N-type semiconductor with an excess of electrons. On the other hand, doping the crystal with an element that has three electrons in its valence layer, like boron, creates a P-type semiconductor with a lack of electrons (an excess of holes) in its lattice.

The contact area between the P-type and N-type is called the PN junction, also known as a diode [21]. Figure 2.1 shows an schematic representation of this junction, together with the space charge density, electric field distribution, and potential distribution. When the N-type and P-type semiconductors are put together, the free electrons will diffuse into the P-type and recombine with the free holes. The same will happen with the free holes

in the P-type, which will diffuse into the N-type. This exchange of carriers is done by diffusion and is described by:

$$J_{n,\text{diff}} = -q \cdot D_n \cdot \nabla n \tag{2.1}$$

$$J_{p,\text{diff}} = q \cdot D_p \cdot \nabla p \tag{2.2}$$

where $J_{n,\text{diff}}$ and $J_{p,\text{diff}}$ are the diffusion currents per unit area for electrons and holes, ∇n and ∇p are the concentration gradients, and D_n and D_p are the diffusion constants [22].

The charge carriers will recombine, forming a charge carrier-free area known as the depletion region. This is a space charge area with its own built-in potential due to the fixed ions in it and where the electric field is directed from the N-type to the P-type (positive to negative). Therefore, any electron or hole in this field will drift following the electric field

$$v_n = -\mu_n \cdot E \tag{2.3}$$

$$v_p = \mu_p \cdot E \tag{2.4}$$

where v_n is the average drift velocity for electrons, v_p for holes, E is the electric field, and μ_n and μ_p are the mobilities for electrons and holes respectively.

2.1.2 The Sensor and Charge Generation (Bethe-Bloch Formula)

On pixel detectors, the sensing part is a reverse-biased PN junction. Applying a positive voltage between the cathode (N-type) and the anode (P-type) will attract the free electrons towards the positive potential, leaving positive ions behind in the depletion regions. Likewise, the holes will be attracted by the negative potential, leaving behind negative ions in the depletion region. Increasing this reverse voltage will fully deplete the sensor. The PN junction in pixel detectors is achieved by adding N-type implants on a P-type substrate (or the other way around). The sensor is a part of the system responsible for generating electrical signals when it interacts with a ionizing particle.

The amount of energy deposited by an ionizing particle can be described by the Bethe-Bloch formula [23]:

$$-\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2m_e c^2\beta^2\gamma^2 W_{\max}}{I}\right) - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right] \tag{2.5}$$

where K is $0.307\,075\,\mathrm{MeV\ cm^2}$, m_e the electron mass, c the speed of light, Z the charge of the incident particle in electrons, A the atomic number of absorption medium, β the velocity of the traversing particle in units of the speed of light, γ the Lorentz factor, $W_{\max}$ the maximum kinetic energy which can be transferred to an electron by a charged particle, I the mean excitation energy, and δ the density-effect correction.

Along the particle trajectory, electron-hole pairs are produced. Minimum Ionizing Particles (MIPs) produce ~ 80 electron-hole pairs per µm path length in Si. This number is valid for thick layers, and it will vary with the thickness of the layer [24]. These electron-hole pairs manifest as a current pulse to be used by the detection system. Silicon is a material used to detect low-energy photons (up to $\sim 20\,\mathrm{keV}$), and it is widely used in particle detector applications (especially monolithic applications) due to a wide understanding of its properties, cost-effectiveness, and its extensive use in industrial, and commercial electronics. However, other materials such as Germanium (Ge), Gallium Arsenide (GaAs), Cadmium Telluride (CdTe), Cadmium Zinc Telluride (CdZnTe), and Diamond are used in hybrid applications, where the sensor material can be externally connected to the readout electronics depending on the energy of the detected particle [25].

2.1.3 Signal Formation (Ramo Theorem)

In a PN junction with a built-in electric field directed from positive to negative voltage, if a charged particle passes through the sensor, it will generate electron-hole pairs. Under this electric field, they will drift parallel to it, inducing a current pulse on the detection electrodes that will vanish when the charges are collected.

The instantaneous current generated on a k detector electrode by the movement of a charge q with a drift velocity vector $\boldsymbol{v}$ and a weighting field vector $\boldsymbol{E}_w$ can be calculated using the Ramo theorem [26] as:

$$i_{\mathrm{k}}(t) = q \cdot \boldsymbol{v} \cdot \boldsymbol{E}_w \tag{2.6}$$

To calculate the weighting field vector $\boldsymbol{E}_w$, the electrode of interest should be raised to unit potential, while all other electrodes are set to zero potential. Technology Computer-Aided Design (TCAD) simulations are needed to study how the sensor geometry, charge and electric field distribution affects the sensor performance. TCAD [27] simulations are a helpful tool for sensor designers to understand how the shape and delay of this current

pulse are going to change depending on the position of the charge deposited with respect to the collection electrode. Knowing this information, the front-end designer can tune the integration time of the system so that it is significantly longer than the collection time, ensuring the input pulse can be modeled as a Dirac pulse; making it possible to achieve a complete integration of the charge, avoiding ballistic deficit effects. This simplifies the mathematical analysis of the front-end amplifier. This simulation of the detector signal is also important for the optimization of the noise performance of the front-end linked to the detector capacitance which is proportional to the width of the depletion region.

2.1.4 Processing Chain

The current pulse generated by the sensor is amplified and shaped in the front-end electronics. Various signal acquisition modes are available, including current mode, voltage mode, or a mode incorporating a CSA at the input [28]. A schematic representation of front-end electronics utilizing the CSA mode is presented in Figure 2.2.

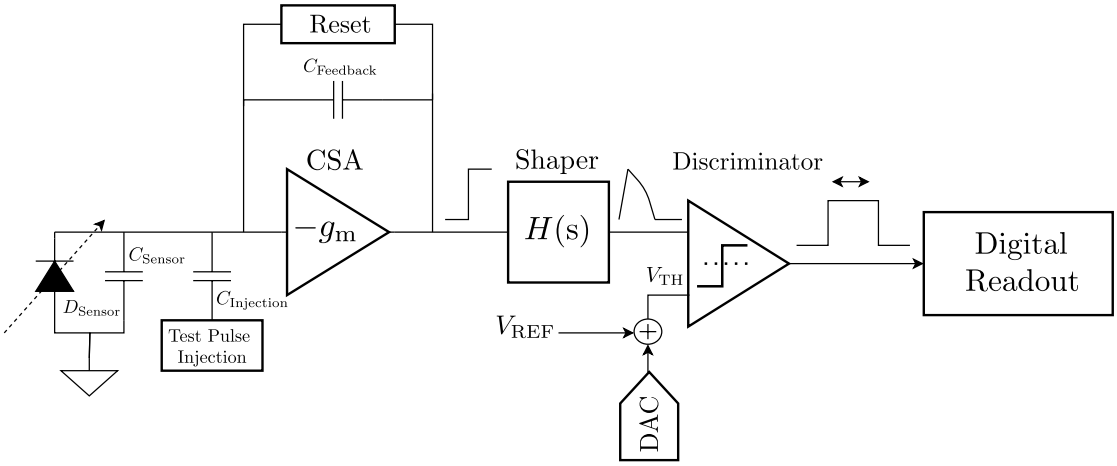

Figure 2.2: Block diagram of a common processing chain. The signal is generated at the sensor, which is modelled as a diode in parallel to a capacitance. This signal is integrated by the CSA, filtered by the shaper and compared to a threshold at the discriminator.

In the CSA mode, a current signal from the sensor is integrated in a charge-sensitive preamplifier. The preamplifier's output generates a voltage step proportional to the total charge in the detector. In a simplified version, this voltage step is directed to a discriminator, comparing it to a threshold signal and generating a full swing signal, whose rising/falling edge and pulse duration can be use to determine the arrival time of the particle or its energy. Signals below the threshold-defined minimum energy are excluded from further processing, while signals above the threshold are handled by the logic. By setting a sufficiently high threshold and ensuring a high CSA gain, noise hits can be eliminated, resulting in noise-free data acquisition. In other cases, the voltage pulse from the CSA is directed to a shaper. The shaper adjusts pulse timing according to specific requirements and filters out noise to optimize the signal-to-noise ratio.

Once the signal reaches the digital logic, four different measurements are available, depending on the digital logic configuration and whether data is processed on the pixel or in the periphery [29]:

- The Time-of-Arrival (ToA) measurement involves storing information about the time when a hit occurred. This can be achieved using a global time-stamp or a shutter signal as a time reference as depicted in Figure 2.3.
- The Time-over-Threshold (ToT) measurement, as represented in Figure 2.3, extracts the energy of the signal by measuring the time during which the output of the amplification stage remains above the applied threshold. The duration of this time is proportional to the charge generated in the sensor.
- Storing energy information also allows for correcting the "time walk" effect. Time walk occurs when different ToA values are recorded based on the input charge amount. ToT information helps extract the delay for the signal to cross the threshold, allowing for time walk correction and improving timing measurement accuracy.
- For applications where only the number of detected particles is crucial and detailed time and energy information is not needed, photon counting is a suitable measurement method. Photon counting involves counting the number of hits above the applied threshold.

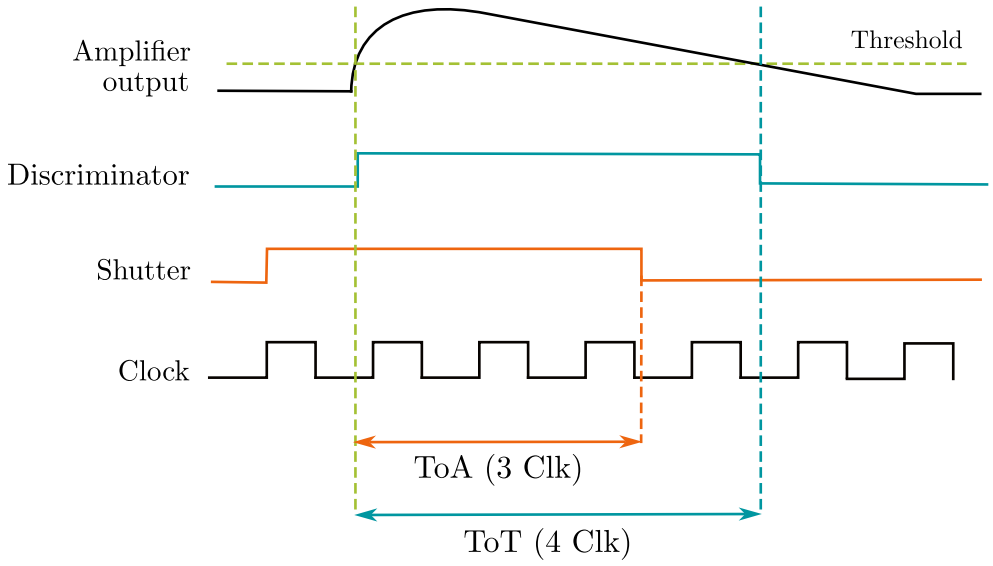

Figure 2.3: Graphical representation of the ToT and ToA measurements.

2.2 Radiation Detectors

Radiation detectors are formed by an array of individual sensors. In most cases, each of them will have its own readout system. In the case of silicon, these matrices are built as an array of reversed-bias diodes, each with a geometrical shape defined by the requirements of the experiment (area covered and spatial resolution). At this point, there are two different types of detectors depending on whether the readout circuit shares the same substrate as the sensor (monolithic) or if they are two independent entities (hybrid).

2.2.1 Hybrid Pixel Sensors

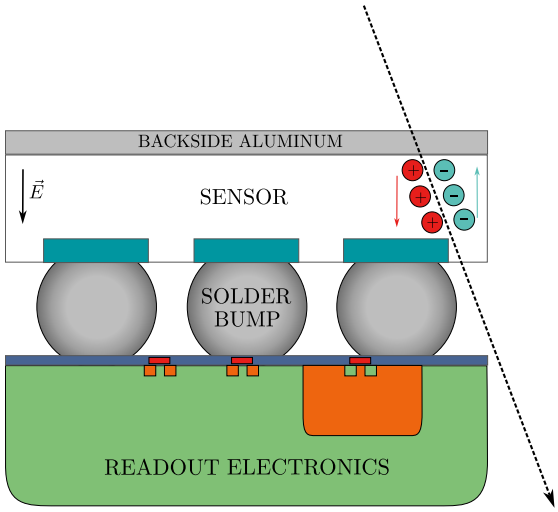

Figure 2.4: Simplistic representation of a hybrid sensor. The backside aluminum is connected to a positive potential (attracting electrons) while the other side is connected to a negative potential. Once there is ionization on the sensor, the holes while be attracted by the negative bias and detected by the readout electronics.

Hybrid pixel sensors, depicted in Figure 2.4, are formed by a sensor and the readout electronics. The pixel sensor matrix is crafted from a specified sensor material, while the readout electronics are developed through a standard CMOS process, mirroring the array configuration of the sensor matrix. This autonomy between the readout electronics and the sensor stands out as a primary advantage of these detectors, enabling separate optimization.

The selection of the sensor material depends on how the incident charge will interact with the material and the specific requirements of the experiment or application. For instance, silicon proves suitable for detecting MIPs due to its low energy bandgap (1.12 eV) [30, 31]. However, for particle tracking, materials like diamond are more fitting, providing higher radiation tolerance and a larger energy bandgap (5.6 eV) [32]. The material selection considers factors such as density, energy bandgap, atomic number, or carrier lifetime.

Conversely, readout electronics can be optimized for low-noise ($100\,e^-rms$), radiation hardness, and detection rate [33]. This performance makes hybrid pixel detectors the ideal choice for tracking applications in extreme radiation environments, as evidenced by their use in the inner layers of two LHC detectors: ATLAS and CMS [34].

The connection between the sensor and the readout chip is established in every pixel using flip-chip and bump-bonding [35]. However, the bump-bonding technique imposes limits on the minimum pixel size and increases sensor capacitance (10-100 fF), leading to higher power consumption for the same performance and, consequently, a larger material budget. Moreover, the module assembly, is a complex and expensive process, particularly for large-area detectors.

2.2.2 Monolithic Active Pixel Sensors

There are different flavours of MAPS (e.g. the HVCMOS, SiGe, or CCDs of SOI [36–38]), yet we will describe the TPSCo 65 nm type. This kind of MAPS integrate the sensor and readout electronics on the same substrate, utilizing silicon with a thin epitaxial layer, typically a few micrometers thick, making them the standard for visible light detection. Figure 2.5 depicts a typical implementation of a monolithic sensor, where the collection electrode is formed by implanting an nWELL in a P-type substrate, with the readout electronics implemented alongside it. The nMOS transistors are situated on their respective pWELL, while the pMOS transistors are on their nWELL.

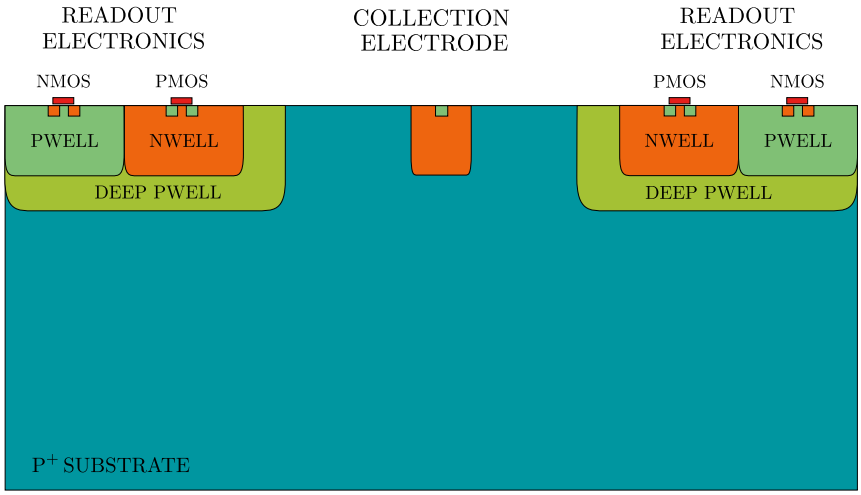

Figure 2.5: Cross section of a MAPS with a small collection electrode.

To enhance charge collection, the sensor is reverse-biased to promote drift-based collection rather than diffusion-based. This involves biasing the nWELLs to a positive potential and the pWELLs to a negative one. However, there is a concern that the exposed nWELL of the pMOS from the readout electronics could also absorb some charge, as it would be positively biased. To address this, the nWELL is implanted on a deep pWELL, effectively

shielding it from the depletion region. This implementation introduces some challenges. Achieving full depletion of the p-type substrate over the entire pixel area is difficult due to the small size of the collection electrode (necessary for low sensor capacitance) and the requirement for large areas for complex readout circuits [39].

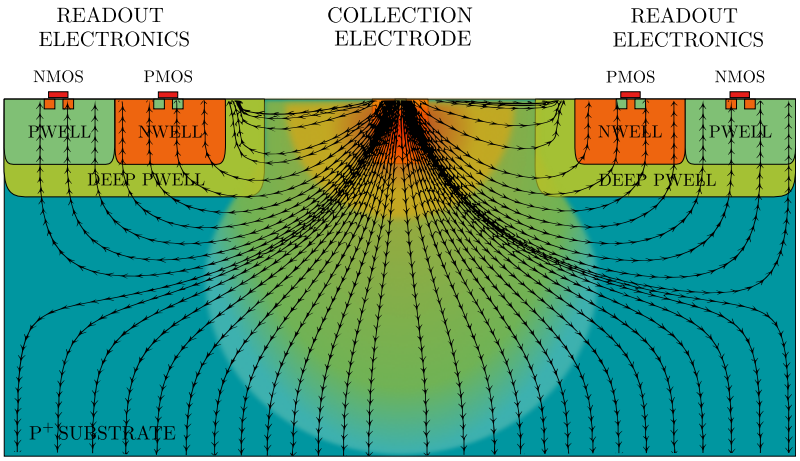

Figure 2.6: Simplistic representation of the effect of reverse biasing in a cross-section of a monolithic sensor. The nMOS are located at the pWELL (dark green). Black arrow lines represent the field lines of the depleted sensor, and the gradient is the magnitude of the electric field. The collection electrode would be biased at a positive voltage while both the P^+ substrate and the pWELL would be biased at the same negative voltage, creating the field lines depicted.

Another challenge is the effect of back biasing on the nMOS transistors' performance. Figure 2.6 shows a simplistic representation of the effect of reverse biasing in a cross-section of a monolithic sensor, where the P^+ substrate would be biased below 0 V, while the collection electrode is at a positive potential to fully deplete the sensor. The nMOS transistors are located at the pWELL (dark green). The bulk is connected to this pWELL and needs to be biased to the same potential as the P^+ substrate to create the field lines shown in the picture [40, 41]. The effect of this back-gate biasing has to be carefully addressed, as it can induce unwanted threshold voltage shifts due to the body effect [7].

Thanks to the absence of bump-bonding, MAPS offer a distinct advantage over hybrid sensors by allowing the realization of smaller pixels and a lower pixel capacitance, contributing to reduced power consumption and, consequently, a smaller material budget and lower noise. However, the inability to interchange the sensor sets a constraint on its potential use in HEP applications. Substantial efforts are being made to implement a large collection electrode design where the readout electronics are inside the collection electrode, offering detector capacitance values similar to those obtained with a hybrid sensor. However, the collection electrode is more closely coupled to the readout electronics.

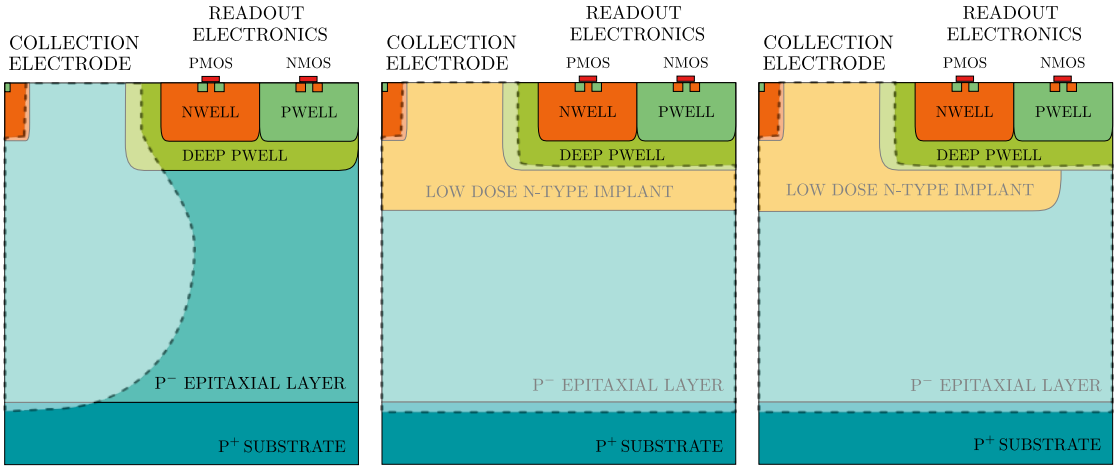

Figure 2.7: Cross section of the sensor in the TPSCo 65 nm imaging technology: a) standard process, b) modified process with low-dose n- implant, c) with gap in the low-dose n- implant.

The TPSCo 65 nm Process

The standard sensor of the TPSCo 65 nm imaging process is similar to its predecessor in 180 nm, with differences in doping levels and dimensions [42]. The epitaxial layer is 10 µm thick, which for a MIP particle means a total of 800 electron-hole pairs generated. Even though the transistor size has become smaller, achieving pixel pitches smaller than 15 µm is challenging. Therefore some modifications on the sensor have been introduced to fully deplete the epitaxial layer and optimize the electric field and therefore the drift velocity. Doing so a considerable enhancing of the speed of charge collection is achieved, despite the ratio between the pixel pitch and its thickness. Figure 2.7 shows: a) the standard sensor process b) a first modification with a low dose N-type implant, and c) the previous modification with a gap between the implant and the edge of the pixel. In the pixels implemented in this work, the collection electrode is an octagonal-shaped nWELL with a diameter of 1.14 µm and is distanced 1.93 µm from the surrounding pWELL containing the circuitry. The cut in the N-implant is 2.5 µm wide and centered along the pixel edges. This geometry represents a trade-off between a small sensor capacitance (below 5 fF) and a large lateral electric field, leading to collection times in the sub-nanosecond range [43].

2.3 State-of-the-Art: Recent Front-End Developments for MAPS on TPSCo 65 nm

After the TPSCo 180 nm, used in the ALPIDE chip [44], the TPSCo 65 nm process is the next candidate for developing new monolithic active CMOS pixel sensors at CERN. At the beginning of 2021, there were two main Front-End (FE) developments for two

different ASIC: the Monolithic Stitched Sensor (MOSS), intended to be a first step in the development of the ALICE ITS3 upgrade [45], and the H2M, developed with the idea of exporting the Timepix topology into monolithic technology.

This section provides a brief introduction to the FEs present in these two ASICs, with the intention of setting a starting point for the front-end designed and implemented in Chapter 5.

2.3.1 Monolithic Stitched Sensor (MOSS)

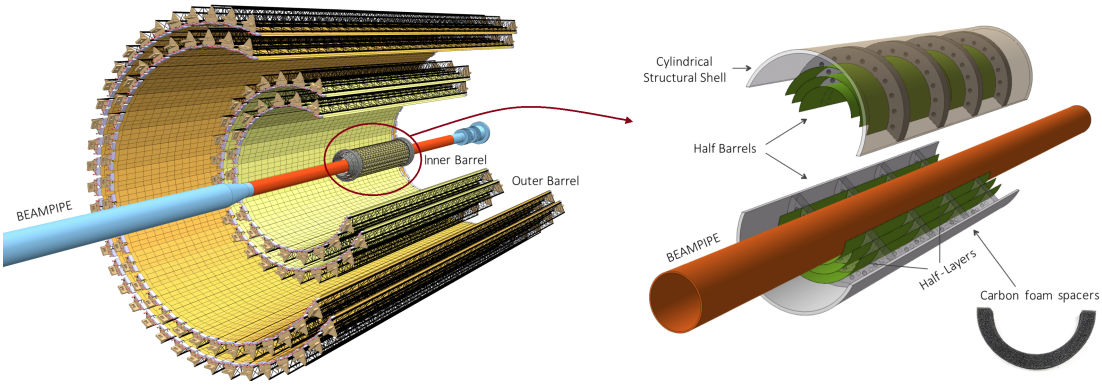

Figure 2.8: ITS2 (left) and its proposed upgrade ITS3 (right). The ITS3 upgrade aims to replace the inner tracker by a fully cylindrical one where the silicon detectors are flexible [46].

The Inner Tracking System (ITS) of the ALICE experiment, presented in Figure 2.8, plays a crucial role in reconstructing the trajectories of heavy-ion collisions. Currently, the ITS [47] utilizes pixel sensors with a granularity of 27 µm×29 µm, arranged in seven cylindrical layers placed within two concentric barrels. A significant upgrade has been proposed to enhance tracking detection.

The key drivers for the ITS upgrade are twofold [48]: enhancing the granularity of the sensors and minimizing the material budget within the detector volume. Achieving finer granularity, targeted at 15 µm×15 µm pixels, is expected to improve the precision of particle track reconstruction, particularly for short-lived particles with complex decay paths. Simultaneously, reducing the material budget is crucial for minimizing the deflection of charged particles as they traverse the detector, leading to more accurate measurements of their momenta and trajectories. Several innovative technologies are being implemented to achieve these goals, with the most notable being the adoption of stitched sensors.

The MOSS chip [19] aims to explore the feasibility of the stitching technique for particle detection, studying yield, supply distribution, signal propagation, and performance parameters. Its block diagram is presented in Figure 2.9. The chip, designed to prove

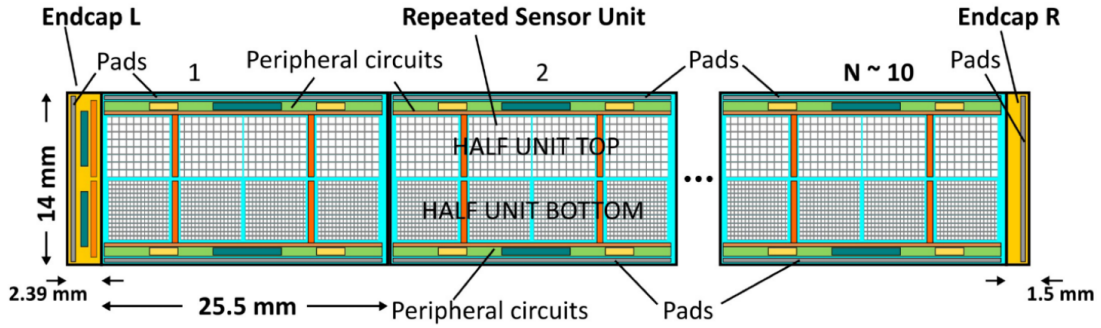

Figure 2.9: Concept diagram of the MOSS chip [49].

stitching, consists of ten repeated sensor units with different pixel array pitches. The chip's primary goals include understanding stitching's feasibility, wafer-size chip design, and studying various performance parameters.

The repeated sensor unit is subdivided into two half units with pixel arrays of different pitches. The top half unit contains four matrices of 256×256 pixels with a pitch of 22.5 µm. The bottom one contains four matrices of 320×320 pixels with a pitch of 18 µm. Each half unit operates independently, allowing isolation of defects in a portion while keeping others functional, facilitating defect analysis based on circuit density.

The stitching technique [49] involves subdividing a design reticle into sub-frames corresponding to photomask sub-frames. During manufacturing, photomasks are selectively exposed over wafers, connecting sub-units at stitching regions to create a large device. Precise translation and alignment are crucial, and conservative design rules must be followed in stitching regions for proper interconnection.

MOSS Front-End

The front-end of the MOSS chip is based on that of the Digital Pixel Test Structure (DPTS) chip [51], which, in turn, is derived from the Monolithic from ALice To Atlas 2 (MALTA2) chip [52] but adjusted for a smaller pixel pitch (approximately 15 µm). This circuit is depicted in Figure 2.10 together with the current consumption per branch. The front-end is a continuously active circuit that performs the reset of the collection electrode, the amplification of the generated charge, and the digitization of the amplified signal through a discrimination stage. The basic principle of this front-end relies on the transfer of charge from a capacitance to the output node. The amplification stage of the front-end in the MOSS chip is based on an input pMOS transistor (M1) connected in a source-follower configuration, with its gate connected to the sensor. This input transistor is loaded with an nMOS transistor (M2), whose gate is connected to the source of the input transistor. Upon a particle hit, the negative current step on the collection electrode is buffered by the input transistor and provided to the gate of the nMOS transistor. The latter behaves

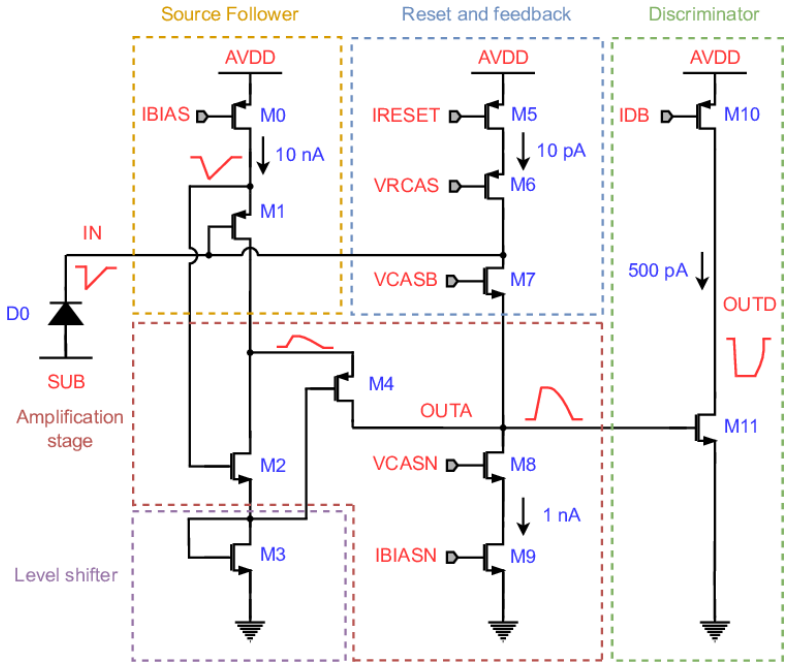

Figure 2.10: Schematic of the front-end in the DPTS chip [50].

as a common-source device, and a voltage signal is obtained across the drains of the two transistors. After pulse generation, feedback, reset, and discriminator networks are attached to obtain the final pulse for the digital logic [53].

Compared to the front-end in the DPTS, the `IBIAS` and `IBIASN` currents are set to larger nominal values, specifically 25 nA and 2.5 nA, respectively. At the same time, the gate of M4 is connected to the drain of M3, and the gate voltage of M3 can be easily tuned. The nominal settings are presented in Table 2.1. This configuration results in a gain of $\approx 1\,\mathrm{mV/e^-}$ (at $\approx 150\,\mathrm{e^-}$), a rise time of $\approx 1.5\,\mu\mathrm{s}$, threshold dispersion of $\approx 16\,\mathrm{e^-}$, and a noise level of $\approx 17\,\mathrm{e^-}$, all for a power consumption of 36 nW. It is important to mention the intrinsic non-linearity performance of this type of front-end, which translates to a nonlinear gain. Therefore, for a charge of a few electrons, the gain is $\approx 0.7\,\mathrm{mV/e^-}$, whereas it is $\approx 1\,\mathrm{mV/e^-}$ with an injected charge of $\approx 150\,\mathrm{e^-}$. For an injected charge of $500\,\mathrm{e^-}$, the front-end gain is $\approx 0.57\,\mathrm{mV/e^-}$. However, the ToT of the analog output signal has a linear dependence on the input charge. The described behavior is visible in Figure 2.11, which shows the performance of the DPTS front-end. Red lines correspond to input signals, blue to output signals of the amplification stage, and green to the discriminator output [50].

2.3.2 Hybrid-to-Monolithic (H2M)

During the past years, the Medipix Collaboration has developed two families of practically noise-free hybrid imaging pixel detectors. These two ASIC families are: (i) the Medipix

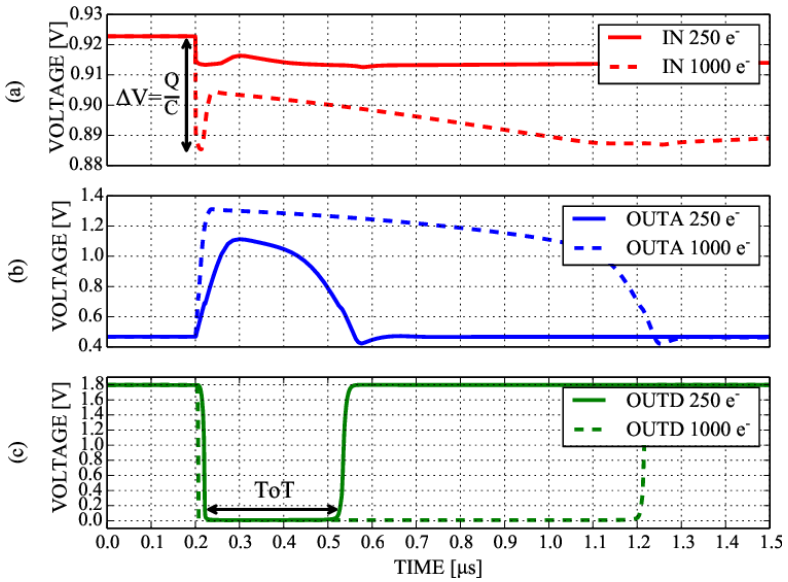

Figure 2.11: Performance of the DPTS front-end. Red lines correspond to input signals, blue to output signals of the amplification stage, and green to the discriminator output. The gain of the amplifier is intrinsically nonlinear and decreases with the input charge. However, the ToT is linear with the charge as it is proportional to the discharge time of the collection electrode [50].

ASICs, which integrate data from multiple pixel hits and provide frame-based images, and (ii) the Timepix ASICs, which aim to send off-chip as much information as possible about individual interactions for further processing.

The Timepix family has four ASICs (Timepix, Timepix2, Timepix3, and Timepix4), with Timepix3 being the most versatile. Developed as an alternative to Medipix2's 2D projections via threshold-based hit counting, Timepix incorporates a distributed clock per pixel based on Time to Digital Converter (TDC). This allows the determination of the arrival time of particles with respect to a clock or shutter reference, enabling not only ToT but also ToA measurements while retaining the original photon counting mode from the Medipix ASICs [54, 55].

The H2M ASIC is a monolithic pixel sensor chip designed using the TPSCo 65 nm CMOS imaging process, and its block diagram is presented in Figure 2.12. It features a 64×16 pixel array with a 35 µm pitch, resulting in a total active area of $2.24 \times 0.56\,\mathrm{mm}^2$. Each pixel comprises a collection electrode, analog front-end, and digital logic. The digital logic, based on an 8-bit counter, can operate in four modes: ToT, ToA, photon counting, and triggered mode. The analog front-end includes a collection n-well electrode, a CSA with Krummenacher feedback, and a continuous-time threshold discriminator.

This project investigates the challenges and opportunities of transitioning a known hybrid pixel detector architecture, like Timepix, to a monolithic design. Specifically, it aims

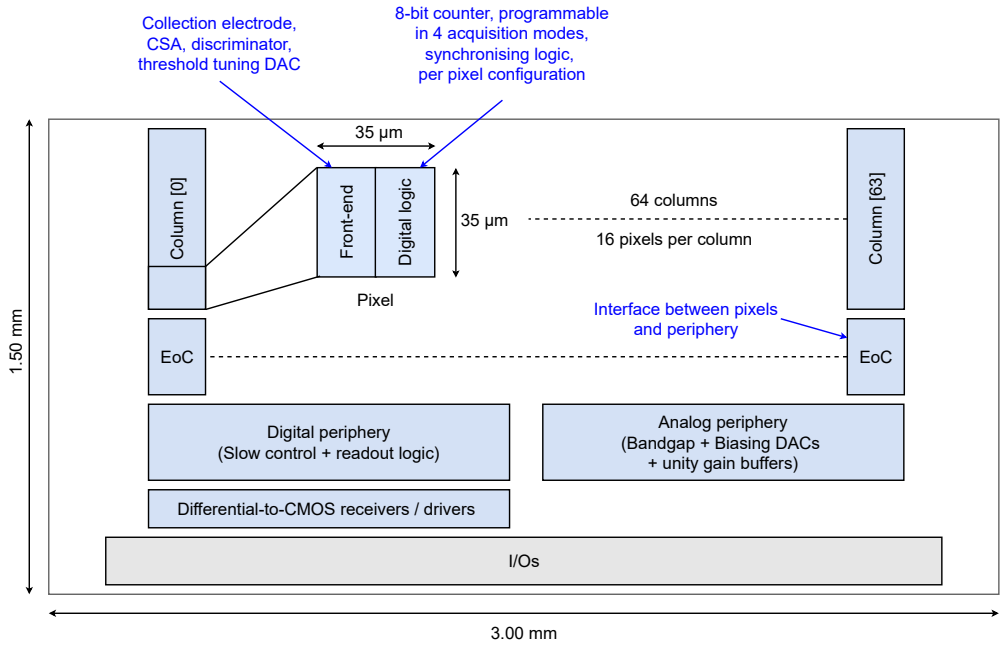

Figure 2.12: Block diagram of the H2M chip [56].

to explore the challenges of migrating a hybrid architecture to a monolithic chip by comparing the H2M's behavior with similar hybrid ASICs at the system level. By adopting a monolithic design, the H2M system benefits from lower mass and integration cost compared to traditional hybrid detector technologies. The bumping process needed by these hybrid nodes increases significantly the cost of production which can be a drawback for certain applications like the use of Timepix in education [57, 58].

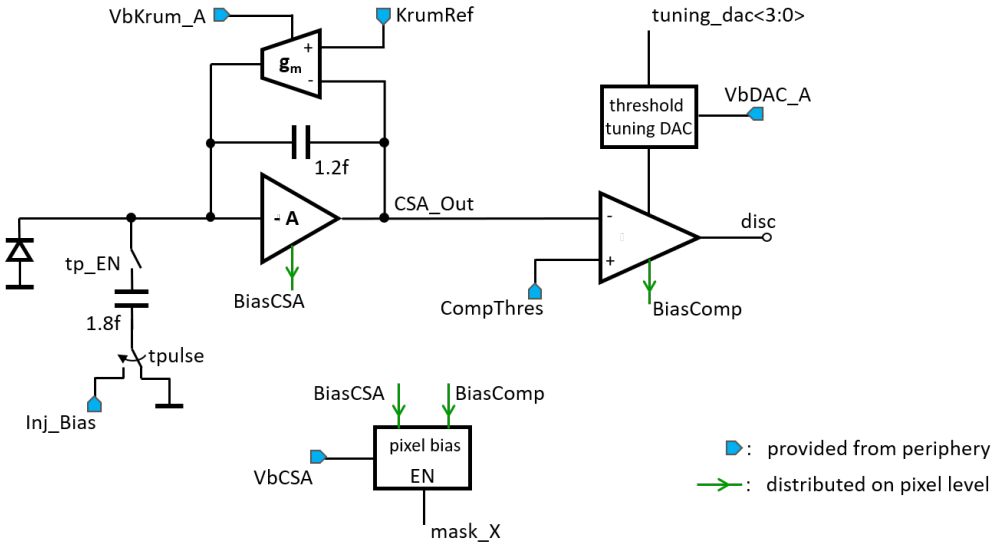

Figure 2.13: Front-end of the H2M [56].

The analog periphery of the chip delivers stable and temperature-independent biasing currents and voltages to the analog front-end. It is based on three main IP blocks: Digital-to-Analog Converter (DAC), Rail-to-Rail (R2R) amplifier, and a bandgap. The H2M analog periphery consists of 6 biasing 8-bit DACs used to bias the front-end to the desired operating point. Each DAC has a rail-to-rail unity gain buffer connected to its output, capable of driving the load of the multiple front-ends biased by the DAC. The analog periphery, designed by the author, is presented in Appendix A. On the other hand, the H2M digital periphery includes a state machine for generating test pulses.

At the bottom of the chip, 34 Input/Output (I/O) pins are allocated. Thirty I/O pins include analog and digital I/Os, power supplies, and ground connections. The two I/O pins on the right and the two I/Os on the left connect to the two reverse bias voltages substrate (`SUB`) and `PWELL`. The H2M digital I/Os are differential lines that use the Scalable Low Voltage Signaling (SLVS) interface. The chip I/Os can be connected through wire bonding.

H2M Front-End

The analog front-end, depicted in Figure 2.13, is composed of a collection electrode, a charge-sensitive amplifier, and a comparator along with a 4-bit DAC for threshold equalization. Additionally, a test signal can be generated through an injection capacitance connected to the CSA's input. The CSA incorporates a feedback network, providing compensation for leakage current and a linear discharge of the feedback capacitance. Its bias current is globally set by an 8-bit current DAC in the periphery, determining the discharge rate of the feedback capacitance.

Post-layout simulations reveal a preamplifier gain of approximately $0.12\,\mathrm{mV/e^-}$ for nominal settings, detailed in Table 2.1. The CSA saturates at around $5\,\mathrm{ke^-}$ input charge. After a transient noise analysis while scanning the threshold voltage, the CSA noise is $\approx 3.2\,\mathrm{mV\,rms}$ or $27\,\mathrm{e^-\,rms}$. ToA is below 15 ns for input charges larger than $400\,\mathrm{e^-}$, and the timewalk is below 10 ns for pulses larger than $400\,\mathrm{e^-}$. Due to the increasing slope of at the CSA output with increasing signal charge, jitter is reduced with higher input charge reaching approximately 250 ps at $800\,\mathrm{e^-}$. The ToT becomes linear for charge pulses larger than $\sim 1\,\mathrm{ke^-}$, with a slope of $\sim 155\,\mathrm{ns/ke^-}$.

Table 2.1: Nominal settings of the H2M and MOSS front-ends.

H2M FE			MOSS FE		
Signal	Value	Unit	Signal	Value	Unit
`BiasCSA`	1.3 - 2.6	µA	`IBIAS`	25	nA
`BiasComp`	1.1 - 0	µA	`IBIASN`	2.5	nA
`KrumRef`	325	mV	`IRESET`	5	pA
`CompThres`	325	mV	`IDB`	25	nA
`VbCSA`	675	mV	`VCASN`	200	mV
`VbKrum_A`	990	mV	`VCASB`	80	mV
`VbDAC_A`	886	mV	`VSHIFT`	600	mV
`Inj_Bias`	0 - 350	mV			

2.4 Aspects to Consider on the Design of a CSA

In Chapter 5 presents the design of a low-power, low-noise front-end circuit based on a CSA. The performance of such FEs, particularly timing and noise, is heavily dependent not only on the sensor capacitance but also on the remaining circuit parameters. These architectures require continuous reset of the feedback capacitor and compensation for the sensor's leakage current. Additionally, depending on the application and sensor type, the CSA may need to handle both positive and negative input charges, enabling the readout chip to function with various sensors (electron or hole collection). The desired performance is constrained by the feedback capacitance, the gate capacitance of the input transistor, and the feedback network. Therefore, the design involves a trade-off between different elements, focusing on optimizing either speed, noise, power consumption, or compactness. The next section presents a mathematical model of the CSA to provide an overview of how these parameters influence stability and timing, as well as to identify the main noise sources within the circuit. Several conclusions will be extracted regarding a design for low-noise and low-power such as the one presented on this thesis.

2.4.1 Transfer Function of CSA

The type of front-end with CSA mode is based on a transconductance amplifier, which integrates the input current coming from the collection electrode and translates it into a voltage. As the readout electronics demand an output pulse for ToT or ToA calculations, a feedback capacitance (C_{FB}), which performs the integration, together with a feedback resistor (R_{FB}), to discharge the feedback capacitance, are included; as shown in the schematic in Figure 2.14. This transconductance amplifier can be modeled as a voltage-dependent current source ($G_m V_{\mathrm{in}}$) and an output resistance between drain and source (r_{ds}) in parallel. Using the Laplace transform to solve this small signal model circuit, and for the moment, not taking into account the feedback network, we can obtain the following transfer function:

$$\frac{V_{\text{out}}(s)}{I_{\text{in}}(s)} = \frac{-1 + \frac{C_{\text{FB}}}{G_m}s}{sC_{\text{FB}}\left(1 + \frac{C_{\text{T}}^2}{C_{\text{FB}}G_m}s\right)} \tag{2.7}$$

Where $C_{\text{T}}^2 = C_{\text{FB}}C_{\text{in}} + C_{\text{FB}}C_{\text{L}} + C_{\text{in}}C_{\text{L}}$, C_{L} is the load capacitance, C_{in} is the input capacitance, and C_{FB} is the feedback capacitance. C_{in} is a sum of the intrinsic gate capacitances of the input transistor (Section 4.1.2) and the detector capacitance C_{DET}. In Equation (2.7), G_m is the transconductance of the input transistor. Note that the poles are dominated by G_m, C_{FB} and C_{T}^2.

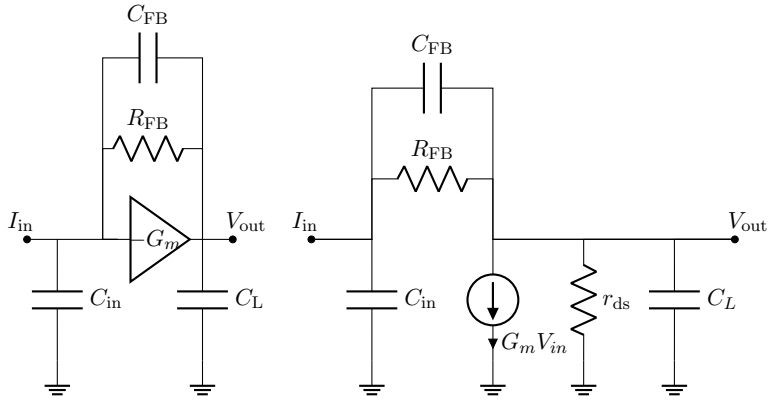

Figure 2.14: Schematic of the CSA (left) and its small signal model (right).

2.4.2 Output Pulse Amplitude vs. CSA Gain

The relation between the amplitude of the output pulse ΔV_{out} and the remaining parameters of the circuit will be an important matter in the design of the transconductance amplifier and the decision regarding the value of the feedback capacitance. This relation can be expressed as:

$$\Delta V_{\text{out}} = \frac{A_v\, Q_{\text{in}}}{C_{\text{DET}} + C_{\text{FB}}(1 + A_v)} \tag{2.8}$$

Where Q_{in} is the input charge, C_{DET} is the detector capacitance, and A_v is the gain of the amplifier. Assuming $A_v \gg 1$, then $\Delta V_{\text{out}} \approx \frac{Q_{\text{in}}}{C_{\text{FB}}}$, which makes the output pulse amplitude proportional to the input charge and inversely proportional to the feedback capacitance.

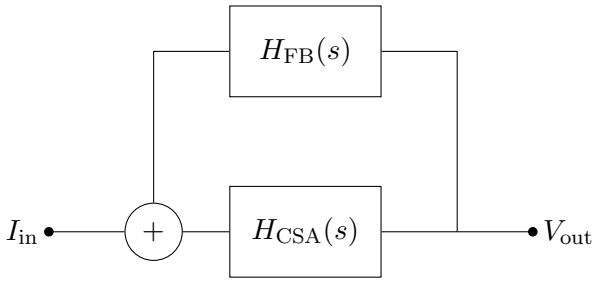

Figure 2.15: Feedback system with CSA and feedback network.

2.4.3 Transfer Function of CSA with Feedback Network

In the previous calculations, the feedback network is excluded; however, it has to be present to discharge the feedback capacitance. In this circuit, the feedback is not a resistor per se but a circuit with its own transfer function as depicted in Figure 2.15. However, the feedback has a fixed transconductance ($G_{\mathrm{FB}} = 1/R_{\mathrm{FB}}$). Therefore, including R_{FB} in the extraction of the transfer function from the circuit in Figure 2.14:

$$\frac{V_{\mathrm{out}}(s)}{I_{\mathrm{in}}(s)} = \frac{R_{\mathrm{FB}}}{\left(1 + \frac{C_{\mathrm{T}}^2}{C_{\mathrm{FB}} G_m} s\right)(1 + C_{\mathrm{FB}} R_{\mathrm{FB}}\, s)} \tag{2.9}$$

where the rise and falling time are:

$$\tau_r = \frac{C_{\mathrm{T}}^2}{C_{\mathrm{FB}} G_m} \quad \text{and} \quad \tau_{\mathrm{f}} = C_{\mathrm{FB}} R_{\mathrm{FB}} \tag{2.10}$$

From these equations, it is possible to derive that the rise time is proportional to the sum of the capacitances in the circuit and inversely proportional to the transconductance of the input transistor, while the falling time is defined the feedback capacitance and resistor.

2.4.4 Noise Sources on the Processing Chain

Figure 2.16 shows the main noise sources of the amplifier. The first one is the shot noise introduced by the sensor diode. It can be modelled by a current source in parallel with the input current and it has a single-sided Power Spectral Density (PSD) of:

$$\frac{I_n^2}{\Delta f} = 2qI_{\mathrm{leak}} \tag{2.11}$$

Where I_{leak} is the leakage current at the detector, Δf denotes the bandwidth over which the noise PSD is measured, and q is the value of the elementary charge. The other two sources of noise come from the the feedback transistor and the input transistor, and their transconductances (G_{FB}, G_m). They can be modelled as a parallel current source to the feedback resistance and a voltage source in series with the input transistor. Both of them introduce flicker and thermal noise, however we will just focus on the latter as the flicker noise becomes insignificant due to the large bandwidth of the amplifier. The PSD of the thermal noise is defined as:

$$\frac{v_n^2}{\Delta f} = 4kT\Gamma R \tag{2.12}$$

Here, v_n represents the root mean square voltage of thermal noise, k is the Boltzmann constant ($k \approx 1.38 \times 10^{-23}$ J/K), T is the absolute temperature, Γ noise related parameter, and R stands for the resistance. To study the influence of the different parameters of the circuit on the noise we calculated their contribution to the Equivalent Noise Charge (ENC). For the calculation we part from the small signal model taking into account each noise source separately. From there, we extract the transfer function from the output voltage $V_{\text{out}}(s)$ to each noise source $e_n(s)$.

With these transfer functions we can extract each output noise power V^2_{rmsOUT}. To do so we calculate the integral of the power spectral density multiplied by the transfer function. The PSD is a measure of the noise power per unit bandwidth at a given frequency. The square root of the power spectral density is equal to the ENC.

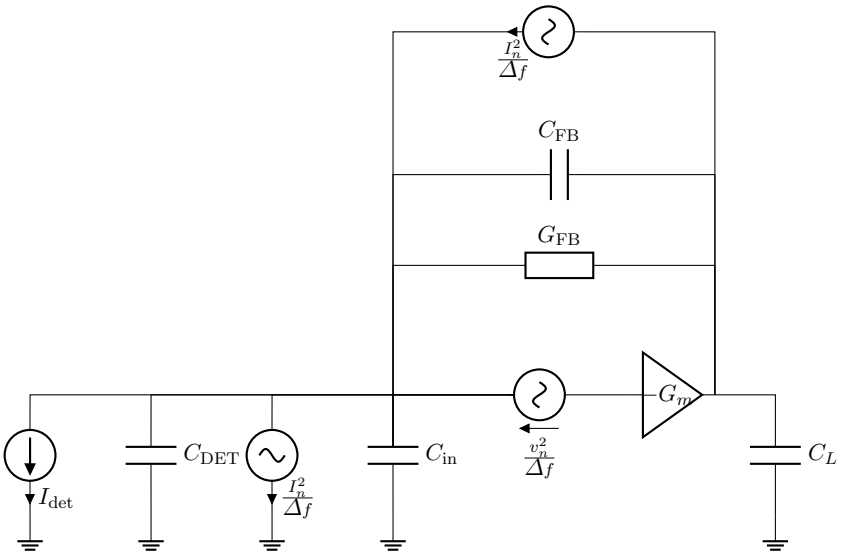

Figure 2.16: Small signal model with the two thermal noise sources and the shot noise source.

Series Thermal Noise

The small signal model with the thermal noise source from the input transistor is represented in Figure 2.17. Solving the circuit, the transfer function between the output voltage $V_{\text{out}}(s)$ and the noise $e_n(s)$ is:

$$\frac{V_{\text{out}}(s)}{e_n(s)} = \frac{(C_{\text{DET}} + C_{\text{FB}} + C_{\text{in}})\, G_m}{s\,(C_L + C_{\text{FB}})} \tag{2.13}$$

To extract the r.m.s voltage at the output we have to integrate the noise spectrum over the bandwidth:

$$V^2_{\text{rmsOUT}} = \int_0^\infty \left| \frac{V_{\text{out}}(\omega)}{e_n(\omega)} \right|^2 \frac{4kT\Gamma}{G_m}\, dW = \frac{(C_{\text{DET}} + C_{\text{FB}} + C_{\text{in}})4kT\Gamma}{C_L + C_{\text{FB}}} \tag{2.14}$$

The contribution of the series thermal noise to the total ENC in e^-r.m.s is:

$$\text{ENC}_{\text{Series Thermal Noise}} = \sqrt{\frac{C_{\text{FB}}(C_{\text{DET}} + C_{\text{in}} + C_{\text{FB}})^2 4kT\Gamma}{(C_{\text{DET}}C_{\text{FB}} + C_{\text{FB}}C_{\text{in}} + C_{\text{DET}}C_L + C_{\text{FB}}C_L + C_{\text{in}}C_L)q^2}} \tag{2.15}$$

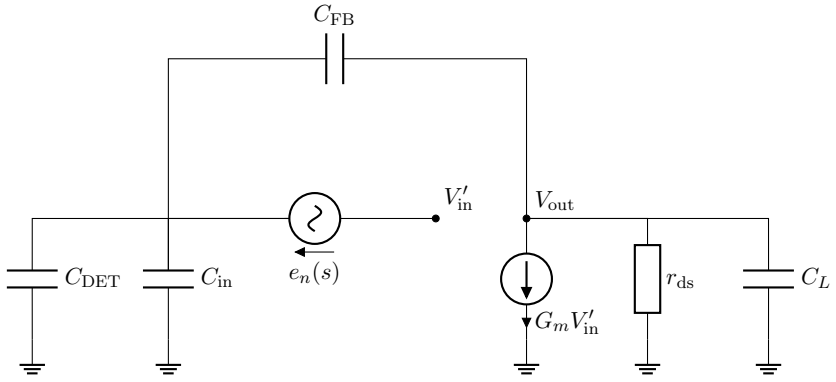

Figure 2.17: Small signal model with the thermal noise source from the input transistor.

Parallel Shot Noise

The small signal model with the shot noise source from the input diode is represented in Figure 2.18. Solving the circuit, the transfer function between the output voltage $V_{\text{out}}(s)$ and the noise $e_n(s)$ is:

$$\frac{V_{\text{out}}(s)}{e_n(s)} = \frac{1}{1 + \frac{C_{\text{FB}}}{G_{\text{FB}}} s} \tag{2.16}$$

To extract the r.m.s voltage at the output we have to integrate the noise spectrum in the bandwidth. Again, for the integral to converge we need to take into account the feedback transconductance in the calculation of the transfer function:

$$V^2_{\text{rmsOUT}} = \int_0^\infty \left| \frac{V_{\text{out}}(\omega)}{e_n(\omega)} \right|^2 2qI_{\text{leak}}\, dW = \frac{2\,q\,I_{\text{leak}}}{C_{\text{FB}}\,G_{\text{FB}}} \tag{2.17}$$

The contribution of the shot noise to the total ENC in e^-r.m.s is:

$$\text{ENC}_{\text{Parallel Shot Noise}} = \sqrt{\frac{2\,I_{\text{leak}}\,C_{\text{FB}}}{q\,G_{\text{FB}}}} \tag{2.18}$$

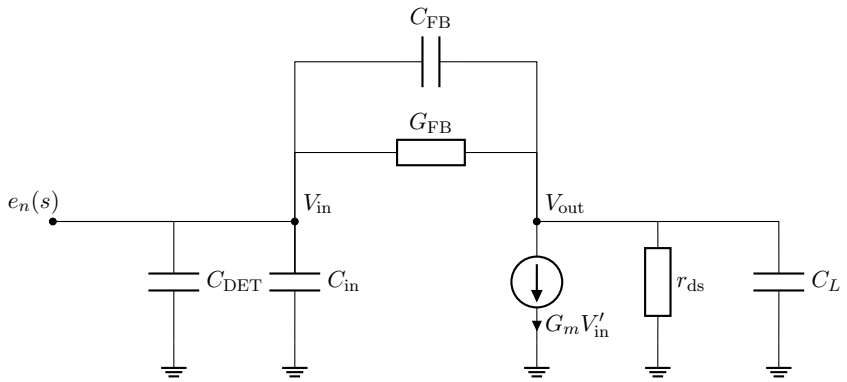

Figure 2.18: Small signal model with the shot noise source from the input diode.

Parallel Thermal Noise

The small signal model with the thermal noise source from the feedback transistor is represented in Figure 2.19. Solving the circuit, the transfer function between the output voltage $V_{\text{out}}(s)$ and the noise $e_n(s)$ is:

$$\frac{V_{\text{out}}(s)}{e_n(s)} = \frac{1}{1 + \frac{C_{\text{FB}}}{G_{\text{FB}}} s} \tag{2.19}$$

To extract the r.m.s voltage at the output we have to integrate the noise spectrum in the bandwidth. In order that the integral can converge we need to take into account the feedback transconductance in the calculation of the transfer function:

$$V^2_{\text{rmsOUT}} = \int_0^\infty \left| \frac{V_{\text{out}}(\omega)}{e_n(\omega)} \right|^2 \frac{4\text{ k T}\Gamma}{G_{\text{FB}}}\, dW = \frac{4\text{ k T}\Gamma}{C_{\text{FB}}} \tag{2.20}$$

The contribution of the shot noise to the total ENC in e^-r.m.s is:

$$\text{ENC}_{\text{Parallel Thermal Noise}} = \sqrt{\frac{4kT\Gamma C_{\text{FB}}}{q^2}} \tag{2.21}$$

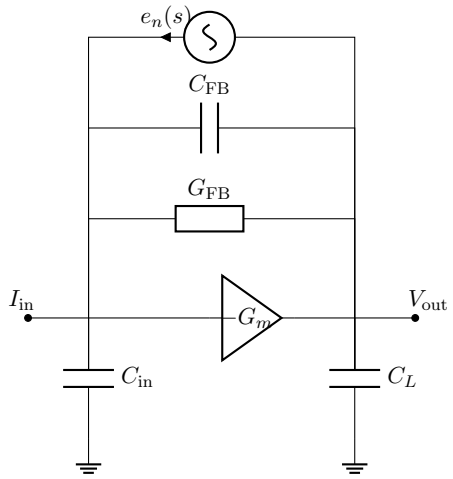

Figure 2.19: Small signal model with the thermal noise contribution from the feedback transistor.

2.5 Summary

Both hybrid and monolithic pixel sensors are widely used in the high-energy physics community, with applications ranging from particle accelerators to education. At the beginning of 2021, there were two main prototype chips developed using the TPSCo 65 nm technology: MOSS and H2M. Each chip provides a front-end with two complementary topologies, leading to two different performances in noise, power consumption, and speed.

For the design of these types of FEs is important to take into account not only the elements present on the FE itself but also the optimization of the PN junction forming the collection electrode, the charge generation, the signal formation, and the rest of the processing chain. As the thesis will conclude with the design and implementation of a front-end

based on a CSA, the author provided a study of how the different elements present in this topology affect stability, noise, and speed performance. The main conclusions drawn from this study regarding low-power design are:

- Fixing the power consumption and therefore the transconductance of the input transistor, then the values of C_{FB} and C_{T}^2 play an important role in the stability of the circuit.
- The CSA gain must be high enough ($\sim 40\,\mathrm{dB}$) that the amplitude of the output pulse depends only on Q_{in} and C_{FB}.
- Lowering the power consumption and therefore G_m and keeping a low value of C_{FB} will boost the influence of the parasitic capacitances and intrinsic gate capacitances on the rise time.

And the main conclusions, important for low-noise, are:

- The series thermal noise will be influenced by the capacitances present in the FE. Assuming a low value of C_{FB} to boost gain, the instrinsic gain gate capacitances and the parasitics from the layout will influence this noise source.
- The parallel shot noise is proportional to C_{FB} but inversely proportional to G_{FB}.
- The parallel thermal noise will be proportional just to C_{FB}.

3 Characterization of TID Effects: Experimental Details and Results

The next upgrade planned for the CERN complex is the HL-LHC, which will introduce higher luminosity and collision energies. The TPSCo 65 nm process stands as the primary candidate for developing new monolithic active CMOS pixel sensors at CERN. The anticipated higher luminosity is expected to result in a maximum TID of up to 1 Grad (SiO_2). Moving to more advanced nodes with smaller feature sizes should enable reduced power consumption and the integration of more intelligence within the same pixel area. Additionally, the thinner gate oxide associated with transistor size reduction enhances tolerance to TID [59, 60].

For the development of these new pixel sensors and their sub-blocks, designers require a better understanding of the technology and its performance using real samples. This will help to avoid unexpected behavior in their analog and digital designs. For this purpose, several Transistor Test Structure (TTS) including both pMOS and nMOS have been designed and tested.

Ionizing radiation can induce unwanted leakage current on nMOS devices, as well as variations in threshold voltage and drain current. Shifts in all these parameters can change the biasing point of analog circuits and and the performance of digital circuits. Some of these effects can be mitigated using appropriate layout techniques (e.g., [61]). The TTSs and the measurement set-up are presented in Section 3.2. The results of TID tests up to 1 Grad (SiO_2) on the core 1.2 V devices are presented in Section 3.3, and the in-depth analysis of transistor size-related effects is presented in Section 3.4, Section 3.5, and Section 3.6. The comparison of TID effects on transistors from two different splits will be presented in Section 3.7. Finally, a brief overview of 3.3 V devices and its tolerance to TID is presented in Section 3.8.

3.1 Radiation-Induced Effects

This section presents the theory underlying the different types of radiation effects. Subsection 3.1.1 covers the effect related with the accumulated charge on the gate oxide. Three important figures of merit are introduced: percentage of variation of the drain current ($\%I_{\mathrm{ON}}$), threshold voltage (V_{TH}), and transconductance parameter (K_{μ}). Subsection 3.1.2 details the effects related with the presence of the spacers, which is a major concern of short channel devices. On the other hand, effects related with the charge accumulated at the shallow trench isolation, being these a major concern of narrow channel devices, are covered in Subsection 3.1.3. Radiation-induced leakage current is presented at Subsection 3.1.4 at last.

3.1.1 Gate Oxide Effects

As the technology nodes are decreasing in size, the gate oxide thickness is decreasing too. Studies like [62] showed how, at low temperatures, the radiation-induced voltage shifts separate from the t_{ox}^2 scaling law; proving the hardness of thinner oxides to radiation [63, 64]. This leads to the assumption that the origin of performance degradation in modern CMOS technologies is principally due to the presence of the spacers and Shallow Trench Isolation (STI), both represented in Figure 3.1, and not to charge trapped at the gate oxide. However, the effect of the gate oxide thickness on this technology will be reported in Section 3.4. To study radiation-induced effects, we will use the percentage of variation of the maximum drain current ($\%I_{\mathrm{ON}}$), which is calculated as follows:

$$\%I_{\mathrm{ON}}(\mathrm{TID}) = 100\frac{I_{\mathrm{ON}}(\mathrm{TID}) - I_{\mathrm{ON}}(\mathrm{TID} = 0\,\mathrm{rad})}{I_{\mathrm{ON}}(\mathrm{TID} = 0\,\mathrm{rad})}, \tag{3.1}$$

where $I_{\mathrm{ON}}(\mathrm{TID})$ is the value of the maximum drain current measured at one step of the irradiation process, and $I_{\mathrm{ON}}(\mathrm{TID} = 0\,\mathrm{rad})$ is the maximum drain current measured before irradiation. This maximum drain current can be measured when the transistor is biased at two different operating regions: linear ($I_{\mathrm{ON}}^{\mathrm{lin}}$) and saturation ($I_{\mathrm{ON}}^{\mathrm{sat}}$). On the following results, the transistors are always biased to be in saturation.

The performance of a transistor can be characterized not only by the variations of the maximum drain current but also by the variations regarding the threshold voltage and the transconductance parameter. The drain current delivered by the transistor in the linear region can be expressed as [65]:

$$I_{\mathrm{D}} = \mu_{\mathrm{n}} C_{\mathrm{OX}} \frac{W}{L} 2[(V_{\mathrm{GS}} - V_{\mathrm{TH}})V_{\mathrm{DS}} - V_{\mathrm{DS}}^2]. \tag{3.2}$$

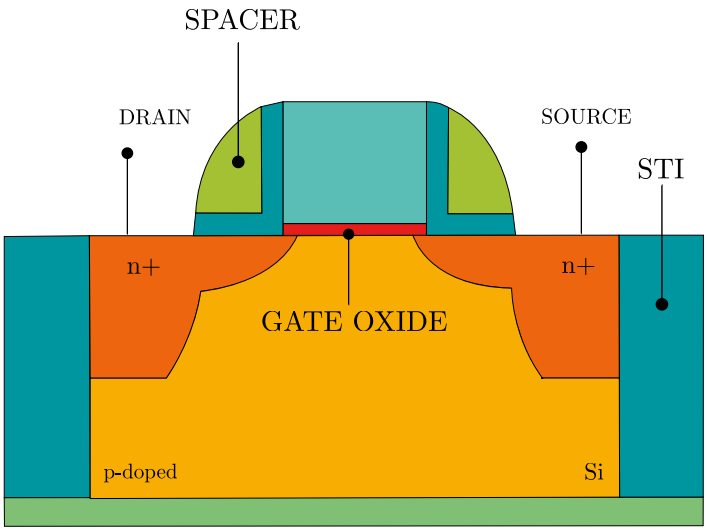

Figure 3.1: Representation of an nMOS transistor section with gate oxide, STI, and spacers, being the last two thicker and richer in defects making them more sensitive to TID effects.

Deriving the previous expression with respect to the drain-to-source voltage V_{DS}, it is possible to calculate the maximum drain current delivered by a transistor in saturation:

$$I_{\mathrm{D,\,max}} = \frac{1}{2}\mu_{\mathrm{n}} C_{\mathrm{OX}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 \tag{3.3}$$

In this equation, the transconductance parameter, in saturation, is equal to

$$K_{\mu} = \frac{\mu_{\mathrm{n}} C_{\mathrm{OX}}}{2} \frac{W}{L} \tag{3.4}$$

where μ_{n} is the mobility, and C_{OX} is the gate oxide capacitance per unit area, W the width, and L the length. As we will see later, ionizing radiation trapped on the sides of the channel can represent a variation in the series resistance i.e. variations in the nominal width or length of the transistor. Variations in the transconductance parameter can hence be traced as variations in the series resistance. Its value can be estimated from the measurements as the derivative of $\sqrt{I_{\mathrm{D}}^{\mathrm{sat}}}$ with respect to the gate-to-source voltage V_{GS}. In saturation, the threshold voltage is the zero of the tangent to the $I_{\mathrm{D}}(V_{\mathrm{GS}})$ curve, where the first derivative is maximum [66].

3.1.2 Spacer-Related Effects

Radiation-Induced Short Channel Effects (RISCEs) can be described as in [67, 68]: (i) an increase of resistivity on the sides of the transistor induced by the accumulation of positive charges in the spacers and (ii) temperature-induced transport of hydrogen ions

H^+ from the spacers to the gate oxide. The representation of both effects can be found in Figure 3.2. On pMOS transistors, these two processes are visible during irradiation and annealing, respectively. In the case of the nMOS, both processes are visible already during irradiation, making its study more difficult. On Subsection 3.5.1 we will focus on the pMOS as it is possible to separate the effect due to irradiation from temperature.

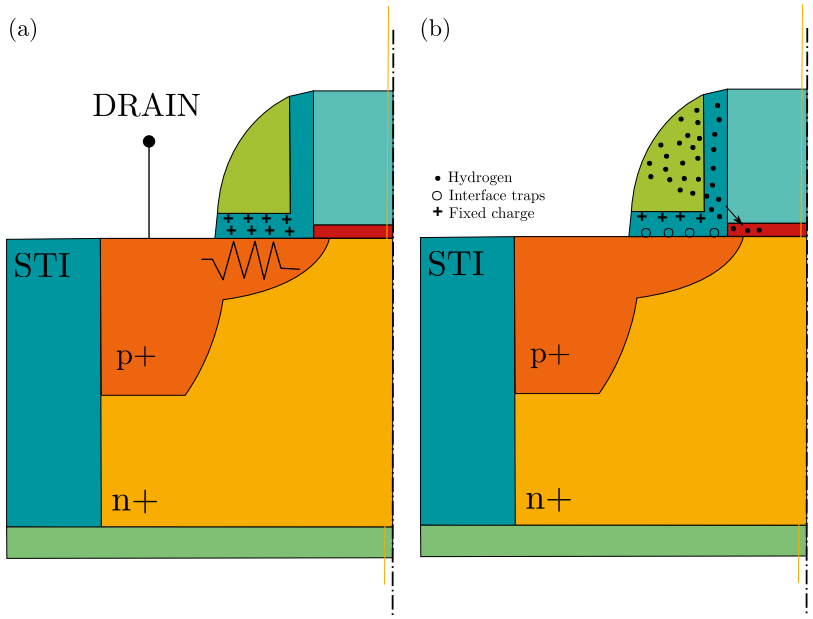

Figure 3.2: Profile of a pMOS transistor showing (a) increase of the series resistance at the sides of the transistor due to the accumulation of positive charges at the spacers and (b) the temperature-induced activated transport of H^+ into the gate oxide. Under proper electric field direction and temperature, H^+ ions can drift into the gate oxide. They depassivate the Si-H bonds at the interface, generating interface traps.

3.1.3 Shallow Trench Isolation Effects

Radiation-Induced Narrow Channel Effects (RINCEs) have been first mentioned in [69]. RINCEs are related to the charges accumulated in the STI, which generate an electric field, narrowing the effective channel. TID affects differently nMOS transistors and pMOS transistors. As depicted in Figure 3.3, in nMOS devices, at the beginning of irradiation, the positive charges accumulate in the STI lowering the threshold voltage and increasing the drain current. As we increase the TID level, the negative charges accumulate at the STI/Si interface traps and counterbalance for the field generated by the trapped holes [70]. These two compensating effects cause a non-monotonic behavior on nMOS devices while the behavior of pMOS is monotonic. This is due to the fact that both the charges at the STI and at the STI/Si interface traps have the same positive sign, increasing V_{TH}, and decreasing the maximum drain current.

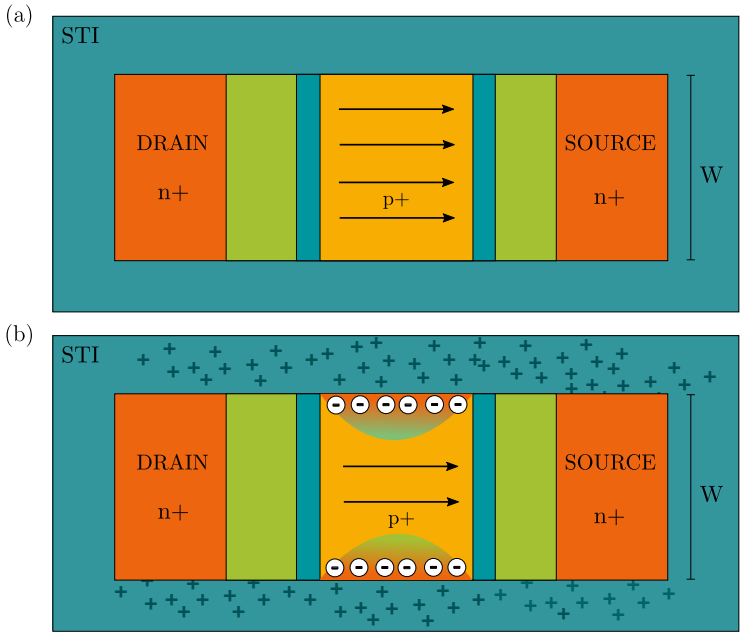

Figure 3.3: Top view of an nMOS transistor where: (a) before irradiation and with an inversion layer formed, the current flows from drain to source and (b) during irradiation the positive charge gets accumulated at the STI oxide whereas the negative charge gets accumulated at the interface traps between STI and Si. This narrows the nominal channel decreasing the drain current.

3.1.4 Leakage Current

nMOS devices suffer radiation-induced leakage current increase (I^{sat}_{OFF}) [10]. I^{sat}_{OFF} is the drain-to-source current measured when $V_{GS} = 0\,V$ and the transistor is biased to work in saturation ($V_{DS} = 1.2\,V$). During irradiation, when $V_{GS} = 0\,V$, positive charges accumulate on the borders of the STI, attracting electrons to the sides of the channel and, eventually, inverting the silicon at these points. As a consequence, the current will have new paths to flow increasing I^{sat}_{OFF} [71]. This I^{sat}_{OFF} can be several orders of magnitude higher than the I^{sat}_{OFF} measured before irradiation, increasing the power consumption of nMOS devices in off-state [72]. As the charges accumulated at the STI are positive they repeal the holes on the pMOS channel, not increasing I^{sat}_{OFF}.

3.2 Measurements Set-up and Transistor Test Structures

Several TTSs including both pMOS and nMOS have been designed and tested. These TTSs include core CMOS devices (rated at 1.2 V), as well as 3.3 V I/O devices. They contain two arrays of transistors, where either the width or the length varies, allowing to test the radiation response on different transistor dimensions. In this case the TTSs contain for both nMOS and pMOS:

- **For Gate Oxide (GO) effects studies:** wide and long transistors (6 µm x 5 µm).
- **For STI effects studies:** narrow and long transistors (0.2 µm x 6 µm).
- **For small channel effects studies:** narrow and short transistors (0.2 µm x 0.1 µm).
- **For RISCE studies:** array of transistors with width fixed at 1.0 µm and length ranging from 0.1 µm to 1.0 µm.
- **For RINCE studies:** array of transistors with length fixed at 0.1 µm and length ranging from 0.2 µm to 1.0 µm.

Later on, the first gradient of transistors will be used for RISCE studies and the second for RINCE studies.

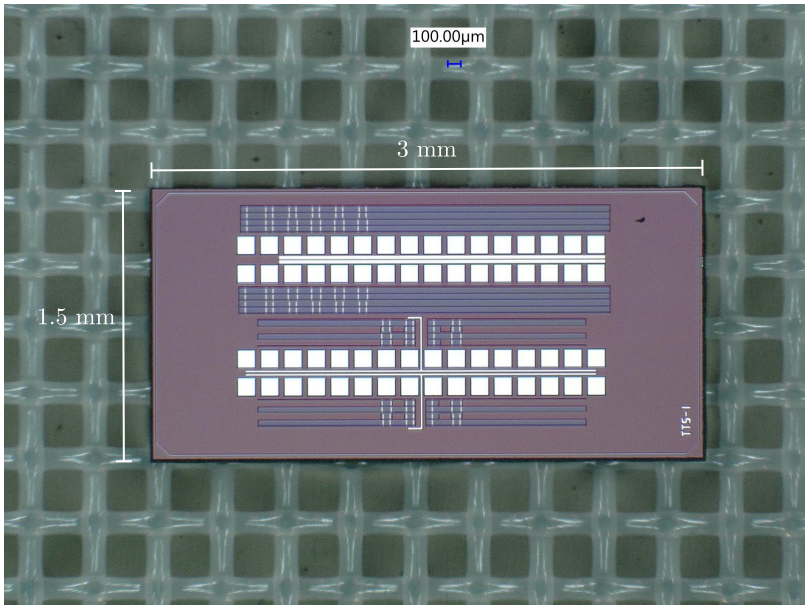

Figure 3.4: TTS1 chip containing both nMOS and pMOS (i) wide and long transistors (6 µm x 5 µm) (ii) narrow and long transistors (0.2 µm x 6 µm) (iii) narrow and short transistors (0.2 µm x 0.1 µm). It also includes several nMOS and pMOS transistors with width fixed at 1.0 µm and length ranging from 0.1 µm to 1.0 µm, and on the contrary, nMOS and pMOS transistors with length fixed at 0.1 µm and length ranging from 0.2 µm to 1.0 µm.

Two different setups were used: (i) for bulk bias, pre-irradiation, and annealing measurements, and (ii) for irradiation measurements. Both of them are composed by a semiconductor parameter analyzer, switching matrix, wafer probe station with a probe card and a thermal chuck[I]. This setup allows to measure bare chips, like the TTS shown in Figure 3.4, , where the terminals of the transistors are contacted via the needles of

[I]Thermal chucks are primarily used on probe systems (manual, semiautomatic or fully automatic) to heat or cool semiconductor wafers. In this case it allowed to reach the 100 °C during annealing.

the probe station. In Fig. 3.4 each of the white squares on the chip corresponds to one of the terminals of the transistors. In addition, the irradiation set-up includes an X-ray source capable of delivering a dose-rate up to 10 Mrad (SiO_2) per hour. Both set-ups are controlled with LabVIEW Graphic User Interface (GUI).

The measurements were taken first before irradiation and after several defined levels of irradiation. Two type of characteristics were measured: (i) $I_D(V_{GS})$ in both linear and saturation and (ii) $I_D(V_{DS})$ in weak, moderate and strong inversion. During annealing, the same measurements were taken in predefined steps of time at 100 °C temperature. All transistors were measured at $V_{GS} = V_{DS} = \pm 1.2$ V (negative sign for pMOS and positive for nMOS). From these measurements the values of I_{ON}, V_{TH}, and K_μ were extracted, following the procedure explained at Subsection 3.1.1. All the calculations and plots were processed using Python scripts.

Figure 3.5: Wafer probe station with a probe card and a thermal chuck used to perform the back-bias measurements.

A first irradiation up to 1 Grad was performed to test the reliability of this technology to irradiation. However, during the annealing at 100 °C of irradiated transistors there was a failure of the setup, which did not allow to finish the annealing. At this point, after probing its robustness, a new irradiation up to 300 Mrad with a successful 100 °C annealing during 85 h took place. The data allowed to trace the different effects of high TID levels on this node. The TTSs were printed in two different processes (splits) therefore coming from two different wafers; being Wafer 13 (WAF13) the standard

process (split 1) and Wafer 22 (WAF22) the modified one (split 4). Due to an Non-Disclosure Agreement (NDA) agreement, differences between these two processes can not be disclosed. The irradiation measurements were taken using an TTSs from WAF13. To ensure consistency between the standard and the modified process, several measurements before irradiation and at different TID levels up to 300 Mrad of TTSs from WAF22 were performed. Finally, the back bias dependence before irradiation was measured.

3.3 First Measurements at 1 Grad TID

We performed the first measurement up to 1 Grad (SiO_2) to obtain a preliminary overview of the behavior of the technology and its robustness to irradiation. Figure 3.6 shows the percentage variation of I_{ON}^{sat} for nMOS transistors with widths ranging from 0.2 µm to 5.0 µm and lengths from 0.1 µm to 6.0 µm. In general, the degradation of the maximum drain current of the nMOS devices is quite low, being the smallest size device the one reaching the highest variation ($\approx -15\,\%$).

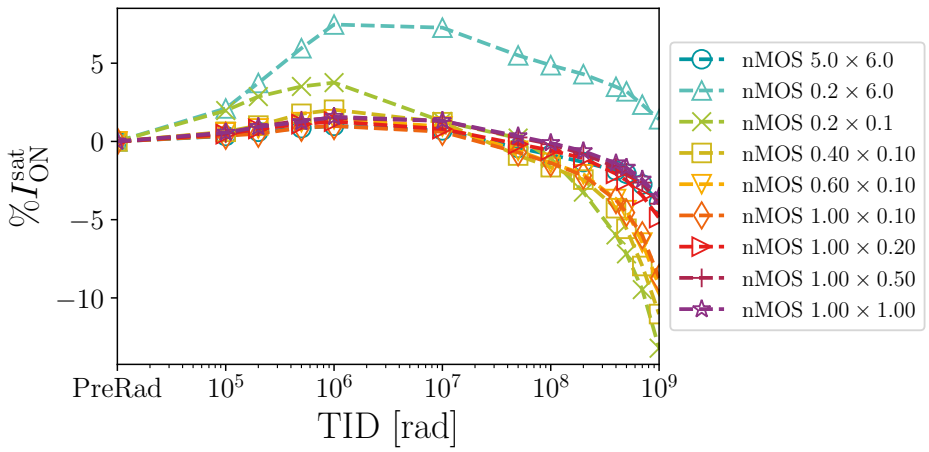

Figure 3.6: Percentage variation of I_{ON}^{sat} for nMOS transistors with widths ranging from 0.2 µm to 5.0 µm and lengths from 0.1 µm to 6.0 µm.

The percentage of variation of I_{ON}^{sat} for pMOS devices is shown in Figure 3.7. In this case, pMOS devices suffer a major deterioration of the maximum drain current than nMOS devices. Again the minimum size device is the one with a bigger variation ($\approx -80\,\%$).

The behavior seen on both nMOS and pMOS matches with the results shown in [73], from the same technology node but a different foundry. For both nMOS and pMOS, there is a correlation between the drain current drop and the size of the transistor (smaller sizes are less resilient to radiation). This points out the presence of both RISCE and RINCE. We would like to remark the presence of the non-monotonic behavior of nMOS devices already mentioned in Subsection 3.1.3 as well as the monotonic behavior of the pMOS devices.

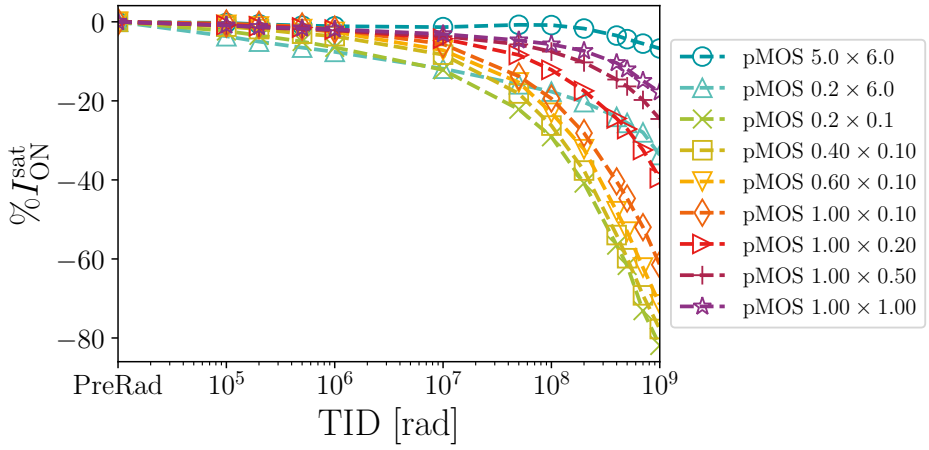

Figure 3.7: Percentage variation of I_{ON}^{sat} for pMOS transistors with widths ranging from 0.2 µm to 5.0 µm and lengths from 0.1 µm to 6.0 µm.

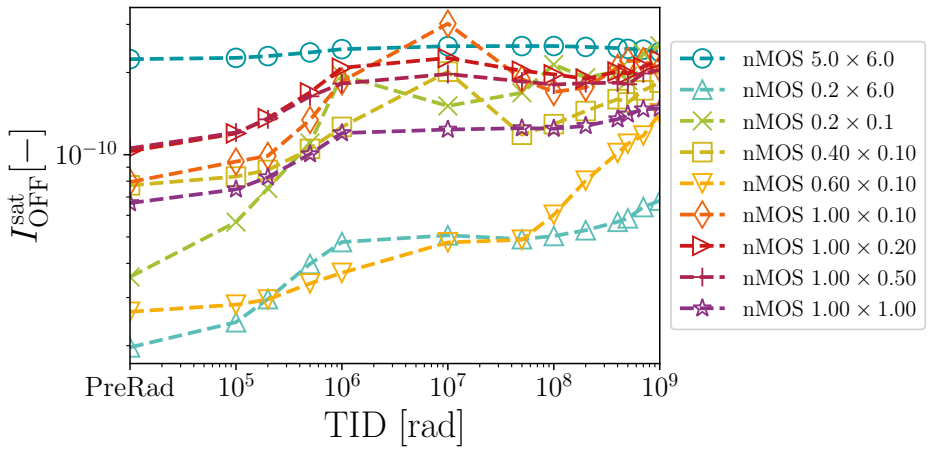

Figure 3.8: Variation of I_{OFF}^{sat} for nMOS transistors with widths ranging from 0.2 µm to 5.0 µm and lengths from 0.1 µm to 6.0 µm.

Figure 3.8 shows the evolution of I_{OFF}^{sat} during irradiation up to 1 Grad (SiO_2). I_{OFF}^{sat} increases less than an order of magnitude from its pre-radiation value. The minimum size device shows a lower pre-radiation leakage current and a higher increase of I_{OFF}^{sat} during the exposure. This leads to assuming that transistors with high nominal pre-radiation leakage current will see a lower increase in I_{OFF}^{sat} than transistors with a smaller initial leakage current.

From these results it is possible to conclude the reliability of this technology to irradiation. Still, it continues showing the consequences of three known radiation effects: RISCE, RINCE, and leakage current, with significantly higher importance the first two. Therefore, the next subsection will focus on the qualification of this technology showing the results obtained at 300 Mrad TID exposure of TTS1 WAF13 devices.

3.4 Gate Oxide-Related Effects

Gate oxide-related effects have been introduced in Subsection 3.1.1. These are related with the positive charge accumulated at the gate oxide. From previous studies [67], it is known that the effects related with the STI and the spacers are less visible in wide and long devices. Figure 3.9 shows the percentage of variation of I_{ON} of a wide and long nMOS and pMOS transistor. Both show a modest drop of the maximum delivered drain current ($\approx 2.5\,\%$ @ 300 Mrad) which proves again that the origin of performance degradation is principally due to the presence of the spacers and STI, and not to charge trapped at the gate oxide.

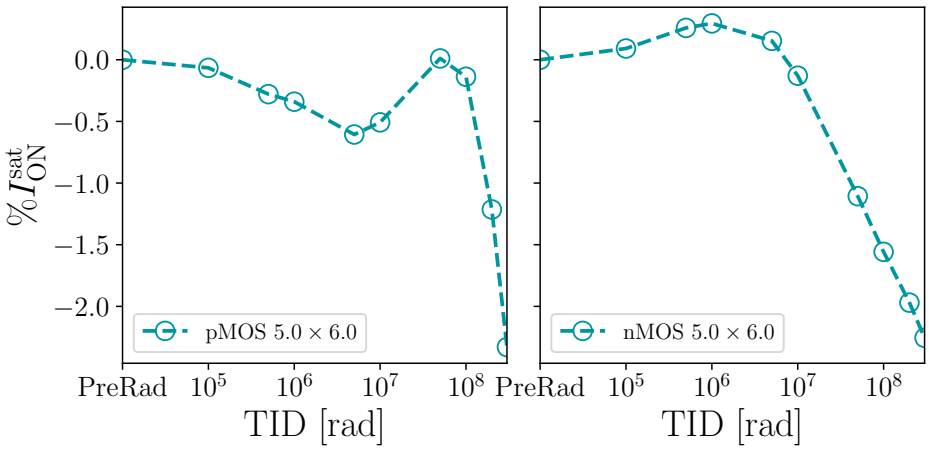

Figure 3.9: Percentage variation of I_{ON} of a wide and long pMOS (left) and nMOS (right) transistor. In this case the variations are dominated by the gate oxide effects. However, both nMOS and pMOS show a similar response with a low variation up to $\approx 2.5\,\%$.

3.5 Channel Length-Related Effects

3.5.1 Radiation-Induced Short Channel Effects (RISCE)

As described in Subsection 3.1.2, RISCE can be defined as (i) the accumulation of positive charges in the spacers during irradiation, and (ii) the temperature-induced transport of H^+ ions from the spacer into the gate oxide during annealing. These two processes will induce a degradation on I_{ON}^{sat} for both pMOS and nMOS but with different importance. Figure 3.10 shows the percentage of variation of I_{ON}^{sat} for both nMOS and pMOS transistors with a width of 1.0 µm and a length ranging from 0.1 µm to 1.0 µm. The shortest pMOS transistor reaches a shift of -35 % compared with the -5 % of its equivalent nMOS transistor, confirming the robustness of the nMOS transistors to RISCE.

The two previously described processes are visible, on pMOS, during irradiation and annealing respectively. But for the nMOS they occur both at the same during annealing

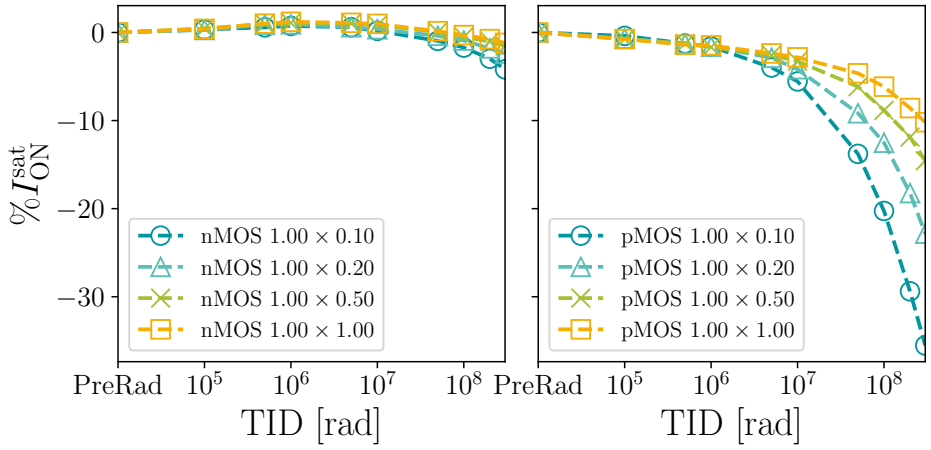

Figure 3.10: Percentage variation of I_{ON}^{sat} during irradiation of nMOS (left) and pMOS (right) for transistors with width 1.0 µm and length from 0.1 µm to 1.0 µm.

and irradiation, making more difficult its study. This is why we will focus just on the pMOS.

Figure 3.11 shows, for several short pMOS devices, the percentage of variation of the maximum drain current ($\%I_{ON}^{sat}$), threshold voltage shift ($\Delta|V_{TH}^{sat}|$) and the percentage of variation of the transconductance ($\%K_U^{sat}$). Variations of the latter are directly related to variations in the series resistance. The values are plotted during irradiation up to 300 Mrad (SiO_2) (left) and during 85 h annealing at 100 °C (right).

The increase in the series resistance due to the positive charges trapped in the spacers is visible during irradiation where at 300 Mrad (SiO_2) the I_{ON}^{sat} drops 36 % while K_U^{sat} decreases by $\approx 20\,\%$. On the other hand, the temperature-activated transport of H^+ in pMOS devices is visible during annealing where the V_{TH} increases ≈175 mV from its value before irradiation while K_U^{sat} remains stable, recovering its value after annealing at 25 °C. This temperature-dependent behavior matches with the results obtained from similar studies performed on other 65 nm technologies [74].

3.5.2 Leakage Current

Radiation-induced leakage current has been introduced in Subsection 3.1.4. This leakage current is negligible on the pMOS as the charges accumulated at the STI are positive, not attracting the holes on the pMOS channel, neither increasing I_{OFF}^{sat}. Therefore, they will not be covered in this subsection.

In Section 3.3 we confirmed that I_{OFF}^{sat} increases less than an order of magnitude from its pre-radiation value. In order to study the dependency with the size, Figure 3.12 shows the evolution of I_{OFF}^{sat} during irradiation up to 300 Mrad (SiO_2). The left plot contains

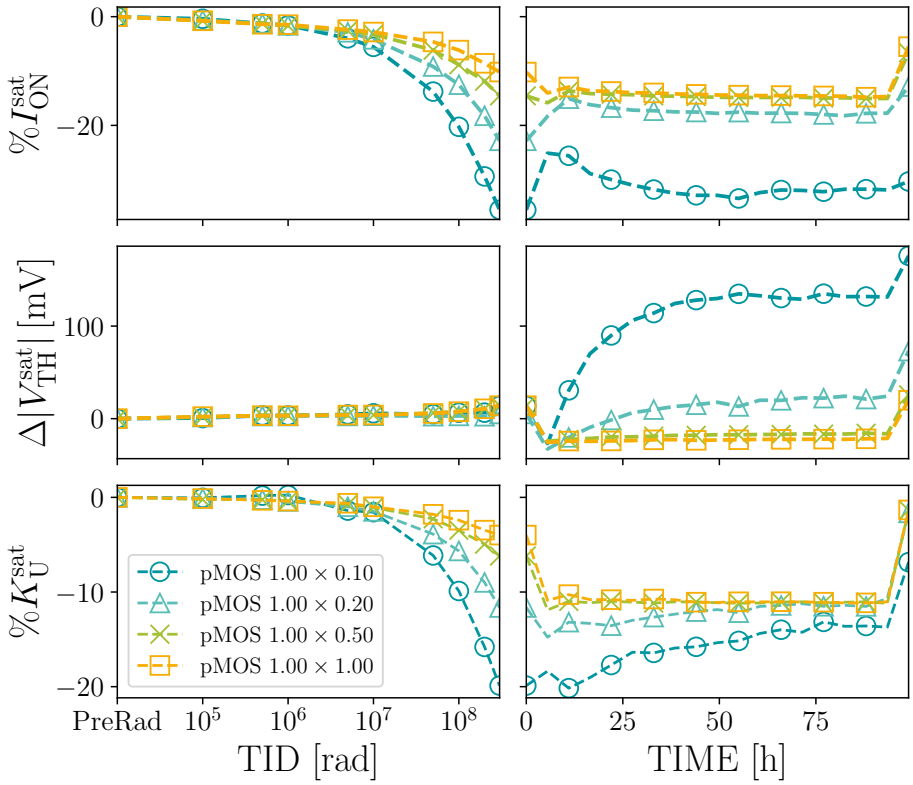

Figure 3.11: Percentage of variation of the maximum drain current ($\%I_{ON}^{sat}$) (up), threshold voltage shift ($\Delta|V_{TH}^{sat}|$) (middle) and the percentage of variation of the transconductance ($\%K_U^{sat}$) (bottom). The values are plotted during irradiation up to 300 Mrad (SiO_2) (left) and during 85 h annealing at 100 °C (right). The last point was measured at the end of the annealing at 25 °C. The width of the transistors is fixed to 1.00 µm and lengths range from 0.1 µm to 1.0 µm.

results for nMOS transistors with lengths of 0.10 µm and widths ranging from 0.20 µm to 1.0 µm, and the right plot, for nMOS transistors with widths fixed to 1.00 µm and lengths ranging from 0.10 µm to 1.0 µm. The black markers at the end of each plot correspond to the values of I_{OFF}^{sat} measured after 85 h of annealing at 100 °C. It is not possible to correlate the increase of I_{OFF}^{sat} with the length of the transistor, as it could be expected from previous studies [75]. Regarding the post-annealing values, there seems to be a good recovery of the leakage current values, almost returning to their pre-radiation values before TID exposure.

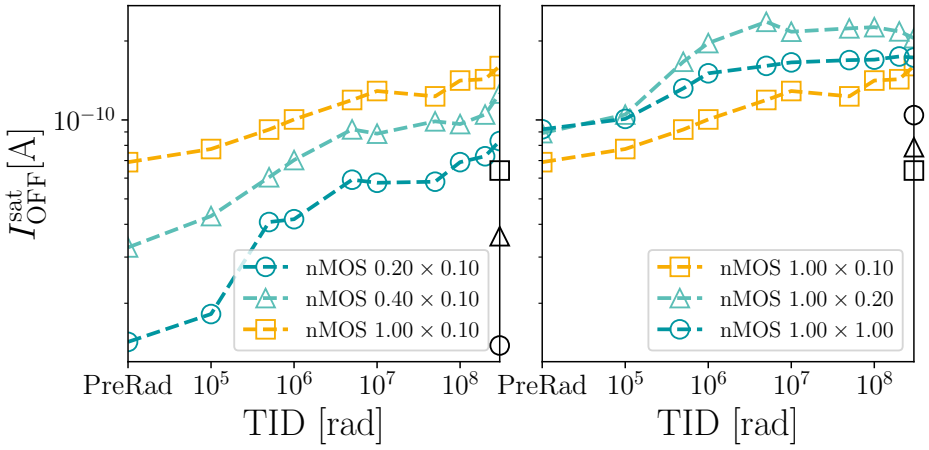

Figure 3.12: Evolution of I_{OFF}^{sat} during irradiation up to 300 Mrad (SiO_2). On the left, for nMOS transistors with lengths of 0.10 µm and widths ranging from 0.20 µm to 1.0 µm. On the right, for nMOS transistors with widths fixed to 1.00 µm and lengths ranging from 0.10 µm to 1.0 µm. The black markers at the end of each plot correspond to the values of I_{OFF}^{sat} measured after 85 h of annealing at 100 °C.

3.6 Channel Width-Dependent Effects

3.6.1 Radiation-Induced Narrow Channel Effects (RINCE)

RINCE was introduced in Subsection 3.1.3. This radiation-induced effect is related to the charge accumulated on the STI which generates an electric field, narrowing the effective channel.

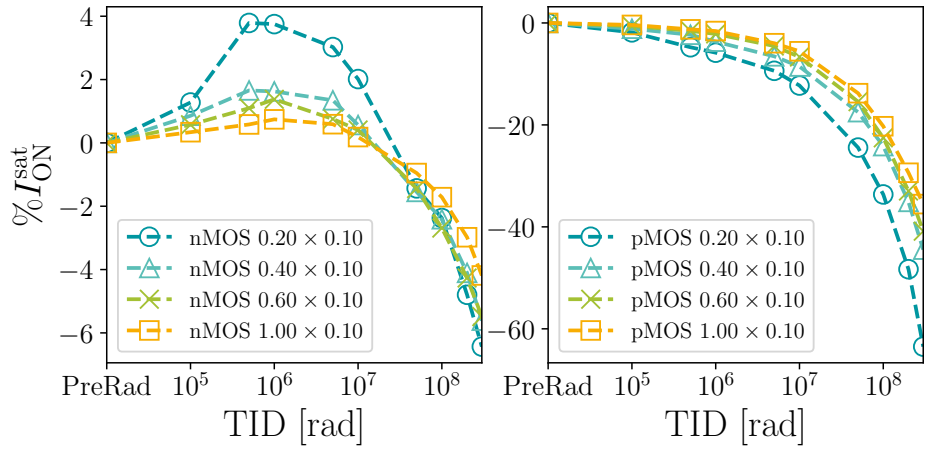

Figure 3.13: Variation of I_{ON}^{sat} during irradiation of nMOS for transistors (left) and pMOS transistors (right) with width from 0.2 µm to 1.0 µm and length 0.1 µm. The transistors were biased with $V_{DS} = V_{GS} = 1.2$ V.

Figure 3.13 shows the percentage of variation of I_{ON}^{sat} for nMOS transistors (on the left) and pMOS transistors (on the right) with a length of 0.10 µm and width ranging from 0.20 µm to 1.0 µm, during irradiation. In Subection 3.1.3 was already explained how RINCE affects different narrow nMOS transistors and narrow pMOS transistors. At the beginning of irradiation, the positive charges accumulate in the STI lowering the threshold voltage and increasing the drain current. As we increase the TID level, the negative charges accumulate at the STI/Si interface traps and counterbalance for the field generated by the trapped holes [70]. These two compensating effects cause a non-monotonic behavior on nMOS devices visible in Figure 3.13, specially on the narrowest transistor. However, this helps to keep the drain current degradation to ≈ 6 %.

Looking at the results from the pMOS in Figure 3.13, the behavior is monotonic, as the maximum drain current decreases with the TID dose. This is due to the fact that both the charges at the STI and at the interface between the STI and the silicon have the same positive sign, increasing V_{TH}, and causing the maximum drain current to decrease drastically up to ≈ 60 %.

3.7 Process Comparison

3.7.1 Pre-Radiation Measurements

All the previous studies where focused on transistors from WAF13 which is the standard process, however on the following designs, the modified process will be used. In order to achieve a general comparison between these standard (WAF13) and the modified (WAF22) process, three different sizes of transistors have been chosen: (i) wide and long transistors (6 µm x 5 µm) (ii) narrow and long transistors (0.2 µm x 6 µm) (iii) narrow and short transistors (0.2 µm x 0.1 µm).

Transistors from WAF13 and WAF22 show a similar behavior, delivering a maximum drain current on the same order of magnitude and a similar V_{TH}. However, there is a difference in leakage current among pMOS and nMOS devices. Whereas the leakage current on the pMOS devices between both splits shows a negligible variation, the leakage current on the nMOS shows a variation up to 3 orders of magnitude between split 1 and split 4, being bigger on the latter one. The results of the maximum drain current (I_{ON}) and the leakage current (I_{OFF}), measured when $V_{GS} = 0$ V, can be found in Table 3.1 for nMOS and Table 3.2 for pMOS, for both in linear and saturation region. It is visible that nMOS devices from WAF22 tend to show a bigger I_{OFF} in both linear and saturation, especially on the narrow devices, even though this is the optimized process.

Table 3.1: Maximum drain current I_{ON} and leakage current I_{OFF} measured in linear and saturation region for narrow and short, large and short and narrow and long nMOS devices from WAF13 and WAF22.

Transistor	Wafer	I_{ON}^{lin} [µA]	I_{OFF}^{lin} [pA]	I_{ON}^{sat} [µA]	I_{OFF}^{sat} [pA]
nMOS LVT 5.0 x 6.0	WAF13	4.64	0.11	112.65	37.89
	WAF22	4.56	0.01	108.57	9.09
nMOS LVT 0.2 x 6.0	WAF13	0.17	−0.26	4.34	2.16
	WAF22	0.17	−6.60	4.14	31.47
nMOS LVT 0.2 x 0.1	WAF13	5.99	−0.29	99.78	1.89
	WAF22	6.16	7.39	101.53	929.34

Table 3.2: Maximum drain current I_{ON} and leakage current I_{OFF} measured in linear and saturation region for narrow and short, large and short and narrow and long pMOS devices from WAF13 and WAF22.

Transistor	Wafer	I_{ON}^{lin} [µA]	I_{OFF}^{lin} [pA]	I_{ON}^{sat} [µA]	I_{OFF}^{sat} [pA]
pMOS LVT 5.0 x 6.0	WAF13	−1.18	−2.01	−26.00	−90.60
	WAF22	−1.21	−3.94	−26.32	−93.35
pMOS LVT 0.2 x 6.0	WAF13	−0.05	0.00	−1.21	−3.05
	WAF22	−0.05	0.70	−1.21	−3.80
pMOS LVT 0.2 x 0.1	WAF13	−2.07	−0.07	−46.39	−1.71
	WAF22	−2.01	−0.06	−43.90	−1.29

3.7.2 300 Mrad TID Measurements

In order to make sure that the performance under irradiation is similar to transistors from WAF13, we irradiated transistors from WAF22 up to 300 Mrad. Figure 3.14 shows the percentage variation of I_{ON}^{sat} for pMOS transistors with widths ranging from 0.2 µm to 5.0 µm and lengths from 0.1 µm to 6.0 µm. In gray color and dashed line, but with the same symbol as their equivalent from WAF22, the measurements of transistors from WAF13 are shown. As expected, the degradation of pMOS devices is quite significant, reaching ≈ 60 %. This behavior matches with the measurements from pMOS devices from the standard process.

Percentage variation of drain current I_{ON}^{sat} for nMOS is shown in Figure 3.15. The measurements of transistors from standard process are shown again in gray dashed lines for comparison. It is interesting to see how the positive variation of nMOS devices from WAF22 is higher than on devices from WAF13, still the dependence on the size is similar between the two processes. The non-monotonic behavior explained on Subsection 3.6.1 is visible, specially on narrow channel transistors. Again, it is possible to confirm the similar behavior of nMOS transistors from modified and standard process.

Looking at the variation of radiation-induced leakage current of nMOS transistors shown in Figure 3.16, they behave quite similar than transistors from standard process. The

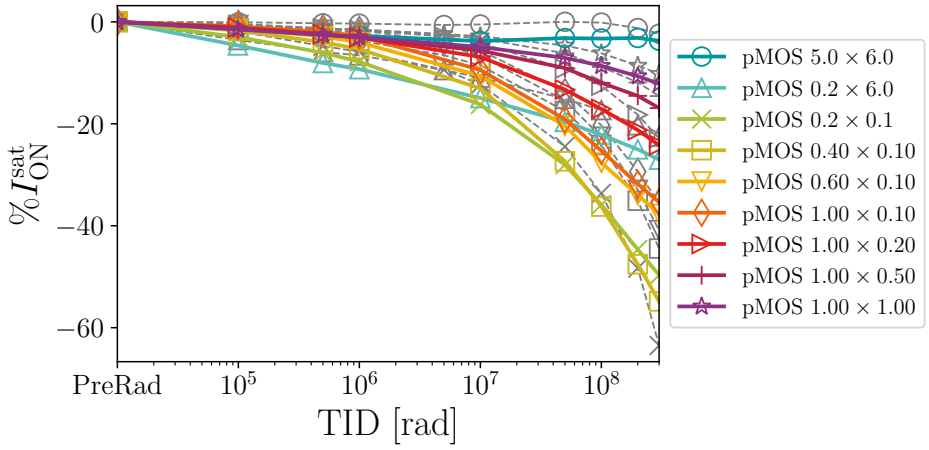

Figure 3.14: Percentage variation of I_{ON}^{sat} for pMOS transistors from WAF22 (modified process) with widths ranging from 0.2 µm to 5.0 µm and lengths from 0.1 µm to 6.0 µm. The transistors were diode biased with $V_{DS} = V_{GS} = -1.2\,V$.

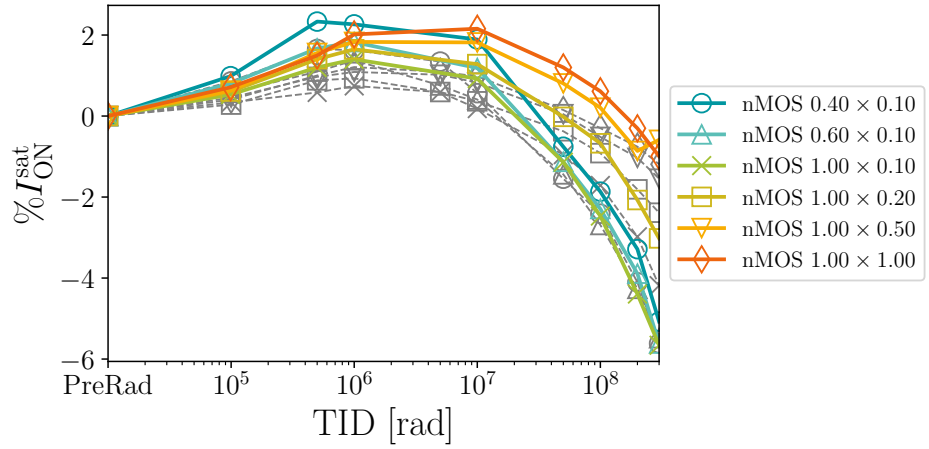

Figure 3.15: Percentage variation of I_{ON}^{sat} for nMOS transistors from WAF22 (modified process) with widths ranging from 0.2 µm to 1.0 µm and lengths from 0.1 µm to 1.0 µm. The transistors were diode biased with $V_{DS} = V_{GS} = 1.2\,V$.

initial leakage current before irradiation tends to be higher but its increase during irradiation tends to be similar or even smaller than the one seen in standard process transistors. Again small size devices show a bigger variation from non-irradiated to its value at the end of irradiation. But no clear dependency is observed neither with the width nor the length. In the case of the 1.0 µm x 0.5 µm transistor, there is a peak of the leakage current at the end of the irradiation due to a problem on the setup.

Comparing the measurements of transistors from WAF13 and WAF22 confirms that both processes show a equally robust behavior.

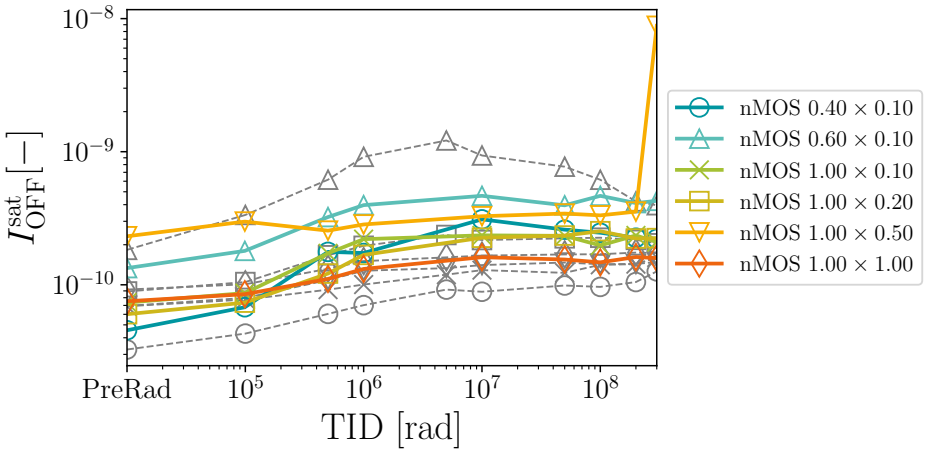

Figure 3.16: Variation of I_{OFF}^{sat} for nMOS transistors with widths ranging from 0.2 µm to 1.0 µm and lengths from 0.1 µm to 1.0 µm. The transistors were diode biased with $V_{DS} = V_{GS} = 1.2$ V.

3.8 Measurements at 200 Mrad TID of Thick Oxide Devices

The Process Design Kit (PDK) of this technology also includes 3.3 V devices. For the design of the front-end presented in Chapter 5, one of these thick oxide devices will be used because of the need of higher voltage headroom for our design. Therefore it is important to study their performance degradation with TID to ensure the robustness of the design. As seen in Section 3.1, transistors with thicker oxide are expected to experience a significant degradation due to the larger surface available for the charges to accumulate at the gate oxide. Therefore, we performed measurements up to 200 Mrad (SiO_2) to gain a preliminary overview of the behavior of these devices and their robustness to irradiation.

As shown in Figure 3.17, the percentage variation of I_{ON}^{sat} for nMOS and pMOS transistors with different gate oxide thicknesses (L: 9.5 nm, LT: 6.5 nm, BMT: bulk devices). Even though the BMT transistors are included and the results are presented, we will focus on L and LT devices as these are the possible candidates for our design. Unlike the standard devices, both thick gate oxide nMOS and pMOS show similar degradation of $\approx 50\,\%$, with the pMOS degradation slightly higher. The increase in gate oxide thickness makes both nMOS and pMOS less radiation-tolerant. However, there is a significant difference in degradation between the L and the LT devices, with the latter tending to have half the degradation of the former. This will be considered during the design of our FE.

Figure 3.18 shows the evolution of I_{OFF}^{sat} during irradiation up to 200 Mrad (SiO_2). I_{OFF}^{sat} increases less than an order of magnitude from its pre-radiation value for BMT devices but has a higher initial leakage current value. L and LT transistors suffer an increase in

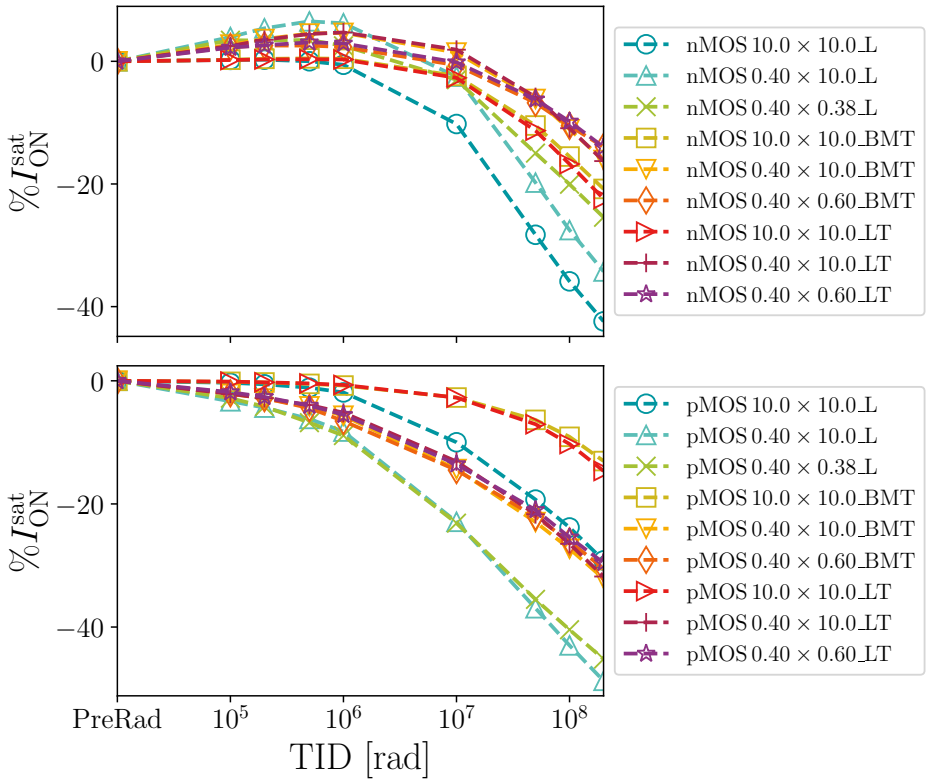

Figure 3.17: Percentage variation of I_{ON}^{sat} for nMOS (top) and pMOS (bottom) transistors with different gate oxide thicknesses (L: 9.5 nm, LT: 6.5 nm, BMT: Bulk).

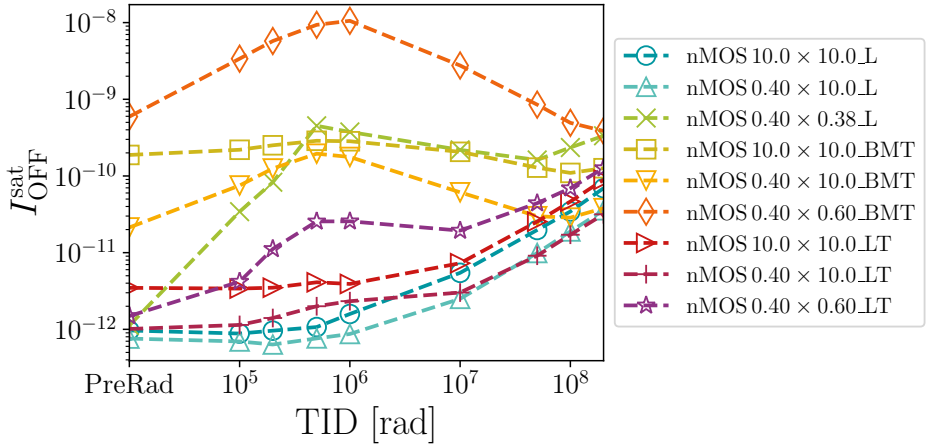

Figure 3.18: Variation of I_{OFF}^{sat} for nMOS transistors with different gate oxide thicknesses (L: 9.5 nm, LT: 6.5 nm, BMT: Bulk).

leakage current of almost two orders of magnitude. Both LT and L minimum size devices show a larger increase in I_{OFF}^{sat} during exposure.

3.9 Summary

TID can induce unexpected and unwanted effects that can deteriorate the performance of the design though the years of exposure. The TPSCo 65 nm CMOS image sensor technology will be incorporated in the development of monolithic active CMOS pixel sensors at CERN. Therefore it is important for the designers to have a characterization of the technology under irradiation sources. In this chapter, we presented the irradiation response of TPSCo 65 nm transistors, focusing on the standard devices (1.2 V) and thick oxide devices (3.3 V I/O).

We explained how to extract the maximum drain current in saturation ($I_{\mathrm{ON}}^{\mathrm{sat}}$), the leakage current in saturation ($I_{\mathrm{OFF}}^{\mathrm{sat}}$), the transconductance parameter (K_{U}), and the threshold voltage (V_{TH}). After reviewing the theory underlying the main irradiation effects (RINCE, RISCE, leakage current), we conducted an exhaustive analysis of these parameters and TID effects on standard devices. Irradiation results up to 1 Grad (SiO_2) prove the resilience of nMOS transistors to irradiation (max. $\approx 15\,\% I_{\mathrm{ON}}^{\mathrm{sat}}$ drop) while pMOS transistors show similar degradation (max. $\approx 80\,\% I_{\mathrm{ON}}$ drop) to other 65 nm studies. Irradiation test up to 300 Mrad (SiO_2) and subsequent annealing at 100 °C confirmed the presence of RISCE and RINCE. We measured V_{TH} shifts up to -200 mV, followed by a fast recovery of K_{U} and V_{TH} after annealing. In addition, we measured a small and monotonic radiation-induced leakage current increase on nMOS transistors of less than one order of magnitude. Minimum size devices show a higher increase of I_{OFF} during irradiation.

Two different processes are available for this technology: standard and modified. This irradiation study was performed in devices from WAF13 corresponding to the standard process. Moreover, a comparison with transistors from the modified process was offered, confirming the similar performance of both. Finally, a test on thick gate oxide devices demonstrated the higher vulnerability to TID of these devices, reaching both pMOS and nMOS L transistors a degradation of $\approx 50\,\%$ at 200 Mrad. However, LT devices seem to have a better performance due to their smaller gate oxide thickness (6.5 nm).

This chapter covers a preliminary characterization of this technology, but this subject requires further studies. Increasing the number of measured transistors will allow for quantifying the device-to-device variation. However, in view of these results, and taking into account the design of the front-end that will be presented, a few sizing recommendations can be extracted: (i) whenever possible it is recommended to use wide transistors (≥ 600 nm) and long transistors (≥ 500 nm) (ii) regarding radiation induced leakage current effects, it is not possible to correlate it neither with the width nor the length.

4 Study of TID and Back Bias Effects on the Analog Design Parameters

In Chapter 3, various parameters have been extracted from irradiation measurements, including the variation of the maximum drain current in saturation ($I_{\mathrm{ON}}^{\mathrm{sat}}$), the variation of the leakage current in saturation ($I_{\mathrm{OFF}}^{\mathrm{sat}}$), the transconductance parameter (K_{U}), and the threshold voltage (V_{TH}). Through the analysis of these parameters, we investigated the TID effects on this technology. Some conclusions drawn from this chapter include the resilience of nMOS transistors to irradiation, the increase in resistivity on the sides of the channel due to the accumulation of positive charges on the spacers, the variation of the threshold voltage during annealing, and the degradation of the leakage current during irradiation. The process demonstrated sensitivity to radiation and degradation mechanisms similar to previously studied 65 nm CMOS technologies [73].

Over the past years, numerous publications have utilized these Figures of Merit (FoMs) to investigate the physics underlying TID effects [64, 67, 68, 74, 75]. However, the parameters were derived from the traditional representation of the $I_{\mathrm{D}}(V_{\mathrm{GS}})$ characteristic of a transistor, dependent on the overdrive voltage $V_{\mathrm{OV}} = V_{\mathrm{GS}} - V_{\mathrm{TH}}$ as shown in

$$I_{\mathrm{D,\,max}} = \frac{1}{2}\mu_n C_{\mathrm{OX}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2. \tag{4.1}$$

This renders them an outdated representation of how TID can affect the analog performance of more advanced technology nodes, where the operating point tends to be closer to weak inversion[I].

Therefore, building upon the work presented in [10–12] on the 28 nm node, this chapter offers a characterization of these effects using the simplified EKV Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) model introduced in Section 4.1.1. This model employs four parameters to fully describe the performance of a transistor over the range from weak to strong inversion. This allows us to study not only the

[I] Weak inversion is the biasing stage when the gate voltage is below the threshold voltage.

transconductance efficiency but also the large- and small-signal parameters across a wide range of operating points. For the extraction, we make use of a Python routine, presented in Section 4.2, capable of extracting the four main parameters describing the EKV model at different irradiation levels and bulk biases. After introducing this routine, we will employ it to study TID effects on large-signal characteristics in Section 4.3 and small signal characteristics in Section 4.4. Finally, we will offer a brief study regarding the effect of back biasing on analog performance in Section 4.5, using the proposed EKV extractor to understand how the bulk effect affects the main parameters used in the EKV model.

4.1 Modelling of MOS Devices Using the EKV Model

4.1.1 The Simplified EKV Model

The downscaling of the CMOS technologies during the past years allowed for increasing the number of transistors per chip, improving the functionality together with the transient performance. This downscaling comes with a lower supply voltage, which is advantageous regarding the power consumption of the circuits. However, the threshold voltage could not be scaled by the same ratio as this would increase the drain leakage current [76]. This reduces the overdrive voltage $V_{\mathrm{OV}} = V_{\mathrm{GS}} - V_{\mathrm{TH}}$, moving the operating point of the transistors from strong to moderate or even weak inversion. The simplified charge-based EKV (sEKV) MOSFET model offers a transistor description that spans from strong to weak inversion [77]. It introduces the Inversion Coefficient (IC) to replace the overdrive voltage $V_{\mathrm{GS}} - V_{\mathrm{TH}}$, which is defined as:

$$\mathrm{IC} = \frac{I_{\mathrm{D}}}{I_{\mathrm{SPEC}}} \tag{4.2}$$

where the specific current I_{SPEC} can be defined as [78]

$$I_{\mathrm{SPEC}} = I_{\mathrm{spec}\square}\frac{W}{L} \tag{4.3}$$

and the specific current per square $I_{\mathrm{spec}\square}$ is

$$I_{\mathrm{spec}\square} = 2nU_{\mathrm{T}}^2\mu_0 C_{\mathrm{OX}} \tag{4.4}$$

with n being the slope factor, U_{T} is the thermal voltage, μ_0 is the channel mobility and C_{OX} is the gate oxide capacitance per unit area. The IC determines the channel inversion level of a MOSFET [13, 79]:

- **IC $<$ 0.1 or weak inversion (WI)** is the zone where we can achieve the highest current efficiency (i.e. maximize the transconductance given a current) and the minimum V_{DSat}. It is recommended for low-power designs and offers better mismatch for differential pairs.
- **0.1 $<$ IC $<$ 10 or moderate inversion (MI)** is the zone where we can achieve a good trade off between speed and current efficiency.
- **IC $>$ 10 or strong inversion (SI)** is the zone where we can achieve the highest speed and better mismatch for current mirrors.

The following equation represents the normalized transconductance efficiency as a function of the normalized drain current:

$$\frac{G_m n U_{\mathrm{T}}}{I_{\mathrm{D}}} = \frac{\sqrt{(\lambda_{\mathrm{c}}\mathrm{IC}+1)^2+4\mathrm{IC}}-1}{\mathrm{IC}[\lambda_{\mathrm{c}}(\lambda_{\mathrm{c}}\mathrm{IC}+1)+2]} \tag{4.5}$$

The equation includes the velocity of saturation (VS) effects in short channel devices, where λ_{c} [80] is

$$\lambda_{\mathrm{c}} = \frac{L_{\mathrm{sat}}}{L} \tag{4.6}$$

with L_{sat} being the portion of the channel where the carrier drift velocity saturates. In the EKV model the $I_{\mathrm{D}}(V_{\mathrm{G}})$ of a MOSFET in saturation is

$$\frac{V_{\mathrm{G}} - V_{\mathrm{TH}} - nV_{\mathrm{S}}}{nU_{\mathrm{T}}} = \log[q_{\mathrm{s}}/2] + q_{\mathrm{s}} \tag{4.7a}$$

$$q_{\mathrm{s}} = \sqrt{(\lambda_{\mathrm{c}}\mathrm{IC}+1)^2+4\mathrm{IC}}-1 \tag{4.7b}$$

where V_{TH} is the threshold voltage and V_{S} the voltage from source to bulk. From this normalization we can see that with only four parameters ($V_{\mathrm{TH}}, \lambda_{\mathrm{c}}, I_{\mathrm{spec}}, n$) the EKV can model the behavior of a MOSFET from weak to strong inversion continuously and independently of the technology.

4.1.2 Modeling of Gate Capacitances

Some of the noise sources of the processing chain depend on the gate capacitances. Later on, to model the total ENC contribution in any region of inversion, these capacitances need to be correctly described. The intrinsic gate capacitance of a MOS device is equal

to the sum of the capacitances gate-to-source, gate-to-bulk and gate-to-drain. Using the EKV model, the unitary gate-to-source (C_{GSU}) and gate-to-bulk (C_{GBU}) capacitances are [81]:

$$C_{\mathrm{GSU}} = C_{\mathrm{OXU}}\left(\frac{1}{\mathrm{IC}f(\mathrm{IC})} + \frac{3}{2}\right)^{-1} \tag{4.8}$$

$$C_{\mathrm{GBU}} = C_{\mathrm{OXU}}\frac{n-1}{n}\left(1 - \frac{\mathrm{IC}f(\mathrm{IC})}{1+\frac{3}{2}\mathrm{IC}f(\mathrm{IC})}\right) \tag{4.9}$$

where $f(\mathrm{IC})$ is

$$f(\mathrm{IC}) = \frac{1}{\frac{1}{2}\left(1+\sqrt{4\cdot \mathrm{IC}+1}\right)}, \tag{4.10}$$

n is the slope factor, and C_{OXU} is the unitary gate oxide capacitance per unit area, which is calculated as

$$C_{\mathrm{OXU}} = \frac{\epsilon_{\mathrm{OX}}}{t_{\mathrm{OX}}}. \tag{4.11}$$

In the previous expression, t_{OX} denotes the thickness of the oxide layer, and ϵ_{OX} the permittivity of the oxide layer. The total gate-to-source (C_{GS}), gate-to-bulk (C_{GB}) and gate-to-drain (C_{GD}) are:

$$C_{\mathrm{GS}} = C_{\mathrm{GSU}}WL \tag{4.12}$$

$$C_{\mathrm{GB}} = C_{\mathrm{GBU}}WL \tag{4.13}$$

$$C_{\mathrm{GD}} = C_{\mathrm{OXU}}W \tag{4.14}$$

4.2 Proposal of EKV Parameters Extractor using Python

The progressive downscaling of MOSFETs made compact models such as the Berkeley Short-channel IGFET Model (BSIM) [82] have become more complex to meet the demands of these advanced technology nodes. This complexity poses a challenge for

analog integrated circuit designers, making it more difficult to strike the right trade-off between transistor sizing and bias current.

The sEKV model offers an alternative to these models, utilizing four parameters for modeling the operating point from weak to strong inversion through the IC design methodology. This makes it a suitable choice for designing analog integrated circuits based on more modern technologies. However, to employ this methodology, the four parameters must be extracted since they are not readily available in the PDK. Extraction can be done manually from simulations or measurements [78, 83], turning this iterative process into a time-consuming task with several iterations needed to find the best match.

Recently, an open-source Python-based parameter extractor (SEKV-E) [9] has been published. The tool extracts sEKV parameters from given transfer characteristics using the direct extraction and the multi-stage optimization process. It effectively addresses the overfitting issue arising from nonlinear least squares and can be applied to various technologies, temperatures, dimensions, and back-gate voltages. However, it lacks the capability to extract parameters at different irradiation levels.

The tool we have developed builds upon SEKV-E as a starting point. However, it takes a more natural approach, leveraging the mathematics and physics underlying the model to extract each parameter. It initially leaves aside the velocity of saturation effect, incorporating it at the final stage of the extraction. Additionally, it sidesteps pre-filtering of the data to prevent missing information. The overfitting issue due to the nonlinearity of the nonlinear least squares (also well-addressed in SEKV-E) is rectified in our code by weighting the cost function. On the following paragraphs we will explain the different steps of the optimization done by our code (available at [8]) using simulation data as an example.

Step 1: Extraction of n and First Approximation of $I_{\mathbf{spec}}$ (assuming $\lambda_{\mathbf{c}} = 0$)

For the first part of the extraction we will need to use either simulated or measured $I_{\mathrm{D}}(V_{\mathrm{GS}})$ curves. For this proof of concept we will use simulation data from a wide and a short nMOS transistor. Calculating the derivative of I_{D} with respect to V_{GS} we can obtain the gate transconductance G_m. Assuming no velocity of saturation effects, Equation (4.5) reduces to:

$$f(\mathrm{IC}) = \frac{G_m n U_{\mathrm{T}}}{I_{\mathrm{D}}} = \frac{2}{1 + \sqrt{4\mathrm{IC} + 1}} \tag{4.15}$$

In weak inversion IC has values close to zero. Therefore, assuming IC ≈ 0 we can express the slope factor as:

$$n = \frac{I_{\mathrm{D}}}{U_{\mathrm{T}} G_m} \tag{4.16}$$

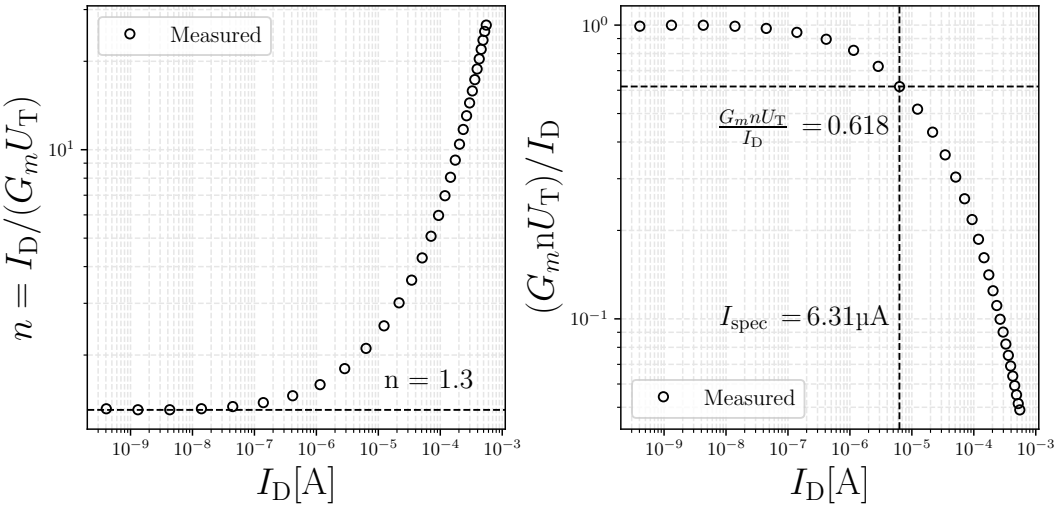

Figure 4.1: First step (left): n as a function of I_{D}. The slope factor can be extracted from the plateau and its value will be fixed for the rest of the extraction as it is free from velocity of saturation effects. Second step (right): $G_m n U_{\mathrm{T}}/I_{\mathrm{D}}$ as a function of I_{D}. I_{spec} is the value of I_{D} where $G_m n U_{\mathrm{T}}/I_{\mathrm{D}}$ becomes 0.618. The extracted value of I_{spec} must be adjusted later on the optimization process, as it is dependent on velocity of saturation effects.

Using the previously calculated transconductance, the simulated drain current and assuming $U_{\mathrm{T}} = 26\,\mathrm{mV}$ we can plot n as a function of I_{D}, as shown in Figure 4.1. The slope factor can be extracted from the flat region and its value will be fixed for the rest of the extraction. At moderate inversion IC = 1 and $I_{\mathrm{spec}} = I_{\mathrm{D}}$ such that Equation (4.15) will be equal to the golden ratio:

$$\frac{G_m n U_{\mathrm{T}}}{I_{\mathrm{D}}} = \frac{2}{1+\sqrt{5}} \approx 0.618 \tag{4.17}$$

We can extract I_{spec} as the value of I_{D} where $G_m n U_{\mathrm{T}}/I_{\mathrm{D}}$ becomes 0.618, as plotted in Figure 4.1. However, this value of I_{spec} is a first approximation as it is dependent on velocity of saturation effects and therefore we will need to optimize it.

Step 2: Optimization of λ_{c} and I_{spec} (assuming Velocity of Saturation Effects)

With the extracted values of I_{spec} and n, and assuming an initial value for λ_{c} ($\lambda_{\mathrm{c}} = 0$ in our code) we can plot $G_m n U_{\mathrm{T}}/I_{\mathrm{D}}$ using the simulation data and Equation (4.5). We will see that both curves do not match so we will use an optimizer for reducing the large

fitting error of I_{spec} and λ_c. Using global optimization, we find the global minimum of the fit cost function within the given bounds. The many local minima are effectively handled by the employed differential evolution algorithm [84]. The cost function will be the sum of the squares of the residuals (least squares), being the residuals the difference between the value extracted from the simulation and the one obtained from the model. The bounds will allow us to extract values with a realistic physical meaning ($0 < \lambda_c < 1$, and $0 < I_{\text{spec}}$). Figure 4.2 shows the curves before and after the optimization. The over-fitting on the strong inversion region due to denser sampling is avoided weighting the cost function by using the square root of the differences between the drain current samples. The values extracted for λ_c and I_{spec} will be fixed for the rest of the extraction.

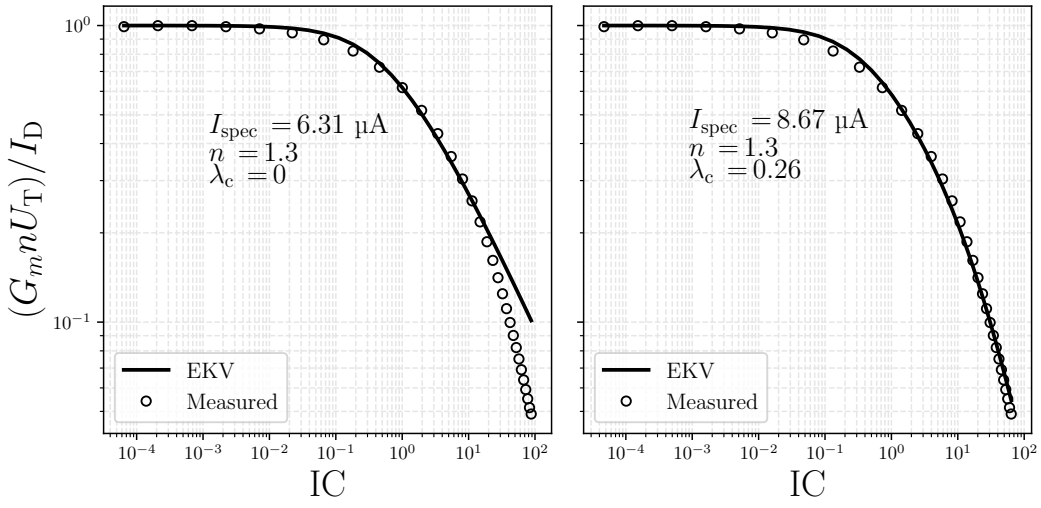

Figure 4.2: Plot of $G_m nU_T/I_D$ using the simulation data and Equation (4.5) before optimization (left) and after optimization (right). To avoid over-fitting on the strong inversion region due to denser sampling, we weighted the cost function using the square root of the differences between the drain current samples.

Step 3: Extraction of threshold voltage V_{TH}

Having fixed I_{spec}, λ_c, and n it is possible to plot the $I_D(V_G)$ curve after the extraction. We can plot the measured $I_D(V_{GS})$ curves together with the modeled ones using (4.7a). To extract the threshold voltage we will follow the same methodology as before. In Figure 4.3 we can see the $I_D(V_{GS})$ curves before (left) and after (right) optimizing.

Step 4: Extraction of output conductance G_{DS}

The extraction of the drain-to-source output conductance (G_{DS}) is done directly from the simulation data. To do so, we need $I_D(V_{DS})$ measurements at different gate voltages.

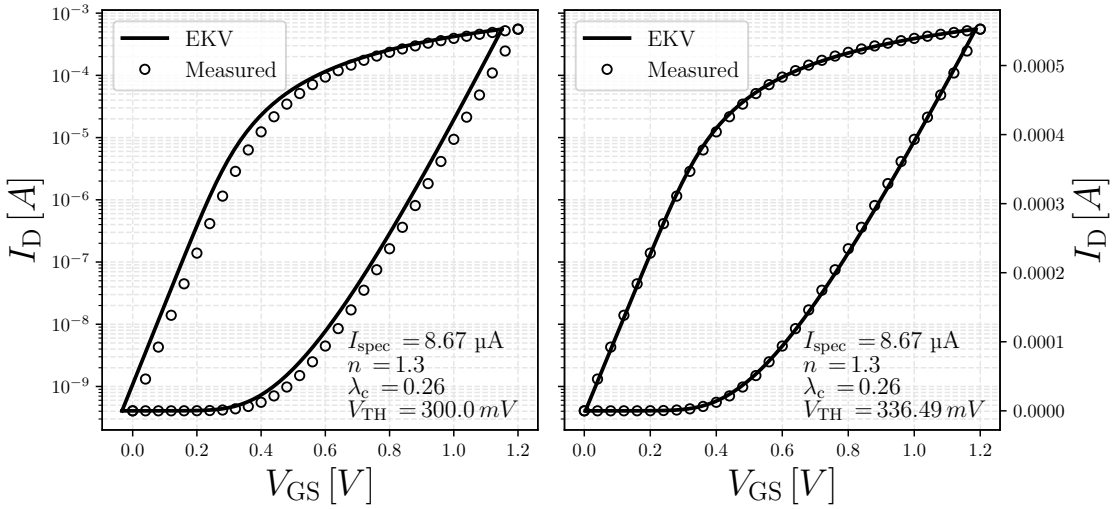

Figure 4.3: $I_D(V_{GS})$ curves before (left) and after optimizing (right) in both linear and logarithmic scale. The four main parameters (I_{spec}, n, λ_c, V_{TH}) are also reported.

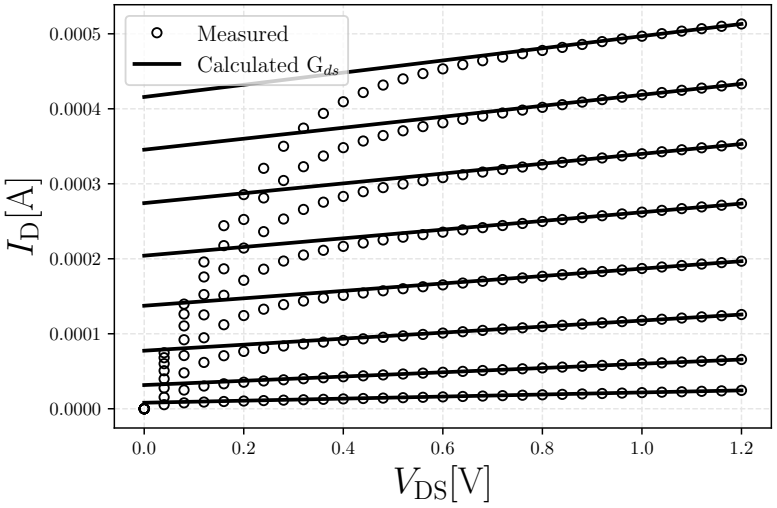

Figure 4.4: $I_D(V_{DS})$ curves before irradiation and calculated G_{DS} for different gate voltages ranging from 0.2 V to 1.2 V.

From each curve we will calculate the derivative and G_{DS} will be the mininum absolute value, which tends to be at $V_{DS} = 1.2\,V$.

Conclusion

The extraction example has demonstrated how the proposed code effectively handles the extraction of the main sEKV parameters using simulation data from a long and narrow nMOS transistor. In the following sections, we will employ this extractor to investigate

the Total Ionizing Dose (TID) effects on both large and small signal characteristics, along with the impacts of different back-gate biases on this technology. Throughout this exploration, we will observe how TID induces degradation in each of the parameters, consequently affecting the transfer characteristics.

However, the normalized transconductance will prove to be robust against these variations, rendering it a valuable tool in analog design across different biasing scenarios.

4.3 TID Effects on Large-Signal Characteristics

Analysis of large-signal characteristics is essential for examining circuits where transistors amplify or process signals that are not small variations around the quiescent operating point. It is crucial for understanding how the devices behave under different operating conditions and input signal levels [65]. In this section we will cover the TID effects on the transfer characteristics and the four parameters of the EKV model.

4.3.1 TID Effects on $I_{\mathrm{D}}(V_{\mathrm{GS}})$ Characteristics

Figure 4.9 illustrates the large-signal transfer characteristic extraction for four different sizes of nMOS (blue) and pMOS (orange): wide and long, narrow and long, wide and short, and minimum size. Filled symbols represent the transfer characteristics before irradiation, and the contour symbols represent measurements at 1 Grad. Black lines correspond to the sEKV extraction. The simplified EKV MOSFET model aligns with the measurements from pre-irradiation, passing through all TID levels, up to 1 Grad.

The comparison between pre-irradiation measurements and those at high TID indicates an increase in leakage current during irradiation in narrow and minimum size nMOS devices but demonstrates robustness regarding drain current degradation. Narrow and short pMOS devices exhibit significant drain current degradation alongside a slight threshold voltage shift due to TID effects. These results highlight that the sEKV model can match the pre-irradiation measurements on all different levels of inversion with these four parameters. However, irradiation effects cause the extracted parameters to differ from pre-irradiation measurements, as will be shown in the following sections.

4.3.2 TID Effects on EKV Model Parameters

Slope Factor

Figure 4.5 shows the evolution of the slope factor (n) with TID for four different extreme sizes of nMOS (blue) and pMOS (orange) transistors. All nMOS transistors experience an increase in their slope factor with TID, with the two narrow transistors being more

vulnerable. The pMOS devices show a smaller increase, except for the narrow devices. This slight increase might be due to the negative gate voltage, which is unfavorable for hole transport. The increase in the nMOS corresponds to the charges trapped on the STI interface, which will induce a negative threshold voltage shift and an increase in the slope factor.

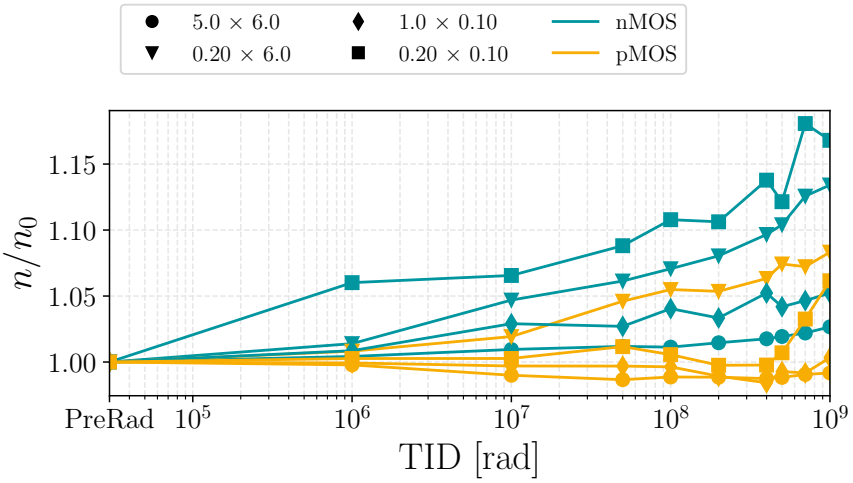

Figure 4.5: Evolution of the slope factor n with TID for four different extreme sizes of nMOS (blue) and pMOS (orange) transistors. Narrow nMOS transistors exhibit a more significant increase, while pMOS devices, especially in narrow configurations, show a slight upward trend, influenced by charge trapping effects on the STI interface.

Specific Current

Figure 4.6 illustrates the evolution of the specific current (I_{spec}) with TID for four different extreme sizes of nMOS (blue) and pMOS (orange) transistors. In nMOS transistors, the variation of the specific current is negligible; however, there is a considerable degradation in pMOS devices. This variation follows the same trend as the degradation of the drain current described in Section 3.3. However, it could be induced by charges accumulated at the spacers or the STI.

Figure 4.7 shows the variation of I_{spec} for pMOS transistors with a fixed length and different widths, and vice versa. It can be observed that keeping the length to the technological minimum and varying width will not reduce the current degradation. However, maintaining the width at a more moderate value and varying the length will ameliorate the degradation. Additionally, examining transistor 0.20 µm x 6.00 µm in Figure 4.7, the decrease of I_{spec} is similar to the maximum size device. Therefore, we can conclude that shorter transistors will experience a major degradation of I_{spec} due to the charges accumulated on the spacers.

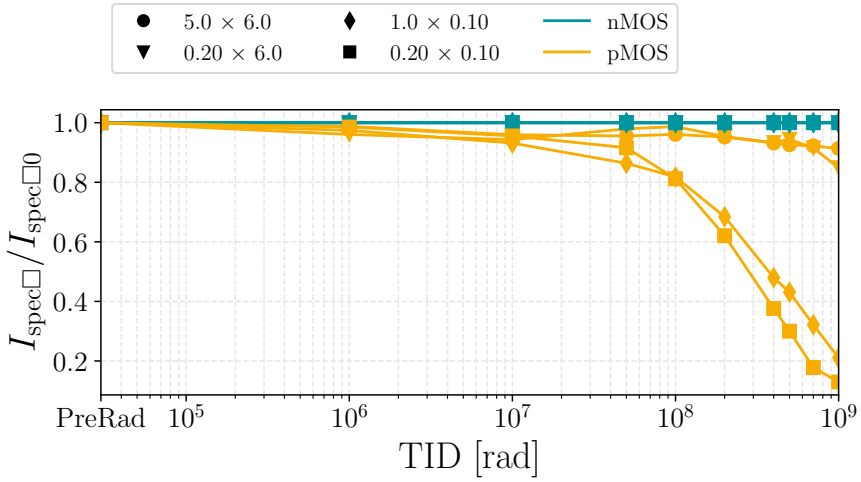

Figure 4.6: Evolution of the specific current (I_{spec}) with TID for four different extreme sizes of nMOS (blue) and pMOS (orange) transistors. In nMOS transistors, the variation of the specific current is negligible; however, there is a considerable degradation in pMOS devices.

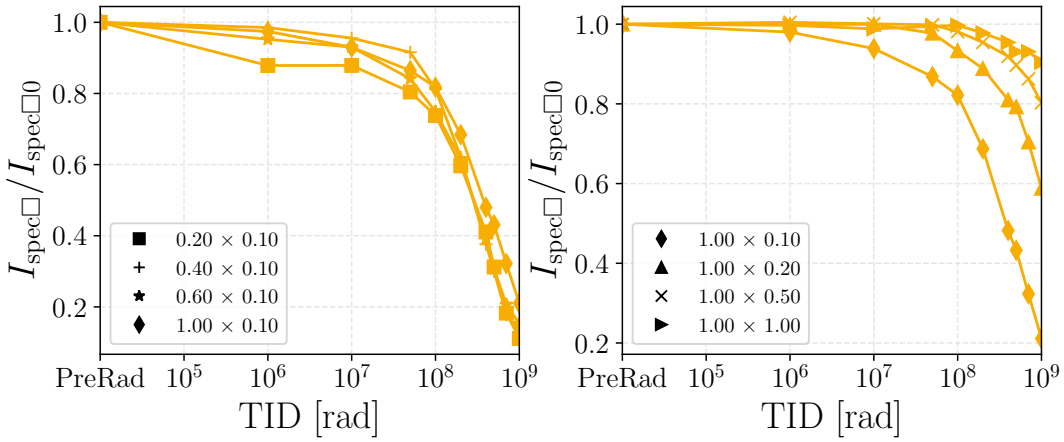

Figure 4.7: Variation of I_{spec} for pMOS transistors with a fixed length and different widths (left), and pMOS transistors with fixed width and different lengths (left).

Threshold Voltage

Figure 4.8 illustrates the evolution of the threshold voltage (V_{TH}) with TID for four different extreme sizes of nMOS (blue) and pMOS (orange) transistors. The shift in the threshold voltage of nMOS devices is negative, while for the pMOS, it is positive. This difference is attributed to the opposite sign of the charges in the channel and their interaction with the positive charges accumulating on the STI (Subsection 3.1.3). However, the shift is approximately 50 mV, which, for our purposes, is negligible. It is also

worth mentioning that the dropping and sudden recovering of the threshold voltage for nMOS devices matches with the non-monotonic behavior presented in Subsection 3.6.1.

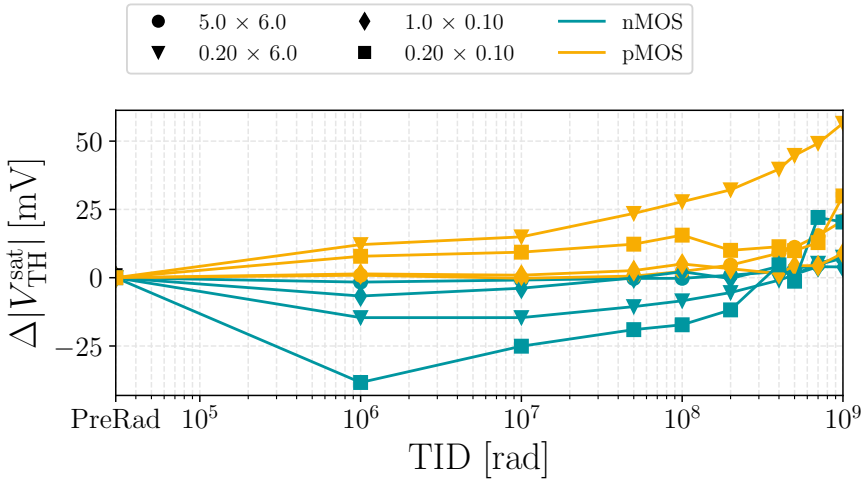

Figure 4.8: Evolution of the threshold voltage (V_{TH}) with TID for four different extreme sizes of nMOS (blue) and pMOS (orange) transistors.

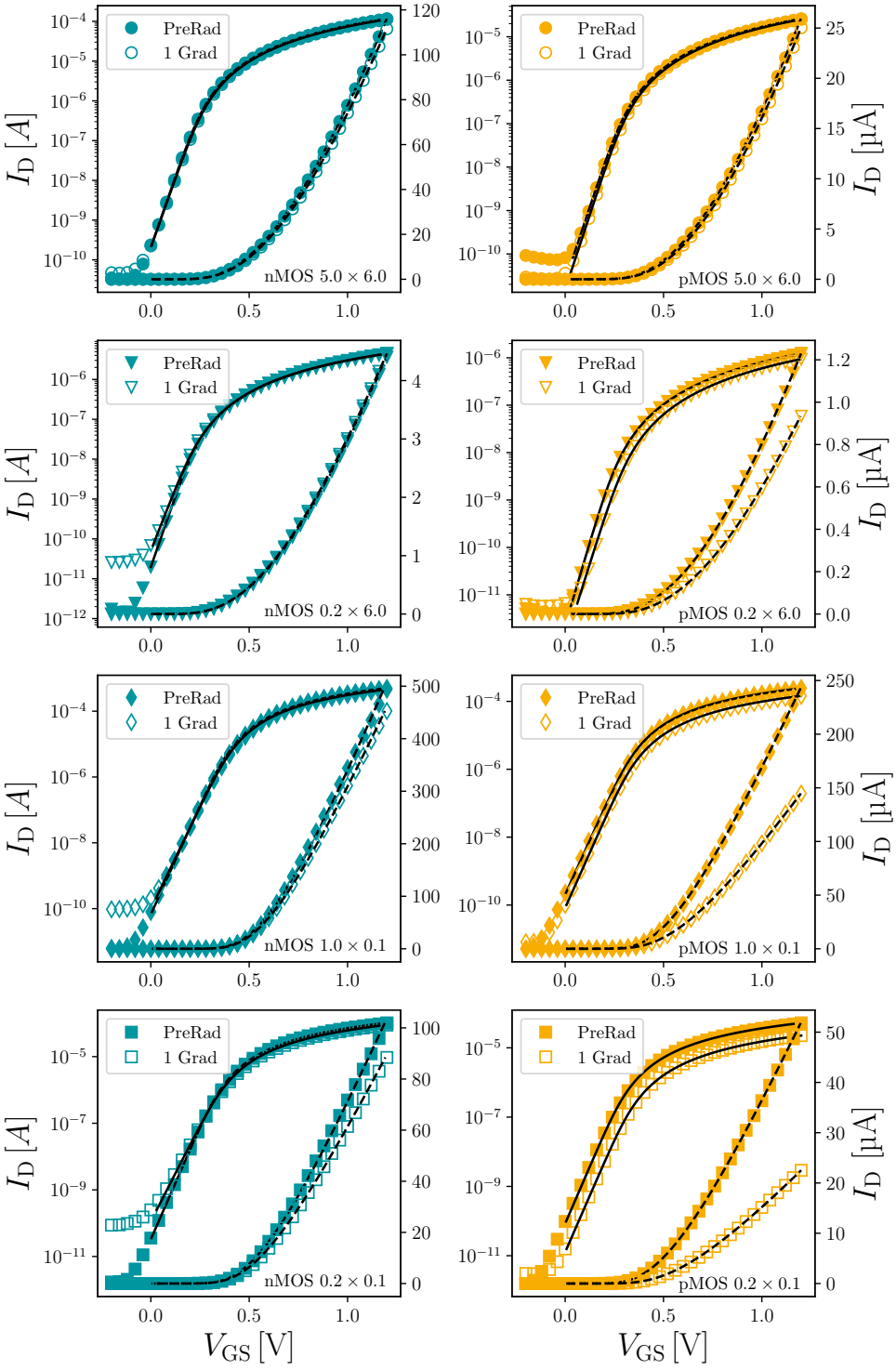

Figure 4.9: Large-signal transfer characteristic extraction for four different sizes of nMOS (blue) and pMOS (orange): wide and long, narrow and long, wide and short, and minimum size. Filled symbols represent the transfer characteristics before irradiation, and the empty ones represent measurements at 1 Grad. Black lines correspond to the EKV extraction.

4.4 TID Effects on Small-Signal Characteristics

Small-signal analysis aids in determining parameters such as transconductance (G_m), output conductance (G_{DS}), and intrinsic gain by examining the linearized small-signal model of the transistor around its operating point. Small-signal models simplify the analysis of complex circuits and are frequently utilized in the design of amplifiers which rely on the intrinsic gain of the input transistors [65]. In this section we will see how TID can affect the output conductance and how the normalization removes the effect of irradiation.

4.4.1 TID Effects on Output Conductance

Figure 4.10 displays the output characteristic of a wide and short nMOS transistor (left) and a pMOS transistor (right) before (filled symbols) and after (contour symbols) irradiation. These values of G_{DS} were extracted from the measurements and not from the model. Generally, the nMOS transistors of this technology exhibit significant robustness to TID, and this applies to the output conductance as well. Under TID, there is a slight increase in the Early voltage[II] along with a decrease in G_{DS}, but both are negligible compared to the effects observed in pMOS devices. In the case of narrow and short pMOS devices, degradation due to RISCE also affects the Early voltage, which increases and nearly halves the output conductance. This will have a significant effect on the intrinsic gain of pMOS devices, which will tend to have a higher intrinsic gain during irradiation, while the nMOS devices will maintain a relatively stable one.

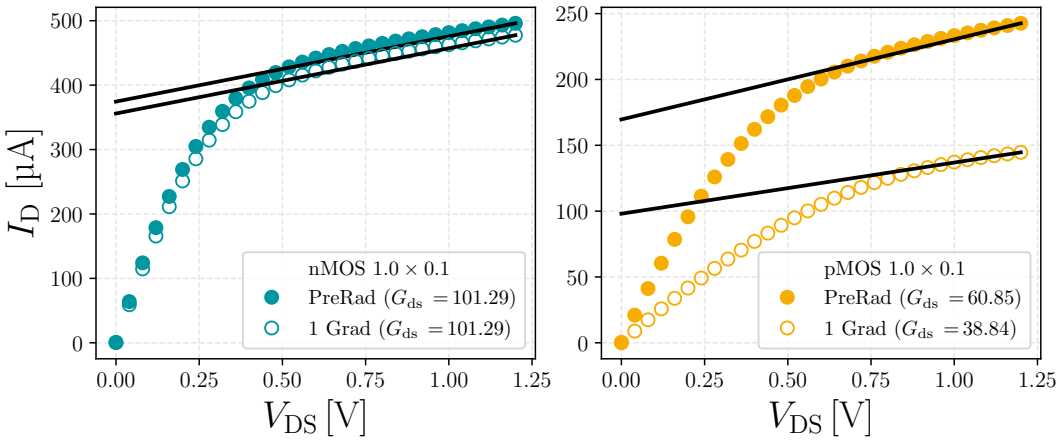

Figure 4.10: Output characteristic of a wide and short nMOS transistor (left) and a pMOS transistor (right) before (filled symbols) and after (empty symbols) irradiation. These values of G_{DS} were extracted from the measurements and not from the model.

[II]The Early voltage (V_A) is defined as the extrapolated drain-to-source voltage (V_{DS}) at which the drain current (I_{D}) would theoretically become zero, indicating the point where the output conductance (G_{DS}) is zero.

4.4.2 TID Effects on Transconductance Efficiency

Transconductance efficiency, introduced in Section 4.1.1, is influenced by velocity of saturation effects, making the irradiation effects on λ_c more pronounced in short devices. Figure 4.11 illustrates the normalized transconductance efficiency of wide and long, as well as wide and short, nMOS transistors (blue) and pMOS transistors (orange) before and after irradiation in relation to the inversion coefficient. The respective values of λ_c are also provided.

The presence of velocity of saturation effects is evident in short-channel devices, where the transconductance efficiency experiences a more rapid decline. This behavior is effectively captured by λ_c. At high TID levels, under strong inversion, there is a slight degradation in the transconductance efficiency for short nMOS devices, while there is an increase for short pMOS devices. However, the variation is negligible. It is important to highlight that all measured points before and after high TID levels closely align with the curves of the simplified EKV MOSFET model, emphasizing the insignificant impact of TID on normalized transconductance.

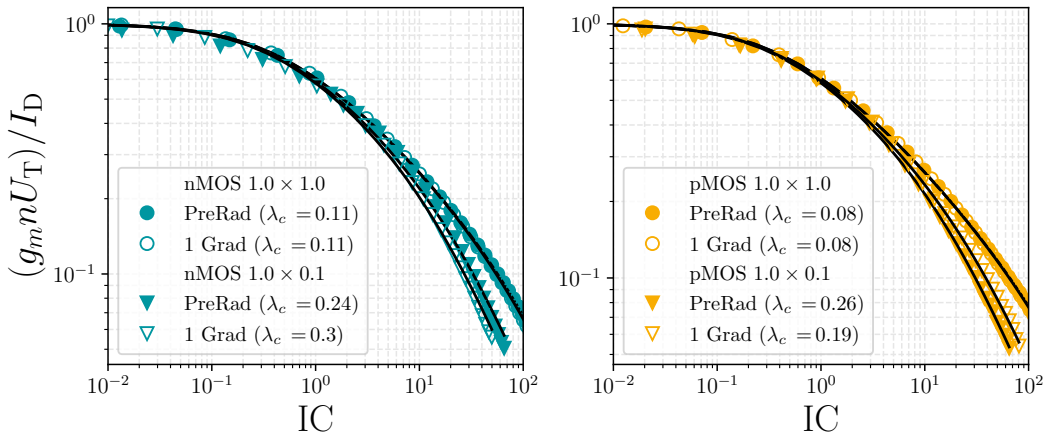

Figure 4.11: Normalized transconductance efficiency of wide and long, as well as wide and short, nMOS transistors (blue) and pMOS transistors (orange) before and after irradiation in relation to the inversion coefficient. The respective values of λ_c are also provided.

4.5 Influence of Back Bias on the Analog Performance

4.5.1 Body Effect

There are certain pixel designs where the nMOS transistors on the pixel matrix are biased with their bulk to source at voltages down to $-6\,\mathrm{V}$. This is done to fully deplete the sensor in order to improve the charge collection [40, 41]. However, significant reverse bulk bias might induce a considerable threshold voltage shift due to the body effect and

therefore a decrease of the maximum drain current [65]. Using Figure 4.12 as a reference, on the nMOS depicted in Figure 4.12a we assume that the transistor is biased with certain drain-to-source voltage (V_{DS}). The gate-to-source voltage (V_{GS}) is smaller than the threshold voltage (V_{TH}) but large enough to create a depletion layer without inverting the channel. As we start to decrease the voltage from substrate to source (V_{PWELL}) more electrons will move to this depletion layer from the substrate, leaving holes behind, as described in Figure 4.12b. V_{TH} is related to the charge at the depletion layer following [85]:

$$V_{\mathrm{TH0}} = \phi_{\mathrm{MS}} + 2\phi_{\mathrm{F}} + \frac{Q_{\mathrm{d}}}{C_{\mathrm{OX}}} \tag{4.18}$$

In this equation, V_{TH0} represents the threshold voltage, ϕ_{MS} is the metal-semiconductor work function difference, ϕ_{F} denotes the semiconductor Fermi potential, Q_{d} signifies the charge at the depletion layer, and C_{OX} stands for the oxide capacitance. This implies that we will need a higher value of V_{GS} to create an inversion layer, as the V_{TH} will increase as Q_{d} increases and V_{PWELL} decreases. This body effect can be mathematically described as

$$V_{\mathrm{TH}} = V_{\mathrm{TH0}} + \gamma(\sqrt{2\phi_{\mathrm{F}} + V_{\mathrm{SB}}} - \sqrt{|2\phi_{\mathrm{F}}|}) \tag{4.19}$$

where V_{SB} is the voltage from source to bulk and γ is the body effect coefficient. The increase of threshold voltage shift due to the body effect will therefore decrease the maximum drain current. These two consequences must be carefully studied in order to avoid unexpected behaviours on the analog designs [7].

4.5.2 Back Bias Measurements and Simulations

In order to study the influence of negative bulk biasing on nMOS devices, we measured the $I_{\mathrm{D}}(V_{\mathrm{GS}})$ curves for maximum and minimum size devices, with their bulks biased at 0 V, −1.2 V, and −6 V. The results are plotted in Figure 4.13. The extracted values of V_{TH} and its respective shift from the nominal value (at $V_{\mathrm{PWELL}} = 0\,\mathrm{V}$) are shown in Table 4.1. Measurements of nMOS transistors with a pwell biasing of −6 V show an increase of the nominal V_{TH} of ≈260 mV together with a ≈ 40% drop of $I_{\mathrm{ON}}^{\mathrm{sat}}$.

In the interest of testing the accuracy of the models, we compared the measurements with the simulations using typical (TYP) corner[III]. The extracted values of V_{TH} and $I_{\mathrm{ON}}^{\mathrm{sat}}$, together with their shift and percentage of variation from the nominal value (at

[III] Corner simulations enable circuit designers to evaluate the behavior of their designs under variations in temperature, supply voltage, ground voltage, and process parameters. The term S denotes slow process variations, TYP represents typical process variations, and F signifies fast process variations.

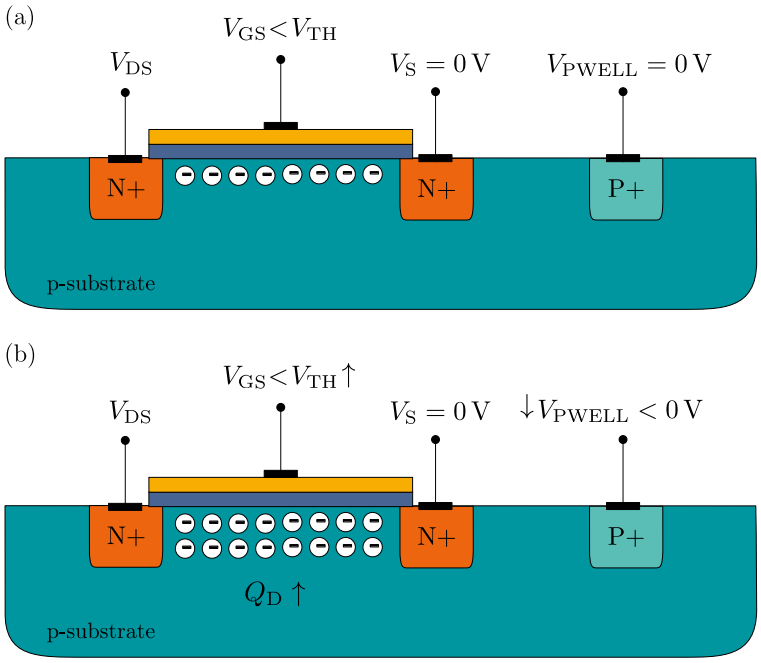

Figure 4.12: Representation of the "body effect". In a) the nMOS device is biased with a V_{GS} not over V_{TH} but enough to create a depletion layer. In b) the V_{PWELL} drops, the charge at the depletion layer (Q_d) increases forcing the V_{TH} to increase. Therefore we will need a higher V_{GS} to invert the channel.

Table 4.1: Extracted values of V_{TH} from the measurements and simulation (TYP corner) showed at Figure 4.13 for $V_{PWELL} = 0, -1.2\,V, -6\,V$. The respective V_{TH} shift from the nominal value (V_{TH}^{sat} measured at $V_{PWELL} = 0, -1.2\,V, -6\,V$) is shown in parenthesis.

Size [µm]	V_{PWELL} [V]	$\lvert V_{TH}^{sat}\rvert$ [mV]	$\lvert V_{TH,\,TYP}^{sat}\rvert$ [mV]	
5.0/6.0	0	223.4	223.1	(−0.4)
	-1.2	354.7	352.5	(−2.2)
	-6	487.1	650.5	(+163.5)
0.2/0.1	0	315.2	241.1	(−74.1)
	-1.2	413.7	321.8	(−91.1)
	-6	483.2	371.3	(−111.9)

$V_{PWELL} = 0, -1.2\,V, -6\,V$), can be found on Table 4.1 and Table 4.2 respectively. Figure 4.13 reports the simulated (BSIM) $I_D(V_{GS})$ characteristics in black color to ease the comparison with the measurements. In the case of the maximum size device, at a bias of $-6\,V$, the measured V_{TH} error with respect to the simulation reaches $\approx 160\,mV$. Regarding the minimum-size device, for both the V_{TH} and I_{ON}^{sat} there is a significant error compared with the simulation, but on the same order of magnitude for the three biases. However, the V_{TH} shift is overestimated for maximum size devices and underestimated for minimum size devices, in both cases not accurate at large reverse biases.

Table 4.2: Extracted values of I_{ON}^{sat} from the measurements and simulation (TYP corner) showed at Figure 4.13 for $V_{PWELL} = 0, -1.2\,V, -6\,V$. The respective percentage of variation of I_{ON}^{sat} from the nominal value (I_{ON}^{sat} measured at $V_{PWELL} = 0, -1.2\,V, -6\,V$) is shown in parenthesis.

Size [µm]	V_{PWELL} [V]	I_{ON}^{sat} [µA]	$I_{ON,\ TYP}^{sat}$ [µA]	
	0	109.5	118.4	(7.8 %)
5.0/6.0	-1.2	80.5	87.7	(8.9 %)
	-6	64.6	44.6	(−30.4 %)
	0	101.2	120.0	(18.6 %)
0.2/0.1	-1.2	84.4	104.8	(24.1 %)
	-6	76.5	98.2	(28.4 %)

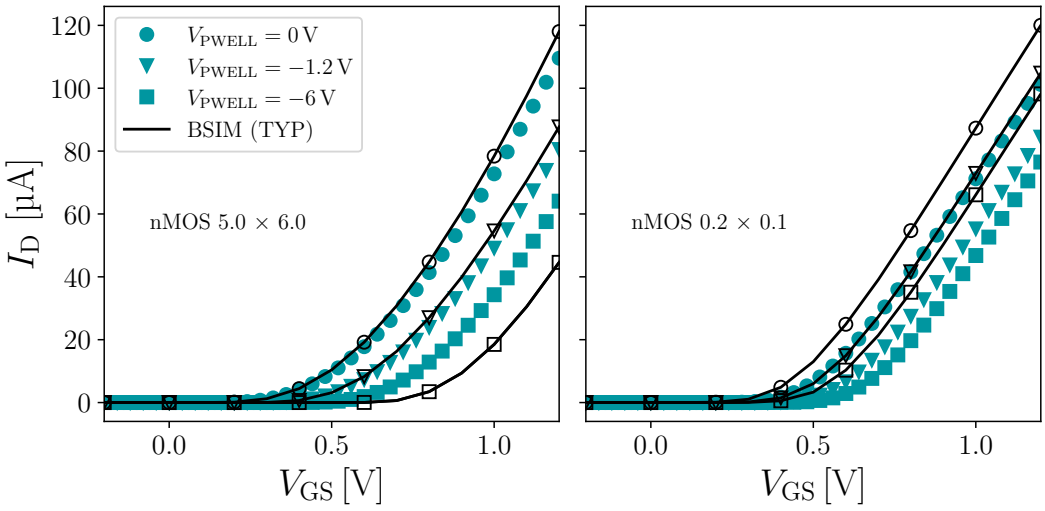

Figure 4.13: $I_D(V_{GS})$ of a maximum size 5 µm x 6 µm device (left) and a minimum size 0.2 µm x 0.1 µm device (right) measured at $V_{PWELL} = 0\,V$ (circles), at $V_{PWELL} = -1.2\,V$ (triangles) and at $V_{PWELL} = -6\,V$ (squares). Black colored curves correspond to their equivalent simulations (TYP corner).

4.5.3 EKV Back Bias Fitting

The previous simulations employed the BSIM model available in the design kit. The sEKV extractor introduced earlier can also be utilized to capture the effects of the back-gate voltage on the analog performance of this technology. Figure 4.14 illustrates the measured $I_D(V_{GS})$ curves for maximum and minimum size devices, with their bulks biased at 0 V, −1.2 V, and −6 V along with the EKV fit. The extraction is successful in comparison to the approximation of the BSIM model for back-gate voltages down to −6 V. Table 4.3 showcases the influence of the bulk bias on the four parameters ($V_{TH}, \lambda_c, I_{spec}, n$) that the sEKV employs to model the behavior of a MOSFET.

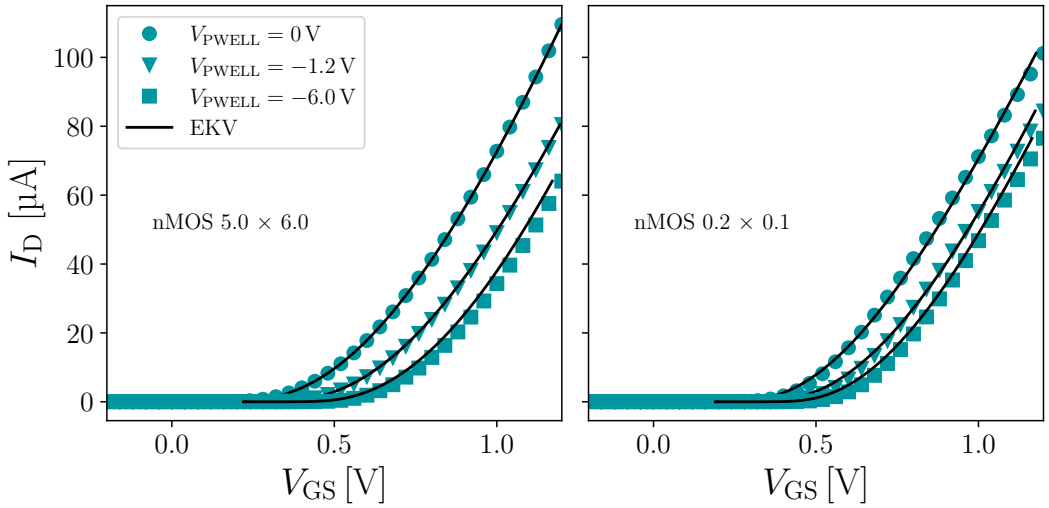

Figure 4.14: $I_D(V_{GS})$ of a maximum size 5 µm x 6 µm device (left) and a minimum size 0.2 µm x 0.1 µm device (right) measured at $V_{PWELL} = 0\,V$ (circles), at $V_{PWELL} = -1.2\,V$ (triangles) and at $V_{PWELL} = -6\,V$ (squares). Black curves correspond to the EKV fitting.

The threshold voltage remains the parameter most significantly affected by the bulk effect. A high bulk bias voltage attracts more charge to the bulk of the device, which depletes the sensor at the surface of the device, making it more challenging for electrons to drift from the source to the drain. However, the remaining parameters do not exhibit substantial variations which eases the modeling of nMOS transistors with at different back-gate voltages. It is also crucial to note that there is a slight discrepancy between the threshold voltage derived from the measurements using the technique described in [66], which was previously used in Section 3.5 to extract the threshold voltage variation during irradiation and TID, and the one modeled by the sEKV. This inconsistency comes from the technique employed for extraction.

Table 4.3: Extracted values of $V_{TH}, \lambda_c, I_{spec}, n$ from the measurements and EKV fitting showed at Figure 4.14 for $V_{PWELL} = 0, -1.2\,V, -6\,V$.

Size [µm]	V_{PWELL} [V]	V_{TH} [mV]	I_{spec} [µA]	n	λ_c
	0	250.08	0.67	1.18	-
5.0/6.0	-1.2	371.99	0.56	1.12	-
	-6	473.46	0.49	1.03	-
	0	294.86	0.55	0.96	0.10
0.2/0.1	-1.2	371.66	0.39	0.87	0.07
	-6	444.03	0.49	0.91	0.08

4.6 Summary

In this chapter, we conducted a modeling-based analysis of the radiation and back-gate effects on TPSCo65 nm. Beginning with the SEKV-E [9] , we developed our Python-based sEKV parameter extractor [8]. This routine utilizes measured or simulated transfer characteristics to extract the main sEKV parameters. The update that distinguishes this code from the SEKV-E is the ability to perform the extraction for a wide range of irradiation steps.

The simplified EKV MOSFET model and the proposed extractor were utilized to investigate TID effects on analog performance. Both large and small signal parameters were extracted and matched with measurements across the entire range of device operation. The main four model parameters (threshold voltage, slope factor, specific current, and velocity of saturation parameter) were extracted at every irradiation step up to 1 Grad. The influence of TID effects, such as RINCE and RISCE, on these design parameters was confirmed and discussed.

Subsequently, the normalized transconductance efficiency was calculated from pre- and post-irradiation measurements, aligning well with the curves of the simplified EKV MOSFET model. Consequently, we concluded that although TID influences the design parameters of 65 nm MOSFETs, normalization effectively removes the effects of TID from the transconductance efficiency. Therefore, the sEKV model can be employed for radiation-tolerant circuit design.

Additionally, we presented a study on the performance degradation of nMOS transistors under negative back-gate biases. Measurements of nMOS transistors with a p-well biasing of $-6\,\mathrm{V}$ showed an increase in the nominal V_{TH} of approximately 260 mV. For bulk biases down to $-1.2\,\mathrm{V}$, the measured V_{TH} matched the simulation. However, this was not the case for a bias of $-6\,\mathrm{V}$, where the error concerning the BSIM model reached approximately 160 mV. Nevertheless, the sEKV model accurately captured the threshold voltage shift induced by the body effect. However a more detailed study of performance degradation due to the body effect and its correlation with transistor sizing would be beneficial for designers.

In conclusion, this chapter demonstrated how the sEKV can be used to model transistor performance over a wide range of operating points using the IC design approach. This, in combination with the presented code or the sEKV-E, makes it a powerful tool for analog designers, as we will see in the next chapter.

5 Implementation of a Novel Low-Power and Low-Noise Front-End

On Chapter 2 we introduced two recent chip prototype developments using the the TPSCo 65 nm technology: the MOSS and the H2M. The MOSS prototype imposes strict constraints on power consumption to ensure scalability to wafer-level dimensions in stitched CMOS sensors. This necessitates a design that is robust against voltage drop and power supply variations. Another constraint is the low noise for the front-end, crucial for amplifying faint signals generated in the small depletion region of the sensor.

Chapter 3 and Chapter 4 layed out a overview and preliminary characterization of this monolithic technology. Utilizing the information from these chapters, we will design a low-power, low-noise front-end that combines the low-power requirements of the MOSS front-end with a similar transconductance topology used in the H2M front-end. This transconductance topology is advantageous for its linearity and straightforward mathematical model. Using the sEKV model and the IC design approach [86], Section 5.2 will delve into the fundamental limits on the design of low-power and low-noise front-ends. Section 5.3 will concentrate on the design procedure, presenting the steps to define different elements forming the front-end (charge sensitive amplifier, feedback network, discriminator, and feedback capacitance) based on specifications such as gain, the possibility to adjust the baseline, system speed, or stability criteria, among others. This design will include a 3-bit DAC for threshold equalization.

Section 5.4 deals with the schematic simulations, while Section 5.5 will cover the extracted layout simulations, where the influence of parasitic capacitances at the input and output nodes of the system will play a crucial role in the expected performance of the FE, influencing transient performance and the detection range. To conclude, Section 5.6 will offer a comparison of this topology with the two presented in Chapter 2, reflecting on the advantages and disadvantages of these different topologies and the consequences of achieving such low power consumption. In general terms, the design developed in this chapter will demonstrate how this type of front-end, based on a transconductance

amplifier, can be used in monolithic applications that require low power consumption and where the focus is on detecting and amplifying MIP signals.

5.1 Specifications and Objectives

One of the advantages of modern CMOS technologies becomes a limitation in the design; this is the low power consumption. These types of technologies, with a low supply voltage (that is 1.2 V for this node), tend to work in weak inversion or sub-threshold region. However, in weak inversion, the transconductance efficiency reaches its maximum at the cost of losing speed.

For this design, we offer an alternative to the front-ends implemented in the H2M and the MOSS chip, focusing not only on low noise and low power but also on robustness, taking into account power drops and power supply variations. The design is based on a transconductance amplifier (similar to the one used in the H2M) to take advantage of its linearity and feasible mathematical modeling, but with a reduction in the current at the input transistor.

Table 5.1: MOSS front-end specifications at the time of the ER1 submission for an input capacitance of 5 fF [50].

Specification	Value
Gain	$0.5\,\mathrm{mV/e^-}$
Nominal threshold	$100\,\mathrm{e^-}$
Threshold mismatch	$16\,\mathrm{e^-rms}$
ENC	$17\,\mathrm{e^-rms}$
Peaking time	1.5 µs
Power consumption	36 nW

Our objective is to match the simulation values from the MOSS front-end at the time of the Engineering Run 1 (ER1) submission [50] which can be found in Table 5.1. Nonetheless, we will always prioritize stability and robustness over power consumption, and we will take into account the fundamental limitations on these type of topologies.

5.2 Study of Fundamental Limits on the Design of Low-Power and Low-Noise Front-Ends

As we saw in Chapter 2, all the parameters in the processing chain play an important role in noise and transient performance. As a starting point for our study, we will use [13]. This work describes the optimization of the front-end readout electronics for high-granularity hybrid pixel detectors, using the Timepix 4 [87] front-end as an example.

The theoretical study aims to minimize noise and jitter. The front-end is modeled using the EKV model and follows a design procedure inspired by [78, 83, 86, 88, 89].

Table 5.2: Prefixed parameters used during the modelling.

Parameter	Value
Pixel Side	15 µm
Input Charge	100 e^-
Bias Input Transistor	20 nA
Detector Capacitance	1 fF
Leakage Current	100 pA

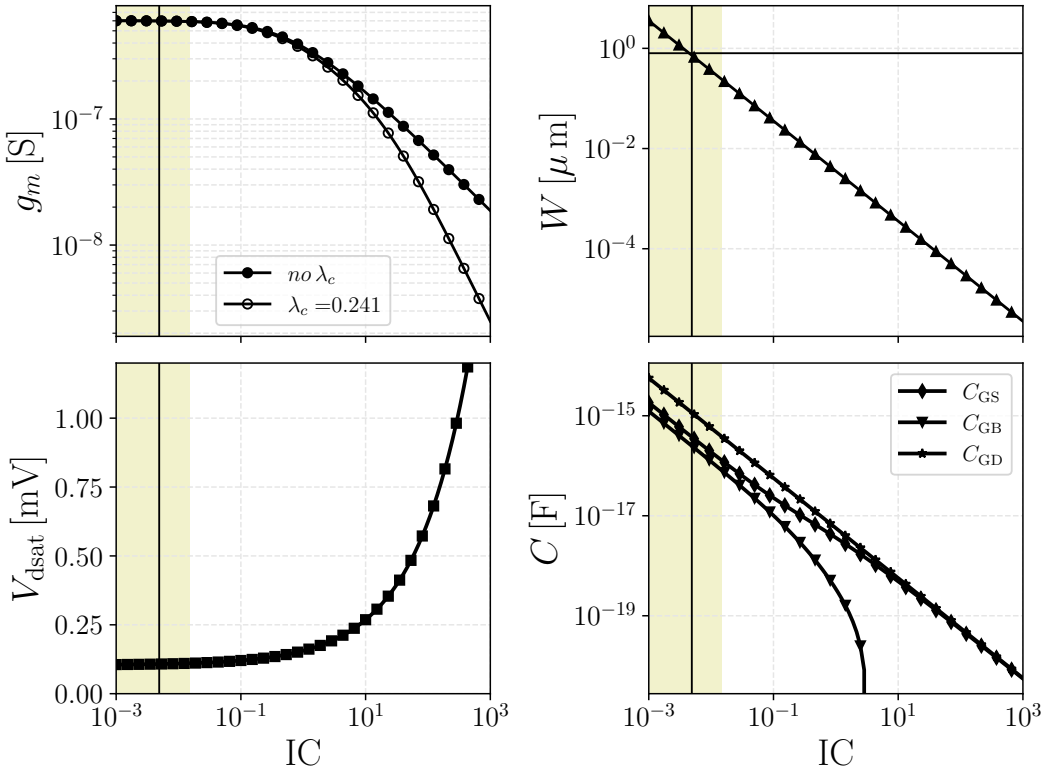

Figure 5.1: Transconductance (g_{m}), width (W), saturation voltage (V_{dsat}), or the gate capacitance values ($C_{\mathrm{GS}}, C_{\mathrm{GB}}, C_{\mathrm{GD}}$) versus the IC. The yellow shaded part is the area of interest as this is the range of widths available in the technology. The horizontal and vertical black lines mark the operating points of the selected width of 800 nm.

However, the procedure will be adapted to our monolithic design. In our case, we will use the EKV extractor presented in Section 4.2 to extract the main EKV parameters of this technology. The parameters will be used afterward to calculate the dependency of the main noise sources in our circuit (derived in Subsection 2.4.4) and the jitter on the IC and, therefore, the size of the input transistor. For these calculations, we will need to compute the gate capacitances using the formulas discussed in Subsection 4.1.2, which

likewise have a dependency on the inversion coefficient. Certain noise parameters used in our calculations, such as Γ, will have the same value as the ones used in the reference paper [87], as they are also extracted from a 65 nm technology. In Section 2.1.4, we covered how certain parameters such as the system capacitances (feedback, parasitic, and detector), as well as the feedback element or the leakage current, can influence the noise. In this study, we will fix certain parameters to specific values to evaluate the expected performance of our design. These fixed values are listed in Table 5.2, with the biasing current of the input transistor being particularly significant. Otherwise, the calculations will follow the same path as [13].

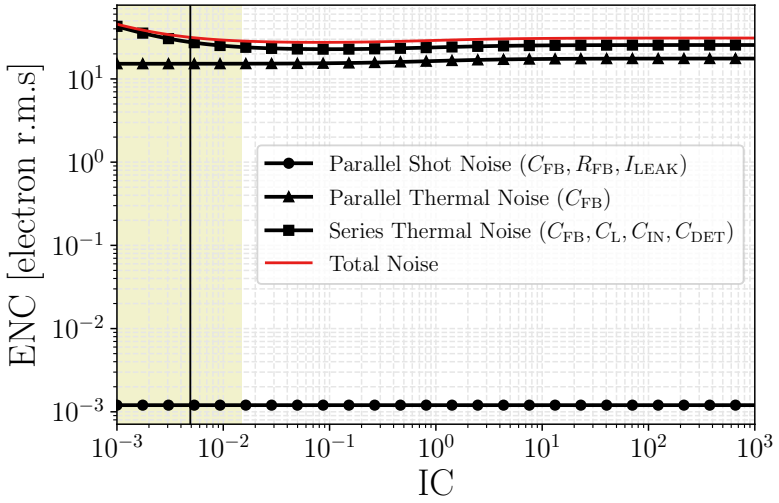

Figure 5.2: Parallel shot noise, parallel thermal noise and series thermal noise, together with the total noise contribution versus IC.

Figure 5.1 summarizes some of the limitations of the transconductance (g_m), width (W), saturation voltage (V_{dsat}), and the gate capacitances (C_{GS}, C_{GB}, C_{GD}), and its dependency on IC, where

$$V_{dsat} = U_T \left(2\sqrt{IC} + 4\right). \tag{5.1}$$

At the top left we can see how, assuming a low bias current, will operate the transistor in weak inversion, maximizing its transconductance efficiency. The picture at the top right depicts the relation between the width and the IC. The yellow shaded area is our area of interest as this is the range of widths available in the technology. The horizontal black line crosses at the decided width of 800 nm. This is a trade-off between radiation tolerance and minimization of the gate capacitances and noise. The saturation voltage will be at its minimum, around 0.110 V. However, in weak inversion, the gate capacitances read a maximum of few fF. This is disadvantageous in terms of noise as shown by previously derived expression

$$\text{ENC}_{\text{Series Thermal Noise}} = \sqrt{\frac{C_{\text{FB}}(C_{\text{det}} + C_{\text{in}}(\text{IC}) + C_{\text{FB}})^2 4kT\Gamma}{(C_{\text{det}}C_{\text{FB}} + C_{\text{FB}}C_{\text{in}}(\text{IC}) + C_{\text{det}}C_L + C_{\text{FB}}C_L + C_{\text{in}}(\text{IC})C_L)q^2}}, \tag{5.2}$$

where C_{in} is the sum of the gate capacitances ($C_{\text{GS}}, C_{\text{GB}}, C_{\text{GD}}$). This correspondence is visible in Figure 5.2 where the parallel shot noise, parallel thermal noise and series thermal noise, together with the total noise contribution versus IC are shown. Assuming the values in Table 5.2, the series thermal noise which sources from the input transistor is the largest contributor, followed by the parallel thermal noise which is influenced by the feedback capacitance. The total noise is also represented and, at the selected operating point, it is estimated at $23\,\text{e}^-$.

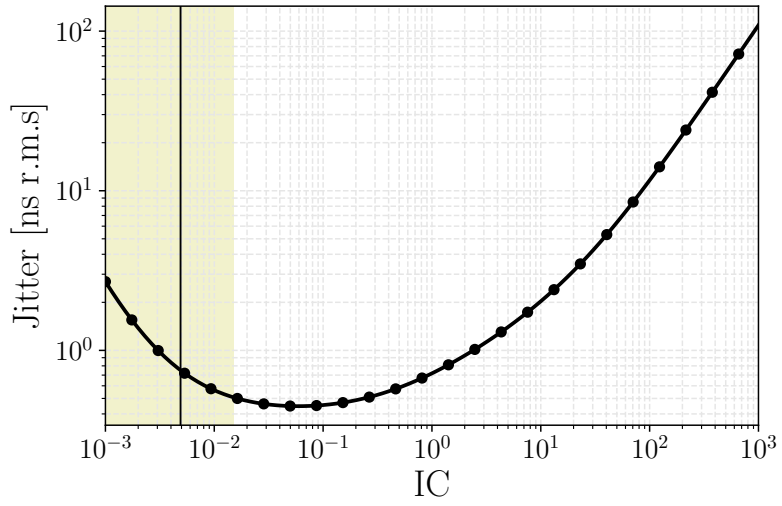

Figure 5.3: Jitter versus the inversion coefficient. In the area of interest, the jitter reads below 10 ns. The jitter will be limited by the noise and the feedback capacitance value, and will decrease as the input charge increases.

Regarding the transient performance, Figure 5.3 displays the jitter versus the inversion coefficient. In our area of interest, the jitter is below 10 ns. The jitter is calculated according to:

$$\text{Jitter} = \frac{q\,\text{ENC}_{\text{Total}}}{\frac{dv_{\text{out}}}{dt}\,C_{\text{FB}}} \tag{5.3}$$

where $\frac{dv_{\text{out}}}{dt}$ is the slope, dependent on the feedback capacitance and the input charge. This implies that the jitter will be limited by the noise and the feedback capacitance value, and will decrease as the input charge increases.

In conclusion, to boost the amplification of low energy signals the feedback capacitance must have a small value. At the same time, we have the low-power requirement to ease power dissipation. These two constraints will not enhance transient performance but will minimize noise levels. However, if we increase the bias current, the transconductance will increase while the remaining capacitances in the circuit will remain around fF. At the same time, the operating point would move towards moderate inversion for the same width. Therefore, by increasing power consumption, we could improve the speed while maintaining the same noise level. It is also important to highlight one of the drawbacks of this transconductance topology, which is the feedback that introduces a parallel thermal noise source. However, this noise source depends on the feedback capacitance (2.21). Therefore, by maintaining a low value for the capacitance, we can keep the noise within specifications.

5.3 Design Procedure

5.3.1 Charge Sensitive Amplifier

The Charge Sensitive Amplifier (CSA), introduced in Subsection 2.4.1, is responsible for amplifying and transforming the current pulse generated by the collection electrode into a voltage pulse. It is commonly referenced that the CSA is based on a Common Source (CS) amplifier [1, 25]. As explained in Subsection 2.4.2, in these types of designs, it is important to keep the gain of the CSA high so that the amplitude of the output pulse is proportional to the ratio between the input charge and the feedback capacitance, removing the influence of the sensor capacitance. In this case, we will aim for a gain higher than 40 dB , without excessive boosting, to keep the power budget low (i.e., avoiding the need to add more gain-boosting stages). Based on the CS, we simulated four different types of single-ended amplifiers with different gain-boosting techniques: cascoded CS, CS with regulated cascode, CS with folded cascode, and differential amplifier with folded cascode [1, 90, 91]. These are presented in the top left, top right, bottom left, and bottom right of Figure 5.4, respectively. For the simulation, we assumed ideal voltage and current sources, an ideal feedback capacitance of 0.5 fF (choice explained in Subsection 5.3.5), and an ideal feedback resistance high enough to separate the rise and fall time constants (2.10).

The extracted parameters, presented in Table 5.3, are:

- **Gain:** refers to the ratio of the output signal amplitude to the input signal amplitude. It will quantify the amplification of the topology.
- **Power Supply Rejection Ratio (PSRR):** indicates the ability of our design to withstand fluctuations in the power supply.

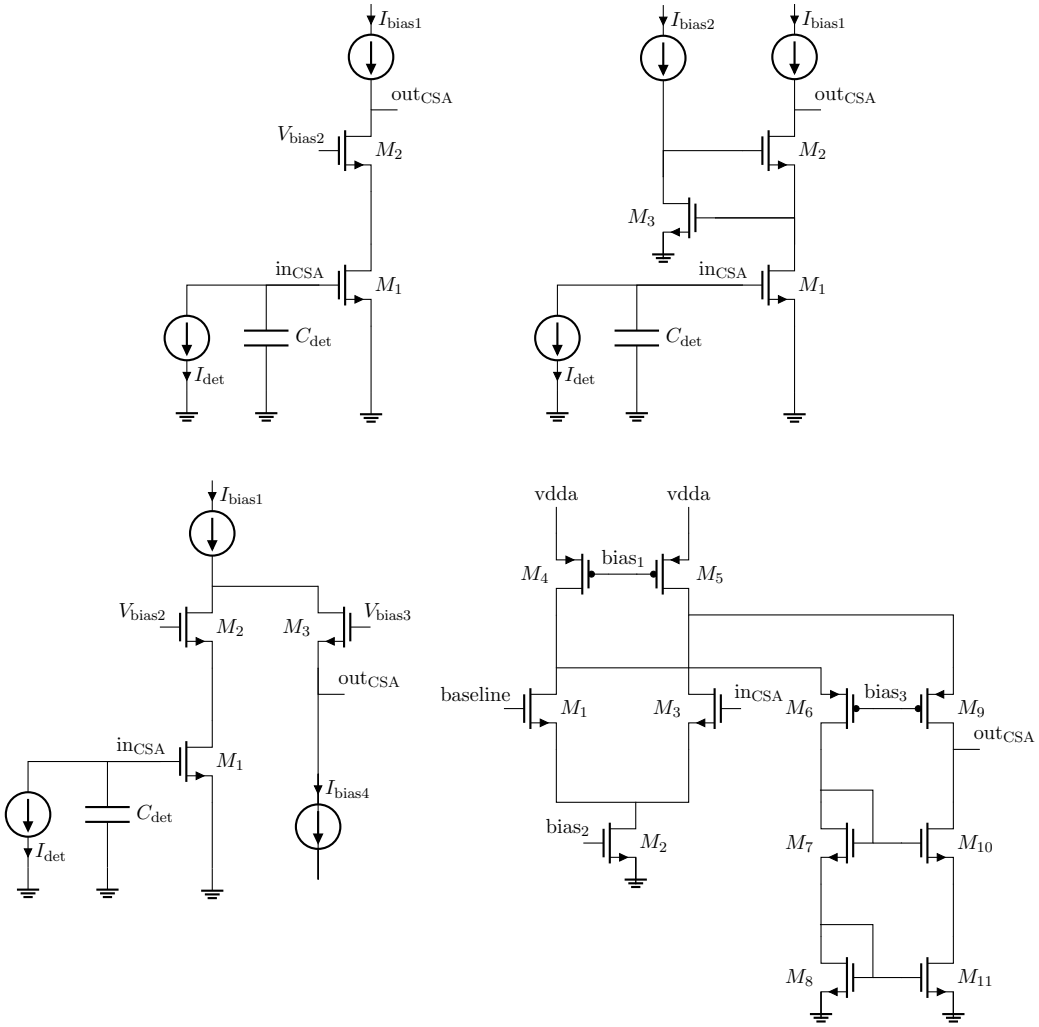

Figure 5.4: Single-Ended CSA Topologies: cascoded common source (up left), common source with regulated cascode (up right), common source with folded cascode (bottom left), and differential amplifier with folded cascode (bottom right).

- **Phase Margin (ϕ_m):** is a parameter used in control system analysis. It represents the difference between the phase of the open-loop system at the frequency where the gain 0 dB and 180 degrees. A higher phase margin indicates greater stability in a feedback system.
- **3 dB Frequency (f_{3dB}):** is the frequency at which the output signal is attenuated 3 dB (half the power) compared to the maximum value. It is often used to define the bandwidth of a system.
- **Unity Gain Bandwidth (f_T):** is the frequency at which the open-loop gain of an amplifier drops to 0 dB.
- **Number of Biasing Lines:** refers to the amount of separate biasing paths used to establish the appropriate operating point (bias point) for transistors in a circuit.

Table 5.3: Topology comparison of three single-ended charge sensitive amplifier topologies: cascoded CS (A), CS with regulated cascode (B), CS with folded cascode (C), and (D) differential amplifier with folded cascode. The simulated parameters are: gain, Power Supply Rejection Ratio (PSRR), phase margin (ϕ_m), the 3 dB frequency (f_{3dB}), unity gain bandwidth (f_T) and number of biasing lines.

Topology	Gain (dB)	PSRR	ϕ_m (°)	f_{3dB} (KHz)	f_T (MHz)	Biasing Lines
A	40.8	-51.6	92.1	132.8	15.3	2
B	49.9	-52	85.6	45.1	13.3	2
C	45.4	-48.6	73.9	127.6	12.7	4
D	54.3	-49	72.2	15.2	5.3	3

Looking at Table 5.3, we see that all the topologies have sufficient gain for our purpose, but the introduction of the regulated cascode and the folded cascode is noticeable in the gain. The regulated cascode topology has a lower bandwidth, which can make the matching of R_{FB} difficult and would slow down the response of our system. The number of biasing lines is the same for the simple CS and the regulated cascode, but doubles for the folded cascode, increasing the complexity of power distribution across the pixel matrix. The PSRR is similar for all of them. Therefore, the best choice for our design would be a cascoded common source, which, being single-ended, would also account for lower noise.

However, as we will see in Subsection 5.3.2, due to the low feedback capacitance of our design, we encountered some challenges using the Krummenacher feedback [92], which includes baseline adjustment. Therefore, we needed to use an amplifier that would allow us to set the baseline. The differential amplifier shown at the bottom right of Figure 5.4, which includes a folded cascode stage for gain enhancement [93], achieves a gain exceeding 40 dB with the addition of only one more biasing line. Table 5.3 includes the simulation results of this topology while Figure 5.5 shows the gain of the amplifier. One clear disadvantage is the lower bandwidth, which will slow down the system, making it difficult to match the feedback network. The results obtained with this CSA will be presented in Section 5.4.

5.3.2 Feedback Network

A crucial component of the front-end is the feedback system. While the CSA merely requires tuning to achieve the necessary gain at a defined power consumption, the feedback system must synchronize with the speed of the CSA, which has limited bandwidth. It must ensure stability, enable the retuning of the falling time, and withstand the increase in leakage current from the sensor. We explored three different topologies [25]: Krummenacher feedback, current mirror feedback, and continuous reset.

Fixing the CSA current at 20 nA, the first feedback we tested was the Krummenacher, as it is the most common used because of its leakage current compensation network.

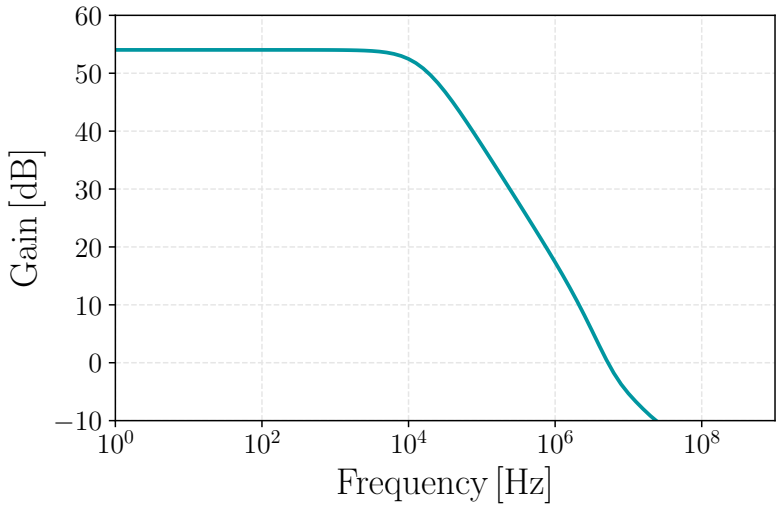

Figure 5.5: Gain of the differential CSA.

Depicted on the left in Figure 5.6, this feedback discharges the feedback capacitance, unbalancing the differential pair formed by M_{1a} and M_{1b}. After signal integration, the baseline is recovered by the low-frequency feedback loop, which adjusts the output voltage of the CSA to match the reference voltage (V_{REF}). Transistor M_2, together with the capacitance C_{leak}, form the low-frequency leakage current compensation network [92]. However, due to the small bandwidth of the CSA, the current on the feedback has to decrease considerably (to the pA range) to match the speed of the feedback to the CSA.

Additionally, the stability issue that comes with this feedback becomes apparent with the small value of C_{FB}. Solving the circuit formed by the amplifier and the Krummenacher feedback, we obtain a fourth order transfer function

$$\text{H}(s) = \frac{A_0(s - z_0)(s - z_1)}{(s - p_0)(\text{s} - p_1)(s - p_2)(s - p_3)} \tag{5.4}$$

The parasitic capacitance (in red in the schematic) at the bottom node, created by the transistors forming the differential pair (M_{1a}, M_{1b}), introduces poles p_2 and p_3. Depending on the capacitance, these poles may become complex conjugate poles, causing an undershoot in the output signal. There are two possible solutions to this problem: (1) decreasing the width of the transistors in the differential pair to reduce their capacitance; (2) increasing the feedback capacitance so that $C_{\text{FB}} > 2C_{\text{parasitic}}$ [94, 95].

Figure 5.7 shows the result of these two solutions applied when the CSA biasing current is 20 nA, the Krummenacher biasing current is 20 pA and the feedback capacitance is 0.5 fF. The simulation on the right corresponds to when C_{FB} is fixed, and on the left, when the width is fixed. To enable the first solution, the transistor width must

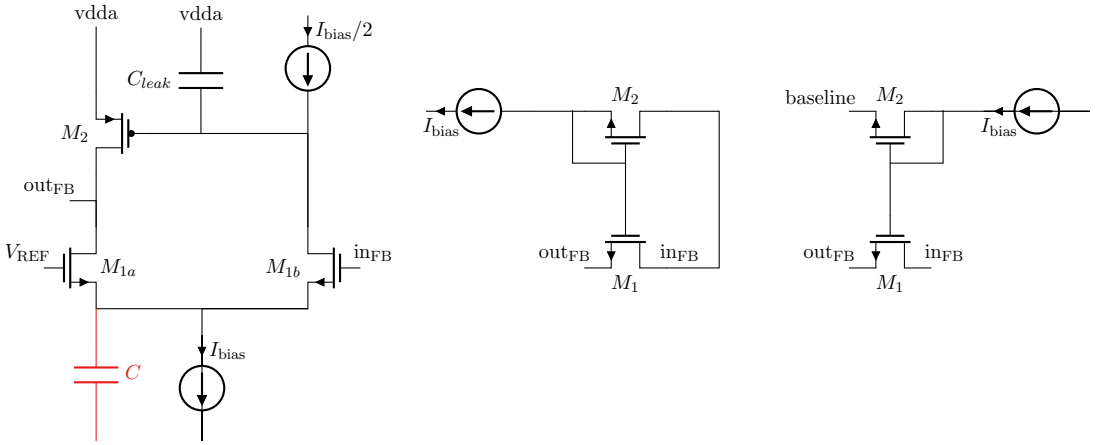

Figure 5.6: Explored feedback topologies [25]: Krummenacher feedback (left), current mirror feedback (middle), and continuous reset (right). The red colored component is the parasitic capacitance created by the differential pair.

be reduced to the minimum allowed by the technology, which compromises radiation robustness (Section 3.6). On the other hand, increasing the feedback capacitance value would decrease amplification of small charge signals (Subsection 2.4.2), which is against the main purpose of this design. Even though the first solution could be feasible, the feedback capacitance of 0.5 fF would still be smaller than $2C_{\text{parasitic}}$. Therefore, we had to discard this feedback.

The current mirror feedback is illustrated in the center of Figure 5.6. In the absence of a signal, the input voltage closely matches the output voltage. This small voltage difference, of a few millivolts, corresponds to the saturation voltage of M_2, maintaining it within the linear region. Although the feedback resistor is small, it ensures baseline stability. Upon the arrival of a signal, the output voltage increases, pushing M_2 into the saturation region. The replica of the bias current discharges the capacitor, and adjusting this biasing current alters the falling time. This topology can withstand DC fluctuations induced by currents larger than the biasing one, and it was initially introduced in [96, 97], where a small recovery time and, consequently, a small feedback resistor were essential. Nevertheless, during the tuning of this feedback, this was not the case. The required biasing current had to be around 1 pA, falling within the leakage current range of this technology, compromising the robustness of this feedback to DC fluctuations.

The feedback depicted on the right in Figure 5.6, is a continuous reset feedback [98–100]. It is based on a thick-gate-oxide (6.5 nm) nMOS transistor with the source connected to the input and the drain connected to the output of the amplifier. The gate is biased with a replica circuit whose source is connected to the baseline signal and the drain to an input current. This configuration keeps the baseline fixed against variations, increasing the robustness of the system. This topology is based on [101–103]. To achieve the desired output, this current would have to be 100 pA, which is on the same order of magnitude

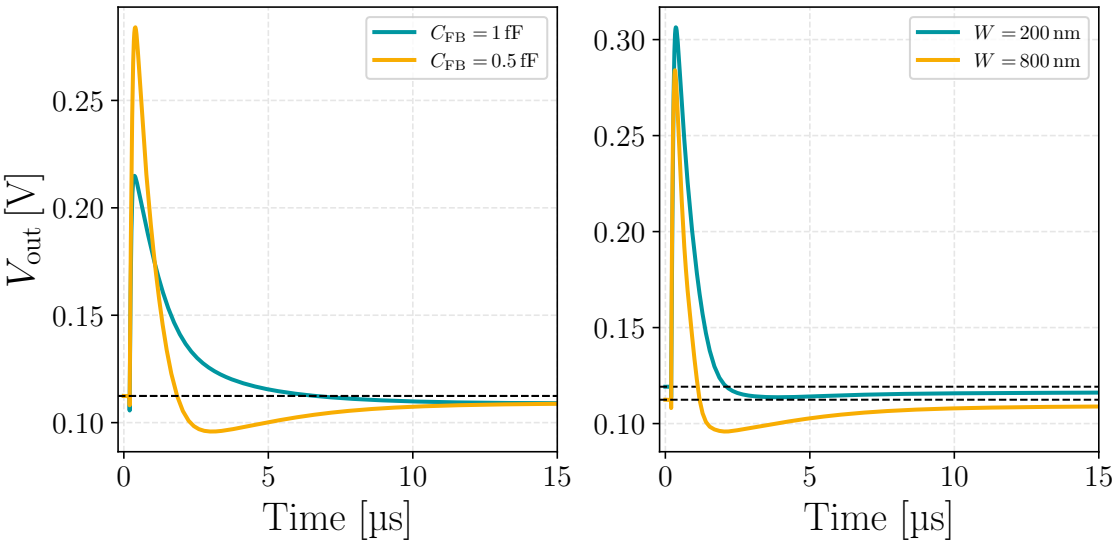

Figure 5.7: Result of the two possible solutions to reduce the undershoot introduced by the Krummenacher feedback, applied when the CSA biasing current is 20 nA, the Krummenacher biasing current is 20 pA and the feedback capacitance is 0.5 fF. On the left, keeping the width fixed and changing the feedback capacitance. On the right, fixing C_{FB} and varying the width.

as the leakage current of this technology. Therefore, the transistor is replicated 100 times to maintain the input current within a reliable range (nA). The decision to use the thick gate oxide was due to the negative V_{GS} on the feedback transistor if a Low-Voltage Threshold (LVt) transistor were used, which means that the transistor would be in the off state. The results obtained with the feedback will be presented in Section 5.4.

5.3.3 Discriminator

Recent comparison can be found in [104]. However, considering the low-power budget and aiming to minimize the area, we opted for a two-stage CMOS Operational Transconductance Amplifier (OTA), similar to a Miller OTA. It provides good resolution at lower gain because of the two gain stages. Additionally, the close proximity of the two logic levels reduces the constraint on the gain, leveraging the transconductance achievable with 10 nA on the input transistors [1].

The first stage incorporates an operational amplifier with an active load. It compares the output of the CSA with a threshold voltage (V_{th}). When the input signal matches the threshold voltage, M_{1a} and M_{1b} drive the same current. If the input signal is lower than the threshold (no hit), M_{1b} draws more current. When the signal surpasses the threshold (hit condition), a positive pulse reaches the gate of M_{1a}, causing it to draw more current. Consequently, M_{1b} drives less current to maintain balance.

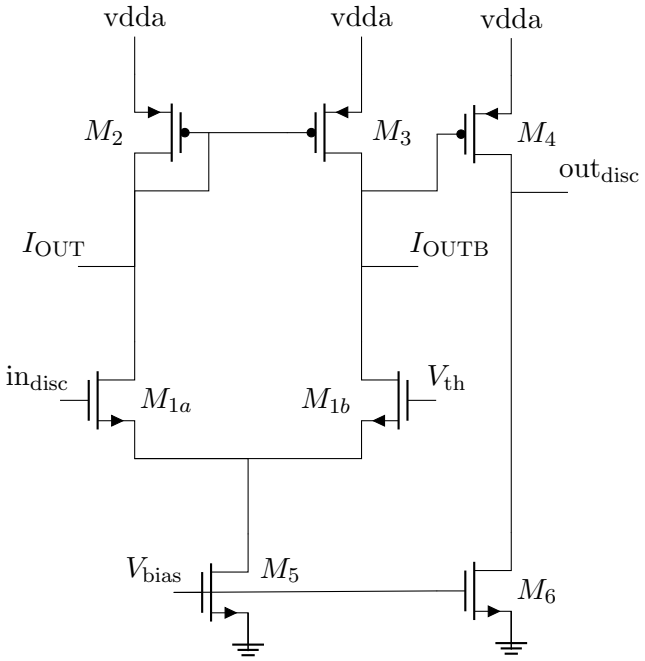

Figure 5.8: Discriminator, based on a two-stage CMOS OTA.

The second stage translates the current signal from the first stage into a digital signal. Transistor M_4 is crucial in this stage. In the absence of a hit, M_4 experiences a decrease in its gate voltage, setting the output voltage to vdda. However, when there is a hit, M_4 drives less current, causing the output voltage to drop to zero.

This topology is also used in [105–107], where all the designs aim for low power consumption. The results obtained with this discriminator will be presented in Section 5.4.

5.3.4 3-bit Threshold DAC

During manufacturing, analog circuits will suffer variations due to post-processing fluctuations. Using certain layout techniques can help mitigate these effects (e.g. aligning transistors in the same direction, utilizing consistent metal coverage, or maintaining uniform finger geometry [108]. However, even using some of these techniques in our presented schematic and layout design phases there will be variations on the baseline level (offset), some of them also induced by dopant fluctuations or edge roughness [109]. The offset causes a pixel-to-pixel threshold mismatch which can affect time-over-threshold measurements. The threshold dispersion follows a normal Gaussian distribution. After threshold equalization, it transforms into a uniform one, where the width is equal to the tuning DAC step value [110]:

$$\sigma_{eq} = \frac{I_{\text{LSB}}}{\sqrt{12}} \tag{5.5}$$

The step value is the Least Significant Bit (LSB) current of the DAC. The pixel detector's minimum detectable energy is influenced by random noise from the electronics and threshold dispersion after correction. The Minimum Detectable Charge (MDC) can be approximated by:

$$Q_{\text{min}} = 6\sqrt{\text{ENC}^2 + \sigma_{eq}^2} \tag{5.6}$$

In this equation, ENC represents the electronic noise of the analog front-end, while σ_{eq} signifies the standard deviation of the uniform distribution. The inclusion of the factor 6 ensures that 99.9% [111] of the pixels in the matrix are free from noise. Calibration DACs can be used to address pixel-to-pixel threshold mismatches. After calculations, a 3-bit binary weighted DAC is sufficient for the presented design. Its transfer function is depicted in Figure 5.9. This figure shows the mean and standard deviation of the difference between the two output currents, obtained after 400 Monte Carlo runs.

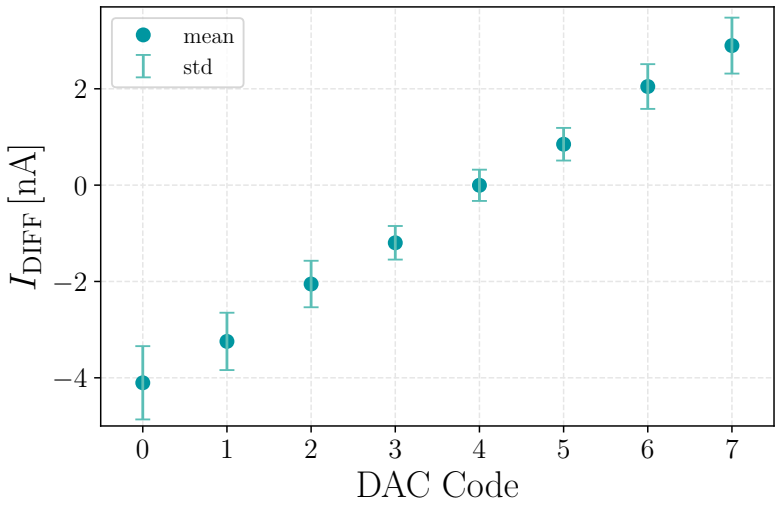

Figure 5.9: Mean and standard deviation of the difference (I_{DIFF}) between the positive output current (I_{OUT}) and the negative output current (I_{OUTB}), obtained after 400 Monte Carlo runs.

Figure 5.10 illustrates the configuration of a 3-bit DAC. Nodes I_{OUT} and I_{OUTB} are connected to the respective nodes of the discriminator in Figure 5.8. The injected current induces an imbalance in the discriminator, consequently modifying its effective threshold. For example, if the baseline level is below the threshold, transistor M_{1b} in Figure 5.8 will drive a higher current than M_{1a}. To mitigate the current mismatch between the

branches of the differential pair, a small current is introduced into the I_{OUTB} node while simultaneously drawing an equivalent amount from the I_{OUT} node.

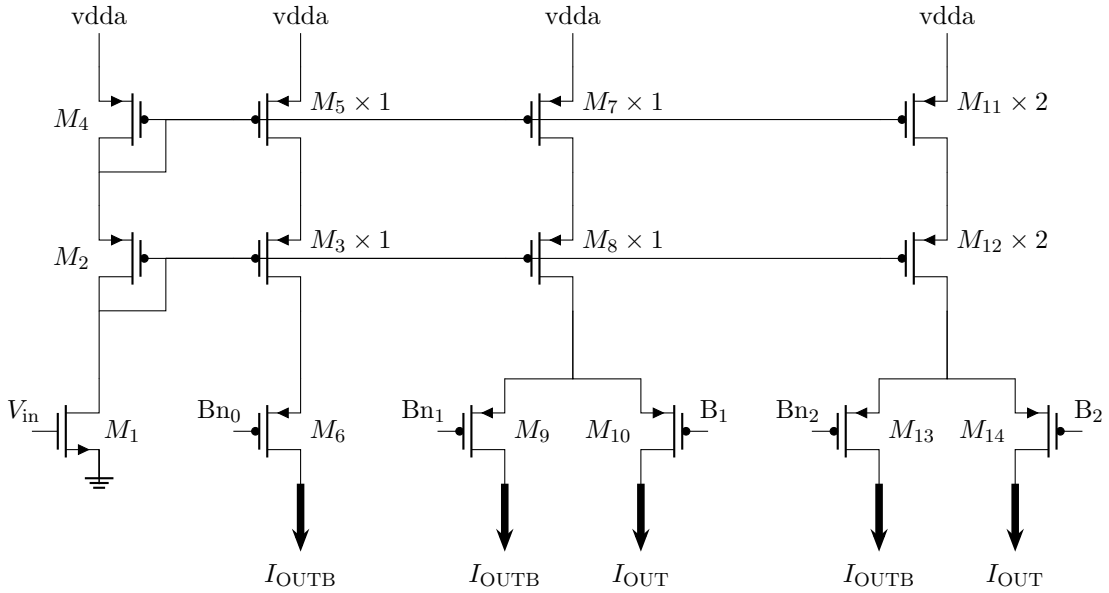

Figure 5.10: Schematic 3-bit DAC.

The diode-connected transistors on the left of the circuit will mirror I_{LSB} to the current branches on the right within the 3-bit DAC. This current array deviates from a conventional 3-bit binary structure, with the Most Significant Bit (MSB) branch having fewer components, occupying less area of the pixel. Additionally, the same current factor scales the first two branches. The pMOS switches that control these branches are configured by the digital logic of the pixel using a 3-bit digital code. This arrangement produces two complementary output currents, I_{OUT} and I_{OUTB}, as shown in Table 5.4. The difference in output currents ranges from $3I_{\mathrm{LSB}}$ to $-4I_{\mathrm{LSB}}$, with an I_{LSB} step.

Table 5.4: Complementary output currents of the DAC, I_{OUT} and I_{OUTB}, with its difference I_{DIFF} and corresponding DAC code.

B<2:0>	I_{OUT}	I_{OUTB}	I_{DIFF}
000	$3 \cdot I_{\mathrm{LSB}}$	0	$3 \cdot I_{\mathrm{LSB}}$
001	$3 \cdot I_{\mathrm{LSB}}$	I_{LSB}	$2 \cdot I_{\mathrm{LSB}}$
010	$2 \cdot I_{\mathrm{LSB}}$	I_{LSB}	I_{LSB}
011	$2 \cdot I_{\mathrm{LSB}}$	$2 \cdot I_{\mathrm{LSB}}$	0
100	I_{LSB}	$2 \cdot I_{\mathrm{LSB}}$	$-I_{\mathrm{LSB}}$
101	I_{LSB}	$3 \cdot I_{\mathrm{LSB}}$	$-2 \cdot I_{\mathrm{LSB}}$
110	0	$3 \cdot I_{\mathrm{LSB}}$	$-3 \cdot I_{\mathrm{LSB}}$
111	0	$4 \cdot I_{\mathrm{LSB}}$	$-4 \cdot I_{\mathrm{LSB}}$

5.3.5 Feedback Capacitance

As we have previously seen, the feedback capacitance has an important influence on noise, gain, and rise time. Monolithic active pixel sensors are characterized by a low detector capacitance (2 fF for this node) [39]. This eases the detection and amplification of MIP signals. To maintain the low power consumption requirement and leverage the advantages of the low detector capacitance, the feedback capacitance had to be tuned accordingly. Figure 5.11 shows the variation of the amplitude and rise time of the CSA's output pulse, and on its baseline noise, with respect to the feedback capacitance. Using this graph, we can find a trade-off between these three parameters. Keeping the feedback capacitance low is advantageous for gain and noise, however, the rise time will increase.

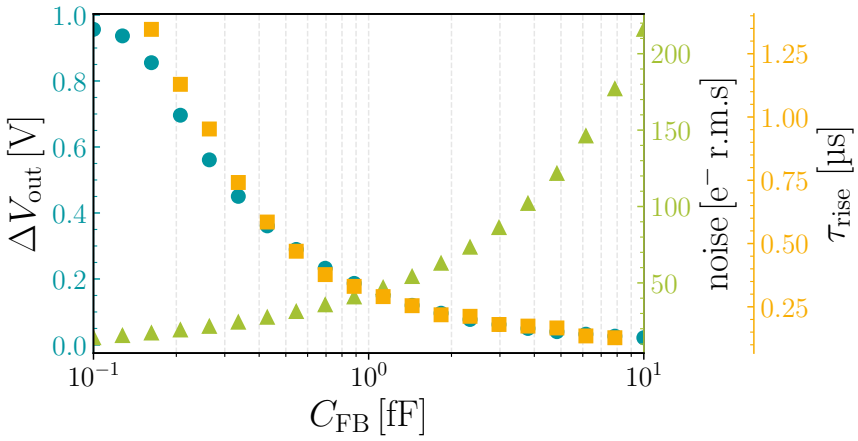

Figure 5.11: Influence of feedback capacitance on the amplitude and rise time of the CSA's output pulse, and on its baseline noise. In order to boost the detection of small input charges and reduce noise, the feedback capacitance will be set to 0.5 fF.

At the same time, from (2.7), we can see that C_{FB} has an influence on stability. Figure 5.12 shows the different CSA outputs that we can get with different C_{FB} values and the same input charge, and the influence of its value on the stability of the system. As expected from the previous plot, the gain amplitude will increase, but going to a too low feedback capacitance value will render the CSA unstable. After several iterations, we kept the value of the feedback capacitance at 0.5 fF, which gave the best trade-off between speed, noise, gain, and stability.

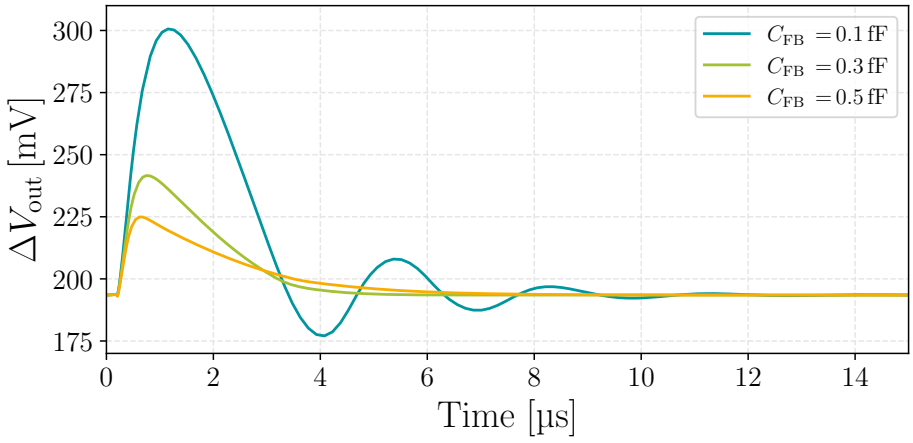

Figure 5.12: Different CSA outputs for different C_{FB} values and the same input charge. The value C_{FB} plays an important role on the stability of the FE.

5.4 Schematic Simulations

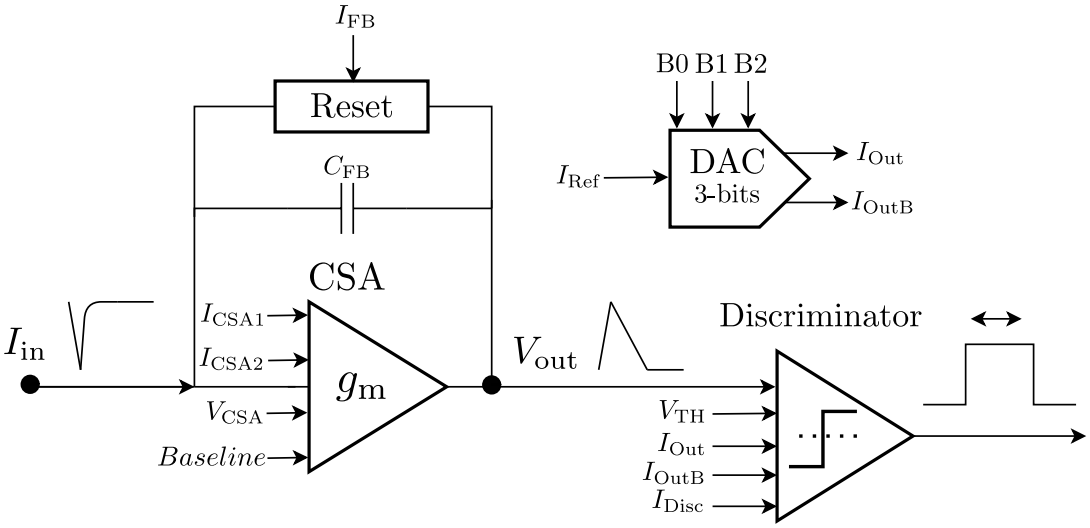

Figure 5.13: Block digram of the implemented FE and the biasing lines of each designed sub-block.

From this point onward, all plots correspond to the low-power mode, where the CSA is biased with 10 nA, the feedback with 1 nA, and the discriminator with 20 nA. The feedback capacitance is 0.5 fF.

Figure 5.13 shows, for reference, the block diagram of the implemented FE and the biasing lines of each designed sub-block. Figure 5.14 showcases the output of transient simulations of the CSA with input pulses ranging from 100 e^- to 3000 e^-. On the left, the output voltage versus time is presented for input charges ranging from 100 e^- to 2000 e^-. The cleanliness of the pulse is similar to the one from the H2M, but without

the undershoot induced by the Krummenacher feedback. The rise time is around 500 ns, and the return to the baseline is well below 30 µs, both measured for 2000 e^-.

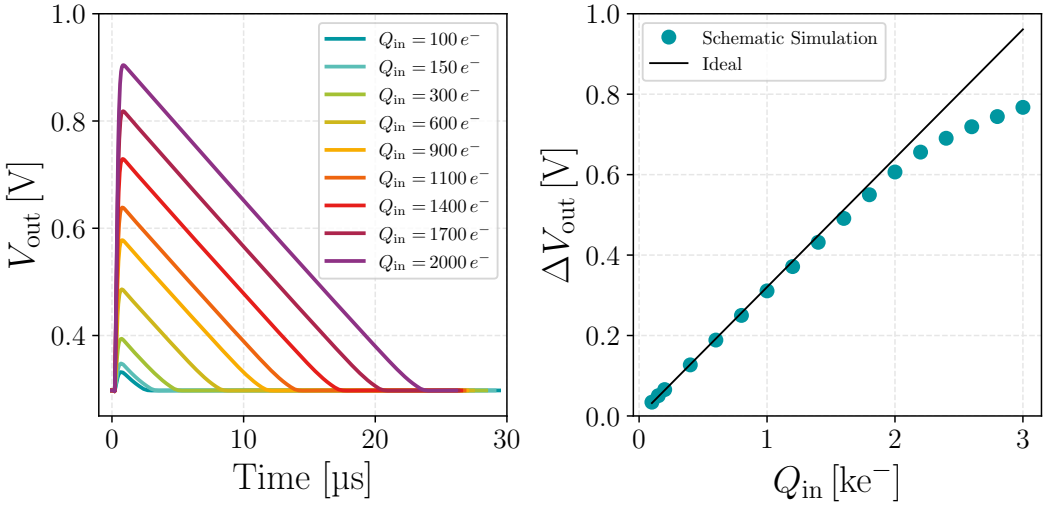

Figure 5.14: Output of a transient simulation of the CSA with input pulses ranging from 100 e^- to 3000 e^-. On the left, the output voltage versus time is presented for input charges ranging from 100 e^- to 2000 e^-. On the right, the maximum amplitude of the output pulse against the input charge.

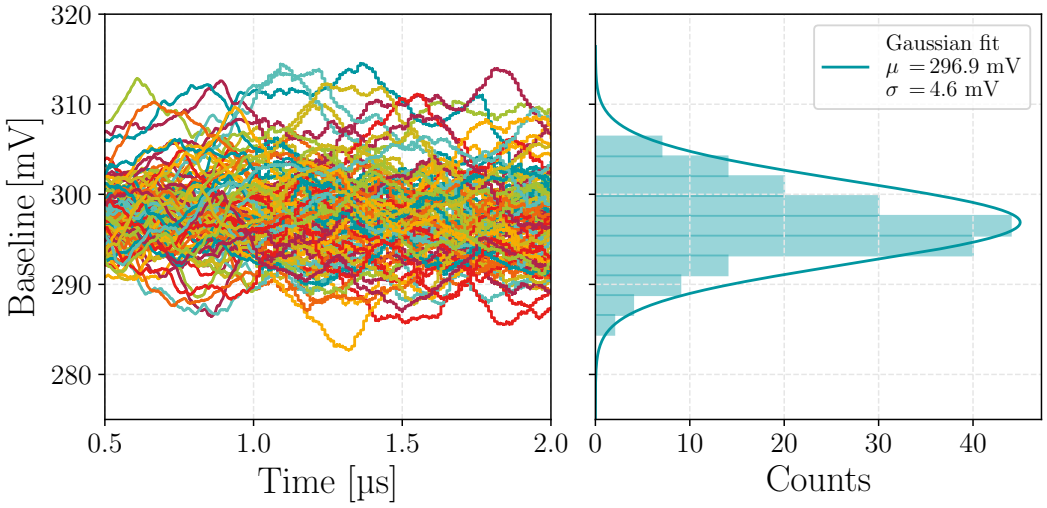

Figure 5.15: Noise measurement of the FE. Blue bars correspond to measured counts while scaning the baseline and the blue line to the Gaussian fit. The standard deviation is the noise of the system which is 5 mV or 17 e^-.

In Figure 5.14, on the right, the maximum amplitude of the output voltage pulse against the input charge is illustrated. Blue dots correspond to simulations, and the black line represents the ideal, calculated as Q_{in}/C_{FB}. The simulated gain is linear up to 2000 e^-, with a slope around 0.3 mV/e^-, showing good agreement with the calculated function.

Figure 5.15 displays the noise simulation of the FE. Blue bars correspond to measured counts while scanning the baseline and the blue line to the Gaussian fit. This is the result of a transient noise simulation, with 400 runs of 30 µs each, without input charge. The CSA's noise has a Gaussian shape where the mean corresponds to the DC baseline level, and the standard deviation to the noise, which in this case is 5 mV or 17 e^-.

Figure 5.16 shows the threshold dispersion of the discriminator. This is the result of a Monte Carlo simulation with 200 runs where at the top is presented the simulated number of counts versus the threshold voltage together with the Gaussian fit, and at the bottom, the discriminator output voltage versus the threshold voltage. The unequalized threshold, which is the standard deviation, is 12 mV or 40 e^-. Using Equation (5.6) and the previously extracted noise gives a minimum detectable charge of 261 e^-. However, the introduction of the 3-bit DAC is already good enough to lower the minimum detectable charge by equalizing the threshold. Figure 5.16 shows the number of events counted while scanning the threshold voltage for a single pixel. To simulate it, we used the noise edge detection method [112]. To reduce the computational time we performed the scan just for the minimum and maximum DAC code. The results show that the DAC is capable of shifting the effective threshold, compensating the pixel to pixel threshold mismatches. The means of the Gaussians are correctly spaced 6σ, and the σ of both corresponds well with the noise of the system previously simulated. Redoing the calculations, we obtain a noise of 17 e^-, an equalized threshold of 10 e^-, and a minimum detectable charge of 118 e^-.

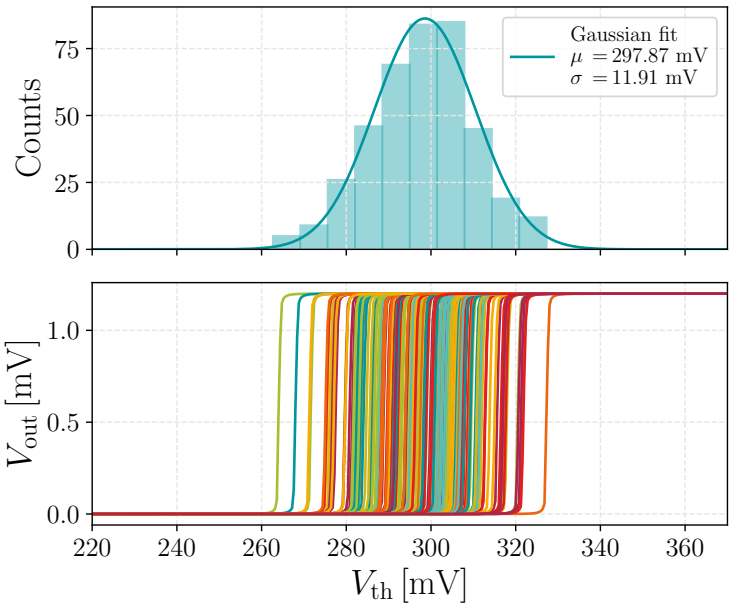

Figure 5.16: Result of a Monte Carlo simulation with 200 runs. At the top, the simulated number of counts versus the threshold voltage together with the Gaussian fit. At the bottom, the discriminator output voltage versus the threshold voltage. The unequalized threshold, which is the standard deviation, is 12 mV or 40 e^-.

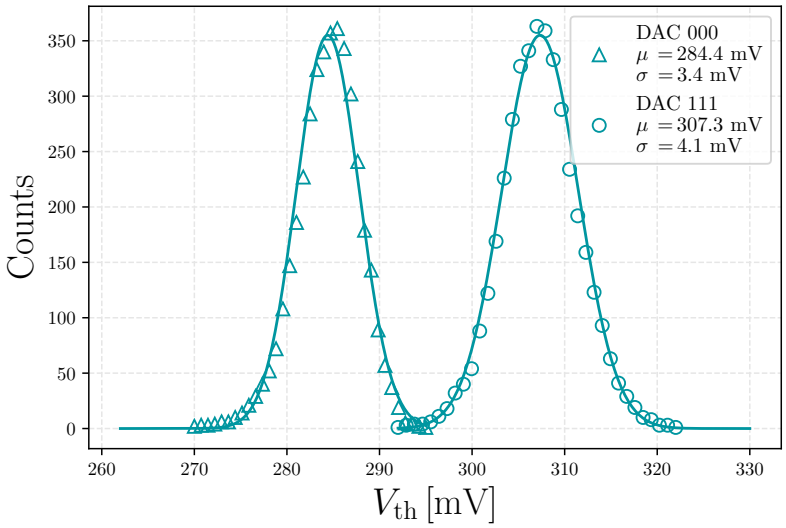

Figure 5.17: Number of events counted while scanning the threshold voltage for a single pixel. To extract these results we used the noise edge detection method.

5.5 Post-Layout Extraction Simulations

5.5.1 Layout Considerations

The layout (mask layout) represents the real geometry of the physical circuit elements formed by the various metal, oxide, and semiconductor layers. The finalized mask layout is then transferred to silicon through a photolithography process [113]. After validating the design at schematic level, the layout was routed. The front-end layout is depicted in Figure 5.18, featuring various sub-blocks: (1) collection electrode, (2) feedback capacitance, (3) feedback transistor, (4) input transistor, (5) CSA, (6) discriminator, and (7) 3-bit DAC, adding up to a total area of 320 µm^2. The sub-blocks correspond to the sub-circuits previously designed. Their layouts were routed individually while taking the global routing into account.

The PDK of the TPSCo 65 nm includes 7 metal layers. Metal 1 to Metal 2 were used for routing, with Metal 3 reserved exclusively for `vdda` and `vssa` routing (on top and bottom), and Metal 4 for the feedback capacitance. The gap between the collection electrode and the CSA accounts for distance Design Rule Check (DRC) rules between wells. The feedback capacitance, the feedback transistor, and the input transistor are kept together and as close as possible to the collection electrode to minimize parasitic capacitance on the input node and prevent degradation of transient performance.

The feedback capacitance was implemented by interconnecting metals [114]. Initially, the use of the three metal-to-metal capacitances connected in series each of them with the minimum value available on the PDK, which in total would be equal to 0.5 fF, was considered. However, the isolation and matching of this capacitance are crucial, as

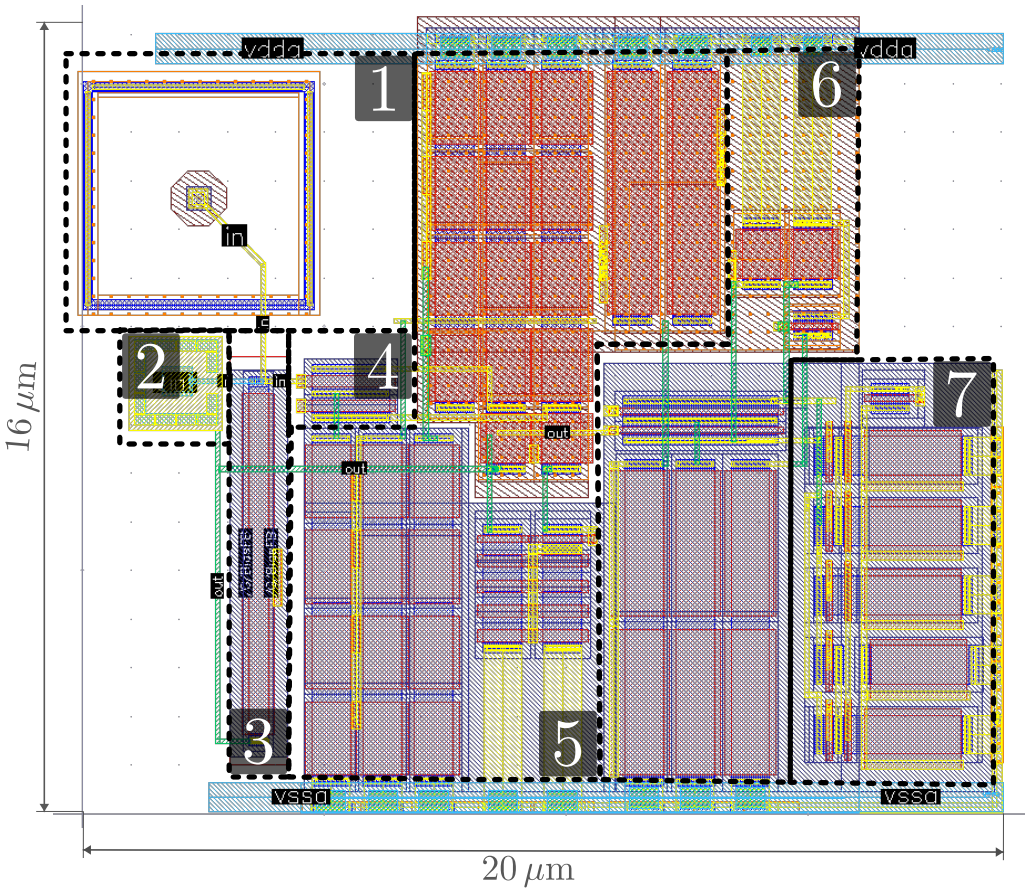

Figure 5.18: Layout of the low-power, low-noise front-end. The FE includes: (1) collection electrode, (2) feedback capacitance, (3) feedback transistor, (4) input transistor, (5) CSA, (6) discriminator, and (7) 3-bit DAC. This results in a total size of 320 µm^2.

fluctuations in this capacitance can lead to performance variations of the FE. The idea of interconnecting metals relies on precise matching, where the field lines of one plate of the capacitor should end up in the other plate. Hence, the inner terminal of the capacitance (in Metal 3) is surrounded by Metal 2 and Metal 4. An schematic view of the feedback capacitance and its implementation using interconnecting metals is offered in Figure 5.19

Because of space constraints, the use of dummy transistor to combat mismatch is not feasible. However, already in the schematic phase, the sizing of the transistors took into consideration radiation hardness and layout mismatch. The widths of the transistors were chosen in multiples of 800 nm to facilitate stacking and alignment, thereby reducing border effects. The routing maximizes the use of Metal 1 (used both vertically and horizontally), while Metal 2 is used for vertical routing, except in one case where it was used horizontally to reduce parasitic capacitances. Nevertheless, despite the methodical organization of the layout, parasitic capacitances are still present in our design, of the same order of magnitude as the feedback capacitance. This will have an effect on the transient performance of the FE.

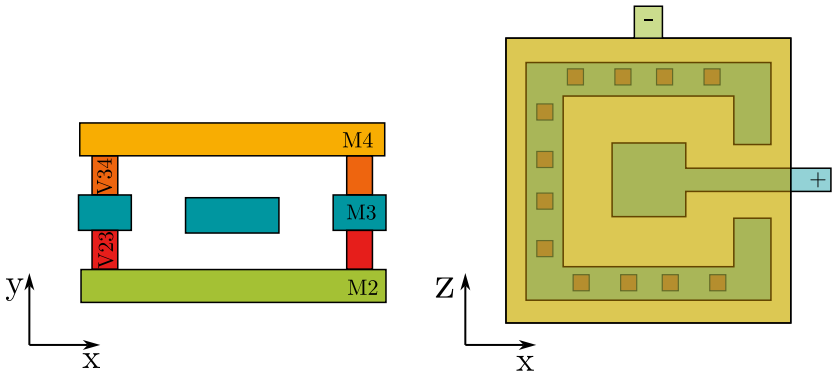

Figure 5.19: Schematic view of feedback capacitance based on interconecting metals. The inner terminal of the capacitance (in Metal 3) is surrounded by Metal 2 and Metal 4.

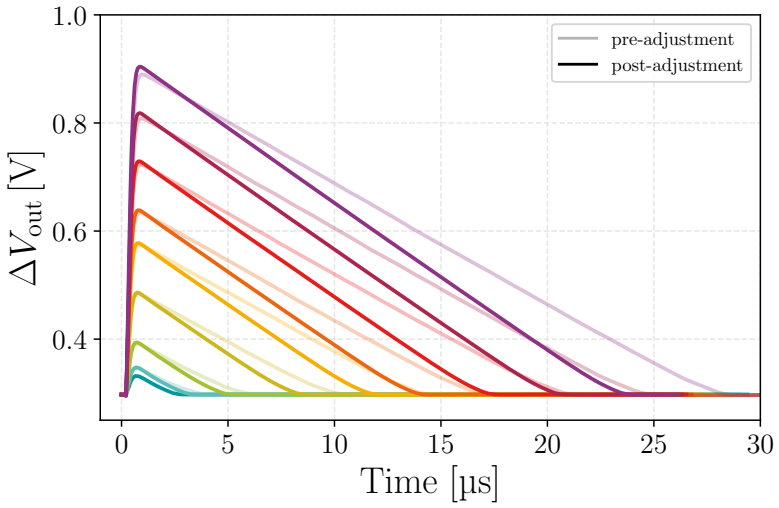

Figure 5.20: Transient simulation output of CSA with increased bias current: layout results. This plot shows the output voltage versus time but with a feedback biasing current of 1.25 nA. After adjustments, the transient performance becomes comparable to the schematic.

5.5.2 Influence of Parasitic Capacitances on the FE Performance

Figure 5.21 showcases the output of a transient simulation of the CSA with input pulses ranging from 100 e^- to 3000 e^-. On the left, the output voltage versus time is presented for input charges ranging from 100 e^- to 2000 e^-. Solid lines correspond to the schematic, and dashed lines correspond to the layout. To achieve similar performance, we had to increase the feedback current from 1 nA to 1.25 nA. If the bias current of the CSA is high enough, the transconductance of the input transistor, together with the feedback capacitance, will dominate the transient performance of the FE [Eq 2.10]. However, as the bias current decreases, the transconductance also decreases to its minimum. With the small value of C_{FB}, increasing parasitic capacitances (C_{IN}, C_L) will dominate the

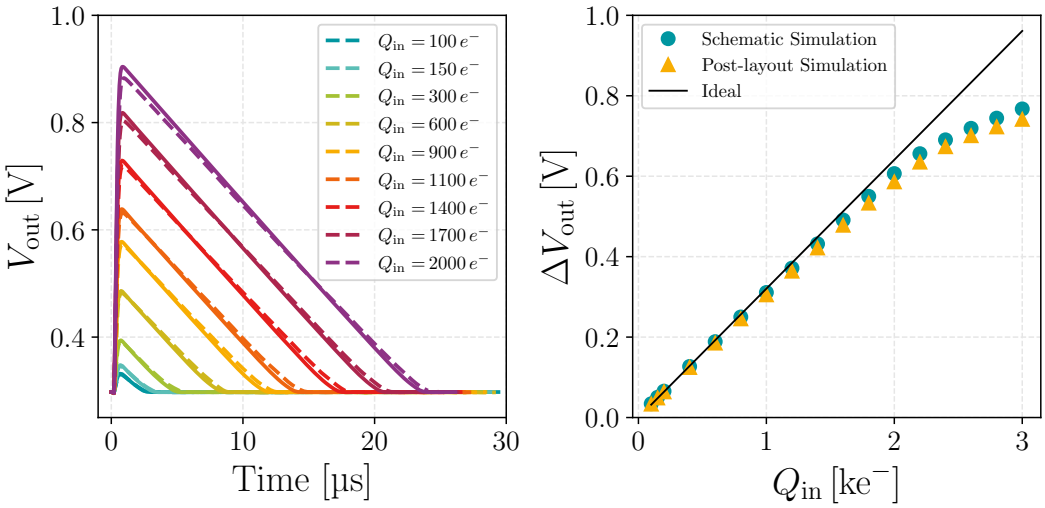

Figure 5.21: Transient simulation output of the CSA: comparison between schematic and layout. On the left, output voltage versus time for input charges ranging from 100 e$^-$ to 2000 e$^-$. The solid lines represent the schematic, while the dashed lines represent the layout. On the right, the maximum amplitude of the output pulse against the input charge. Blue dots correspond to schematic, orange dots to layout, and the black line represents the ideal. To achieve similar performance, the feedback current was increased from 1 nA to 1.25 nA.

transient performance. This effect is visible in Figure 5.20, which is the result of the same simulation as on Figure 5.21, but with a feedback biasing current of 1.25 nA.

Once the adjustment is done, the transient performance is comparable to the one of the schematic. In Figure 5.21, on the right, the maximum amplitude of the output pulse against the input charge is illustrated. Again, blue dots correspond to schematic, orange dots to layout, and the black line represents the ideal. The results are comparable to the ones achieved in the schematic simulation, showing linear behavior up to 2000 e$^-$ and a slope around 0.3 mV/e$^-$. Figure 5.22 displays the noise simulation of the extracted layout, with a standard deviation of 7 mV or 20 e$^-$. The stronger noise could be explained with the larger parasitic capacitances, which increase the series thermal noise as described in Section 5.2.

Figure 5.23 shows the threshold dispersion of the discriminator. The same as for the schematic, this is the result of a Monte Carlo simulation with 200 runs where at the top, the simulated number of counts versus the threshold voltage together with the Gaussian fit is presented. Meanwhile, at the bottom, the discriminator output voltage versus the threshold voltage is shown. The unequalized threshold, which is the standard deviation, is 13 mV or 43 e$^-$. Using Equation (5.6) and the previously extracted noise leads to a minimum detectable charge of 284 e$^-$. Using the 3-bit DAC, the equalized threshold

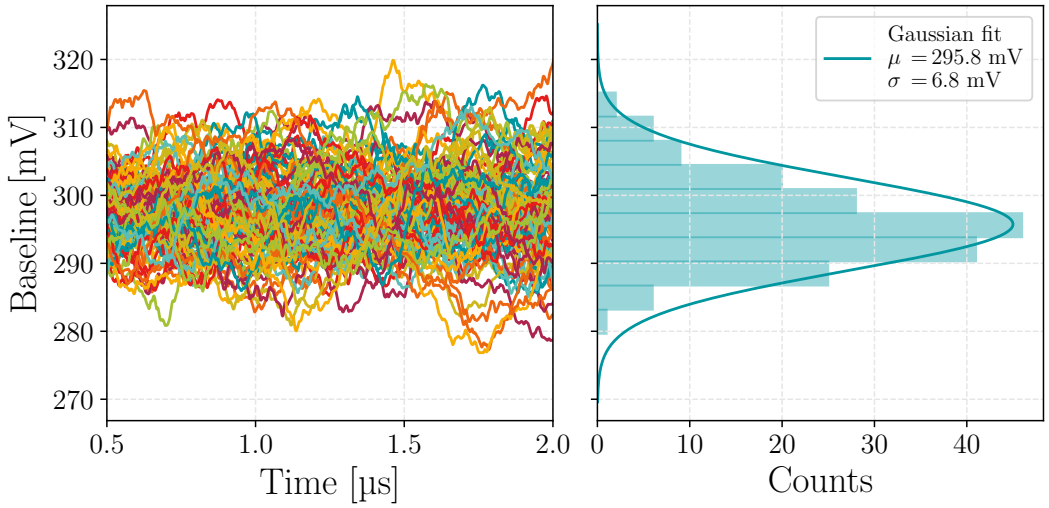

Figure 5.22: Noise measurement of extracted layout for CSA. The plot displays the noise measurement with a standard deviation of 7 mV or 20 e^-. The increase in noise can be attributed to the rise in parasitic capacitances, leading to an increase in series thermal noise.

would be 11 e^-, which, assuming a noise of 20 e^-, would lead to a minimum detectable charge of 136 e^-.

5.5.3 ToA and ToT Measurements

The expected behavior for Time-of-Arrival (ToA) and Time-over-Threshold (ToT) for test pulses up to 4000 e^- is shown in Figure 5.24. ToA measurements allow to measure the time of arrival of a particle while ToT measurements allow to calculate the energy of the particle by integrations.

The result is based on the nominal settings and the threshold is set to the unequalized minimum detectable charge 284 e^-. For charges larger than 500 e^-, the dispersion on the ToA drops to its minimum, being at its maximum around the threshold. Timewalk is defined as the ToA of a pulse 1000 e^- above threshold (in this case, a pulse of 1284 e^-); the measured timewalk is 850 ns. The Time-over-Threshold (ToT) is linear from 400 e^- with a slope of 11 µs/ke^-.

5.5.4 Voltage Drop

The biasing of this FE is expected to be similar to the one of the H2M, where a certain number of voltage-controlled current sources are used to bias the CSA, discriminator, feedback, and trimming DAC of each pixel. The power distribution is done at the column level [110], where all pixels on the same columns share the same power connections. This

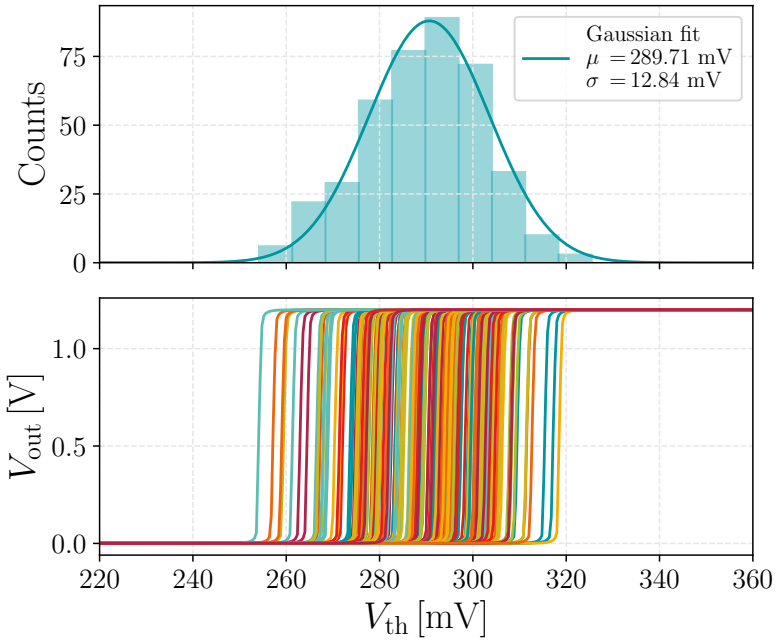

Figure 5.23: Threshold dispersion in discriminator: layout results. This plot illustrates the simulated number of counts versus the threshold voltage, along with a Gaussian fit. The unequalized threshold, represented by the standard deviation, is 13 mV or 43 e^-. Using the 3-bit DAC, the equalized threshold could be reduced to 11 e^-, resulting in a minimum detectable charge of 136 e^-.

ensures a uniform distribution across all pixels. The worst-case power distribution is a series of 256 pixel resistances (R_{pix}). The resistance of each pixel depends on the CMOS technology metal resistance ($R_{\square}$) and the metal line width:

$$R_{\text{pix}} = \frac{\text{pixel side}}{\text{metal width}} \cdot R_{\square}$$

Where the voltage drop can be calculated as:

$$V_{\text{Drop}} = I \cdot R_{\text{pix}} \cdot \frac{N^2}{2}$$

where N is the number of pixels per column. Figure 5.25 shows the worst-case power supply voltage drop for a pixel at the top for different biasing currents, where we assume a pixel side of 55 µm, a power distribution through Metal 8 which, assuming a minimum width of 0.2 µm, leads to an $R_{\square}$ of 85 mΩ.

Table 5.5 shows each block power (`vdda`) and ground (`vssa`), with each biasing current, and the respective power voltage drops achieved. The CSA and discriminator power lines

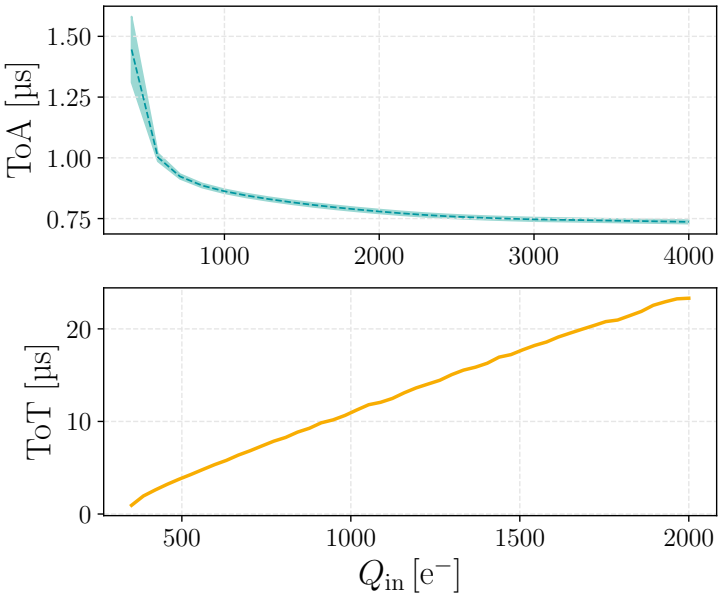

Figure 5.24: Time-of-Arrival (ToA) (left) and Time-over-Threshold (ToT) (right). The threshold is set to the unequalized minimum detectable charge (284 e$^-$). For charges larger than 500 e$^-$, the dispersion on ToA decreases to its minimum. Timewalk measures 850 ns. The ToT is linear from 400 e$^-$, with a slope of 11 µs/ke$^-$.

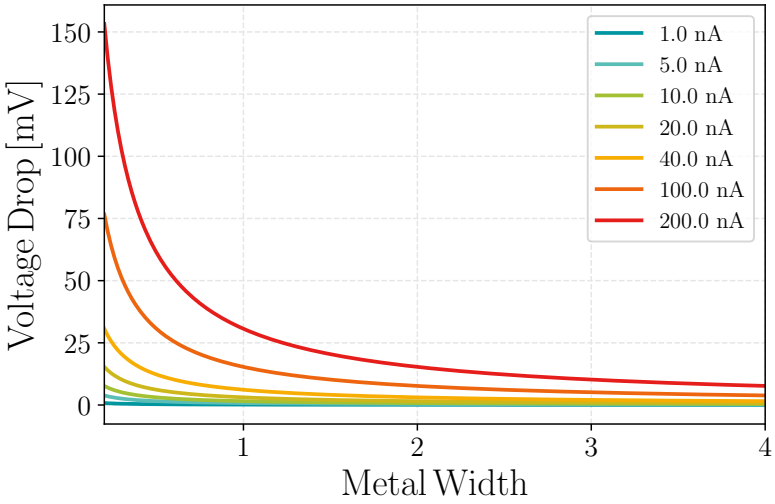

Figure 5.25: Worst-case power supply voltage drop for a pixel at the top.

experience the worst voltage drops because of the high currents they have to drive. This voltage drop, was tested on simulation leading to a negligible effect on the performance of the FE.

Table 5.5: Power lines (`vdda` and `vssa`), nominal currents, voltage drops, and metal widths for each block in the pixel front-end. The CSA and discriminator power lines experience significant voltage drops due to high currents, but simulations show negligible impact on the FE performance.

Power Line	Nominal Current [nA]	Voltage Drop [mV]	Metal Width [µm]
vdda_{CSA}	20	15.3	0.2
vssa_{CSA}	20	15.3	0.2
$\text{vdda}_{\text{Disc}}$	40	29.5	0.2
$\text{vssa}_{\text{Disc}}$	40	29.5	0.2

5.5.5 High-Power Mode

This front-end was designed for low-power purposes where transient performance is not the priority. However, certain designs might require faster timing for precise measurements while maintaining high gain. In such cases, this front-end can be biased with higher power consumption (bias CSA at 200 nA) to reduce the rise time from 500 ns to 50 ns. This is feasible thanks to the flexibility of this design. The increase in power consumption of the CSA results in higher transconductance for the input transistor, mitigating the effects induced by parasitic capacitances, reducing noise, and decreasing the system's rise time. The pulses obtained with this front-end are presented in Figure 5.26. Additionally, although the feedback capacitance is very small, the falling time can be tuned to be faster by increasing the feedback current from 1 nA to 4 nA.

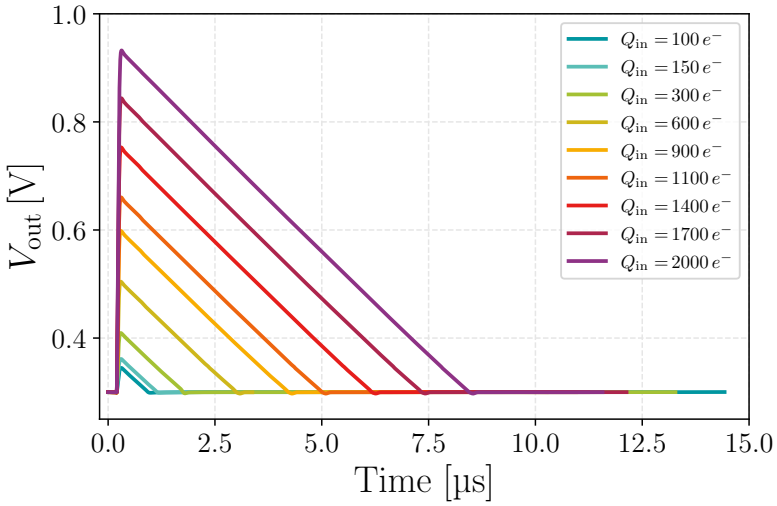

Figure 5.26: Output of a transient simulation of the CSA with input pulses ranging from 100 e^- to 2000 e^-. The output voltage versus time is presented for input charges ranging from 100 e^- to 2000 e^-. The CSA was biased at 200 nA and the feedback at 4 nA.

5.6 Comparison with the H2M and MOSS Front-Ends

The presented front-end showcases a wide linear detection range spanning from 136 e^- to 2000 e^-, featuring a linear gain of 0.3 mV/e^-, a response time of 500 ns, and a minimum detectable charge of 136 e^- in low-power mode (8.5 mW/cm^2). Its highly tunable nature enables a transient response of approximately 50 ns, all achieved by increasing the consumption to 114 mW per cm^2. Table 5.7 offers a comparison between the power consumption of the three FEs, and Table 5.6 provides a comparison of their performances. The simulations of the MOSS FE were extracted with an input of 5 fF.

Table 5.6: Simulation extracted specifications for the MOSS and H2M front-ends and comparison with the proposed design (low-power and high-power modes). The threshold for the H2M and proposed FEs is equalized.

Quantity		MOSS FE	Low-Power FE	High-Power FE	H2M FE
Gain	mV/e^-	0.5	0.3	0.3	0.12
MDC	e^-	100	136	118	220
Threshold	e^- r.m.s	16	11	10	25
ENC	e^- r.m.s	17	20	17	27
Peaking time	ns	1500	500	50	10
Area	µm^2	42	320	320	525

Table 5.7: Nominal settings of the H2M, MOSS, and the proposed FEs (for both low-power and high-power modes).

H2M FE			MOSS FE			Low/High-Power FE		
Signal	Value	Unit	Signal	Value	Unit	Signal	Value	Unit
`BiasCSA`	2.6 - 1.3	µA	`IBIAS`	25	nA	`ICSA`	10/200	nA
`BiasComp`	1.1 - 0	µA	`IBIASN`	2.5	nA	`IDISC`	20/100	nA
`KrumRef`	325	mV	`IRESET`	5	pA	`IFB`	1.25/4	nA
`CompThres`	325	mV	`IDB`	25	nA	`IDAC`	1	nA
`VbCSA`	675	mV	`VCASN`	200	mV	`VDISC`	750	mV
`VbKrum_A`	990	mV	`VCASB`	80	mV			
`VbDAC_A`	886	mV	`VSHIFT`	600	mV			
`Inj_Bias`	0 - 350	mV						

The power consumption of the H2M FE exceeds the limits suitable for scaled systems (i.e., a power density of 20 mW/cm^2 for the pixel sensors for the inner barrel of the ALICE ITS3 upgrade [115]). Yet, it continues to be the fastest FE, followed by the proposed FE working at high-power mode. On the contrary, the MOSS FE, with an extremely low power budget, gives the best performance in terms of gain and noise, the latter due to the lack of a feedback network for compensation. However, the peaking time of 1.5 µs makes it the slowest system. Additionally, due to the lack of threshold equalization, its threshold dispersion cannot be corrected. The proposed front-end, working at low-power mode, falls between these two. Like the H2M, it is based on CSA topology, which is a well-known, reliable, easy-to-model, and easy-to-tune topology. The gain, with respect to

the one achieved by the H2M FE, has been enhanced, enabling it to detect MIPs signals. The inclusion of a 3-bit DAC facilitates the equalization of the threshold, ensuring it remains lower than that of the MOSS front-end. Moreover, operating the proposed front-end in high-power mode maintains the same gain and area, while improving the minimum detectable charge, reducing the threshold and peaking time, and achieving noise levels comparable to those of the MOSS front-end.

Table 5.8 shows the performance of this front-end in terms of noise, amplitude of the output pulse, baseline, rise time, and fall time, under different corners, temperatures, and voltage drops, proving its robustness and capacity to maintain stability under different biasing conditions. Nevertheless, critical areas for improvement or potential weaknesses compared to the other designs are identified:

- **Size:** The current size is optimized for a 35 µm pixel pitch (similar to H2M) but is too large for the 15 µm of the MOSS. Future iterations could incorporate smaller transistors or peripheral placement of specific ones to enhance adaptability.
- **Feedback Capacitance:** A metal-to-metal capacitor with a low value but a potential ±20 % post-production shift was chosen to mitigate mismatch. Post-layout simulations with maximum and minimum variations affirm the front-end's robustness across corners.
- **Feedback Current:** The feedback current, around 1 nA, divided between 100 transistors on the periphery to achieve 10 pA, signifies that even a small variation in this current can substantially impact the falling time, as seen in previous sections. Again, corners confirm the variations on the falling time but always within a reasonable limit that can be retuned.

Both MOSS and the proposed front-ends, each with distinct topologies, offer options for low-power applications but come with inherent risks. For example, both designs rely on currents on the order of pA, comparable to the leakage current of this technology. In the case of the MOSS FE, this results in nMOS transistors barely conducting, leading the front-end to rely on leakage current, causing operational instability and lower yield. Moreover, despite the notable improvements in power consumption, detection range, and noise levels compared to H2M, achieving an identical transient performance would necessitate a power consumption closer to that of H2M. Striving for the minimum power consumption may result in significant performance consequences. Increasing the input transistor bias current could result in a more relaxed and performant operation, albeit requiring adjustments to the power dissipation requirements.

Table 5.8: Corner simulations (FS, SF, FF, SS, TYP) of the presented front-end working in low-power mode with an input charge of 1000 e^-.

		Value	@vdda [V]	@Temperature [°C]	@Corner
Noise [e^- r.m.s]	Min.	17.9	1.20	-30	SS
	Nom.	20.7	1.20	27	TYP
	Max.	24.0	1.20	-30	FF
Vout Amplitude [mV]	Min.	309.4	1.20	100	FS
	Nom.	321.1	1.20	27	TYP
	Max.	323.5	1.20	-30	FS
Baseline [mV]	Min.	292.2	1.20	100	FS
	Nom.	297.0	1.20	27	TYP
	Max.	299.4	1.08	27	SS
Rise Time [ns]	Min.	309.6	1.20	-30	FS
	Nom.	372.5	1.20	27	TYP
	Max.	503.0	1.08	27	SS
Fall Time [µs]	Min.	13.2	1.20	-30	FS
	Nom.	20.5	1.20	27	TYP
	Max.	23.9	1.20	100	TYP

5.7 Summary

This chapter delves into the design of a low-power, low-noise front-end utilizing TP-SCo 65 nm technology. The initial constraint for our design was the low-power biasing current for the CSA, resulting in a considerable reduction in the transconductance of the input transistor and, consequently, a loss of gain. The second constraint was the necessity for a low feedback capacitance to effectively amplify small input signals. Considering these constraints, the CSA design focused on enhancing gain while keeping the power budget low. We compared several topologies, all based on a common-source amplifier. In the case of not requiring adjustment of the baseline level, the cascoded common-source amplifier seemed to be the simplest and most effective approach. However, to address the need for baseline tuning, a differential amplifier with a folded cascode gain stage was chosen. The narrow bandwidth of the amplifier posed challenges in tuning the feedback network, requiring a feedback current of the same order of magnitude as the leakage current of this technology. This challenge was overcome by employing constant current feedback with a replica circuit as biasing, ensuring the system's robustness. A two-stage differential amplifier was chosen for the discriminator, allowing for threshold equalization thanks to a 3-bit binary weighted DAC.

Table 5.9 offers a comprehensive overview of key specifications (extracted from post-layout simulations and presented throughout the chapter) for the designed FE, operating in both high and low power modes. Essential parameters, including total current, power density, gain, noise levels, and minimum detectable charge, are presented for both modes, providing a thorough understanding of the FE's capabilities under different operational

scenarios. However, it is important to mention the slight difference in performance for the low-power mode between the schematic and the layout simulation due to parasitic capacitances on the input and output nodes and the small feedback capacitance. This should be taken into account in the design of future front-ends with such a small power budget.

The low-power mode is tailored for applications like the ALICE ITS3 upgrade, which is particularly advantageous for systems with relaxed rise time requirements and limited cooling capabilities. In contrast, the high-power mode is optimized for applications such as a larger-scale version of the H2M, aspiring to achieve performance comparable to Timepix1 or Timepix2 systems [116, 117], especially in terms of timing precision. A comparison of the designed front-end with these two existing systems was offered, pointing out the pros and cons of this and the other two designs, such as higher noise and an increase in power consumption, better linearity, and more robustness within the same area, etc. Additionally, some possible changes in the design to adapt it to a larger scale version of the H2M or a new MOSS prototype were proposed.

In conclusion, this design proves the possibility of designing a low-power, low-noise front-end on the TPSCo 65 nm technology based on the transconductance amplifier. This can allow different ASICs to take advantage of a more robust and easy to model topology, well prepared for time and energy measurements.

Table 5.9: Final specifications of our design for high-power and low-power modes for a 35 µm × 35 µm pixel size.

Quantity		High Power	Low Power
I_{CSA}	nA	200	10
I_{DISC}	nA	150	20
I_{FB}	nA	4	1.25
Total Current	nA	351	31.25
Total Power	nW	1320	107
Power Density	$\mathrm{mW/cm^2}$	114	8.5
Gain	$\mathrm{mV/e^-}$	0.3	0.3
Rise Time	ns	≈ 50	≈ 500
Noise	mV r.m.s.	5	7
Noise	$\mathrm{e^-}$ r.m.s.	17	20
Unequalized Threshold	mV r.m.s.	12	13
Unequalized Threshold	$\mathrm{e^-}$ r.m.s.	40	43
Equalized Threshold	mV r.m.s.	3	3
Equalized Threshold	$\mathrm{e^-}$ r.m.s.	10	11
MDC	$\mathrm{e^-}$	118	136

6 Conclusions and Outlook

The present thesis demonstrates how a front-end based on a transconductance amplifier can be used in monolithic applications that require low power consumption, focusing on detecting and amplifying MIP signals. Chapter 2 covers the foundations of the thesis, delving into pixel detectors used in high-energy physics experiments and certain mathematical considerations requeired for the design of FEs based on a CSA. Subsequently, Chapter 3 and Chapter 4 present a complete characterization of this technology node under irradiation sources and differetn back biases, using the EKV model to understand its analog performance. Finally, using the knowledge from the previous chapters, Chapter 5 covers the design and simulation, at schematic and layout levels, of a low-noise and low-power front-end for monolithic active pixel applications using the TPSCo 65 nm node.

Chapter 2 introduces pixel detectors used in high-energy physics experiments. These detectors typically consist of a sensor with a collection electrode and readout electronics. The chapter begins with an explanation of the PN junction, a key element in analog design and the collection electrode in pixel detectors. It then explores how ionizing particles interact with the sensor to detect charge. Section 2.1 concludes by outlining the main components of the processing chain and distinguishes between hybrid pixel sensors, where the sensor and readout electronics are on separate substrates, and monolithic pixel sensors, where they share the same substrate. The design presented in this thesis uses the monolithic TPSCo 65 nm node, and therefore, in Section 2.3, we introduced two recent front-end prototype designs using this node: MOSS and H2M. The first one is a low-power, low-noise, and low-area proposal for the ALICE ITS3 upgrade, characterized by its unconventional topology for an FE, based on a common source follower for the amplification stage. The second one is a small prototype chip which aims to export an hybrid topology into a monolithic one. Its FE has a larger footprint and power consumption, but with a more traditional and robust topology based on a CSA. Finally, Section 2.4 introduces considerations on the design of front-ends based on a CSA

regarding noise, stability, and time performance, which were taken into account in the design presented in Chapter 5.

These types of pixel detectors, used in high-energy physics experiments, are distributed as a pixelated layers around the collision point. For example, a pixel detector in the HL-LHC is expected to endure a Total Ionizing Dose (TID) level of up to 1 Grad (SiO_2). The TPSCo 65 nm process is the primary candidate for developing new monolithic active CMOS pixel sensors for vertex measurements in high-rate and hostile environments at CERN. Ionizing particles accumulate on different parts of the transistors present in the pixel. We distinguished four different effects: gate-oxide effects, spacer-related effects, STI-related effects, and leakage current. Therefore, to avoid unexpected behavior during operation in analog and digital designs, the response of the TPSCo 65 nm to TID was studied.

In Chapter 3, various Transistor Test Structures (TTS) devices, including pMOS and nMOS, were designed and tested for this purpose. Results from TID tests up to 1 Grad (SiO_2) show that nMOS transistors exhibit a maximum $\approx 15\%$ drop in their maximum delivered drain current, while pMOS transistors show a significant $\approx 80\%$ drop. The study confirms the presence of RINCE and RISCE, with threshold voltage V_{TH} shifts up to $-200\,\mathrm{mV}$ and subsequent recovery after annealing. Comparisons between standard and modified processes indicate similar performance, while thick oxide devices show higher vulnerability to TID.

Various parameters were extracted, including the variation of the maximum drain current in saturation ($I_{\mathrm{ON}}^{\mathrm{sat}}$), the variation of the leakage current in saturation ($I_{\mathrm{OFF}}^{\mathrm{sat}}$), the transconductance parameter (K_{U}), and the threshold voltage (V_{TH}). Numerous publications have utilized these figures of merit to investigate the physics underlying TID effects. Yet, these parameters were derived from the traditional representation of the $I_{\mathrm{D}}(V_{\mathrm{GS}})$ characteristic of a transistor, dependent on the overdrive voltage $V_{\mathrm{OV}} = V_{\mathrm{GS}} - V_{\mathrm{TH}}$. This renders them an outdated representation of how TID can affect the analog performance of more advanced technology nodes, where the operating point tends to be closer to weak inversion.

Consequently, in Chapter 4, the simplified EKV MOSFET model was used to characterize TID effects on the TPSCo 65 nm technology, building on previous work done for the 28 nm node. Using a Python routine, this model, extracted key parameters threshold voltage, velocity of saturation, slope factor, and specific current ($V_{\mathrm{TH}}, \lambda_{\mathrm{c}}, I_{\mathrm{spec}}, n$) at different irradiation levels and bulk biases. The presented routine has three characteristic points: (i) the velocity of saturation effect is not taken into account until the final stage of the extraction, (ii) it avoids pre-filtering of the data to prevent missing information, and (iii) the overfitting issue due to the nonlinearity of the nonlinear least squares is rectified by weighting the cost function.

The analysis confirmed TID-induced effects such as RINCE and RISCE and demonstrated that normalization can mitigate the TID impact on transconductance efficiency. Additionally, the study examined performance degradation of nMOS transistors under negative back-gate biases, accurately capturing threshold voltage shifts. The sEKV model and extraction routine are powerful tools for analog designers, enabling effective modeling of transistor performance across various operating points in radiation-tolerant circuit designs.

Finally, Chapter 5 presents the design of a low-power, low-noise front-end utilizing TPSCo 65 nm technology, integrating insights from Chapters 3 and 4. Utilizing the sEKV model and an IC design approach, fundamental limits on low-power and low-noise front-ends were explored, leading to a comprehensive design procedure. Some of the limitations are:

- To boost the amplification of low energy signals the feedback capacitance must have a small value.
- Small feedback capacitance value together with low-power consumption are not beneficial in terms of transient performance but will keep the noise low.
- An increase in power consumption would improve the speed while maintaining the same noise level.
- One of the drawbacks of this transconductance topology is the feedback that introduces a parallel thermal noise source.

The linear detection range of the designed front-end spans from $136\,e^-$ to $2000\,e^-$, featuring a linear gain of $0.3\,mV/e^-$ and a minimum detectable charge of $136\,e^-$ in low-power mode ($8.5\,mW/cm^2$), with a rise time of 500 ns, and a noise of $20\,e^-rms$. The designed FE demonstrates the viability of a low-power, low-noise approach on TPSCo 65 nm technology. Applications range from MOSS chips for the ALICE ITS3, offering improved robustness and a more traditional topology easy to model and operate, to an upgrade to a larger-scale version of the H2M chip, where its current FE could not be used due to its high power consumption.

The presented results confirm the presence of irradiation effects observed in other well-known 65 nm nodes, making the TPSCo 65 nm a promising node for the high-energy physics community. Nonetheless, further studies are needed to quantify device variability and comprehensively understand radiation-induced effects. The presented sEKV extractor, can extract the four sEKV parameters at different irradiation steps. Yet, for analog designers, it would be beneficial to extract these four parameters for a transistor size independent of the irradiation level. For this purpose, the author proposes an extension of the code to model the “parallel transistors” generated alongside the channel when

charges accumulate on the spacers, leading to the transistors to appear narrower. The implementation of the presented FE requires two main steps. With the approval of the ITS3 upgrade in 2024, the first step has been taken. However, the MOSS chip still needs to undergo further testing to ensure that its FE meets the project's requirements. The designed FE is offered as an alternative. Secondly, the small-scale H2M chip is being successfully tested, but the development of a larger-scale version where the presented FE could be included is needed.

A H2M Analog Periphery: Design and Testing

The development of the Hybrid-to-Monolithic (H2M) project commenced in the last trimester of 2020. By the end of the first trimester of 2021, the design of the analog periphery had begun, with the completion date set for the end of 2021. The whole design of the periphery was carried out by the author. The chip was submitted in mid-2023, and it is currently undergoing successful testing, resulting in the following publications [14–18]. Simultaneously, certain sub-blocks of this periphery were utilized in the periphery of the MOSS chip, leading to the subsequent publication [19].

The designed and tested analog periphery delivers stable and temperature independent biasing currents and voltages to the analog front-end of the prototype chip. It is based on three main blocks: a DAC, a R2R amplifier, and a bandgap. In the first stage of the thesis, an 8-bit DAC was successfully designed and characterized. Using this DAC as a base, three different circuitries were developed to adapt each current DAC output range to the specifications delivered for the front-end. These are used to bias the Krummenacher amplifier, CSA, and the trimming threshold, all located at the analog front-end. The layout of the DAC is shown in Figure A.1.

Afterwards, an R2R amplifier was implemented based on the architecture from R. Hogervorst [118] previously used in Timepix2 [117] and Timepix4 [87] designs. This block was used as a unity gain buffer to isolate the output node of the current DACs from the input node of the front-end biasing point. This R2R was also used to design a voltage DAC. Using the current steering 8-bit DAC, the binary weighted output current is transformed to a voltage, which is scaled with the R2R buffer from vdda to vssa. The layout of the R2R is presented in Figure A.2.

Two additional blocks were designed by the author. First, a trimming block for the bandgap was developed to ensure compensation for any unexpected variation in the delivered current. Second, based on the R2R, a monitoring block to control the operating point of all the voltage and current DACs from the digital pads. The 8-bit DACs need a stable input current which is transformed into an output current range. To fulfill this

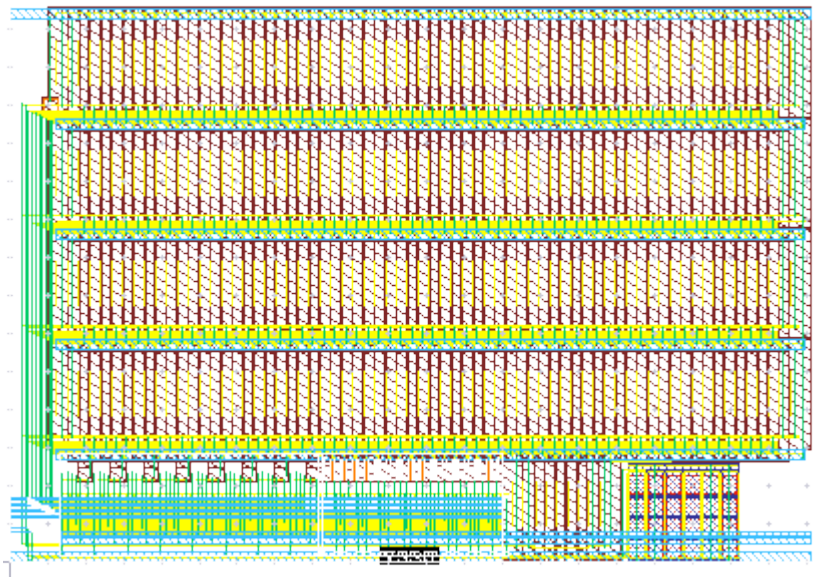

Figure A.1: Layout of the 8-bit DAC. The main block is a matrix of transistors distributed in centroid configuration for better mismatch.

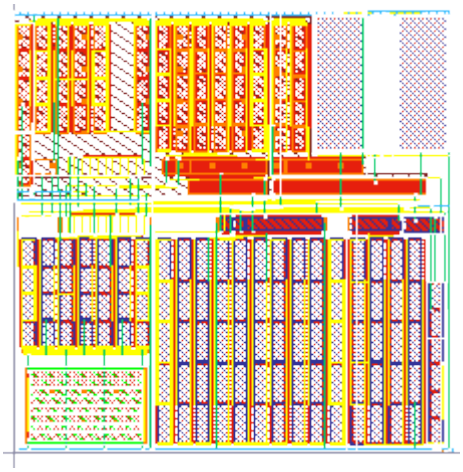

Figure A.2: Layout of the R2R block.

purpose, we used the bandgap designed at NIKHEF [119]. This bandgap delivers a constant, stable, and temperature-independent current (or voltage) which can be used to bias other circuits. In our case, circuitry was designed to match the required input current range to that delivered by our DAC. This periphery was brought together successfully at the layout level and confirmed to have good behavior once connected to the front-end at the schematic level.

The layout of the analog periphery is shown in Figure A.3. Inside the main rectangle (which is the guard ring), on the right, we can find three voltage DACs, and on the left, the three current DACs. These six DACs generate the necessary voltages and currents to

bias the CSA, Krummenacher feedback, DAC and comparator on the FE. The circuitry at the bottom of these blocks is the set of current mirrors used to adapt the output range of each DAC to the specifications of the FE (e.g. from the original 50 nA to 1.2 µA range to the necessary 1.3 µA to 2.6 µA range needed for the CSA). To the left of this main block, we can find the bandgap with its adapting network.

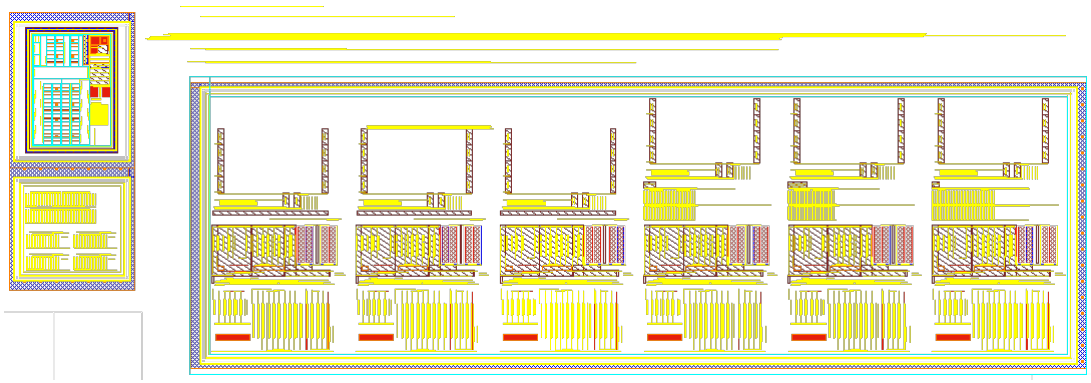

Figure A.3: Layout of the analog periphery. Inside the main rectangle (which is the guard ring), on the right, we can find three voltage DACs, and on the left, the three current DACs. The circuitry at the bottom of these blocks is the set of current mirrors used to adapt the range delivered by each DAC to the specifications of the FE.

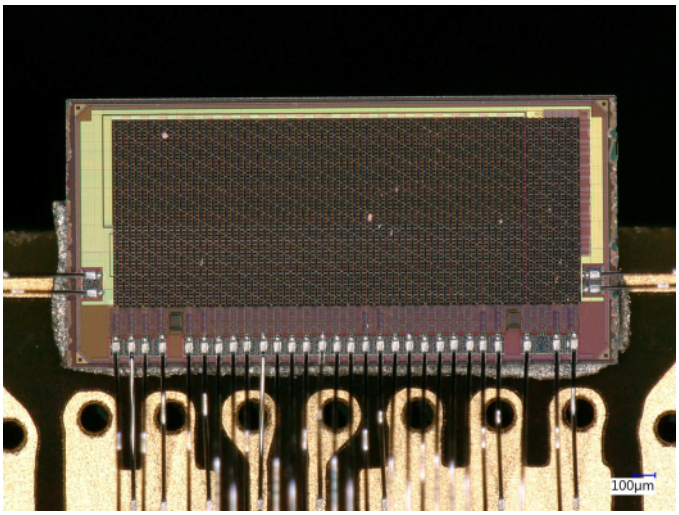

Figure A.4: The H2M chip bonded to be tested. Picture taken by J. Alozy.

After returning from the foundry, the chip was prepared for testing (Figure A.4). As a first step, a scan of the DAC's output current was performed. Figure A.5 shows the simulated transfer function of the 8-bit DAC compared with the measured mean and standard deviation. The slope difference between the measurements and the simulation is clear; however, it is important to consider that the simulations were performed without connecting the DACs to the FE. After further investigation, we concluded that this difference in slope is due to the lack of voltage headroom of the transistors on the FE. The measured Differential NonLinearity Error (DNL) and Integral NonLinearity Error (INL)

are shown in Figure A.6. The DNL is the deviation of the output steps from the ideal analog LSB value

$$\mathrm{DNL}[n] = I_{\mathrm{out,real}}[n+1] - I_{\mathrm{out,real}}[n] - I_{\mathrm{LSB}}, \tag{A.1}$$

and the INL is defined as the deviation of the actual input-output characteristic from the ideal transfer characteristic

$$\mathrm{INL}[n] = \sum_{i=0}^{n} \mathrm{DNL}[i] \tag{A.2}$$

[120]. The DNL is below 1 LSB and the INL below 0.5 LSB, ensuring non missing codes.

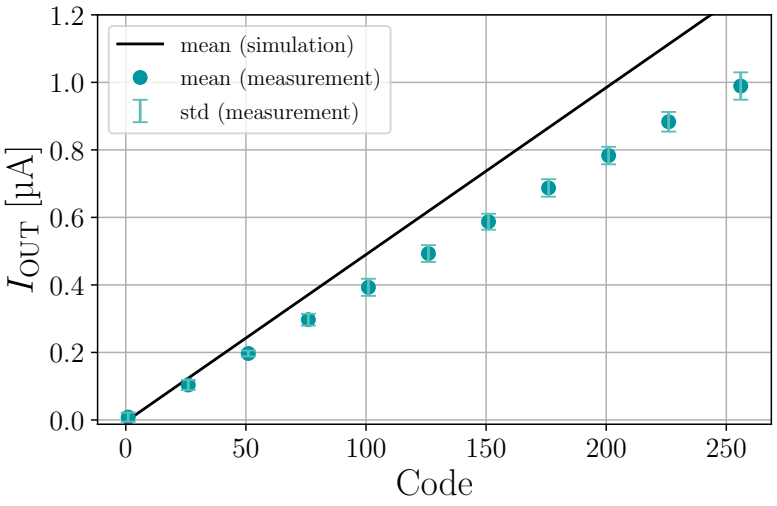

Figure A.5: Simulated transfer function of the 8-bit DAC compared with the measured mean and standard deviation. The slope difference between the measurements and the simulation is due to the lack of voltage headroom of the transistors on the FE.

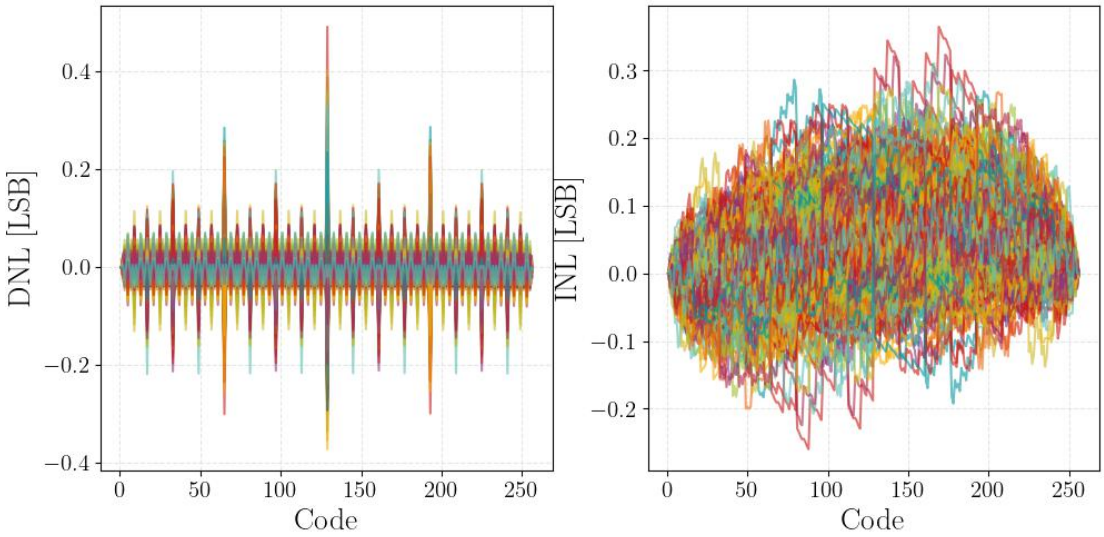

Figure A.6: Measured DNL and INL. The DNL is below 1 LSB and the INL below 0.5 LSB, ensuring non missing codes.

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