Control of a Modular Multiport Solid State Transformer for a Flexible High Power Charging Infrastructure

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***Index Terms*—Solid-State Transformer, Multi-level converters, Cascaded H-Bridge, Control strategy, Charging infrastructure for EVs**

***Abstract*—This paper presents a control strategy for a Multiport Solid-State Transformer designed to connect multiple EV charging stations to the medium-voltage AC grid. The transformer employs a Cascaded H-Bridge converter composed of identical switching cells, each incorporating a Dual Active Bridge to provide galvanic isolation between the AC grid and the charging ports. Steady-state modelling of the multilevel converter is used to identify the permissible power imbalance between charging ports, ensuring stable operation. The proposed real-time control method facilitates independent output power control for each port while maintaining effective cell voltage balancing across the converter. Furthermore, dynamic switch matrix reconfiguration enhance the converter's operational range. The control strategy is validated through simulations and experimental measurements, demonstrating improved flexibility and performance for scalable EV charging infrastructure.**

I. Introduction

The increasing electrification of the transport sector requires expansion of charging infrastructure with charging powers up to hundreds of kilowatts. This poses a particular challenge to the distribution grid and power electronics. Conventional charging stations have several charging points, each equipped with a galvanically isolated DC/DC converter to overcome the normative requirements for electrical safety [1]. The charging ports are connected to the Medium Voltage Alternating Current (MV-AC) grid via a low voltage converter and a line frequency step-down transformer. This topology results in double galvanic isolation from the MV-AC grid, which increases the material costs and reduces the system efficiency [2]. Several Solid State Transformers (SSTs) topologies have been proposed in the literature to eliminate this double galvanic isolation when interfacing several low voltage DC charging points to the MV-AC grid. The proposed topologies are based on modular SSTs, where each cell incorporates a full bridge on the AC side and a galvanically isolated DC/DC converter. The cells of each converter arm are connected in series on the AC side to enable the direct connection to the MV-AC grid. In [3], a delta-connected Cascaded H-Bridge (CHB) converter with Quadruple Active Bridges as cell DC/DC converters is presented. The cells of each converter arm are connected in parallel on the DC side, forming an output port of the converter. However, unequal load conditions must be compensated for by a complicated winding arrangement of the transformers or by injecting a circular current. In [4] a star connected CHB converter with cell integrated Battery Energy Storages (BESs) is proposed. For this system, N cells of each converter arm are connected in parallel on the DC side to form an output port. The power of each output port can be controlled independently by using the cell's integrated BES as an energy buffer. A similar topology shown in Fig. 1 was proposed in [5], omitting the BES and thus reducing the converter size. To allow reconfiguration of the converter, a switch matrix has been added to the DC side. A balancing strategy for the grid-side DC-link capacitors was introduced in [6]. PI controllers are employed to adjust the AC output voltage of the cells, mitigating unequal load scenarios. However, the boundaries of load imbalance remain unexplored in the existing literature. This paper aims to provide an

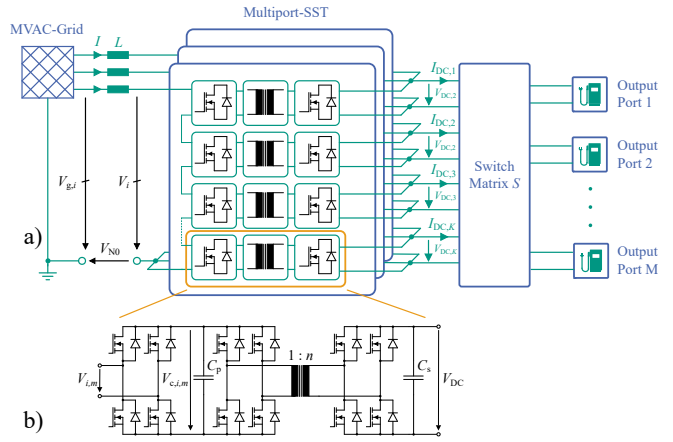

Fig. 1: a) Converter and b) cell topology of the proposed MP-SST

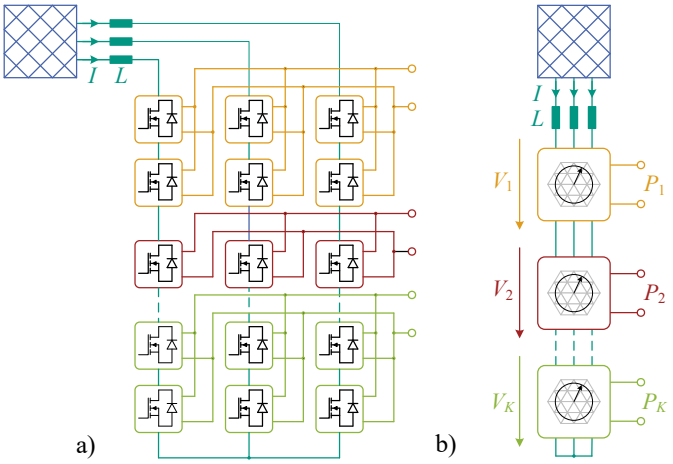

Fig. 2: a) Exemplary cell grouping and b) corresponding functional equivalent model of the MP-SST for one switching state of the switch matrix

in-depth analysis of the Multiport Solid State Transformer (MP-SST), facilitating the determination of the maximum permissible load imbalance. The paper begins with a steady-state analysis of the converter, followed by the development of a real-time control strategy. This includes independent output power control for different charging ports, cell voltage balancing, and AC-side regulation. Additionally, a methodology for the online reconfiguration of the switch matrix is proposed. The theoretical framework is validated through simulation results and experimental measurements conducted on a low-voltage prototype.

II. System Description

The converter structure is shown in Fig. 1a. The converter is based on a three phase CHB in star connection. Each converter cell consists of a full bridge on the AC side and a Dual Active Bridge (DAB). On the DC side, cell groups of three cells, one from each phase, are connected in parallel on the output side. The cell groups are connected to the input of a switch matrix. The output of the switch matrix is connected to the charging ports. In this way, the cell groups can be dynamically connected to the charging ports depending on the load situation. The switch matrix is described by the $M \times K$-matrix $\boldsymbol{S}$, with M cell groups and K output ports. For a connection from the cell group m to the output port k, $S_{m,k} = 1$, otherwise, $S_{m,k} = 0$. Each cell group can be connected to only one output port. The number of cell groups assigned to port k is denoted with n_k.

A. Steady-State Model

Fig. 2 shows the functional equivalent model of the MP-SST for an arbitrarily selected switching state of the switch matrix. Each output port k is modelled as a power source with output power P_k on the DC-side. On the AC-grid, the output port is represented as a three-phase voltage source with the phase-to-phase voltage $\underline{V}_\mathrm{k}$. It is assumed that the converter is operated in steady state and that the losses of the converter can be neglected. Under these assumptions, the AC-side voltage balance is described by

$$\underline{V}_\mathrm{g} = \sum_{k=1}^{K} \underline{V}_k + \mathrm{j}\omega L \underline{I} \tag{1}$$

with the grid voltage $\underline{V}_\mathrm{g}$, the grid current I and the filter inductance L. The equation shows the series connection of the individual ports. Each port provides a sinusoidal output voltage $\underline{V}_k$, which is limited by the available total DC-link voltage of the port. The maximum output voltage is

$$V_{k,\max} = \frac{\min\left[V_{k,\mathrm{U}} + V_{k,\mathrm{V}}, V_{k,\mathrm{V}} + V_{k,\mathrm{W}}, V_{k,\mathrm{W}} + V_{k,\mathrm{U}}\right]}{\sqrt{2}} \tag{2}$$

$V_{k,i}$ is the cell voltage sum associated with port k calculated by:

$$V_{k,i} = \sum_{m=1}^{M} S_{m,k} V_{\mathrm{c},i,m} \tag{3}$$

Here, $i = \{\mathrm{U}, \mathrm{V}, \mathrm{W}\}$ is the phase index and $V_{\mathrm{c},i,m}$ is the DC-link voltage of the individual cells. If all converter cells have the same DC-link voltage V_c, (2) is simplified to $V_{\mathrm{k,max}} = \sqrt{2} n_k V_\mathrm{c}$.

To ensure that the DC link voltages of the SST cells of a port remain constant, the port must be supplied with exactly the same amount of power on the AC side as is

drawn on the DC side and vice versa. The power P_k supplied to a port is dependent on the grid current I, which is shared by all ports, and the AC-output voltage of the port. It is calculated from

$$P_k = \sqrt{3}\mathrm{Re}\left(\underline{V}_k \underline{I}^*\right) \tag{4}$$

The port output power P_k can therefore be controlled independently of each other as long as the AC-side voltage balance is maintained and the maximum port voltage $V_{\mathrm{k,max}}$ is not exceeded.

B. Power Control of the Ports

For a high power charging station, each connected Battery Electric Vehicle (BEV) will request a charging power P_k^* at port k, which may depend on the battery type, capacity, state of charge and the battery's open circuit voltage. To charge the vehicle as fast as possible, the charging station tries to supply the requested power P_k^*. For the proposed MP-SST, the achievable port powers P_k^* are linked by (1) and (4), so the P_k^* may have to be reduced depending on the configuration and operating point. A flowchart for the proposed algorithm for the power reduction is shown in Fig. 3. In order to transmit active power, a sufficient amount of cells need to be assigned to output ports with $P_k^* > 0\,\mathrm{W}$. This requirement is formulated as

$$\sum_{k=1}^{K} \left(V_{k,\max} \cdot \mathrm{sgn}\left(P_k^*\right)\right) \geq V_\mathrm{g} \tag{5}$$

, assuming $|\omega L \underline{I}| \ll V_\mathrm{g}$, thus neglecting load dependent voltage drop at the filter inductance L, Otherwise, the converter is only able to supply reactive power to the grid. In the first step, the nominal port output voltages V_k^* are calculated with

$$V_k^* = \frac{P_k^*}{P_\mathrm{tot}^*} V_\mathrm{g} \quad \text{with } P_\mathrm{tot}^* = \sum_{k=1}^{K} P_k^* \tag{6}$$

For each port, the virtual duty cycle $D_k = V_k^*/V_{k,\max}$ is calculated. D_k describes the ratio of the expected three-phase output voltage of the port to its maximum possible output voltage and is therefore an indicator for the power reserve of the port. For stable converter operation, D_k must not exceed 1.

In the next step, the ports are sorted by D_k in descending order, so that the ports with the lowest power reserve and highest duty cycle are first in the list. The index of the sorted list is referred to as κ. The first port in this sorted list is considered first. If this port

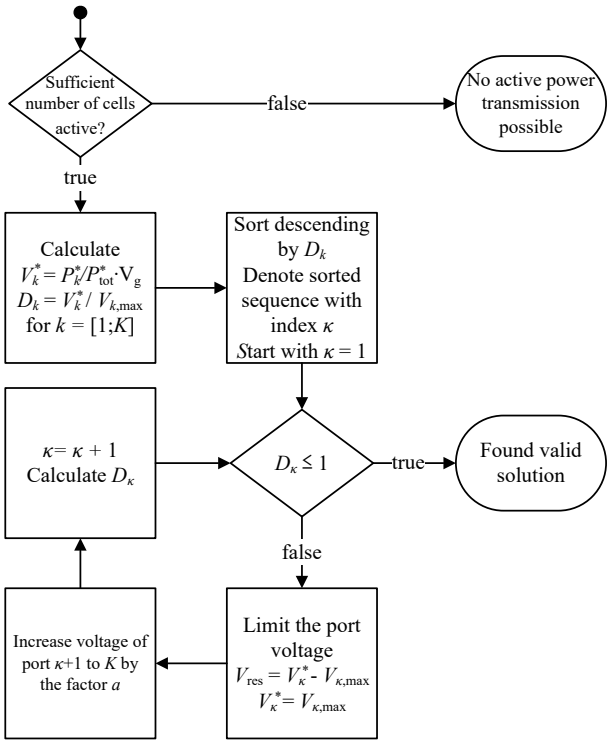

Fig. 3: Flowchart for the calculation of voltage setpoints V_k

exceeds the permissible D_κ of 1, the exceeding voltage $V_\mathrm{res} = V_\kappa^* - V_{\kappa,\max}$ is calculated and the output voltage of the port is then reduced to $V_\kappa^* = V_{\kappa,\max}$. This effectively reduces the output power of this port. In order to maintain the voltage balance of (1), the exceeding voltage V_res needs to be supplied by the ports $\kappa + 1$ to K. This is done by increasing the output voltages of these ports using

$$V_\nu^* = (1+a)V_\nu^* \quad , \nu \in [\kappa+1, K] \tag{7}$$

with

$$a = \frac{V_\mathrm{res}}{\sum_{\nu=\kappa+1}^{K} V_\nu^*} \tag{8}$$

Afterwards, the new duty cycles D_κ are calculated and the algorithm repeats with the next element of the list. The algorithm finishes successfully once $D_\kappa \leq 1$ is fulfilled, as this means that all ports comply with their maximum output voltage. This port power control can be used as part of the converter control structure, limiting the port output power setpoints P_k^* so that the converter can operate without the cell voltages permanently deviating from the nominal value.

III. Control Structure

The control structure can be divided into the control of the AC-grid side and the DC output ports, decoupled by the cell's DC-link capacitances.

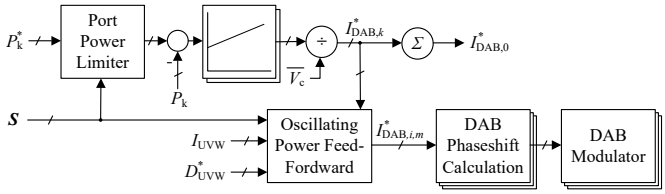

Fig. 4: Structure of the output port power control with the power limiter and oscillation power feed-forward

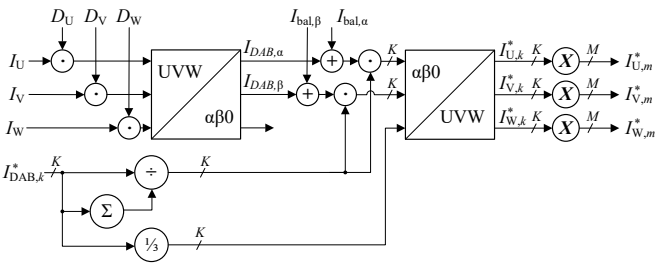

Fig. 5: Signal flow diagram of the DAB setpoint calculation with oscillating power feed forward and port output power control

A. Output Power Control

The output port control is depicted in Fig. 4. The port power setpoints P_k^* are limited using the algorithm presented in Section II-B with regard to the currently selected switch matrix $\boldsymbol{S}$. For each port, a PI-controller is used to compensate the converter losses, the non-linear converter behaviour and other disturbances. Subsequent, the necessary port output current $I^*_{\mathrm{DAB},k}$ on the input of the DABs are calculated using the mean value $\bar{V}_\mathrm{c}$ of the cell voltages $V_{m,i,\mathrm{k}}$. The setpoints for the individual DABs $I^*_{\mathrm{DAB},i,m}$ are derived by extending the oscillating power feed-forward presented in [7] to multiple output ports, which is described in more detail in the next subsection. The DAB Phaseshift Calculation calculates the necessary phase shifts for the DAB from the requested cell current $I^*_{\mathrm{DAB},i,m}$. Depending on the operation point of the DAB, either Singe Phase Shift (SPS) or Triangular Current Mode (TCM) is chosen. SPS-modulation is beneficial for unity voltage gain, while TCM allows the efficient operation in wide voltage gain operation points [8]. This enables the SST operation in a wide output voltage range, which is necessary for the direct connection to the vehicle's batteries.

B. Oscillating Power Feed-Forward

The instantaneous power on the AC side of the converter for a symmetric AC grid is described by

$$\begin{aligned} P_i(t) =& \frac{\hat{V}_\mathrm{g}\hat{I}}{2}\begin{bmatrix}\cos(\varphi)+\cos(2\omega t+\varphi)\\ \cos(\varphi)+\cos(2\omega t-\frac{2\pi}{3}+\varphi)\\ \cos(\varphi)+\cos(2\omega t-\frac{4\pi}{3}+\varphi)\end{bmatrix}\\ &-\frac{V_{\mathrm{N0}}\hat{I}(t)}{2}\begin{bmatrix}\cos(\omega t+\varphi)\\ \cos(\omega t+\frac{2\pi}{3}+\varphi)\\ \cos(\omega t+\frac{4\pi}{3}+\varphi)\end{bmatrix}\end{aligned} \tag{9}$$

, where $\hat{V}_\mathrm{g}$ and $\hat{I}$ are the grid voltage and current. φ is the phase displacement between the grid voltage and current, $\omega = 2\pi f_\mathrm{grid}$ is the grid frequency and $V_{\mathrm{N0}}(t)$ is the zero voltage component, which describes the voltage difference between the converter star point and the grid star point. The instantaneous power $P_i(t)$ consists of a constant component, a component oscillating with twice the grid frequency and a component which is dependent on the grid current and the zero voltage component. The oscillations occur due to the separation of the DC-links between the converter phases. Applying the Clarke Transformation [9] to (9) leads to:

$$P_{\alpha\beta0}(t) = \frac{\hat{I}\hat{V}_\mathrm{g}}{2}\begin{bmatrix}\cos(2\omega t+\varphi)\\ \sin(2\omega t+\varphi)\\ \cos(\varphi)\end{bmatrix} + \frac{\hat{I}V_{\mathrm{N0}}(t)}{2}\begin{bmatrix}\cos(\omega t+\varphi)\\ -\sin(\omega t+\varphi)\\ 0\end{bmatrix} \tag{10}$$

, where $P_{\alpha\beta0} = [P_\alpha, P_\beta, P_0]^T$. It can be seen that P_0 represents the active power of the converter, while P_α and P_β describe the reactive power oscillating internally between the converter phases. It is possible to use this relationship to control the active power transmitted by the DABs while also feeding forward the internal reactive power oscillations to reduce the effort required for cell balancing. Fig. 5 shows the setpoint calculation for the individual DABs. The oscillating currents $I_{\mathrm{DAB},\alpha}$ and $I_{\mathrm{DAB},\beta}$ are calculated from the measured AC grid current I_i and the duty cycle phase sum $D_i = \sum_{m=1}^{M} D_{i,m}$, where $D_{i,k}$ are the duty cycles of the individuals cells, calculated by the CHB modulator. The signals $I_{\mathrm{bal},\alpha}$ and $I_{\mathrm{bal},\beta}$ are generated by the inter-phase balancer described in the next subsection. The oscillating currents are distributed among the converter ports according to the requested active port current $I_{\mathrm{DAB},k}$. If no active power is transmitted, the oscillating currents are distributed equally between all cells. For each port, the instantaneous setpoints $I^*_{i,k}$ for each phase are calculated with an inverse Clarke Transformation. From these phase current vectors, the cell current setpoints $I_{i,m}$ are calculated by multiplication with the transformation matrix $\boldsymbol{X} = \boldsymbol{J}\boldsymbol{S}$, where $\boldsymbol{J}$ is a diagonal matrix with the reciprocal of the number of cells per port $\frac{1}{n_1}$ to $\frac{1}{n_K}$ on the diagonal axis. This transformation matrix distributes the port power equally to all corresponding cells of each port.

C. AC-Side Control

The cascaded control structure for the AC-grid side with an superimposed voltage controller and an underlaid current control in a rotating dq-reference frame is shown in Fig. 6. The voltage controller regulates the average DC-link voltage of all converter cells, generating the setpoint for d-current controller. The output current setpoint $I^*_{\mathrm{DAB},0}$ of all cells is fed forward to the d-current controller to improve the converter performance during dynamic operation point changes. The separate controller for the q-current enables the provision of reactive power to the grid. From the converter's voltage setpoint V^*_{dq}, the output voltages for the three phases are calculated. The CHB-modulator applies the Phase-Disposition Pulse Width Modulation (PD-PWM) [10] with a fixed switching frequency to generator the AC voltage. For each phase, a single CHB cell is operating in PWM-mode, while the other CHB cells have a constant output voltage, either with an active switching state or in bypass mode. The modulator uses a full sorting approach based on the cells DC-link voltage to decide whether a cell is operating in PWM, active or bypass-mode [11]. Cells with a lower cell voltage discharge less on average than cells with a higher cell voltage, resulting in an intra-phase balancing of the cell voltages. The inter-phase balancing is achieved by manipulating

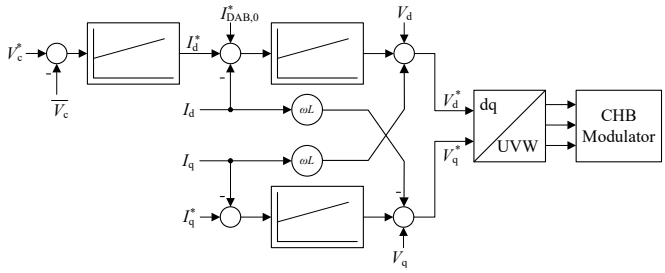

Fig. 6: Control of the AC-side with the DC-link voltage controller and the dq-current controller. $I^*_{\mathrm{DAB},0}$ is provided by the DC-side control loop

the oscillating power of the DABs depending on the DC-link voltage imbalance. To do this, the sum of the DC-link voltages $V_{\mathrm{c},i} = \sum_{m=1}^{M} V_{\mathrm{c},i,m}$ for each phase are obtained and transformed to the $\alpha\beta$-frame using the Clarke transformation. The resulting voltages $V_{\mathrm{c},\alpha}$ and $V_{\mathrm{c},\beta}$ describe the voltage imbalance between the phases that are to be reduced to zero. Two PI-controllers are used to calculate the necessary balancing currents $I_{\mathrm{bal},\alpha}$ and $I_{\mathrm{bal},\beta}$ from $V_{\mathrm{c},\alpha}$ and $V_{\mathrm{c},\beta}$, respectively. With this approach, inter-phase balancing is possible without interfering with the output power control.

Tab. I: Parameters of the simulated medium voltage converter and the low voltage laboratory prototype

Parameter	Simulation	Laboratory prototype
M	10	8
K	4	3
V_{c}	1200 V	55 V
n_k	$[3, 3, 2, 2]^{\mathrm{T}}$	$[3, 4, 1]^{\mathrm{T}}$
$P_{\mathrm{cell,nom}}$	35 kW	2.5 kW
$V_{\mathrm{DC},k}$	$[750\,\mathrm{V}, 700\,\mathrm{V}, 725\,\mathrm{V}, 675\,\mathrm{V}]^{\mathrm{T}}$	$[670\,\mathrm{V}, 700\,\mathrm{V}, 700\,\mathrm{V}]^{\mathrm{T}}$
$V_{\mathrm{g,LL}}$	10 kV	400 V
L	4 mH	1 mH
f_{sw}	10 kHz	50 kHz
C_{p}	4.5 mF	8.7 mF
C_{s}	3.5 mF	82 µF

D. Online modification of the switch matrix

During operation of the BEV charging station, the power requirements of the charging ports will vary depending on the size and state of charge of the BEV battery. In addition, if no vehicle is connected to the port, no power is required. The switch matrix should be modified according to the current power demand of the ports to increase the utilisation of the converter. It is not possible to simply change the switch matrix due to the capacitors at the output of the cell groups. Disconnecting cells from one port and connecting them directly to another port would result in very high inrush currents if the DC voltages of the ports are different. A four-step procedure is therefore proposed. First, the transferred power of the cell group to be assigned to another port is reduced to zero. Second, the cell group is disconnected from its original port. The cell group is now connected to no physical output port, but can be considered as a virtual port. As the third step, the transferred power is manipulated so that the output DC-link voltage $V_{\mathrm{DC,virt}}$ of the virtual port can be controlled. A PI-controller is then used to regulate $V_{\mathrm{DC,virt}}$ to the voltage of the port to which the cell group is to be connected. As the final step, if the difference between these two voltages is small enough, the connection can be made without exceeding the current limit of the switches.

IV. Simulation

A simulation model is used to validate the MP-SST converter control scheme. The parameters of the simulated converter, which is connected to a 10 kV AC-grid, are shown in Tab. I. The converter has 4 ports. The simulation of the electrical system is done with PLECS, while the converter control is simulated with MATLAB Simulink. The AC-grid is simulated as an ideal voltage source, the batteries connected to the charging ports are

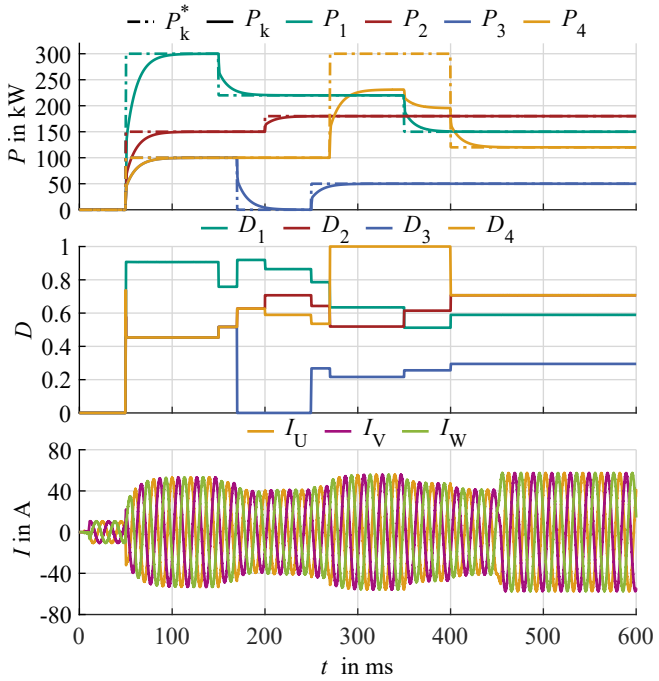

Fig. 7: Simulation results of the MP-SST showing the power control of the separate output ports and the AC-grid side behaviour of the converter

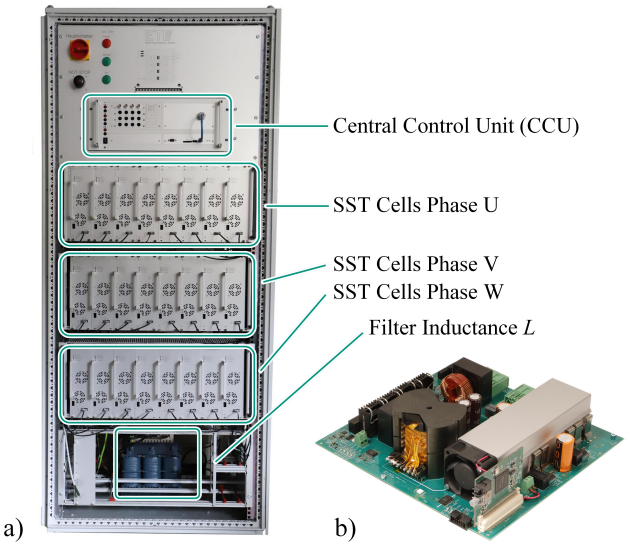

Fig. 8: a) Prototype of the MPSST converter and b) Single SST cell

modelled as voltage sources with an internal resistance. The switching and control frequency of the converter is 10 kHz. A possible charging scenario for operation with a fixed switch matrix is shown in Fig. 7. Compared to a real charging station, where each charging process will take several minutes, the scenario is speed up to reduce the simulation time required.

In the beginning, the converter is operating in idle mode. A small q-current is drawn from the grid to enable the cell voltage balancing without transferring active power. At $t = 50\,\text{ms}$, all 4 ports start to request power P_k^* (dashed line). Subsequently, the actual transferred power P_k (solid line) increases until the setpoints are reached. Simultaneously, the grid current on the AC-side increases to cope for the power drawn from the DC-side. In the following, different setpoints are requested, which the converter at first is able to fulfil. The virtual port duty cycles D_k react to the port power changes, indicating changes in the load distribution between the ports on the AC-side.

At $t = 280\,\text{ms}$, the requested power at Port 4 rises to $P_4^* = 300\,\text{kW}$. It can be seen that the transferred power is capped at 200 kW, while D_4 rises to 1. At this point, the output power of this port is limited by the AC-side of the converter. Since the port is at its AC-side voltage limit, the power of the port can only be increased by increasing the AC-side current. But this would lead to an increase of the power of the other ports, which is not allowed. If the DC-side power would be increased without an associate increase of the AC-power, this would lead to the discharging of the DC-link capacitors and thus unstable operation of the converter. The operation point is an example of a bad relative load constellation, which is expressed by the P_k^* to n_k ratio. Port 4 has the highest relative load of 150 kW per cell group, while port 3 has the smallest relative load of 25 kW per cell group. This leads to the high spread in the virtual duty cycles D_k, leading to a poor utilisation of the converter. In this case, it would be favourable to change the switch matrix so n_4 is increased while the other n_k are decreased to balance the relative load constellation. At $t = 350\,\text{ms}$, the setpoint P_1^* is reduced, which leads to a further reduction of P_4. Only after reducing the setpoint P_4^*, the converter is able to deliver the requested power. However, the cell voltages remain stable in all operation points.

V. Experimental Validation

The simulation results are validated using the scaled down laboratory prototype shown in Fig. 8. The parameters of the converter are given in Tab. I. Each phase of the MP-SST consists of eight identical converter cells shown in Fig. 8b, which incorporate power electronics, galvanic isolation, the necessary measurements and a Field Programmable Gate Array (FPGA) as the Local Control Unit (LCU).

The *ETI-SoC-System*, a modular signal processing platform based on a *Zynq™7030* System on Chip (SoC),

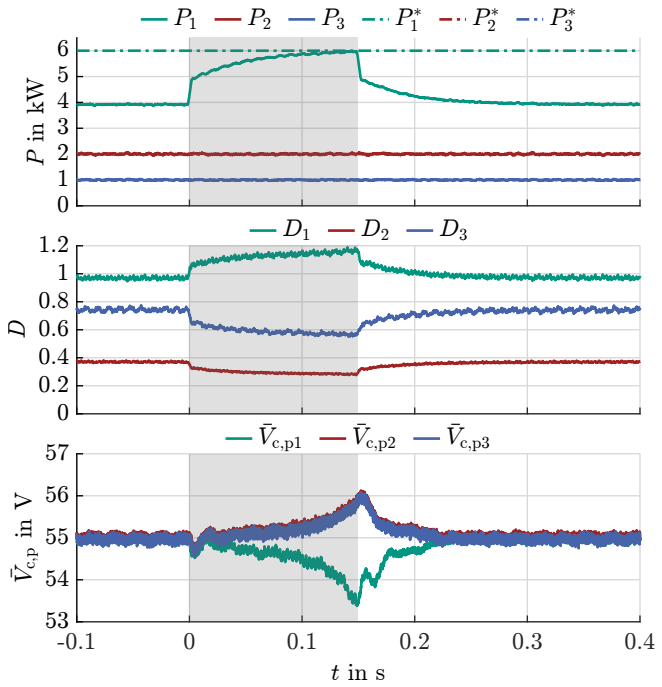

Fig. 9: Unstable converter operation when exceeding the allowed power imbalance. The port power limiter is deactivated from $t = 0$ to $0.15\,\mathrm{s}$ (highlighted region), which leads to diverging DC-link voltages.

is used as the Central Control Unit (CCU) [12]. The CCU is responsible for the system operation, sequence control and the control of the output power, cell voltage balancing and AC-side control.

The CCU communicates with the LCUs of all the converter cells via bidirectional fiber optic links. With the measured values received, the CCU calculates the set-points for the DABs and the CHB, and sends them back to the LCUs. The switching frequency $f_{\mathrm{sw}} = 50\,\mathrm{kHz}$ is chosen to reduce the size and weight of the passive components, mainly the medium frequency transformer of the DAB. Due to the high computational effort, the control system calculates the setpoints only every other switching cycle, thus reducing the control frequency to $25\,\mathrm{kHz}$.

The converter is connected to a $400\,\mathrm{V}$ low voltage AC-grid, three electronic loads are used to emulate vehicle batteries connected to the output ports.

A. Necessity of the Port Power Limiter

To verify the need for the port power limiter, the MP-SST is deliberately operated beyond its allowed power imbalance. Fig. 9 shows the corresponding measurement. Here, $\bar{V}_{\mathrm{c,p1}}$, $\bar{V}_{\mathrm{c,p2}}$, $\bar{V}_{\mathrm{c,p3}}$ are the mean values of the cells' DC-link voltages connected to port 1, 2 and 3, respectively. In the beginning, the port power limiter is activated and the converter is unable to meet the power demand $P_1^* = 6\,\mathrm{kW}$ of port 1. Instead, the power is limited to $P_1 \approx 4\,\mathrm{kW}$, as indicated by $D_1 \approx 1$. At $t = 0\,\mathrm{s}$ the port power limiter is disabled. The output power controller then increases the power of port 1 to $6\,\mathrm{kW}$, increasing the virtual duty cycle D_1 to 1.2. Therefore, port 1 should also increase its input power on the AC-side by increasing its output voltage V_1. As port 1 is already operating close to its maximum AC output voltage $V_{1,\mathrm{max}}$, no further increase is possible. So the difference in power is supplied by discharging the DC-link voltages of port 1, resulting in a decrease in $\bar{V}_{\mathrm{c,p1}}$. The converter tries to counteract this by increasing the AC-grid current I_{d}, which in turn increases the input powers of port 2 und 3, leading to rising $\bar{V}_{\mathrm{c,p2}}$ and $\bar{V}_{\mathrm{c,p3}}$. If the power imbalance is not reduced, the diverging DC-link voltages will exceed the permissible voltage, causing the converter to trigger an under- or overvoltage error of the cells. When the power limiter is reactivated at $t = 0.15\,\mathrm{s}$, the CHB modulator is able to reduce the difference between the DC-link voltages, indicating stable converter operation.

B. Output Power Control

Figure 10 shows the measurement results of the prototype for a given load scenario. The converter is operated with a fixed switch matrix. In the beginning, the converter operates in idle mode without delivering active power to the output ports. A small q-current I_{q} is necessary to enable the cell voltage balancing. The active operation of the converter starts at $t = 5\,\mathrm{s}$, when the three ports start to request powers P_k^* from the converter. Subsequently, the output power controller increases the powers P_k accordingly to fulfil the demand. Simultaneously, the AC-grid is adjusted to ensure power balance within the converter. Therefore, the d-component of the AC-grid current I_{d} rises. Since the d-component will be sufficient for the cell voltage balancing, the q-current I_{q} is reduced to zero. During the scenario, the requested power P_k^* changes several times. In the beginning, the power controller is able to follow the setpoints, which results in changes of the virtual duty cycles D_k and the AC-grid current I_{d}. The virtual duty cycles D_k stay below the threshold of 1, which indicates a sufficiently balanced load condition of the converter. At $t = 40\,\mathrm{s}$, port 1 requests $P_1^* = 5\,\mathrm{kW}$. However, the converter is only able to increase the power of port 1 to $P_1 = 4\,\mathrm{kW}$, which increases the virtual duty cycle D_1 to 1. As explained in Section V-A, a further increase of the output power P_1 would lead to diverging DC-link voltages, which will result in an unstable operation.

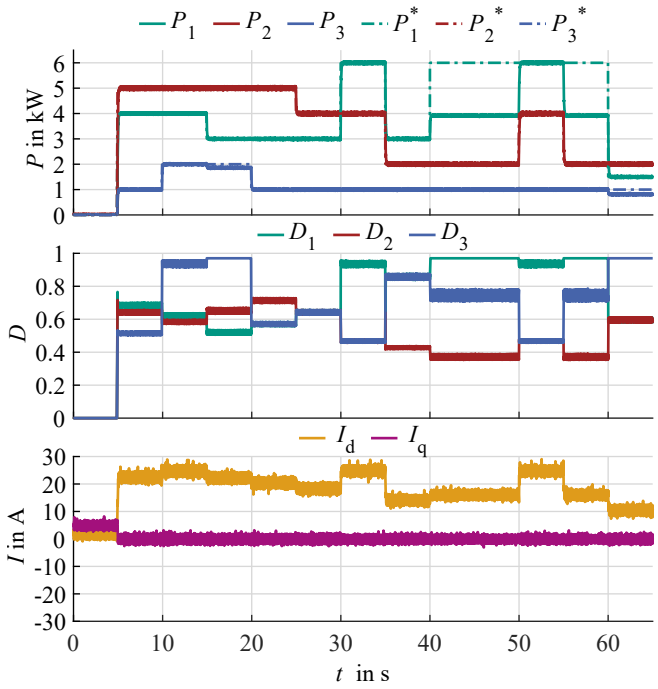

Fig. 10: Measurement Results for the low voltage prototype with $M = 8$ cells per phase and three separately controlled output ports.

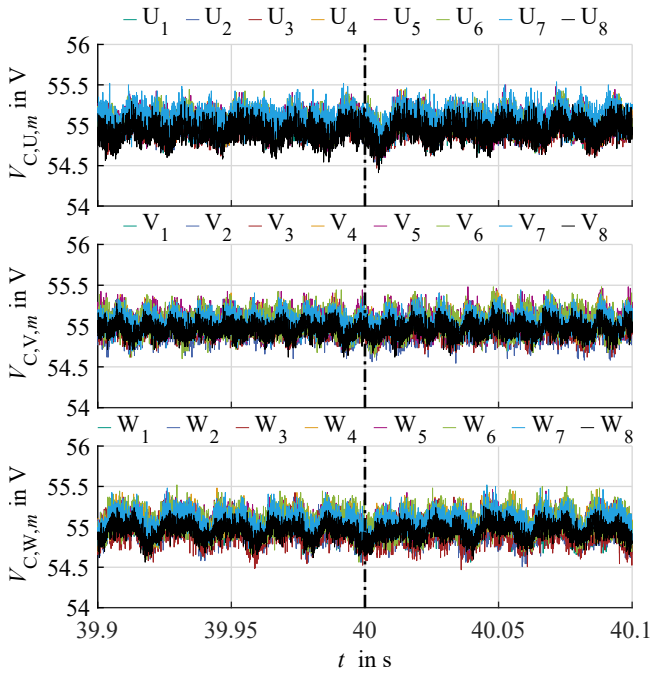

Fig. 11: CHB Cell voltages during an operation point change at $t = 40\,\mathrm{s}$ (dashed line). The envelope of the voltage ripple shows a $2f_{\mathrm{grid}}$-periodicity.

When the requested power P_2^* is increased to $4\,\mathrm{kW}$ at $t = 50\,\mathrm{s}$, the power distribution between the ports is changed, as indicated by the change of the virtual duty cycles D_k. Due to reduced power imbalance, the converter is able to supply the full requested power to all three ports. Similiar power limitations occur during the interval $t = 55 - 60\,\mathrm{s}$ at port 1 and $t = 60 - 65\,\mathrm{s}$ at port 3. The online reconfiguration of the switching matrix could have reduced the impact of the power limitation by reducing the power imbalance through optimized interconnection of the cell groups.

The DC-link voltages of the converter cells are shown in Fig. 11. The graph shows a small section of the measurement of Fig. 10 during the operation point change at $t = 40\,\mathrm{s}$. A voltage ripple of $\pm 0.5\,\mathrm{V}$ around the nominal value of $\bar{V}_{\mathrm{C}} = 55\,\mathrm{V}$ is observed. At $t = 40\,\mathrm{s}$, a small temporary drop of the DC-link voltages is visible, which is caused by the operation point change. The feedforward control suppresses low-frequency harmonics of the cell voltage ripple by distributing the power of the ports to the phases according to the current AC-grid angle. Within the cells of a phase, the feedforward control assumes that the power is distributed evenly between the cells of the port. However, as only one cell per phase is operated with PWM in one modulation period, this assumption is only correct for the average over several periods. The resulting short-term power imbalance leads to the high-frequency ripple in the cell voltage. The envelope of the ripple shows a periodicity of $100\,\mathrm{Hz}$, which correspondents to twice the grid frequency.

C. Online Reconfiguration of the Switch Matrix

Fig. 12 shows the online reconfiguration of the switch matrix. In the beginning, the converter is not able to fulfil the requested charging power $P_k^* = [5, 1, 1]\,\mathrm{kW}$ due to the disadvantageous switch matrix configuration $n_k = [3, 4, 1]$. This operation point would exceed the converters imbalance capability, therefore the output power is capped to $P_1 = 2.5\,\mathrm{kW}$ and $P_3 = 800\,\mathrm{W}$, while P_2 reaches the demanded value. At $t = 0\,\mathrm{s}$, a reconfiguration of the switch matrix is triggered. To reduce the converters imbalance, two cell groups from port 2 are switched to port 1. As described in Section III-D, the reconfiguration is initiated by reducing the cell group's power to zero and disconnecting the two cell groups from port 2. Since the DC output voltage of port 1 $V_{\mathrm{port},1} = 670\,\mathrm{V}$ is different from the DC output voltage of port 2 $V_{\mathrm{port},2} = 700\,\mathrm{V}$, the DC output voltage of the cell group needs to be reduced to $V_{\mathrm{DC,virt}} = 670\,\mathrm{V}$ prior to establishing the connection with port 1. Otherwise, the connection of the differently charged output capacitances of the different converter cell groups would result in unacceptably high inrush currents. After the voltages are

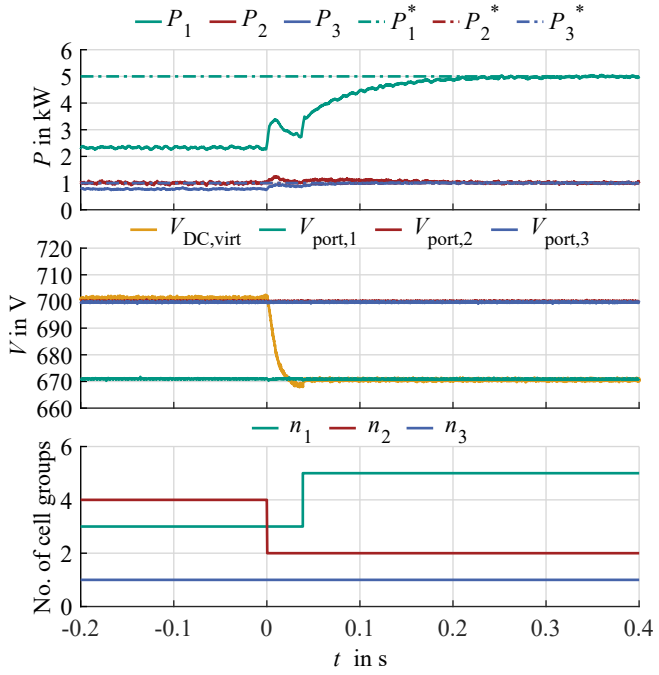

Fig. 12: Measurement of the online reconfiguration of the switch matrix. Two Cell groups connected to port 2 are switched to port 1 to optimise the output power

aligned, the connection is established at $t = 50\,\mathrm{ms}$. After the reconfiguration is finished, the converter is able to provide the requested charging power $P_1^* = 5\,\mathrm{kW}$ and $P_3^* = 1\,\mathrm{kW}$ without exceeding its imbalance capability. The reconfiguration process including the adaption of the output power is finished after $200\,\mathrm{ms}$. Compared to the charging time of electric vehicles, this switching time is sufficiently short. It is therefore possible to use the MP-SST with the dynamically reconfigurable switch matrix for this application.

VI. Conclusion

This paper presented the steady state analysis and control concept of a MP-SST, which connects multiple DC charging ports directly to the MV-AC grid. Under the assumption of a sufficient voltage reserve of the converter, the concept enables an independent output power control. When operating with limited voltage reserve, even challenging load imbalances can be managed by online modification of the switch matrix to ensure optimal power supply to the output ports. Simulation data and measurement results using a low voltage prototype validate the presented control concept.

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