IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 5 March 2025, accepted 6 April 2025, date of publication 10 April 2025, date of current version 22 April 2025.

Digital Object Identifier 10.1109/ACCESS.2025.3559218

RESEARCH ARTICLE

On-Chip CMOS Shorted Bow-Tie Antenna Enhanced by 3D Printed Parasitic Resonator Operating Around 246 GHz

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This work was supported in part by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) through the Project Adaptive Millimetre-wave Integrated Systems (ADAMIS) under Grant 394221495, in part by BMBF through the Program Forschungslabore Mikroelektronik Deutschland (ForLab) under Grant 16ES0948, in part by DFG via the Excellence Cluster 3D Matter Made to Order under Grant EXC-2082/1-390761711, in part by the European Research Council (ERC) Consolidator Grant through the project TeraSHAPE under Grant 773248, in part by the Bundesministerium für Bildung und Forschung (BMBF) Project Open6GHub under Grant 16KISK010, and in part by Karlsruhe School of Optics and Photonics (KSOP).

ABSTRACT This work describes the design process, manufacturing, and measurement of an antenna system consisting of an on-chip feeding element enhanced by 3D printed parasitic resonators operating around 246 GHz. The antennas are intended to be fed by the differential output of a wideband binary phase shift keying (BPSK) transmitter. The state-of-the-art is evaluated, and multiple possible complementary metal-oxide-metal (CMOS) back-end of line (BEOL) antenna structures are identified and compared against each other. The best option, in the form of a shorted bow-tie antenna, is selected. A parasitic resonator structure based on 3D printing and metallization is designed and improved using common mode analysis. The design and optimization process is detailed and explained. The realized designs are measured and compared against a similar concept using metallic resonators on a glass substrate as parasitic resonators. This is the first demonstration of a direct 3D printed structure on a CMOS antenna operating around 246 GHz.

INDEX TERMS 3D printing, mmWave antennas, antenna measurement.

I. INTRODUCTION

Current developments in mobile communication and sensing push for more applications within the sub-THz spectrum ranging from 100 GHz to 300 GHz. This range offers multiple windows in the atmospheric attenuation, lending themselves for wideband, high-data-rate communication systems and precision sensing. While semiconductor technology has matured enough to conquer the frequency range, packaging and antenna solutions have to catch up.

The wavelength within the frequency range is still too large for efficient antenna designs on the thin metal stack-ups present in most complementary metal-oxide-metal (CMOS) or silicon-germanium (SiGe) processes. Simultaneously, established thick-film processes used for printed circuit board (PCB) manufacturing are at their technological limit, realizing the necessary structures. Another packaging concept reaching maturity is embedded-wafer level ball grid array (eWLB), showing great promise [1]. However, it faces issues due to the low number of available metal layers and tight constraints on the assembly process. Hence, an interest in enhancing the performance of on-chip antennas is present [2], [3].

Multiple approaches were presented before to enhance on-chip antennas. One is using an external lens, either silicon or dielectrics; see [4] and [5]. Other approaches

The associate editor coordinating the review of this manuscript and approving it for publication was Kai-Da Xu.

TABLE 1. State-of-the-art of on-chip differential antennas.

Ref.	[7]	[13]	[14]	[14]	[15]	**This work**	**This work**
Type	Dipole antenna with backside reflector	Dipole with bondwires	Half cloverleaf	Slot bow-tie	Vivaldi like	Shorted bow-tie with 3D resonator	Shorted bow-tie with glass resonator
Gain in dBi	4	2	3	4	1.2	4.4	2.1
Bandwidth in GHz	25	20	65	80	23	75	62
Relative Bandwidth	19.6%	12.5%	34.6%	44.5%	23.2%	28.5%	24.7%
Center Frequency in GHz	127.5	160	187.5	180	178.5	262	251
Surface Area in mm^2	-	0.6	0.84	0.6	0.35	0.64	0.64
Backside Reflector	Yes	No	Yes	Yes	Yes	No	No

use dielectric resonator antennas [6]. Another approach to overcome the thin substrates present in the back-end of line (BEOL) is using the thickness of the bulk substrate to realize a backside reflector [7]. Lastly, some approaches use parasitic patches to enhance the bandwidth using thin film processes [8], [9].

A differential antenna is sought for a binary phase shift keying (BPSK) transmitter presented in [10]. This work investigates using 3D printing to enhance an on-chip differential feeding element to be used with the BPSK transmitter. Reference [11] showed an approach to selectively metalize the 3D printed structure with the help of printed shadowing structures. Utilizing this technique, two different 3D printed parasitic resonators are designed. Due to the direct print on the surface of the chip, complicated and precise positioning and attachment of separately manufactured parts is not necessary. For comparison, a classical thin film parasitic patch is fabricated as well. To the authors' knowledge, this is the first work presenting a directly printed metallic resonator antenna on-chip operating around 250 GHz with a differential feed.

The paper is structured as follows: First, the feeding element on chip is discussed and designed. Next, the parasitic resonator design is explained and analyzed. It is followed by the fabrication and measurement of the three designs presented in this work.

II. ON CHIP FEEDING ELEMENT DESIGN

The targeted application necessitates a differential antenna with a bandwidth of at least 50 GHz centered around 246 GHz, which equates to a 20% relative bandwidth. Radiation through the bulk silicon is avoided to simplify the interconnect and packaging. Tab. 1 overviews previously published differential antennas on chip and a coplanar waveguide (CPW)-fed slot bow-tie antenna. The thin substrate limits the achievable performance of on-chip antennas without external enhancing elements. The realized gain is consistently low with a maximum reported value of 4 dBi. Designs using the microwave monolithic integrated circuit (MMIC) thickness to integrate a backside reflector report issues with the final thickness and resulting shifts in center frequency. The slot-bow tie reports the best bandwidth for the smallest size from all antennas. However, it does not fit the differential feed requirement but indicates a good starting point for the on-chip feeding element.

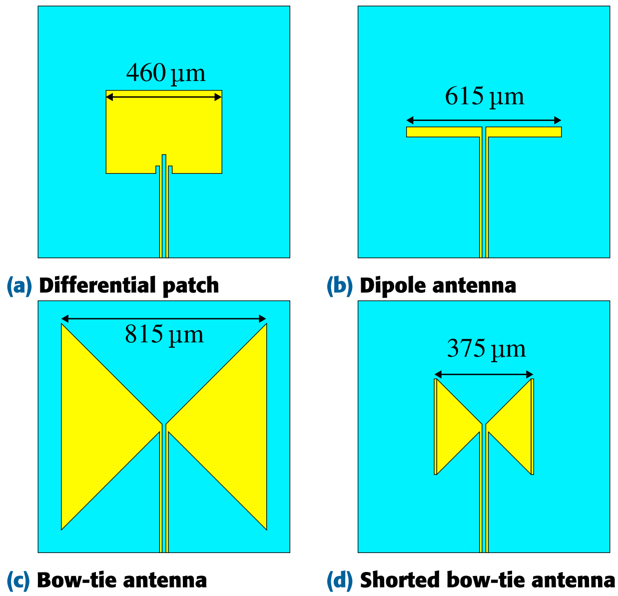


FIGURE 1. Simulated layouts of possible on-chip wideband differential antenna geometries without backside reflector.

Using the state of the art, possible candidates for on-chip wideband differential feeding elements without backside reflectors are evaluated. Four candidates are considered, which are the simple dipole antenna [7], differential patch antennas [9], and a bow-tie antenna [12] without and with a short at the end. The geometries of the possible antennas with their simulated dimensions are shown in Fig. 1.

All four antennas shown in Fig. 1 are simulated in *CST Microwave Studio* and evaluated for their initial behavior without an external resonator. These results are plotted in Fig. 2. The simulations themselves show poor matching and radiation efficiency, which is to be expected due to the thin stack-up and the lack of a resonator. At this step, only the qualitative difference between the four tested antennas is evaluated.

The patch antenna is matched at a single frequency, making it unsuitable for the desired application. Of the three dipole-type antennas, the normal bow-tie antenna achieves the highest radiated power. However, it shows a narrow band peak. The best option is the shorted bow-tie antenna, showing consistent wideband radiation and matching. Due to the short at the end of the bow tie, the width of the antenna is halved, reducing the size of the antenna [16].

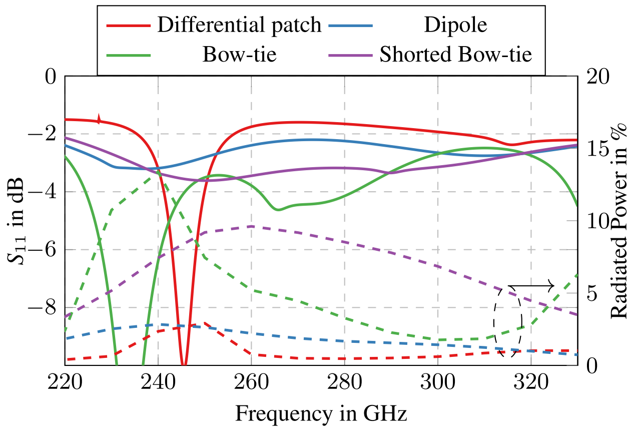
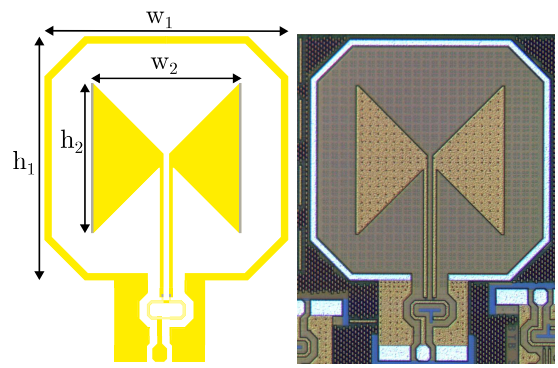


FIGURE 2. Simulated input match and radiated power of the four tested feeding elements without resonator.



(a) Layout **(b)** Fabricated chip with balun

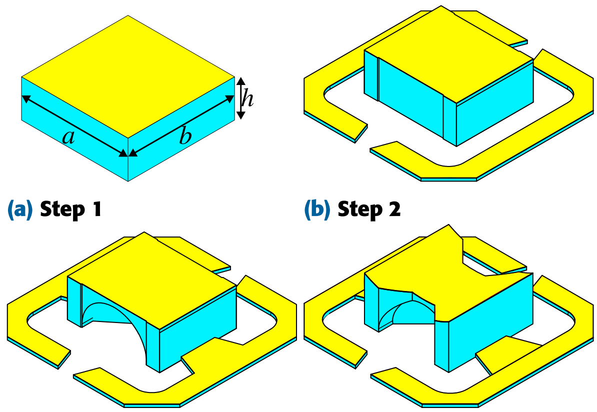
FIGURE 3. Layout and chip micrograph of the realized bow-tie antenna.

Based on this result, the final on-chip feeding element is designed. The antenna flares outwards at a 45° angle for maximum bandwidth. Further, a ground wall is drawn around the antenna to give a deterministic boundary for the field within the chip itself. Fig. 3 shows the layout and realized chip. An on-chip Marchand balun is used to probe the differential antenna with single-ended probes for measurement. The width and height of the overall antenna is $w_1 = 800\,\mu\text{m}$ by $h_1 = 800\,\mu\text{m}$ and the antenna elements themselves are $w_2 = 400\,\mu\text{m}$ by $h_2 = 400\,\mu\text{m}$.

III. RESONATOR DESIGN AND OPTIMIZATION

To improve the feeding element from the currently poor performance, a parasitic metal structure is introduced. This feature is implemented using 3D printing of a base structure and a metallization step. Using the process shown in [11], many design freedoms can be utilized. However, the process has limits; for example, metalized 90°-walls are not possible.

A simple rectangular metal patch is assumed to be the starting point for the parasitic resonator. It is tuned in width, length, and substrate height to give the best initial solution.



(a) Step 1 **(b)** Step 2 **(c)** Step 3 **(d)** Step 4

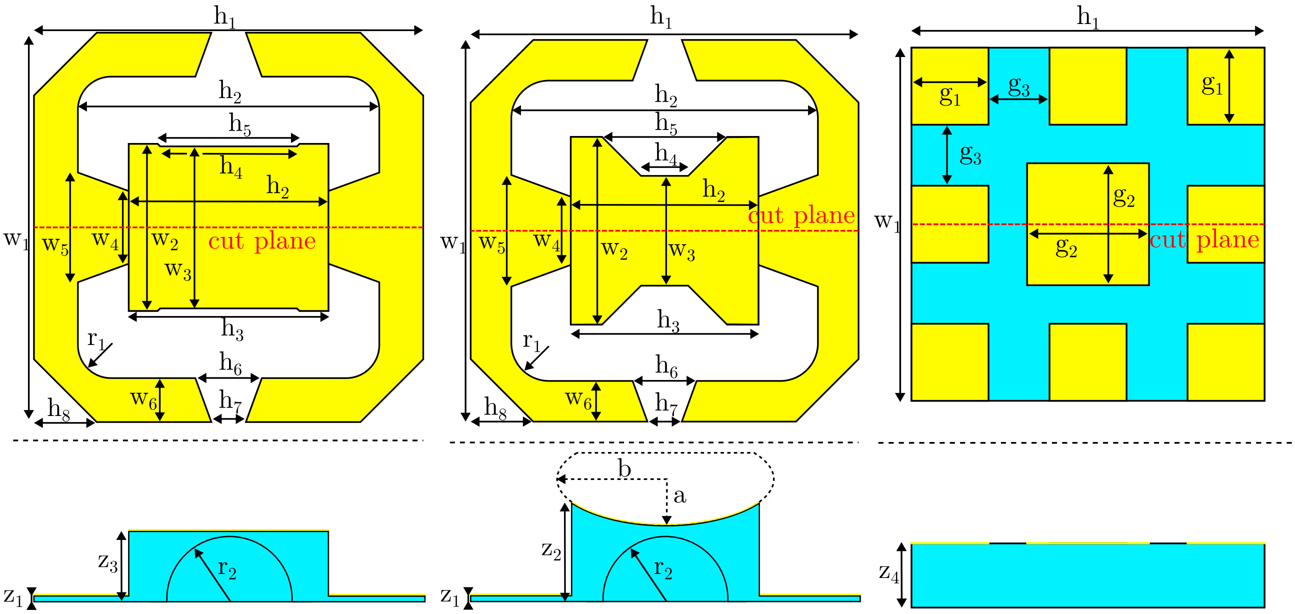
FIGURE 4. Step-by-step improvement of the resonator layout by employing common mode analysis to identify unwanted modes and implementing measures to compensate them.

The initial design is shown in Fig. 4(a). The value for a is $250\,\mu\text{m}$, b is $250\,\mu\text{m}$ and h is $100\,\mu\text{m}$.

With this initial step, a characteristic mode analysis (CMA) is performed to analyze possible modes of excitement. The analysis yields multiple strong possible modes due to the square structure of the patch as shown in Fig. 6(a) to Fig. 6(b). Elongating one side helps in suppressing some of the undesired modes. Further, a split ring on a lower height is added to suppress the excitement of the corners, yielding the structure shown in Fig. 4(b). Simulations of this improved structure show that a mode exists where only the lower split ring is exited as shown in Fig. 6(e), while the desired mode is shown in Fig. 6(d). Another, less relevant mode is possible where the power is concentrated in the dielectric of the center resonator, shown in Fig. 6(f). Indents to the ring close to the center resonator are added to suppress the unwanted mode, yielding the structure shown in Fig. 4(c), the final form of the first resonator design with the resulting field distribution shown in Fig. 6(g).

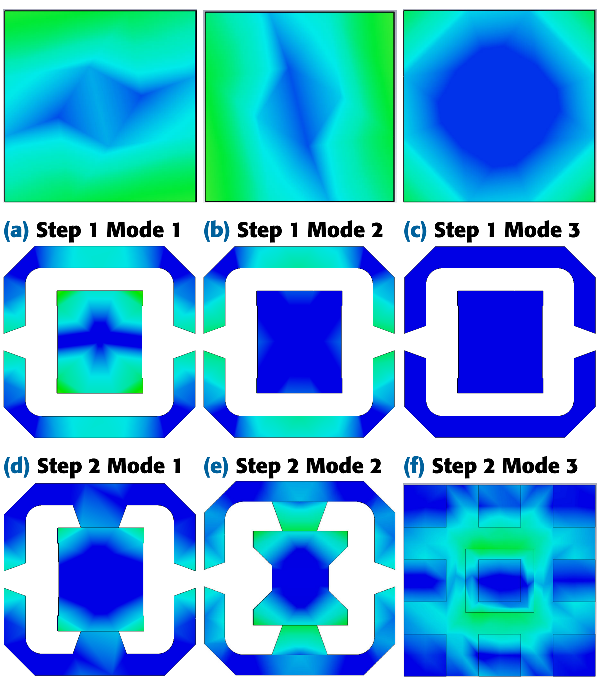
To improve the design further, the 3D printed substrate block is hollowed out to reduce dielectric losses and keep the impedance of the feeding microstrip line on the chip constant. The central resonator is optimized further to improve the structure and profit from the possibilities of 3D printing. By adding indents on the rectangular resonator at the center, the field strength in the metallization is better controlled. Lastly, the top side is curved in an elliptical shape. The final structure of the second resonator is shown in Fig. 4(d) and the resulting field distribution shown in Fig. 6(h).

As a comparison, a different approach using parasitic patches on a glass substrate is shown in Fig. 6(i), which was first presented in [17]. The design is fabricated by sputtering a gold layer on a glass sheet, which is then structured using a pico-second laser system. The resonator is glued in place manually on the same feeding element shown in Fig. 3. The final structures are shown in Fig. 5, and their design values are given in Tab. 2.



(a) **Design 1** **(b)** **Design 2** **(c)** **Design 3**

FIGURE 5. **Top and side view of the three different resonators designed.**



(a) **Step 1 Mode 1** **(b)** **Step 1 Mode 2** **(c)** **Step 1 Mode 3**

(d) **Step 2 Mode 1** **(e)** **Step 2 Mode 2** **(f)** **Step 2 Mode 3**

(g) **Step 3 Mode 1** **(h)** **Step 4 Mode 1** **(i)** **Glass Resonator**

FIGURE 6. **Electric field strength distribution over the four iterations of the resonator and different significant modes as well as a classical 9 element metallic parasitic resonator.**

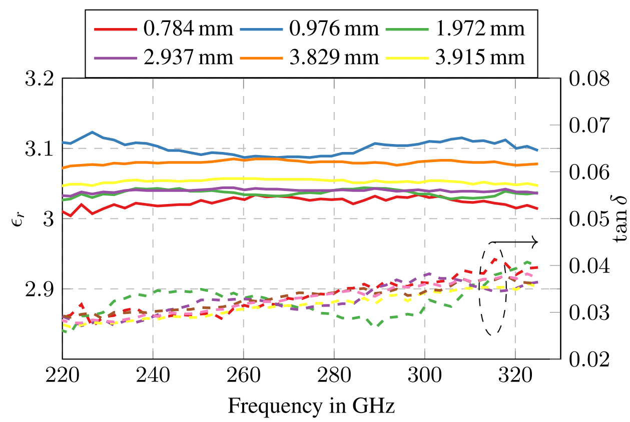


FIGURE 7. **Measured dielectric properties for the 3D printing resin for various thicknesses.**

The 3D printed dielectric is made of *HTL resist* manufactured by *Boston Micro Fabrication (BMF)*. The material measurements of the resin are shown in Fig. 7 and show an average ϵ_r of 3.05 and an average $\tan\delta$ of 0.035 up to 330 GHz. The resin is measured with a *SwissTo12* waveguide-based dielectric measurement jig with samples of different thicknesses. The thickness of all samples were measured after printing for their final value and given also in Fig. 7. This resin is not optimized for RF applications, which results in a high-loss tangent compared to the silicon dioxide of the CMOS BEOL or high-purity alumina. However, it fairs comparably well against other polymers currently used in 3D printing and high-frequency applications [18].

3D printing enables many options to reduce the amount of dielectric used, minimizing losses in the dielectric. Hence, a strong motivation is given to optimize the structure. In order to quantify the possible gain in the present design, the loss contribution of all components is considered. To evaluate the different materials influence, a complete antenna assembly simulation is done in *CST Microwave Studio*. The metal

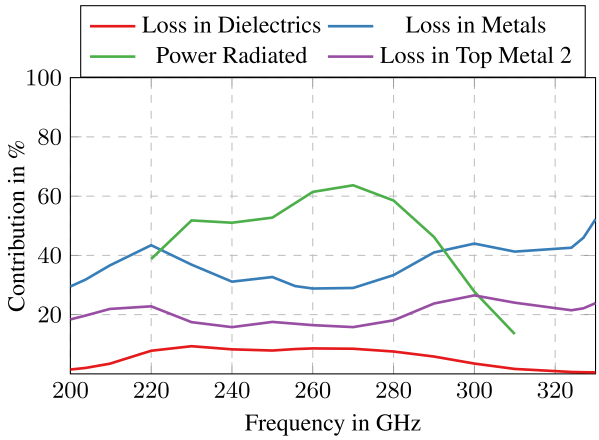


FIGURE 8. Simulated percentage of radiated power and losses in dielectrics and metals.

TABLE 2. Design values of the antennas.

Design 1		Design 2		Design 3	
Par.	Value	Par.	Value	Par.	Value
w_1	266 µm	w_1	620 µm	w_1	550 µm
w_2	266 µm	w_2	300 µm	h_1	550 µm
w_3	258 µm	w_3	180 µm	g_1	120 µm
w_4	116 µm	w_4	109 µm	g_2	190 µm
w_5	175 µm	w_5	178 µm	g_3	95 µm
w_6	70 µm	w_5	65 µm	z_4	100 µm
h_1	620 µm	h_1	620 µm		
h_2	480 µm	h_2	490 µm		
h_3	318 µm	h_3	300 µm		
h_4	218 µm	h_4	318 µm		
h_5	226 µm	h_5	318 µm		
h_6	107 µm	h_6	102 µm		
h_7	55 µm	h_7	55 µm		
h_8	100 µm	h_8	100 µm		
r_1	53 µm	r_1	60 µm		
r_2	109 µm	r_2	100 µm		
z_1	10 µm	z_1	10 µm		
z_3	113 µm	z_2	156 µm		
		a	180 µm		
		b	250 µm		

thickness on the resonator is assumed to be 600 nm of copper, which is a typical value for the e-beam physical vapor deposition (PVD) process used. Extracting the losses per material gives the plot in Fig. 8. The dielectric losses are the smallest loss contribution, with about 10% of power dissipated. Much more detrimental to the overall efficiency are the losses in the metals, especially the loss in the topmost metal layer of the BEOL stack with close to 20%. The loss of Top Metal 2 is included in the blue curve for the loss in the metals. Hence, only marginal efficiency gains can be achieved by adding voids to the structure. Hence, no further optimization of the structure above the already mentioned aspects are considered.

IV. MANUFACTURING

The shorted bow-tie feeding element is realized in the BEOL process of *IHPs* 130 nm *SG13G2* technology using top metal

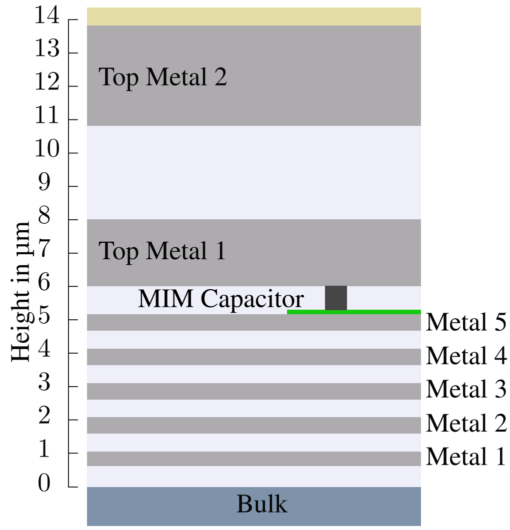
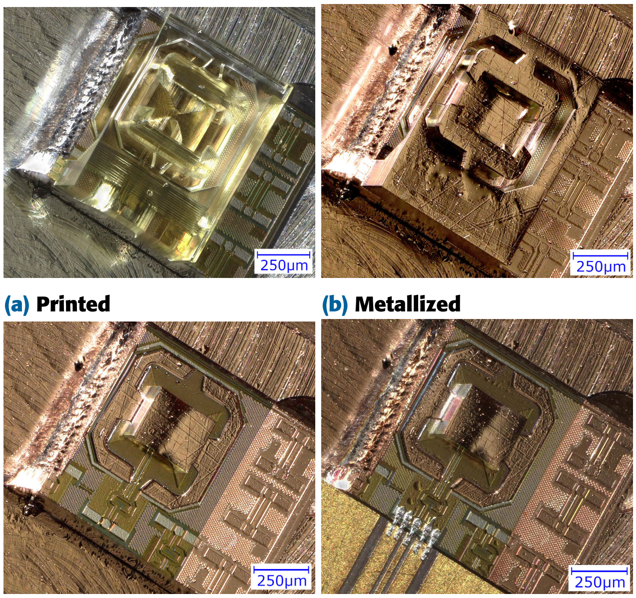


FIGURE 9. To scale cross section through the used CMOS stackup.

2 for the bow-tie element and feed lines and metal 2 for the ground plane. The stack-up is shown in Fig. 9. The distance between top metal 2 and metal 2 is 8.74 µm. To ease the integration into a system and give a well-defined border for the antenna, a ground wall is placed 100 µm around the antenna itself. The chip micrograph is shown in Fig. 3(b). The antenna is built in two versions: The first is directly connected to an on-chip balun to ease measurements and is shown here. A second version has a differential pad presented in [19] and is used in [17].

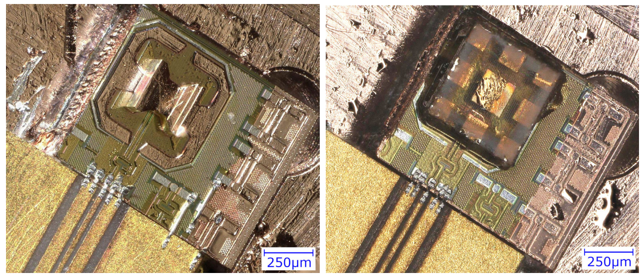
In order to 3D print on the antenna the chips are glued to a carrier. This carrier is mounted into a *microArch S130*, *BMF Boston Micro Fabrication* projection micro-stereolithography (PμSL) 3D printer. This machine can project features down to 2 µm in x- and y- direction with a 1 µm resolution of the mechanical stage. The height of each layer is at a minimum 5 µm. The alignment of the 3D printed structure is done with the integrated vision system, utilizing the same illumination system and optics based on a 405 nm UV LED at below-threshold exposure values. After alignment, the resonator structure and the shadowing structures are printed in one go. The antenna is small enough to avoid lateral stitching of the single projection print fields, which are 3.84 mm by 2.16 mm in size. After printing, unexposed photo-resist is removed in a development process by rinsing the sample in isopropyl alcohol (2-propanol) for 10 minutes, followed by a UV post-exposure at a temperature of 65 °C for 5 minutes. The antenna with the 3D printed structure is shown in Fig. 10(a).

Following the curing step, the metallization is applied. For this highly-directive metal coating, an electron-beam PVD process is used in a *Leybold GmbH Univex 400* machine at a pressure of $<$0.8 mPa. The first layer is an aluminum adhesion layer with a thickness of 30 nm. Next, the main layer of copper is applied. To passivate the surface, another titanium layer is deposited as a diffusion barrier and



(a) Printed **(b)** Metallized **(c)** Without Shadowing **(d)** Final Assembly

FIGURE 10. The different manufacturing steps of the 3D printed antenna.



(a) Design 2 assembled **(b)** Design 3 assembled

FIGURE 11. Micrograph of the assemblies of design 2 and 3.

finished with a thin gold layer. The final thickness is around 600 nm. The sample after the metallization step is shown in Fig. 10(b). After metal deposition, the shadowing structures of the antennas are removed manually, revealing the physical structure. This is shown in Fig. 10(c).

During the integrated circuit (IC) design stage a decision was made to place the ground-signal-ground (GSG)-pad close to the antenna itself to conserve chip area and hence, costs. However, as shown in [20], the used wafer probes radiate significantly and influence the antenna pattern measurement. In an attempt to alleviate this issue, 10 mm of CPW line on alumina is connected to the probe pad via bond wires to move the probe further away from the antenna. The CPW loss is measured separately and removed from the measurement results. While this helps reduce the influence of the wafer probes, the CPW line and the bond-wire transition add issues to the measurement. In order to keep the distance between the pad and the CPW short, the edges of both the IC and CPW lines are carefully ground down to a perfect 90° angle. Grinding the samples allows a minute gap of less than 10 μm. The distance is bridged with 17 μm of aluminum bond wire. The final assembly is shown in Fig. 10(d). The alumina of the CPW has a thickness of 244 μm while the IC has a thickness of 300 μm. To compensate for the height difference, a metal shim is laser cut and glued with conductive die-attach film underneath the CPW line. This yields a maximum height difference of 5 μm. The final assembly of the other two designs is shown in Fig. 11(a) and Fig. 11(b).

V. MEASUREMENT

All samples are measured using a free space antenna measurement setup shown in Fig. 12. A *VDI VNAX-WR3.4* transmit-receive (T/R) module stimulates the samples using a *GGP PicoProbe 325B* on-wafer air-coplanar (ACP) probe. The receiver is a *VDI MixAMC-I WR-3.4* fundamental mixer. The distance between the antenna under test (AUT) and the receiver is 68 cm. The system is calibrated using the known antenna method [21].

Measurement of the samples proved difficult and was limited by the measurement equipment and available measurement setups. A principal issue of probe-based antenna measurements is the interaction between the antenna and the probe itself [22], [23]. Investigations on this issue in lower frequency ranges with modified on-wafer probes did not improve this issue [24]. Another approach is the use of mathematical calculations to suppress the reflections, such as the mathematical absorber reflection suppression (MARS) method [25]. Other approaches employ time gating to remove such reflections [26]. However, these methods necessitate precise phase information and oversampling of the spatial domain to reconstruct the different radiation centers [27]. Translating the phase accuracy into the spatial domain results in a positioning accuracy requirement of better than 33 μm to limit the phase uncertainty below 10°, which is not feasible due to vibration, air movement, and thermal expansion. Hence, these methods cannot be employed to reconstruct the antenna pattern at sub-THz frequencies with the current measurement setups.

An alternative measurement approach using non-contact reflection type measurements was demonstrated in [28]. While it shows great promise, it also introduces challenging requirements. Multiple samples with deterministic terminating impedance have to be manufactured. The manufacturing differences between the samples must be controlled and minimal enough to prevent mathematical artifacts and unreasonable result uncertainty. Due to the economics of CMOS chip production, multiple samples with different terminating impedances could not be realized. Hence, this approach is ruled out.

Thus, to extract the most information from the limited measurements, two simultaneous approaches are used. Firstly, we simulate the physical setup thoroughly to use it in a qualitative assessment of the measured results. By decompositioning the physical effects we can determine that the measured data to be a result of a working antenna.

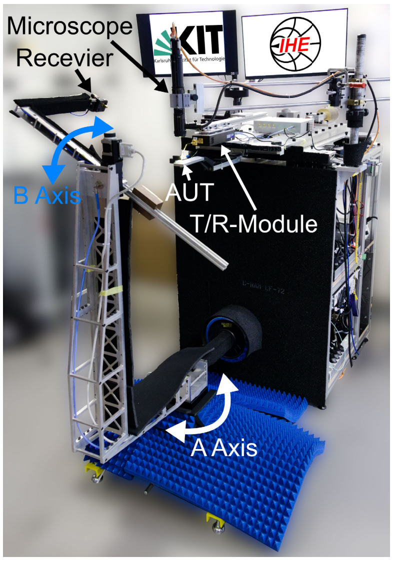


FIGURE 12. Photograph of the used antenna measurement setup.

Lastly, to make the results more readable the measured patterns are filtered in the 2D Fourier domain to reduce as much effects as we reasonably can. The lost energy of this filtering step is calculated using Parsevals Theorem and the results are corrected for it.

The interaction between probe and antenna is reduced by introducing the feeding line. In this configuration the measured input return loss is the superposition of multiple effects, that are challenging to control and evaluate without destroying the samples. Hence, the input match measurement is omitted from further analysis. As a reference, the simulated values are shown in Fig. 13. Both designs 1 and 2 show similar input match values. However, design 2 extends further down to lower frequencies ranging from 220 GHz to 272 GHz. Design 3 achieves a wider input match bandwidth from 220 GHz to 294 GHz.

The CPW lines that feed the AUTs are measured on a wafer prober using two *VDI VNAX-WR3.4* T/R modules and *GGB PicoProbes 325B* ACP probes. The results are shown in Fig. 14. The match stays below −10 dB for almost the whole band and only exceeds this above 310 GHz. The insertion loss is between −8.3 dB to −12.6 dB at 330 GHz. This yields a worst-case loss of 1.2 dB mm^{-1}, which is in line with the simulation. Although the loss is quite high with more than 10 dB, it is within the dynamic range of the measurement system and can be calibrated afterward.

Measuring the feeding bow-tie itself, as shown in Fig. 3(b), showed severe limitations due to probe and transition radiating as described in [20]. With an expected realized gain of less than −4 dBi for the shorted bow-tie feeding element itself and a feeding loss of about 10 dB, the radiated power is in the same range as the probe radiation itself [20]. Hence, the measurement is dominated by the probe radiation, which was observed. While this did not yield any direct result about the feeding element, it showed that it does behave as expected.

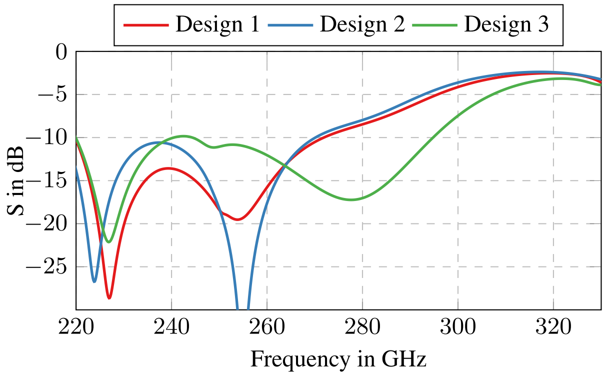


FIGURE 13. Simulated input match of the tree designs.

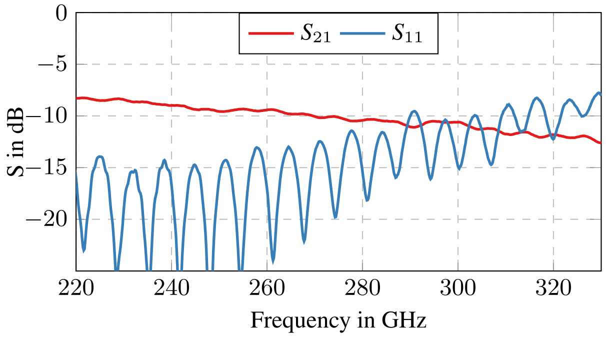


FIGURE 14. Measured insertion loss and reflection of the feeding CPW line.

A. DESIGN 1

The first design shown in Fig. 5(a) is measured. Fig. 15 shows the pattern in the E-plane, and Fig. 16 shows the pattern in the H-plane. The CPW line loss is de-embedded from the measured gain. In the E-plane, a good match between simulation and measurement is achieved for 240 GHz and 260 GHz while the pattern at 220 GHz is severely reduced. This effect can be observed in the H-plane as well, although it becomes apparent, that the lower frequency is more heavily influenced by the probe body. The plot of the gain over frequency shows an overall reduced gain, which can be explained by a shift in the pattern through the probe body. In the H-plane plot the pattern peaks at −55° while it loses energy at boresight. The increase in gain with frequency can be observed. Both samples measured show a very similar behavior over frequency, indicating a good repeatability of the process. Sample 2 shows, however, deviations for low frequencies and a higher gain at 250 GHz and 275 GHz, indicating that the issues at these frequencies lie within the bond-wire transition and not the resonator structure. The peak gain at boresight is 4.4 dBi at 275 GHz. Depending on the measurement a 3 dB bandwidth of 75 GHz is observed with a simulated bandwidth of around 80 GHz.

B. DESIGN 2

Next, the second design with the curved resonator is measured. The results of the E-plane and H-plane are shown in Fig. 18 and Fig. 19. The measured pattern deviates

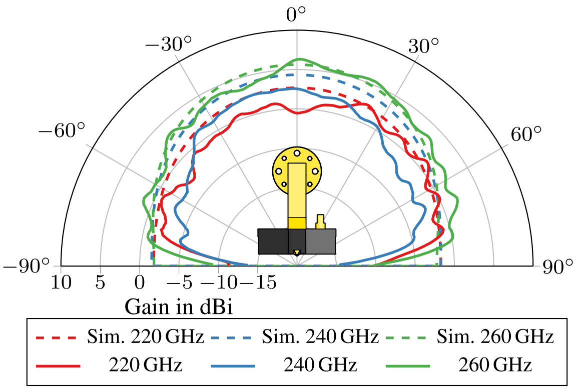


FIGURE 15. E-plane field pattern of design 1.

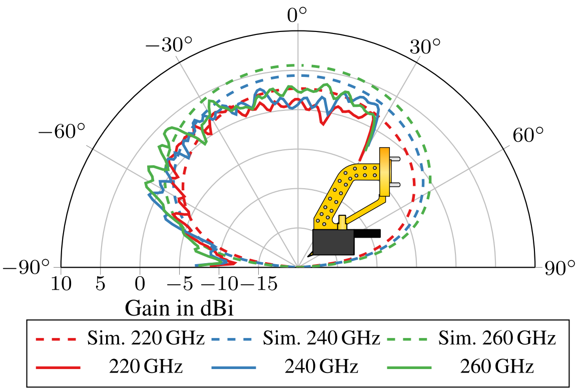


FIGURE 16. H-plane field pattern of design 1.

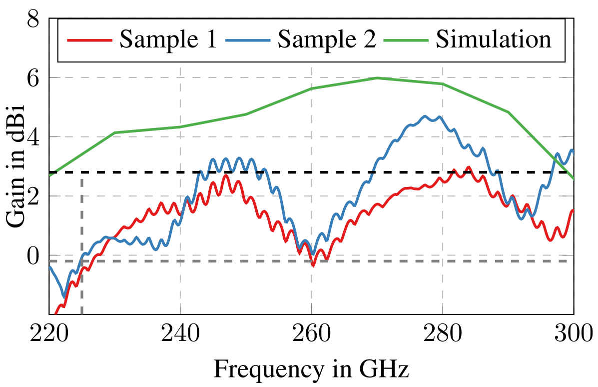


FIGURE 17. Measured and simulated gain at boresight of design 1.

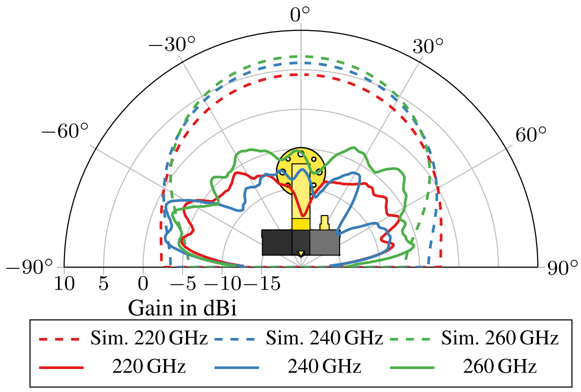


FIGURE 18. E-plane field pattern of design 2.

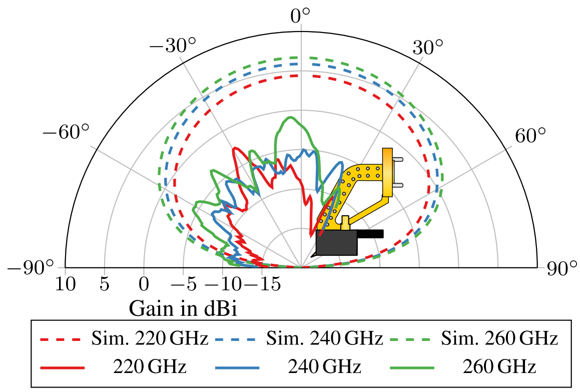


FIGURE 19. H-plane field pattern of design 2.

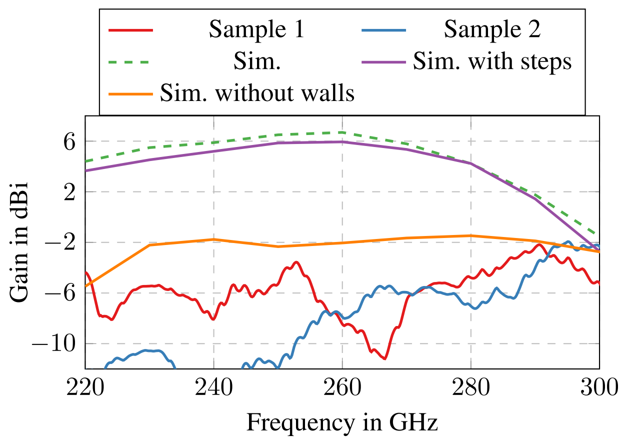


FIGURE 20. Measured and simulated gain at boresight of design 2.

significantly from the simulated response and barely exceeds 0 dBi. This deviation is also present in the gain over frequency depicted in Fig. 20. One noticeable difference between the design and the realized sample is the introduced steps due to the slicing. Two more simulations were conducted to evaluate the influence. Firstly, the elliptical shape is approximated by the steps with the realized height and width. The surface is electrically connected, and the 90° walls of the steps are assumed to be electrically connected. This simulation with the steps shows only little deviation from the actual elliptical shape. A second simulation assumes the 90° walls of the steps to be unconnected. This shows a significant drop in gain below −1.5 dB. This is in line with the measurements, which also show this behavior. A significant difference to [11], where such curved shapes were successfully printed and metalized, is the used printer.

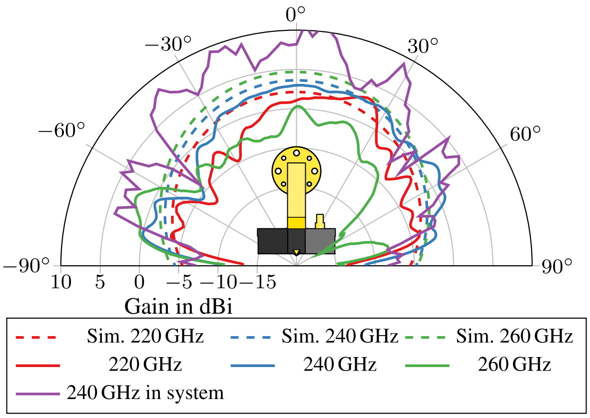


FIGURE 21. E-plane field pattern of the design 3. The in system measurement is in EIRP.

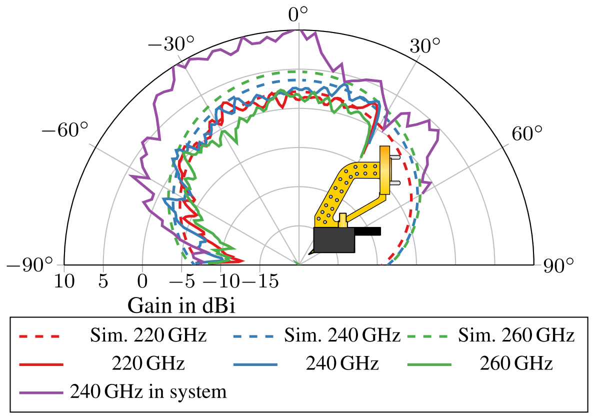


FIGURE 22. H-plane field pattern of the design 3. The in system measurement is in EIRP.

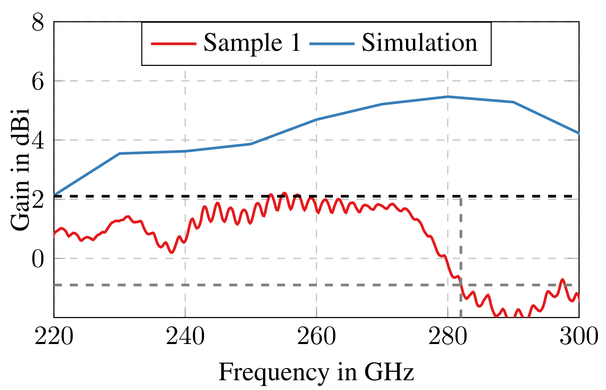


FIGURE 23. Measured and simulated gain at boresight of design 3.

While in [11], an in-house-built multi-photon lithography system with a 40×/1.4 objective was used for fabricating layers of 100 nm height, this work used the *BMF* printer. The *BMF* machine has a technically possible minimum slicing height of 1 µm, which, however, does not produce reliable results without extensive experimentation. Hence, a slicing height of 5 µm is used. Consequently, the height difference is too large to connect successfully with the used metal deposition process. Future works utilizing the freeform possibilities of 3D printing should consider the slicing height and metal deposition process for improved results. An additional galvanic metallization step might be used to overcome the issue of unconnected steps.

C. DESIGN 3

Lastly, the third design, which uses a glass resonator, is measured. Fig. 21 and Fig. 22 show the measured E-plane and H-plane patterns. Additionally, the pattern from the in system measurement presented in [17] is overlayed, which is however the EIRP in dBm, not the realized gain. In the E-plane, a strong tilt to 25° is visible, which should not be possible from the design. The antenna and resonator are strictly symmetric; they should have a symmetric pattern, which they show in the in-system measurement. Misalignment of the resonator to the antenna is not the root cause here. Simulations show that even 50 µm lateral shift is not enough to cause such a beam tilt. It is, therefore, assumed that the bond wire interconnect is radiating more than assumed due to a loose bond wire. This can be observed in the E-plane pattern in Fig. 21. The ripple is much stronger than the ripple present in the first design shown in Fig. 15, indicating the problematic transition. In the H-plane, shown in Fig. 22, the pattern shows the same reflection issues as before. Comparing it qualitatively to the simulation it does match. Compared to the in system measurement it shows a similar trend. Concerning the gain over frequency at boresight, shown in Fig. 23, a reduction in gain of around 2 dB is visible up to 270 GHz, After that the radiated power drops significantly, which should not be the case from the simulation. The peak at boresight is 2.1 dBi and the 3 dB bandwidth is 62 GHz around 251 GHz. From the H-plane plot in Fig. 22, it is apparent that the realized gain is indeed higher but is influenced by the vicinity of the probe.

Comparing the results with the state of the art in differential on-chip antennas presented in Tab. 1, this work presents the highest realized gain of all published antennas in this range. While the bandwidth is below other published results and below our simulation results, it is still highly competitive and within the design requirements set by the BPSK transmitter. The presented designs do not need a metallic backside reflector and, hence, have no direct requirement for the chip height. Due to the possibility of precise alignment and direct printing of the 3D printed structure with respect to the underlying IC or antenna, no separate assembly steps are necessary. However, even the glass resonator assembly is straightforward as the transparent substrate allows for the easy aliment of the metallic resonators to the feeding element with established pick-and-place technology.

VI. CONCLUSION

This work presents the design of a resonator-loaded on-chip shorted bow-tie antenna, as well as the manufacturing and measurements. To the author's knowledge, this is the first time a shorted bow-tie feeding element is used to feed a 3D printed resonator for applications above 200 GHz. A new 3D printing approach was successfully used to print a geometric structure directly on the CMOS BEOL antenna. A metal layer is deposited on the structure in a subsequent processing step. This is the first time direct printing and metallization of functional antenna structures on a CMOS chip is successfully demonstrated above 200 GHz. The measured 3D printed antenna improves over a more classical design with metal patches in both gain and bandwidth. Both antennas exceed the state of the art regarding realized gain and ease of assembly. A more complicated 3D structure with curved surfaces was tested. This design showed the shortfalls of the currently available 3D printers and metallization technique but shows promise for future designs to increase gain and bandwidth. The successfully demonstrated antennas push the state-of-the-art for on-chip differential antennas and pave the way for future commercialization of the frequency range above 200 GHz. Due to the compact design of the feeding element compared to its bandwidth, the deterministic boundary with the ground wall, and the good efficiency of the overall assembly, it offers itself to be used in future communications systems and phased arrays.

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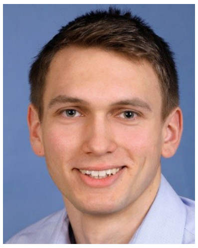

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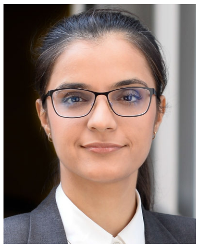

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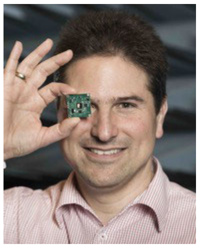

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