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A Cost-Effective Nonresonant Inverter Topology for Domestic Induction Heating

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ABSTRACT Nonresonant inverter topologies are a reliable, self-protective, and cost-effective solution for induction heating (IH) appliances. In this article, a novel nonresonant inverter topology, particularly suitable for domestic IH applications, is proposed. The proposed topology achieves high output voltage levels, addressing the main drawback of nonresonant topologies compared to resonant ones, which is an increased voltage demand for the same output power. In addition, both switching devices operate against a common ground, enabling a cost-effective implementation with high power density. In this article, the proposed inverter is described, its different operating modes are analyzed, and a power control strategy is derived. A comparison with conventional resonant topologies reveals a potential cost reduction of approximately 13 % in the main power electronics components, due to the elimination of resonant capacitors and the possibility of using more cost-effective gate drivers. Experimental results demonstrate that the output power can be seamlessly controlled from zero to 3.6 kW, while maintaining zero-voltage switching across a wide operational range. This ensures efficient operation with a maximum estimated efficiency of 98.3 %.

INDEX TERMS Domestic induction heating (IH), high-voltage (HV) transistors, home appliance, zero-voltage switching (ZVS).

I. INTRODUCTION

While in many applications, the conversion of electrical energy into heat corresponds to an undesirable generation of losses—it is crucial in heating processes. A well-known heating process within the domestic area is the usage of cookers and ovens. Within the past years, cookers and ovens have had the highest volume in sales compared to other major appliances, such as refrigerators, washing machines, or dishwashers. In the following years, the numbers are estimated to remain the highest [1].

Therefore, there is a great interest in improving the user experience during cooking, while on the other hand offering cost-effective solutions. Compared to classical heating systems, such as electroresistive, halogen, or gas cooktops, induction heating (IH) offers several advantages due the fact that the heat is generated directly within the cookware, significantly improving the cooking process [2], [3]. The main advantages of IH cooktops over other technologies are the cleanliness, the safety, as well as the efficiency of the heating process [4].

The power transfer of an IH system relies on applying an alternating magnetic field to the IH load, which is composed of the cooking vessel and the spiral wound induction coil (see Fig. 1). Different models exist to describe the behavior of the IH load. Some of these approaches make use of multiple passive components [5], [6], [7]. However, the simplest and most commonly used model is the series connection of an equivalent inductor L_{eq} and an equivalent resistor R_{eq} as depicted in Fig. 2 [8], [9]. Analytical approaches [10] or finite-element analyses (FEAs) are used to parameterize the equivalent impedance model [11], [12], [13].

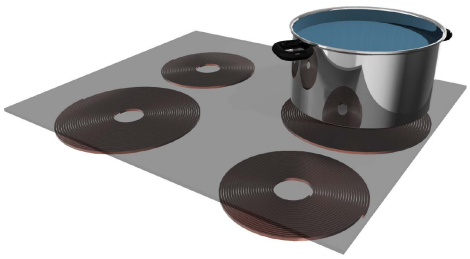

FIGURE 1. Exemplary design of a conventional domestic IH cooktop with four inductors, where the glass-ceramic plate and a single pot are shown.

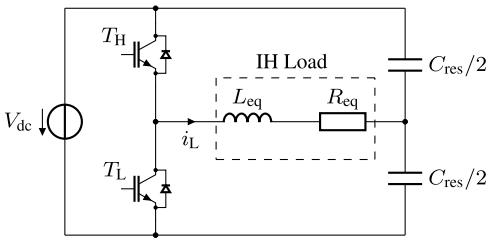

FIGURE 2. Equivalent circuit diagram of an SRHB inverter with IH load depicted as a series connection of the equivalent inductance L_{eq} and the equivalent resistance R_{eq} as well as the split resonant capacitor consisting of two capacitors of value $C_{res}/2$.

Regarding the power electronics system of a domestic IH system, the most commonly used inverter topologies are the resonant single-switch inverter for an output power P of up to 2 kW [14], [15], [16], the series-resonant half-bridge (SRHB) inverter ($P < 5$ kW) [17], [18], [19], [20] as well as the series-resonant full-bridge (SRFB) inverter ($P > 5$ kW) [21], [22]. Of those topologies, the SRHB offers the best compromise between cost, performance, and control complexity, making it the preferred inverter topology in many domestic IH applications [23]. The equivalent circuit diagram of the SRHB inverter including the IH load is depicted in Fig. 2.

However, all resonant topologies are facing critical design challenges [24], which can be stated as follows.

1) The use of bulky resonant capacitors increases the system costs as the number of required components increases, additionally leading to a higher printed circuit board (PCB) cost. Furthermore, the lifetime of resonant capacitors is reduced if they are exposed to high temperature and humidity as given in domestic IH systems. This results in a reduced lifetime of the overall system.
2) Usually, resonant inverters are tuned to a specific quality factor at resonant frequency $Q_{res}(f_{res})$ [25]. Tolerances introduced by the resonant capacitors or variation in cookware material, and therefore, parameter variation of L_{eq} and R_{eq}, can lead to detuning of the resonant tank.
3) IH load material characteristics as well as cookware placement on the cooktop change frequently and affect the safe operating area of the inverter [26]. In the worst case, this can lead to inverter failure.
4) When using HB or FB inverters, galvanic isolation for the high-side gate drivers and bootstrap circuits are needed. Thus, the component count and costs are increasing.

Nonresonant inverter topologies offer the possibility to overcome these challenges as no resonant capacitors are used. In addition, due to the ohmic-inductive character of the IH load, in contrast to resonant inverter topologies, nonresonant topologies are self-protective. However, due to the large air gap between the inductor and the cooking vessel, the lack of resonant capacitors increases the voltage demand at equal levels of output power in comparison to resonant inverter topologies. So far, in literature the maximum output power of nonresonant inverter topologies for use in zone-controlled IH systems is reported being less than 2 kW [24], [27]. The most recent usage of nonresonant inverter topologies are presented in [28], [29], and[30] but refer to flexible cooking surfaces with a maximum output power of approximately 670 W per inductor.

Hence, in this article for the first time a cost-effective, nonresonant inverter topology with a maximum output power of 3.6 kW is presented. This increase in output power is achieved through the magnetic coupling of two inductors allowing to double the output voltage in comparison to HB inverter topologies. An analysis of the proposed inverter as well as a description of the inductor modeling and design are described in detail in the remainder of this article.

The rest of this article is organized as follows. In Section II, the proposed topology is described, the different operation modes are explained, and a comparison with conventional inverter topologies in terms of component count and costs is presented. In Section III, the modeling and design of the dedicated inductor is explained. In addition, the power control scheme of the inverter combining different operation modes is explained on the example of simulation data. The selection of snubber capacitor values and inverter dead time is performed with measurement data in Section IV. In addition, in this section, experimental results up to a power of 3.6 kW are presented to prove the feasibility of the proposed inverter topology. Finally, Section V concludes this article.

II. PROPOSED INVERTER TOPOLOGY

A. COUPLED INDUCTOR INVERTER (CII)

The CII makes use of two magnetically coupled inductors L_1 and L_2 as shown in Fig. 3(a). Herein, the components L_p and R_p represent the IH load. By connecting the inductors L_1 and L_2 in opposite winding direction to the positive terminal of the DC-Link, the output voltage of the inverter is doubled [31]. The second inductor terminal is connected to the drain terminal of a transistor, being switched against common ground level. In comparison to state-of-the-art inverter topologies, this characteristic leads to major advantages in terms of a simple and cost-effective implementation of the inverter as neither galvanic isolation nor a bootstrap circuit is needed for the gate drivers.

The inverter can be operated in different operation modes, which are described in the following subsections. For

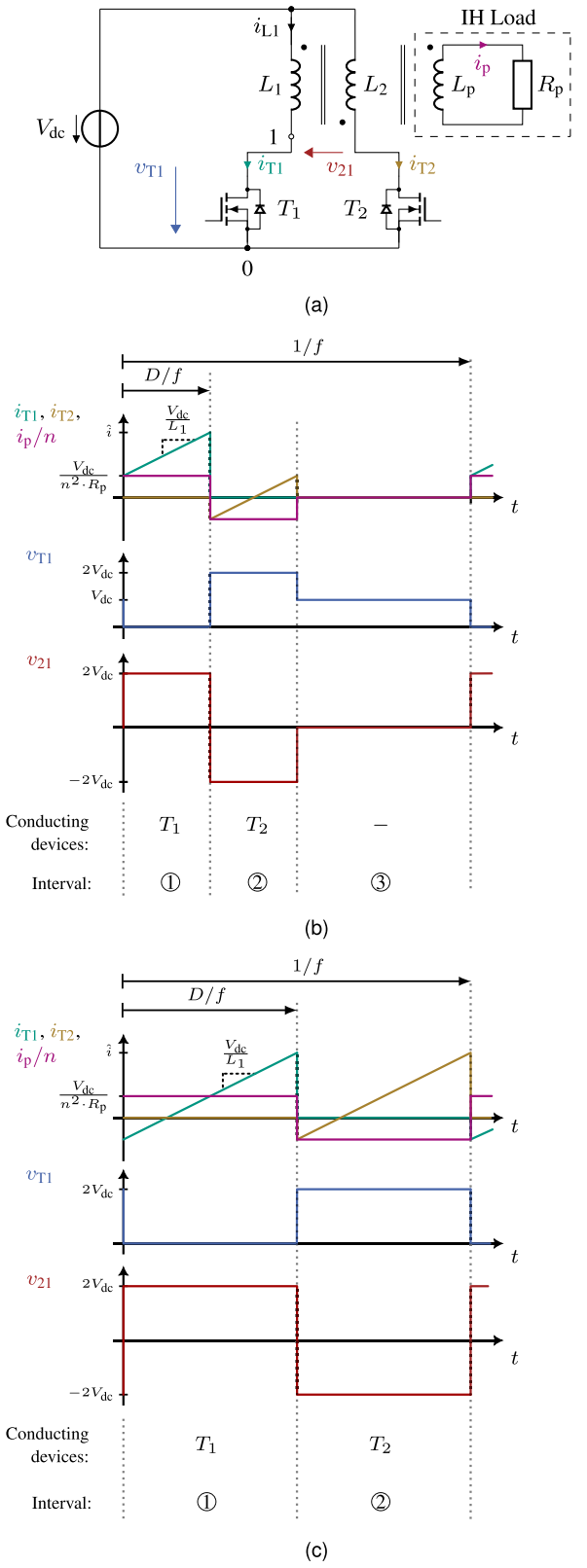

FIGURE 3. Proposed circuit. (a) Equivalent circuit diagram of the CII with IH load depicted as inductance L_p and resistance R_p. (b) Exemplary waveforms of currents i_{T1} and i_{T2} and scaled current i_p/n as well as voltages v_{T1} and v_{21} for a single period using duty-cycle control with $D = 0.25$. (c) Exemplary waveforms of currents i_{T1} and i_{T2} and scaled current i_p/n as well as voltages v_{T1} and v_{21} for a single period with $D = 0.5$.

modeling purposes, ideal magnetic coupling between L_1 and L_2 is assumed, resulting in a coupling factor of unity. For the sake of simplicity, the inverter dead time T_d and the equivalent capacitance C_{eq} of the switching nodes against ground, e.g., between nodes 1 and 0 in Fig. 3(a), are neglected when discussing the waveforms presented in following subsections.

B. INVERTER OPERATION MODES

1) DUTY-CYCLE CONTROL

Both transistors, T_1 and T_2, are periodically switched ON and switched OFF and the inverter output voltage can be controlled by a variation of the duty cycle D in the range of $0 \leq D < 0.5$, while the inverter is operated at a fixed frequency f.

Exemplary waveforms for operation of the CII with duty-cycle control and a duty cycle D of 0.25 are shown in Fig. 3(b). During interval ①, device T_1 is conducting. The initial current value, after the turn-ON transition of T_1, depends on the DC-Link voltage V_{dc}, the number of turns in the inductors $n_1 = n_2 = n$ as well as the value of R_p. It has to be mentioned, that R_p does not have a fixed value, but depends on the operating point of the inverter, determined mainly by the switching frequency f and the current through the inductor i_{L1}. However, as long as T_1 is conducting, the current through L_1 is increasing with a slope of V_{dc}/L_1 until it reaches its maximum $\hat{i}$ immediately before switching OFF T_1. At the same time, the current in the IH load, denoted by i_p, is constant with a value of $V_{dc}/(n \cdot R_p)$. The magnetic energy stored in L_1 is being decreased during interval ②while T_2 is conducting. During this interval, the device T_1 has to block a voltage of $2 \cdot V_{dc}$, and voltage v_{21} is negative with a value of $-2 \cdot V_{dc}$. At the same time, the current i_p is negative with a value of $-V_{dc}/(n \cdot R_p)$. After T_2 is switched OFF, both devices remain switched OFF for the remainder of the period and the currents i_{T1}, i_{T2}, and i_p are zero. At the end of interval ③, the transistor T_1 is switched ON again. It is depicted that before being switched ON, T_1 blocks the voltage V_{dc}, while the inverter current is zero. Even though parasitic capacitances are neglected in this analysis, in a real hardware setup, the described characteristic leads to increased switching losses as zero-voltage switching (ZVS) conditions are not fulfilled [32].

2) FREQUENCY CONTROL (FC)

To mitigate the problem of increased switching losses during the turn-ON transition of T_1, FC can be used. Due to the characteristic of the load, the power transferred to the cookware can be controlled by varying the switching frequency f of the switches T_1 and T_2. In this case, the duty cycle D is set to 0.5. Exemplary waveforms of the currents i_{T1}, i_{T2}, and i_p/n as well as the voltages v_{T1} and v_{21} over a single period for operation of the inverter with FC are given in Fig. 3(c). The waveforms show that, while the switch T_1 is conducting during interval ①, the current through the inductor L_1 is increasing with a slope of V_{dc}/L_1. Meanwhile, the current i_p in the IH load remains constant with a value of $V_{dc}/(n \cdot R_p)$. During interval ②, the switch T_1 is blocking a voltage of $2 \cdot V_{dc}$, while

theswitch T_2 is conducting, and voltage v_{21} is negative. In this interval, the magnetic energy stored in the inductor L_1 is completely discharged by L_2 and the current through the IH load i_p is negative with a value of $-V_{dc}/(n \cdot R_p)$.

Contrarily to the behavior depicted in Fig 3(b), ZVS can be achieved when using FC, as the current through the semiconductor devices is negative before the turn-ON transition [see Fig. 3(c)]. However, to achieve ZVS behavior, sufficient dead time T_d needs to be considered. ZVS is obtained if the charge Q_{eq} stored in C_{eq} is completely discharged during the inverter dead time. The minimum dead time $T_{d,min}$ to achieve ZVS behavior can analytically be determined by integrating the current through C_{eq} as follows:

$$Q_{eq}(V_{dc}) = \int_0^{T_{d,min}} i_{C_{eq}}\, dt = 2 \cdot C_{eq}(V_{dc}) \cdot V_{dc}. \qquad (1)$$

3) DISCONTINUOUS OPERATION

Besides operation with duty-cycle or FC, the CII can be operated in discontinuous operation mode (DM). Therefore, the transistor T_2 is permanently turned OFF and the transistor T_1 is periodically turned ON using a duty cycle D within the range of $0 \leq D < 0.5$. Hence, the equivalent circuit diagram can be simplified as depicted in Fig. 4(a), where T_2 is replaced by a single diode D_2 in the schematic.

Exemplary waveforms for discontinuous operation are shown in Fig. 4(b) with a duty cycle D of 0.25. It can be seen that immediately after switching on T_1, at the beginning of interval ① the current through T_1 is increasing with a slope of V_{dc}/L_1 with an initial value of $V_{dc}/(n^2 \cdot R_p)$. During this interval, the voltage v_{21} is positive with a value of $2 \cdot V_{dc}$ and the current i_p in the IH load is constant. Once T_1 is switched OFF at the end of interval ① T_1 has to block a voltage of $2 \cdot V_{dc}$ and voltage v_{21} becomes negative. During this interval, diode D_2 is conducting and the magnetic energy in the system is decreasing. The current i_p is flowing in negative direction. At t_1, the current i_{D2} becomes zero, while i_p still has a value of $-V_{dc}/(n \cdot R_p)$. Therefore, after t_1, the current i_p as well as the voltages v_{T1} and v_{21} are decreasing with a time constant τ of L_p/R_p down to zero and values of V_{dc} and zero, respectively. From the condition of volt-second balance for voltage v_{21}, t_1 can be determined according to

$$2 \cdot DT - t_1 + \tau \cdot \exp\left(-\frac{T - t_1}{\tau}\right) - \tau = 0 \qquad (2)$$

with $T = 1/f$ and f as switching frequency of transistor T_1. The derivation of (2) is given in Appendix A. As demonstrated for duty-cycle control, the waveforms of inverter currents and voltage v_{T1} show that in discontinuous operation, ZVS behavior is not achieved and additional losses during the turn-ON transition of T_1 occur. These additional losses $P_{sw,on}$ can be calculated through

$$P_{sw,on} = \frac{1}{2} \cdot C_{eq} \cdot v_{T1,0}^2 \cdot f \qquad (3)$$

where $v_{T1,0}$ is the voltage over T_1 during the turn-ON transition with a value in the range of $V_{dc} \leq v_{T1,0} \leq 2 \cdot V_{dc}$.

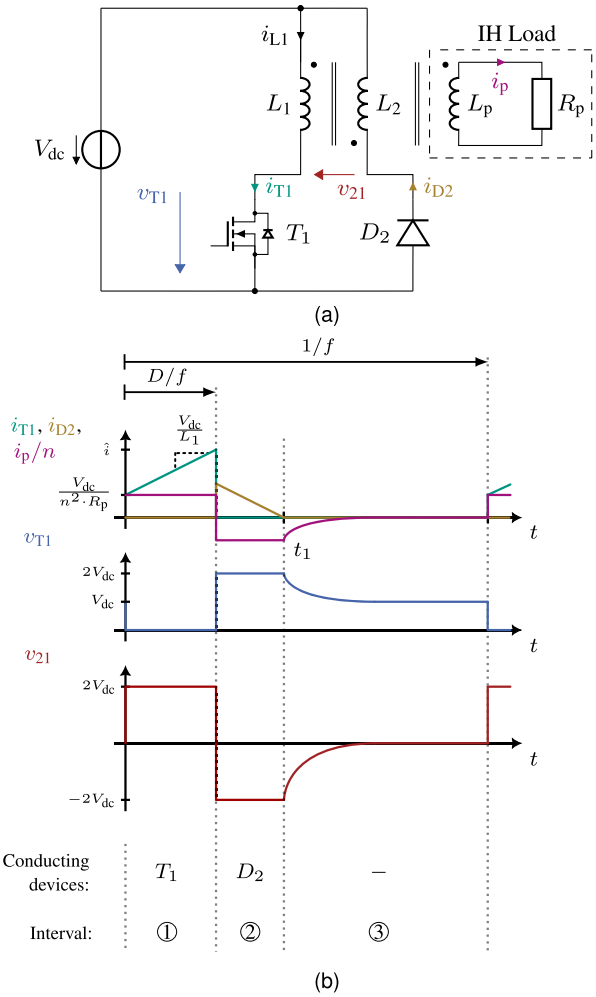

FIGURE 4. Proposed circuit. (a) Equivalent circuit diagram of the CII for operation in DM. (b) Exemplary waveforms of currents i_{T1} and i_{D2} and scaled current i_p/n as well as voltages v_{T1} and v_{21} for a single period with a duty cycle D of 0.25.

When comparing different modulation schemes, FC provides the highest efficiency since it enables ZVS. However, relying solely on this method does not allow seamless output power regulation down to 0 W, as the switching frequency f would approach infinity. Neither duty cycle control nor discontinuous operation achieves ZVS. However, discontinuous operation offers a higher level of safety than duty cycle control because only one transistor is actively switched. Therefore, a hybrid approach—using FC for high output power and discontinuous operation for low power levels—is advantageous for hardware implementation and is presented as the preferred control strategy in the following discussion.

C. COMPARISON WITH CONVENTIONAL INVERTER TOPOLOGIES

Table 1 gives a comparison of state-of-the-art resonant inverter topologies used in domestic IH systems, being the SRHB and the SRFB inverter with non-resonant inverter topologies, being the nonresonant FB (NRFB) inverter and the CII. Herein, the power range P_o of the inverter, the

TABLE 1. Comparison of Different Inverter Topologies

Topology	P_o/kW	SP	$V_{o,max}$	N_T	$V_{CE,max}$	N_C	E_T/€	E_G/€	E_C/€	$\sum E$/€
CII	≤ 3.6	✓	V_{dc}	2	$2 \cdot V_{dc}$	-	2.03	0.42	-	4.49
NRFB	≤ 2	✓	V_{dc}	4	V_{dc}	-	1.83	0.82	-	8.95
SRHB	≤ 5	✗	$\sqrt{0.5} \cdot V_{dc}$	2	V_{dc}	1 to 2	1.83	0.82	0.69	5.17
SRFB	> 5	✗	V_{dc}	4	V_{dc}	1	1.83	0.82	0.69	9.64

self-protection (SP) capability, the maximum output voltage $V_{o,max}$, the number of semiconductor switches N_T, the blocking voltage of the semiconductors $V_{CE,max}$, the number of resonant capacitors N_C as well as averaged cost E_T of a transistor, the cost E_G of the gate circuitry, and the cost E_C of a resonant capacitor, which includes the cost of the PCB area for a capacitor are compared. All given costs are listed for a quantity of one for each component. Costs of the gate circuitry for the HB and FB inverters are estimated under the assumption of using a half-bridge gate driver and bootstrapping. Hence, the total costs for each topology are calculated by taking into account the minimum number of components needed to design each topology. For the SRHB these are: two IGBTs, a single half-bridge gate driver, and a single resonant capacitor. For the CII, two IGBTs and a single gate driver IC with two drivers and two outputs are mandatory. However, it has to be mentioned that especially the number of required resonant capacitors might be greater as listed in Table 1 as the current-carrying capability of the capacitors usually is lower than the load current leading to increased total costs.

The cost values are derived by averaging prices listed on popular distributor webpages, such as *Mouser Electronics, Premier Farnell,* and *DigiKey,* based on the highest available quantity discount for each product. Prices for six different products of a component are averaged across at least four distributors, excluding the highest and lowest values to reduce outliers. Table 3 in the Appendix outlines the requirements for each product, of which the most cost-effective options from different manufacturers are selected.

In comparison to the SRFB inverter, the SRHB inverter offers a better balance between cost, performance, and control complexity, and is therefore, the preferred choice for IH systems with a maximum appliance power lower than 5 kW [23]. However, self-protectiveness is not given. While the NRFB features this characteristic, it is not competitive to the SRHB in terms of cost. Contrarily, through the lack of resonant capacitors and the low requirements on the gate drive circuitry, the CII allows a cost-effective implementation of the power electronics. Nevertheless, it has to be mentioned that additional cost arise for the inductors as additional terminals need to be soldered when compared to conventional inductor designs and are not considered in this comparison. Hence, it has to be outlined that the cost advantage in the power electronics system of the CII is based on the possibility of using of cost-effective gate drivers and the lack of resonant capacitors. The total system cost greatly rely on the overall system design including the manufacturing cost of the inductor, which among others, depends on the manufacturing technology and the automation degree.

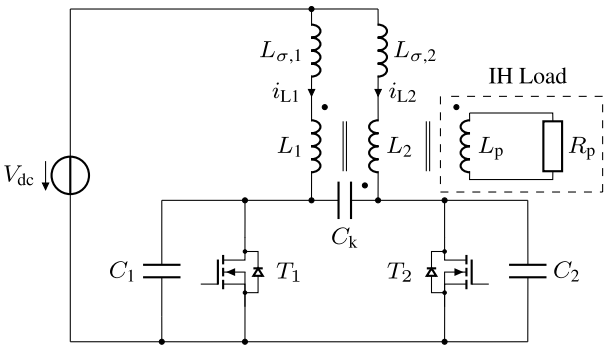

FIGURE 5. Equivalent circuit diagram of the CII with leakage inductances $L_{\sigma,1/2}$, coupling capacitance C_k, and snubber capacitors $C_{1/2}$.

III. MODELING, PARAMETRIZATION, AND POWER CONTROL STRATEGY

A. MODELING AND DESIGN OF THE IH LOAD

The values of the IH load, being L_p and R_p, influence the inverter behavior. Due to the high magnetic coupling between L_1 and L_2, conventional modeling approaches making use of a serial connection of an equivalent inductance L_{eq} and an equivalent resistor R_{eq} (see Section I) are not applicable for the CII. Instead, the IH load is modeled by the single turn inductance L_p, which is magnetically coupled to L_1 and L_2, and the resistor R_p. The values of L_1, L_2, and R_p, determining the power transfer to the IH load, are not constant over frequency f. In addition, in a hardware implementation, the coupling factor of L_1 and L_2 is not unity, introducing the leakage inductances $L_{\sigma,1}$ and $L_{\sigma,2}$. The leakage inductances are within the commutation path of T_1 and T_2, and external snubber capacitors C_1 and C_2, acting as lossless snubbers, are used to reduce the voltage spikes over the transistors. Besides magnetic coupling, also capacitive coupling between L_1 and L_2 occurs, resulting in the equivalent circuit diagram as given in Fig. 5.

Parametrization of the model is performed using small and large signal measurements as well as simulation results by means of FEA. The values of L_1 and L_2 as well as L_p and R_p are determined using FEA. Due to computational effort, the internal litz wire structure of the turns is not defined within the geometrical description of the FEA model. However, the frequency-dependent winding losses are determined according to [33].

The magnetic material properties of the cookware bottom are defined corresponding to [12] and are depicted in Fig. 7 in

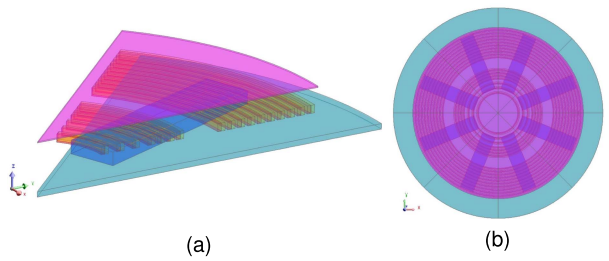

FIGURE 6. Finite-element model of the inductor-pot system. (a) Part model with aluminum shielding in light blue, ferrite bar in dark blue, turns of inductor 1 in red, turns of inductor 2 in yellow, and cookware bottom in pink color. (b) Top view of full IH load, derived from part model depicted in (a).

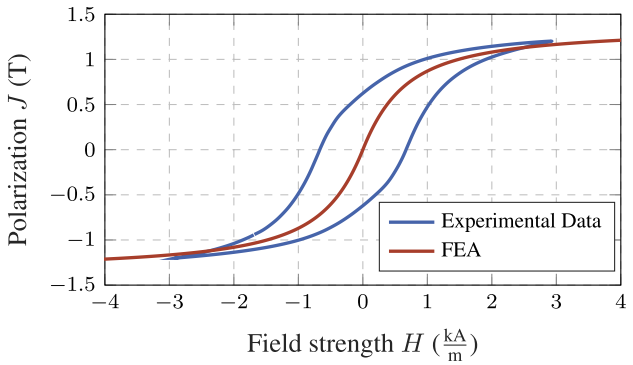

FIGURE 7. Comparison of the magnetization curve used in FEA software and measurement data of stainless steel material specimen of type AISI 430.

red color. The measurement data represented by the blue curve were determined by means of Epstein frame measurements of stainless steel probes of type AISI 430, which is typically used in IH cookware. It can be seen that hysteresis effects are not negligible. Hence, the corresponding hysteresis losses are added to the FEA results in the postprocessing according to

$$P_{\text{hyst}} = 4 \cdot \hat{B} \cdot H_{\text{c}} \cdot V_{\text{eff}} \cdot f \tag{4}$$

with $\hat{B}$ being the amplitude of the magnetic flux density in the cookware bottom, H_{c} as magnetic coercive field strength of the magnetic material, V_{eff} being the effective volume of the cookware bottom determined through the penetration depth and the geometric dimensions of the vessel, and f as frequency. The specific resistance ρ of the cookware material is assumed to be $577 \cdot 10^{-9}\,\Omega$m. As stated in [34], the temperature dependence of materials used in IH systems is negligible. Therefore, the electromagnetic material properties of the cookware bottom are regarded as independent of temperature changes. The RMS values of the rectangular voltage applied to the inductors is given through

$$V_{1,\text{push}} = V_{\text{dc}} \cdot \sqrt{2 \cdot D}. \tag{5}$$

Assuming a symmetric coupling, the operating point dependent values of L_{p} are determined according to

$$L_{\text{p}} = \frac{L}{n^2} \tag{6}$$

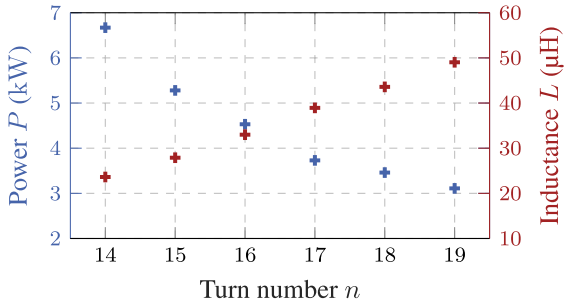

FIGURE 8. FEA results of the transferred power P and values of inductances L_1 and L_2 (no load) in dependence of turn number n. Simulations are performed with a constant DC-Link voltage V_{dc} of 230 V, and a switching frequency f of 25 kHz for a duty cycle D of 0.5.

with n being the number of turns of inductors L_1 and L_2. The values of R_{p} are derived from the power P transferred to the cookware and can be calculated as

$$R_{\text{p}} = \frac{V_{1,\text{push}}^2}{n^2 \cdot P} = \frac{V_{\text{dc}}^2 \cdot 2 \cdot D}{n^2 \cdot P}. \tag{7}$$

Within the application, the maximum input power of the inverter is limited to 3.6 kW, which is determined by the single-phase connection to the European voltage grid ($V = 230$ V and $I = 16$ A). The IH load is designed in such a way that the target frequency $f(P_{\text{max}})$ equals 25 kHz. Therefore, FEA simulations are performed for a variation of turn number n at a fixed frequency f of 25 kHz, a constant DC-Link voltage V_{dc} of 230 V, and a duty cycle D of 0.5. A pot with an outer diameter d_{o} of 220 mm is modeled to be above the inductors in a vertical distance d_{z} of 7 mm. For variation of the turn number n, the inner and outer diameters of the inductors are fixed at $d_{\text{i,Ind.}} = 50$ mm and $d_{\text{o,Ind.}} = 215$ mm, respectively. Exemplarily, the FEA model for a turn number n of 17 is depicted in Fig. 6(a).

The transferred power P and the values of the inductances L_1 and L_2 (without a pot placed above the inductors) are given in Fig. 8 in dependence of the turn number n. It can be seen, that the transferred power P decreases with an increase of the turn number n. This is due to the fact that the impedance of the inductor rises for increasing turn numbers n. This corresponds to the increase of the inductance L with the increase of the turn number n. However, a transferred power P of approximately 3.6 kW is reached for a turn number n of 17. According to (7), the corresponding value of R_{p} is 47.1 mΩ and the inductance L without a pot placed above the inductor is 38.9 µH for this specific inductor design. Therefore, for the inductor with a turn number n of 17, the parameter values of L and R_{p} are determined in dependence of frequency f and duty cycle D. Fig. 9 shows simulation results for values of the inductances L_1 and L_2 and of the resistance R_{p} for varying frequency f and duty cycle D. As the values of R_{p} increase with frequency f, leading to a decrease in output power P_{o}, the values of L decrease with rising f. This is because the opposing field generated by the eddy currents in the pot bottom increases with frequency f.

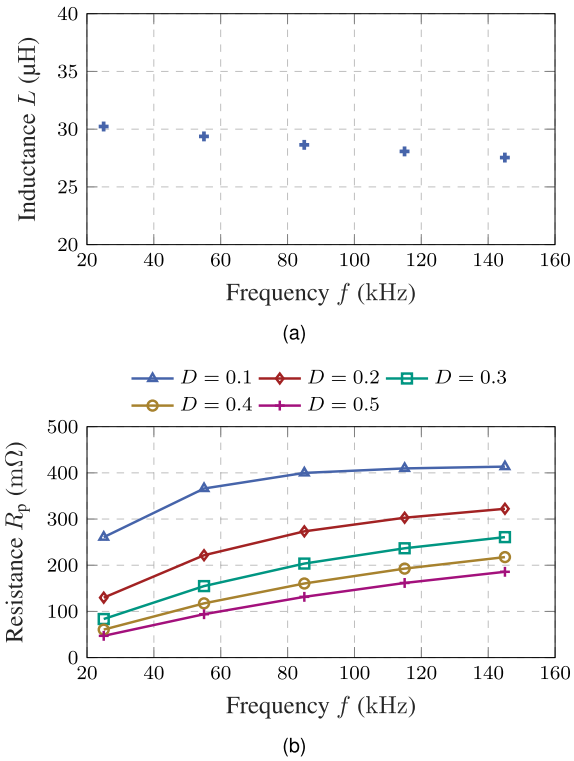

FIGURE 9. Variation of impedance over frequency. (a) Values of inductance L over frequency f at a duty cycle D of 0.5. (b) Resistance R_p over frequency f for varying duty cycle D.

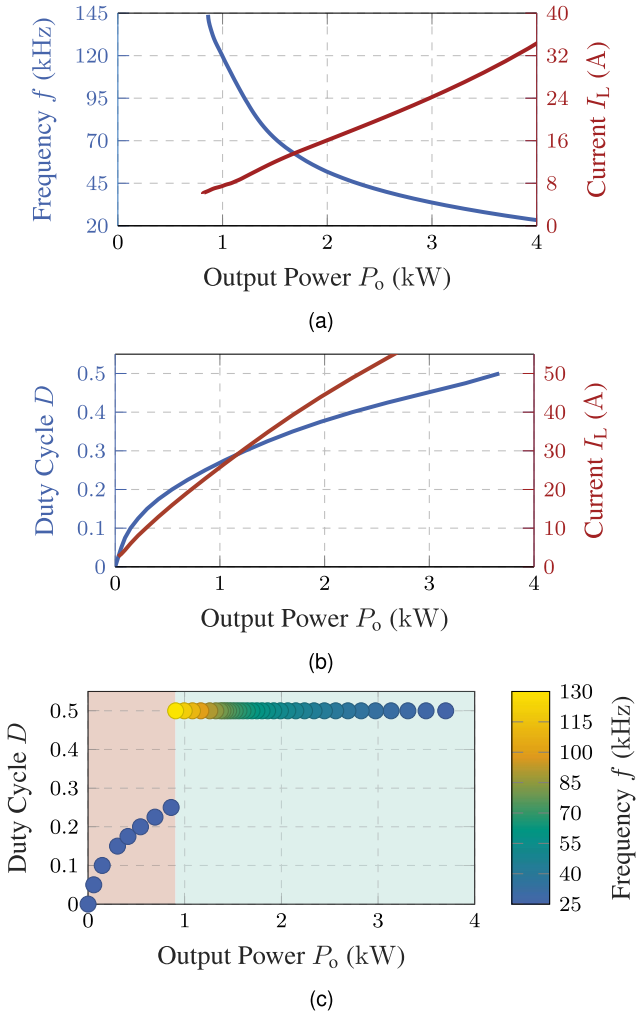

FIGURE 10. Simulation results of inverter output power (a) with FC, (b) in DM, as well as (c) combined control strategy of the CII. FC control is used up to a maximum frequency f of 130 kHz (see green highlighted region), DM is used for low output power range (see red highlighted region).

B. POWER CONTROL SCHEME

To derive a power control scheme for the inverter, the parameter values of L and R_p given in the previous section serve as input parameters for an electrical circuit model (see Fig. 5). Simulation results of the output power P_o over frequency f are depicted in Fig. 10(a) for FC. It is shown that the output power P_o reaches a value of approximately 3.6 kW at a frequency f of 25 kHz. In this operating point, the RMS current through the inductors L_1 and L_2 is approximately 29 A [see the red curve in Fig. 10(a)]. For an output power P_o of zero, the switching frequency f tends toward infinity. Above a frequency f of approximately 130 kHz, the switching frequency has to be increased overproportional to achieve a further reduction of output power P. As depicted in Fig. 10(b), DM allows seamless output power control down to 0 W. Hence, the combined control strategy of the inverter is defined such that in the low power range up to an output power of approximately 860 W, DM is used. In this operating point, the maximum duty cycle D is 0.25, while the inverter is operated with a switching frequency f of 25 kHz. For higher output power levels, the inverter is operated with FC up to a maximum frequency of 130 kHz while achieving ZVS.

IV. EXPERIMENTAL RESULTS

A. HARDWARE PROTOTYPE

To demonstrate the feasibility of the proposed inverter topology, a prototype is built that is depicted in Fig. 11(a). The PCB consists of four identical inverters of which one is marked by box ①. Each inverter is designed to deliver a maximum power P_o of 3.6 kW using 1.2-kV silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs). In addition, an input filter and an active rectifier stage is implemented (see ④ and ③, respectively). The digital interface is implemented through an *AMD Artix 7* field-programmable gate array (FPGA) board (see ②). Additional hardware components and specifications are listed in Table 2. The inductors are designed according to the results presented in Section III-A with a turn number n of 17. The inductor is made from litz wire and the corresponding litz wire bundles are separated, such that the inductors L_1 and L_2 are galvanically isolated [see Fig. 11(b)]. The values of the leakage inductances $L_{\sigma,1/2}$ are measured with an *LCR* meter according to [35]. The coupling capacitance C_k between L_1 and L_2 is determined through comparison of large signal measurements and electric circuit simulations.

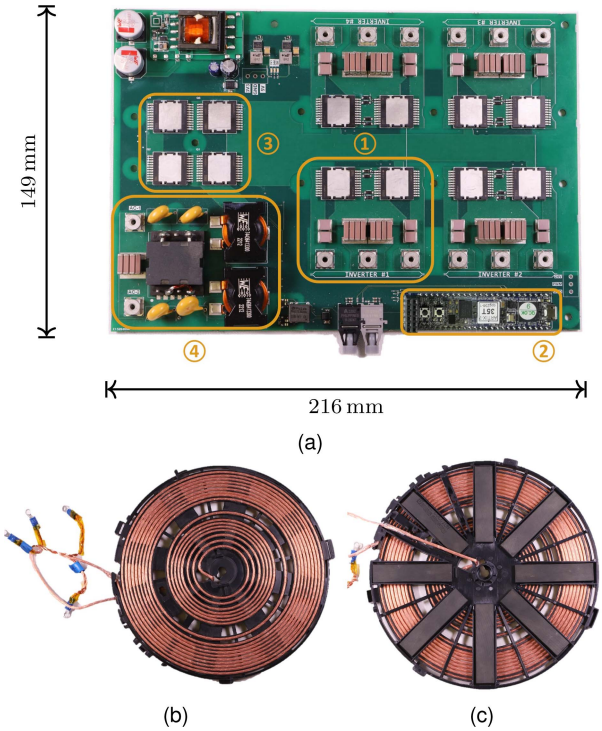

FIGURE 11. Hardware prototype of the proposed topology. (a) PCB of the hardware prototype with inverter stage and DC-Link as well as snubber capacitors ①, FPGA control board ②, rectifier stage ③, and input filter ④. (b) Top and (c) bottom views of designed inductors with $n = 17$ turns and outer diameter $d_{o,Ind.} = 215$ mm. The two inductors are made from the same litz wire by separation of the corresponding wire bundles as to be seen in (b).

TABLE 2. Hardware Components and Specifications of Prototype

Parameter	Symbol	Value
Max. drain-source voltage	$V_{DS,max}$	1.2 kV
Drain-source resistance	$R_{ds,on}$	20 mΩ
Max. output power	P_{max}	3.6 kW
Frequency at P_{max}	$f(P_{max})$	25 kHz
DC-Link capacitance (C0G)	C_{dc}	7.04 µF
Snubber capacitance (C0G)	$C_{1/2}$	2.4 nF
Leakage inductance	$L_{\sigma,1/2}$	500 nH
Coupling capacitance	C_k	2.15 nF

B. SWITCHING BEHAVIOR AND ZVS REGIONS

To limit the voltage spikes during turn-OFF transitions, snubber capacitors are added in parallel to the transistors. However, the larger the capacitance in parallel to the transistors, the lower is the maximum frequency at which ZVS is achieved. Therefore, simulations are carried out to determine the maximum allowable capacitance, while at the same time achieving ZVS over a wide operating range. Then, the maximum values of the snubber capacitors $C_{1/2}$ for different values of the inverter dead time T_d are given in Fig. 12(a). It can be seen that depending on the dead time selection, the maximum snubber capacitance decreases strongly with an increase in switching frequency f. As the results presented in Fig. 10 show, for high values of frequency f in the range above 130 kHz, the output

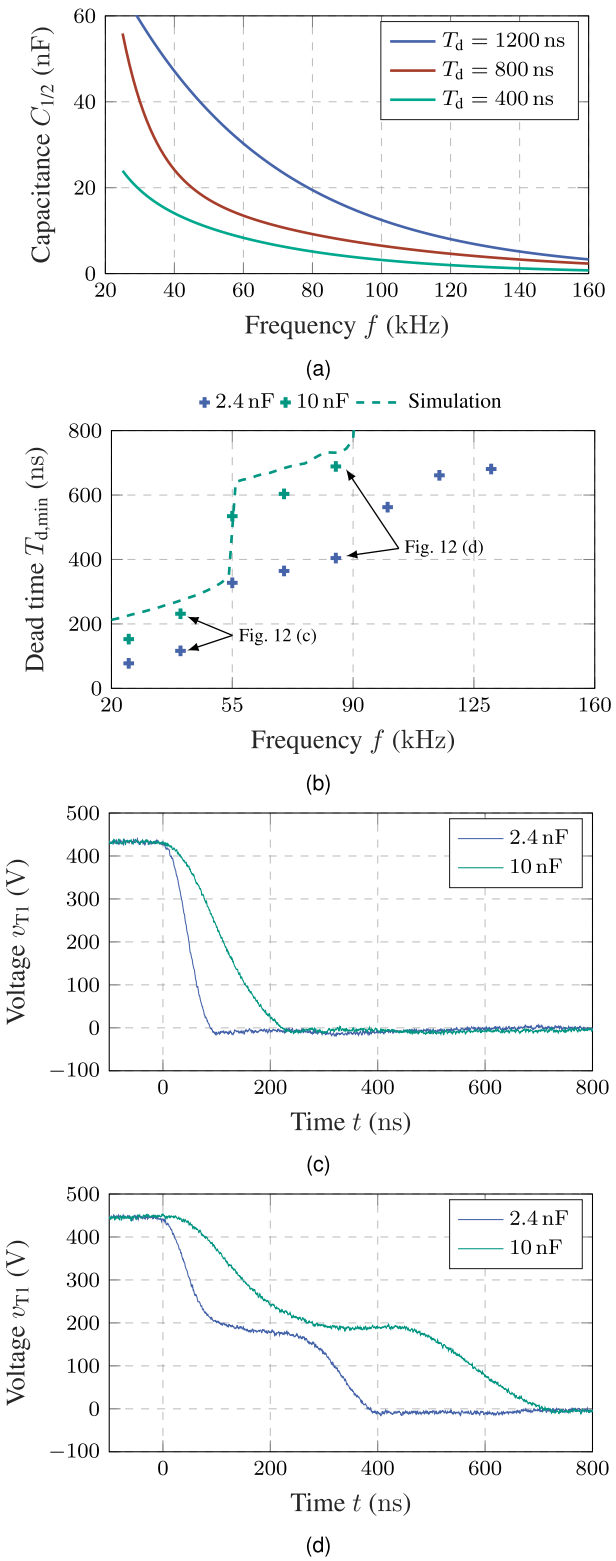

FIGURE 12. Operating characteristics of the proposed topology. (a) Maximum capacitance values of $C_{1/2}$ for different values of dead time T_d enabling ZVS. (b) Experimental and simulation results of minimum dead time $T_{d,min}$ over frequency f to achieve ZVS for different values of the snubber capacitors $C_{1/2}$. Experimental waveforms of voltage v_{T1} (c) for operation of the inverter at a frequency f of 40 kHz and (d) for operation of the inverter at a frequency f of 85 kHz for different values of snubber capacitance.

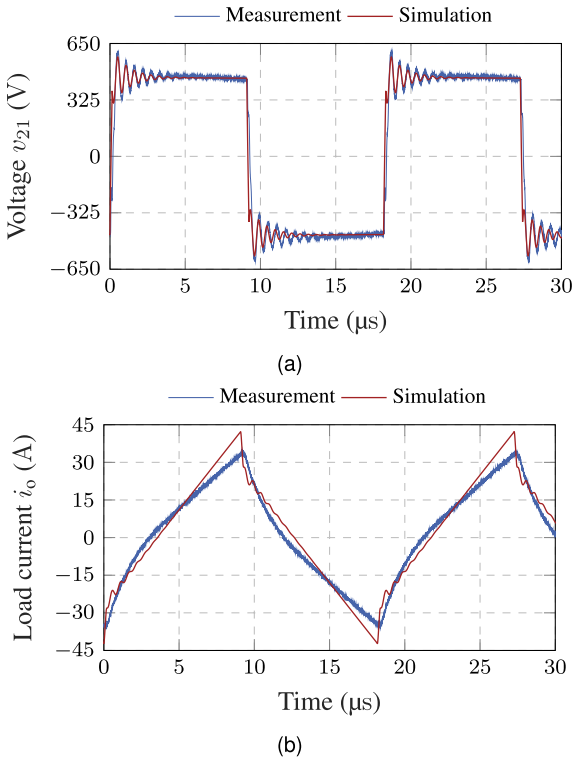

FIGURE 13. Experimental and simulation results. (a) Measurement and simulation results of voltage v_{21} and (b) measurement and simulation results of current $i_o = i_{L1} - i_{L2}$ for operation of the inverter with a switching frequency f of 55 kHz at a constant DC-Link voltage V_{dc} of 230 V.

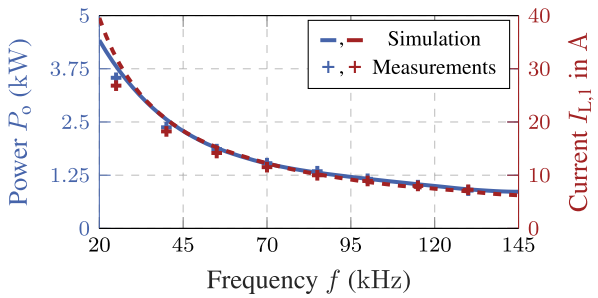

FIGURE 14. Simulation (-) and measurement (+) results of the output power P_o over frequency f for operation of the CII with FC at a constant DC-Link voltage V_{dc} of 230 V and a fixed duty cycle D of 0.5.

power can only be further decreased through an overproportional increase of frequency f. This fact either demands for low values of snubber capacitance or high values of inverter dead time. The minimum dead time necessary to achieve ZVS for different values of frequency f and snubber capacitance is depicted in Fig. 12(b) for simulation and measurement results. It can be seen, that there are frequencies for which the minimum dead time increases significantly, e.g., as the comparison of minimum dead time in the intervals from 20 to 55 kHz and 56 to 90 kHz for a snubber capacitance value of 10 nF shows. As shown in Fig. 12(c) and (d), this behavior occurs independently of the choice of the snubber capacitor value and is related to the resonant commutation process of

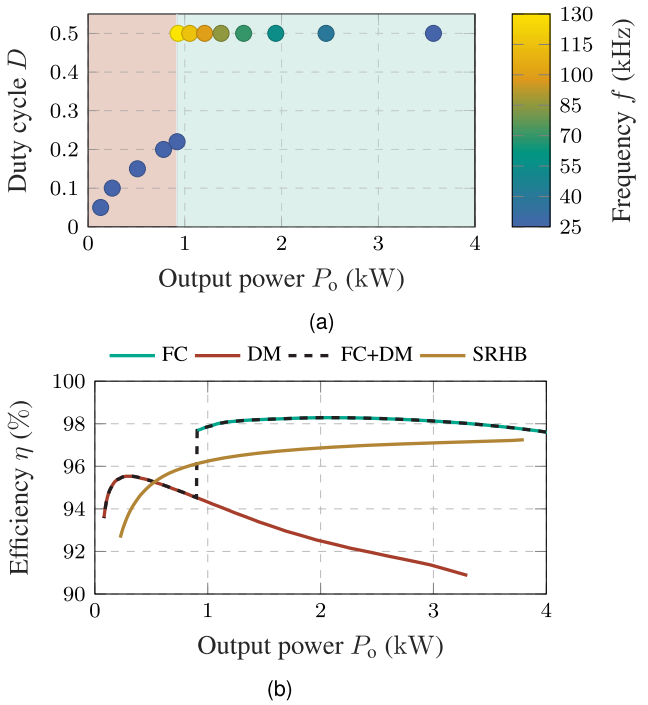

FIGURE 15. Inverter performance. (a) Experimental results of the power control strategy of the CII in DM for low output power (see red highlighted region) and with FC enabling ZVS (see green highlighted region). (b) Estimated inverter efficiency in comparison to SRHB inverter.

the current during the dead time T_d, which is determined by the resonant frequency f_{res} of value

$$f_{res} = \frac{1}{2\pi\sqrt{L_{\sigma,1/2} \cdot C_{1/2}}}. \tag{8}$$

Based on the results presented in Fig. 12, a snubber capacitor value of 2.4 nF in combination with a constant inverter dead time T_d of 800 ns gives a good compromise between a wide operation range in which ZVS is achieved and controllability of the output power without extensive increase in switching frequency.

C. MEASUREMENT RESULTS

To prove the feasibility of the inverter concept and to demonstrate the power control scheme presented in Section III-B, different experiments are performed. The experiments are performed while a pot with an outer diameter d_o of 220 mm is placed above the inductors in a vertical distance d_z of 7 mm. First, the voltage v_{21} along with the current i_o is measured for the operation of the inverter with FC at a switching frequency f of 55 kHz and a constant DC-Link voltage V_{dc} of 230 V. The current i_o is given as

$$i_o = i_{L1} - i_{L2} \tag{9}$$

with i_{L1} and i_{L2} being the current through inductors L_1 and L_2 as depicted in Fig. 5.

The measurement results are compared to simulation results in Fig. 13. Herein, the electrical circuit simulation is

(a)

(b)

FIGURE 16. **Experimental results at different operating conditions. (a) Measured waveforms of input voltage (yellow trace), input current (green trace), inverter voltage v_{21} (red trace), and current $i_{o,push}$ (blue trace) for the operation of the inverter with FC at a switching frequency *f* of 25 kHz. (b) Measured waveforms of input voltage (yellow trace), input current (green trace), inverter voltage v_{21} (red trace), and current $i_{o,fw}$ (blue trace) for operation of the inverter in discontinuous operation at a switching frequency *f* of 25 kHz with a duty cycle *D* of 0.22.**

parameterized with the values for R_p and L_p as given in Fig. 9, which results in values of 93.9 mΩ and 29.4 µH, respectively. The comparison of measurement and simulation data of the voltage v_{21} shows a good match between the proposed model and the experimental results. Especially the oscillating frequency after the switching events is nearly the same within measurement and simulation data. Greater deviation between measurement and simulation results can be observed for the load current depicted in Fig. 13(b). There is a deviation of approximately 7 A regarding the current amplitude. This is due to the fact that the magnetic nonlinear properties of the IH load is not considered in the transient electrical circuit simulations. This can be denoted by the constant slope of the load current for positive output voltage in comparison to the varying slope that occurs in the measurement data. Nevertheless, the deviation in RMS values of the load current is 22.15 A in simulation and 19.73 A for the experimental data. In this operating point, the output power, which is determined by

$$P_o = \frac{1}{T} \cdot \left(\int_0^T v_{L1} \cdot i_{L1}\, dt + \int_0^T v_{L2} \cdot i_{L2}\, dt \right) \tag{10}$$

shows a relative deviation of approximately 2.6 % between measurement and simulation results. While the measured output power $P_{o,m}$ is 1862 W, it is 1911 W within the simulation model. The output power P_o for operation of the inverter with FC at a DC-Link voltage V_{dc} of 230 V is given in Fig. 14. The comparison of measurement and simulation results shows a good match with the highest deviation for low values of frequency f. At a frequency f of 25 kHz, the measured output power is 3538 W, whereas the value obtained through simulation data is 3750 W. This corresponds to a relative derivation of approximately 6 %.

To further validate the power control strategy presented in Section III-B, experiments are performed with the inverter being operated in DM as well as with FC. To emulate the common grid, the inverter is connected to an ac power supply, which is operated with an output frequency f_g of 50 Hz and an RMS value of the output voltage V_g of 230 V. The power control strategy is depicted in Fig. 15(a), where the duty cycle D and the switching frequency f are depicted over the output power P_o. A comparison to the simulation results depicted in Fig. 10(c) shows that for a maximum switching frequency of 130 kHz, an output power P_o of 906 W is reached in simulation, while the measurement results give a value of 931 W. This corresponds to a relative deviation of 2.7 %. The estimated inverter efficiency for the different inverter operation modes of the CII is given in Fig. 15(b). It can be seen that the highest efficiency is achieved with FC under ZVS conditions with a maximum estimated efficiency of 98.3 % at 2.15 kW. However, in the low output power range FC demands for an overproportional increase of the switching frequency to further reduce the output power. This results in the risk of losing ZVS conditions at high switching frequencies. Therefore, in low output power range, the switching frequency is reduced to its minimum value of 25 kHz and the inverter is operated in DM. In this operation mode, the inverter efficiency decreases. However, comparing the efficiency of the CII with the one of the SRHB, it can be seen that the CII shows a better efficiency than the SRHB inverter, which is beneficial only in power range from 500 to 900 W. The efficiency of the SRHB is calculated according to a resonant tank design as given in [23] and assuming the use of the same SiC-MOSFETs as for the CII.

The measured waveforms of the inverter input voltage, input current, as well as the output voltage v_{21} and current i_o depicted in Fig. 16 for two exemplary operating points using FC and DM in steady-state operation prove the robustness and the feasibility of the inverter concept for operation on the common grid. When using FC, the current amplitude reaches values of approximately 100 A at a maximum value of 325 V for V_{dc} . The voltage spike during the switching transition equals approximately 900 V, validating the snubber capacitor selection and effectively damping the overshoot. Ringing effects can be observed following the switching events, which are caused by oscillations between the leakage inductance and the snubber capacitors. When the inverter operates in DM, as shown in Fig. 16(b), these oscillations become even more pronounced. Effective damping can be achieved by employing an *RC* snubber network. Nevertheless, the simulation results presented in the previous sections are validated also for operation of the inverter in DM and connection to the common voltage grid.

V. CONCLUSION

In this article, a new cost-effective nonresonant inverter topology, CII, applied to domestic IH applications is proposed. Compared to the SRHB inverter, which is the most commonly used inverter topology in domestic IH systems, no bulky resonant capacitors are necessary and the use of cost-effective low-side gate driver ICs is possible. Even though the CII only makes use of two semiconductor devices, the maximum voltage applied to the IH load can reach the DC-Link voltage V_{dc} and is, therefore, the same as in the NRFB inverter. The comparison with different inverter topologies shows that the CII is advantageous not only in terms of cost but also by offering SP capability as well as seamingless power control from zero up to the maximum power of the inverter. In comparison to the SRHB with a maximum estimated efficiency of 97.3 %, the CII reaches a higher estimated efficiency with a maximum of 98.3 %.

To achieve the aforementioned benefits, additional effort is necessary when designing the inductor, as the functional principle of the CII depends on the magnetic coupling of the two inductors L_1 and L_2. Through this, the conventional modeling approach making use of the series connection of L_{eq} and R_{eq} is not suitable when modeling the CII. Therefore, an alternative modeling approach is presented and parametrization of the model is performed in this article. In addition, to reach high efficiency, proper snubber capacitor selection is crucial, which is addressed in Section IV-B.

The measurement results over the complete output power range up to 3.6 kW prove the feasibility and robustness of the concept and its design. Moreover, in comparison to state-of-the-art resonant inverters, the CII advantageously allows to reduce the continuous power down to 0 W without flicker issues. This beneficial characteristic of the CII is proven through measurement results with a minimum continuous power of 50 W. Hence, the CII is a cost-effective and self-protective inverter topology while offering advantages in terms of minimum continuous output power, which is beneficial for specific cooking processes, e.g., melting of butter or chocolate. In addition, a higher estimated efficiency than conventional topologies is reached in a broad output power range.

APPENDIX A
DISCONTINUOUS OPERATION MODE (DM)

The following appendix describes the determination of t_1 in DM. Due to volt-second balance across the inductances L_1 and L_2, it follows:

$$\int_0^T v_1\,dt = \int_0^T v_2\,dt = \int_0^T v_{21}\,dt = 0. \tag{11}$$

For v_1, this results in

$$\int_0^T v_1\,dt = \int_0^{D\cdot T} V_{\mathrm{dc}}\,dt + \int_{D\cdot T}^{t_1} -V_{\mathrm{dc}}\,dt + \int_{t_1}^{T} -V_{\mathrm{dc}}\cdot\exp\left(-\frac{t-t_1}{\tau}\right)dt = 0. \quad (12)$$

Solving the integral leads to

$$2V_{\mathrm{dc}}\cdot DT - V_{\mathrm{dc}}\cdot t_1 + V_{\mathrm{dc}}\cdot\tau\cdot\exp\left(-\frac{T-t_1}{\tau}\right) - V_{\mathrm{dc}}\cdot\tau = 0 \quad (13)$$

and finally, to

$$2\cdot DT - t_1 + \tau\cdot\exp\left(-\frac{T-t_1}{\tau}\right) - \tau = 0. \quad (14)$$

APPENDIX B
COMPONENT REQUIREMENTS

TABLE 3. Basic Component Requirements for the Comparison of Different Inverter Topologies

Si-IGBT		
Parameter	Symbol	Value
Max. Voltage	$V_{\mathrm{CE,max}}$	$\geq 1.1\,\mathrm{kV(CII)}/\geq 600\,\mathrm{V(others)}$
Max. Current	I_{C}	$\geq 60\,\mathrm{A}$
Power Dissipation	P_{d}	$\geq 280\,\mathrm{W}$
Sat. Voltage	$V_{\mathrm{CE,sat}}$	$\leq 2\,\mathrm{V}$
Gate Driver		
Topology		Description
CII		Low-Side Gate Driver with two drivers and two outputs
Others		Half-Bridge Driver suitable for bootstrap operation up to 600 V with matching fast recovery diode
Resonant Capacitor		
Parameter	Symbol	Value
Min. DC-Voltage	$V_{\mathrm{DC,min}}$	$\geq 630\,\mathrm{V}$
Min. Capacitance	C_{min}	$220\,\mathrm{nF}$
Estim. Area (Footprint)	A_{C}	$234\,\mathrm{mm}^2$
PCB Cost	E_{PCB}	$4.069\,€/\mathrm{dm}^2$

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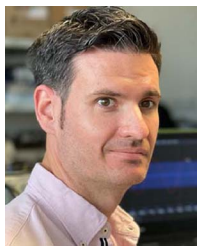

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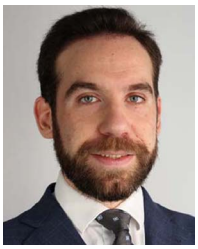

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