Application-Oriented Test Setup for Measuring Dynamic Output and Transfer Characteristics of GaN-HEMTs

1st Philipp Swoboda
Elektrotechnisches Institut (ETI)
Karlsruhe Institute of Technology (KIT)
Karlsruhe, Germany
philipp.swoboda@kit.edu

2nd Martin Fein
Elektrotechnisches Institut (ETI)
Karlsruhe Institute of Technology (KIT)
Karlsruhe, Germany
martin.fein@kit.edu

3rd Simon Frank
Elektrotechnisches Institut (ETI)
Karlsruhe Institute of Technology (KIT)
Karlsruhe, Germany
s.frank@kit.edu

4th Andreas Liske
Elektrotechnisches Institut (ETI)
Karlsruhe Institute of Technology (KIT)
Karlsruhe, Germany
andreas.liske@kit.edu

5th Marc Hiller
Elektrotechnisches Institut (ETI)
Karlsruhe Institute of Technology (KIT)
Karlsruhe, Germany
marc.hiller@kit.edu

***Abstract*—Apart from the excellent switching and conduction properties of power GaN-HEMTs, trapping effects are still an issue degrading the device's performance. As conventional methods have been proven inadequate for device characterization with respect to trapping, new application-oriented characterization methods have been developed in recent years. In this paper, an application-oriented test setup for measuring output and transfer characteristics is presented, which extends an existing setup for the measurement of the dynamic on-resistance. Initial results indicate that there is a significant change in characteristics dependent on the applied off-state drain voltage bias. Additionally, several typical trapping phenomena such as the dynamic on-resistance, threshold voltage shift and current collapse were observed.**

***Index Terms*—Dynamic on-state resistance, gallium nitride high-electron-mobility transistors (GaN-HEMT), power semiconductor device characterization, conduction-losses, double pulse test (DPT), threshold voltage shift, transfer and output characteristics**

I. Introduction

Trapping effects such as threshold voltage shift or $V_{\mathrm{gs,th}}$-shift, the dynamic on-resistance $dR_{\mathrm{ds,on}}$ and current collapse are still present in today's power GaN-HEMTs. Those effects are mainly stimulated by applying a gate or a drain voltage bias to the device, when it is blocking. Previous investigations have shown that the impact of those effects on the device's performance depends on the magnitude and duration of the applied voltage bias [1]–[4]. In many cases, those effects are reversible, if a relaxation interval is inserted in which the biases are removed.

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Conventional methods for device characterization, as used for Si-based devices, are often inadequate, as the device is operated under idealistic conditions and not in an application-oriented scenario. The influence of trapping is neglected, since no preconditioning with drain or gate bias is applied to the device under test (DUT) prior to the measurement. To tackle that issue, several application-oriented characterization methods have been developed in recent years. In the majority of publications, the dynamic on-resistance $dR_{\mathrm{ds,on}}$ was investigated, mostly in a modified double pulse test (DPT) setup, which is close to an actual power electronic converter [1], [5]–[7].

Further, the $V_{\mathrm{gs,th}}$-shift phenomenon gained academic attention in recent years [2], [3]. In [2], the standardized method according to IEC60747-8-4 [8] for evaluation of the threshold voltage $V_{\mathrm{gs,th}}$ was expanded by additional circuitry to allow investigations on the $V_{\mathrm{gs,th}}$-shift phenomenon under consideration of drain- and gate-bias. The applied drain-bias V_{ds} during the $V_{\mathrm{gs,th}}$-measurement was kept at a constant low voltage of $2.4\,\mathrm{V}$, which is much lower than a typical V_{ds} in a real hard-switching application. This, however, allows a more isolated investigation of the $V_{\mathrm{gs,th}}$-shift, as V_{ds}-dependent effects, such as Drain-Induced Barrier Lowering (DIBL), do not occur. Strong $V_{\mathrm{gs,th}}$-shifts of up to $500\,\mathrm{mV}$ were observed both under applied drain and gate bias in [2], with time constants of up to the hour range.
The test circuit presented in [3] allows $V_{\mathrm{gs,th}}$-measurements, whilst a V_{ds}-bias of up to $400\,\mathrm{V}$ is applied. Thereby, the DUT was switched under zero load current, which is more close to a real application and includes V_{ds}-dependent effects like DIBL. The results show a significant time-dependent $V_{\mathrm{gs,th}}$-shift.

Further, the output characteristics was measured using a device analyzer. Thereby, a V_{ds}-bias of $400\,\mathrm{V}$ was applied prior to the measurement. The result was a poorer performance of the device, indicated by an increased $R_{\mathrm{ds,on}}$, a knee-point that was shifted downwards and a decreased saturation current.
However, no previous work has been found that investigates those "dynamic" output and transfer characteristics in a converter-like setup, as it was done especially in the $dR_{\mathrm{ds,on}}$-investigations [1], [4].

In this paper, a test setup is presented, which is capable of measuring both transfer and output characteristics with respect to trapping, which includes the evaluation of the threshold voltage $V_{\mathrm{gs,th}}$. It extends an existing test setup to investigate the dynamic on-resistance $dR_{\mathrm{ds,on}}$ [4]. The measurement is carried out in a converter-like setup, whereby the DUT is switched under an inductive load, as often the case in a real power electronics application. Similar to [3], the threshold voltage $V_{\mathrm{gs,th}}$ can be measured as a part of the transfer characteristics under fully applied blocking voltage V_{ds} of up to $400\,\mathrm{V}$. This makes the characterization very close to the application.

The paper is structured as follows: First, the test circuit with its auxiliary circuitry around the DUT is described. This is followed by a description of the proposed measurement procedures for transfer and output characteristics. Subsequently, a short description of the practical test setup is provided. Finally, first measurements are shown and their results discussed.

II. Description of the Test Circuits

A. Overview

The main part of the test setup is an advanced DPT-circuit, consisting of a full bridge with one additional device LS1 connected in parallel to the DUT (Fig. 1). As with most power electronic circuits, an inductive load L_{DPT} is used, which is connected between the two switching nodes. The additional

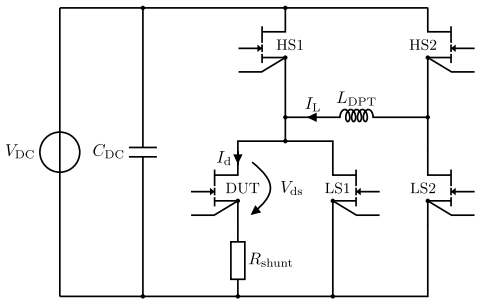

Fig. 1: Modified Double Pulse Circuit

device LS1 is required for the test procedures, to i.a. reduce the self-heating of the DUT. Its further purposes are described in the following sections.
In contrast to a conventional DPT setup, the given setup allows to control the applied drain-bias $V_{\mathrm{ds,IDLE}}$ on the DUT, when no measurement is performed. By switching HS1 and HS2 on, $V_{\mathrm{ds,IDLE}}$ becomes the DC-link voltage V_{DC}, whereas when LS1 and LS2 are turned on, $V_{\mathrm{ds,IDLE}}$ becomes zero. This ability is crucial to control the trapping effects of GaN-HEMTs. The test circuit was first introduced in [4], where it

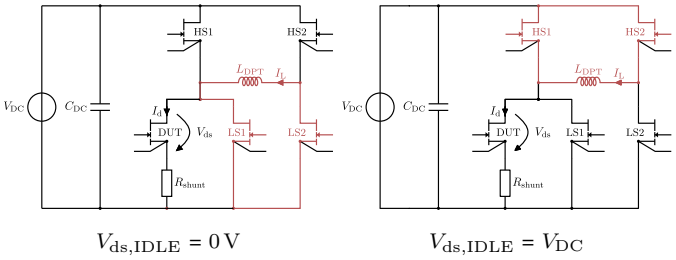

Fig. 2: Idle states for drain-bias preconditioning

was used for $dR_{\mathrm{ds,on}}$-measurements. In this paper, the circuit is expanded by additional circuitry, which enables output and transfer characteristics measurements.

B. Adaptive Gate Driver

As the procedure for transfer characteristics requires a slowed-down hard-switching event, the rise time at the gate needs to be adjustable down to several hundreds of nanoseconds. Further, for measuring the output characteristics at different magnitudes of the gate voltage V_{gs}, the gate driver must be capable of adjusting its output voltage. At the same time, parasitic turn-on of the DUT must be prevented, which requires a low-impedance path from the gate to the source in the off-state.

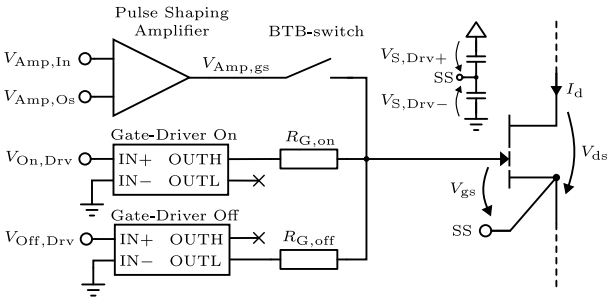

Fig. 3: Adaptive Gate Driver

To meet those requirements, an adaptive gate driver is required which is depicted in Fig. 3. It consists of a pulse shaping amplifier (PSA) and two commercially available gate-drivers [9], which are supplied by two adjustable bipolar power supply rails $V_{\mathrm{S,Drv+}}$ and $V_{\mathrm{S,Drv-}}$. The gate-drivers feature two outputs each, one for turn-on (OUTH) and another one for turn-off (OUTL). By combining their logic inputs $V_{\mathrm{On,Drv}}$ and $V_{\mathrm{Off,Drv}}$ and by tieing their outputs together via the gate resistors $R_{\mathrm{G,on}}$ and $R_{\mathrm{G,off}}$, a gate-driver with tristate-output is formed. The gate can either be left floating or be tied to $V_{\mathrm{S,Drv+}}$ or $V_{\mathrm{S,Drv-}}$ via the gate resistors (see TABLE I).
Although the two gate-drivers can provide a low-impedance path from the gate to the supply rails, they cannot adjust

TABLE I: Truth Table of the formed Tristate Gate-Driver

$V_{\mathrm{On,Drv}}$	$V_{\mathrm{Off,Drv}}$	V_{gs}
H	H	$V_{\mathrm{S,Drv+}}$
L	L	$V_{\mathrm{S,Drv-}}$
L	H	Floating
H	L	Forbidden

V_{gs} in magnitude and speed. This feature is provided by a PSA (Fig. 4), which can be connected to the gate-node of the DUT using two back-to-back (BTB)-connected transistors. Its output voltage $V_{\mathrm{Amp,gs}}$ is controlled by the two inputs $V_{\mathrm{Amp,In}}$ and $V_{\mathrm{Amp,Os}}$. Both of them are generated by a digital-to-analog converter (DAC). To filter out the stairs of

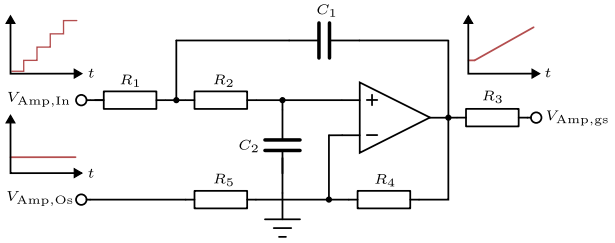

Fig. 4: Pulse Shaping Amplifier

the DAC-signal, $V_{\mathrm{Amp,In}}$ is smoothed by a Sallen-Key low-pass filter [10], which is composed of R_1, R_2, C_1 and C_2. Due to its low magnitude, $V_{\mathrm{Amp,In}}$ does not fit the required range of V_{gs}, which can be for instance from $-6\,\mathrm{V}$ to $6\,\mathrm{V}$. Thus, amplification and offset shift is required. This feature is provided by the non-inverting amplifier part of the PSA, formed by R_4 and R_5. The offset is thereby controlled by $V_{\mathrm{Amp,Os}}$. As $V_{\mathrm{Amp,Os}}$ is a DC-signal, there is no need for filtering. The DC transfer function of the PSA is

$$V_{\mathrm{Amp,gs}} = V_{\mathrm{Amp,In}} \cdot \left(1 + \frac{R_4}{R_5}\right) - V_{\mathrm{Amp,Os}} \cdot \frac{R_4}{R_5} \,. \qquad (1)$$

Note that it is not possible that both the PSA and the gate-drivers are active at the same time. If the gate of the DUT needs to be charged with a reduced and adjustable speed to a certain magnitude, the two gate-driver outputs OUTH and OUTL need to be left floating and the BTB-switch needs to be turned on, which connects the PSA to the gate. Outside the measurement phase or when the inductor is charging, the gate potential is pulled against the $V_{\mathrm{S,Drv-}}$-potential, providing a low-impedance path, whilst the BTB-switch is turned off.

C. Clamp Circuit

As the DUT can see blocking voltages of up to $400\,\mathrm{V}$ while the on-state voltages are no higher than $15\,\mathrm{V}$, a clamp circuit is required. This enables measurements of the on-state drain voltage V_{ds} with high accuracy, which is required for the output characteristics. The actively controlled clamp circuit is depicted in Fig. 5 and was already described in [4]. The

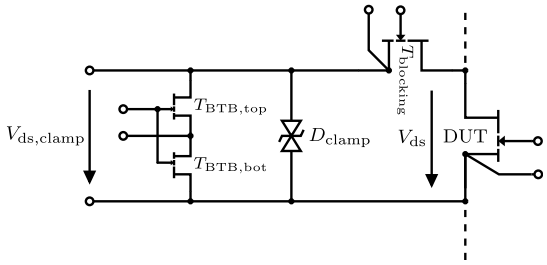

Fig. 5: Clamp Circuit with High Accuracy

only difference is the choice of the TVS-diode D_{clamp}, which has now a higher clamp voltage V_{clamp} of $19\,\mathrm{V}$, extending the measurement range to about $\pm 15\,\mathrm{V}$. With the higher measurement range, the output characteristics can be acquired for V_{ds} of up to $15\,\mathrm{V}$.

D. High-Voltage Comparator

A high-voltage comparator is crucial for the operation of the actively controlled clamp circuit and the measurement procedure for the output characteristics. The simplified circuitry is depicted in Fig. 6. The task of the comparator is to check whether V_{ds} has fallen below a certain threshold $V_{\mathrm{Comp,th}}$, such as $12\,\mathrm{V}$. If that is not the case, the clamp circuit must

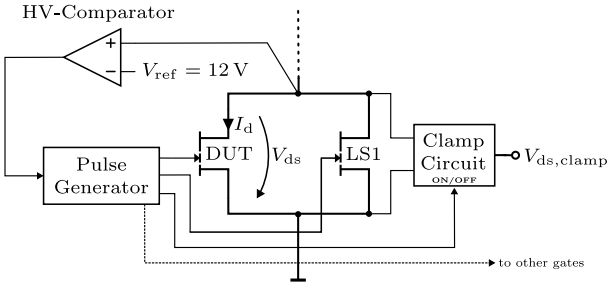

Fig. 6: Simplified Circuitry of the High-Voltage Comparator

not turn-on, to prevent damage to the clamp circuit or to the measurement equipment. This situation can be caused, for instance, when V_{gs} is below $V_{\mathrm{gs,th}}$. In this case, V_{ds} will not drop. Further, during an output characteristics measurement, the comparator has to check whether V_{ds} exceeded the threshold, to turn-off the clamp circuit and to turn-on the bypass switch LS1. More details about that are given in the following section.

III. Measurement Procedures

A. Transfer Characteristics

The procedure for measuring transfer characteristics is depicted in Fig. 7. The individual steps of the procedure are separated in time by the vertical grey bars and numbered as follows:

① Inductor charging phase
② Freewheeling phase
③ Measurement phase
④ Idle state

First the inductor L_{DPT} is charged by switching on HS2 and LS1 ①. The duration of this phase defines the maximum drain current I_{d} of interest in the transfer characteristics curve. Second, a freewheeling phase ② is inserted by only turning HS2 on, while HS1 is left in the off-state. As the current I_{L} is positive, the current will flow through HS1 in reverse. Finally, the measurement phase ③ is initiated by applying a V_{gs}-ramp with adjustable ramp-time t_{ramp} and adjustable final value $V_{\mathrm{gs,max}}$ to the DUT. The current slowly commutates from HS1 to the DUT as depicted in Fig. 7, while V_{gs} is increasing to its final value $V_{\mathrm{gs,max}}$.

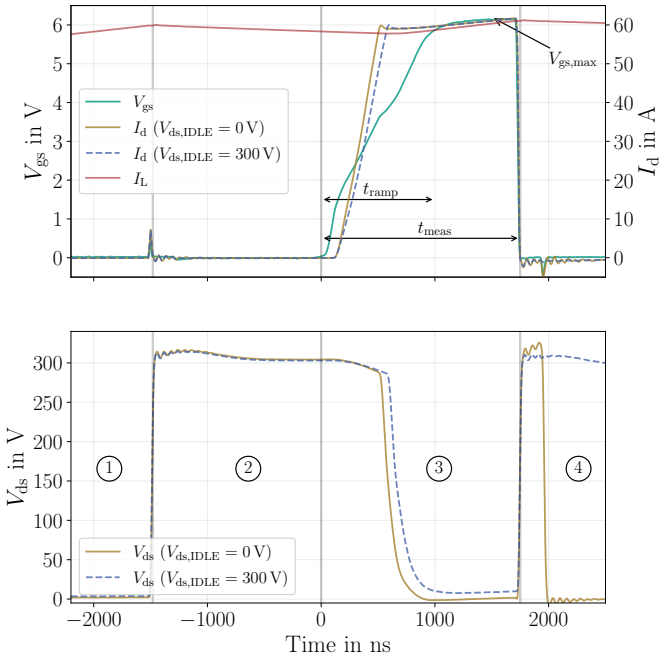

Fig. 7: Procedure for Transfer Characteristics Measurement

The choice of the ramp-time t_{ramp} is crucial for the accuracy of the measurement. For an ideal measurement, the channel current I_{ch} equals the measurable drain current I_{d} and the internal gate voltage $V_{\mathrm{gs,int}}$ equals the measurable gate voltage at the terminals V_{gs}. Due to the parasitic capacitances, inductances and resistances of the transistor (see Fig. 8), this can never be the exact case, as their currents and voltage drops affect the measurable quantities I_{d} and V_{gs}. Those parasitic effects, however, can be weakened significantly by slowing down the switching speed. Slower switching speeds also allow to filter the signals, which reduces the noise of the measurement. In contrast, when the switching speed is set too slow, the self-heating of the DUT can become excessive, as the switching energy heavily increases due to larger overlap in time of V_{ds} and I_{d}. Therefore, the optimal t_{ramp} has to be examined by performing circuit simulations including the thermal model of the DUT.

From Fig. 7 another effect can be seen: The drain voltage V_{ds} is smaller than V_{DC} while the current I_{d} is increasing. This voltage drop is mainly caused by the resistive elements in the loop, such as the current shunt, the Equivalent Series Resistance (ESR) of the DC-link capacitor and the tracks on the PCB. As soon as the drain current I_{d} has reached the inductor current I_{L}, the main drop of V_{ds} is initiated, at which V_{DC} is gradually taken over by HS1.

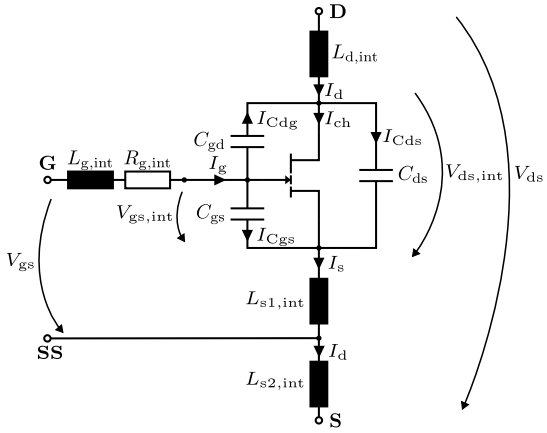

Fig. 8: Equivalent Circuit of a GaN-HEMT with parasitics

It is apparent that the procedure is very close to a real hard-switching turn-on event. The only difference is that the switching speed of an actual application is much higher. By plotting the drain current I_{d} against the gate-source voltage V_{gs}, the transfer characteristics at $V_{\mathrm{ds}} \approx V_{\mathrm{DC}}$ is obtained. After the measurement phase with the duration t_{meas} is finished, either HS1 and HS2 or LS1 and LS2 will be switched on ④, to define $V_{\mathrm{ds,IDLE}}$ to be V_{DC} or 0 V, until the next measurement is conducted.

B. Output Characteristics

The procedure for the output characteristics is depicted in Fig. 9. In short, it consists of the following steps:

① Charge the gate of the DUT to the desired V_{gs}
② Measurement interval
③ Optional: Turn on LS1, if V_{ds} exceeds 12 V
④ Idle state (Upper freewheeling state in the given case)

The idle state ④ is left by applying a gate-source voltage V_{gs} to the DUT ①. If V_{gs} is above $V_{\mathrm{gs,th}}$, the drain-source voltage V_{ds} of the DUT will drop. Subsequently, HS2 is turned on, which causes the inductor current I_{L} to rise. The maximum possible drain current I_{d} and on-time of the DUT is defined by the duration of the measurement interval t_{meas}, when the DUT and HS2 is turned on at the same time ②.
While I_{d} is increasing, the drain-source voltage V_{ds} of the DUT increases as well due to the $R_{\mathrm{ds,on}}$. If the current I_{d} is high enough for a certain V_{gs}, the saturation region is reached, which leads to a faster increase of V_{ds}. In case V_{ds} exceeds the comparator threshold $V_{\mathrm{Comp,th}}$ of 12 V, the inductor current I_{L} will be bypassed through switch LS1, which prevents V_{ds} to increase further and terminates the measurement phase. This optional step ③ is necessary to avoid destruction of the DUT due to excessive self-heating.
Fig. 9 shows both cases, with and without the optional step.

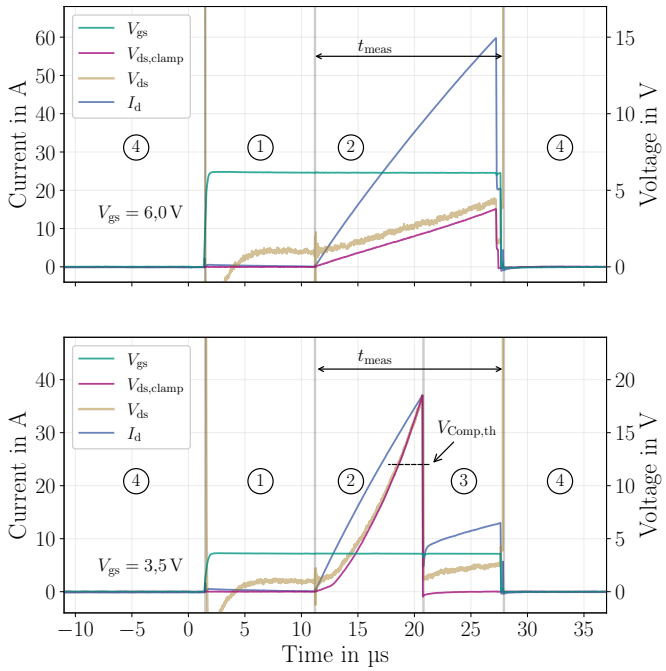

Fig. 9: Raw Data of Output Characteristics Measurement at $V_{ds,IDLE}$ = 300 V

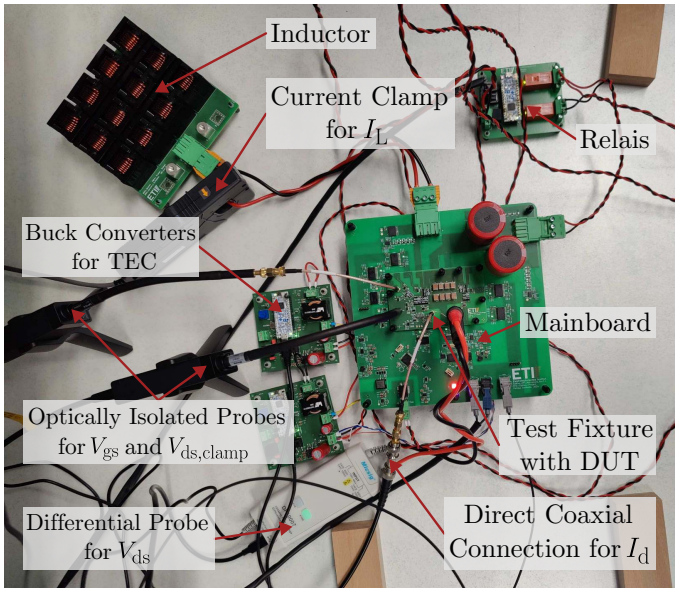

Fig. 10: Picture of the Test Setup

In the lower graph for $V_{gs} = 3.5\,V$, the drain current I_d becomes high enough to reach the saturation region and exceeds $V_{Comp,th}$. The sudden drop of I_d close to $V_{Comp,th}$ indicates that LS1 was switched on. Both switches are operating in parallel in this case. In the upper graph with $V_{gs} = 6.0\,V$, the DUT remains in the linear region and the measurement is terminated, when the interval t_{meas} has elapsed.

By plotting I_d against V_{ds} within the measurement interval ②, the output characteristics at the desired gate-source voltage V_{gs} is obtained. After the measurement has finished, $V_{ds,IDLE}$ is applied at the DUT ④. In contrast to the procedure for the transfer characteristics, the parasitic influence on the measurement, except self-heating, is negligibly small. This arises from the fact, that the slopes of I_d and V_{ds}, that cause parasitic voltage drops and currents, are several magnitudes slower than it is the case with the transfer characteristics measurement. Nevertheless, it is reasonable to perform circuit simulations, to assess self-heating.

IV. Practical Realization of the Test Setup

As already mentioned, the given test setup depicted in Fig. 10 is an expansion of the one introduced in [4]. The major part is the mainboard, on which the exchangeable test fixture is mounted. Further, it contains the control circuit, which includes the circuits introduced in section II. On the test fixture, the DUT is mounted together with the test circuit depicted in Fig. 1. It further employs coaxial connectors for the connection of the measurement equipment to measure the signals of interest I_d, V_{gs}, $V_{ds,clamp}$ and V_{ds}. Both V_{gs} and $V_{ds,clamp}$ are measured using two optically isolated differential probes of the type *SigOFIT MOIP02P* from *Miscsig* [11]. The current is measured using shunt-resistors with a total resistance of $40\,m\Omega$, which are mounted on the test fixture. As the voltage drop on the shunt resistors can be very small, the voltage is measured directly with the oscilloscope via a series termination and a coaxial cable to achieve a good measurement accuracy. For additional monitoring of the applied drain-bias, the drain source voltage V_{ds} is measured using a conventional differential probe. Not shown in Fig. 10 is the oscilloscope, which is a *WavePro 404HD* with 4 GHz bandwidth, 12-bit resolution and 0.5 % full-scale gain accuracy from *LeCroy* [12].

Due to the strong temperature coefficient of GaN-HEMTs, it is important to conduct the measurements at a defined temperature. This is achieved by using a thermoelectric cooler (TEC), which allows a temperature control with high dynamic [4]. The TEC is powered by two back-to-back connected buck converters, which are also shown in Fig. 10. The controlled variable is the case temperature T_c of the DUT, which is measured with a thermally well-connected NTC-resistor.

The voltage V_{DC} is provided by a high voltage power supply, whose poles are disconnected during a measurement using two relais, to reduce common-mode disturbances.

V. Measurements and Discussion

A. Measurement Conditions

The following measurements are carried out using the GS66508B GaN-HEMT with a Schottky p-GaN gate from GaN-Systems. It has a current rating of 30 A and a voltage

rating of 650 V. In the off-state of the DUT, the gate-source voltage V_{gs} is set to 0 V. The charging time of the inductor L_{DPT}, which is t_{charge} for the transfer characteristics and t_{meas} for the output characteristics, is always set such that the desired current I_{d} is reached. The inductance L_{DPT} has a nominal value of 90 µH. Further, the case temperature T_{c} is kept constant at 25 °C using the TEC-based temperature control. These conditions apply to all measurements.

Whenever the drain-bias $V_{\mathrm{ds,IDLE}}$ is changed, a relaxation time of 20 min is introduced to ensure that the traps are in a steady state. However, since trapping effects are also caused by any gate stress V_{gs}, the influence of this on the treshold voltage $V_{\mathrm{gs,th}}$ is the first part of the investigation. The threshold voltage $V_{\mathrm{gs,th}}$ is defined at the threshold, when the drain current I_{d} exceeds 100 mA. For all transfer characteristics measurements or $V_{\mathrm{gs,th}}$-measurements, the ramp time t_{ramp} is set to 1 µs.

The transient junction temperature rise ΔT_{j} due to self-heating was simulated with the thermal model from the datasheet [13]. It was shown, that ΔT_{j} completely decayed within one second after a measurement. Thus, if the interval between two consecutive measurements t_{IDLE} is chosen larger than one second, T_{j} is not expected to accumulate.
For the output characteristics, ΔT_{j} was always below 10 K for currents I_{d} of up to 60 A. For the transfer characteristics, ΔT_{j} was 0.5 K at 5 A, 10 K at 30 A and 30 K at 60 A.
Consequently, except for the $V_{\mathrm{gs,th}}$-measurements at 5 A, self-heating can not be neglected. However, as the pulse pattern applied to the DUT is identical with and without applied drain-bias $V_{\mathrm{ds,IDLE}}$, this is not expected to affect the general outcome of the result.

B. Consideration of the Threshold Voltage Shift

Any voltage V_{gs} applied to the gate results in a $V_{\mathrm{gs,th}}$-shift. To acquire the characteristics, charging of the gate is essential, which in turn means that trapping at the gate or $V_{\mathrm{gs,th}}$-shift always occurs.
For reproducible measurements, these influences must be taken into account and by an appropriate timing of the measurements, the $V_{\mathrm{gs,th}}$-shift can be kept at an almost constant level. The measurements need to be conducted periodically, with a constant measurement time t_{meas}, when a voltage is applied to gate and a constant resting time t_{IDLE}, when V_{gs} is zero.

Fig. 11 shows measurements of the time dependency of $V_{\mathrm{gs,th}}$ at different $V_{\mathrm{gs,max}}$, t_{IDLE} and t_{meas}. The measurements were conducted at a very low V_{DC} of 5 V with zero drain bias $V_{\mathrm{ds,IDLE}}$, to minimize the impact of drain-induced trapping and DIBL. In addition, the current I_{d} was limited to 5 A, to minimize self-heating and to allow a reduced full-scale range of the oscilloscope, resulting in a more accurate determination of $V_{\mathrm{gs,th}}$. Between every measurement curve, the DUT rests for 10 min, to restore the initial state of $V_{\mathrm{gs,th}}$. This can be

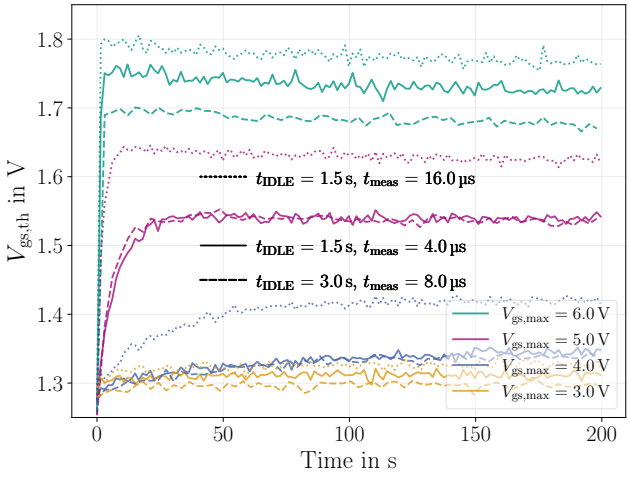

Fig. 11: Time dependency of $V_{\mathrm{gs,th}}$-shift

recognized by the fact that all curves start at $V_{\mathrm{gs,th}} \approx 1.27\,\mathrm{V}$. It can be seen that the greatest change of $V_{\mathrm{gs,th}}$ for all curves occurs within the first hundred seconds. After that, $V_{\mathrm{gs,th}}$ changes only in low tens of mV-steps. Further, the higher $V_{\mathrm{gs,max}}$, the higher the $V_{\mathrm{gs,th}}$-shift and the smaller the trapping time constant. For $V_{\mathrm{gs,max}}$ smaller than 3.0 V, the $V_{\mathrm{gs,th}}$-shift becomes negligibly small and is therefore not depicted in Fig. 11. When comparing different combinations of t_{IDLE} and t_{meas}, a different steady state $V_{\mathrm{gs,th}}$ was observed in most of the cases. Two measurements are therefore only comparable, if their t_{IDLE} and t_{meas} are identical.

In order to obtain reproducible measurements, it is crucial that $V_{\mathrm{gs,th}}$ is in a steady state. For the transfer characteristics measurements this state can be achieved, by always setting $V_{\mathrm{gs,max}}$ to 6 V. In this case, $V_{\mathrm{gs,th}}$ reaches its steady state within a couple of measurements or seconds. By only considering the last of ten consecutive measurements, the transfer characteristics measurement becomes reproducible.
The output characteristic measurement, on the other hand, is associated with greater effort, as the measurements have to be conducted at different on-state V_{gs}. Between each output characteristics curve, defined at a certain V_{gs}, a resting time of 10 min has to be inserted. Further, much more consecutive measurements have to be conducted, until $V_{\mathrm{gs,th}}$ has reached its steady state. With $t_{\mathrm{IDLE}} = 1.5\,\mathrm{s}$ and 60 consecutive measurements, reproducible results can be produced, by only considering the last measurement.

C. Transfer Characteristics

Two major effects, that significantly affect the transfer characteristics, are part of the investigation: The DIBL-effect and trapping induced by applying a drain-bias $V_{\mathrm{ds,IDLE}}$ in the off-state. All measurements are conducted periodically, consisting of ten consecutive measurements, as described earlier, with $t_{\mathrm{meas}} = 4.0\,\mu\mathrm{s}$ and $t_{\mathrm{IDLE}} = 1.5\,\mathrm{s}$.

In Fig. 12 the influence of V_{ds} on the steady state $V_{\mathrm{gs,th}}$ at different $V_{\mathrm{ds,IDLE}}$ is shown. As expected, the DIBL-effect occurs and significantly affects the threshold voltage $V_{\mathrm{gs,th}}$. Between 100 V and 400 V, this effect is noticeably stronger, if a drain-bias $V_{\mathrm{ds,IDLE}}$ is applied in the pauses between the measurements, as the absolute sensitivity $\|dV_{\mathrm{gs,th}}/dV_{\mathrm{ds}}\|$ is much higher. However, this is not the case within the first 50 V. In this case, the curve for $V_{\mathrm{ds,IDLE}} = 0\,\mathrm{V}$ shows a stronger slope.

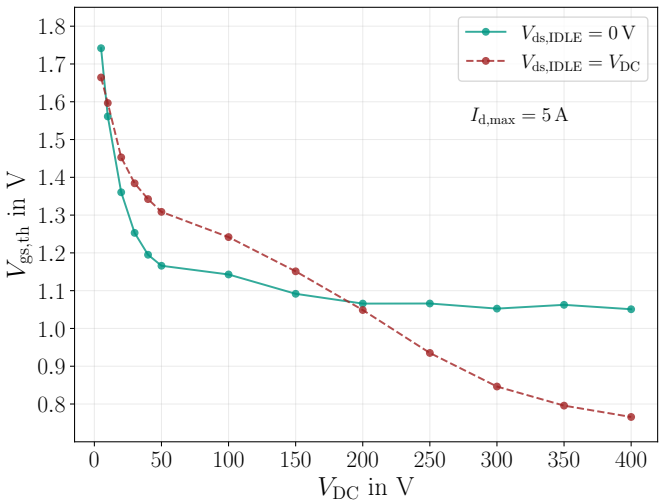

Fig. 12: Influence of V_{ds} on $V_{\mathrm{gs,th}}$ (DIBL-effect)

Important to mention is that $V_{\mathrm{gs,th}}$ at zero drain bias $V_{\mathrm{ds,IDLE}}$ and $V_{\mathrm{DC}} = 5\,\mathrm{V}$ is 1.72 V, which is very close to the typical value of 1.7 V from the datasheet of the DUT [13]. Here, $V_{\mathrm{gs,th}}$ was defined at $I_{\mathrm{d}} = 7\,\mathrm{mA}$, while the DUT was operated as diode-connected transistor.

The actual transfer characteristics at chosen V_{DC} and different $V_{\mathrm{ds,IDLE}}$ is shown in Fig. 13. It can be clearly seen, that the curves for a V_{DC} of 300 V increase earlier than the curves for 100 V. This indicates the DIBL-effect and coincides with the results shown in Fig. 12. As shown in Fig. 12, this effect appears to be stronger, if a drain-bias $V_{\mathrm{ds,IDLE}}$ is applied in the off-state of the DUT. Further, the slope or transconductance g_{m} of the curves differs dependent on $V_{\mathrm{ds,IDLE}}$ and is lower, if a bias $V_{\mathrm{ds,IDLE}}$ is applied. The transconductance g_{m}, however, does not appear to be significantly affected by V_{DC}.
If the average transconductance $\hat{g}_{\mathrm{m}}$ is considered between 10 A and 50 A, the result for $V_{\mathrm{ds,IDLE}}$ of V_{DC} is about $25\,\mathrm{A\,V^{-1}}$. For a $V_{\mathrm{ds,IDLE}}$ of 0 V, one obtains about $30\,\mathrm{A\,V^{-1}}$.

Consequently, a reduced transconductance leads to a lower current rise during switching, as it can also be seen in Fig. 7. In [3], switching transients are shown with and without applied drain-bias $V_{\mathrm{ds,IDLE}}$, that yield a slower current rise, after a $V_{\mathrm{ds,IDLE}}$ was applied for 30 min. Further, a turn-on loss increase of 20 % was reported.

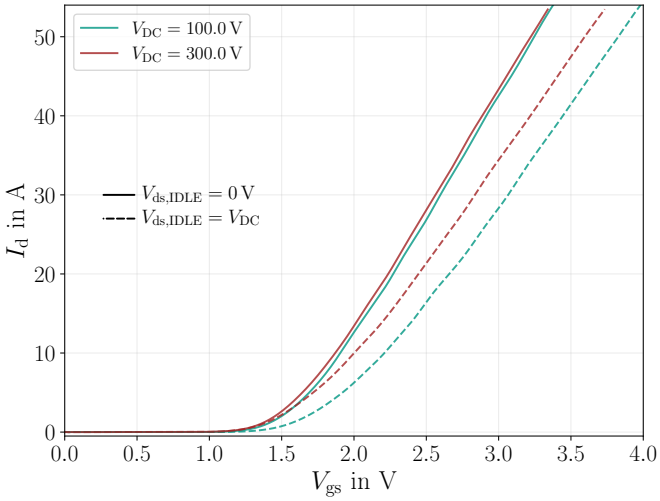

Fig. 13: Transfer Characteristics Comparison

D. Output Characteristics

For the output characteristics measurements, a maximum drain-current I_{d} of 60 A was chosen, while the resting-time t_{IDLE} between two periodical measurements was set to 1.5 s. As described earlier, the result was extracted only from the last measurement, after 60 measurements were performed. In Fig. 14 the output characteristics at $V_{\mathrm{DC}} = 100\,\mathrm{V}$ with

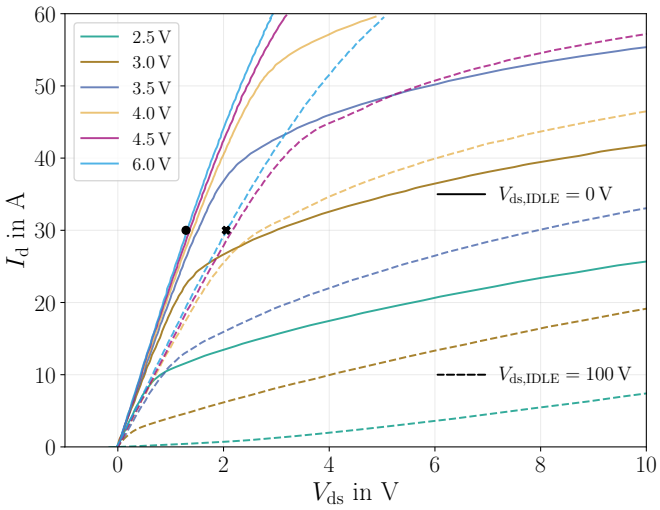

Fig. 14: Output Characteristics Comparison at $V_{\mathrm{DC}} = 100\,\mathrm{V}$

and without applied drain-bias $V_{\mathrm{ds,IDLE}}$ are shown. It can be clearly seen, that the curves for an applied drain-bias $V_{\mathrm{ds,IDLE}}$ indicate a poorer performance than the curves without bias. First, the slope of the linear region is reduced. From particular interest is the slope at $V_{\mathrm{gs}} = 6\,\mathrm{V}$, as this refers to the on-resistance $R_{\mathrm{ds,on}}$. Without applied bias $V_{\mathrm{ds,IDLE}}$, the on-resistance $R_{\mathrm{ds,on}}$ at the rated current $I_{\mathrm{d}} = 30\,\mathrm{A}$ is $46.2\,\mathrm{m\Omega}$ (•), which comes close to the value of $50\,\mathrm{m\Omega}$ from the datasheet [13]. With the bias $V_{\mathrm{ds,IDLE}}$ applied, the on-resistance $R_{\mathrm{ds,on}}$ is $76.2\,\mathrm{m\Omega}$ (✖), which results in an increase

of 65 %.
Second, the knee point of the characteristics is shifted towards lower currents and the saturation current is decreased. For a V_{gs} of 2.5 V, the linear region seem to disappear completely and the curve looks similar to the characteristics of a diode. The decrease of the saturation current correlates with the transfer characteristics measurements, as g_{m} is reduced with applied drain-bias $V_{\mathrm{ds,IDLE}}$. It can be assumed, that the shifted knee point, the disappearing linear region at low V_{gs} and the reduced g_{m} refers to the current collapse effect [14].

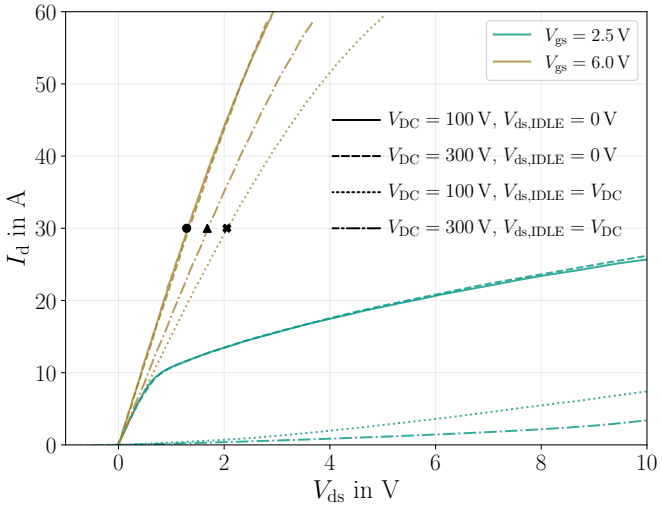

Fig. 15: Output Characteristics Comparison at different V_{DC}

In Fig. 15 the output characteristics at two different V_{DC}, 100 V and 300 V, is shown. As expected, the curves without drain-bias $V_{\mathrm{ds,IDLE}}$ coincide. In this case, the DIBL-effect does not occur, as the DUT is switched under zero voltage. At an applied bias $V_{\mathrm{ds,IDLE}}$ of 300 V, the $R_{\mathrm{ds,on}}$ is 59.3 mΩ (▲), which is 28 % more than the original value at $V_{\mathrm{ds,IDLE}} = 0\,\mathrm{V}$. This voltage-dependency indicates the effect of the dynamic on-resistance $dR_{\mathrm{ds,on}}$, which is reported in earlier investigations [1], [4]. Both studies reported that the $dR_{\mathrm{ds,on}}$ is reduced towards higher V_{DC}. It should be also noted, that all three $R_{\mathrm{ds,on}}$-values are very close to the results from our previous $dR_{\mathrm{ds,on}}$-investigation [4]. In this case, the same DUT was used, but from a different batch.

VI. Conclusions and Future Work

Within this contribution, new methods are provided to measure the transfer and output characteristics of GaN-HEMTs in an environment that is close to an actual power converter. Those methods were already realized in a practical test setup and results were provided. The results show, that trapping stimulated by gate and drain bias significantly affects the device's characteristics. It could be shown that the effect of the dynamic on-resistance $dR_{\mathrm{ds,on}}$ and the threshold voltage shift are present in the investigated DUT. Further, we assume that the current collapse effect still occurs, because of the i.a. reduced transconductance g_{m} and the shifted knee point, after a drain bias $V_{\mathrm{ds,IDLE}}$ was applied for 20 min.

Future studies could focus on the variation between different batches, different DUTs with different gate structures and the influence of the temperature on the characteristics. Thanks to the modular design of the test setup and the already existing temperature control using a TEC, the prerequisites for those investigations are given.
In addition, the switching losses and conduction-losses could also be investigated. An initial study already reported increased switching losses under the influence of trapping [3]. If the variation between the different batches is moderate, compact models can be developed using the obtained data, that include the influence of trapping.

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