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Realistic behavioral model for ReRAMs capturing non-idealities



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Memristors are a class of emerging electronic devices for in-memory computation systems, which promise to overcome the von Neumann bottleneck in traditional computer architectures. Simulation plays a critical role in designing circuits for memristive in-memory computation systems. Fast and reliable simulations require a behavioral model that accurately emulates device characteristics, accounting for real-world non-idealities. In this work, we present a memristor behavioral model that incorporates key non-idealities, including cycle-to-cycle and device-to-device resistance variations, threshold voltage variations, resistance drift in the absence of external stimulus and variations in switching dynamics. The model has been fitted to experimental data from two types of real devices: vacuum-processed self-directed channel memristors and inkjet-printed electrochemical metallization memristors, showing good agreement with both datasets. This model is used to simulate memristive stateful logic gates. Our study highlights the significance of considering device non-idealities in the practical design of memristive circuits.

Memristors are a class of two-terminal electronic components whose internal resistance is determined based on the history of applied external voltage or current. A memristor can be programmed in a non-volatile manner into a high- or low-resistive state (or a state in between)^{1–3}. This unique feature was initially exploited for non-volatile memory and is recently gaining more and more interest in in-memory computation (IMC) systems^{4–6}. IMC is a solution to overcome the von Neumann bottleneck, i.e., the limited throughput and large energy consumption in computing systems due to the intensive data movement between the separated memory and processing units⁷. In memristive-based IMC systems, the non-volatile resistive switching characteristics are exploited to store data and perform in-situ computational tasks within the memory cell itself^{4–6}. The IMC systems are expected to provide high-performance and low-power computing platforms, which will facilitate further development of data-intensive applications and enhance their performance.

One promising implementation of memristive IMC systems relies on stateful logics, in which the logic inputs and outputs are represented by the state (i.e., resistance level) of memristors, and the Boolean operations are achieved by conditional resistive switching between memristors^{6,8}. Realizing a functioning memristor-based IMC circuit requires the synergy of multiple stateful logic gates incorporated in a memristive crossbar. Therefore, simulation is an important step in assessing and optimizing the design of a memristive IMC circuit. An accurate, fast, and compact behavioral model is

crucial for a reliable and computationally efficient simulation. The importance of such a model is further heightened in the memristive circuits and systems community since access to this technology is significantly more limited than traditional complementary metal-oxide semiconductor (CMOS), and simulation is the key design tool in the community. For larger circuits, this challenge is further aggravated not only because the access is more limited but also because the time necessary for simulations using physics-based models grows exponentially, limiting the size of circuits that can be simulated. This makes the design of circuits with practical relevance very difficult since the correct functionality of a conceptual circuit heavily depends on technological parameters as well as the non-idealities of the devices in that given technology. Here, circuit-technology co-design is crucial as it ensures that both the circuit and the underlying technology are optimized synergistically. By considering the unique characteristics and limitations of the underlying technology, engineers can address potential issues at the early stage of the circuit design, which will eventually yield multiple desirable attributes of the circuits, including enhanced reliability, reduced power consumption, increased speed, and improved scalability. This synergistic approach allows for the development of robust and innovative electronic systems.

There are a few widely accepted memristor compact models, including Strachan's TaOx model⁹, Stanford ReRAM model¹⁰, RWTH Aachen model¹¹, TEAM model¹², and VTEAM model¹³. These reported compact

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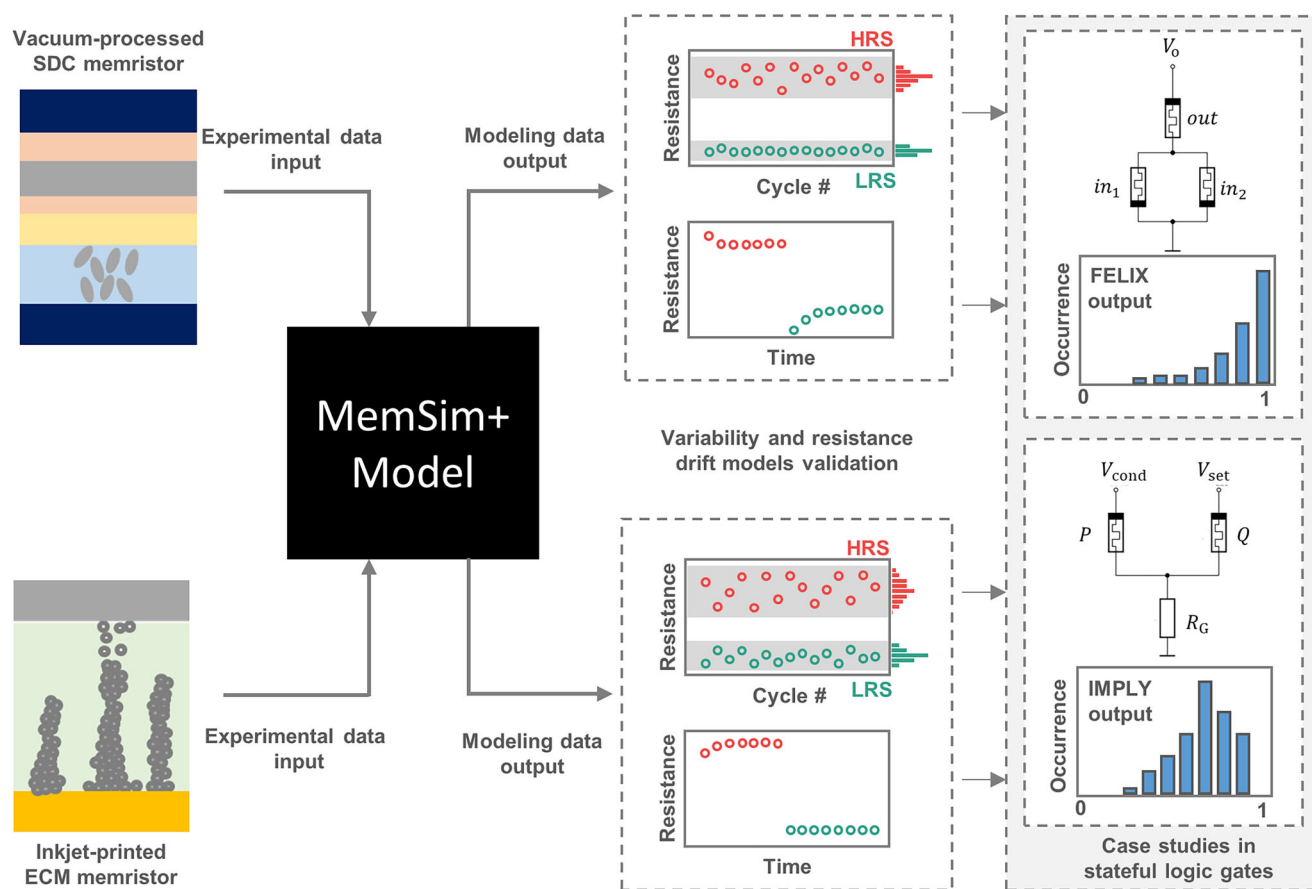


Fig. 1 | Schematics of workflow. Two completely different types of memristors, i.e., vacuum-processed SDC and inkjet-printed ECM memristors, are characterized through electrical measurements. The experimental data serves as input to extract device characteristics parameters, which are used to complete the technology-specific MemSim+ model. The comprehensive technology-specific model can simulate device non-idealities, including D2D and C2C variations, as well as the

resistance drift effect. The technology-specific MemSim+ model is validated by comparing the simulated device behavior with the experimental data of the respective memristor. The validated MemSim+ models are used to simulate stateful logic. The circuit's performance based on different technologies can be directly compared through output distribution, considering device behavioral non-idealities.

models have their own strengths and can describe the resistive switching behavior of memristive devices. Nonetheless, these models only consider one physical state variable while overlooking non-idealities of memristive technology, such as device-to-device (D2D) variations, cycle-to-cycle (C2C) variations, and resistance drift^{14–16}. We note that in the literature, we can find models that model drift; however, the implication of the term used in those papers is different than ours. For instance, in¹⁷, state drift is induced by the application of read voltage pulses, while in¹⁸, resistive drift is stimulated through the combined application of voltage and temperature. In contrast, we define drift as a change in resistance in the absence of any stimulus. These factors are highly important for designing any memristive circuit and system, including those based on stateful logic. Although some works^{19–24} extended existing models to reflect non-idealities, variability was mainly incorporated in a single model. None of these works considers the full aspects of real-world non-idealities. In addition, almost all of these variability-aware models were experimentally validated through one type of memristive device and may not be necessarily generalizable.

In this work, we present MemSim+, a realistic behavioral model fitted to measurement data that considers and simulates D2D and C2C variations of resistance, threshold voltage, resistance drift, and speed of state change. The developed behavioral model is validated through experimental data collected from two memristor types: vacuum-processed self-directed channel (SDC) memristors and inkjet-printed electrochemical metallization (ECM) memristors. The simulated device performance closely replicates the non-idealities observed in experimentally measured data of both memristor technologies, achieving a minimum Cohen's d of 0.0059 for low resistance

state (LRS) in SDC memristors and a Cohen's d of 0 for SET voltage in ECM memristors. MemSim+ was applied to simulate two stateful logic gates (IMPLY and FELIX OR) as case studies, assuming implementation using SDC and ECM memristors. The key metrics of the logic gates' operation were assessed considering device non-idealities. The assessment results further guided the subsequent optimization of the circuit design through adjustments to critical design parameters, significantly improving the output correctness probabilities. These results showcase the significance of circuit-technology co-design and their co-dependence, as well as the importance of considering non-idealities in the behavior of real devices when developing a behavioral model of memristors.

Results and discussion

Concept description

A key advantage of behavioral models is their independence from the underlying technology. This renders them universal and broadens their usage potential. Two types of memristors are studied to verify the universality of MemSim+. Their structures and underlying mechanisms are illustrated with the cross-sectional schematics in Fig. 1. The upper device, known as an SDC memristor, is fabricated using magnetron sputtering. The resistive switching of this type of device relies on the reversible concentration change of Ag that agglomerates along an SDC in the active layer²⁵. The device at the bottom is categorized as ECM memristor, in which the resistive switching is attributed to the formation and rupture of conductive filaments in the active layer²⁶. A detailed description of the resistive switching mechanisms in these two types of memristors is provided in Supplementary

Note S1 and Supplementary Fig. S1. The ECM memristor is fabricated with inkjet printing, which is a solution-based additive manufacturing method. The details of fabricating the ECM memristor are described in the Methods section.

The two types of memristors are electrically characterized separately, following the protocol described in the Methods section. The purpose is to extract key characteristic parameters from the experimental data, which can affect the operation of memristive circuits. These key characteristics are incorporated into the developed MemSim+ model to complete the construction of a comprehensive statistical model encompassing D2D and C2C variations for both technologies. The MemSim+ model, using statistically collected parameters across all devices, is then employed to simulate their respective electrical behavior and to model important figures of merit such as threshold voltage, resistance distribution, resistance drift, and speed of resistive switching. The simulated data is then compared with the experimental data to verify the model. The comprehensive MemSim+ models of two types of memristors are used for circuit simulation as case studies. The development of the MemSim+ model and its application in circuit simulation are discussed in detail in the following sections.

MemSim+ model descriptions

The MemSim+ model is developed based on a linear equation, which describes the current-voltage (I – V) characteristics of a memristor at a particular state:

$$v(t) = \left[R_{\text{on}} + \frac{R_{\text{off}} - R_{\text{on}}}{w_{\text{max}} - w_{\text{min}}} (w_{\text{max}} - w(t)) \right] \cdot i(t), \quad (1)$$

where the state variable of a memristor, voltage, and current at a particular instant of time are represented by $w(t)$, $v(t)$, and $i(t)$, respectively. w_{max} and w_{min} are two bounds of $w(t)$ at which the device's resistance at LRS (R_{on}) and at High Resistance State (HRS) (R_{off}) are determined. This description method is widely used in behavioral models of memristors^{12,13,27–29}.

The state-switching dynamics of MemSim+ are described by the derivative of the state variable:

$$\frac{dw(t)}{dt} = \begin{cases} k_{\text{off}} \cdot \left(\frac{v(t)}{v_{\text{off}}} - 1 \right)^{\alpha_{\text{off}}} & , 0 < v_{\text{off}} < v(t) \\ \Theta(t) & , v_{\text{on}} < v(t) < v_{\text{off}} \\ k_{\text{on}} \cdot \left(\frac{v(t)}{v_{\text{on}}} - 1 \right)^{\alpha_{\text{on}}} & , v(t) < v_{\text{on}} < 0, \end{cases} \quad (2)$$

where SET and RESET differ in three parameter pairs, including coefficients of state change rate (k_{off} and k_{on}), threshold voltage (v_{off} and v_{on}), and degree of (non-)linearity (α_{off} and α_{on}). Instead of a precise window function, MemSim+ leverages the inherent properties of a diode, specifically its ability to allow current to flow only in one direction after crossing the threshold voltage (with the ideal diode threshold voltage being 0 V), to model a similar behavior at reduced complexity. This property enables the voltage to be limited to a specific range^{12,30}. A complex window function, which is derived from the physics-based model³¹, will largely increase the complexity of behavioral models^{12,13}. This will sacrifice the speed of a behavioral model. A term that represents a decaying integral of resistance change ($\Theta(t)$) simulates the drift of the memristor in the absence of stimulus or under conditions where the stimulus is unable to trigger resistive switching. $\Theta(t)$ is defined as the integral of the drift depending on the state of the memristor, which is calculated using

$$\frac{d\Theta(t)}{dt} = -\frac{\Theta(t)}{\tau} + \begin{cases} \theta_{\text{off}} \cdot k_{\text{off}} \cdot \left(\frac{v(t)}{v_{\text{off}}} - 1 \right)^{\alpha_{\text{off}}} & , 0 < v_{\text{off}} < v(t) \\ 0 & , v_{\text{on}} < v(t) < v_{\text{off}} \\ \theta_{\text{on}} \cdot k_{\text{on}} \cdot \left(\frac{v(t)}{v_{\text{on}}} - 1 \right)^{\alpha_{\text{on}}} & , v(t) < v_{\text{on}} < 0, \end{cases} \quad (3)$$

where τ is the fade-out time constant, θ_{off} and θ_{on} represent the influence of state change on the initial drift rate during SET and RESET processes, respectively. The ascending resistance drift in the LRS is modeled by correspondingly decreasing the value of the state variable $w(t)$ from w_{max} as defined by Equation (2) and Equation (3). Similarly, the descending resistance drift in the HRS is captured by those same equations. These resistance drifts affect both state variables as well as the resistance of memristors. However, Equation (2) falls short in capturing the descending resistance drift in LRS, which requires an increase in the state variable $w(t)$ from w_{max} and similarly the ascending resistance drift in HRS due to the constraints of the state variable $w(t)$, which is restricted to the range $[w_{\text{min}}, w_{\text{max}}]$. Consequently, instead of affecting the state $w(t)$, these drifts only impact the resistance. According to the definition of $\Theta(t)$, the resistance drift can be integrated over time:

$$D(t) = \int_0^t \Theta(t) + c, \quad (4)$$

where $D(t)$ represents the drift over time. By incorporating $D(t)$ in Equation (1), the I – V characteristics of a memristor considering resistance drift effect can be expressed as:

$$v(t) = \left[R_{\text{on}} \left(1 - \frac{D(t)}{w_{\text{max}}} \right) + \frac{R_{\text{off}} - R_{\text{on}}}{w_{\text{max}} - w_{\text{min}}} (w_{\text{max}} - w(t)) \left(1 - \frac{D(t)}{w_{\text{max}}} \right) \right] \cdot i(t). \quad (5)$$

The above equations, describing the MemSim+ model, are implemented using sub-circuits in LTspice. A detailed description of this implementation is provided in Supplementary Note S10.

Variation model

Unlike nominal models largely and typically used, MemSim+ is a behavioral model based on equations that -with appropriate coefficients- emulate the memristors' behavior. An important aspect is that fixed coefficients can describe a single behavior, which omits the variability in the memristors' behavior. Therefore, in the fitting process, distributions for coefficient values are considered and extracted to reproduce these variations. In this variation model, C2C variations refer to changes in a memristor's properties, such as threshold voltages, rates of state change, and programmed resistance between each switching cycle. D2D variations encompass the aforementioned dissimilarity in device properties across different memristors (of the same technology). To assess C2C variation in device parameters, the stimulus described in the Method was repeatedly applied, 100 times to SDC memristors and 50 times ECM memristors, respectively. To capture D2D variations, 26 SDC memristors and 8 ECM memristors were characterized.

To model C2C and D2D variations, the Simulation Program With Integrated Circuit Emphasis (SPICE) function `.gauss()` and `if-else` command formatted as `if(cond., arg1, arg2)` are utilized to dynamically set model parameters rather than using nominal values. In this structure, if the condition is true, `arg1` is selected; otherwise, `arg2` is executed. The `.gauss` function generates random values based on a normal distribution (G), given a specified mean and standard deviation. In addition, to more accurately represent the real characteristics of fabricated memristors, a modified Gaussian distribution, which we call clipped Gaussian distribution (cG) is introduced. The clipped Gaussian distribution randomly selects values according to the specified mean and standard deviation, and it excludes values outside the clipping point (i.e., does not produce any value in the clipped region). This function is used as a suitable (SPICE-compatible) function to model (strongly) lobe-sided distributions. More detailed information on clipped Gaussian can be found in Supplementary Note S3 and Fig. S3. To replicate this behavior, we use a conditional statement to select a random value from the valid Gaussian distribution up to three times. If none of these values fall within the acceptable range, the

Table 1 | Parameters used in MemSim+ model and their corresponding nominal values of SDC and ECM memristors

Parameters	Explanation	Nominal values	
		SDC	ECM
R_{off}	Resistance at HRS.	180 k Ω	1933.15 Ω
R_{on}	Resistance at LRS.	13.9079 k Ω	174 Ω
V_{off}	SET threshold voltage.	0.34 V	1.56 V
V_{on}	RESET threshold voltage.	−0.2145 V	−0.39 V
k_{off}	Coefficient of state change rate during SET.	12.4 mm s ^{−1}	121.7 mm s ^{−1}
k_{on}	Coefficient of state change rate during RESET.	−2.3 mm s ^{−1}	−7.6 mm s ^{−1}
θ_{off}	Coefficient of resistance drift after SET	705.433 ms ^{−1}	0
θ_{on}	Coefficient of resistance drift after RESET	1013.65 ms ^{−1}	410.25 ms ^{−1}
τ	Drift fade-out time constant	5 s	50 s
a_{off}	Degree of (non-)linearity for SET.	2	2
a_{on}	Degree of (non-)linearity for RESET.	2	2
w_{max}	Value of state variable at LRS.	3 nm	3 nm
w_{min}	Value of state variable at HRS.	0 nm	0 nm

function defaults to the mean value with a probability of $(1 - \frac{R_{\text{VG}}}{R_{\text{total}}})^3$, where R_{VG} represents the resistance values selected from the valid Gaussian distribution, and R_{total} represents the resistance values selected from the Gaussian distribution. The SPICE command for a clipped Gaussian (in this example, for the value of R_{off}) is given by:

$$\text{.param } R_{\text{off}} = \text{if}(R_{\text{off}1} \leq 40 \text{ k}\Omega, \text{if}(R_{\text{off}2} \leq 40 \text{ k}\Omega, \text{if}(R_{\text{off}3} \leq 40 \text{ k}\Omega, R_{\text{off}\mu}, R_{\text{off}3}), R_{\text{off}2}), R_{\text{off}1})$$

which translates to

$$R_{\text{off}} = \begin{cases} R_{\text{off}1}, & \text{if } R_{\text{off}1} > 40 \text{ k}\Omega, \\ R_{\text{off}2}, & \text{if } R_{\text{off}1} \leq 40 \text{ k}\Omega \text{ and } R_{\text{off}2} > 40 \text{ k}\Omega, \\ R_{\text{off}3}, & \text{if } R_{\text{off}1} \leq 40 \text{ k}\Omega \text{ and } R_{\text{off}2} \leq 40 \text{ k}\Omega \text{ and } R_{\text{off}3} > 40 \text{ k}\Omega, \\ R_{\text{off}\mu}, & \text{otherwise.} \end{cases} \quad (6)$$

where $R_{\text{off}1}$, $R_{\text{off}2}$, and $R_{\text{off}3}$ are the three randomly selected values from the Gaussian distribution, $R_{\text{off}\mu}$ is the Gaussian mean value, 40 k Ω is the clipping point, and R_{off} is the result of a randomly selected clipped Gaussian value. Our approach enables the simulation of both C2C and D2D variations of memristors, encompassing variations in HRS and LRS resistance, threshold voltage, resistance drift, and resistance change dynamics.

Fitting

In this section, the respective model-fitting process for SDC memristors and ECM memristors is introduced in four parts: resistance in HRS and LRS, threshold voltages, observed resistance drift, and resistance change rate. The parameter values for the nominal model (corresponding to nominal values) for both SDC and ECM memristor technologies are presented in Table 1. Table 2 provides the distributions of individual parameters, including Gaussian (G), clipped Gaussian (cG), and clipped Gaussian (cG^*) with conditions, respectively denoted as G_N^M , cG_N^M , and cG_N^{*M} , where M represents the type of memristor (either SDC or ECM) and N indicates the modeled variable (e.g., R_{off} or V_{on}). The values of G_N^M , cG_N^M , and cG_N^{*M} are determined during the fitting process, such that they represent the realistic behavior of

actual memristors for both technologies. A flowchart is provided in Supplementary Fig. S18 under Supplementary Note S10 for an intuitive demonstration of the model-fitting and validating process.

LRS and HRS. The variations in LRS and HRS are key properties in a memristor behavior and are of substantial interest to designers of memristive circuits. The experimental data of SDC memristors show that the LRS (R_{on}) exhibits a Gaussian distribution $G_{R_{\text{on}}}^{\text{SDC}}$, whereas the distribution of the HRS (R_{off}) is very lobe-sided and better fits into a clipped Gaussian $cG_{R_{\text{off}}}^{\text{SDC}}$. The behavior of ECM memristors is more complex. The LRS (R_{on}) varies significantly and doesn't fit into one Gaussian. Hence, the experimental results are captured using three Gaussian distributions: $G_{R_{\text{on}1}}^{\text{ECM}}$, $G_{R_{\text{on}2}}^{\text{ECM}}$, and $G_{R_{\text{on}3}}^{\text{ECM}}$. To fit into the model, a random value is selected from $G_{R_{\text{on}1}}^{\text{ECM}}$, if it falls within the range of [116.32, 230] Ω ; if it exceeds 230 Ω , a value is selected from $G_{R_{\text{on}3}}^{\text{ECM}}$, ensuring it lies within [100, 500] Ω . In all other cases, $G_{R_{\text{on}2}}^{\text{ECM}}$ is used. The data of HRS (R_{off}) follows a clipped Gaussian distribution, characterized by $cG_{R_{\text{off}}}^{\text{ECM}}$. A detailed discussion on why and how we have used multiple Gaussians for modeling the memristance of ECM better is provided in Supplementary Note S3. The extracted distributions are fitted to the proposed SPICE MemSim+ model.

The stimuli with the same parameter values as those used during the experiments are applied to the modeled memristors to test the suitability of fitted functions. For SDC memristors 2600 simulation runs (corresponding to 26 devices, with each device undergoing 100 cycles) and 400 simulation runs for ECM memristors (corresponding to 8 devices, with each device undergoing 50 cycles), were executed for this evaluation. The obtained experimental and modeled memristances for SDC memristors and ECM memristors are in good agreement, as illustrated in Fig. 2a, b, respectively. A more intuitive comparison is provided in Supplementary Fig. S8, where normal distribution curves of the experimental and modeled data are superimposed. Cohen's d^{32} is calculated (Supplementary Note S4) to assess the standardized difference between the mean of experimental and modeled data with respect to the memristance of two types of memristors. The calculated d further indicates a close agreement between the modeled and experimental data, with effect size³³ ranging from very small (d for R_{on} in SDC = 0.0059) to small (d for R_{off} in SDC = 0.4204; d for R_{on} and R_{off} in ECM = 0.2469 and 0.3157, respectively). The reasoning behind selecting Gaussian and clipped Gaussian approaches is elaborated in detail in Supplementary Notes S3.3 and S3.4 for SDC and ECM technologies, respectively.

Threshold voltages. The threshold voltages of the memristors were extracted from the hysteresis curves recorded during repeated resistive switching cycles. For SDC memristors (measurement) and modeled memristors of both SDC and ECM technologies (using LTspice simulations with the MemSim+ model fitted to both technologies), the threshold voltages are calculated by the maximum derivative of current with respect to the voltage from I – V curves, which is illustrated in Supplementary Figs. S9 and S10. In the case of ECM memristors, the SET threshold voltage is defined as the voltage at which the maximum value of the derivative of voltage with respect to current occurs, while the RESET threshold voltage is identified at the point where current drops during the voltage sweeping, i.e., the voltage where the maximum current is observed. The variability of the experimental threshold voltages measured from SDC memristors and ECM memristors can not be captured with a single Gaussian distribution or clipped Gaussian distribution. For SDC memristors, the SET threshold voltage V_{off} is modeled using Gaussian distribution $G_{V_{\text{off}}}^{\text{SDC}}$, if it falls within the range of [150, 600] mV; otherwise, it is modeled using $G_{V_{\text{off}}}^{\text{SDC}}$. Similarly, RESET threshold voltage (V_{on}) is selected from $G_{V_{\text{on}}}^{\text{SDC}}$ if it is within [−550, 0] mV, or from $G_{V_{\text{on}}}^{\text{SDC}}$ otherwise. For ECM memristors, SET threshold voltage is fitted with $G_{V_{\text{off}}}^{\text{ECM}}$, if the voltage is below 2.30 V. When SET voltage exceeds this

Table 2 | Values of MemSim+ model parameters of two memristor technologies

Technology	SDC technology				ECM technology			
Parameters	μ	σ	CP or Range	Type	μ	σ	CP or Range	Type
R_{off}	118.40 k Ω	99.70 k Ω	> 40 k Ω	$cG_{R_{off}}^{SDC}$	1933.15 Ω	648.62 Ω	>1300 Ω	$cG_{R_{off}}^{ECM}$
R_{on1}	13.87 k Ω	2.61 k Ω		$G_{R_{on1}}^{SDC}$	248.25 Ω	167.92 Ω	[116.32, 230.00] Ω	$G_{R_{on1}}^{ECM}$
R_{on2}					170.57 Ω	26.28 Ω		$G_{R_{on2}}^{ECM}$
R_{on3}					413.56 Ω	216.15 Ω	[100, 500] Ω	$G_{R_{on3}}^{ECM}$
V_{off1}	375.94 mV	115.84 mV	[0.15 0.60] V	$G_{V_{off1}}^{SDC}$	1.47 V	0.51 V	<2.30 V	$cG_{V_{off}}^{*ECM}$
V_{off2}	289.22 mV	37.32 mV		$G_{V_{off2}}^{SDC}$				
V_{on1}	− 240.58 mV	112.97 mV	[−0.55, 0.00] V	$G_{V_{on1}}^{SDC}$	−569.56 mV	421.15 mV	[−1, −0.19] V	$G_{V_{on1}}^{ECM}$
V_{on2}	− 217.82 mV	38.11 mV		$G_{V_{on2}}^{SDC}$	−400.89 mV	163.12 mV	<−0.19 V	$cG_{V_{on2}}^{*ECM}$
k_{off}	12.40 mm s ^{−1}	0.28 mm s ^{−1}		$G_{k_{off}}^{SDC}$	406.48 mm s ^{−1}	259.35 mm s ^{−1}	>40.80 mm s ^{−1}	$cG_{k_{off}}^{*ECM}$
k_{on}	− 2.30 mm s ^{−1}	2.00 μ m s ^{−1}		$G_{k_{on}}^{SDC}$	− 62.37 mm s ^{−1}	56.343 mm s ^{−1}	<−12.00 mm s ^{−1}	$cG_{k_{on}}^{*ECM}$
θ_{off}	705.43 ns ^{−1}	433.28 ns ^{−1}	> 81.50 ns ^{−1}	$cG_{\theta_{off}}^{*SDC}$	0	0		
θ_{on}	1013.65 ns ^{−1}	622.59 ns ^{−1}	> 107.23 ns ^{−1}	$cG_{\theta_{on}}^{*SDC}$	410.25 ns ^{−1}	0		

μ , σ mean values and standard deviation of Gaussian distributions, CP clipping point of clipped Gaussian distributions.

threshold, it is represented by mean values due to observed higher probability in this range. RESET threshold voltage is dynamically selected from $G_{V_{on1}}^{ECM}$, if between −1000 mV and −190 mV, or from $cG_{V_{on2}}^{ECM}$. The MemSim+ model can closely simulate the distribution of threshold voltage that is experimentally measured from SDC and ECM memristors, as depicted in Fig. 2c, d, respectively. The results presented in Fig. 2c, d are also plotted as superimposed normal distribution curves in Supplementary Fig. S11 for statistical analysis. The good agreement between modeled and experimental measured threshold voltage distribution is indicated by Cohen's d values: for SDC memristors, $d = 0.4975$ and 0.3805 corresponding to V_{on} and V_{off} , respectively, while for ECM devices, $d = 0.2108$ and 0 for V_{on} and V_{off} , respectively.

Resistance drift. Resistance drift is a common phenomenon in memristors, referring to a deviation in resistance from the designed value in the absence of external electrical stimuli^{34–36}. This non-ideality affects the performance of the practical memristive circuits and, therefore, needs to be considered when designing memristive circuits^{37–39}. The simulation of resistance drift in the MemSim+ model is performed by representing the average resistance drift in both LRS and HRS states across multiple devices. The drift model describes an exponential behavior, where at $t = 5\tau$ the value deviates by less than 0.1% from its value at $t \rightarrow \infty$. τ is set to one-fifth of the observed duration (t) of resistance change due to drift. The experimental data of SDC memristors indicate that the average ascending resistance drift is ~6 k Ω in LRS, and the average descending resistance drift is around 8 k Ω in HRS from the programmed values. These drifts diminish within ~25 s for both states, leading to τ being set at 5 s. The extraction of the coefficient of resistance drift after SET and RESET (θ_{off} and θ_{on}) for modeling the resistance drift follows a process similar to that of simulating state change dynamics, where the threshold voltage and the coefficient of the state change rate corresponding to the nominal value model are considered. The ascending resistance drift in LRS and the descending resistance drift in HRS are modeled using clipped Gaussian distributions $cG_{\theta_{off}}^{*SDC}$ and $cG_{\theta_{on}}^{*SDC}$ respectively. The coefficients of resistance drift influence both the state as well as resistances of the memristors for these drifts. For ECM memristors, the average ascending resistance drift is 131.32 Ω in HRS. The changes in resistance over 100 seconds were modeled exponentially by setting τ to 33.34 s. The details of this fitting and calculation are described in Supplementary Note S7. No drifts occur in the LRS state of ECM

memristors, hence θ_{off} is set to zero for these memristors. To extract θ_{on} of ECM memristors, similar to the approach used for SDC memristors, k_{on} , v_{on} , and other parameters were chosen from the nominal value model, with only resistance variations considered. The fitted value of θ_{on} does not exhibit any distribution and is properly represented by a nominal value of 203.04 ns^{−1}. The θ_{on} only alters the resistance without affecting the state of the memristors, as the minimum value of $w(t)$ is w_{min} , which cannot be further reduced. The modeled resistance drifts closely replicate the experimentally observed resistance drift phenomenon, as illustrated in Fig. 2e and in Fig. 2f for SDC and ECM memristors, respectively.

State change dynamics. The rates of resistance change during the SET and RESET processes are highly complex, driven by several interdependent factors that we aim to observe and replicate as closely as possible. These intricate processes are modeled using parameters such as k_{off} , k_{on} , α_{off} , α_{on} , v_{off} , v_{on} , and the applied voltage. The path traversed during resistance changes is governed by α_{off} and α_{on} , which are fixed at 2 to reduce mathematical complexity at the cost of accuracy. Meanwhile, k_{off} and k_{on} scale the state change linearly, whereas variations in the threshold voltages v_{off} and v_{on} significantly influence the time required to change the resistance. The changes in resistance, including the initial and final resistance values, as well as the required time obtained from experimental data during the SET and RESET pulses for both technologies, are noted. The variability in k_{on} and k_{off} arises from differences in transition times between states that are extracted from the SET and RESET experiments, as well as from fluctuations in the threshold voltages. Once the threshold voltage is crossed, the resistance state of the device transitions completely from one state to another when the applied voltage is increased by 100 mV for SDC memristors and by 300 mV for ECM memristors. The SDC experimental data reveal a Gaussian distribution $G_{k_{off}}^{SDC}$ and $G_{k_{on}}^{SDC}$ for both k_{off} and k_{on} , respectively. For the ECM technology, although k_{off} and k_{on} do not perfectly follow a Gaussian or clipped Gaussian distribution, they can still be approximated using these distributions under certain conditions. Specifically, k_{off} is modeled using a Gaussian distribution, $G_{k_{off}}^{ECM}$, for values greater than 40.80 mm s^{−1}; if the sampled value is below this, the mean values are used instead due to the higher occurrence of mean values compared to the Gaussian distribution. Similarly, the k_{on} parameter is

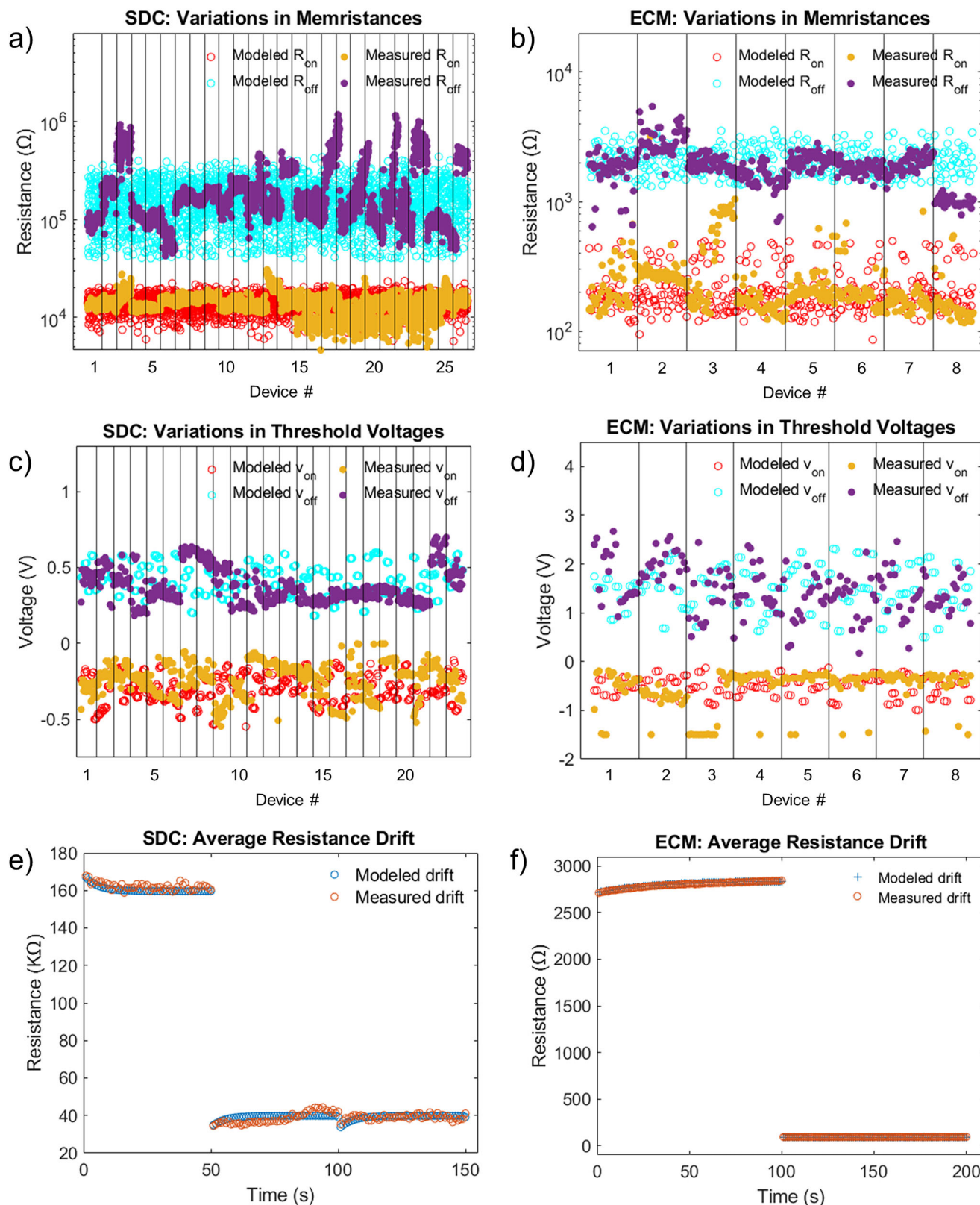


Fig. 2 | Data comparison between experiments and MemSim+ model of two memristor technologies. **a** Combined SET/RESET cycles for 26 SDC devices, each undergoing 100 cycles. **b** Combined SET/RESET cycles for 8 ECM devices, each undergoing 50 cycles. **c** Combined threshold voltages of 23 SDC devices, selected 20

measurements per device at the end of the forming. **d** Combined threshold voltages of 8 SDC devices, 20 measurements per device at the end of the hysteresis curve. **e** Average resistance drifts in LRS and HRS of 26 SDC devices. **f** Average resistance drifts in HRS of 8 ECM devices.

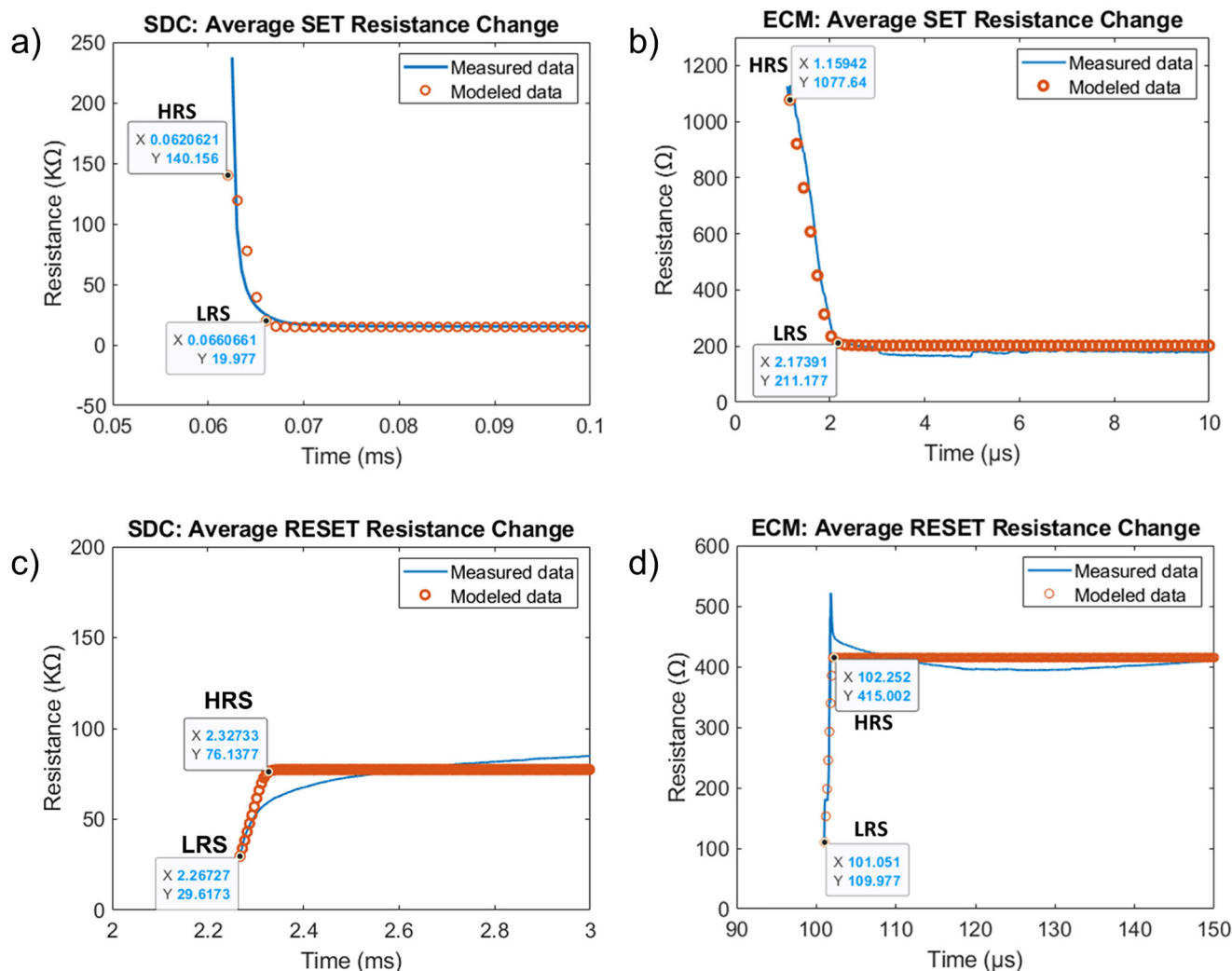


Fig. 3 | Comparison of state change dynamics between experimental data and MemSim+ model for two memristor technologies. State change dynamics are derived from the speed of state transitions between HRS and LRS during SET and RESET operations. HRS and LRS are overall mean values calculated from 26 SDC

and 8 ECM memristors, respectively. Each SDC memristor was cycled 100 times while each ECM memristor was cycled 50 times. **a, b** SET of SDC and ECM memristor, respectively. **c, d** RESET of SDC and ECM memristor, respectively.

approximated using a clipped Gaussian distribution $cG_{k_{on}}^{*ECM}$. The k_{on} is initially sampled from the distribution $G_{k_{on}}^{ECM}$ such that if the sampled value does not fall within the acceptable range defined by the distribution after three sampling attempts, a fixed value of -745 mm s^{-1} is selected instead of the mean value. Fig. 3a, b demonstrate a good degree of agreement during the SET pulse for SDC and ECM technology. However, during RESET pulse, we see that it follows the overall trend as opposed to instantaneous values. This is because the HRS state varies continuously, and we modeled the HRS state with a fixed resistance value using piecewise linear segments.

Case study

Several memristive logics have been reported⁴⁰, among which many are stateful logics^{41–43}, including prominent ones such as Material Implication (IMPLY)⁴⁴, and Fast and energy-efficient Logic in Memory (FELIX)⁴⁵. In stateful logic, the input and output logic values are represented by the state of a device (e.g., the resistance of a memristor), and logic gates function based on the application of certain, predefined voltages to achieve the desired output. The case study in this work focuses on IMPLY logic and (2-bit) FELIX OR gate to underline the significance of considering variations in the design of memristive logic circuits.

The circuit diagram, as well as the truth table of IMPLY logic and FELIX OR gates, are illustrated in Fig. 4. The design constraints for IMPLY logic is $V_{set} > v_{off}$, $V_{set} > V_{cond}$, and $R_{on} < R_G < R_{off}$ where V_{set} , V_{cond} are the required voltages to perform the IMPLY operation, and R_G is a load resistor.

For 2-bit FELIX OR logic, the design constraints are defined as:

$$v_{offmax} \left(\frac{R_{on} \parallel R_{off1} + R_{off}}{R_{off}} \right) < V_0 < v_{offmin} \left(\frac{R_{off2} \parallel R_{off1} + R_{off}}{R_{off}} \right) \quad (7)$$

where v_{offmax} and v_{offmin} are the maximum and minimum set threshold voltages of the memristor, and V_0 is the operating voltage required to implement the OR function. Additional design constraints are given in⁴⁵ and⁴⁶, and are detailed in Supplementary Notes S8 and S9 for IMPLY logic and FELIX OR, respectively.

Setup

To validate the advantages of the MemSim+ model, simulations of logic gates based on SDC and ECM memristors were conducted using the LTspice simulator⁴⁷. These simulations use nominal parameter values, as outlined in Table 1, and parameter values with variations, as detailed in Table 2. In the case study, the logic gates are simulated under three scenarios

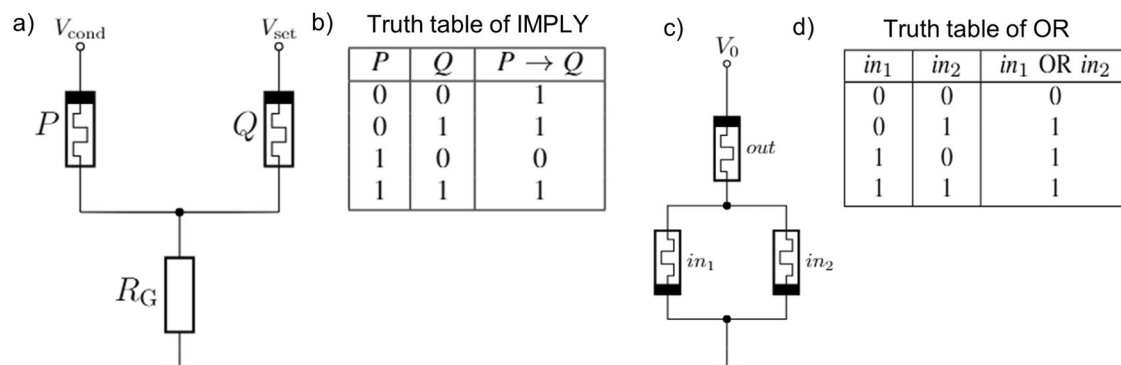


Fig. 4 | Circuit diagram and truth table. a, b Circuit diagram and truth table of logic gate IMPLY. **c, d** Circuit diagram and truth table of FELIX OR gate.

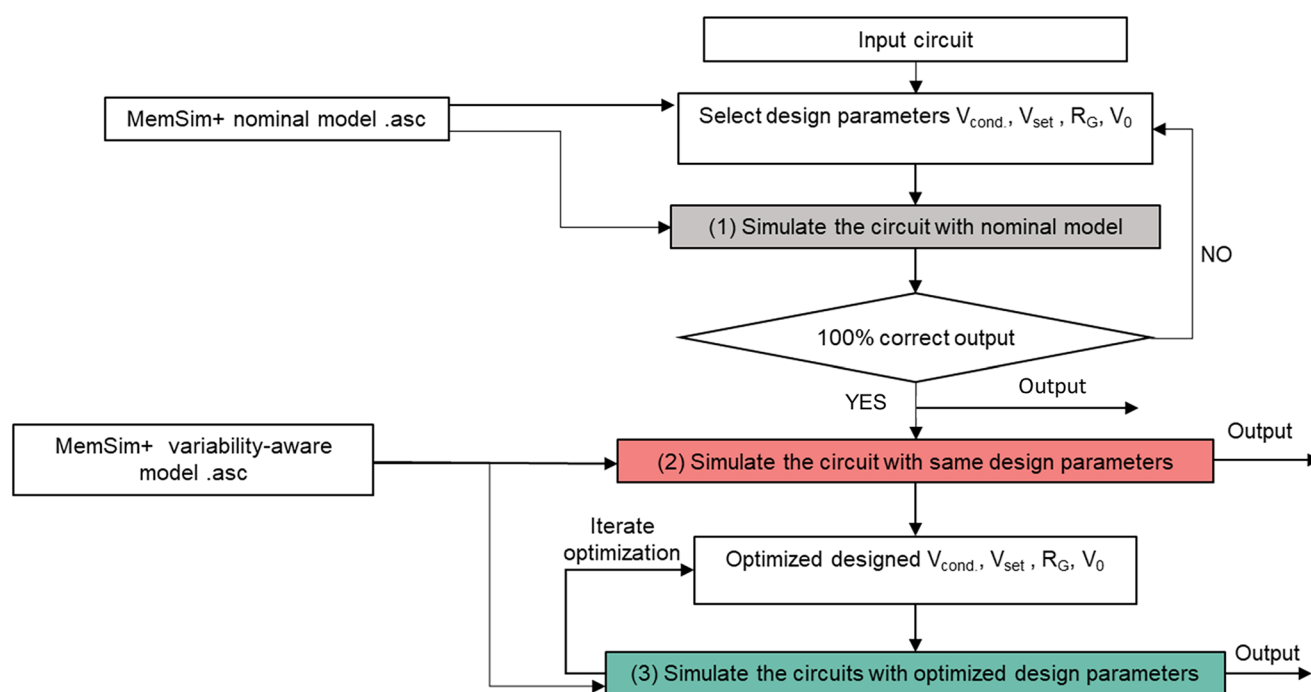


Fig. 5 | Flowchart of the simulation setup. Each circuit was simulated and optimized through three sequential scenarios: nominal (1), realistic (2), and optimized (3). In the first scenario (gray box), the MemSim+ nominal model was used along with the selected design parameters to ensure the overall output was 100% correct. Next, the circuit was simulated again with the same design parameters while using

the MemSim+ variability-aware model in the second scenario (red box). When considering the device variability, the simulated output in the second scenario dropped significantly from 100%. Therefore, the third scenario (green box) was engaged to maximize the overall output correctness by iteratively optimizing the design parameters.

for both memristor technologies. The flowchart for the simulations is provided in Fig. 5.

As shown in Fig. 5, the three scenarios are: 1) Nominal (gray box): The logic gates were designed using a nominal model, similar to other works^{44,45}. This approach reflects the traditional practice in circuit design, where circuits are simulated using models with nominal parameter values. 2) Realistic (red box): To assess the impact of parameter variations in circuit design, the probabilities of correct output calculation were determined by simulating the memristive logic gates using a variation model under the same setup conditions as in the first scenario (i.e., designed using nominal values). 3) Optimized (green box): By analyzing and taking into account the variation patterns of key parameters (R_{off} , R_{on} , V_{off} , V_{on}) that influence gate functionalities, the adjustable parameters, including operating voltages (V_{cond} and V_{set} of IMPLY; V_0 of FELIX) and the resistance value of the load resistor (R_G of IMPLY), were systematically altered to improve the probability of output correctness.

The range of these key parameters is shown separately in Supplementary Table S1. The resulting correct output probabilities were observed

and recorded, highlighting the critical effect variations have on logic gate performance. There are several degrees of freedom concerning the investigated logic, for instance, execution time (pulse duration) or the selection of certain voltages from an allowed interval, which result in different trade-offs for performance (e.g., speed) or different aspects of robustness. However, it is out of the scope of this work to find an optimal gate design. We rather concentrate on showing this effect, which is possible to study thanks to the MemSim+ model.

For simplicity, logical value mapping threshold of 0.5 is used as example, where $0 \leq s < 0.5 \hat{=}$ '0' and $0.5 \leq s \leq 1 \hat{=}$ '1', where s denotes the state of the memristor. Additionally, the results for various logic mapping schemes, considering different noise margins (the undefined region between the low logic and high logic), are provided in Supplementary Tables S2–S5. Overall correctness of logical operation was calculated as the overall probability of correctly processed outputs, i.e. $P_{\text{correct}} = \frac{1}{4}P_{00} + \frac{1}{4}P_{01} + \frac{1}{4}P_{10} + \frac{1}{4}P_{11}$, where P_{correct} is the overall correctness, and P_{ij} are the probabilities of the individual input combinations (for input i and j) to yield correct outputs. It is worth noting that although individual cases might

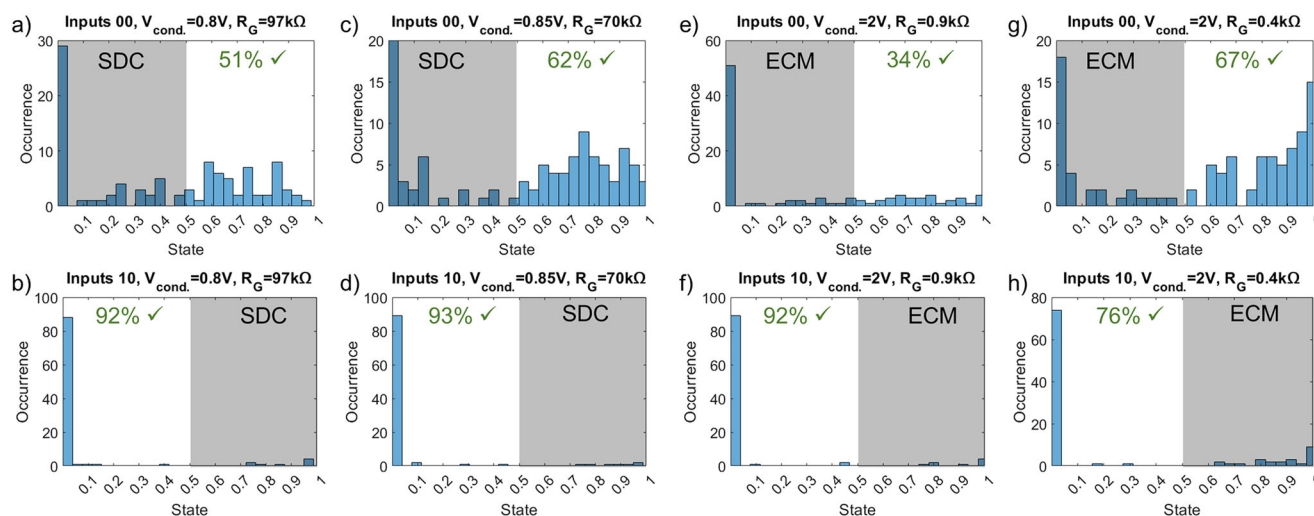


Fig. 6 | Simulated output histogram of IMPLY implemented with SDC and ECM memristors. IMPLY outputs correspond to the input combinations ‘00’ and ‘10’ simulated under the realistic and optimized scenarios. SDC technology: **a** Inputs ‘00’ and **b** Inputs ‘10’ under the realistic scenario with $V_{\text{cond.}} = 0.8 \text{ V}$ and $R_G = 97 \text{ k}\Omega$.

c Inputs ‘00’ and **d** Inputs ‘10’ under the optimized scenario with $V_{\text{cond.}} = 0.85 \text{ V}$ and $R_G = 70 \text{ k}\Omega$. ECM technology: **e** Inputs ‘00’ and **f** Inputs ‘10’ under the realistic scenario with $V_{\text{cond.}} = 2 \text{ V}$ and $R_G = 0.9 \text{ k}\Omega$. **g** Inputs ‘00’ and **h** Inputs ‘10’ under the optimized scenario with $V_{\text{cond.}} = 2 \text{ V}$ and $R_G = 0.4 \text{ k}\Omega$.

experience a minor impact in relation to the logic mapping scheme, the overall correctness in all case studies shows to be negligibly impacted by the logic mapping schemes, as shown in Supplementary Figs. S12–S15.

Circuit-technology co-design and results

For the SDC memristors, the IMPLY circuit was designed by selecting the midpoint between the LRS and HRS as R_G , which is calculated as $97 \text{ k}\Omega$. All calculations under all three scenarios of IMPLY logic for SDC memristors are provided in Supplementary Note S8.1. Given the design constraints of the circuit, it has been determined that for a logic input of ‘10’, the value of $V_{\text{cond.}}$ must exceed 0.76 V , while for a logic input of ‘00’, $V_{\text{cond.}}$ should remain below 1.64 V to ensure proper circuit operation. These determinations are based on a V_{set} of 1 V . For the logic inputs ‘01’ and ‘11’, the probability of correctness of 100% was achieved without specific constraints on $V_{\text{cond.}}$. This is because if the constraints for the inputs ‘00’ are satisfied, then inputs ‘01’ and ‘11’ will automatically be satisfied as well (Supplementary Note S8.1). As a result, when $V_{\text{set}} = 1 \text{ V}$ and $V_{\text{cond.}} = 0.8 \text{ V}$, an overall correctness of 100% is realized under the nominal scenario.

The simulation results of the realistic scenario reveal that the circuit does not perform as flawlessly as it did in the nominal scenario. In the realistic scenario, the individual output correctness dropped to 51% and 92%, respectively, for the input of ‘00’ and ‘10’, as the simulated histograms in Fig. 6a, b shows. This highlights the necessity of accounting for parameter variations to enhance performance. Taking into account the variations (R_{off} , R_{on} , v_{off}) in memristors, R_G was subsequently adjusted to $32 \text{ k}\Omega$, which is the midpoint between maximum R_{on} and minimum R_{off} . A worst-case analysis (Supplementary Note S8.1) using the extreme values of R_{off} , R_{on} , and v_{off} has indicated that no solution exists for V_{set} and $V_{\text{cond.}}$ ensuring 100% output correctness in all input combinations. Still, the simulation under optimized scenario suggested that (Supplementary Table S2), an optimal overall correctness of 88.75% is achievable, when V_{set} , $V_{\text{cond.}}$, and R_G are assigned values of 1 V , 0.85 V , and $70 \text{ k}\Omega$ respectively. Specifically, individual output correctness of case ‘00’ and ‘10’ was optimized to 62% and 93%, respectively, as shown in Fig. 6c, d.

For the ECM memristors, the IMPLY circuit has been designed by selecting R_G as the midpoint between the LRS and HRS, calculated as $1 \text{ k}\Omega$ for the nominal scenario. All calculations for the three scenarios of IMPLY logic for the ECM memristors are detailed in Supplementary Note S8.2. Considering the circuit design constraints, $V_{\text{cond.}}$ should have been greater than 0.90 V for logic inputs ‘10’ and less than 1.19 V for logic

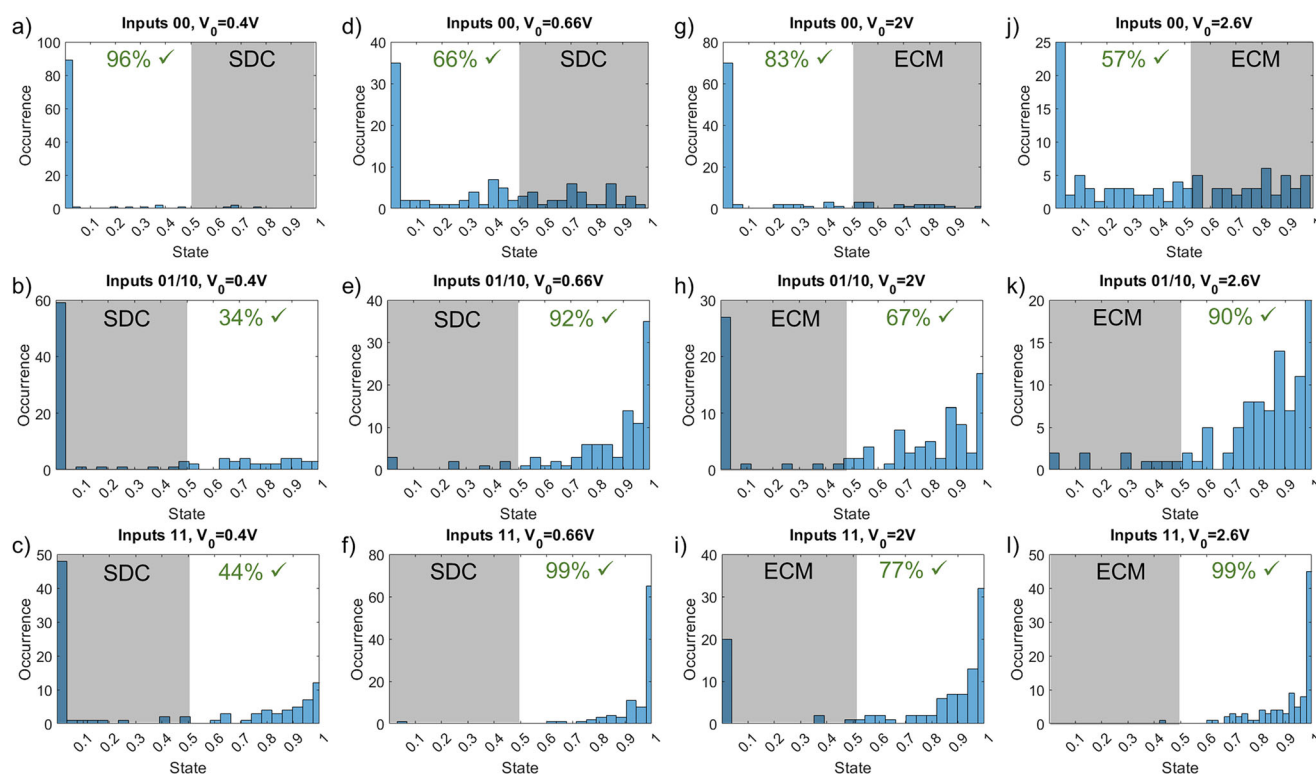
‘00’ when V_{set} is 2.5 V . Calculation and detailed discussion for this phenomenon is provided in Supplementary Note S8.2. Consequently, R_G has been adjusted to 200Ω and $V_{\text{cond.}}$ to 2 V , according to the calculations derived from the optimization for the nominal scenario in Supplementary Note S8.2, can provide a sufficient voltage margin to ensure proper circuit functionality. The simulation results indicate that in the nominal scenario, the circuit operates with a 100% success rate. When considering variability under the realistic scenario, the resistor value R_G was adjusted to a mid-range value between the maximum R_{off} and minimum R_{on} , settling at 900Ω . With this adjustment, the overall output correctness dropped to 81.50%. Previous optimization efforts in the nominal scenario have demonstrated that decreasing R_G enhances the success rate; simulation results indicate an improved success rate of 85.75% with R_G set to 400Ω . The optimization details are provided in Supplementary Note S8.2. The histograms of the output for inputs ‘00’ and ‘10’ across both technologies are presented in Fig. 6e–h, offering a visual representation of the data within the range of 0 to 1 and aiding in the selection of the logical mapping scheme.

The FELIX OR gate performs correctly with a probability of 100% at V_0 of 0.4 V for the SDC technology and 2 V for the ECM technology, as required under the nominal scenario for both technologies, and the calculations are provided in Supplementary Note S9. A circuit designer, who considers the memristor model as a black box, would expect this behavior on a real device. In an experiment, however, the memristive circuit might not work for unknown reasons. The simulation under the realistic scenario is capable of emulating the reality of memristors’ behavior and showing the probability of correct outputs for all input logic combinations, as detailed in Table 3. The two cases inputs ‘01’ and ‘10’ do not need to be distinguished since FELIX is symmetrical regarding the inputs. Due to variations in memristors’ parameters, the probability of occurrence of correct output for FELIX OR gate is 52.00% and 73.50% as presented in Table 3 for both technologies in the realistic scenario. To address this issue, V_0 is recalculated by considering the parameter variations obtained from the proposed model for both technologies. Increasing V_0 raises the probability of correctness for the logic states ‘01’, ‘10’, and ‘11’ while decreasing it for the logic state ‘00’, and vice versa when V_0 is reduced, as shown in Table 3. Supplementary Note S9 contains all the calculations for the three scenarios of FELIX logic applied to both technologies. Through variation-aware optimization, we achieved a probability of correct output of 87.25% for the SDC technology and 84.00% for the ECM technology. Figure 7 displays the output histograms corresponding to the logic inputs ‘00’, ‘01’, ‘10’, and ‘11’ for both

Table 3 | The probability of occurrence of correct output for all the inputs combinations ('00' '01' '10' and '11') at nominal voltage and optimized voltages for IMPLY logic and FELIX logic gates for both technologies, considering variations

Gates	IMPLY logic gate						FELIX OR logic gate					
	SDC technology			ECM technology			SDC technology			ECM technology		
R_G (k Ω)	97		70	0.20	0.90	0.40	—			—		
V_{cond}/V_0 (V)	0.80	0.80	0.85	2	2	2	0.40	0.40	0.66	2	2	2.6
Scenario	N.	R.	O.	N.	R.	O.	N.	R.	O.	N.	R.	O.
00	100	51	62	100	34	67	100	96	66	100	83	57
01	100	100	100	100	100	100	100	34	92	100	67	90
10	100	92	93	100	92	76	100	34	92	100	67	90
11	100	100	100	100	100	100	100	44	99	100	77	99
$P_{correct}\%$	100	85.75	88.75	100	81.50	85.75	100	52	87.25	100	73.5	84.00

Simulation under scenarios: N. nominal, R. realistic, O. optimized.

**Fig. 7 | Simulated output histogram of FELIX OR implemented with SDC and ECM memristors.** FELIX OR outputs correspond to input combinations '00' '01' '10', and '11' for both technologies under realistic and optimized scenarios. For SDC under realistic scenario ($V_0 = 0.4$ V): **a** Inputs '00'. **b** Inputs '01'/'10'. **c** Inputs '11'. ForSDC under optimized scenario ($V_0 = 0.66$ V): **d** Inputs '00'. **e** Inputs '01'/'10'. **f** Inputs '11'. For ECM under realistic ($V_0 = 2$ V): **g** Inputs '00'. **h** Inputs '01'/'10'. **i** Inputs '11'. For ECM under optimized scenario ($V_0 = 2.6$ V): **j** Inputs '00'. **k** Inputs '01'/'10'. **l** Inputs '11'.

technologies, providing qualitative information about the correct output for various logical mapping schemes.

All design parameters involved in three simulation scenarios for the IMPLY and the FELIX OR logic gates based on two memristor technologies, together with the corresponding individual and overall output correctness for all input combinations, are summarized in Table 3. An intuitive comparison of overall output correctness simulated under three scenarios is provided in Fig. 8 as bar diagrams, where optimization of IMPLY (Fig. 8a) and FELIX OR (Fig. 8b), based on two different memristor technologies, is quantitatively demonstrated. The results for selected logical mapping schemes other than 50–50% are detailed quantitatively in Supplementary Notes S8 and S9. Due to space limitations, we only studied simulations based on SDC and ECM memristors.

However, MemSim+ is capable of modeling other types of memristors and simulating circuits based on those devices.

Conclusion

The work at hand presents the MemSim+ model for ReRAMs, a realistic behavioral model that can capture non-idealities, including resistance drift, as well as C2C and D2D variations. MemSim+ is fitted to experimental data from vacuum-processed SDC memristors and ECM memristors fabricated using inkjet printing technology. The model is implemented in SPICE without additional procedural, software, or solver engines. By incorporating the statistical variation of model parameters, our model enables a more robust and reliable simulation of memristive circuits and systems. This is demonstrated by the case study that

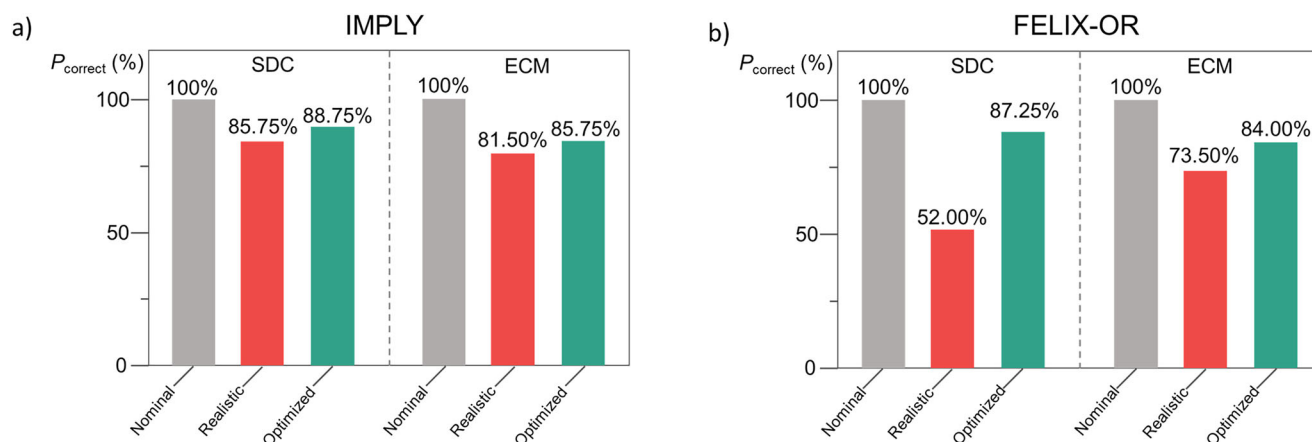


Fig. 8 | Overall correctness of simulated logical operations. The simulation results of IMPLY (a) and FELIX OR (b) based on SDC and ECM memristors are presented with overall correctness P_{correct} , which is the weighted sum of individual correctness

P_{ij} of all input combinations, with equal weights of $\frac{1}{4}$. For both technologies, each logic gate was simulated in three scenarios sequentially: nominal (gray bin), realistic (red bin), and optimized (green bin).

variation-aware circuit-technology co-design can significantly enhance the correctness probabilities of the IMPLY logic gate circuit, achieving correctness probability up to 88.75% ($\uparrow 3.00\%$) for SDC technology and 85.75% ($\uparrow 4.25\%$) for the ECM technology. Additionally, for the FELIX OR gate, the correctness probabilities increase to 85.75% ($\uparrow 35.25\%$) for SDC technology and 84.00% ($\uparrow 10.50\%$) for the ECM technology. The findings also indicate that the typical simulation approach (using nominal values) leads to lower chances of the fabricated circuits functioning as expected. The results showcase the significance of circuit-technology co-design and their co-dependence, as well as the importance of considering non-idealities in the behavior of real devices when designing memristive circuits and systems.

Methods

Characterization of SDC memristors

Commercial SDC memristors (W+SDC 16 Discrete Memristor Encapsulated Edge⁴⁸) were electrically characterized to provide experimental data. The electrical characterizations were performed on a breadboard with the core components of the setup consisting of a low-input-offset operational amplifier⁴⁹ and a multi-function instrument serving as a function generator and oscilloscope⁵⁰. To avoid introducing unnecessary parasitics and charge injection effects from CMOS switching and multiplexing circuits, each memristor in the array was directly wired to the amplifier. A diligent USB oscilloscope was used to simultaneously apply the input stimulus and record the circuit's response. The stimulus is applied to the active electrode of the memristor while the counter electrode is held at a virtual ground by the amplifier (Setup diagram and detailed description see Supplementary Fig. S2 and Supplementary Note S2.). The memristors were formed by applying a fixed sinusoidal voltage of 0.8 V, with a frequency of 100 Hz for a duration of 160 ms. Subsequently, experiments to study conductance state and resistance drift were performed. These are briefly outlined next.

SET & RESET: The memristor's state is alternated between set (LRS) and reset (high resistance state), interleaved with read pulses to identify the established state. That is, a set pulse of amplitude 1 V (1 ms) was applied, followed by a read pulse of 0.1 V (200 μ s). Next, a -1 V (1 ms) reset pulse is applied, followed by a similar read pulse. The procedure was repeated 100 times.

Resistance drift: Resistance drift is defined as a change of the memristor state in the absence of any stimulus or the stimulus whose amplitude is between the threshold voltages. To identify these dynamics, a -0.5 V reset pulse followed by three set pulses of 0.5 V was applied. In between the write pulses, 50 read pulses were issued to record the state of the memristor. All stimuli were applied one second apart.

Fabrication of ECM memristors

The fabrication process of inkjet-printed memristors is described in the following. The counter Au electrodes were patterned by laser-ablating a commercially available Au-coated glass (Sigma Aldrich) using a Trumpf TruMicro 5000 picosecond laser. The storage layer, covering the gold electrode, is fabricated by inkjet printing of an in-house-prepared Zinc nitrate-based salt, and precursor ink was prepared by dissolving 0.1 M $\text{Zn}(\text{NO}_3)_2 \cdot 6\text{H}_2\text{O}$ (98%, Sigma Aldrich) in a mixed solution of de-ionized water and glycerin (Merck) (9:1 in volume). The ink was later printed onto Au counter electrodes with a drop-on-demand piezo inkjet printer (DMP2831, Fujifilm). After printing, annealing of the precursor at 400 °C over 2 h is required, to form the ZnO thin film. For the active electrode, a commercially obtained silver nanoparticulate dispersion ink (Silverjet DGP, Sigma Aldrich) was inkjet-printed onto the ZnO layer vertically, to build a crossing junction with the counter electrode, and subsequently annealed at 120 °C for 1 h.

Characterization of ECM memristors

Electrical characterizations on inkjet-printed memristors were carried out at room temperature with a semiconductor parameter analyzer (4200A-SCS, Keithley). The device under test was probed with a probe station (Cascade SUMMIT200) connected to the semiconductor parameter analyzer. For all electrical characterization, the Ag active electrode was electrically stimulated while the Au counter electrode remained grounded at all times.

The threshold voltage was collected through quasi-static voltage sweeping with a forward-and-backward sweeping rate of 0.01 V per step and 0.1 V per step, respectively. First, the printed memristors were formed following the voltage sweeping protocol of 0 V $\rightarrow$ 10 V $\rightarrow$ 0 V with a Compliance Current (CC) of 3 mA. Next, the formed devices were RESET and SET 20 cycles following the voltage sweeping protocol: RESET: 0 V $\rightarrow$ -1.5 V $\rightarrow$ 0 V without CC and SET: 0 V $\rightarrow$ 3 V $\rightarrow$ 0 V with a CC of 3 mA.

SET & RESET: The HRS and LRS resistance values were collected through a dynamic pulsed voltage. The voltage pulse is generated by a Keithley 4225-PMU and 4225-RPM. The width and amplitude of voltage pulse were fixed at 10 μ s and 3 V for SET, and at 50 μ s and -2.5 V for RESET. A read pulse (1 μ s in width and 0.01 V in height) was used to determine the resistance after each SET and RESET voltage pulse.

Resistance drift: To evaluate the resistance drift of HRS and LRS, the device under test was SET and RESET using the same voltage pulse as aforementioned, while after each operation voltage pulse, the resistance was continuously read by 100 repeated voltage pulses (0.2 s in width and 0.01 V in height). An interval of 1 s was put between two read pulsed voltages.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Code availability

The code supporting this work is available at <https://github.com/ElectX/MemSim-Model>, providing access to relevant scripts and resources to the model MemSim+.

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Conceptualization and methodology: G.G., D.R., and N.T.; fabrication: H.H.; measurements: H.H. and L.V. Fitting: G.G. and D.R.; simulation and co-design: G.G.; validation: G.G., H.H., D.R., L.V., and N.T.; formal analysis: G.G. and N.T.; investigation: G.G., H.H., and N.T.; resources: J.A. and N.T.; writing—original draft preparation: G.G., D.R., H.H., L.V., and N.T.; writing—review and editing: G.G., H.H., L.V., G.M., J.A., and N.T.; supervision, project administration, and funding acquisition: J.A. and N.T. All authors have read and agreed to the published version of the manuscript.

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The authors declare no competing interests.

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