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Improvement of Positive and Negative Feedback Power Hardware-in-the-Loop Interfaces Using Smith Predictor

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Abstract

Power hardware-in-the-loop (PHIL) creates a safe test environment to connect simulations with real hardware under test (HuT). Therefore, an interface algorithm (IA) must be chosen. The ideal transformer method (ITM) and the partial circuit duplication (PCD) are popular IAs, where a distinction is made between voltage- (V-) and current-type (C-) IAs. Depending on the sample time of the simulator and further delays, simulation accuracy is reduced and instability can occur due to negative feedback in the V-ITM and C-ITM control loops, which makes PHIL operation impossible. In the case of positive feedback, such as with the V-PCD and C-PCD, the delay causes destructive interference, which results in a phase shift and attenuation of the output signal. In this article, a novel damped Smith predictor (SP) for positive feedback PHIL IAs is presented, which significantly reduces destructive interference while allowing stable operation at low linking impedances at V-PCD and high linking impedances at C-PCD, thus reducing losses in the system. Experimental results show a reduction in phase shift by 21.17° and attenuation improvement of 24.3% for V-PCD at a sample time of 100 µs. The SP transfer functions are also derived and integrated into the listed negative feedback IAs, resulting in an increase in the gain margin (GM) from approximately one to three, which significantly enhances system stability. The proposed methods can improve stability and accuracy, which can be further improved by calculating the HuT impedance in real-time and dynamically adapting the SP model. Stable PHIL operation with SP is also possible with SP model errors or sudden HuT impedance changes, as long as deviations stay within the presented limits.

Keywords: digital real-time simulator; ideal transformer method; partial circuit duplication; power hardware-in-the-loop; Smith predictor; time delays

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1. Introduction

Power hardware-in-the-loop (PHIL) enables the analysis of interactions between physical hardware under test (HuT) and a simulation in a safe laboratory environment. For example, solar inverters [1–3], cables [4], grid protection systems [5,6], and energy storage systems [7] serve as HuT. The system of interest can be models of DC microgrids [8] or other digital twins, such as benchmark networks [9,10]. These models are simulated in real-time on appropriate digital real-time simulators (DRTSs) with defined sample times. For phasor simulations and models that do not require such a high level of accuracy, a larger sample time can be chosen [11], which is typically between 1 and 10 ms [12]. Electromagnetic transient (EMT) simulations and models that require a higher level of

accuracy are calculated with sample times in the microsecond range. In addition to the more expensive DRTS, less expensive PHIL setups, but with longer sample times, can be realized based on programmable logic controllers, microcontrollers, or PCs [11,13,14].

To connect the real HuT to the simulation, a power amplifier (PA) is used. The PA typically receives its setpoint via an optical link (OL) or analog interface, which, depending on the PHIL interface algorithm (IA), can either be a current or voltage signal that is calculated by the DRTS. To account for the behavior of the HuT, the voltage and current at the HuT are measured either by additional measurement systems or by measurement systems integrated into the PA and are subsequently fed back into the simulation. The system time delay consists of two components: the sample time and the time needed for communication, conversion, and measurement of signals. Hence, lower communication latency is preferred, making OL communication favorable due to its lower latency [11,15]. Because PHIL setups are mixed-signal systems, the sum of the continuous time delays must ideally be smaller than the sample time of the DRTS [16], to ensure that the total closed loop time delay can be assumed as twice the simulation DRTS sample time [17,18]. Otherwise, the total system time delay can consist of three or more discrete sample times, which may result in lower stability and accuracy. In practice, it is challenging to model reality accurately with a PHIL setup due to time delays and non-ideal transmission behavior caused by the low-pass behavior of the PA, DRTS discretization effects, and other parasitic effects, as shown in [10,19]. For a more accurate stability analysis of the system, it is necessary to determine the closed loop and all system parameters as accurately as possible [20].

In addition, an appropriate IA must be selected to match the setup, where a distinction is made between the voltage-type (V-) and current-type (C-) IA, which describes the setpoint for the PA. In [12,21], the ideal transformer method (ITM) is referred to as the most commonly used IA because it is easy to implement and provides a high level of accuracy. However, it is shown in [19,21] that the ITM quickly reaches its stability limit, which is caused by two factors: the ratio between the simulated impedance and the actual HuT impedance, as well as the time delay and parasitic effects of the system. The stability and the scope of the setup can be improved by introducing a first-order low-pass filter (LPF) in the measurement feedback, which is shown in [10,22]. However, this reduces the bandwidth, dynamics, and accuracy of the PHIL setup. In [23], a coupling method is presented, which was transferred to PHIL in a modified form and is known as partial circuit duplication (PCD). In [12,24], the method is used for large-scale systems when the HuT is bonded to the simulated system through a linking impedance. The PCD method has the advantage that it is theoretically always stable and the gain margin (GM) increases with increasing linking impedances at V-PCD and decreasing linking impedance at C-PCD. However, this results in increased system losses, as well as lower accuracies [25]. In all IAs, there is a trade-off between dynamics, bandwidth, accuracy, scope, and, most importantly, the stability of the system [25].

The effect of time delay on system stability and accuracy depends on the IA used [26,27]. For negative feedback control loops, such as V-ITM and C-ITM, the stability and accuracy decrease for higher time delays. In contrast, for positive feedback control loops, such as V-PCD and C-PCD, phase shift and attenuation increase with time delay due to destructive interference, which significantly reduces accuracy. These negative effects also occur in other, more stable IAs, such as the damping impedance method (DIM) and the transmission line model (TLM) presented in [21,25,28], and increase with larger time delay. For both categories of IAs, additional noise perturbation in the control loop, such as measurement noise, further reduce stability and accuracy. Hence, this paper aims at developing methods that compensate the time delay of the system to ensure more accurate PHIL simulations. To achieve this, a method based on the Smith predictor (SP) is proposed.

The SP is a method from control theory that can be used to compensate time delay and its negative effects in systems. First applications of SP-based approaches can be found in [29,30], where an SP is applied to V-ITM. In [29], an SP circuit for this IA is presented. The improvement of stability is validated and a real-time sliding discrete Fourier transform measurement of the HuT impedance is added.

This article highlights the novelty of an advanced filtered SP developed for positive feedback PHIL setups, which represents a significant advancement for the V-PCD and C-PCD IAs, by reducing the destructive interference. This indicates a significant reduction in both phase shift and attenuation. This new damped SP compensates the time delay and also enables practical, more accurate, and stable operation of the PHIL setup at low linking impedances for V-PCD and high linking impedances for C-PCD, thereby reducing power losses in the system. The article also demonstrates how an SP significantly improves system stability—by approximately a factor of three—for systems with negative feedback control loops, by compensating the time delay and ensuring higher accuracy. First, the SP is applied to the V-ITM, which is already established in [29]. Furthermore, as a novelty, this article shows the first application of an SP in the C-ITM. The article shows how real-time impedance calculation of the passive HuT using measured values and dynamic adaptation of the SP model significantly improves stability and maintains a nearly constant GM.

This article is structured as follows: Section 2 provides a general overview of the system time delay composition and the operating principle of the PCD and ITM IAs. Section 3 derives the mathematical functions and block diagrams of the SP for V-ITM, C-ITM, V-PCD, and C-PCD, which compensate the system time delay. The advanced damped SP for V-PCD and C-PCD with positive feedback is presented. The simulation results are shown and analyzed in Section 4. In Section 5, experimental results are presented to validate the simulation results and demonstrate the enhanced stability and accuracy of the practical PHIL setups. Finally, Section 6 offers the conclusion and provides a brief outlook.

2. Interface Algorithms

The most common and straightforward IAs are the ITM and PCD. A qualitative visual comparison of the two IAs is shown in Figure 1, and they are examined in more detail in the following sections. A distinction is made between V-IA and C-IA, which are based on voltage and current setpoints, respectively. Depending on the IAs, the measured HuT current or voltage is fed back into the simulation.

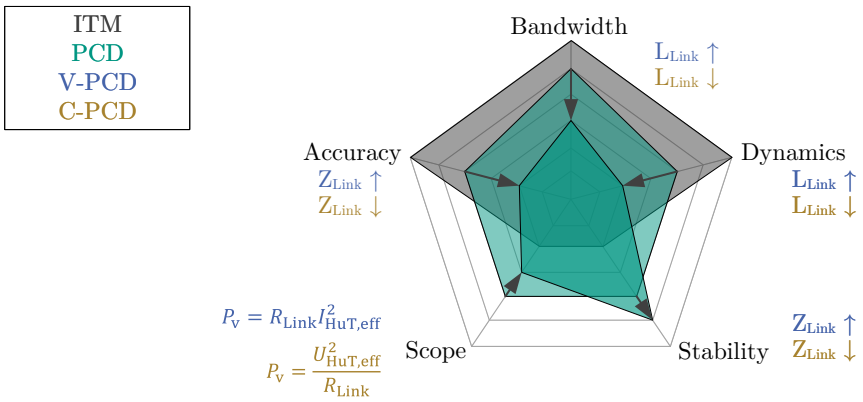

Figure 1. Comparison between ITM and PCD IA - the linking impedance effects the trade-off between accuracy, bandwidth, dynamics, stability, and scope.

The continuous open loop time delay $T_{d,Cont}$ of each IA consists of the simulation sample time T_{DRTS}, the digital-to-analog conversion time $T_{D/A}$, the analog-to-digital conversion time $T_{A/D}$, the measurement time T_{Meas}, and additional time delays T_{Rest}:

$$T_{\mathrm{d,Cont}} = T_{\mathrm{DRTS}} + T_{\mathrm{D/A}} + T_{\mathrm{Meas}} + T_{\mathrm{A/D}} + T_{\mathrm{Rest}} \tag{1}$$

However, since PHIL is a coupling of a discrete and continuous system, the closed loop time T_{d}, which is here important for the stability, equals twice the DRTS sample time if the continuous system is fast enough:

$$T_{\mathrm{d}} = 2 \cdot T_{\mathrm{DRTS}} \mathrel{\widehat{=}} z^{-2} \tag{2}$$

2.1. Ideal Transformer Method

2.1.1. Voltage-Type ITM

The IA based on the V-ITM is illustrated in Figure 2. The voltage V_{RTS} across an ideal controlled current source is calculated in the simulation and transmitted to a PA as a setpoint, which is presented as a controlled voltage source. Depending on the actual HuT impedance Z_{HuT}, a current I_{HuT} flows. This current is measured and fed back into the simulation. The voltage V_{RTS} is calculated in the DRTS depending on the calculated simulation voltage V_{Sim} and the simulated impedance Z_{Sim}, which depends on the simulated network. The block diagram of the control circuit is shown in Figure 3, the parameters of which are discussed next.

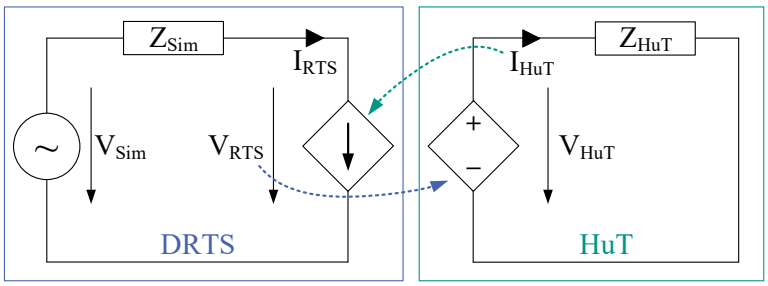

Figure 2. Equivalent circuit of V-ITM IA.

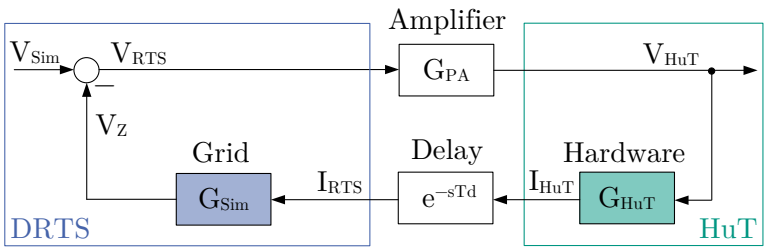

Figure 3. Block diagram of V-ITM IA.

The transfer function of the simulation G_{Sim} includes the simulated inductance L_{Sim} and resistance R_{Sim}:

$$G_{\mathrm{Sim}} = Z_{\mathrm{Sim}} = s\,L_{\mathrm{Sim}} + R_{\mathrm{Sim}} = s\,620\,\mu\mathrm{H} + 22.18\,\Omega \tag{3}$$

The transfer function of the hardware G_{HuT} is given by the series connection of the hardware inductance L_{HuT} and the real resistance R_{HuT}:

$$G_{\mathrm{HuT}} = \frac{1}{Z_{\mathrm{HuT}}} = \frac{1}{s\,L_{\mathrm{HuT}} + R_{\mathrm{HuT}}} = \frac{1}{s\,620\,\mu\mathrm{H} + 22.18\,\Omega} \tag{4}$$

The open loop transfer function $G_{\mathrm{O,ITM}}$ includes the second-order low-pass behavior of the PA G_{PA}, which slightly improves stability due to its negative poles but also reduces accuracy and bandwidth for $\omega_0 = 180\,\mathrm{kHz}$ and $D = 0.9$:

$$G_{\mathrm{PA}} = \frac{1}{\frac{s^2}{\omega_0^2} + \frac{s\,2D}{\omega_0} + 1} \tag{5}$$

$$G_{\mathrm{O,ITM}} = G_{\mathrm{PA}} G_{\mathrm{HuT}} G_{\mathrm{Sim}} e^{-sT_{\mathrm{d}}} \tag{6}$$

Analyzing the open loop transfer function according to (6) for stability with different system time delays results in Figure 4. The GM decreases here with increasing time delay T_{d}. The setup becomes unstable if the time delay is too large, meaning that operation is not possible in this case. The closed loop transfer functions are calculated by dividing the output signals of the IA by the input voltage V_{Sim} and G_{C} results for V-ITM as follows:

$$G_{\mathrm{C,VITM}} = \frac{G_{\mathrm{PA}}}{1 + G_{\mathrm{PA}} G_{\mathrm{HuT}} G_{\mathrm{Sim}} e^{-sT_{\mathrm{d}}}} \tag{7}$$

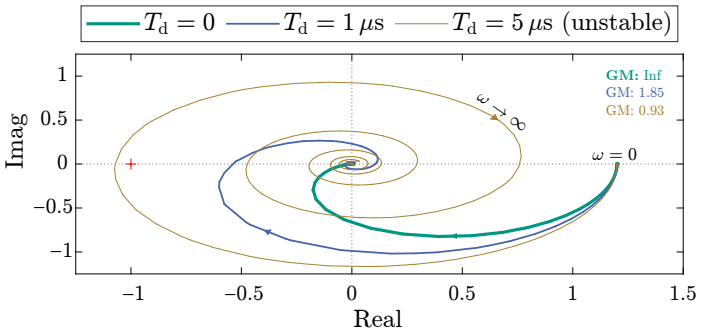

Figure 4. Influence of system time delay on GM: V-ITM ($Z_{\mathrm{Sim}} = 1.2 \cdot Z_{\mathrm{HuT}}$, see (3) and (4)) or C-ITM ($Z_{\mathrm{HuT}} = 1.2 \cdot Z_{\mathrm{Sim}}$, see (8) and (9)).

2.1.2. Current-Type ITM

The C-ITM according to Figure 5 is similar to the equivalent circuit of the V-ITM, where the current I_{RTS} is calculated in the simulation as the setpoint for the PA, which is presented as a controlled current source. Depending on the HuT current and the HuT impedance Z_{HuT}, the voltage V_{HuT} results. This voltage is measured and fed back into the simulation using an ideal controlled voltage source. The new current value is calculated depending on the simulated impedance Z_{Sim} and the simulation voltage V_{Sim}. The corresponding block diagram of the control circuit is shown in Figure 6 and the transfer function is derived next. The simulation and HuT transfer functions are defined as

$$G_{\mathrm{Sim}} = \frac{1}{Z_{\mathrm{Sim}}} = \frac{1}{s\,L_{\mathrm{Sim}} + R_{\mathrm{Sim}}} = \frac{1}{s\,620\,\mu\mathrm{H} + 22.18\,\Omega} \tag{8}$$

$$G_{\mathrm{HuT}} = Z_{\mathrm{HuT}} = s\,L_{\mathrm{HuT}} + R_{\mathrm{HuT}} = s\,620\,\mu\mathrm{H} + 22.18\,\Omega \tag{9}$$

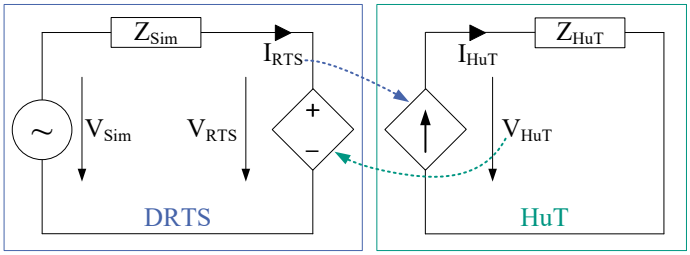

Figure 5. Equivalent circuit of C-ITM IA.

The GM also decreases here with increasing time delay, which can be seen in Figure 4. Assuming that the PA has the same transfer function for setting a voltage (constant voltage mode) as for setting a current (constant current mode), the same Nyquist stability conditions

apply to C-ITM as to V-ITM and both methods only differ in the fact that the ratio of the impedances is reciprocal. The open loop transfer function is calculated according to (6) and the closed loop transfer function is calculated as follows:

$$G_{\mathrm{C,CITM}} = \frac{G_{\mathrm{Sim}} G_{\mathrm{PA}}}{1 + G_{\mathrm{Sim}} G_{\mathrm{PA}} G_{\mathrm{HuT}} e^{-s\,T_{\mathrm{d}}}} \tag{10}$$

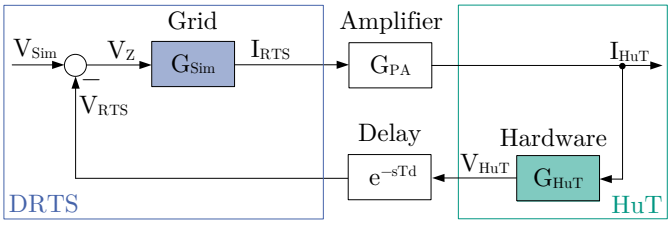

Figure 6. Block diagram of C-ITM IA.

2.2. Partial Circuit Duplication

2.2.1. Voltage-Type PCD

Figure 7 shows the equivalent circuit of the V-PCD method. The linking impedance Z_{Link} represents the coupling impedance between the HuT and the PA. It is also implemented in the simulation, affecting the current I_{RTS} along with the variables V_{Sim}, V'_{HuT}, and Z_{Sim}, which determine the voltage across the simulated impedance Z_{Sim}. The voltage V_{Sim} is used to calculate the setpoint for the PA, which acts as a controlled voltage source. As a result of the voltage V'_{RTS}, a real current I_{HuT} flows depending on Z_{Link} and Z_{HuT}. The real voltage V_{HuT} is measured and fed back into the simulation by an ideal controlled voltage source.

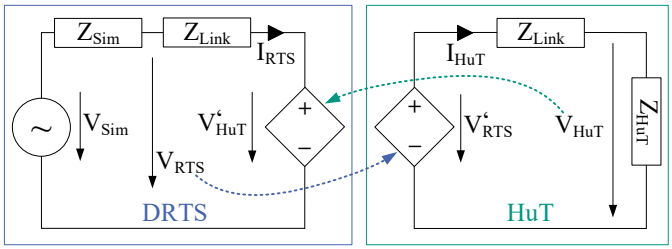

Figure 7. Equivalent circuit of V-PCD IA.

To transform the equivalent control diagram in Figure 7 into the block diagram in Figure 8, the following additional transfer function G_{Gain} is introduced according to [28]:

$$G_{\mathrm{Gain}} = \frac{Z_{\mathrm{Sim}}}{Z_{\mathrm{Link}}} \tag{11}$$

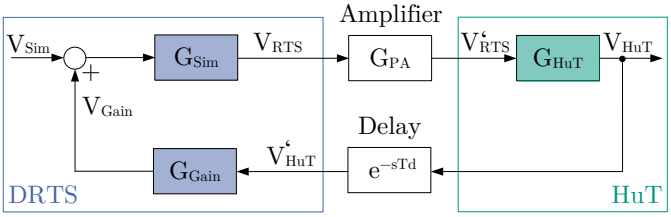

Figure 8. Block diagram of V-PCD IA.

In the V-PCD control loop, positive feedback occurs, which causes destructive interference due to time delays in the system. The influence of the time delay on the output signal V_{HuT} is illustrated in Figure 9, where the attenuation and phase shift increase with increasing time delay. Note that in an ideal system without time delay, there is no destructive interference and thus no additional phase shift and attenuation.

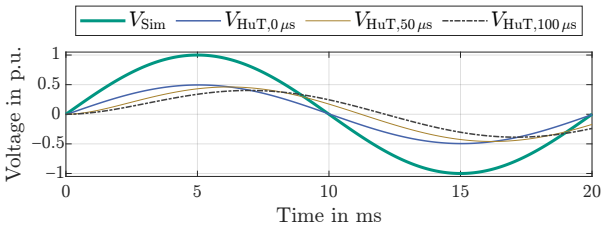

Figure 9. Influence of the time delay on the attenuation and the phase shift of the output signal in the V-PCD due to destructive interference with $Z_{\text{Sim}} = Z_{\text{HuT}}$ and $Z_{\text{Link}} = R_{\text{Sim}}/50$; see (14) and (15).

The transfer functions and impedances of the simulation and the hardware are defined as follows:

$$G_{\text{Sim}} = \frac{Z_{\text{Link}}}{Z_{\text{Link}} + Z_{\text{Sim}}} \tag{12}$$

$$G_{\text{HuT}} = \frac{Z_{\text{HuT}}}{Z_{\text{Link}} + Z_{\text{HuT}}} \tag{13}$$

$$Z_{\text{Sim}} = s\,L_{\text{Sim}} + R_{\text{Sim}} = s\,620\,\mu\text{H} + 22.18\,\Omega \tag{14}$$

$$Z_{\text{HuT}} = s\,L_{\text{HuT}} + R_{\text{HuT}} = s\,620\,\mu\text{H} + 22.18\,\Omega \tag{15}$$

The general open loop transfer function can be determined from Figure 8:

$$G_{\text{O,PCD}} = G_{\text{Sim}} G_{\text{PA}} G_{\text{HuT}} G_{\text{Gain}} e^{-s\,T_{\text{d}}} \tag{16}$$

The Nyquist criterion is used to analyze the stability of the open loop transfer function, for which the positive feedback has to be considered, as depicted in Figure 10. Whereas the PHIL setup using V-PCD is always stable in theory and only becomes unstable if Z_{Link} is zero, the experimental setup shows that noise and numerical errors can cause unstable states for small Z_{Link}. It should be noted that while large Z_{Link} values increase stability, they come at the cost of higher losses and lower accuracy. Hence, the choice of Z_{Link} is not straightforward and must be carefully considered. In practical setups, a minimum value of Z_{Link} is often predefined by the coupling impedance and is assumed to be fixed, which is why the first compromise between accuracy, losses, and stability is often defined in this setup. In addition to the coupling impedance, system time delays further reduce accuracy. The V-PCD open loop transfer function $G_{\text{O,VPCD}}$ can be calculated using (16). The closed loop transfer function of the V-PCD with positive feedback is calculated as follows:

$$G_{\text{C,VPCD}} = \frac{G_{\text{Sim}} G_{\text{PA}} G_{\text{HuT}}}{1 - G_{\text{O,VPCD}}} \tag{17}$$

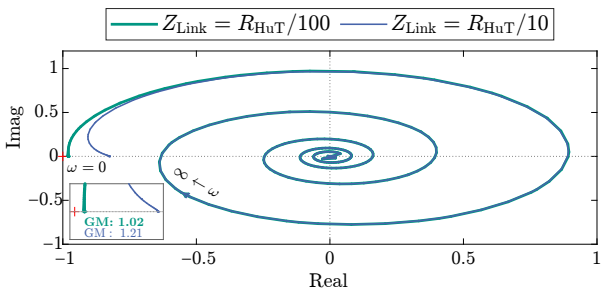

Figure 10. Influence of the linking impedance on the GM of the V-PCD, at $T_{\text{d}} = 5\,\mu\text{s}$ and $Z_{\text{HuT}} = Z_{\text{Sim}}$; see (14) and (15).

2.2.2. Current-Type PCD

Figure 11 shows the equivalent circuit of the C-PCD. In this setting, the total current I'_{RTS} results from the voltage V_{Sim}, the simulation impedance Z_{Sim}, the simulated linking

impedance Z_{Link}, and the current I'_{HuT} from the last simulation step provided by the ideal current source. This setpoint is transmitted to the PA and set, which acts as a controlled current source. The current I'_{RTS}, the impedance Z_{HuT}, and the linking impedance Z_{Link} result in the total current I_{HuT}, which is measured and fed back to the simulation using an ideal current source. After converting the current source into a voltage source on the simulation side, the control circuit in Figure 12 is obtained.

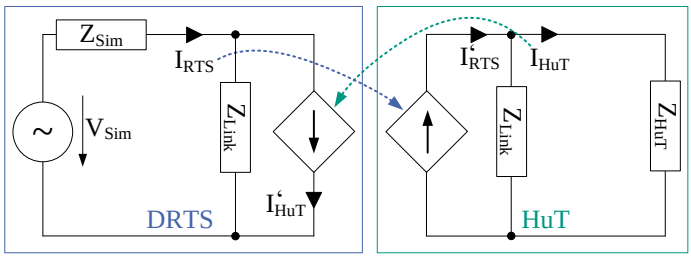

Figure 11. Equivalent circuit of C-PCD IA.

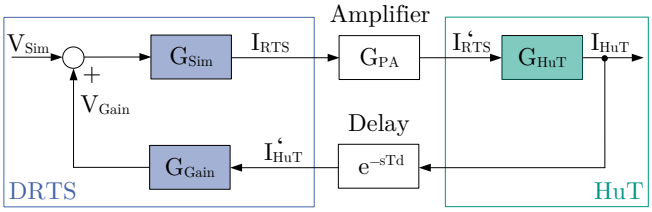

Figure 12. Block diagram of C-PCD IA.

The impedances of both the simulation and the HuT are determined according to (14) and (15). The transfer functions of the C-PCD control loop are defined as follows:

$$G_{\text{Gain}} = Z_{\text{Link}}, \quad G_{\text{Sim}} = \frac{1}{Z_{\text{Link}} + Z_{\text{Sim}}} \tag{18}$$

$$G_{\text{HuT}} = \frac{Z_{\text{Link}} Z_{\text{HuT}}}{(Z_{\text{Link}} + Z_{\text{HuT}}) Z_{\text{HuT}}} \tag{19}$$

Whereas the C-PCD open loop transfer function $G_{\text{O,CPCD}}$ is calculated according to (16), the closed loop transfer function with positive feedback is defined as follows:

$$G_{\text{C,CPCD}} = \frac{G_{\text{Sim}} G_{\text{PA}} G_{\text{HuT}}}{1 - G_{\text{O,CPCD}}} \tag{20}$$

Figure 13 shows that a small linking impedance Z_{Link} has a positive effect on stability. However, this reduces the accuracy. For an infinite Z_{Link}, the control loop is theoretically unstable. In practice, parasitic effects such as measurement noise and numerical errors can also cause the control loop to become unstable for finite Z_{Link}.

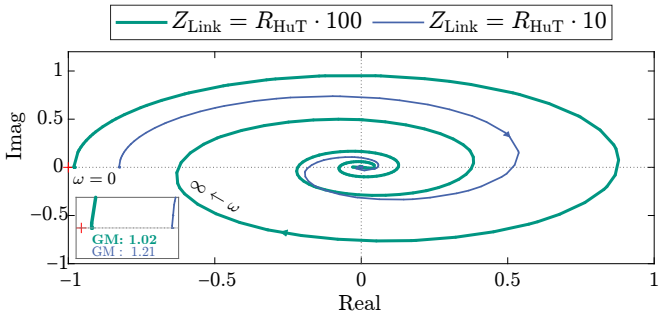

Figure 13. Influence of the linking impedance on the GM of the C-PCD, at $T_{\text{d}} = 5\,\mu\text{s}$ and $Z_{\text{HuT}} = Z_{\text{Sim}}$; see (14) and (15).

3. Smith Predictor

3.1. Compensated Voltage-Type ITM

To compensate system time delay, ref. [29] shows that an expression must be found that includes the estimated open loop transfer function without time delay $\widetilde{G}^*_{\mathrm{O}}$ and the estimated total time delay $\widetilde{T}_{\mathrm{d}}$, which is summarized and shifted to the feedback path for simplified calculation. For V-ITM, the closed loop transfer function without time delay G^*_{C} with SP is obtained as

$$G^*_{\mathrm{C,VITM}} = \frac{G_{\mathrm{PA}}}{1 + G^*_{\mathrm{O,VITM}} e^{-s\,T_{\mathrm{d}}} + \widetilde{G}^*_{\mathrm{O,VITM}} \left(1 - e^{-s\,\widetilde{T}_{\mathrm{d}}}\right)} \tag{21}$$

The equation for the SP can be transformed into a block diagram and integrated into the V-ITM, resulting in the control circuit depicted in Figure 14. If the estimated open loop transfer function, consisting of G_{PA}, G_{Sim}, and G_{HuT}, is ideal, the closed loop equation can be simplified:

$$G^*_{\mathrm{C,VITM}} = \frac{G_{\mathrm{PA}}}{1 + \widetilde{G}^*_{\mathrm{O,VITM}}} \tag{22}$$

In this SP approaches, the time delay is mathematically completely compensated, as the corresponding terms cancel each other out completely for an ideal SP model.

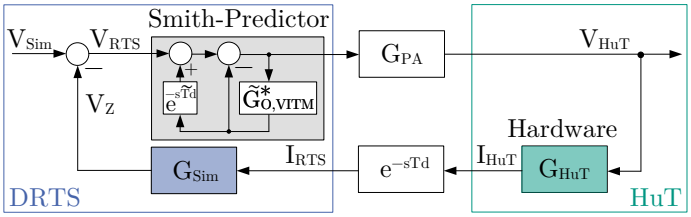

Figure 14. Block diagram of compensated V-ITM IA.

With the ideal estimated model, an impedance ratio of 1.2, and complete compensation of the time delay, the Nyquist curve of the open loop system is illustrated in Figure 15.

For different time delays and an impedance ratio of 1, this results in a GM rounded to 3.0, as shown in Table 1.

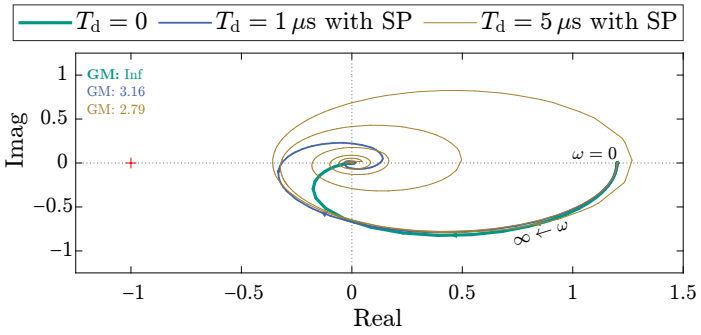

Figure 15. Time delay compensation by the SP at the V-ITM increases GM, with $Z_{\mathrm{Sim}} = 1.2 \cdot Z_{\mathrm{HuT}}$; see (3) and (4) (cf. Figure 4).

3.2. Compensated Current-Type ITM

As with the V-ITM, the estimation of the open loop transfer function and the time delay must be known for complete compensation. The following mathematical expression is derived for the closed loop:

$$G^*_{\mathrm{C,CITM}} = \frac{G_{\mathrm{PA}} G_{\mathrm{Sim}}}{1 + G^*_{\mathrm{O,CITM}} e^{-s\,T_\mathrm{d}} + \widetilde{G}^*_{\mathrm{O,CITM}} \left(1 - e^{-s\,\widetilde{T}_\mathrm{d}}\right)} \tag{23}$$

The block diagram of the SP is illustrated in the left diagram in Figure 16. The closed loop with ideal time delay compensation is defined as

$$G^*_{\mathrm{C,CITM}} = \frac{G_{\mathrm{PA}} G_{\mathrm{Sim}}}{1 + \widetilde{G}^*_{\mathrm{O,CITM}}} \tag{24}$$

The rounded GM of the compensated open loop with SP is 3.0 for an impedance ratio of 1, as shown in Table 1.

Table 1. Theoretical GMs at different time delays for ITM and PCD with and without SP. For PCD an LPF is added in the SP (marked as $*$).

$Z_{\mathrm{Sim}} = Z_{\mathrm{HuT}} = s\,620\,\mu\mathrm{H} + 22.18\,\Omega \mid Z_{\mathrm{Link,VPCD}} = R_{\mathrm{Sim}}/50 \mid Z_{\mathrm{Link,CPCD}} = 50\,R_{\mathrm{Sim}} \quad *f_{\mathrm{c,LPF}} = 6\,\mathrm{kHz}$						
T_d in µs	V-ITM/C-ITM	V-ITM/C-ITM with SP	V-PCD	V-PCD with SP $*$	C-PCD	C-PCD with SP $*$
5	1.1199	2.9692	1.0404	1.0404	1.0404	1.0404
50	1.0018	2.9994	1.0105	1.0404	1.0521	1.0404
70	1.0009	2.9997	1.0095	1.0404	1.0465	1.0404
100	1.0005	2.9999	1.0106	1.0404	1.0435	1.0404

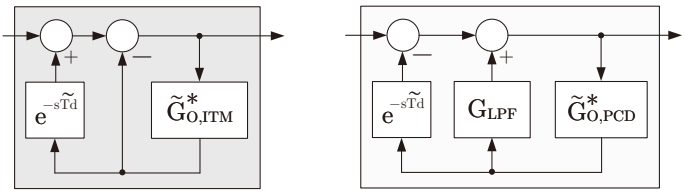

Figure 16. Block diagram of SP for ITM (**left**) and PCD (**right**).

3.3. Compensated Voltage-Type PCD

Theoretically, the control loop of the V-PCD can only become unstable if Z_{Link} equals zero. A complete compensation of time delay eliminates the destructive interference and thus the resulting attenuation and phase shift. Due to the positive sum in the control loop, the SP transfer function must be derived in a modified way. The closed loop transfer function is defined as

$$G^*_{\mathrm{C,VPCD}} = \frac{G_{\mathrm{PA}} G_{\mathrm{Sim}} G_{\mathrm{HuT}}}{1 - \widetilde{G}^*_{\mathrm{O,VPCD}} \left(1 - e^{-s\widetilde{T}_\mathrm{d}}\right) - G^*_{\mathrm{O,VPCD}} e^{-s\,T_\mathrm{d}}} \tag{25}$$

In practice, effects such as measurement noise and numerical errors can lead to instability when Z_{Link} is small. If the time delay is completely compensated by the SP, i.e., two sample times, the control loop can become unstable due to the effects mentioned or due to a minimal difference in the estimated model. This effect can be also observed when using the SP, since the SP does not significantly increase the GM, as can be concluded from Table 1. Therefore, the aim is to completely compensate the time delay, while maintaining sufficient attenuation at low Z_{Link} in order to be able to keep the system stable. Therefore, a filtered SP is derived, which provides additional damping through an added first-order LPF. The block diagram of the filtered SP is illustrated in the right of Figure 16. The transfer function of the compensated closed loop is defined as follows:

$$G^*_{\mathrm{C,VPCD}} = \frac{G_{\mathrm{PA}} G_{\mathrm{Sim}} G_{\mathrm{HuT}}}{1 - \widetilde{G}^*_{\mathrm{O,VPCD}} \left(G_{\mathrm{LPF}} - e^{-s\widetilde{T}_{\mathrm{d}}} \right) - G^*_{\mathrm{O,VPCD}} e^{-s\,T_{\mathrm{d}}}} \tag{26}$$

The integrated LPF reduces the dynamics and bandwidth depending on the cut-off frequency $f_{\mathrm{c,LPF}}$, which should therefore be selected as high as possible and be adapted to the setup. With an ideal estimated model, integrated LPF and complete time delay compensation, the following closed loop transfer function is achieved:

$$G^*_{\mathrm{C,VPCD}} = \frac{G_{\mathrm{PA}} G_{\mathrm{Sim}} G_{\mathrm{HuT}}}{1 - \widetilde{G}^*_{\mathrm{O,VPCD}} G_{\mathrm{LPF}}} \tag{27}$$

The significance and influence of the LPF for positive feedback IAs are explained using a clear example, which also makes practical design easier.

The following stability limit results for the Nyquist stability analysis with SP and integrated LPF:

$$| - \widetilde{G}^*_{\mathrm{O,VPCD}} G_{\mathrm{LPF}} + \widetilde{G}^*_{\mathrm{O,VPCD}} e^{-s\widetilde{T}_{\mathrm{d}}} - \underbrace{G^*_{\mathrm{O,VPCD}} e^{-sT_{\mathrm{d}}}}_{G_{\mathrm{O,VPCD}}} | = 1 \tag{28}$$

For this example, the estimated model of the SP assumed to be ideal:

$$\widetilde{G}^*_{\mathrm{O,VPCD}}\, e^{-s\widetilde{T}_{\mathrm{d}}} = G^*_{\mathrm{O,VPCD}}\, e^{-s\ T_{\mathrm{d}}} \tag{29}$$

If Z_{Link} is also negligibly small, the following stability limit results:

$$| - \widetilde{G}^*_{\mathrm{O,VPCD}} G_{\mathrm{LPF}}| = \left| - \underbrace{\frac{\widetilde{Z}_{\mathrm{Sim}} \widetilde{Z}_{\mathrm{HuT}}}{\widetilde{Z}_{\mathrm{Sim}} \widetilde{Z}_{\mathrm{HuT}}}}_{=1} \underbrace{\frac{1}{\frac{1}{2\pi f_{\mathrm{c,LPF}}} s + 1}}_{G_{\mathrm{LPF}}} \right| = 1 \tag{30}$$

The example shows that, in addition to the value of Z_{Link}, stability can also be determined by selecting the LPF cut-off frequency. The idea behind the filtered SP is to compensate the negative characteristics of attenuation and phase shift caused by the time delay while increasing stability, whereby a smaller attenuation and phase shift caused by the LPF must be accepted. In addition to the theoretical design of the LPF cut-off frequency, it must be tuned in the PHIL setup, as parasitic effects are present in practice.

3.4. Compensated Current-Type PCD

The positive feedback of the control circuit means that the LPF also must be added in the C-PCD and the approach is equivalent to the approaches for the V-PCD. The closed loop transfer function is defined as follows:

$$G^*_{\mathrm{C,CPCD}} = \frac{G_{\mathrm{PA}} G_{\mathrm{Sim}} G_{\mathrm{HuT}}}{1 - \widetilde{G}^*_{\mathrm{O,CPCD}} \left(G_{\mathrm{LPF}} - e^{-s\widetilde{T}_{\mathrm{d}}} \right) - G^*_{\mathrm{O,CPCD}} e^{-s\,T_{\mathrm{d}}}} \tag{31}$$

The following compensated closed loop transfer function results from the ideal estimated model, where the time delay is completely compensated:

$$G^*_{\mathrm{C,CPCD}} = \frac{G_{\mathrm{PA}} G_{\mathrm{Sim}} G_{\mathrm{HuT}}}{1 - \widetilde{G}^*_{\mathrm{O,CPCD}} G_{\mathrm{LPF}}} \tag{32}$$

In the right block diagram of Figure 16, the SP for C-PCD is depicted. The GM of the open loop with and without compensation by the SP is listed in Table 1.

4. Simulation Results

To simulate the time delay compensation with the SP, MATLAB/Simulink is used. The transfer functions of the SP are discretized with the Tustin approximation and represented as a rational linear time-invariant (LTI) function in the z-domain. This allows changing the parameters of the SP in real-time and adjusting the estimated model at each discrete time step.

4.1. Negative Feedback: ITM

The behavior of the SP is analyzed in a simulation. Figure 17 illustrates the HuT current using the C-ITM, when a noise source is added at time $t = 15\,\text{ms}$ for a control loop operated at the stability limit. It can be observed that the control loop oscillates and becomes unstable without SP. In this state, the current oscillates at high frequencies with an increasing amplitude, ultimately saturating the entire figure. This unstable condition prevents safe PHIL operation and poses a risk to the HuT. With the SP, the control loop remains stable due to the established GM. The behavior with and without SP can be effectively compared for the V-ITM due to the negative feedback at the controller input and two other factors: Firstly, the system time delay is identical. Secondly, the V-ITM open loop transfer function is the same, except for a reciprocal impedance ratio, assuming the behavior of the PA is identical. For the V-ITM and inductive HuT, the current change is limited by the integrating behavior, which can have a positive effect on stability in practice. The results are shown in Table 1.

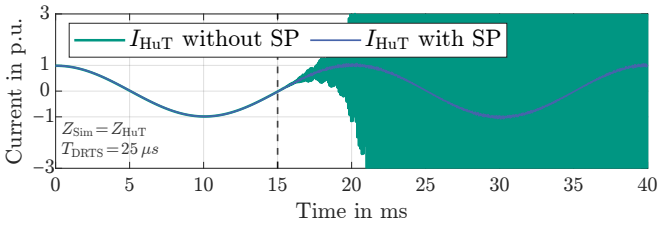

Figure 17. Simulation: C-ITM with activated disturbance factor = 1.1 at t = 15 ms; see (8) and (9).

4.2. Positive Feedback: PCD

When the time delay is completely compensated by the SP, the result in the simulation for V-PCD as well as for C-PCD is an output signal without destructive interference, and thus without attenuation and phase shift, as shown in Figure 9 for V-PCD. Figure 18 shows a V-PCD control loop with damped SP, with $f_{\text{c,LPF}} = 6\,\text{kHz}$. At $t = 15\,\text{ms}$, the filtered SP is deactivated. The results show that the phase shift increases by 9.53° and the attenuation of the output signal increases by 5% without filtered SP (5.2% and 9.44° for C-PCD).

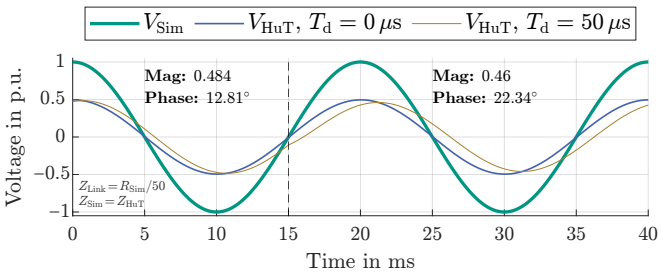

Figure 18. Simulation: Increase in phase shift and attenuation after deactivating compensated SP ($f_{\text{c,LPF}} = 6\,\text{kHz}$) at t = 15 ms at V-PCD; see (14) and (15).

5. Experimental Results

To validate the functionality of the SP in the laboratory, the experimental circuit topology and hardware shown in Figures 19 and 20 are used. The presented setup can be implemented independently of specific DRTS and PA manufacturers. For the PCD IAs, a coupling impedance Z_{Link} is also required. The time delay of the continuous system is 4–6 µs, which is faster than the minimum used sample time T_{DRTS} of 25 µs. Therefore, the maximum time delays according to (2) can be assumed for the SP.

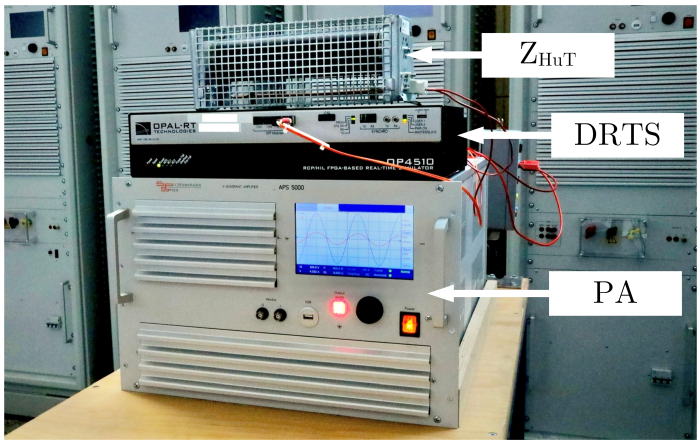

Figure 19. Photograph of the experimental PHIL laboratory setup.

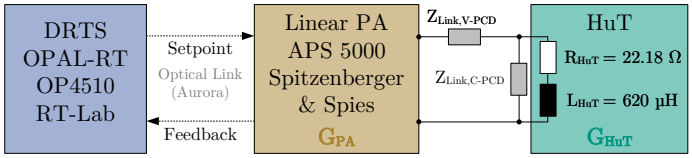

Figure 20. Experimental circuit topology (G_{PA}, compare (5)).

5.1. Negative Feedback: ITM

Figure 21 shows a C-ITM setup with SP, amplified by a disturbance factor of 1.1, where the HuT impedance is provided in Figure 20. At t = 15 ms, the SP is deactivated and the current oscillates. The system becomes unstable and has to be switched off. In this unstable state, the 50 Hz fundamental frequency is superimposed by high-frequency components.

To characterise the unstable state of the PHIL setup, the total harmonic distortion (THD) is calculated. A THD of 5 % is defined as an appropriate threshold for a stable condition, as already shown in [13,19]. Figure 22 shows the stability limit for a C-ITM setup. Without SP the unstable state occurs at a impedance ratio of 1.1. When the SP is activated, the maximum permissible impedance ratio increases to 2.96. Factors such as deviations in the estimated SP model, measurement inaccuracies and numerical errors can influence the result.

The estimated impedance of the HuT ($\widetilde{R}_{\text{HuT}}$ and $\widetilde{L}_{\text{HuT}}$) is calculated in real-time by measuring the HuT voltage, the HuT current, and the phase shift between these 50 Hz values. Based on these measurements, the SP model can be dynamically adapted in real-time. This results in the GM remaining almost constant, as also shown in Figure 22. The slight increase in the THD with the impedance ratio is due to the resulting reduction in the amplitude of the HuT current and a constant noise signal. In theory, with an ideal SP model and no noise, the GM would be constant at a value rounded to 3.0. The measurement results and improvements of the V-ITM are well comparable with the C-ITM results.

In [31] a robust online method for characterizing the HuT's frequency behavior for the SP model is presented, based on harmonic injection and discrete rational transfer function modeling. The frequency response is fitted using a differential evolution optimiza-

tion algorithm, which offers resilience against measurement noise, incomplete datasets, and non-linearities in the z-domain. To demonstrate the effectiveness, a passive solar inverter and an R-L-C series connection are used as HuT. Additionally, the real-time capable technique for estimating the linearized 50 Hz impedance is demonstrated using a grid-feeding solar inverter.

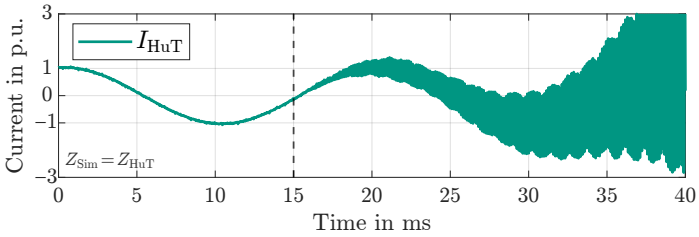

Figure 21. Experiment: Unstable C-ITM with disturbance factor = 1.1 and deactivated SP at t = 15 ms ($T_{\mathrm{DRTS}} = 25$ µs); see (8) and (9) (cf. Figure 17).

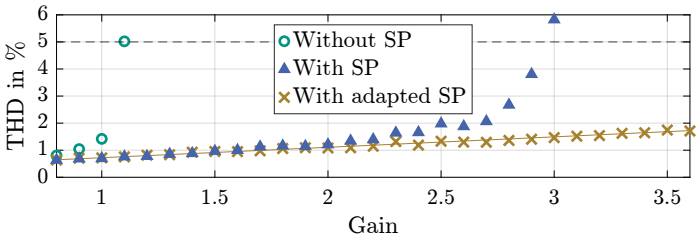

Figure 22. Experiment: C-ITM stability limits with increasing impedance ratio ($T_{\mathrm{DRTS}} = 25$ µs), which means $Z_{\mathrm{HuT}} = \mathrm{Gain} \cdot Z_{\mathrm{Sim}}$ (see (8) and (9)).

5.2. Positive Feedback: PCD

Figure 23 shows the influence of the SP on the phase shift and attenuation at different sample times. The influence of the filtered SP increases with increasing sample time, since destructive interference without SP also rises with increasing sample time. The cut-off frequency of the SP LPF is adjusted to the different sample times, varying between 4 kHz and 8 kHz, and causes a deviation from the ideal signal due to the damping behavior of the LPF. At a sample time of 100 µs and an LPF cut-off frequency of 4 kHz, the SP reduces the phase shift by 21.17° and the attenuation by 24.3%.

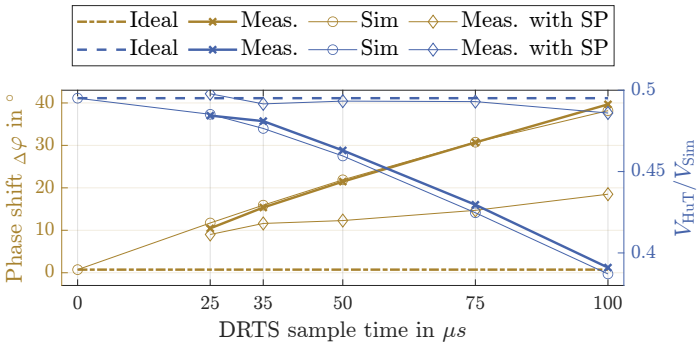

Figure 23. Experiment: Attenuation and phase shift between V_{HuT} and V_{Sim} at V-PCD ($Z_{\mathrm{Link}} = R_{\mathrm{Sim}}/50$ and $Z_{\mathrm{Sim}} = Z_{\mathrm{HuT}}$); see (14) and (15).

In practice, the linking impedance Z_{Link} for V-PCD should be chosen as small as possible to minimize losses and to ensure high accuracy, while maintaining a stable system. Figure 24 illustrates the reduction in phase shift on the left y-axis with SP at a sample time of 50 µs and an LPF cut-off frequency of 6 kHz. The phase shift with SP is significantly reduced, especially at low ratios of Z_{Link} to Z_{Sim}. The right y-axis in Figure 24 illustrates the phase shift reduction with SP at different sample times and adjusted LPF cut-off frequencies.

The reduction in phase shift is more pronounced at lower impedance ratios and increases with higher sample times. Note that the cutoff frequency must be selected based on the sample time and the specific setup. Therefore, in addition to the theoretical design, practical adjustments are made during the experimental setup, starting with a lower cut-off frequency and considering the observed system behavior and prevailing noise level.

Figure 25 demonstrates the impact of cut-off frequency on phase shift and attenuation with a fixed sample time of 50 µs. With a cut-off frequency of 3.2 kHz, the SP significantly reduces both phase shift and attenuation compared to a setup without SP. To minimize phase shift and attenuation with SP, a high cut-off frequency must be chosen. However, it should still be small enough to maintain sufficient GM and ensure stable system operation. A cut-off frequency of 6 kHz works well in this example. Beyond 6 kHz, instability occurs, evident by the increase in output voltage amplitude beyond the theoretical maximum. The measurement results and enhancements of the C-PCD are highly comparable to those of the V-PCD.

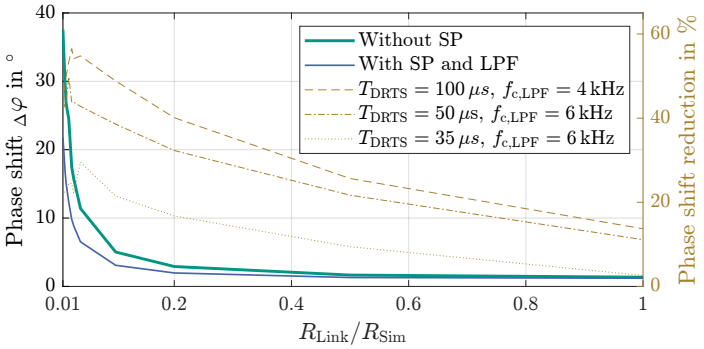

Figure 24. Experiment: V-PCD phase shift between V_{HuT} and V_{Sim} (left y-axis) and phase shift reduction for different time delays with SP (right y-axis) ($Z_{\mathrm{Sim}} = Z_{\mathrm{HuT}}$, see (14) and (15)).

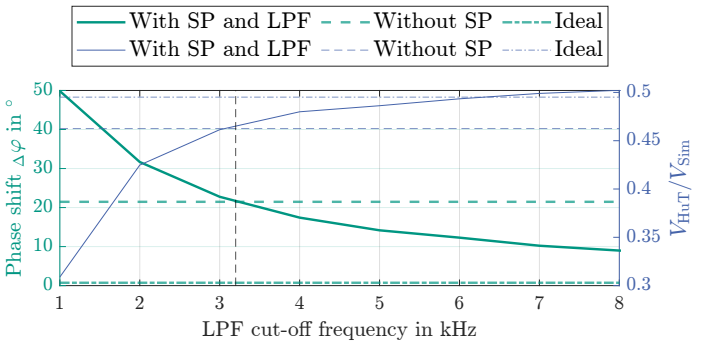

Figure 25. Experiment: V-PCD phase shift and attenuation between V_{HuT} and V_{Sim} ($T_{\mathrm{DRTS}} = 50\,\mu\mathrm{s}$) at different LPF cut-off frequencies, with $Z_{\mathrm{Sim}} = Z_{\mathrm{HuT}}$ and $Z_{\mathrm{Link}} = R_{\mathrm{Sim}}/50$; see (14) and (15).

5.3. Influence of SP Model Deviation

In practical SP approaches, a perfect SP model in the DRTS and a constant HuT impedance are not possible. There are several reasons for this: Firstly, the precise real-time determination of the HuT impedance is infeasible, as it is subject to variations depending on the operating point and additional factors such as temperature. Secondly, in cases of nonlinear HuT behavior, the impedance may change abruptly. Thirdly, the DRTS approximates the differential equations in discrete increments at defined time steps, so all transfer functions used in the simulation are Tustin-discretized and implemented as rational LTI transfer functions. These differences between the discrete SP model and real impedances cause additional deviations. If all these points are considered, stable PHIL operation should be possible within certain limits even if the estimated HuT impedance of the SP is not ideal or if the real HuT impedance changes abruptly.

To investigate the influence of an inaccurate SP model on system stability, the estimated HuT impedance $\widetilde{Z}_{\mathrm{HuT}}$ of the SP model is varied in the first scenario, while the actual HuT impedance Z_{HuT} remains constant. The limits of modeling inaccuracies that still allow stable operation are illustrated in Figure 26. The unstable V-ITM IA configuration with $Z_{\mathrm{Sim}} = 2 \cdot Z_{\mathrm{HuT}}$ is stabilized by the SP. However, if the ratio of inaccuracy exceeds a value of 11 in the experiment, the system begins to run unstably (THD $> 5\%$). Stable operation is preserved for ratios down to 0.01. In theory, the V-ITM IA open loop transfer function with SP and without PA, derived from (21), reaches its Nyquist stability limit at a ratio of four:

$$\text{with} \quad Z_{\mathrm{Sim}} = 2 \cdot Z_{\mathrm{HuT}} \quad \text{and} \quad \widetilde{Z}_{\mathrm{Sim}} = 2 \cdot \widetilde{Z}_{\mathrm{HuT}} \tag{33}$$

$$\left| \frac{2\,Z_{\mathrm{HuT}}}{Z_{\mathrm{HuT}}} e^{-s\,T_{\mathrm{d}}} + \frac{2\,\widetilde{Z}_{\mathrm{HuT}}}{4\,\widetilde{Z}_{\mathrm{HuT}}} - \frac{2\,\widetilde{Z}_{\mathrm{HuT}}}{4\,\widetilde{Z}_{\mathrm{HuT}}} e^{-s\,\widetilde{T}_{\mathrm{d}}} \right| = \left| (2 - 0.5)\, e^{-s\,T_{\mathrm{d}}} + 0.5 \right| < 1 \tag{34}$$

In Figure 26, an increase in THD can already be observed here and the PA further increases the stability limit. Stability improves when the ratio between the estimated and actual HuT impedance is smaller than one. However, the deviations cause a slight deterioration in accuracy.

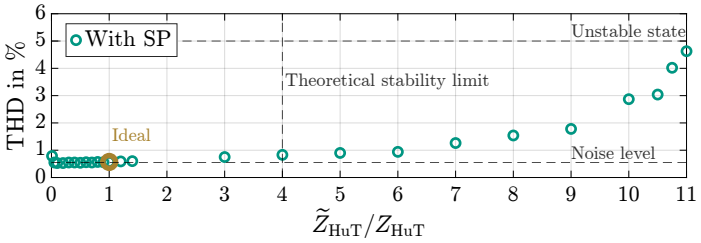

Figure 26. Experiment: Influence of the deviation between estimated SP HuT impedance and real HuT impedance at V-ITM ($T_{\mathrm{DRTS}} = 25\,\mu\mathrm{s}$), with $Z_{\mathrm{Sim}} = 2 \cdot Z_{\mathrm{HuT}}$; see (3) and (4).

In the second scenario, the effect on stability is now examined when the real HuT impedance Z_{HuT} changes, while $\widetilde{Z}_{\mathrm{HuT}}$ remains constant. In this case, the V-ITM setup is also operated under unstable conditions, which means $Z_{\mathrm{Sim}} = 2 \cdot Z_{\mathrm{HuT}}$ and $\widetilde{Z}_{\mathrm{Sim}} = 2 \cdot \widetilde{Z}_{\mathrm{HuT}}$. The following stability condition results in a minimum factor X that constrains the maximum variation of the real Z_{HuT} and must not be undershot. In this example, this leads to $X = 0.4$. If this threshold is not undershot, the system remains stable with a constant SP model, even in the event of a sudden impedance change, as occurs during a low-voltage ride through or with non-linear loads.

$$\left| \frac{2\,Z_{\mathrm{HuT}}}{X\,Z_{\mathrm{HuT}}} e^{-s\,T_{\mathrm{d}}} + \frac{2\,\widetilde{Z}_{\mathrm{HuT}}}{\widetilde{Z}_{\mathrm{HuT}}} - \frac{2\,\widetilde{Z}_{\mathrm{HuT}}}{\widetilde{Z}_{\mathrm{HuT}}} e^{-s\,\widetilde{T}_{\mathrm{d}}} \right| = \left| \left(\frac{2}{X} - 2 \right) e^{-s\,T_{\mathrm{d}}} + 2 \right| < 1 \tag{35}$$

6. Conclusions and Outlook

This article derives the transfer functions of the SP for V-ITM, C-ITM, V-PCD, and C-PCD IAs and integrates them into PHIL simulations and experiments. The SP compensates system time delay in all settings. The V-ITM and C-ITM with negative feedback benefit from the SP's ability to improve stability and accuracy. The GM could be increased from approximately one to three. Real-time HuT impedance calculation and dynamic SP adaptation enhance stability and maintain a nearly constant GM of approximately three. Stable PHIL operation is also possible with a non-ideal SP model or if the HuT impedance changes abruptly, as long as the deviation between the estimated and actual HuT impedance remains within certain limits. In the V-PCD and C-PCD IAs, positive feedback causes destructive interference, increasing phase shift and attenuation with time

delay. A novel damped SP with an integrated LPF compensates time delay, reducing phase shift and attenuation. This filtered SP enables stable, accurate operation for the V-PCD and C-PCD IAs. The filtered SP enabled a reduction in phase shift by 21.17° and a decrease in attenuation by 24.3% for the V-PCD IAs. Compensating time delay with SP expands the use of cheaper DRTS systems with larger sample times by improving stability and accuracy.

Future research will focus on applying the SP approach to further grid use cases, with the objective of analyzing the dynamic behavior of real HuT in compensated PHIL environments.

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Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

The following abbreviations are used in this manuscript:

C-	current-type
DRTS	digital real-time simulator
EMT	electromagnetic transient
GM	gain margin
HuT	hardware under test
IA	interface algorithm
ITM	ideal transformer method
LPF	low-pass filter
OL	optical link
PA	power amplifier
PCD	partial circuit duplication
PHIL	power hardware-in-the-loop
SP	Smith predictor
TLM	transmission line model
V-	voltage-type

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