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ANDESPix: A Digital SiPM for Muon Detectors

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ANDESPix is a digital silicon photomultiplier (SiPM) ASIC designed to readout scintillating fibers with low light intensity, as part of a muon detector, following the same muon detection principle used for muon detectors at the Pierre Auger Observatory. Thereby, photons should be detected with very high time resolution (<100 ps) in order to identify impinging muons and their time of arrival (ToA) on the muon detector. In ANDESPix, each single photon avalanche diode (SPAD) has its own digital readout containing a time-to-digital converter (TDC). The zero-suppressed digital readout allows to receive detailed spatial information of incoming photons. This may lead to better understanding of their nature and increased detector efficiency, as e.g. improved fiber alignment to the SiPM and improved detection of the impinging position along the scintillator bars of the muon detector. ANDESPix is designed in 110 nm CMOS technology from LFoundry (LF11IS). This technology includes a SPAD cell for the wavelength range from 400 nm to 850 nm with high photon detection efficiency (PDE) and low dark count rate (DCR) developed by Fondazione Bruno Kessler (FBK). First measurement results are presented at the symposium.

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1. Introduction

ANDESPix is a digital silicon photomultiplier (SiPM) [1] Application Specific Integrated Circuit (ASIC) which has been specifically designed to detect the photons produced by scintillation and wavelength-shifting (WLS) fibers commonly used in muon detectors [2]. The future ANDES Laboratory [3] will host the next generation of muon detectors that, in turn, will take advantage of the new ASIC. The goal of the ANDESPix is to improve the detector by taking advantage of the better SiPM time resolution and thus calculate the position of impinging muons by measuring the time of arrival (ToA) of each single photon individually.

2. Muon Detector

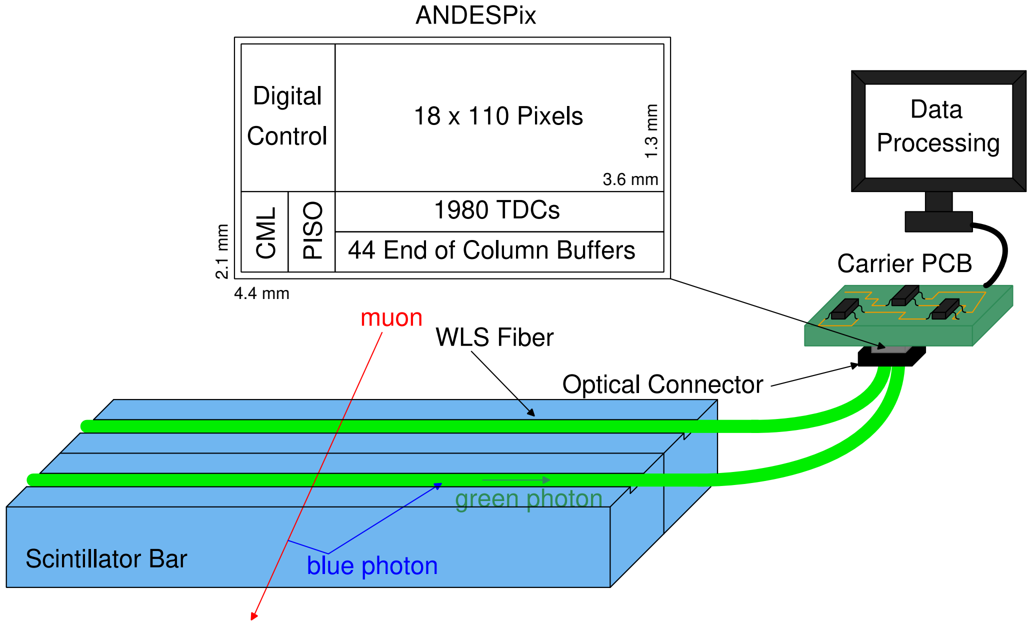

Figure 1: Overview of detector system architecture (not to scale), ANDESPix and principle of muon detection.

The working principle of the muon detector is as follows: An impinging muon generates blue photons (410 nm) in a scintillator bar. These photons are absorbed and re-emitted as green photons at 485 nm by the 1.2 mm diameter WLS fiber which is glued into a trench in the scintillator bar. [4]. A bundle of WLS fibers from several scintilator bars is assembled in an optical connector. The fibers are then coupled to a carrier printed circuit board (PCB) hosting the ANDESPix via the optical connector.

ANDESPix will be connected to the end of two WLS fibers. It should detect the individual times of arrival of the less than 50 photons that arrive per impining muon. The precise amount and timing of the photons depend on the location and path of the incoming muon [2]. The data generated by the detected photons is sent via current mode logic (CML) to a Field Programmable Gate Array (FPGA) for further processing. An overview of the system is shown in figure 1.

Compared to the currently used architecture with analog SiPMs, as e.g. in AMIGA [5], no sophisticated front-end electronics are required on the carrier PCB or detector module.
Additionally, due to the possibility of the ANDESPix to host two fibers, a future detector option with both ends of one fiber connected to ANDESPix is possible for time of flight (ToF) measurements inside the fiber.

3. ANDESPix

ANDESPix was designed in 110 nm CMOS technology from LFoundry (LF11IS) and it includes SPAD cells with high photon detection efficiency (PDE) and low dark count rate (DCR) developed by Fondazione Bruno Kessler (FBK) as an intellectual property (IP) core [6].

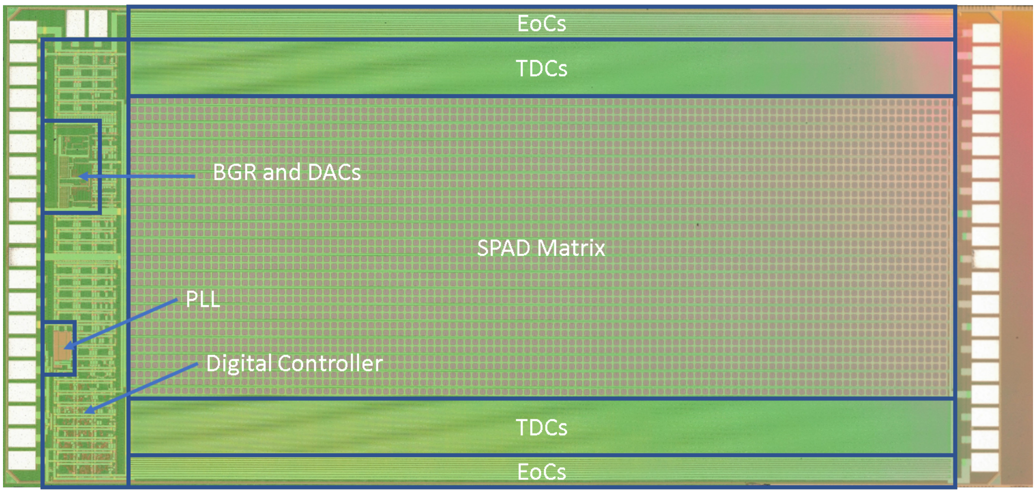

Figure 2: Image of ANDESPix.

ANDESPix, whose image is shown in figure 2, contains a pixel matrix with 1980 pixels. Each pixel hosts two SPADs together with front-end electronics. These SPADs can be enabled individually. Every pixel is connected to its own time-to-digital converter (TDC). The periphery contains a digital controller which manages the readout. Data readout is done with zero suppression, meaning that only pixels registering a photon, called a *hit*, are read out. There is a specific logic in the TDC matrix to select the pixels that have been hit. The TDC data of the selected pixel is first read in an end-of-column buffer (EoC). Then the EoC data is loaded in a parallel-in-serial-out shift register (PISO) and sent via CML to an external data processing unit. This buffered two-bus system ensures fast and secure readout. Using a simple PISO as serializer has the advantage that data could also be only sent partly to speed up readout if e.g. very precise timing is not required. Therefore, each pixel data has a specific ordering. First comes the pixel address (position), followed by a coarse and fine timestamp.
ANDESPix also has a phase-locked loop (PLL) for clock multiplication. Furthermore, there are a bandgap voltage reference (BGR) and two digital-to-analog converters (DAC) to control SPAD biasing.
The total area of the ANDESPix die is 4.4 mm times 2.1 mm and the SPAD matrix (active area)

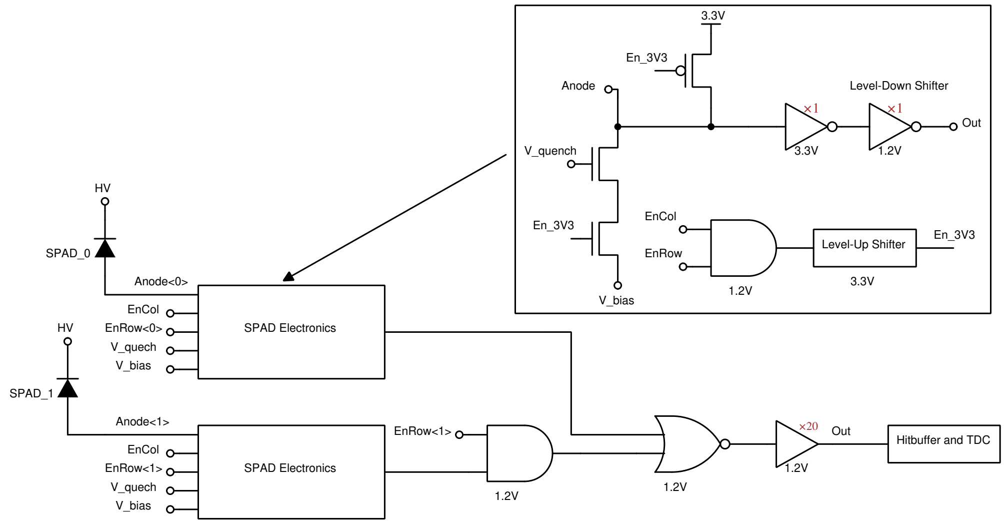

Figure 3: Schematic of the electronics of one pixel.

is 3.6 mm times 1.3 mm. The relatively small periphery area enables a matching assembly of ANDESPix dies on the standard AMIGA optical connector.

4. Pixel Electronics

As seen in figure 3, each pixel hosts two SPADs. The anode of each SPAD is connected to its queching transistor and two transitors to disable/enable it. The SPADs are enabled via a column and row enable signal which is then up-level shifted to drive the enabling transistors. The anode output signal is sent to an inverter acting as a discriminator. Then it is level shifted down from 3.3 V voltage domain to 1.2 V voltage domain in which the standard chip logic works. If only SPAD 0 is enabled, this inverter signal is directly sent to the TDC via a buffer. When the second SPAD (SPAD 1) is also activated, the signal sent to the TDC is the resulting OR of both SPADs. This architecture of combining two SPADs was necessary to meet the required area constraints by the optical connector. Therefore the two SPADs act as just one for the photon detection. However, instead of directly connecting the anodes, the OR of two individual quenching electronics has the advantage that the detector capacitance of both SPADs is lower and consequently the time resolution is higher. A simulated SPAD anode signal and its digital output signal can be seen in figure 4.

The voltage V_quench is the gate voltage of the quenching transistor. V_bias is the bias voltage of the anode. These two voltages are set globally by DAC0 (V_bias) and DAC1 (V_quench). V_bias determines the baseline of the anode voltage in reference to the inverter threshold which is roughly at 1.6 V. The difference between V_quench and V_bias determines the operation mode and resistance of the quenching transistor. As a rule of thumb, the higher this voltage, the faster the anode signal is quenched. Different ANDESPix dies are expected to have varying SPAD parameters due to fluctuating production parameters, the so-called process corners. Therefore, the described bias control seems to be necessary to enhance performance when several ANDESPix sensors are assembled in a matrix.

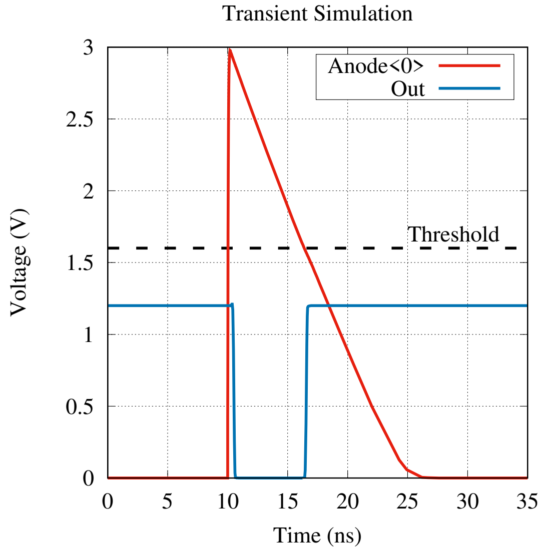

Figure 4: Simulated anode signal and pixel output signal waveforms.

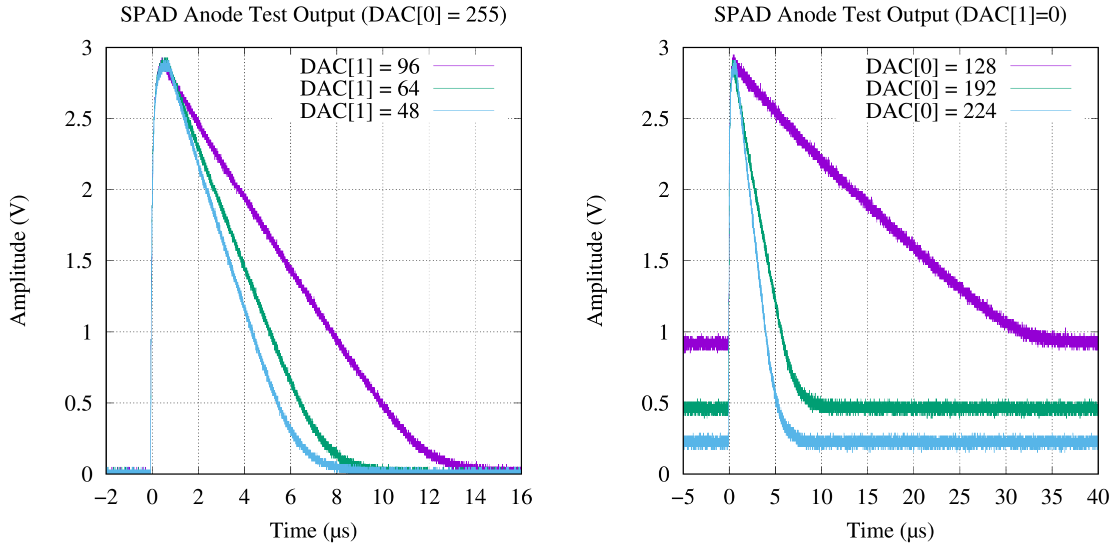

Figure 5: Sweep of DAC1 (left) and sweep of DAC0 (right).

5. First Measurement Results

As a first measurement, a unbuffered test output connected to the anode of one SPAD was characterized. A coaxial cable connected the SPAD to an oscilloscope via SMA connectors and, as a consequence, the SPAD anode was additionally loaded with approximately 100 pF capacitance. So, the signal slopes are significantly slower than inside an unloaded pixel which has a capacitance of the order of 100 fF. The cathode voltage was set to achieve an overvoltage of roughly 3 V. In figure 5 on the left is a measurement for different settings of DAC1. Different recovery times can be observed. This time is significant for afterpulsing behavior and power consumption. As can be

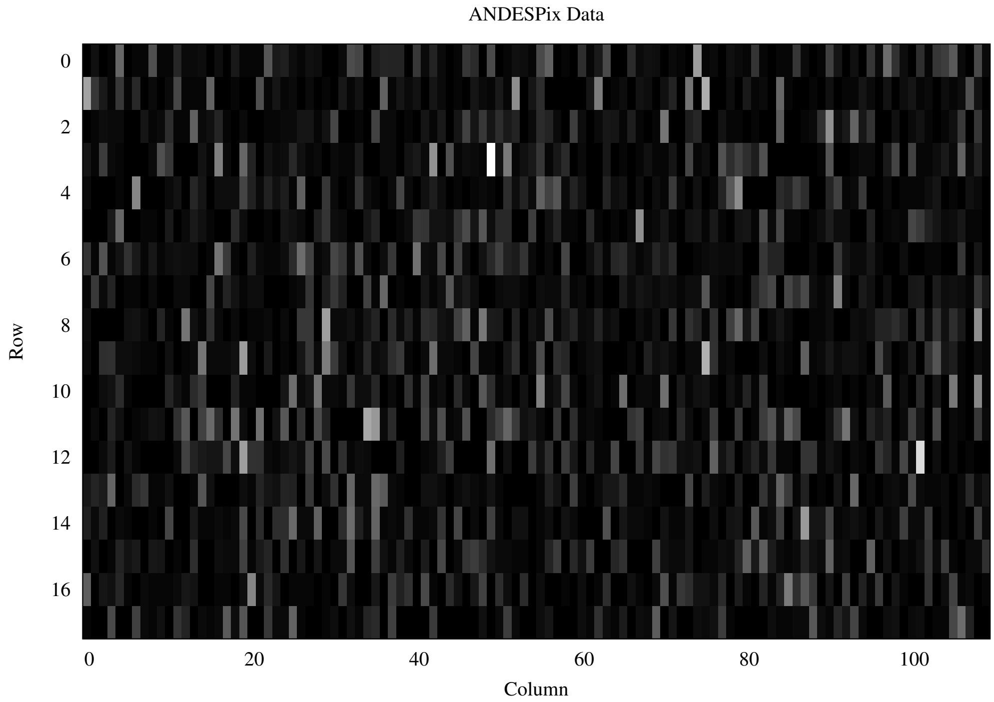

Figure 6: Relative Dark Count Rate (DCR) for each pixel. White = highest, black = lowest.

observed in the plot on the right of figure 5, the baseline of the SPAD anode signal can be manipulated by DAC0. DAC1 is kept at a fixed value. The recovery time also changes because the bias voltage of the quenching transistor is referenced to the baseline. A more detailed characterization of the DACs and anode signal is scheduled.

The dark count rate (DCR) for each pixel was also characterized at room temperature. Therefore, each pixel was enabled individually and readout for a specific time (50 ms). Performing this slow scan of ANDESPix allows the strict concentration on the dark count rate because cross-talk is not present. Afterpulsing is also not measured because the time between two pixel readouts is high and internal afterpulsing counter data was ignored. Figure 6 shows the measured relative DCR. The brightest pixels have the highest DCR. There is a significant difference in DCR between different pixels. Disabling the most noisy pixels significantly reduces the overall DCR and, therefore, it reduces the data rate and increase the sensitivity to photon pulses. The consequently slightly reduced active area seems to be acceptable. Further DCR measurements at different overvoltages, DAC settings and temperatures are planned.

6. Summary

ANDESPix is a digital SiPM specifically designed to readout scintillating fibers with low light intensity. The aim is to better understand the nature of the photon pulses it receives and thus to acquire more information about the particle generating these pulses. Furthermore, it will give us more insight on the behavior of individual SPADs than an analog SiPM as, for example, different DCRs of individual SPADs can be measured. We are able to detect and disable the noisy SPADs

while in an analog SiPM those always contribute to the output signal, putting the threshold for a detection of a real particle to a higher value of photon electrons.
Additionally, measurement proved that it is possible to manipulate the bias of the SPADs of one die while supplying one static cathode voltage. This allows us to keep SPAD operation stable against production and temperature changes.
The characterization of ANDESPix is continuing, with a special focus on the TDC characteristics and timing behavior. However, more DCR measurements are also important. Last but not least, integration of ANDESPix in the muon detector is ongoing and muon detection results are expected soon.

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