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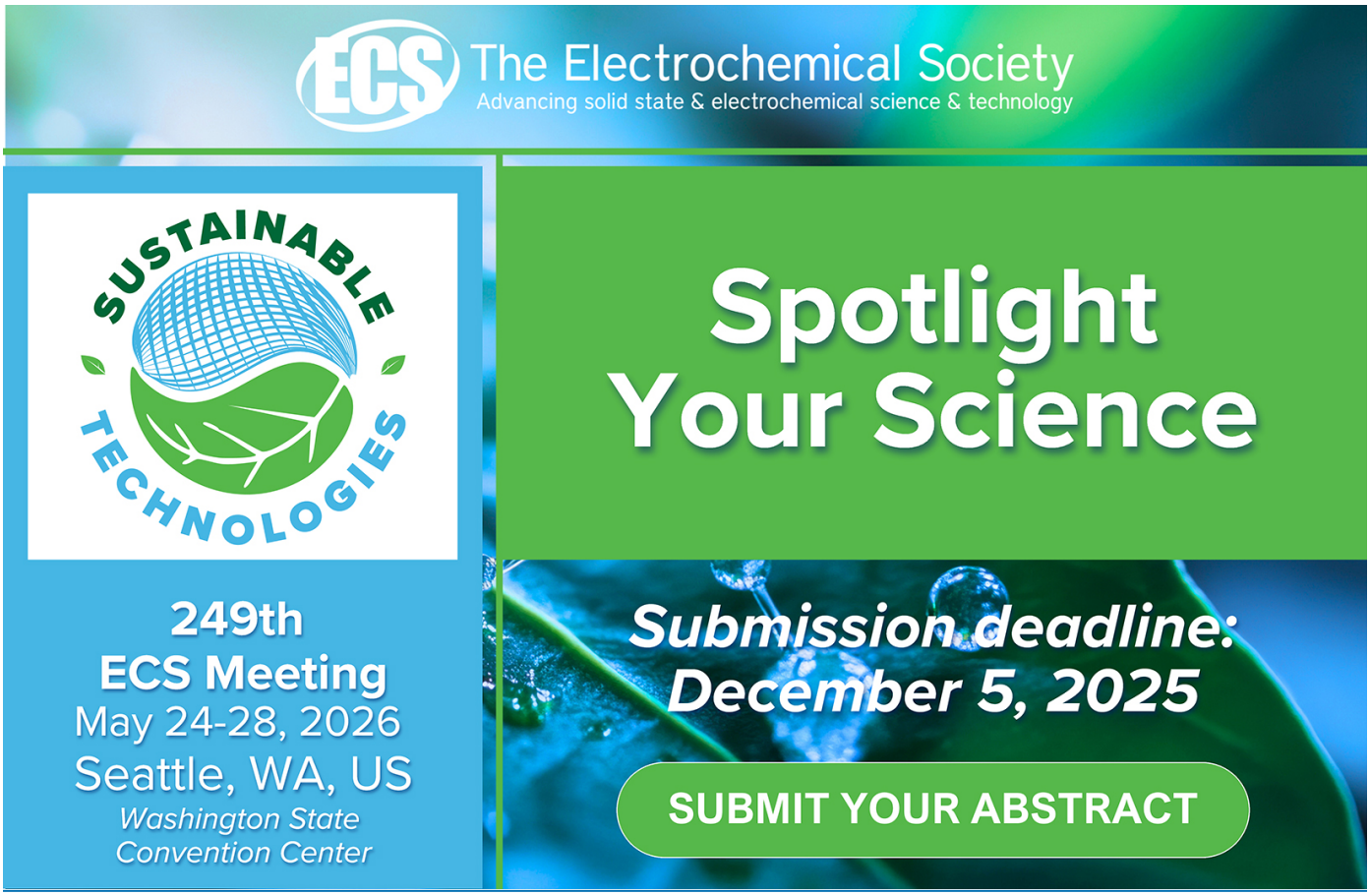

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ATLASPix3 serial powering and multi-chip module studies for future HV-CMOS tracker

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Abstract: High voltage CMOS pixel sensors are proposed in many future particle physics experiments such as the HL-LHC upgrades and future circular colliders. The ATLASPix3 chip consists of 49104 pixels of dimension 50 µm × 150 µm, realised in 180 nm HVCMOS technology. It is the first full reticle size monolithic HVCMOS sensor suitable for construction of multi-chip modules and supporting serial powering through Shunt-Low-Dropout regulators. The readout architecture supports both triggered and triggerless readout with zero-suppression. With the ability to be operated in a multi-chip setting, a 4-layer telescope made with ATLASPix3 was developed, using a readout system made at KIT. To demonstrate the multi-chip capability and for its characterisation, a beam test was conducted at DESY using 3–6 GeV positron beams with the chips operated in triggerless readout mode with zero-suppression. Detailed electrical characterisations of the regulators are presented as well as multi-chip (quad module) readout and serial powering prototyping.

Keywords: Particle tracking detectors (Solid-state detectors); Timing detectors; Trigger detectors; Accelerator Applications

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Contents

1 Introduction

Layouts for future detectors, such as the IDEA detector for the Future Circular Collider [1], require a large tracking area of approximately 100 m^2. The need for mass production to cover this large tracking area makes monolithic sensors specifically suitable. Producing readout electronics and the sensor itself in one go effectively reduces the necessary production steps from three (sensor production, readout production and bonding them together) to just one. The ability to use established, industrial processes for CMOS chips further reduces production cost and time.

ATLASPix3 is a **D**epleted **M**onolithic **A**ctive **P**ixel **S**ensor (DMAPS) built using High Voltage CMOS technology and the established *TSI Semiconductors* 180 nm process. It was produced using a substrate resistivity of approximately 200 Ωcm and features a breakdown voltage of 65 V before irradiation. The chip has a full reticle size of 2.2 cm × 2.0 cm, containing a matrix of 132 × 372 pixels with pixel dimensions of 50 µm × 150 µm (for more chip parameters, see [3]). Each pixel is equipped with individual amplifiers, comparators and threshold tuning circuits, enabling threshold tuning to 80e with a dispersion of approximately 60e and a noise level of about 70e. This low noise is partly achieved by separating digital and analog signals in the peripheral region. ATLASPix3 supports both triggerless and triggered readout modes, with data rates of up to 1.28 Gbit/s (with 64b/66b encoding) for triggered output and 1.6 Gbit/s (with 8b/10b encoding) for untriggered output. It was designed for 25 ns time stamping, enabling a telescope setup to achieve up to 4 ns (corrected) timing resolution. The chip is equipped with Shunt-Low-Dropout (Shunt-LDO or just SLDO) regulators for serial powering and has a typical power consumption of 140 mW/cm^2. ATLASPix3 serves as baseline for planning the outer barrel and disks of the IDEA detector. A power consumption of 100 mW/cm^2[4] is assumed for these layers, which is the order of magnitude ATLASPix3 has already proven as feasible.

2 Serial powering

The SLDO regulators inside the ATLASPix3 chip (figure 1) can supply VDDD and VDDA. They are each made up of a shunt regulator and a linear (low-dropout) regulator, which can be tuned separately, with 3 tuning bits each. The shunt regulates the current that flows into the chip, excess current is

"shunted", as shown in the left graph of figure 2. The voltage applied to the chip is controlled by the linear regulator, as shown in the right graph of figure 2. This configuration enables constant current operation, simplifying the power supply by reducing the number of power lines and minimizing current along power lines. Lower current also reduces magnetic fields and voltage drop along the power lines.

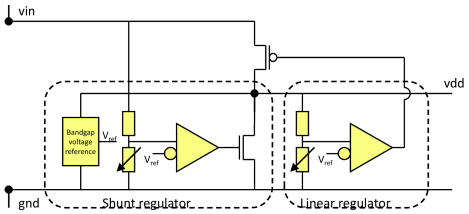

Figure 1. SLDO regulator circuit.

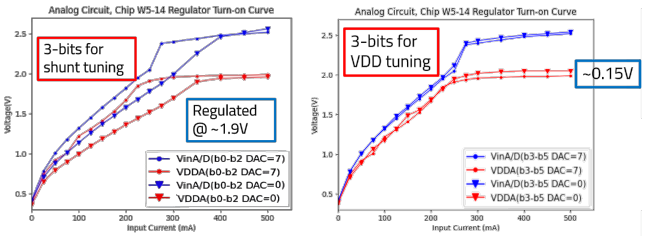

Figure 2. Shunt and VDD tuning [5, Legend upscaled]. Reproduced with permission from [5].

The current threshold can be tuned within approximately 50 mA. Once this threshold is reached, ohmic behavior is observed (see figure 3), the voltage seen by the chip stays constant. This is the case for both parallel and serial powering, showing that both are working as intended. The only major difference in figure 3 is the expected double/half value of current and voltage when comparing serial and parallel powering. Input-referred noise and threshold measurements indicate no performance degradation for serial powering and minor degradation for parallel powering [6].

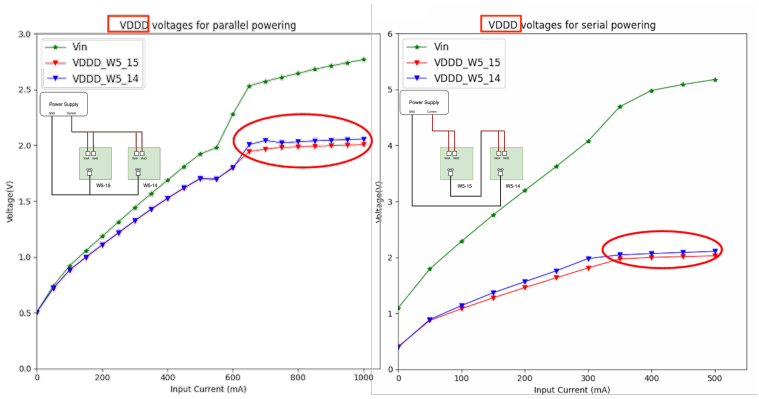

Figure 3. VDDD for parallel and serial powering. Reproduced with permission from [6].

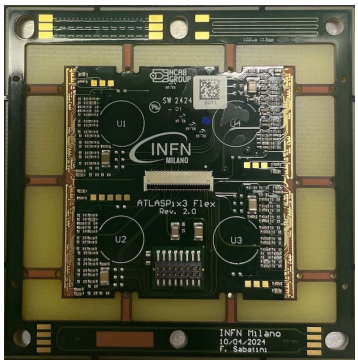

Figure 4. Quad module flex suitable for serial powering. Reproduced with permission from [7].

Figure 4 shows a flex PCB for a quad module. Quad modules inspired by the ATLAS ITk pixel [9], consist of four individual segments sharing data and bias connections. This design covers a larger area with less material compared to single modules, which is especially beneficial in dense tracking areas. Testing of a serial powering chain using quad modules and a stave electrical bus flex (see [10]) is planned, combining the mentioned advantages of serial powering and quad modules, in line with plans for the FCC vertex layers [4]. Using this aluminum bus flex reduces power dissipation along distribution lines, minimizes the number of connections and allows for significant material savings.

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3 Telescope cluster resolution

Two ATLASPix3 telescopes, each with four sensor layers as shown in figure 5, were tested at DESY with 3–6 GeV electron beams. One telescope layer was used as device under test (DUT), to be compared with the reconstructed track from the other layers. Tracks were selected with χ^2/ndof < 5 (Chi-squared divided by the number of degrees of freedom, used to exclude noise hits), and clusters were associated if they were within 0.6 mm of track intersections. Crosstalk, attributed to capacitive coupling, was limited to approximately 1% of hits. These hits can be identified by their Time-over-Threshold (ToT) staying below 20 timestamps. ToT, measured in timestamps (TS), is the time a pixel stays above the detection threshold for one event. This time increases with the deposited charge, generally indicating higher-energy particles with higher ToT. As the real clusters leading up to the main peaks in figure 6 start at approximately 50 timestamps ToT, all crosstalk hits can be safely removed when processing the data. Increasing the bias voltage (abbreviated HV for high voltage) applied to the depleted zone increases its size and consequently the charge deposited inside it. Accordingly, ToT increases with HV (figure 6), accompanied by a moderate increase in cluster size.

The telescope resolution σ_{tel} has upper bounds of 11.4 µm for one-pixel clusters and 12.5 µm for two-pixel clusters (see [7] for measurement graphs and calculations). Both of these values are lower (better) than the binary resolution $\left(\frac{\text{pitch}}{\sqrt{12}} = \frac{50\ \mu\text{m}}{\sqrt{12}} \approx 14\ \mu\text{m}\right)$, in line with simulations suggesting higher achievable resolutions (see [12]). Increasing HV also results in better resolution.

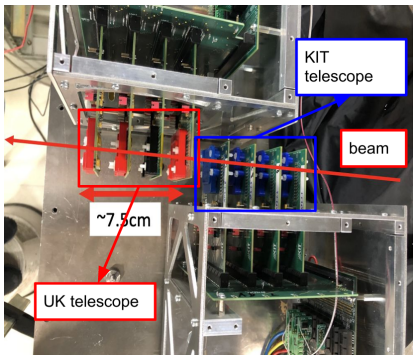

Figure 5. DESY telescope setup. Reproduced with permission from [7].

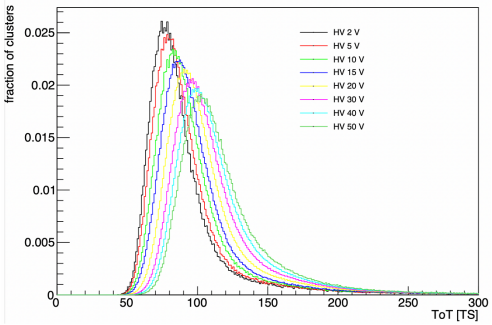

Figure 6. Clusters against ToT for different HVs, crosstalk peaks removed. Reproduced with permission from [7].

4 Pixel efficiency

Using the setup in figure 5 at DESY, Pixel efficiency was calculated by dividing clusters measured with the DUT by track intersections from the other layers.

The average pixel efficiency exceeds 99% above 20 V, resulting in a wide operational range of 45 V (20 V to 65 V) for the bias voltage. Figure 7 shows that most of the unregistered hits at lower bias voltages occur in inter-pixel regions. Particles passing through these regions share their deposited charge between two or more pixels. At lower voltages, the fraction received by each pixel may not be enough to reach the threshold. At 5 V bias voltage, edges between two pixels and especially corners between four pixels can dip as low as 75% efficiency. At 30 V bias voltage, this problem is mostly already solved, with all pixels staying above 99% efficiency. At 50 V bias voltage, even the variation of around 1% that is visible in the 30 V efficiency map is gone, all pixels perform roughly the same.

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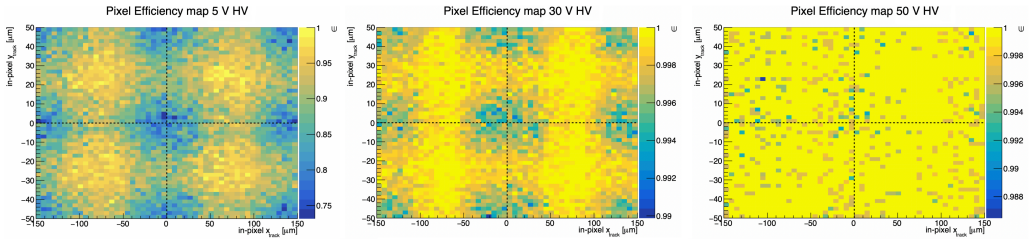

Figure 7. Percentage of particles detected at measured in-pixel positions for different bias voltages. Note the color gradient changing between the three graphs! Reproduced with permission from [6].

5 Compact Telescope Board

The previous ATLASPix3 telescope was built using the KIT GECCO system (see [14] and [15]), a multi-purpose board fit for many different sensor chips. A telescope board for four sensor PCBs was inserted in the GECCO's PCI-E slot. This telescope could take full advantage of existing designs that had already proven reliable, the GECCO system and the ATLASPix3 single carrier PCBs, which can also be used without a telescope board. However, this resulted in one disadvantage: Multiple connections and long traces from the Artix-7 FPGA PCB to the ATLASPix3 chip itself limited the clock speed to 200 MHz, reducing the data rate to 400 Mbit/s instead of the design value and full potential of 1.2 Gbit/s. To utilize the full clock speed, the Compact Telescope Board has been designed and produced, combining the GECCO system and previous telescope board into a single PCB with shorter trace lengths. Modifications of firmware and software for this new board will be done in 2025, including test measurements to investigate achievable clock speeds.

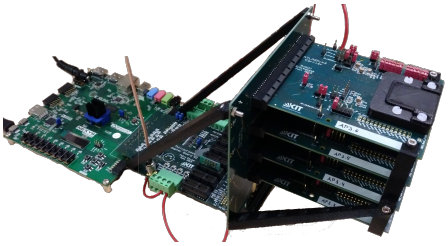

Figure 8. Previous telescope setup. Reproduced with permission from [13].

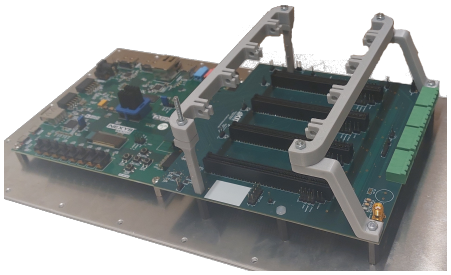

Figure 9. New telescope setup.

6 Conclusion

To summarize, quad modules using ATLASPix3 have been assembled and tested, marking a significant step toward large-area applications. In 2024, a new quad module suitable for material-efficient serial powering has been produced. The Shunt-LDO regulators, which are necessary for serial powering, have been validated in single- and double-chip setups. Additionally, a Compact Telescope Board, integrating GECCO and the previous telescope board has been manufactured. ATLASPix3 has demonstrated high efficiency and better than binary resolution in multi-chip systems, with no performance degradation observed in quad modules. Future work includes prototyping mechanics and cooling systems, testing

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the Compact Telescope Board at higher clock speeds, and assembling several quad modules. Of these, two to three modules will be integrated into a serial-powered chain on an aluminum power bus flex. Two modules with one and two wirebonded chips have already been tested and verified, including powering both modules in series [16]. Efforts will also be made to secure funding for sensor improvements through smaller-scale multi-project wafers (MPWs), since some earlier results indicate potential to significantly reduce power consumption (informal inputs from I. Peric based on [17]).

Acknowledgments

The measurements leading to the results in section 3 and 4 have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF). For more information on DESY see [11]

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