Solar RRL

WILEY VCH

Solar RRL

RESEARCH ARTICLE OPEN ACCESS

Optimization of Photolithographic Fabrication of Photonic Crystals and their Use in High Efficiency Solar Cells

Leon Salomon[1,2] | Michael Rienäcker[3] | Yevgeniya Larionova[3] | Alexej Haller[1] | Sarah Spätlich[3] | Robby Peibst[1,3] | Jan Krügener[1,4]

[1]Institute of Electronic Materials and Devices, Leibniz Universität Hannover, Hannover, Germany | [2]Light Technology Institute, Karlsruhe Institute of Technology, Karlsruhe, Germany | [3]Institute for Solar Energy Research Hamelin, Emmerthal, Germany | [4]Laboratory of Nano and Quantum Engineering, Leibniz University Hannover, Hannover, Germany

Correspondence: Jan Krügener (kruegener@mbe.uni-hannover.de)

Received: 25 June 2025 | **Revised:** 9 September 2025 | **Accepted:** 22 September 2025

Funding: German Ministry for Economic Affairs and Energy, Grant/Award Number: FKZ 003EE1056A; federal state of Lower Saxony; European Union's Horizon Europe research and innovation program, Grant/Award Number: 101146684

Keywords: inverted pyramids | interdigitated back contact solar cells | photolithography | photonic crystals

ABSTRACT

In this work we present an optimized process for the photolithographic fabrication of inverted pyramid photonic crystals (PC) with 3.1 µm periodicity on Si(001)-substrates to improve the light trapping in single junction solar cells. Anisotropic alkaline etch was used to form the pyramids with (111)-sidewalls using partial surface masking with lithographically structured SiO_2. Ridge widths between the pyramids down to (150 ± 50) nm were achieved, while ensuring a yield of multiple $(2 \times 2)\,cm^2$ areas per wafer sample. After deposition of an antireflection stack consisting of AlO_x, SiN_y, and SiO_z with different thickness optimizations a weighted reflection approaching that of a random pyramid reference sample could be shown. We demonstrate a path length enhancement of 25 at a wavelength of 1200 nm for our cell with PCs. This is *en par* with but not superior to the respective value for the reference sample with random pyramids, and still below the Lambertian limit. Furthermore, we present the first POLO^2-IBC (interdigitated back contact) solar cells with such photonic crystals on the front sides. These solar cells feature a power conversion efficiency of 22.9%.

1 | Introduction

For approaching the ultimate single junction efficiency limit of silicon, an optimization of the wafer thickness is essential due to counteracting effects: intrinsic recombination losses can be reduced by decreasing wafer thickness, but this comes at the cost of reduced light absorption in the substrates. Especially light with longer wavelengths is hardly absorbed by thin silicon substrates. Several concepts have been applied to increase light trapping in thin film solar cells toward the Lambertian limit, as described by Yablonovic [1]. Investigated concepts are optimized random pyramids (RP), gratings, or nonperiodic nanostructures. A comprehensive review article about light trapping in silicon thin film solar cells can be found in Ref. [2]. However, the fundamental limitation of photogeneration in a thin, weakly absorbing slab of silicon cannot be overcome this way.

Recently Bhattacharya and John presented a novel approach using regular inverted pyramids (IP) as photonic crystals (PC), which even increase the absorption (compared to Lambertian light trapping) of light in silicon with only a few tens of micrometers [3]. The solution of Maxwell's equations in combination with numerical device simulations showed that photonic crystals hold the potential to improve absorption of near infrared light in silicon by manipulating propagation and thus exceed the traditional Lambertian light trapping, enabling a theoretical efficiency limit well above 30% [4, 5]. The difference between the IP Bhattacharya and John proposed and the well-known inverted

pyramids, e.g. in [6], is their much smaller structure pitch. Whereas "classically" IPs with edge lengths around 10 µm are used, Bhattacharya and John proposed using much smaller edge lengths in the range of 1.3 and 3.1 µm. For these small IPs, with zero ridges between pyramids and an idealized antireflection stack, the authors simulated photocurrent densities above 44 mA/cm^2 for silicon thicknesses of 20 µm and below [7].

Assessing the calculated photocurrent densities from Bhattacharya and John, we previously calculated the maximum achievable silicon single junction solar cell efficiency to 31.6% using a 15 µm thin silicon substrate, assuming only intrinsic recombination [5]. This efficiency is an upper limit similar to the efficiency limit of 29.56% for an ideal 98.1 µm-thick solar cell with Lambertian light trapping [8]. However, Peibst et al. presented a simulated path toward fabricating solar cells with an efficiency above 28% featuring improved light trapping as reported by Bhattacharya and John and reasonable device properties [9].

Beyond a potential efficiency improvement, silicon solar cells based ultrathin wafers but still highly efficient are attractive in terms of a significant reduction of the required energy for wafer production and the related CO_2 emissions, as well as for special applications that benefit from the increased flexibility of the substrates. Indeed, numerous recent works deal with the development of highly efficient solar cells on ≈50–60 µm thin substrates featuring random pyramids as light trapping scheme [10–12]. Typically, double-sided contacted solar cells with passivating a-Si:H/c-Si heterojunction contacts are used, reflecting the utmost importance of excellent surface passivation for very thin substrates [10, 11].

Even though the above-mentioned simulations predict that regular IPs should exhibit increased absorption in the infrared spectral range, this topic is not without controversy [13, 14]. Experimental proof of increased absorption could help to resolve this controversy. Experimentally, several approaches for the fabrication of similar structures as reported by Bhattacharya and John were demonstrated featuring, i.e. deep UV stepper lithography [15]. Although first experimental results already show an improved absorption using photonics crystals on 10 µm thin silicon substrates [16], a proof that the observed increase in absorption can be used to increase photocurrent density in solar cells is still missing.

In this work we optimized a process using conventional i-line contact photolithography with respect to yield and antireflection of the textured structures. This process also works on surfaces with a certain roughness [5] and could thus serve as a reference for future industrial approaches on solar-grade silicon wafers.

We demonstrate the first interdigitated back-contact solar cell with passivating poly-Si-on-oxide (POLO) contacts featuring regular IPs acting as photonic crystals. The major aim of this work is to highlight the issues associated with the integration of these structures into a solar cell process flow. Finally, we present the results of the first solar cell featuring such structures on the front side of the cell.

2 | Status Quo before Optimization and Sample Preparation

The process flow in our work closely resembles the one shown in Figure 2 with anisotropic alkaline etching of IPs with (111)-sidewalls below a lithographically structured SiO_2 layer. The samples used are Si(001)-wafers with shiny-etched surfaces, which exhibit a certain roughness, and feature a thickness of 300 µm. Although the mentioned process flow allows the preparation of regular IPs, these regions still need to be optimized. First, planar ridges remain between the IPs (see scanning electron microscopy (SEM) image in Figure 1a), which lead to an increased reflection and thus negating any positive effect of the photonic crystals on the optics. To be optically irrelevant, these ridges need to be in the range of a few 10s of nanometers [16]. The second critical step, which needs to be optimized, is the pattern transfer from the lithographic mask initially into the hard mask (isotropic wet chemical etching) and subsequently into the silicon (anisotropic wet chemical etching). So far, high-quality structures with small ridges and without extended defects are restricted to relatively small regions of a few square centimeters across a 100 mm wafer. The attempt of large area preparation usually leads to more or less regularIPs with either large ridge widths of a few 100s of nanometers (Figure 1a) or to the occurrence of extended secondary defects like those shown in Figure 1b.

In order to address these issues and to increase the structured area, as needed for actual solar cell applications, certain

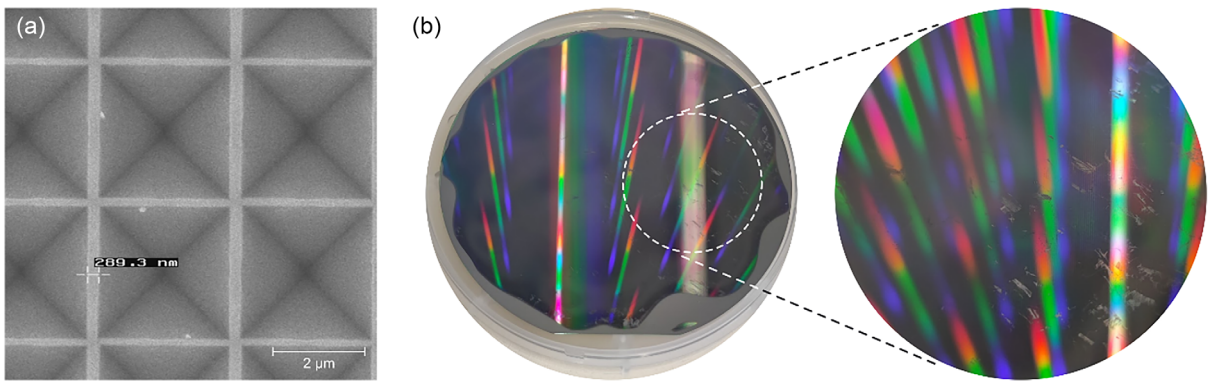

FIGURE 1 | (a) SEM image of regular inverted pyramids with remaining ridges in between. (b) Photograph of 100 mm silicon wafer with regular inverted pyramids on its front side. The color gradients across the surface are a result of the photonic crystals. The magnified region on the right-hand side reveals several extended structural defects.

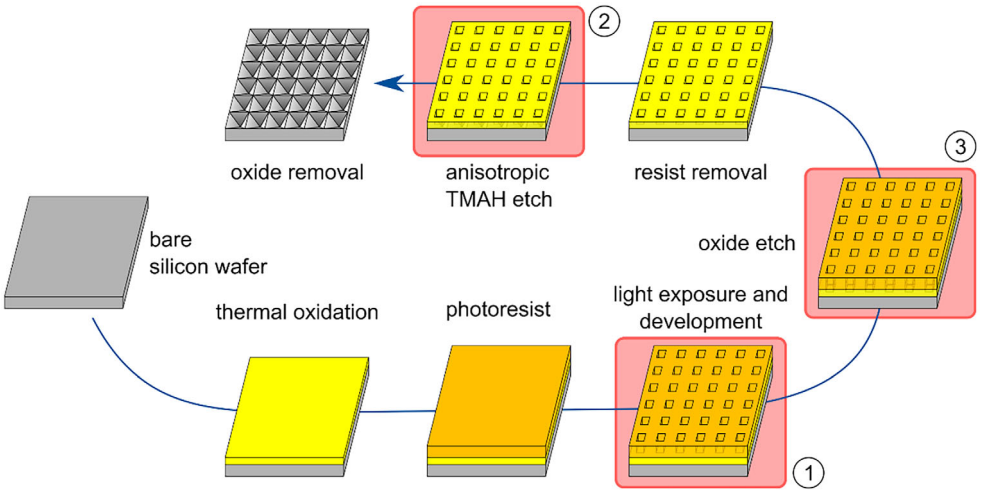

FIGURE 2 | Process flow for the preparation of inverted pyramids for use as photonic crystals in silicon [4]. The optimized process steps are highlighted in red.

optimizations of the process flow are needed. The first key optimization of the process flow aims for an improved pattern transfer from the resist into the oxide hard mask (Figure 2, step 1). Here, the photoresist developer plays a major role in achieving structural fidelity. The second optimization deals with the transfer of the pattern from the SiO_2 hard mask into the silicon surface (Figure 2, step 2). So far, tetramethylammonium hydroxide (TMAH) has been used for the anisotropic etching, resulting in a relatively poor structural yield. Substituting TMAH with potassium hydroxide (KOH) leads to a higher yield but allows no underetching of the pattern in the hard mask, thus yields wider ridges for the used size of openings in the hard mask. Therefore, the last optimization aims for a homogeneous increase of the pattern size in the hard mask (Figure 2, step 3). Here, buffered oxide etch (BOE) is used instead of diluted hydrofluoric acid (HF). The optimization of these three key processes is discussed in more detail in the next section.

Aside from the optimizations, we used the same processes as published earlier [5]. For spectrometric characterization of the prepared structures, an antireflection coating (ARC) is deposited after surface cleaning. Here, a triple-layer stack of aluminum oxide (AlO_x), silicon nitride (SiN_y), and silicon oxide (SiO_z) is used. The corresponding deposition thicknesses perpendicular to the planar surface are 20/54/120 nm for our ARC stack and 20/42/61 nm for an adapted ARC stack, respectively. The former is optimized for (111)-surfaces and thus the pyramid sidewalls. The latter is the optimum for a planar solar cell using the ray tracing tool OPAL 2 [17].

3 | Process Optimization

3.1 | Optimizing the Resist Development

The first optimization step aims for an improved transfer of the desired pattern [5] from the resist into the oxide mask. A direct use of the resist as a masking layer for the anisotropic etching step is not possible, since the resist is also etched by alkaline etchants like TMAH or KOH.

In our earlier work, we found that the development of the hole pattern was not homogeneous across a 100 mm wafer [5]. Often, a mixture of too small or too large holes was obtained. We could identify the manual handling during development as the major parameter, determining the quality of the transferred pattern. We dilute the developer solution (AZ726) with deionized (DI) water (3 parts developer, 1 part DI water) in order to reduce and homogenize the development rate. Thus, the overall process should be a little more robust against variations in handling. Furthermore, the selectivity between developed and undeveloped regions will be increased by dilution [18].

The development duration can be increased from about 20 s without dilution to 60 s with the diluted developer. The impact of the dilution on the pattern transfer can be seen in Figure 3 in worst case scenario. The aforementioned figure shows two silicon wafers after the whole processing sequence of Figure 2. Under nonideal conditions and using the initial development process with undiluted developer, a surface like shown in subfigure (a) can be observed. Only a very small region with regular IPs is visible as indicated by the rainbow-colored flares. Furthermore, using the diluted developer, still under nonideal conditions, yields much larger areas, as shown in subfigure (b). As stated above, these images only represent worst cases and both processes usually result in much larger areas with photonic crystals. Additionally, the homogeneity of the transferred hole diameters is improved. Before dilution, the mean hole diameter is around 1.4 µm, where it is around 0.9 µm (see Figure 3c) afterward as measured by atomic force microscopy (AFM). So aside from reducing the mean hole diameter, the dilution process also narrows the distribution of the hole widths across the sample area. The narrowing of the hole diameters plays a major role in being able to obtain bigger areas with regular IPs, as already hinted by Figure 3.

The optimization of the resist development leads to several other needed adjustments in the process flow. The smaller structure size of the holes obtained for the diluted developer leads to the need of longer anisotropic etching durations. As soon as the etching hits the (111) crystal planes, the etching rate

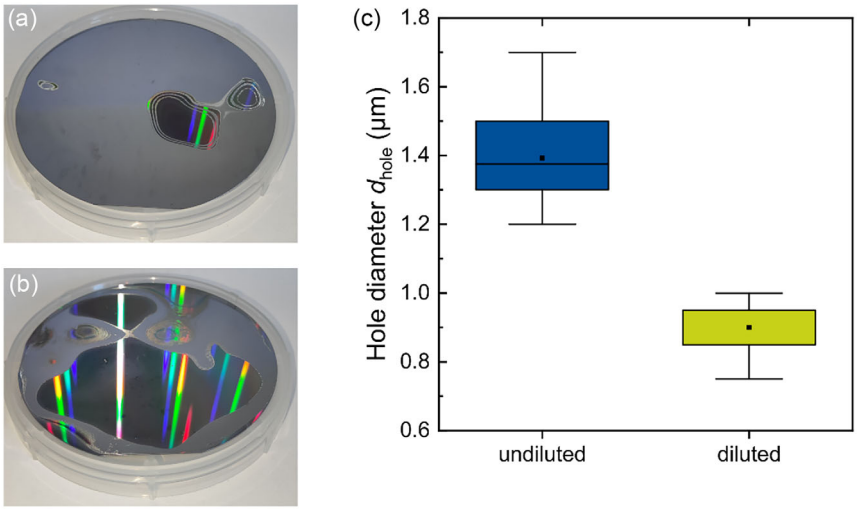

FIGURE 3 | Exemplary worst case scenario photographs of silicon wafers with inverted pyramids on their front sides. Regions with homogeneous inverted pyramids are visible by the rainbow-colored flares. (a) For undiluted developer and 20 s development. (b) For diluted developer and 60 s development. (c) Shows the change in hole diameter for using the undiluted and diluted developer.

decreases by more than 1–2 orders of magnitude [19]. The highly increased etching durations result in an increased occurrence of defects like the ones shown in Figure 1b.

3.2 | Optimizing the Pattern Transfer into the Hard Mask

In the previous section, the optimization of the resist development is presented. However, the smaller diameters of the transferred pattern result in the drawback of longeranisotropic etching. Another way to obtain larger hole diameters is using an adapted photolithographic mask which is planned for future optimization. A different possible way to overcome this problem is to adapt the etching step of the oxide layer. The controlled over-etching of the transferred pattern might allow larger hole diameters, while maintaining a high structural quality. In the original process flow, the oxide layer only needed to be a few nanometers thick. Therefore, diluted HF (1%) was used in the original process flow for structuring the silicon dioxide layer. For the used oxide and the diluted HF, an etching rate of about 6 nm/min is obtained. This etch rate is too low for a high-quality over-etching, because for longer etching durations, the masking ability of the resist vanishes and defects in the resist appear.

Therefore, we substitute the diluted HF with BOE. BOE offers much higher etching rates of about 100 nm/min compared to diluted HF [20]. This way, a significant underetching of the pattern in the resist is possible. Here, the longer the etching process takes, the smaller the mean etching rate gets due to a reduced exchange of material within the hole and the underetched regions compared to full-area etching. The etch rate reduces with increasing etching durations as a result of the aforementioned hindered material exchange. Figure 4a shows the resulting hole diameter within the oxide layer as a function of the etching duration, for an initial hole diameter of around 1.2 µm. Thus, hole diameters of about 2.7 µm are achieved which very close to the desired structure pitch (see Figure 4b). A further increase

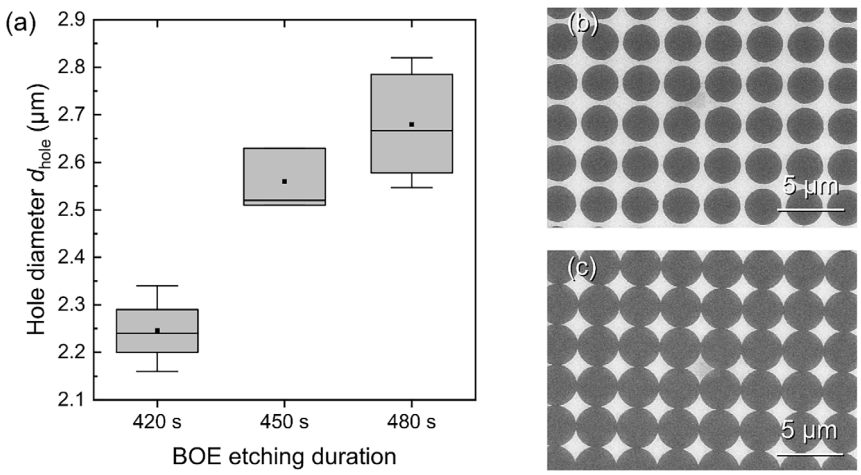

FIGURE 4 | (a) Measured hole diameter for different BOE etching durations. (b) SEM image of holes within the SiO_2 masking layer after 8 min and (c) after 10 min of BOE etching.

in etching duration leads to the formation of defects in the masking layer. Here, the holes coalesce as shown in Figure 4c. Anisotropic etching of the underlying silicon then leads to a highly irregular and defective surface.

3.3 | Optimizing the Anisotropic Etching of the Silicon Substrate

After optimizing the pattern transfer into the hard mask, we try to minimize the ridge width in between the IPs. The combination of improved resist development, together with BOE etching of the oxide, already leads to relatively large holes within the oxide mask. However, we found that a further reduction of the oxide width between the holes often leads to regions where the holes overlap. In these regions, only a defective pattern is etched into the silicon. Thus, we aim for the smallest widths of the oxide between the holes without overlaps, which can be under etched in the anisotropic etching step. In earlier studies, we used TMAH for this step, since it offers high etching rates of non (111)-oriented silicon while having a high selectivity against the oxide mask [21, 22]. However, TMAH seems to be unsuitable for longer etching durations. We observe the formation of structural defects for extensive etching with TMAH, as shown in Figure 5. In order to exclude local discontinuities in the masking layer as the reason for the defect formation during the extensive etching process, we replace the initially used 6 nm thick oxide with a 25 nm thick one. This thicker masking layer should easily withstand the etching step. Nevertheless, the same defect formation as shown in Figure 5 is observed for the thicker masking layer.

We use SEM investigations to reveal the origin of the observed defects. Figure 6 shows two different areas of the same sample after TMAH etching. The masking layer is not etched away before taking these images. For example, in Figure 6a an inverted pyramid without a defect is shown. The oxide masking layer can be recognized as a brighter contrast in the images. Thus, the initial round opening in the oxide layer right above the inverted pyramid is visible. Figure 6b shows a region with the above-mentioned defect. Here, the oxide layer is also intact (bright contrast), but no perfect inverted pyramid is formed. Such defects seem to occur predominantly at positions where the remaining ridges between the IPs are very small. It seems like the TMAH is creeping in between the oxide mask and the silicon substrate. Here, much faster etched crystal planes are etched, leading to the formation of the observed defects.

4 | Optical Sample Characterization

After optimization of the structuring process, as shown in the previous section, the most important aspects of the photonic crystals are their optical properties. The above presented process flow does not lead to perfect IPs, i.e., with ridge widths of a few 10s of nanometers [16], yet. However, we measure the reflection of two samples with ridge widths of 151 ± 49 and 195 ± 1 nm and compare the obtained results with a randomly pyramid textured sample. The former sample surface is coated with an ARC, which is optimized for a planar surface (20 nm AlO_x, 42 nm SiN_y, 61 nm SiO_z, see Figure 7b). The latter sample features an ARC which is optimized for the sidewalls of the pyramids (20 nm AlO_x, 54 nm SiN_y, 120 nm SiO_z, see Figure 7a).

The coated samples are measured with a photospectrometer on an integrating sphere to account for diffuse reflection. The results of these measurements are shown in Figure 7c. In order to compare the obtained results more easily, we perform a quantification of the reflectance in the range of 300 nm to 1100 nm using the AM1.5g irradiation

$$J_{\mathrm{ph,R}} = \int_{300\ \mathrm{nm}}^{1100\ \mathrm{nm}} \frac{e\lambda}{\mathrm{hc}} I_{\mathrm{AM1.5}}(\lambda) R(\lambda) d\lambda \tag{1}$$

The weighted reflection thus obtained is also given in Figure 7c. The lowest photocurrent loss is observed for the random pyramid textured sample ($J_{\mathrm{ph,R}} = 1.14\ \mathrm{mA/cm^2}$), what is not unexpected due to the large fraction of planar regions on the PC samples (≈9.5% and 12.5%). However, for the two samples with PCs, a clear reduction in photo current loss can be obtained when reducing the remaining ridge width from around 200 nm ($J_{\mathrm{ph,R}} = 1.60\ \mathrm{mA/cm^2}$) down to around 150 nm ($J_{\mathrm{ph,R}} = 1.30\ \mathrm{mA/cm^2}$). This difference is not only a result of the smaller areal fraction of the planar regions, but also due to the ARC, which is optimized for a planar surface. Here, the benefit of reduced reflection on the planar regions overcompensates

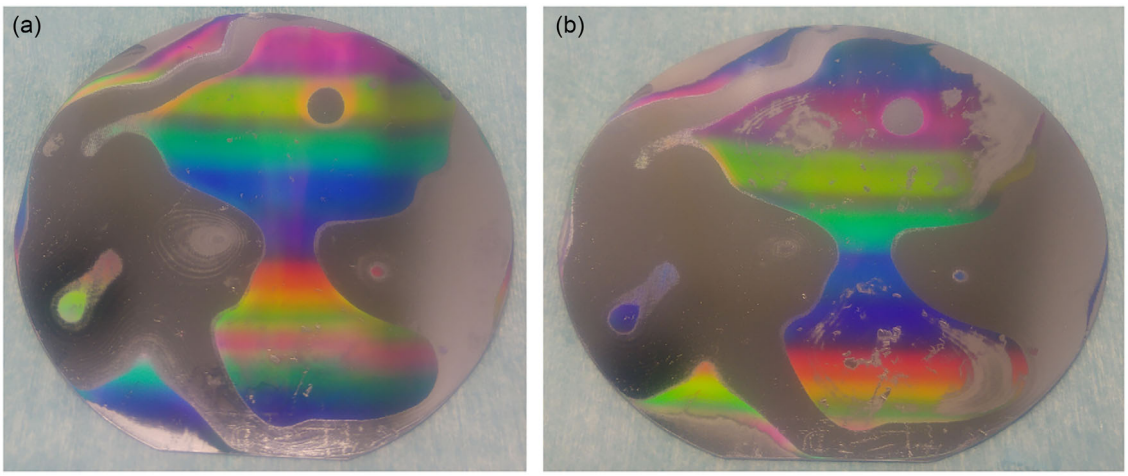

FIGURE 5 | Photographs of a TMAH-etched silicon wafer after (a) 30 min and (b) 37 min of etching.

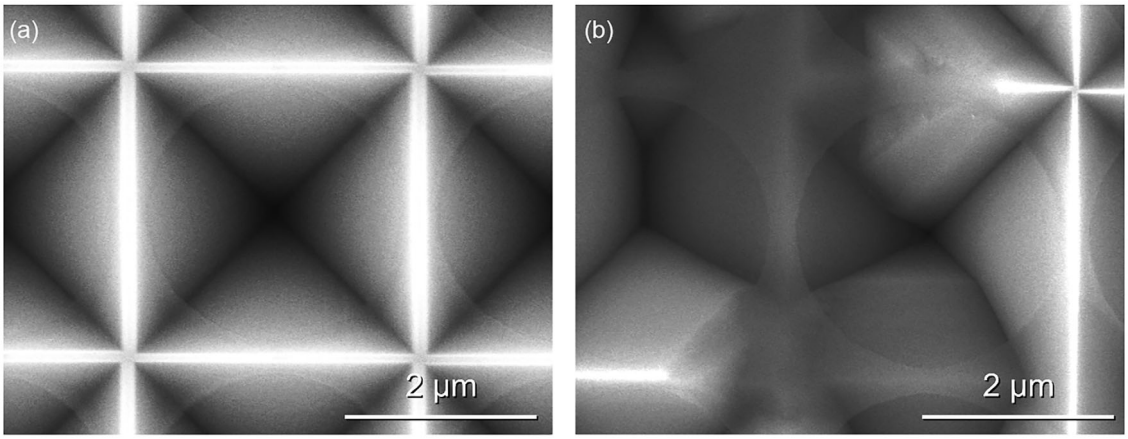

FIGURE 6 | SEM images of TMAH-etched silicon through a silicon oxide mask (a) without and (b) with defect. The round openings within the masking layer can be seen centered above the inverted pyramids.

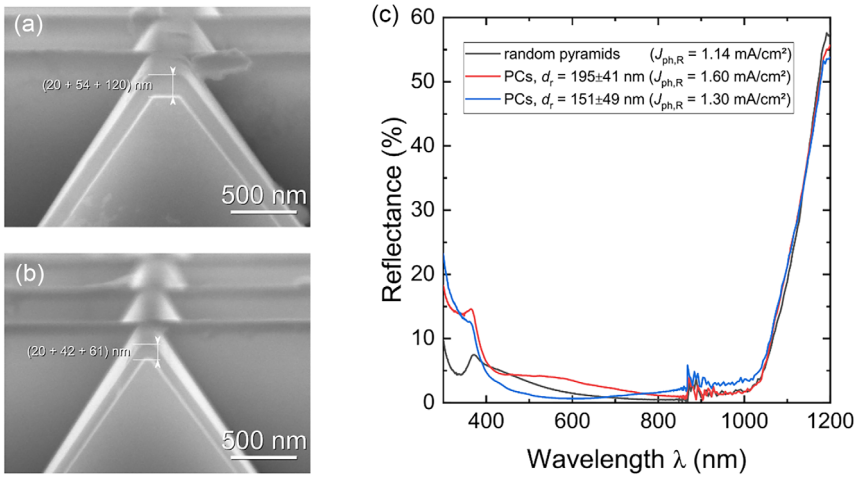

FIGURE 7 | SEM images of photonic crystals with an ARC optimized for (a) pyramid sidewalls and (b) for planar surfaces. (c) Measured spectral reflection of two different photonic crystal samples and a random pyramid textured reference sample. The sample corresponding to the blue curve features an ARC stack as shown in (a), whereas the sample corresponding to the red curve features an ARC as shown in (b).

the nonoptimized reflection behavior on the pyramid sidewalls. Nevertheless, even samples featuring relatively wide planar ridges perform almost as good as the random pyramid textured sample. A further reduction of the remaining ridge width is unavoidable for approaching and even outperforming the RP reference in terms of reflectance.

5 | Implementation of Optimized PCs on POLO^2-IBC Solar Cells

In this section, the first implementation of PCs consisting of regular IPs in POLO^2-IBC solar cells is presented. The solar cells are prepared similar to the ones presented in [23].

5.1 | Baseline Fabrication Process for POLO^2-IBC Cells with Random Pyramids

The following baseline fabrication process yields our random pyramid (RP-)POLO^2-IBC cell in Figure 8a and serves as the benchmark: We use 300-µm-thick 1.3 Ωcm, p-type FZ wafers and follow the process described elsewhere [24, 25] to form the p^+-(i)-n^+ POLO interdigitated rear side by using amorphous Si, masked ion implantation and a subsequent wet oxidation and higher temperature process at 1035°C. Since the p^+-(i)-n^+ rear side prevented us from implementing an advanced hydrogenation scheme for our POLO junctions [25], we removed the p^+-(i)-n^+ junction by KOH etching through the lithographically patterned rear SiO_2 layer. This patterning step results in a trench separation between the pPOLO und nPOLO interdigitated regions and strips the SiO_2 and n^+ poly-Si layers from the front side. The latter results in a KOH-etched rough surface at the front side.

In the next step, we strip the rear SiO_2 and create the random pyramid light trapping structure on the front side by an alkaline wet etch in a KOH-based texturing solution. We protect the rear side from texturing by a sample holder from PTFE. The front side receives a passivating antireflecting $AlO_x/SiN_y/SiO_z$ layer stack after a final RCA cleaning. We deposit a triple-layer stack of $AlO_x/SiN_y/SiO_z$ on the rear side, to passivate the trench region, to hydrogenate the POLO junctions and to facilitate the laser

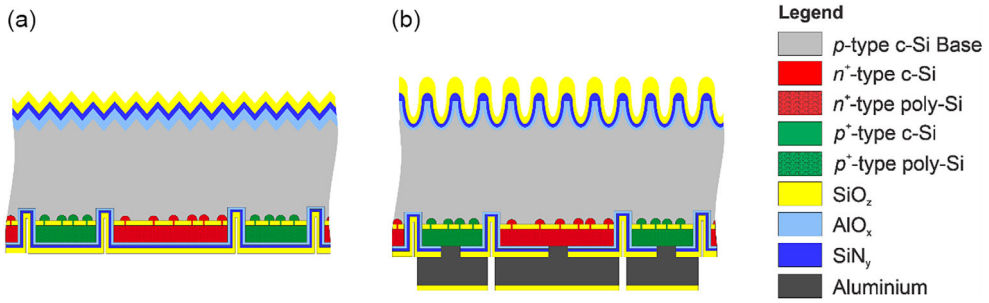

FIGURE 8 | (a) Schematic cross-section of the baseline POLO^2-IBC solar cell with random upright pyramids after front-end processing and (b) schematic cross-section of the modified POLO^2-IBC solar cell with regular inverted pyramids acting as photonic crystals after back-end processing.

contact opening process [26]. Figure 8a schematically shows the cross-section of the cell precursor in this stage, after front-end processing.

During the back-end processing, we locally laser open the rear side dielectric layers to form a contact with the evaporated Al electrode. After contact opening, we deposit a 10 µm-thick Al layer and a SiO_z layer on the rear side and perform the contact separation by locally laser ablating the SiO_z layer and etching the Al layer in the ablated region. The baseline POLO^2-IBC cell yields an efficiency of 26.02% with an open-circuit voltage V_{OC} of 730.2 mV, a short-circuit current density J_{SC} of 42.2 mA/cm^2 and a fill factor *FF* of 84.44%.

5.2 | Modification of Baseline Process for POLO^2-IBC Cells with Inverted Pyramid Photonic Crystal Structure

The fabrication of a photonic crystal structure on the KOH-etched, rough front side of the POLO^2-IBC cell precursor wafer after trench separation and removal of the poly-Si from the front side is challenging so far. Therefore, we adapt the baseline cell process, such that it leaves the chemically–mechanically polished (CMP) surface of the 280-µm-thick, 2.6 Ωcm, p-type FZ wafer intact throughout the cell process. For this purpose, we grow a protective 700-nm-thick SiO_2 layer prior to the cell process. We laser ablate it from the rear side, followed by a subsequent KOH etch to yield a 173-µm-thick wafer and perform a phosphorus diffusion gettering process afterward. All subsequent steps follow the baseline process until the trench separation and poly-Si removal from the front side are carried out. At this stage, we removed the thick protective SiO_2 layer from the polished front side of the cell precursors and fabricated the photonic crystal structure. During the structuring of the photonic crystals on the front side, the back-side is covered with photoresist to prevent any kind of handling and/or processing damage of the POLO junctions.

In Figure 9a a photograph of the front side of the whole solar cell wafer after PC formation is shown. The light reflections in this image clearly show that most of the wafer is structured in a regular manner. However, SEM investigations show that the width of the ridges in between the IPs is in the range of 600 ± 70 nm across the wafer surface. In Figure 9b a corresponding SEM image of the surface structure is shown. For an increased photocurrent density, compared to solar cells with a random pyramid texture, these ridges are too wide. This is mainly due to an increased reflection of these planar regions, even for an adapted ARC. Since the planar regions are crucial for the overall reflectance of the later solar cells, an antireflection coating which is optimized for the planar surface is applied. The ARC, which also acts as a passivation layer, consists of a triple-layer stack of AlO_x (20 nm), SiN_y (42 nm), and SiO_z (61 nm). The thicknesses are optimized using OPAL 2 [17].

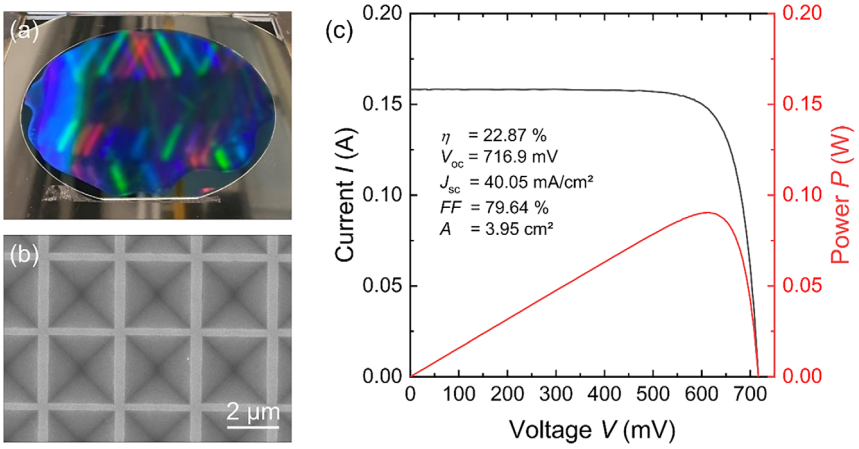

FIGURE 9 | (a) Photograph of the front side of the solar cell wafer, showing large-area photonic crystals. (b) Typical SEM image of the corresponding inverted pyramids. (c) Independently confirmed current–voltage characteristics from ISFH CalTeC of a POLO^2-IBC solar cell with regular inverted pyramids acting as photonic crystals.

Figure 9c shows the independently confirmed (ISFH CalTeC) current–voltage characteristics of the finished solar cell. The first POLO^2-IBC solar cell with photonic crystals achieves an efficiency of 22.9% with an open-circuit voltage V_{OC} of 716.9 mV, a short-circuit current density J_{SC} of 40.1 mA/cm^2 and a fill factor *FF* of 79.6%. The lower *FF* of the PC cell compared to the baseline cell reflects the nonoptimized fabrication process and the issues of the alignment during photolithographic structuring due to a rough surface at the rear side. The latter is a consequence of the KOH thinning process at the beginning of the process and can be eliminated easily by using thin polished wafers or, eventually, an industrial structuring method such a laser structuring.

The lower short-circuit current density of 40.1 mA/cm^2 compared to 42.2 mA/cm^2 for the baseline cell is a result of three mechanisms: increased front-side reflection, lower collection efficiency, and lower near infrared absorption due to the thinner wafer. However, the use of unoptimized photonic crystals does not result in improved light trapping at this stage.

Figure 10a compares the in-house measured reflection and external quantum efficiency (EQE) and the calculated internal quantum efficiency (IQE$_{LT}$) of our POLO^2-IBC cell with random pyramids and photonic crystals. The EQE was scaled by the respective independently confirmed short-circuit current density. We calculate the IQE$_{LT}$ from the scaled EQE and the extrapolated front-side reflectance R_f according to [27]:

$$\mathrm{EQE} = \mathrm{IQE}_{\mathrm{LT}} \cdot \left(1 - R_f\right) \tag{2}$$

Note that IQE$_{LT}$ differs (at least in the long-wavelength range) from the conventionally defined IQE, which is calculated from the total reflectance instead of extrapolated front-side reflectance. We neglect any parasitic absorption of the ARC, because we expect that this contribution approaches zero for wavelengths above 400 nm.

For wavelengths below 900 nm, R_f replicates the measured external reflection as shown in Figure 10a. Above 900 nm, escape reflectance starts to superpose with R_f in the measured external reflectance and prevents a direct measurement of R_f. Therefore, we extrapolate R_f with a second order polynomial fit of the measured external reflection between a wavelength of 800 nm and 900 nm as reported by Brendel et al. [28].

An analysis of the extrapolated front-side reflectance confirms an increased AM1.5g-weighted reflectance of the POLO^2 IBC solar cell with photonic crystals of 4.4% compared to 3.1% with random pyramids. From the internal quantum efficiency, we deduce the electrical collection efficiency η_c according to:

$$\mathrm{IQE}_{\mathrm{LT}}(\lambda) = \eta_c(\lambda) \cdot \left(1 - e^{-\alpha(\lambda)Z(\lambda)W}\right) \tag{3}$$

where $\alpha(\lambda)$, $Z(\lambda)$, and W are the coefficient of absorption, path length enhancement factor, and device thickness, respectively. The exponential absorption law represents the Beer–Lambert law extended by a phenomenological constant $Z(\lambda)$. While this equation is strictly valid in the ray-optical limit, its applicability to wave-optical light trapping schemes, such as those based on photonic crystals, remains theoretically uncertain. However, since the photonic crystal is designed to primarily influence light trapping in the 1000–1200 nm range, we assume that the exponential model remains a reasonable approximation at shorter wavelengths. In this study, it serves as a tool to analyze the solar cell with IPs, which are intended to act as a photonic crystal. If the model does not fully capture the absorption behavior, deviations in $Z(\lambda)$ are expected, potentially leading to values larger than those observed in the reference case with random pyramids.

Since the absorption length $1/\alpha$ of light in silicon between 600 nm and 800 nm is orders of magnitude smaller than the device thickness W, the exponential term approaches zero, the IQE$_{LT}$ is constant and reflects the collection efficiency. We find an almost constant mean collection efficiency of 96.6% (standard deviation of 0.12%) for the POLO^2 IBC solar cell with photonic crystals and 98.5% (standard deviation of 0.07%) for the baseline cell.

As pointed out by McIntosh et al. [29], we expect an even weaker dependence of η_c on λ for $\lambda > 900$ nm due to the low recombination within our POLO^2-IBC cell and the minority carrier collecting rear junction.

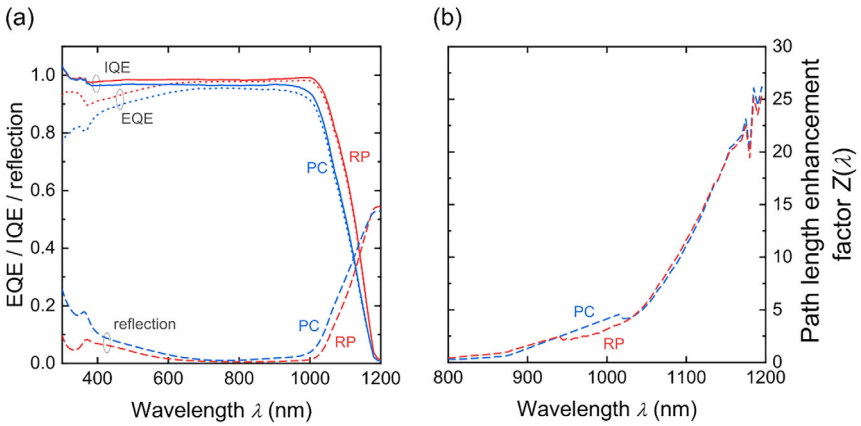

FIGURE 10 | (a) Comparison of the reflection, external and internal quantum efficiency and (b) the path length enhancement factor of the POLO^2-IBC cell with random pyramids (red) and photonic crystals (blue). All data shown is obtained from reference solar cells (see section 5.1) and from solar cells with regular inverted pyramids (this section).

Furthermore, Figure 10a reveals a lower IQE_{LT} for the PC cells compared to the RP cell for wavelengths larger than 1000 nm. The ratio of IQE_{LT} values of the PC versus RP cell equals the ratio of the η_c values of both cells of 0.98 between 600 nm and 900 nm, because the exponential term approaches zero, resulting in complete absorption of light in this strong absorption regime. However, the IQE_{LT} ratio drops linearly by about 0.002/nm between 1000 nm and 1180 nm to a value of ≈0.6. For a constant η_c, we expect a constant ratio of IQE_{LT} values and a decreasing ratio means that the PC cell utilizes less long-wavelength photons for photo generation compared to the RP cell.

According to the relation between IQE_{LT} and η_c, $\alpha(\lambda)$, $Z(\lambda)$, and W, we can expect that a combination of $Z(\lambda)$ and W causes the weaker trapping of light, since $\alpha(\lambda)$ is a material property. Here we assume that the rear sides of the cells are optically equivalent, i.e., the transparency implied by the trench region and the free-carrier absorption in the POLO junction and in the wafer are comparable for both cells. Since both cells were fabricated following the same procedures, we can assume the rear sides are similar.

We calculate the path length enhancement factor from the IQE_{LT}, η_c, and $\alpha(\lambda)$ according to the relation above for the particular thickness of 173 µm and 276 µm for the PC and RP cell, respectively. For $\alpha(\lambda)$ we use the dataset of Schinke et al. [30].

Figure 10b shows the path length enhancement factor for both cells and highlights that the light trapping capability of our PC cell is on par with the RP cell and other published results for random pyramid textures [29]. However, the RP cell absorbs long-wavelength photons more efficient by about 30% and 60% due to the thicker wafer compared to the PC cell at 1100 nm and 1200 nm, respectively.

For a solar cell with isotropic light trapping, thus the ideal Lambertian case, we anticipate a path length enhancement of about 49 at a wavelength of 1200 nm, but for both cells in this work, we observe a value of only about 25, which is partly due to the parasitic free-carrier absorption (FCA) within the wafer and the POLO junction at the rear side. McIntosh et al. have reported similar observations for a diffused junction back-contact cell and corrected the data by excluding FCA by means of a ray-tracing approach [29]. Since this work targets a light trapping scheme that is not covered by the ray optics, it is challenging to correct for free-carrier absorption without relying on a ray-optical model and thus knowing the exact paths of the light. This dilemma needs further theoretical and experimental investigations.

However, demonstrating a path length enhancement above the ideal Lambertian case is one possibility to directly prove that solar cells implementing photonic crystals can be superior in terms of trapping the light. Therefore, the presented $POLO^2$-IBC cell with photonic crystals is a first step in this direction.

6 | Conclusion

In this article, we present optimizations of three crucial processing steps of the preparation of regular inverted pyramid photonic crystals using conventional photolithography: resist development, structure transfer into the dielectric hard mask and the anisotropic etching process. With these optimized process parameters, large areas with regular IPs can be prepared, with reflection properties approaching random pyramid structured samples. For the preparation of large areas with PCs showing even better optical properties even more detailed optimizations in the process flow are needed.

Aside from the optimization of the pattern transfer, we applied regular PCs on $POLO^2$-IBC solar cells. The PCs on these solar cells are not as optimized as on the test samples, meaning too wide ridges in-between the IPs. Such solar cells feature a power conversion efficiency of 22.9%, which is predominantly limited by increased reflection but also by losses in FF and V_{oc} due to a nonoptimized process sequence. We demonstrate a path length enhancement of 25 at a wavelength of 1200 nm for our cell with PCs. This is *en par* with but not superior to the respective value for the reference sample with random pyramids, and still below the Lambertian limit.

Finally, we conclude that despite the progress we achieved in terms of preparation of the regular IPs, we do not observe the anticipated increase in absorptance in the IR region of the spectrum as observed in quantum efficiency. There are several possible explanations for this behavior. First of all, the preparation process of the solar cells presented here is still not optimized properly, e.g. mentioning the wide ridges in between the IPs. Next, an experimental prove of an increased IR absorption in an actual solar cell is still missing, although some hints exist that it actually exists, e.g. by Hsieh et al. [16]. In conclusion, an answer to the question of whether regular IPs do help increase absorption in the IR part of the incident spectrum is still open and subject to further research.

Acknowledgments

We would like to thank G. Glowatzki, R. Ziesenіß, and R. Winter for sample processing. This work is partially funded by the German Ministry for Economic Affairs and Energy (grant FKZ 003EE1056A) and the federal state of Lower Saxony. This work was partially funded by the European Union's Horizon Europe research and innovation program under grant agreement no 101146684.

Open Access funding enabled and organized by Projekt DEAL.

Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request; European Union's Horizon Europe research and innovation program under grant agreement No 101146684.

References

1. E. Yablonovitch, "Statistical Ray Optics," *Journal of the Optical Society of America* 72, no. 7 (1982): 899.

2. R. Saive, "Light Trapping in Thin Silicon Solar Cells: A Review on Fundamentals and Technologies," *Progress in Photovoltaics: Research and Applications* 29, no. 10 (2021): 1055.

3. S. Bhattacharya, I. Baydoun, M. Lin, and S. John, "Towards 30% Power Conversion Efficiency in Thin-Silicon Photonic-Crystal Solar Cells," *Physical Review Applied* 11 (2019): 014005.

4. S. Bhattacharya and S. John, "Photonic Crystal Light Trapping: Beyond 30% Conversion Efficiency for Silicon Photovoltaics," *APL Photonics* 5 (2020): 020902.

5. J. Krügener, M. Rienäcker, S. Schäfer, et al., Photonic Crystals for Highly Efficient Silicon Single Junction Solar Cells, *Solar Energy Materials and Solar Cells* 233 (2021), 111337.

6. J. Zhao, A. Wang, and M. A. Green, "24·5% Efficiency Silicon PERT Cells on MCZ Substrates and 24·7% Efficiency PERL Cells on FZ Substrates," *Progress in Photovoltaics: Research and Applications* 7, no. 6 (1999): 471.

7. S. Bhattacharya and S. John, "Beyond 30% Conversion Efficiency in Silicon Solar Cells: A Numerical Demonstration," *Scientific Reports* 9 (2019): 12482.

8. S. Schäfer and R. Brendel, "Accurate Calculation of the Absorptance Enhances Efficiency Limit of Crystalline Silicon Solar Cells With Lambertian Light Trapping," *IEEE Journal of Photovoltaics* 8 (2018): 1156.

9. R. Peibst, M. Rienäcker, Y. Larionova, et al., "Towards 28%-Efficient Si Single-Junction Solar Cells with Better Passivating POLO Junctions and Photonic Crystals," *Solar Energy Materials and Solar Cells* 238 (2022): 111560.

10. W. Liu, Y. Liu, Z. Yang, et al., "Flexible Solar Cells Based on Foldable Silicon Wafers with Blunted Edges," *Nature* 617 (2023): 717.

11. P. Balaji, W. J. Dauksher, S. G. Bowden, and A. Augusto, "*Development of 40 μm Thin Flexible Silicon Heterojunction Solar Cells*," in Proceedings of the IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC) (A Joint Conference of 45th IEEE PVSC, 28th PVSEC & 34th EU PVSEC (IEEE, 2018), 2100, https://doi.org/10.1109/PVSC.2018.8547385.

12. J. H. Petermann, D. Zielke, J. Schmidt, F. Haase, E. G. Rojas, and R. Brendel, "19%-Efficient and 43 μm-Thick Crystalline Si Solar Cell from Layer Transfer Using Porous Silicon," *Progress in Photovoltaics: Research and Applications* 20, no. 1 (2012): 1.

13. M. A. Green and Z. Zhou, "Light-Trapping by Wave Interference in Intermediate-Thickness Silicon Solar Cells: Comment," *Optics Express* 33, no. 18 (2025): 37499.

14. S. Bhattacharya and S. John, "Light-Trapping by Wave Interference in Intermediate-Thickness Silicon Solar Cells: Reply," *Optics Express* 33, no. 18 (2025): 37503.

15. P. Kuang, S. Bhattacharya, M.-L. Hsieh, S. John, and S. Y. Lin, "Photonic Crystals with a Continuous, Gaussian-Type Surface Profile for Near-Perfect Light Trapping," *Journal of Nanophotonics* 12, no. 2 (2018): 026011.

16. M.-L. Hsieh, A. Kaiser, S. Bhattacharya, S. John, and S. Y. Lin, "Experimental Demonstration of Broadband Solar Absorption beyond the Lambertian Limit in Certain Thin Silicon Photonic Crystals," *Scientific Reports* 10 (2020): 11857.

17. K. R. McIntosh, S. C. Baker-Finch, "*OPAL 2: Rapid optical simulation of silicon solar cells*," in Proceedings of the 38th IEEE Photovoltaic Specialists Conference (IEEE, 2012), 265.

18. C. Koch and T. J. Rinke, Photolithography: Basics of Microstructuring, 4th ed. (MicroChemicals GmbH, 2017).

19. H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel, "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions: I Orientation Dependence and Behavior of Passivation Layers," *Journal of the Electrochemical Society* 137 (1990): 3612.

20. K. R. Williams, K. Gupta, and M. Wasilik, "Etch Rates for Micromachining Processing-Part II," *Journal of Microelectromechanical Systems* 12, no. 6 (2003): 761.

21. P.-H. Chen, H.-Y. Peng, C.-M. Hsieh, M. K. Chyu, "The Characteristic Behavior of TMAH Water Solution for Anisotropic Etching on Both Silicon Substrate and SiO2 Layer," *Sensors and Actuators A: Physical* 93 (2001): 132.

22. O. Tabata, R. Asahi, H. Funabashi, K. Shimaoka, and S. Sugiyama, "Anisotropic Etching of Silicon in TMAH Solutions," *Sensors and Actuators A: Physical* 34 (1992): 51.

23. M. Rienäcker, J. Maksimovic, Y. Larionova, et al., *Integration of Photonic Crystals in Highly Efficient POLO2-IBC Cells–Interplay between Structural, Optical and Electrical Properties*," Presented at SiliconPV. 2023 in Delft, (2023).

24. F. Haase, C. Hollemann, S. Schäfer, et al., Laser Contact Openings for Local Poly-Si-Metal Contacts enabling 26.1%-Efficient POLO-IBC Solar Cells, *Solar Energy Materials and Solar Cells* 186 (2018): 184.

25. M. Rienäcker, Y. Larionova, J. Krügener, C. Kranz, A. Merkle, and D. Walter, "Rear Side Dielectrics on Interdigitating p^+-(i)-n^+ Back-Contact Solar Cells–Hydrogenation vs. Charge Effects," *EPJ Photovoltaics* 12, no. 6 (2021): 1.

26. M. Rienäcker, "*Three-Terminal Tandem Solar Cells Enabled by Back-Contacted Bottom Cells Featuring Passivating, Carrier-Selective Polysilicon Based Junctions*," (PhD thesis, Hannover Institutionelles Repositorium der Leibniz Universität Hannover, 2022), https://doi.org/10.15488/11835.

27. J. A. Rand and P. A. Basore, "*Light-Trapping Silicon Solar Cells-Experimental Results and Analysis*," The Conference Record of the Twenty-Second IEEE Photovoltaic Specialists Conference (IEEE, 1991), 192, https://doi.org/10.1109/PVSC.1991.169207.

28. R. Brendel, T. Dullweber, R. Peibst, C. Kranz, A. Merkle, and D. Walter, "Breakdown of the Efficiency Gap to 29% Based on Experimental Input Data and Modeling," *Progress in Photovoltaics: Research and Applications* 24 (2016): 1475.

29. K. R. McIntosh, T. C. Kho, K. C. Fong, et al., "*Quantifying the Optical Losses in Back-Contact Solar Cells*," 2014 IEEE 40th Photovoltaic Specialist Conference (PVSC) (IEEE, 2014), 115, https://doi.org/10.1109/PVSC.2014.6925360.

30. C. Schinke, P. Christian Peest, J. Schmidt, et al., "Uncertainty Analysis for the Coefficient of Band-to-Band Absorption of Crystalline Silicon," *AIP Advances* 5 (2015): 067168.