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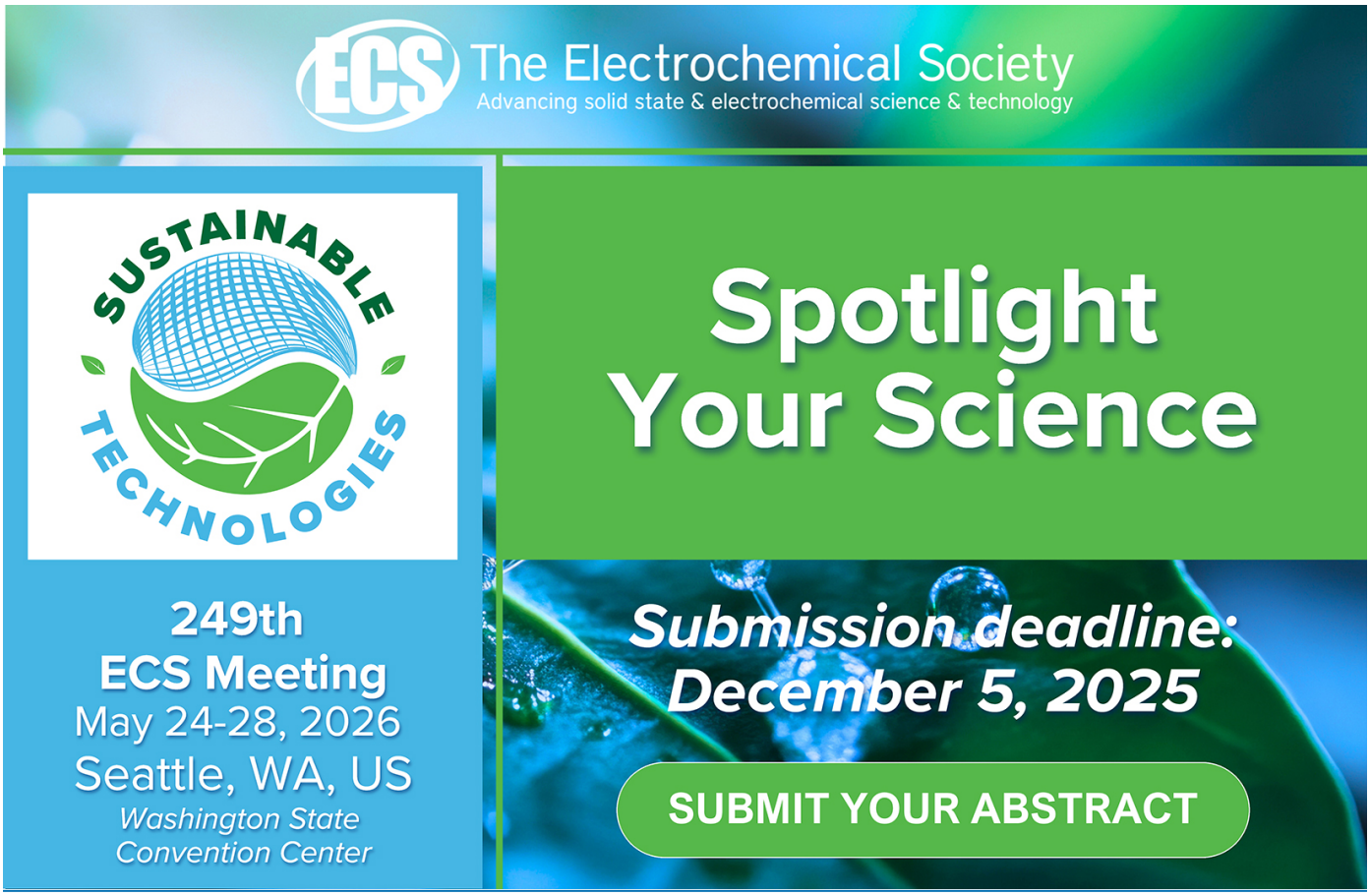

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HGCAL SiPM-on-tile full-stack integration with the Serenity Phase-2 DAQ hardware

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Abstract: For the upcoming high-luminosity LHC, the endcap calorimeters of the CMS experiment will be replaced by the high granularity calorimeter (HGCAL), a sampling calorimeter using both silicon and scintillator as active materials in different regions depending on the radiation dose. This contribution describes the integration details of the scintillator-based front-end into the readout chain of HGCAL. A prototype of the SiPM-on-tile readout chain was successfully operated in two recent beam tests at CERN SPS, demonstrating stable operation in a 3 T magnetic field and synchronization of sensor modules across different optical links. For the first time, both the silicon and SiPM-on-tile sensors of HGCAL are integrated into a single system utilizing a Serenity-Z FPGA card. Coarse event data which would be used for trigger logic are read out synchronously for both sensor types and across multiple layers.

Keywords: Data acquisition circuits; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Front-end electronics for detector readout

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Contents

1 Introduction

The High Granularity Calorimeter (HGCAL) [1] of the Compact Muon Solenoid (CMS) experiment [2] at CERN's Large Hadron Collider consists of two sensor technologies: silicon sensors for the electromagnetic section of the calorimeter as well as parts of the hadronic section, and plastic scintillator tiles read out by a silicon photomultiplier (SiPM) in the rear part of the hadronic section where the projected radiation damage is lower. This so-called SiPM-on-tile technology was developed by the CALICE collaboration [3] and has been optimized for mass production.

A central feature of the HGCAL design is that both the silicon and the SiPM-on-tile sensors share the same readout scheme using the same front-end ASICs. Moreover, all back-end systems of HGCAL are based on the same kind of FPGA platform, the Serenity ATCA cards [4, 5].

A complete vertical (start-to-end) slice of the silicon sensor readout chain was commissioned and validated in a beam test in summer 2023 [6, 7]. For the integration of the SiPM-on-tile modules of HGCAL into the Serenity-based readout, the different arrangement of components in the front-end and an additional ASIC for slow control posed new challenges.

The commissioning of the SiPM-on-tile readout chain was initially done with a separate readout system to make sure that the calibration of the front-end as well as the relation between trigger and DAQ data are well understood. Subsequently, silicon and scintillator modules were connected to the same readout system to demonstrate combined readout of trigger data.

2 The SiPM-on-tile readout chain

In the scintillator section of HGCAL, the SiPMs are mounted directly on the readout board and a scintillator tile wrapped in reflective foil is placed on top of each SiPM. The printed circuit board with SiPMs, scintillator tiles and a readout chip is called tile module.

Both the silicon sensor pads and the SiPMs are connected to the same ASIC, the HGCAL readout chip (HGCROC) [8]. The HGCROC digitizes the analog signals and delivers the time of arrival (ToA) and, depending on the charge measured, an ADC measurement of the signal amplitude or the time over threshold (ToT). The full event information is only sent on demand, when a level-1 accept signal (L1A) is received. Additionally, the HGCROC also forms sums of either 4 or 9 readout channels

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continuously for each bunch crossing. After further processing these trigger sums (abbreviated TC for trigger cells) will be used as input to the global event trigger logic of the CMS detector.

For both the DAQ and the trigger path, there are data concentrator ASICs (ECON) [9], that compress the data sent to the back-end. The trigger data concentrator ECON-T applies one of five user-selectable algorithms to the trigger sums. For example, the super trigger cell (STC) algorithm groups multiple trigger cells together and only sends the sum of each STC and the index of the largest TC. The DAQ data concentrator ECON-D contains a state machine and memory to receive and parse DAQ packets from the HGCROC.

Figure 1 shows how these ASICs are arranged in the SiPM-on-tile readout chain. Up to five tile modules are connected to one motherboard which carries the data concentrators (two ECON-T's and one ECON-D) that are connected to two lpGBTs [10] and a VTRx+ [11] for communication with the back-end. The ECONs are configured via I^2C ports of the lpGBT. The wingboard is a passive board that fans out the signals and receiver lines of the motherboard to different connectors. The connection between the tile modules and the wingboard is either made with flex PCBs or with custom Twinax cables that are up to 1 m long.

Figure 1 also highlights some key differences between the silicon and SiPM-on-tile front-end: the gigabit transceiver slow control adapter (GBT-SCA) ASIC [12] provides I^2C masters, GPIOs and ADCs to the tile module but is not present in the silicon front-end. Moreover, the data concentrators are located on the motherboard, and not on a concentrator mezzanine like on the silicon modules. A low-dropout regulator ASIC (ALDO) is used to adjust the bias voltage of the SiPMs. And finally, there is a LED for gain calibration next to each SiPM.

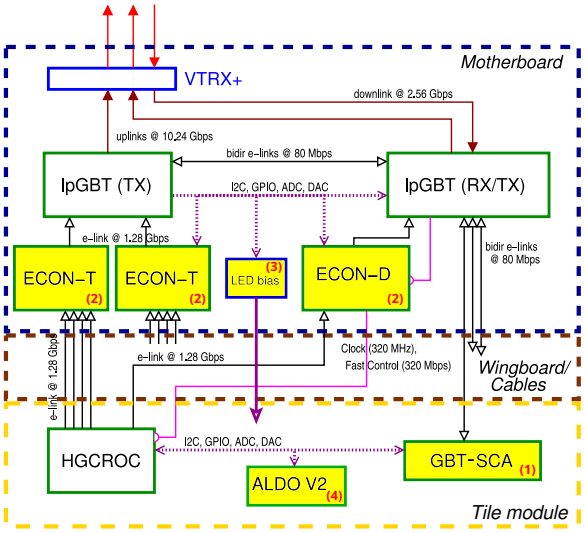

Figure 1. Illustration of the HGCAL SiPM-on-tile readout chain. Some key differences to the silicon readout chain are highlighted in yellow and labeled with numbers: (1) the GBT-SCA ASIC, (2) the location of the data concentrators, (3) the LED-based calibration system and (4) a low-dropout regulator (ALDO) for the SiPM bias voltage.

Commissioning and testing the HGCAL SiPM-on-tile readout chain was conducted with pre-series motherboards, which are equipped with two prototype ECON-T's, but no ECON-D. Instead, an additional lpGBT is present to be able to read out all 11 DAQ links. The absence of the ECON-D

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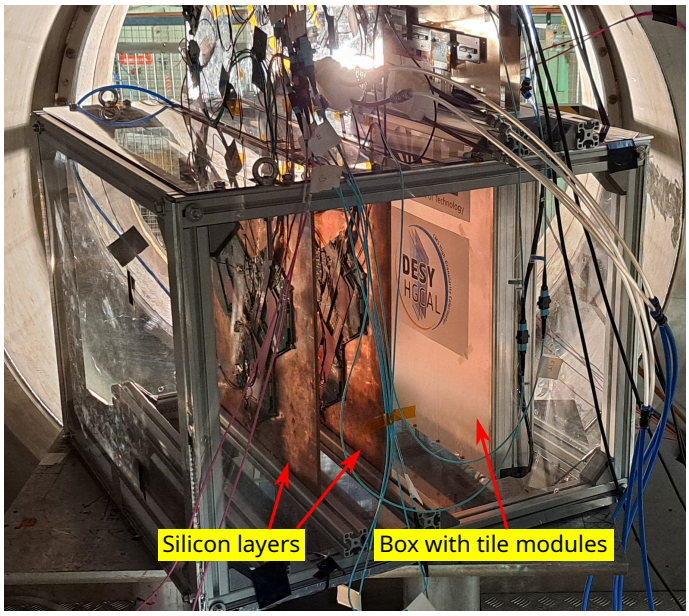
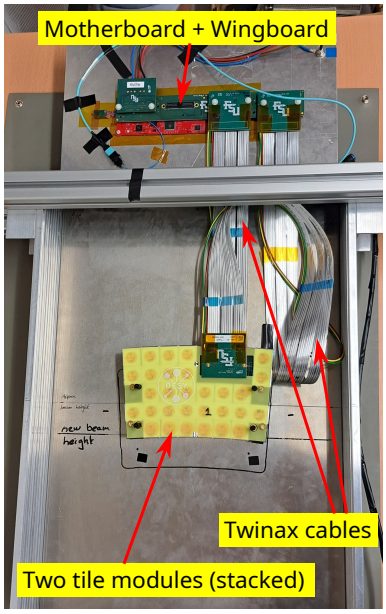
means that the DAQ data arrive at the back-end as HGCROC packets which are different from those of the ECON-D. Therefore, in these beam tests, only the trigger paths of the silicon and scintillator modules were read out together with the same back-end.

3 Validation of the SiPM-on-tile readout

The characterization of HGCAL SiPM-on-tile readout with Serenity was done in summer 2024 at the H2 beam line of CERN's north area facility. The tests were performed with 200 GeV electrons, as well as mixed muon and pion beams of different energies of 150 GeV and 250 GeV. A lead brick located upstream of the detector was used to generate electromagnetic showers from the electron beam. The beam tests were shared with the tests of the HGCAL silicon sensors, and all detector prototypes were placed next to each other in a common frame shown in figure 2. The setup was placed in the superconducting magnet of the H2 beam line.



(a) Frame holding two silicon sensor layers and a light-tight housing for scintillator tile modules. The frame is placed in the center of the superconducting magnet at the H2 beam line.



(b) A stack of two tile modules mounted in the box for scintillator tile modules.

Figure 2. Setup of the combined silicon and SiPM-on-tile beam test at the SPS H2 beam line.

For the first tests presented below, the readout between silicon and scintillator sensors was completely separated. The readout of the SiPM-on-tile front-end was based on a Serenity-Z1.1 with a KU15P FPGA and 10 Gbps UDP links to the DAQ PC.

System stability and operation in a 3 T magnetic field. During the beam tests, the SiPM-on-tile front-end was tested in a 3 T magnetic field for three different orientations. When there was no beam, the setup operated in a validation mode, during which the HGCROC sent pre-defined patterns and the back-end compared these patterns and counted the number of bit errors.

These link integrity tests were conducted for an integrated time of 107.5 h. For 37.5 h of that time the magnetic field was on and different rotations of the detector layers with respect to the

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magnetic fields were tested. The tile modules under test were connected to one or two motherboards with different link configurations.

Only for one hardware configuration, and only when the magnetic field was close to 3 T, one of the DAQ eLinks showed bit errors. A likely explanation is that there were impurities in one of the connectors on the Twinax cable. After changing the Twinax cable and cleaning the connectors with pressurized air, the same link was again observed for 20 h and did not have any deviation from the expected bit patterns.

Layer synchronization. Two different readout configurations were tested: tile modules connected to the same motherboard and two modules connected to different motherboards. When two motherboards were used, the communication happened over two different fibers and two different lpGBTs recovered the back-end clock independently. In all cases, the synchronous readout operated reliably and stably.

Trigger data readout. The ECON-T's were operated in STC4 4E3M mode. This means that the ADC values of four trigger cells from the HGCROC are added together to form a super trigger cell (STC). The value of the energy of the STC is sent in an exponential format with 4 bits for the exponent, and 3 bits for the mantissa (4E3M).

Figure 3 shows a 2D histogram of the energy values of an STC, compared to the sum of ADC and ToT of the DAQ channels for the respective events, accounting for calibration factors, data compression and the STC algorithm. In this preliminary analysis, less than 5 % of the events deviate by more than 50 ADC bins from the expected behaviour. This demonstrates that the relation between trigger and DAQ is well understood and that the relevant calibration parameters in the HGCROC are set properly. The remaining outliers will be investigated in more detailed studies of the beam test data.

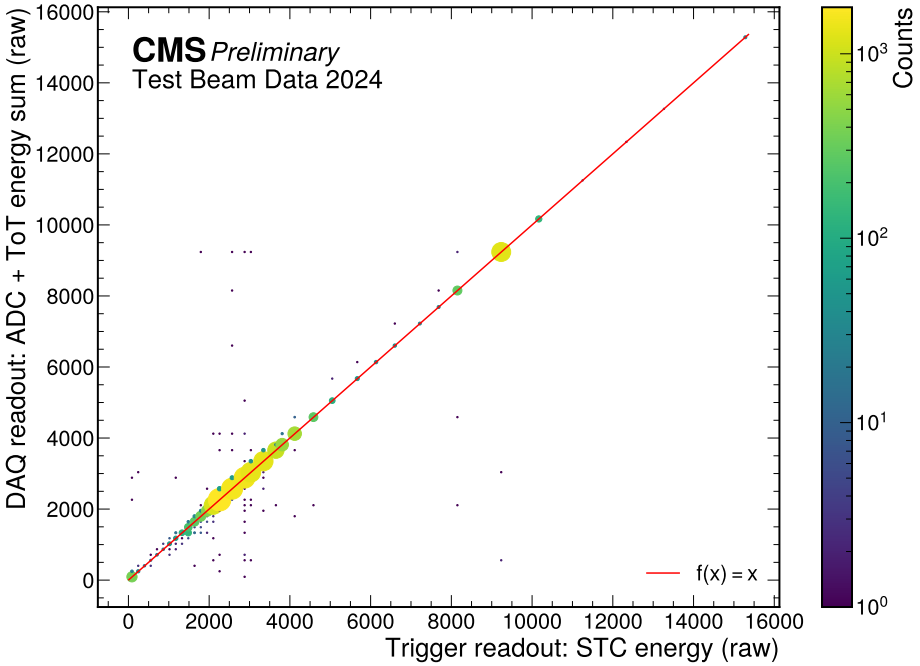

Figure 3. Histogram of the energy value of a super trigger cell (STC) compared to the sum of ADC or ToT from the DAQ readout for all channels in this STC. The histogram bins are represented as colored dots. The color and size of each dot corresponds to the number of events in the bin.

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4 First integrated readout of silicon and SiPM-on-tile modules

The silicon sensor readout for these beam tests was based on a Serenity-Z 1.2 with a VU7P FPGA, a DTH-p1-v2 [13] and a DAQ PC. Two tile modules with the latest, close-to-final, version 3b of the HGCROC were connected to the Serenity-Z 1.2 and trigger data were read out simultaneously for both silicon and SiPM-on-tile sensors. Both of these tile modules were connected to the same motherboard, but trigger data went through two different ECON-T's on that motherboard. The data were taken with electromagnetic showers from 200 GeV electrons.

Figure 4 shows trigger sums of seven consecutive bunch crossings for two tile module layers and a silicon layer. The time position of each bin is corrected by the particle arrival time measured with an external scintillator trigger. The peaks caused by the electromagnetic showers are centered around the fourth bunch crossing in each layer. This demonstrates that the timing of the layers is well aligned and events are read out synchronously for both sensor types.

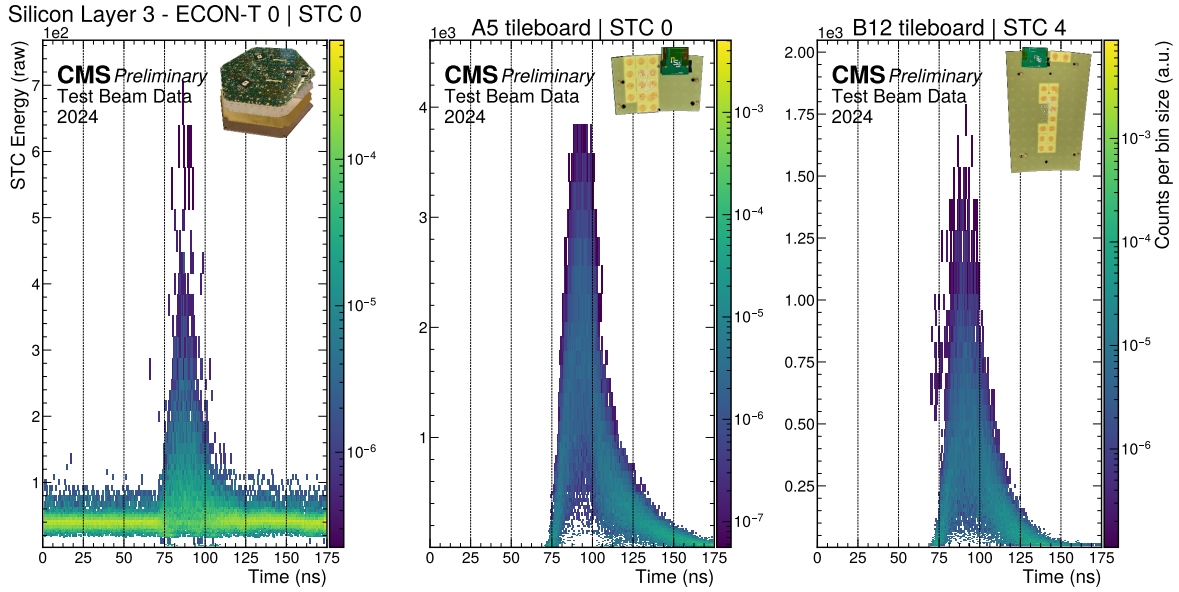

Figure 4. Examples of trigger sums for seven consecutive bunch crossings, corrected by the particle arrival time, for two different scintillator tile layers and a silicon layer. All three detector modules are read out synchronously by the same Serenity board.

5 Conclusion and outlook

A full vertical stack of SiPM-on-tile hardware was tested in two beam tests in summer 2024 together with silicon sensor layers. Stable operation of the HGCAL front-end in magnetic fields up to 3 T, synchronization of multiple tile modules, as well as a good understanding of the relation between trigger and DAQ data with properly calibrated modules has been demonstrated.

After initial verification of proper operability with a separate readout system, the scintillator tile modules were connected to the same Serenity board as the silicon layers, and trigger sum data from both sensor types were read out synchronously. The next step will involve commissioning of the production version of the motherboard and characterizing the DAQ readout of the SiPM-on-tile sensors with the ECON-D data concentrator ASIC.

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