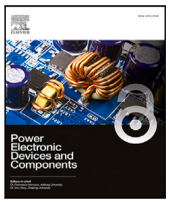
Power Electronic Devices and Components 12 (2025) 100125

Contents lists available at ScienceDirect

Power Electronic Devices and Components

journal homepage: www.journals.elsevier.com/power-electronic-devices-and-components



Real-time power loss optimized operation of a solid state transformer by utilizing the common-mode voltage☆

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ARTICLE INFO

Keywords:
Analytical loss computation
Cascaded H-Bridge
Dual Active Bridge converter
Solid-State Transformer

ABSTRACT

This article presents a general methodology and a real-time capable, analytically solvable model for minimizing the total power losses of a modular Solid-State Transformer (SST). The approach leverages the inherent Degree of Freedom (DoF) offered by the common-mode (CM) voltage u_{cm} in three-phase systems. By systematically adjusting the CM voltage, the power distribution among all sub-modules (SM) is influenced to reduce the total losses of the Dual Active Bridges (DAB) without imposing additional constraints on the SST operation. An analytical loss model, with the CM voltage as the DoF, is derived from measured loss characteristics of an individual DAB module and extrapolated to the full three-phase SST. The proposed optimization method is implemented on a field-programmable gate array which is able to find the global loss minimum in real time. A 45 kW, 400 V_{AC} to 750 V_{DC} SST test bench is used to validate the methodology. The calculated and measured results over the whole power range of the prototype align which confirms the accuracy of the loss model. An overall loss reduction of up to 20% is achieved without sacrificing output voltage quality or requiring changes to the modulation scheme.

1. Introduction

The Solid-State Transformer (SST) offers significant potential for use as a medium voltage (MV) alternating current (AC) to low voltage (LV) direct current (DC) grid coupling interface. It enables controlled active and reactive power flow, as well as higher volumetric and gravimetric power density. In addition, it reduces the number of inverter stages and provides active filtering of grid harmonics compared to a conventional low-frequency transformer (LFT) with an added inverter stage (Ferreira Costa, De Carne, Buticchi, & Liserre, 2017). However, a major drawback of an SST is its lower efficiency compared to the combination of an LFT with an inverter (J.E. & Kolar, 2019). To address this limitation, extensive research has focused on reducing the efficiency gap while enhancing existing benefits and overall SST design, including its lifetime (Ko, Raveendran, Andresen, & Liserre, 2018). A common topology for connecting a MV AC grid to an LV DC microgrid is the input serial output parallel (ISOP) structure, built with similar power sub-modules (SM). These modules transmit energy to either the MV- or the LV-side, depending on the requested power flow direction. The Dual Active Bridge (DAB) is often used as a galvanically isolating power transmission stage. First introduced in Doncker, Divan, and Kheraluwala (1991), it has since been extensively studied and improved. Its main advantages are high dynamic performance, zero voltage switching (ZVS) capability, and controllable bidirectional power flow.

Improving the efficiency of the DABs, and thereby the SMs, directly contributes to increasing the overall efficiency of the SST. Existing approaches typically focus on hardware enhancements or refined modulation schemes. For example, the influence of additional snubber capacitors on the switching behavior of the semiconductors and the resulting efficiency has been analyzed in Inoue and Akagi (2007), Kheraluwala, Gascoigne, Divan, and Baumann (1992), while Lee, Song, Park, and Kim (2023) proposes a systematic procedure for optimal transformer design. Other methods include adapting the switching frequency (Bahmani, Thiringer, & Rabiei, 2016), adjusting module voltages to operate at more efficient operation points (OP) (Liu et al., 2018, 2020), or modifying the modulation scheme according to the required power and voltage ratio (Everts, 2017; F. & Kolar, 2012a, 2012b; Gong et al., 2022; Oggier, Garcia, & Oliva, 2011).

In contrast, this work explores a different approach by utilizing the common-mode (CM) voltage as an additional Degree of Freedom (DoF) inherent in the three-phase system of an SST. Traditionally,

☆ This article is part of a Special issue entitled: 'Selected papers EPE'25' published in Power Electronic Devices and Components.

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https://doi.org/10.1016/j.pedc.2025.100125
Received 17 June 2025; Received in revised form 26 July 2025; Accepted 16 October 2025
Available online 20 October 2025
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NOMENCLATURE

a_{dc}	Duty cycle of a switching module
a_{fix}	Number of modules per phase in an active state
a_x	Duty cycles for the phase modules
B_{pot}	Upper bound of potential local minima
D	Power control decoupling factor
f_{DAB}, f_{CHB}	DAB/CHB switching frequency
f_{FPGA}	Operation frequency of the used FPGA
f_{grid}	Grid frequency
f_{sys}	System control frequency
$i_{AC,x}$	AC current of phase x
i_{bal}	Module voltage balancing current
i_{ff}	Oscillating instantaneous feed forward current
i_{mod}	Module current
$I_{AC,max}$	Maximum phase current
I_d	Current in d-axis
I_p	Primary-side current
I_q	Current in q-axis
k	Index for indicating positive or negative power flow
L_{grid}	Grid filter for calculations
m	Index of respective module
M_{ph}	Amount of modules per phase
n_t	Transformer winding ratio
p_0, p_1, p_2	Parameters for quadratic fit function
P_{DAB}	Nominal power of DAB
P_{losses}	SST Power losses
$P_{losses,brute}$	Power losses with brute force optimized CM voltage
$P_{losses,opt}$	Power losses with analytically optimized CM voltage
$P_{losses,red}$	Power loss reduction of SST
$P_{losses,tri}$	SST power losses with triangular CM voltage
P_{SST}	Nominal power of SST
t	Time
U_d	Voltage in d-axis
U_{grid}	AC grid voltage
U_{mod}	Module voltage
U_p	Primary-side voltage
U_q	Voltage in q-axis
U_s	Secondary-side voltage
$u_{AC,x}$	AC voltage of phase x
u_{cm}	CM voltage
$u_{cm,brute}$	Brute forced optimal CM voltage
$u_{cm,dis}$	CM voltage of a discontinuity
$u_{cm,opt}$	Calculated optimal CM voltage
$u_{cm,pot}$	CM voltage of a potential minima
$u_{cm,tri}$	Triangular CM voltage setpoint
u_{FB}	Output voltage of a module
x	Index for phase U, V or W
γ	Grid angle
λ_{SOV}	Static grid overvoltage factor
φ	Phase angle between voltage and current

the CM voltage is used to maximize the output voltage in multilevel converters (Tolbert & Habetier, 1999). In Angulo, Lezana, Kouro, and Rodríguez (2007) it serves to balance temperature and distribute the power losses of the SMs. This concept is further explored in Ko, Andresen, Buticchi, and Liserre (2017), Ko et al. (2018), where power routing is adapted based on wear indicators to prolong the overall system lifetime. Other applications include power redistribution during fault conditions to improve system resilience (Unruh, Lange, Schafmeister, & Bocker, 2021; Zhao et al., 2021), as well as battery state of charge (SoC) balancing and loss reduction in battery-supported multilevel converters (Maharjan, Yamagishi, & Akagi, 2012; Merz, Hellmann, Specht, & Hiller, 2022; Merz, Korte, Specht, & Hiller, 2020; Spina, Brando, & Dannier, 2024). Moreover, Kopacz, Menzi, Krismer, Rąbkowski, Kolar, and Huber (2024) demonstrate that the CM voltage is essential for the correct operation of certain converter topologies.

Table 1
Switching states of the CHB cell.

State	Conducting	Output voltage u_{FB}	Module current i_{mod}
Positive	T_1, T_4	U_{mod}	i_{AC}
Negative	T_2, T_3	$-U_{mod}$	$-i_{AC}$
Bypass 1	T_1, T_3	0 V	0 A
Bypass 2	T_2, T_4	0 V	0 A

The methodology proposed in this work exploits the CM voltage to optimize the OPs of all power modules with the goal of minimizing total DAB losses. Starting from a basic loss function derived from measurements of a single DAB, a mathematical loss model is developed for the phases and for the complete SST. This combined loss model is minimized in real-time using analytical methods, treating the CM voltage as an active DoF. This yields a set of valid CM voltages u_{cm} that will lead to a global loss minimum for the system. Based on the initial loss model, the power losses of the upcoming OPs for these valid CM voltages are predicted, and the CM voltage corresponding to the minimum losses is selected. The consistency between offline calculations and online measurements validates the method's effectiveness and applicability. It is shown that the approach enables a significant real-time loss reduction of up to 20 %.

This publication is organized as follows: Section 2 describes the system topology and the key components of the investigated SST. Section 3 presents the analytical methodology in several steps. First, Section 3.1 discusses the measured power losses of a single DAB module. Next, Section 3.2 introduces an analytical function that models the total losses across all modules in the SST. In Section 3.3, the role of the CM voltage u_{cm} in loss reduction is explained. Section 3.4 outlines the mathematical optimization procedure used to minimize total power losses by adjusting u_{cm}. Section 4 illustrates the designs of the test benches for the SM and the SST. The calculated and experimental results are presented in Section 5, validating the effectiveness and accuracy of the proposed method. Finally, the findings are summarized in Section 6. Fig. 1 illustrates the overall research methodology followed in this work.

2. Topology

The investigated topology is a three-phase modular Cascaded H-Bridge (CHB)-based SST in star connection. Each SM is individually powered by a galvanically isolated DAB. For the purpose of this publication, the primary-side voltage U_p is seen as constant and controlled by an external voltage source.

2.1. Power module

A single power module, consisting of a CHB cell and a DAB stage, is illustrated in Fig. 2. The DAB, highlighted in blue, enables unrestricted bidirectional power flow and operates at unity gain. The CHB cell, highlighted in green, generates the AC output of each power module. The DABs are set up to transfer enough power to neglect a voltage ripple of the DC link capacitors, and no special DC voltage ripple suppression method needs to be implemented as in Li, Zhang, Wang, Liu, Ji, and Chang (2024).

2.2. SST topology

The overall topology of the SST prototype is depicted in Fig. 3. The DAB stages are connected in parallel and are powered by a bidirectional DC voltage source with an output voltage of U_p. The converter's AC output voltages $u_{AC,x}$, where $x \in \{U, V, W\}$, are generated by a

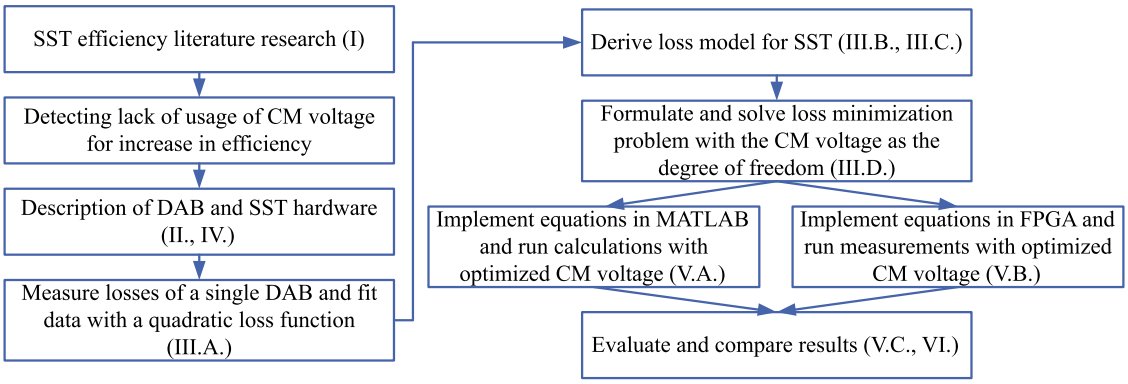

Fig. 1. Flowchart of the research methodology.

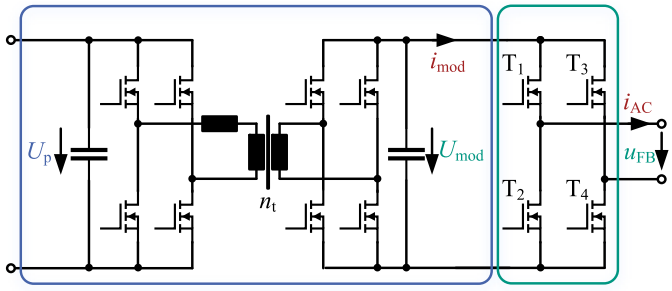

Fig. 2. Power module with DAB stage for power supply (blue) and CHB cell output stage (green).

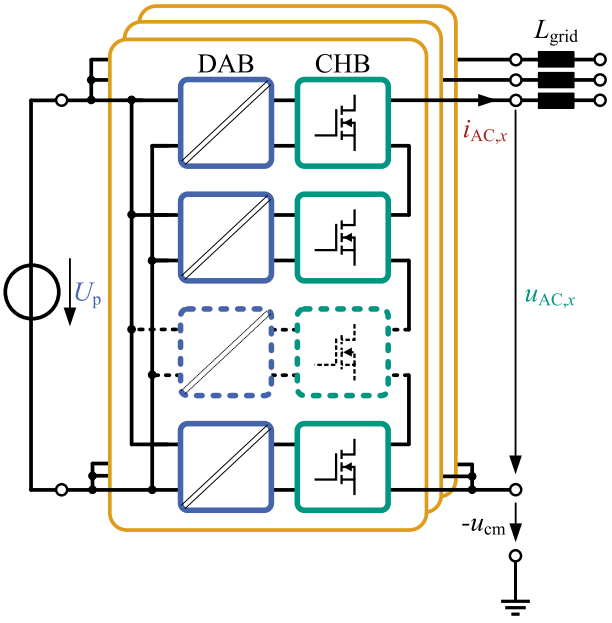

Fig. 3. Three-phase modular ISOP SST for AC/DC grid coupling. The dotted module indicates that multiple modules can be used.

series connection of the CHB cells. Depending on the switching state of the four MOSFETs T_1 to T_4, the CHB cell provides three discrete voltage levels $u_{FB} \in \{+U_{mod}, -U_{mod}, 0\,V\}$. Each SST phase operates using voltage shifted pulse width modulation (VSPWM) with one switching module per phase. An instantaneous unequal power loss distribution within a phase can be balanced in two ways: by frequently replacing the currently active with bypassed modules, and by prioritizing the use of modules with the lowest temperatures for generating the next sinusoidal half-wave of the grid. As a result, overdimensioning of the modules is not necessary, since in average all modules transmit the same power. The switching states with the resulting output voltages u_{FB} and the module current i_{mod} in dependence of the phase current i_{AC} of the CHB cell is shown in Table 1.

2.3. Common-mode voltage

In general the current CM voltage u_{cm} is calculated as shown in (1). The voltage between the phase and the neutral point of the converter is defined as $u^*_{AC,x}$. To enhance voltage utilization of the converter, a triangular-shaped CM voltage $u_{cm,tri}$ is added to the voltage setpoints of the controller. This triangular CM voltage setpoint is calculated as shown in (2). This DoF is further leveraged by the proposed algorithm described in the following sections. In this publication, the harmonic content of the output voltage is not analyzed in detail. This simplification is justified, as the SST operates as a multilevel converter with many voltage levels per phase and an assumed switching frequency in the kilohertz range. More details on reducing the harmonics is described in Mandol, Biswas, Roy, Hosain, and Kibria (2019), Satiawan (2021), for example.

$$u_{cm} = \frac{1}{3} \cdot \sum_x u^*_{AC,x} \tag{1}$$

$$u_{cm,tri} = -\frac{\min\left(u_{AC,UVW}\right) + \max\left(u_{AC,UVW}\right)}{2} \tag{2}$$

3. Proposed optimized operation mode

The proposed power loss-optimized operation mode of the SST aims to reduce overall power losses by considering the individual losses of each DAB at the current OP. Therefore, a mathematical model is developed to analytically describe the power losses of each DAB (Section 3.1). Using this model, the power losses of each phase and the entire SST can be predicted based on the current operating conditions (Section 3.2). The total losses are then minimized by adjusting the CM voltage u_{cm}, which serves as a DoF in the system (Section 3.4). A key requirement when applying the proposed method is ensuring that the setpoints of the superimposed current controller remain unaffected. This is achieved by maintaining the relevant line-to-line voltages of the SST unchanged, even when the CM voltage u_{cm} is modified.

3.1. Power losses of a single DAB

Firstly, the power losses of the DAB stage of a power module operating at unity gain (cf. the blue box in Fig. 2) are measured using a power meter with fixed primary and secondary voltages U_p and U^*_{mod}. The measured losses are fitted to a function based on the module current i_{mod}. It is assumed that the switching losses of the CHB cells

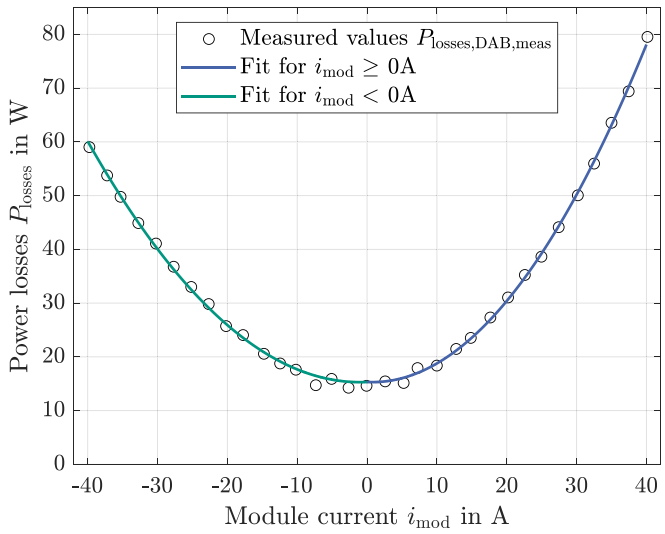

Fig. 4. Measured and fitted power losses of a DAB with $U_{\text{p}} = 750\,\text{V}$ and $U^*_{\text{mod}} = 53.2\,\text{V}$.

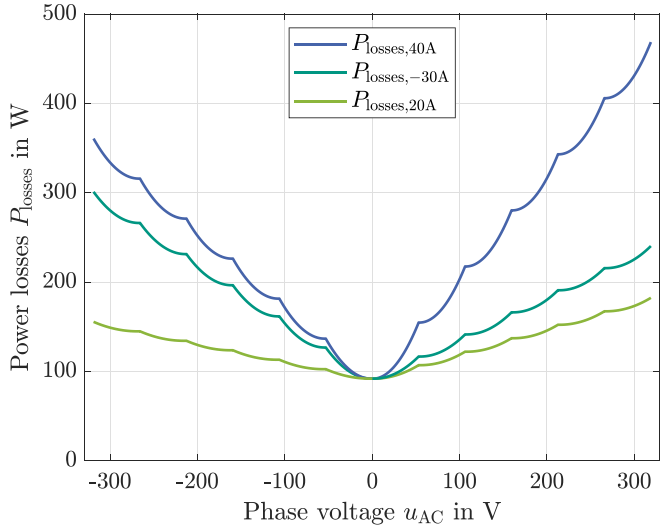

Fig. 5. Calculated power losses of a single phase with six modules for different phase currents and voltages.

remain within the same range as they would without the proposed method. Fig. 4 shows the measured power losses $P_{\text{losses,meas}}$ (black circles) (Merz et al., 2025b). The results reveal an asymmetry between positive and negative module currents. This asymmetry arises from different voltage levels on the primary and secondary sides, leading to different semiconductor switching behavior. More hardware details and an explanation of the experimental test setup is shown in Section 4.

Secondly, to obtain an analytical description of power losses as a function of the module current i_{mod}, the measurement results are used for curve fitting. Due to the observed asymmetry, two separate functions are employed: one for positive output power/current ($i_{\text{mod}} \geq 0\,\text{A}$) and another for negative output power/current ($i_{\text{mod}} < 0\,\text{A}$). Since lower-order polynomials are easier to handle and capture the main loss contributions, a quadratic function is chosen. This choice reflects the typical behavior of losses: copper losses scale quadratically, switching losses linearly, and transformer core losses remain constant under fixed switching frequency and voltages (Menger, Merz, Gehringer, Sommer, & Hiller, 2022), as shown in (3). If sufficient computational power is available, higher-order polynomials or other function types could be used for more precise real-time optimization.

$$P_{\text{losses,DAB}}(i_{\text{mod}}) = p_{2,k} \cdot i^2_{\text{mod}} + p_{1,k} \cdot i_{\text{mod}} + p_{0,k} \tag{3}$$

Thirdly, the variables $p_{0,k}$, $p_{1,k}$, $p_{2,k}$ serve as fitting parameters of the loss function. The index $k \in \{\text{pos}, \text{neg}\}$ indicates whether the power flow within a module is positive or negative, respectively. This distinction ensures an accurate representation of the asymmetric power loss behavior observed during the measurements.

Fourthly, due to physical considerations, it is reasonable that the power losses for very small positive and negative currents, close to 0 A, should be similar. This leads to a constant offset and an intersection of the curves, creating a continuous function that may not be continuously differentiable. Consequently, $p_{0,\text{pos}} = p_{0,\text{neg}} = p_0$. The results of the fitting parameters for the investigated scaled prototype are shown in Section 5.

3.2. Mathematical loss model of SST caused by the DABs

The fitted power loss curves of a single DAB are used to construct an analytical power loss model. This model represents a single phase of the SST and depends on the number of modules per phase, M_{ph}. Fig. 5 illustrates the phase power losses as a function of different phase currents i_{AC} ($i_{\text{AC}} = 40\,\text{A}$ in blue, $i_{\text{AC}} = -30\,\text{A}$ in dark green, $i_{\text{AC}} = 20\,\text{A}$ in light green). As mentioned earlier, each phase operates with VSPWM. In this mode, only one module is actively switching, while the other modules are either in bypass or in an active state (i.e., positive or negative) to achieve the phase voltage setpoints $u^*_{\text{AC},x}$ of the overlaid controller as accurately as possible.

The amount of modules in a phase in an active state is an integer value and denoted by $a_{\text{fix},x}$, where $a_{\text{fix},x} \in \mathbb{Z}$ and $-M_{\text{ph}} \leq a_{\text{fix},x} \leq M_{\text{ph}}$. Each DAB stage of a module in a positive state must deliver the corresponding phase current $(i_{\text{mod}} = i_{\text{AC}})$ to maintain a constant module voltage $U_{\text{mod}} = U^*_{\text{mod}}$. Modules in a negative switching state have to supply the negative phase current $(i_{\text{mod}} = -i_{\text{AC}})$. Modules in bypass state do not transmit any power in this control cycle ($i_{\text{mod}} = 0\,\text{A}$). The DAB stage of the switching module supplies a portion of the phase current, given by $i_{\text{mod}} = a_{\text{dc}} \cdot i_{\text{AC}}$. The duty cycle $a_{\text{dc},x}$ which determines this portion and satisfies $-1 \leq a_{\text{dc},x} \leq +1$, is derived from the voltage setpoint of the current controller. For simplicity it is assumed that the actual module voltages are equal to the setpoint of the module voltage.

It is evident that smaller phase voltages and currents result in lower phase losses. However, phase currents are not a DoF, as they are defined by the superimposed controller and the grid. The resulting mathematical loss model of a single phase is shown in (4).

$$\begin{aligned} P_{\text{losses},x}(a_{\text{fix},x}, a_{\text{dc},x}, M_{\text{ph}}, i_{\text{AC},x}) = {} & p_{2,k,x} \cdot \left(|a_{\text{fix},x}| + a^2_{\text{dc},x} \right) \cdot i^2_{\text{AC},x} \\ & + p_{1,k,x} \cdot \left(a_{\text{fix},x} + a_{\text{dc},x} \right) \cdot i_{\text{AC},x} + p_0 \cdot M_{\text{ph}} \end{aligned} \tag{4}$$

Combining (4) for each phase and considering that the change in CM voltage u_{cm} changes $a_{\text{fix},x}$ and $a_{\text{dc},x}$ as shown in (5) and (6) for each phase x leads to (7). The function 'trunc' is a truncation which means rounding to the next integer in the direction of zero.

$$a_{\text{fix},x}(u_{\text{cm}}) = \text{trunc}\left(\frac{u^*_{\text{AC},x} + u_{\text{cm}}}{U^*_{\text{mod}}} \right) \tag{5}$$

$$a_{\text{dc},x}(u_{\text{cm}}) = \frac{u^*_{\text{AC},x} + u_{\text{cm}}}{U^*_{\text{mod}}} - a_{\text{fix},x}(u_{\text{cm}}) \tag{6}$$

$$P_{\text{losses,total}}(u_{\text{cm}}) = \sum_x P_{\text{losses},x}(u_{\text{cm}}) \tag{7}$$

3.3. Using the common-mode voltage for optimization

Since the investigated SST is a three-phase system in a star connection, it inherently offers the opportunity to use the CM voltage u_{cm}

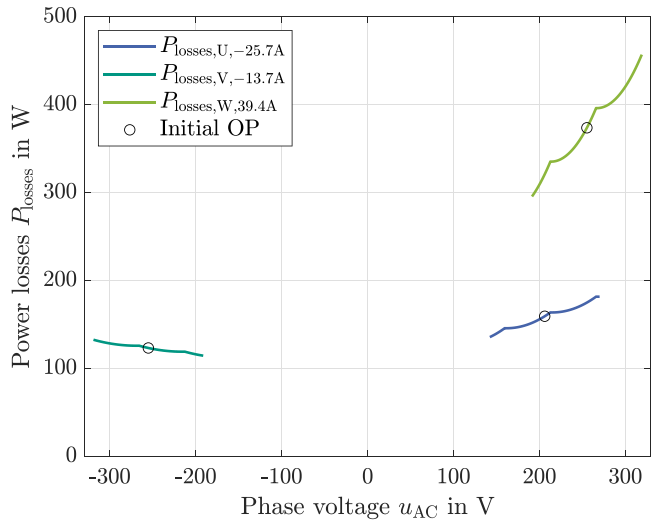

Fig. 6. Calculated power losses of each phase for a specific OP and valid voltage modification range.
($\hat{u}_{\text{AC}} = 325\,\text{V}$, $\hat{i}_{\text{AC}} = 40\,\text{A}$, $\varphi = 65°$, $\gamma = 25°$)

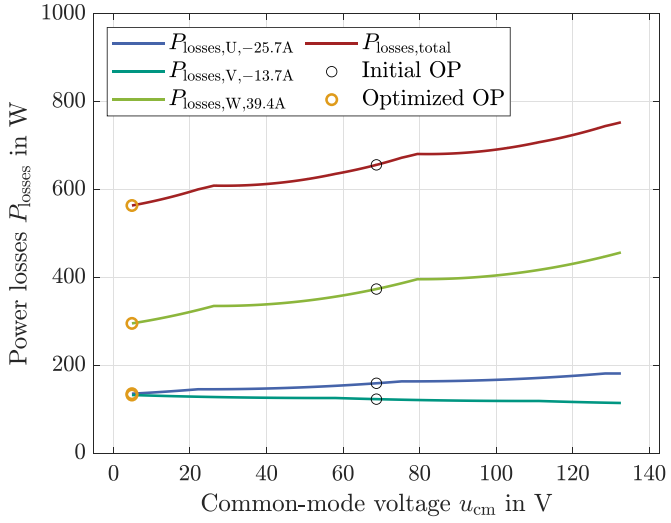

Fig. 7. Losses within each phase and total DAB losses in relation to the valid CM voltage u_{cm} range.
($\hat{u}_{\text{AC}} = 325\,\text{V}$, $\hat{i}_{\text{AC}} = 40\,\text{A}$, $\varphi = 65°$, $\gamma = 25°$)

for various objectives. Primarily, the CM voltage is typically used to increase the maximum output voltage. However, because the SST does not always operate at its voltage limits, the valid CM voltage range of the combined phases, which can be calculated according to (8), can be utilized to reduce the total losses of the DABs. This is achieved by operating more DABs at higher efficiency and fewer at less efficient OPs.

$$-M_{\text{ph}}U^*_{\text{mod}} - \min(u_{\text{AC},x}) \le u_{\text{cm}} \le M_{\text{ph}}U^*_{\text{mod}} - \max(u_{\text{AC},x}) \tag{8}$$

Fig. 6 illustrates the power losses of each phase for an example OP with the setpoint for the CM voltage at $u_{\text{cm}} = 68.7\,\text{V}$ (black circles), derived from the triangular CM voltage shape. When the CM voltage is modified, all three phase voltages shift in the same direction simultaneously to maintain the same line-to-line voltage. However, the losses in each phase change differently depending on the corresponding phase currents.

To highlight the potential for power loss modification, Fig. 7 shows the power losses of each phase as a function of the permissible CM voltage u_{cm} range, according to (8). Additionally, the sum of the phase losses $P_{\text{losses,total}}$ and the initial OP (black circles) are displayed. It is evident that in this case, reducing the CM voltage u_{cm} also reduces the total power losses. Hence, the overall efficiency of the SST is increased, if it is operated at the optimized OP (orange circles).

3.4. Minimizing the overall DAB power losses

Due to the mathematical power loss model of each phase, it is possible to solve this constrained, superimposed optimization problem analytically. Since the power losses are represented by second-order polynomial functions, calculating the local derivatives and setting them to zero to find local minima is simple. Solving (9) for u_{cm} leads to several local minima and a potential global minimum. Given the constraints, the maximum and minimum CM voltages must also be tested to identify the global minimum. By evaluating this limited set of potential local minima with the predicted losses from (7), the global minimum of the power losses is determined and the respective optimal CM voltage $u_{\text{cm,opt}}$ is applied to the output of the SST phases. This minimization process is illustrated in the flowchart shown in Fig. 8. Furthermore, the detailed steps to calculate the analytical solution for (9) is as explained in the following paragraphs.

$$\frac{\mathrm{d}P_{\text{losses,total}}}{\mathrm{d}u_{\text{cm}}} = \sum_x \frac{\mathrm{d}P_{\text{losses},x}}{\mathrm{d}u_{\text{cm}}} = 0\,\text{W}\,\text{V}^{-1} \tag{9}$$

Differentiability assumption: The truncation operator $\text{trunc}(\cdot)$ of (5) yields a piecewise constant derivative. Thus, within intervals of constant $a_{\text{fix},x}$, its derivative vanishes as shown in (10). The derivatives of $a_{\text{dc},x}$ and $a^2_{\text{dc},x}$ with respect to u_{cm} are given in (11) and (12), respectively.

$$\frac{\mathrm{d}a_{\text{fix},x}}{\mathrm{d}u_{\text{cm}}} = 0 \tag{10}$$

$$\frac{\mathrm{d}a_{\text{dc},x}}{\mathrm{d}u_{\text{cm}}} = \frac{1}{U^*_{\text{mod}}} \tag{11}$$

$$\frac{\mathrm{d}a^2_{\text{dc},x}}{\mathrm{d}u_{\text{cm}}} = 2a_{\text{dc},x} \cdot \frac{\mathrm{d}a_{\text{dc},x}}{\mathrm{d}u_{\text{cm}}} = \frac{2a_{\text{dc},x}}{U^*_{\text{mod}}} \tag{12}$$

Phase loss derivative: Throughout this derivation, the currents $i_{\text{AC},x}$ are defined by the controller and the grid, and are therefore assumed to be constant with respect to u_{cm}. Using (10) to (12) with (9) yields (13).

$$\frac{\mathrm{d}P_{\text{losses},x}}{\mathrm{d}u_{\text{cm}}} = \left(2p_{2,k,x}a_{\text{dc},x} \cdot i^2_{\text{AC},x} + p_{1,k,x} \cdot i_{\text{AC},x}\right) \cdot \frac{1}{U^*_{\text{mod}}} \tag{13}$$

Total loss derivative: Inserting (5) and (6) into (13), combining the three phases to the total derivative and setting this expression to zero gives the necessary condition for minimum losses. From the truncation operator of (14) it can be seen that the resulting function has discontinuities and a repetitive behavior whenever a phase voltage $u^*_{\text{AC},x} + u_{\text{cm}}$ equals multiples of U^*_{mod}.

$$\begin{aligned}\frac{\mathrm{d}P_{\text{losses,total}}}{\mathrm{d}u_{\text{cm}}} &= \sum_x \left(2p_{2,k,x}a_{\text{dc},x} \cdot i^2_{\text{AC},x} + p_{1,k,x} \cdot i_{\text{AC},x}\right) \cdot \frac{1}{U^*_{\text{mod}}} \\ &= \sum_x \left(2p_{2,k,x}\left(\frac{u^*_{\text{AC},x} + u_{\text{cm}}}{U^*_{\text{mod}}} - \text{trunc}\left(\frac{u^*_{\text{AC},x} + u_{\text{cm}}}{U^*_{\text{mod}}}\right)\right) \cdot i^2_{\text{AC},x} \right. \\ &\quad \left. + p_{1,k,x} \cdot i_{\text{AC},x}\right) \cdot \frac{1}{U^*_{\text{mod}}} \\ &= 0\,\text{W}\,\text{V}^{-1}\end{aligned} \tag{14}$$

Gradient of loss derivative: Between the discontinuities of (14), the function is linear, since it only depends on the CM voltage u_{cm}. To calculate the derivative's roots analytically, the second derivative is necessary. It is calculated as shown in (15). The result is strictly positive since $2p_{2,k,x} > 0$ holds for the fitting parameters shown in Table 3.

$$\frac{\mathrm{d}^2 P_{\text{losses,total}}}{\mathrm{d}u^2_{\text{cm}}} = \sum_x \frac{2p_{2,k,x}i^2_{\text{AC},x}}{U^2_{\text{mod}}} \tag{15}$$

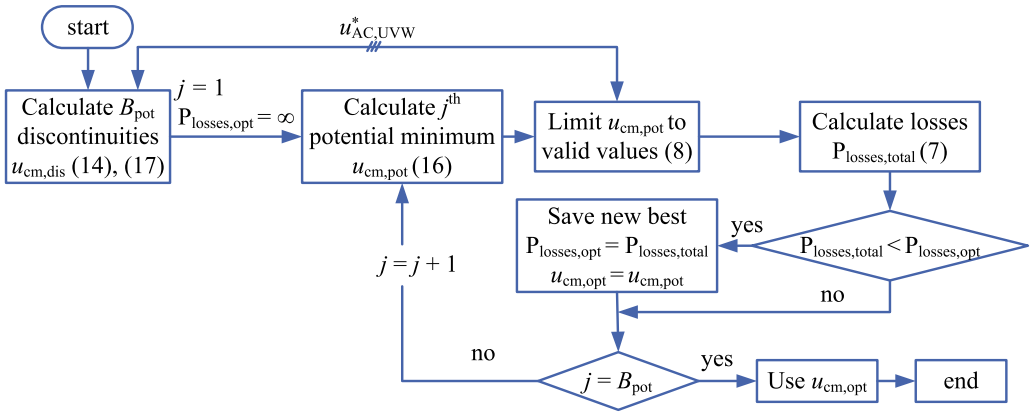

Fig. 8. Flowchart of the minimization process.

Calculating potential local minima: To calculate the CM voltage of the discontinuities $u_{cm,dis}$ and its respective function value $\frac{dP_{losses,total}}{du_{cm}}(u_{cm,dis})$, (14) is used. With the function value and its local gradient, calculated with (15), the root of this piecewise defined function can be calculated with (16). As a result, the CM voltage of a potential minimum $u_{cm,pot}$ is calculated. Evaluating (7) at this CM voltage $u_{cm,pot}$ and comparing the results with all potential minima, including the maximum and the minimum possible CM voltage, leads to the global minimum.

$$u_{cm,pot} = u_{cm,dis} - \frac{\frac{dP_{losses,total}}{du_{cm}}(u_{cm,dis})}{\frac{d^2P_{losses,total}}{du_{cm}^2}(u_{cm,dis})} \tag{16}$$

Amount of potential minima: An upper bound of the amount of potential local minima B_{pot} can be calculated according to (17). It is proportional to the amount of modules per phase M_{ph}. The SST controller has to be capable of calculating and comparing all of these B_{pot} potential local minima within one control cycle to be deterministic. However, in reality the absolute number of local minima is smaller, since the valid CM voltage range is reduced because of the actual voltage setpoints of the superimposed current controllers.

$$B_{pot} = 3 \cdot (2M_{ph} + 1) \tag{17}$$

Example of derivative at mentioned OP: In Fig. 9 the overall derivative of the mentioned OP is shown, revealing two local minima of $P_{losses,total}$ shown in Fig. 7, i.e. $\frac{dP_{losses,total}}{du_{cm}} = 0\,\mathrm{W\,V^{-1}}$. However, the global minimum is found at the minimal CM voltage $u_{cm} \approx 4.8\,\mathrm{V}$. As a result, the power losses at this particular OP can be reduced from $P_{losses,total,old} \approx 660\,\mathrm{W}$ to $P_{losses,total,new} \approx 566\,\mathrm{W}$. The optimized OP is highlighted with the orange circles in Fig. 7.

3.5. Alternative DAB setpoint distribution

If the constant voltage mode of all modules, explained in Section 3.2, is dropped, and all modules receive equal setpoints, the shape of the resulting phase loss function will change. Consequently, the overall SST loss function will also differ. Nevertheless, utilizing the CM voltage remains a valid and effective approach for minimizing the total losses of the SST and the same algorithm can be used.

4. Test bench

This section presents the hardware setup of a single SM, and the SST. Furthermore, the general control architecture of the SST is explained. On top of that, the schematics of the experimental setups used to obtain the loss measurements for both the single DAB and the complete SST is illustrated.

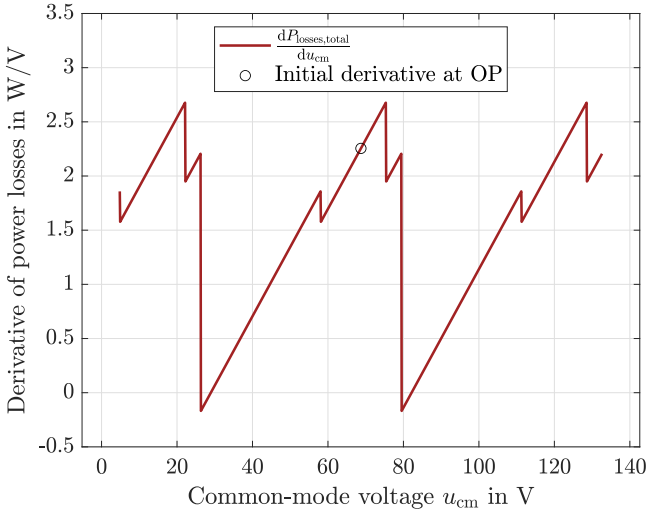

Fig. 9. Derivative of total power losses $\frac{dP_{losses,total}}{dU\mathrm{cm}}$ with respect to the residual CM voltage u_{cm} range ($\hat{u}_{AC} = 325\,\mathrm{V}$, $\hat{i}_{AC} = 40\,\mathrm{A}$, $\varphi = 65°$, $\gamma = 25°$).

4.1. Hardware setup

Fig. 10 shows a picture of a single power module of the SST. It consists of the DAB stage, the CHB cell, a plug-in field-programmable gate array (FPGA) controller board, and current, voltage, and temperature measurement systems. The SST is controlled by a modular signal processing platform that incorporates two ARM-core processors and a high-performance FPGA (Schmitz-Rode, Stefanski, Schwendemann, Decker, Mersche, Kiehnle, et al., 2022). Both the calculated results and the measurements shown in Section 5 are generated with the system, listed in Table 2.

The module parameters are derived from an unscaled system intended for a MV application. An SST connected to the MV AC grid must remain operational under the expected static grid overvoltage of $\lambda_{SOV} = 1.1$, as specified in VDE-AR-N 4110 (VDE, 2023). Given $M_{ph} = 6$ modules per phase and the grid parameters listed in Table 2, the minimum required cell voltage is $U_{mod,min} = 51.9\,\mathrm{V}$, as calculated from (18). Using a transformer with a winding ratio of $n_t = 14.11$ and a primary-side DC voltage of $U_p = 750\,\mathrm{V}$, unity gain in the DAB is achieved at $U^*_{mod} = 53.2\,\mathrm{V}$. Since this OP is well-suited for Single Phase Shift modulation, explained in Doncker et al. (1991), and also satisfies the minimum voltage requirement from (18), it is selected as the module setpoint voltage.

$$U_{mod,min} = \frac{U_{grid}\lambda_{SOV}}{\sqrt{2}M_{ph}} \tag{18}$$

Table 2
System specification.

Parameter	Symbol	Value
Modules per phase	M_{ph}	6
Module voltage	U^*_{mod}	53.2 V
Primary/ DC grid voltage	U_p	750 V
Transformer winding ratio	n_t	14.11:1
DAB/CHB switching frequency	f_{DAB}, f_{CHB}	50 kHz
Maximum phase current	$I_{AC,max}$	60 A
Nominal power of DAB	P_{DAB}	2.5 kW
Nominal power of SST	P_{SST}	45 kW
System control frequency	f_{sys}	50 kHz
AC grid voltage	U_{grid}	400 V
Grid frequency	f_{grid}	50 Hz
Grid filter	L_{grid}	1 mH

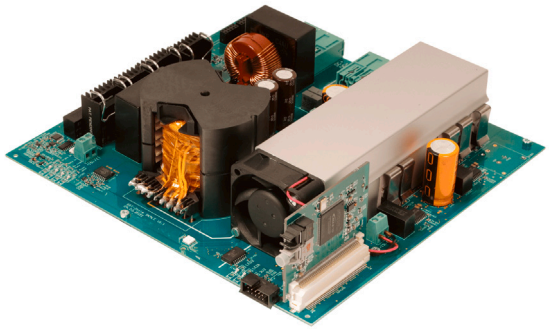

Fig. 10. Hardware of the power module with a DAB stage and the CHB cell.

4.2. Control structure

The control structure of the SST is shown in Fig. 11. It is divided into the AC-side current control (green) and the module voltage control (red). The AC-side grid current is controlled using two PI-controllers operating in a rotating dq-reference frame. This approach allows for independent regulation of the converter's active and reactive power. To enhance control performance and reduce interference, decoupling of the control loops is implemented with the factor $D = 2\pi f_{grid} L_{grid}$. The controllers are tuned using the magnitude optimum method to ensure a fast and well-damped response to setpoint changes (Lutz & Wendt, 1998). Additionally, the measured and transformed voltages of the grid U_d and U_q are added to the output of the controllers as direct feed forward control. The resulting SST voltage setpoints U^*_d and U^*_q are transformed back into the corresponding three-phase voltage references $u^*_{AC,UVW}$. These serve as the basis for the calculation of the optimal CM voltage $u_{cm,opt}$, as described in Section 3. After executing the proposed method, the optimized CM voltage is added to the initial voltage references to obtain the loss-minimizing setpoints $u_{AC,UVW,opt}$.

The respective duty cycles $a_{x,m}$ for the individual modules $m = \{1, 2, \dots, M_{ph}\}$ of phase x are generated by the CHB Scheduler. In each phase, $a_{fix,x}$ modules operate with a fixed positive or negative active state, while one module is assigned a duty cycle $a_{dc,x}$. As the applied CM voltage optimization relies on VSPWM, the duty cycles $a_{x,m}$ are determined accordingly. In the absence of additional constraints, the assignment of $a_{x,m}$ can be exploited to balance the thermal and electrical stress among modules. This is achieved through periodic cycling of the active modules (Angulo et al., 2007), as implemented in this work. Alternatively, dedicated power routing strategies can be used to enhance the converter's lifetime, as proposed in Ko et al. (2017).

The module voltage control maintains the individual module voltages $U_{mod,x,m}$ close to the setpoint U^*_{mod} using a two-layer hierarchical approach. In the first layer, instantaneous oscillating feed forward currents $i_{ff,x,m}$ are computed based on the AC phase currents $i_{AC,x}$ and the duty cycles $a_{x,m}$ of the respective modules. This feed forward control compensates for the inherent phase-to-phase power oscillations characteristic of the CHB topology, thereby reducing the burden on the following voltage balancing control loop (Menger, Merz, Zieglmaier, Schwendemann, & Hiller, 2023).

However, as this layer neglects losses and non-linearities of the DAB, a second control layer is introduced to ensure accurate voltage regulation. In this layer, each SM is equipped with an individual module voltage PI-controller, tuned according to the symmetric optimum criterion (Lutz & Wendt, 1998). The controller calculates the required balancing current $i_{bal,x,m}$, which is added to the feed forward current to form the final module current reference $i^*_{mod,x,m}$. Due to the high efficiency of the DABs, the balancing current is typically much smaller than the feed forward current $\left(i_{bal,x,m} \ll i^*_{mod,x,m}\right)$. Consequently, the deviation in actual power losses from the estimated values of the optimizer is negligible.

4.3. Power loss measurement test setup

Fig. 12 shows the test setup used to measure the losses of a single SM. A test procedure implemented in MATLAB and executed on a PC, controls the two voltage sources that provide the input and output voltages, U^*_p and U^*_{mod}, and the primary-side current I_p, respectively. Additionally, it sends the current setpoints i^*_{mod} to the DAB and triggers the power meter, which records all relevant values. During these measurements, the CHB is operated in a constant positive switching state. The corresponding dataset is available in Merz et al. (2025b). The test setup for evaluating the losses of the complete SST is depicted in Fig. 13. A voltage source on the left-hand side supplies a constant input voltage U_p. On the AC-side, the SST is connected to a filter L_{grid} and interfaced with the institute's 400 V laboratory grid. Another MATLAB-based test procedure generates the SST's current setpoints I^*_d and I^*_q. It also specifies whether the optimization algorithm or the reference mode is active. After the settling time of the phase currents, the power meter is triggered to capture the electrical input and output data. The associated measurements are documented in Merz et al. (2025c).

5. Results

To verify the experimental results, the loss function and the equations presented in Section 3 are implemented in MATLAB. The same equations are also modeled as a signal flow diagram in MATLAB/ Simulink. From this model, FPGA-specific hardware description language (HDL) code is generated and deployed on the control platform. Mentioned FPGA operates at a clock frequency of $f_{FPGA} = 150$ MHz.

5.1. Calculation results

The results of the fitting process for the values shown in Fig. 4 are presented in Table 3. As a reference for the proposed optimization method, indicated with the index opt, the total losses $P_{losses,total}$ and the resulting CM voltage u_{cm} are considered. These are compared to the modulation scheme with a maximized output voltage range (triangular CM voltage shape), indicated by the index tri. It is important to note that the proposed method does not restrict the maximum output voltage. To verify the calculation results of the loss-optimized method, a time-consuming, not real-time capable brute-force algorithm is implemented in MATLAB, indicated by the index brute. The OP shown in Figs. 14 to 16, is $\hat{U}_{AC} = 325$ V, $\hat{I}_{AC} = 40$ A, $\varphi = 0°$. Fig. 14 shows that the analytical and the brute-force approach yield the same results for the CM voltage, which differ from the triangular shape. The black lines indicate the minimum and maximum CM voltage range for this setup and grid voltages. It can be observed that the optimized CM voltage u_{cm} only matches the reference values at grid angles close to integer multiples of $\gamma = 60°$.

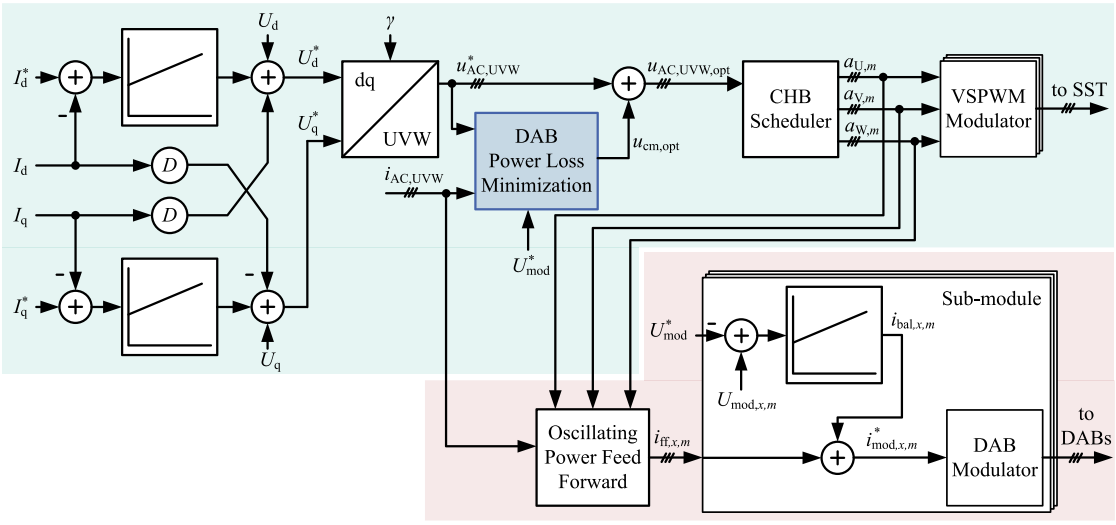

Fig. 11. Employed control structure for the SST with AC-side current control (green) and DC-link voltage control (red). The proposed Power Loss Minimization Algorithm (blue) is integrated into the AC-side current control. Connections consisting of more than one signal are indicated by the three dashes.

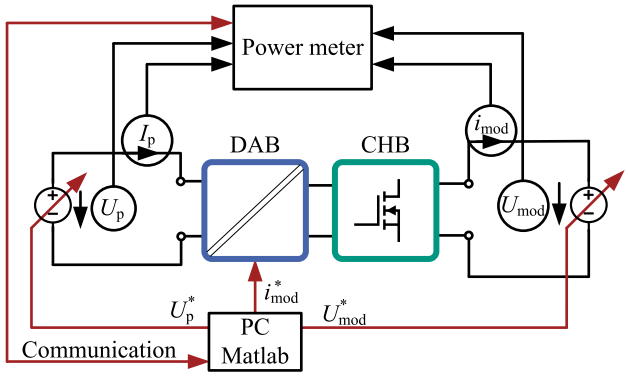

Fig. 12. Test setup to measure the efficiency of an SM to extract the data for the power loss function.

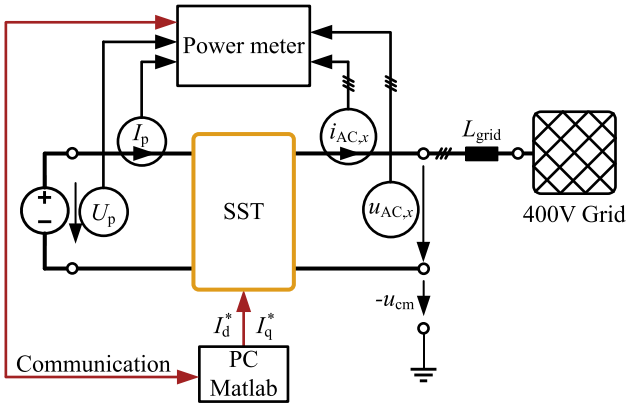

Fig. 13. Test setup to measure the losses of the SST during operation. Connections consisting of more than one signal are indicated by the three dashes.

The resulting phase voltages of the converter are shown in Fig. 15. Although these phase-to-neutral voltages do not resemble a sinusoidal waveform, they are valid. The resulting line-to-line voltage between two phases, which is relevant for controlling the sinusoidal currents, is sinusoidal and shown in red.

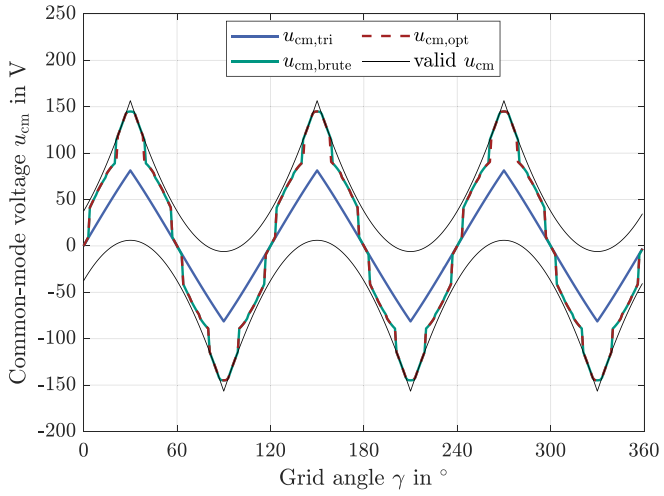

Fig. 14. Comparison of the valid CM voltage u_{cm} for a grid period.

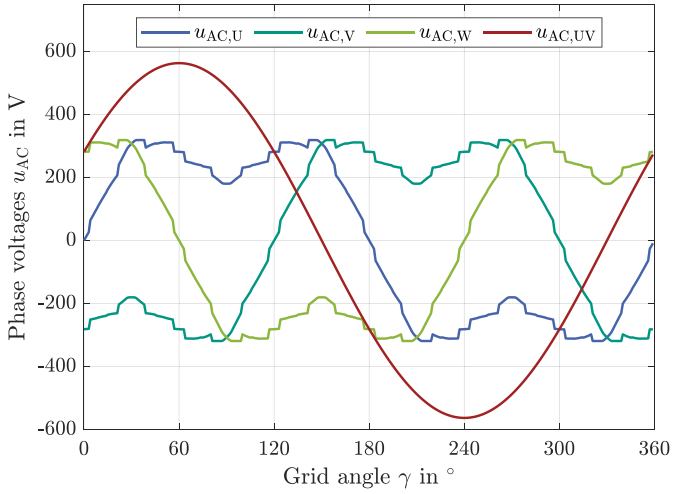

Fig. 15. Resulting calculated, switching period average SST output phase voltages with loss optimized CM voltage. Resulting sinusoidal line-to-line voltage $u_{AC,UV}$ between phases U and V.

Table 3
Fitting parameters specification.

Parameter	Value
$p_{2,\mathrm{pos}}$	40.8 mW A^{-2}
$p_{1,\mathrm{pos}}$	−61.9 mW A^{-1}
$p_{2,\mathrm{neg}}$	29.5 mW A^{-2}
$p_{1,\mathrm{neg}}$	60.4 mW A^{-1}
p_0	15.3 W

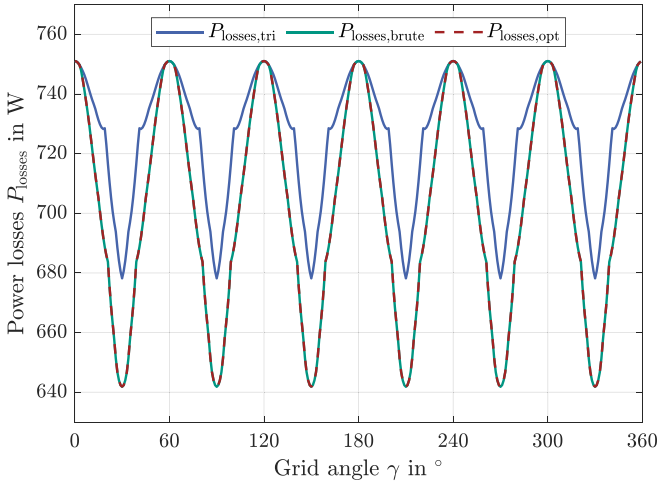

Fig. 16. Comparison of the resulting losses P_{losses} during a grid period.

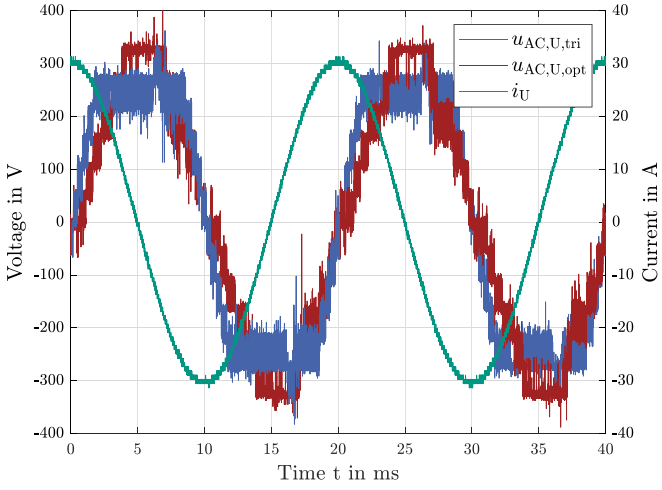

Fig. 17. Measured reference (blue) and optimized (red) voltage and current (green) of phase U with $I_{\mathrm{d}} = 0\,\mathrm{A}$ and $I_{\mathrm{q}} = 30\,\mathrm{A}$.

Fig. 16 shows the calculated power losses P_{losses} for the different calculation methods. It is evident that when the CM voltages u_{cm} are equal, the power losses are equal, too. Hence, the loss-optimized method achieves OPs that result in power losses equal to or lower than those of the reference method. Consequently, the overall efficiency of the DAB stage is improved. As a result of optimizing each OP of the SST, the average power losses over an entire grid period are reduced, thereby improving the system's overall efficiency.

5.2. Experimental results

To evaluate the actual power loss reduction, measurements with different setpoint currents for I_{d} and I_{q} are conducted on the grid. As an example Fig. 17 shows the resulting voltage and current of phase U for an OP of $I_{\mathrm{d}} = 0\,\mathrm{A}$ and $I_{\mathrm{q}} = 30\,\mathrm{A}$ (Merz et al., 2025a). As previously mentioned, the sinusoidal shape of the phase current is not affected by the proposed scheme. However, due to the different CM voltage, the phase voltage takes on a different form.

The loss reduction over the full operation range of the SST is shown in Fig. 18(a) (Merz et al., 2025c). Additionally, a calculation with the same setpoints for voltages and currents is performed to compare the results and assess the accuracy of the model. The calculated results are presented in Fig. 18(b).

Both the measurements and the calculations show high accordance with a reduction in power losses of more than 160 W. However, there are some deviations at low current setpoints which can be caused by the accuracy of the measurement system and harmonic voltages of the grid used in the experiments. The reason for the asymmetric behavior with high positive and high negative currents in the q-direction is due to the effect of the voltage drop across the filter inductance L_{grid}. A positive q-current leads to a decrease in the required voltage in the d-direction, while a negative q-current increases the d-voltage setpoint. Due to this fact, less voltage is necessary to control the current, resulting in a wider range of valid values of the CM voltage u_{cm}. Fig. 18 shows that the power losses of the DAB stages can be significantly reduced in nearly every OP. Fig. 19 shows the relative reduction of the power losses for the calculation with a maximum relative reduction of 20 %.

5.3. Discussion

The proposed optimization method offers several strengths that make it both practical and widely applicable in SST systems. A major advantage is its independence from existing control functions: it does not interfere with modulation strategies or active/reactive power control loops. This allows seamless integration into established SST control architectures, while enabling dynamic adaptation to changing operating conditions such as load steps or grid fluctuations. Additionally, the method is compatible with thermal balancing strategies, as it does not rely on uniform power sharing between modules. This enables the system to prioritize cooler modules through temperature-based selection without compromising electrical loss minimization. The loss model itself is based on experimentally measured data from an actual DAB module rather than idealized assumptions. As a result, the derived polynomial model accurately reflects the real loss behavior and supports effective reduction of total system losses. The method is specifically designed for real-time execution and can be implemented on embedded control platforms. Although the computational complexity of evaluating a single candidate solution is low, the total burden increases with the number of modules per phase M_{ph}. Therefore, a suitable trade-off must be found by considering the available computational resources, control frequency, and the amount of SMs.

Despite its strengths, several limitations should be acknowledged. The effectiveness of the loss minimization strongly depends on the accuracy of the initial loss characterization. Over time, device parameters may drift due to aging, temperature variations, or environmental influences, potentially reducing the accuracy of the loss model. To cope with this issue, adaption of the fitting parameters with online loss estimation will be investigated in future work. Furthermore, accurately fitting the loss functions of MV, high-power systems may require higher-order polynomials or a loss function split into more than two intervals. Therefore, more efficient methods for computing the global minimum are the subject of future research. In addition, the use of the CM voltage is subject to practical limitations. While the optimization focuses solely on minimizing electrical losses, it does not explicitly account for insulation stress or electromagnetic interference (EMI) effects. These factors may constrain the allowable range of the CM voltage in practical implementations and warrant further investigation. Lastly, the experimental validation is based on a 45 kW LV prototype. Although functionally

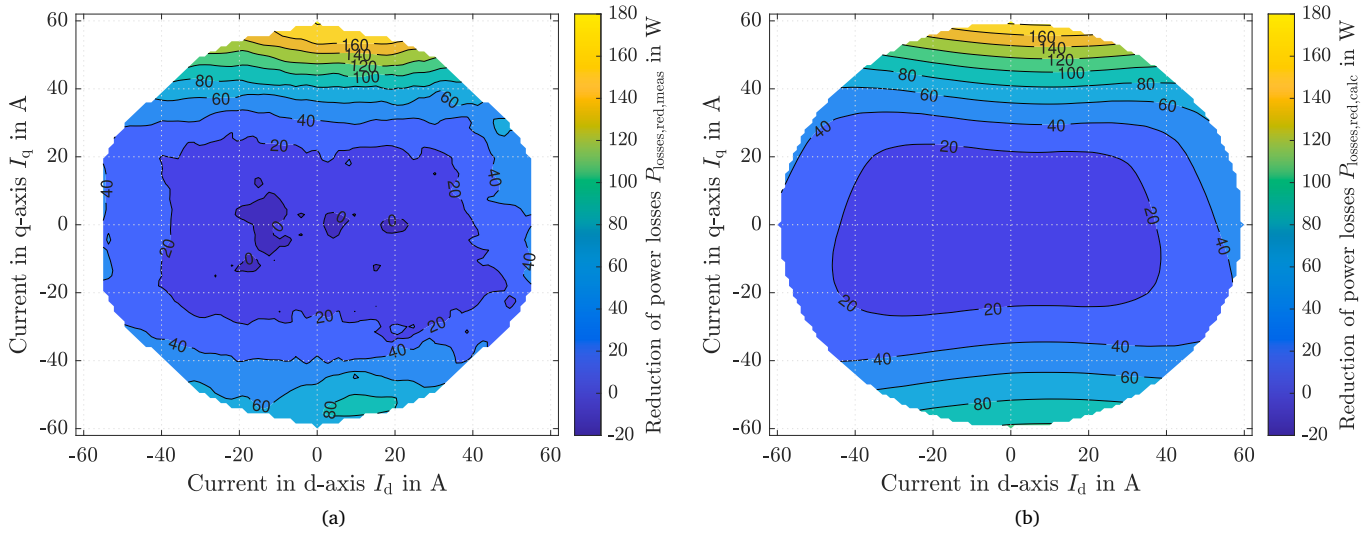

Fig. 18. Reduction of (a) measured power losses $P_{losses,red,meas} = P_{losses,tri,meas} - P_{losses,opt,meas}$ and (b) calculated power losses $P_{losses,red,calc} = P_{losses,tri,calc} - P_{losses,opt,calc}$ at different OP for the loss-optimized method in contrast to the reference.

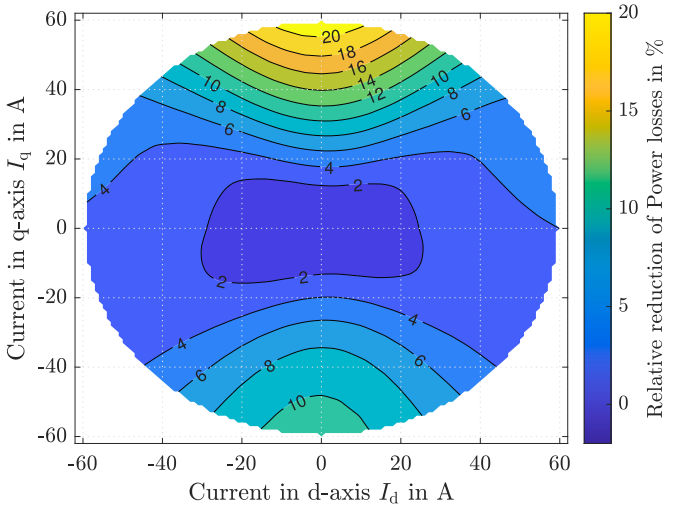

Fig. 19. Calculated relative reduction of the losses of the DAB stages.

representative of typical systems, larger MV grid-connected installations may impose stricter requirements regarding EMI compliance, reliability, and fault tolerance. Consequently, future work will focus on demonstrations using scaled-up DAB prototypes to evaluate the method's applicability in MV SSTs.

6. Conclusion

This work presents a detailed approach to minimize the sum of power losses across all DAB modules of an SST, while being real-time capable. The method is based on a mathematical model of the power losses for a single DAB module. After combining these into a model for a phase and then for the entire SST, the model is used to estimate the total power losses of all 18 DAB modules of the SST prototype. These losses are then minimized by leveraging the residual DoF in the CM voltage u_{cm} of the three-phase system. Calculations demonstrate the resulting CM voltage and the reduced losses of the entire converter by up to 20 %. Experiments validate these calculated results with high accuracy. Further research will explore alternative modulation schemes for the SST, generalize the approach for unscaled high-power DABs, optimize the distribution of power transferred by the DABs, and incorporate the required SM redundancy of SSTs.

CRediT authorship contribution statement

Tobias Merz: Writing – review & editing, Writing – original draft, Visualization, Supervision, Software, Project administration, Methodology, Investigation, Formal analysis, Conceptualization. **Nikolas Menger:** Writing – review & editing, Validation, Supervision, Software, Resources, Methodology, Investigation, Formal analysis, Conceptualization. **Max-Emanuel Siegemund:** Visualization, Validation, Software, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Rüdiger Schwendemann:** Writing – review & editing, Supervision, Project administration. **Marc Hiller:** Supervision, Project administration, Funding acquisition.

Declaration of Generative AI and AI-assisted technologies in the writing process

During the preparation of this work the authors used ChatGPT by OpenAI in order to improve grammar and readability. After using this tool, the authors reviewed and edited the content as needed and take full responsibility for the content of the published article.

Funding

This research did not receive any specific grant from funding agencies in the public, commercial, or not-for-profit sectors.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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