

# **Optic–Electronic–Optic Interferometer for Coherent Add–Drop Multiplexing**

Zur Erlangung des akademischen Grades eines

**DOKTORS DER INGENIEURWISSENSCHAFTEN  
(Dr.-Ing.)**

von der KIT-Fakultät für  
Elektrotechnik und Informationstechnik des  
Karlsruher Instituts für Technologie (KIT)

angenommene

**DISSERTATION**

von

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geb. in Dhaka, Bangladesch

Tag der mündlichen Prüfung:

09.10.2025

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# Kurzfassung

Das schnelle Wachstum des globalen Internetverkehrs, getrieben durch Cloud-Services, 5G und die Internet der Dinge (IoT), erhöht kontinuierlich die Anforderungen an die Kapazität und die Flexibilität optischer Kommunikationsnetze. Rekonfigurierbare optische Add-Drop-Multiplexer (ROADM) spielen dabei eine zentrale Rolle, da sie eine dynamische Kanalnutzung ermöglichen. Der aktuelle Stand der Technik, basierend auf wellenlängenselektiven Schaltern (Wavelength-Selective Switch, WSS), ist in der Regel auf eine Auflösung von 8–10 GHz begrenzt, was den Einsatz von Schutzbändern vergleichbarer Breite zwischen den Kanälen erforderlich macht. Diese Einschränkung verhindert den Einsatz in neuen Szenarien bei denen sehr schmalen Schutzbänder oder spektral überlappende Kanäle genutzt werden und begrenzt damit sowohl die Skalierbarkeit als auch die effiziente Spektrumnutzung. Diese Limitierungen motivieren die Erforschung hybrider Architekturen, die die große Bandbreite optischer Systeme mit der Flexibilität digitaler Signalverarbeitung (DSP) kombinieren.

In dieser Dissertation wird eine neuartige opto-elektronisch-optische (OEO) Interferometer-Architektur für kohärentes Add-Drop-Multiplexing vorgestellt, die eine präzise Manipulation optischer Wellenformen ermöglicht. Die Arbeit präsentiert die erste experimentelle Demonstration eines solchen OEO-Interferometers, einschließlich sowohl einkanaliger als auch mehrkanaliger WDM-Betriebsmodi mit eng benachbarten Kanälen. Wichtige Beiträge dieser Arbeit sind die Entwicklung eines allgemeinen Frameworks für die OEO-Architektur, die Implementierung von Echtzeit-DSP- und Phasenregelungs-Algorithmen sowie die Evaluierung teilintegrierter Interferometer-Module. Die erzielten Ergebnisse

belegen die Realisierbarkeit eines OEO-basierten kohärenten Add-Drop-Multiplexers, liefern neue Erkenntnisse zu Leistungsfähigkeit und Skalierbarkeit und eröffnen neue Perspektiven für flexiblere und effizientere optische Netze.

*Kapitel 1* führt in die Motivation und den Hintergrund dieser Arbeit ein und gibt einen Überblick über den Aufbau der Dissertation.

*Kapitel 2* erläutert die Grundlagen des OEO-Interferometers, einschließlich Funktionsprinzip, Zeitverzögerungs- und Phasenangepassungsbedingungen sowie die Implementierung eines dither-basierten, endlosen Phasenregelungssystems.

*Kapitel 3* beschreibt die in dieser Arbeit verwendeten DSP-Algorithmen. Neben allgemeinen Aufgaben der Signaldetektion werden dabei die spezifischen DSP-Methoden für kohärentes Add-Drop-Multiplexing behandelt. Zudem werden Anpassungen für die Echtzeitausführung und das parallele Eingangssampling diskutiert.

*Kapitel 4* beschreibt die experimentellen Implementierungen des OEO-Interferometers auf progressive Weise – von ersten Machbarkeitsstudie bis hin zu erweiterten Experimenten mit eng benachbarten WDM-Kanälen. Dazu gehören auch Ergebnisse mit einem teilintegrierten Modul.

*Kapitel 5* fasst die wesentlichen Beiträge dieser Arbeit zusammen und gibt einen Ausblick auf offene Forschungsfragen, mögliche Verbesserungen des OEO-Interferometers sowie Perspektiven für zukünftige Entwicklungen.

# Preface

The rapid growth of global data traffic driven by cloud services, 5G, and the Internet of Things continues to push fiber-optic communication networks toward higher capacity and flexibility. Reconfigurable optical add–drop multiplexing (ROADM) plays a central role in enabling dynamic channel management to meet these demands. However, current state-of-the-art wavelength-selective switch (WSS) based systems are typically limited to a resolution of 8–10 GHz, which requires guard bands of comparable width between channels. This constraint makes them unsuitable for emerging scenarios with narrow guard bands or spectrally overlapping channels, thereby restricting scalability and efficient spectral utilization. These limitations motivate the exploration of hybrid architectures that combine the high spectral capacity of optical systems with the adaptability of digital signal processing (DSP).

This thesis introduces a novel optic–electronic–optic (OEO) interferometer architecture for coherent add–drop multiplexing, enabling precise manipulation of optical waveforms. The research presents the first experimental demonstration of such an OEO interferometer, including both single-channel and multi-channel WDM operation with closely spaced channels. Key contributions include the development of a generalized framework for the OEO architecture, the implementation of real-time DSP and phase-control algorithms, and the evaluation of partially integrated interferometer modules. These results demonstrate the feasibility of OEO-based coherent add–drop multiplexing, provide new insights into performance and scalability, and pave the way for more flexible and efficient optical networks.

*Chapter 1* introduces the motivation and background of this work, followed by an outline of the thesis organization.

*Chapter 2* explains the fundamentals of the OEO interferometer, including its principle of operation, time-delay and phase-matching constraints, and the implementation of a dither-based endless phase-control system.

*Chapter 3* presents the DSP algorithms employed in this work, covering both general signal recovery tasks and the specific DSP methods required for coherent add-drop operation. Adaptations for real-time execution and parallel input samples are also discussed.

*Chapter 4* describes the experimental implementations of the OEO interferometer in a progressive manner, ranging from proof-of-concept setups to advanced experiments with narrowly spaced WDM channels, including demonstrations with a partially integrated module.

*Chapter 5* concludes the thesis by summarizing the main contributions and providing an outlook that highlights open research questions, potential improvements to the OEO interferometer, and opportunities for future developments.

# Achievements of the Present Work

This thesis demonstrates a novel optic–electronic–optic (OEO) interferometer for coherent add–drop multiplexing. The concept relies on converting optical waveforms into the electronic domain, applying signal processing, and subsequently remodulating them back to the optical domain with preserved phase information. This approach enables flexible channel manipulation and improved spectral efficiency beyond the limits of conventional all-optical or all-electronic systems.

The following list summarizes the main achievements of the present work:

**First experimental realization of an OEO interferometer:** To the best of our knowledge, this thesis presents the first laboratory demonstration of an OEO interferometer capable of selectively removing and reinserting coherent optical signals while preserving both phase information and signal integrity. The concept is validated in a stepwise manner, progressing from single-channel proof-of-concept experiments to advanced wavelength-division multiplexing (WDM) scenarios. Across all experiments, a channel suppression of approximately 18 dB is achieved for QPSK modulation. In the final demonstration, three WDM channels, each with a 2 GBd QPSK signal and 2.9 GHz channel spacing, were processed, exhibiting only a modest OSNR penalty of 0.4–0.5 dB at a bit error ratio of  $10^{-4}$ .

**Experimental validation of a partially integrated OEO module:** In collaboration with Fraunhofer HHI, a photonic–integrated-circuit (PIC) of the OEO interferometer was realized. This thesis contributes to the experimental validation of the integrated module, confirming the feasibility of OEO-based add–drop operation in a compact platform.

**Comprehensive system architecture and DSP adaptation for OEO interferometers:** The dissertation demonstrates a comprehensive analysis of the OEO architecture, including time-delay constraints and phase-matching requirements. Furthermore, established DSP methods for signal recovery and synchronization are adapted to the specific requirements of the OEO architecture, supporting real-time operation on a field-programmable gate array (FPGA) with parallel input processing.

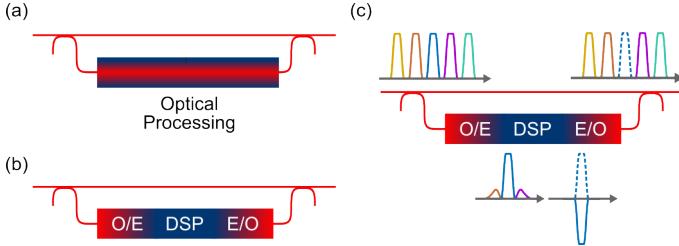
**Endless phase stabilization using dither-based control:** A robust, endless phase control system based on dithering techniques is developed and validated, ensuring long-term phase stability of the OEO interferometer under practical conditions.

# 1 Introduction

The relentless growth of global data traffic, fueled by cloud computing, 5G/6G networks, and emerging AI workloads, continues to challenge the limits of optical transport. To keep pace, coherent optical transceivers have been enhanced by advances in high-speed data converters, electro-optic modulators, narrow-linewidth lasers, and real-time digital signal processors, leading to significant improvements in bandwidth, spectral efficiency, and cost-effectiveness.

Despite these gains, purely electronic processing faces fundamental bandwidth and sampling-rate limits, whereas purely optical processing lacks programmability. This has motivated increasing interest in hybrid optical–electronic architectures, which combine the bandwidth and parallelism of optics with the flexibility and adaptability of digital signal processing (DSP). As an example, in recent years, a growing set of photonic-assisted processing methods has been reported to overcome the intrinsic bandwidth bottlenecks of conventional all-electronic systems, enabling high-speed waveform synthesis, efficient spectral multiplexing, and wideband optical sampling [1–4].

In this context, this thesis investigates the optic–electronic–optic (OEO) interferometer architecture, which enables dynamic and flexible manipulation of optical waveforms. In this scheme, the optical signal is first converted into the electrical domain, processed through DSP, and reconverted into the optical domain, while preserving both phase and polarization coherence, as illustrated in Fig. 1.1(b). Conventional interferometers, based on transparent optical paths (Fig. 1.1(a)), are typically limited to basic functions such as phase shifts and time delays, enabling applications such as electro-optic modulators [5] and differential phase-shift-keying (DPSK) decoders [6]. In contrast, the OEO approach provides significantly



**Fig. 1.1:** Comparison of (a) a conventional interferometer with an optically transparent processing path, (b) an optic–electronic–optic (OEO) interferometer with a digital electronic processing path, and (c) the selective insertion and removal of channels in ultra-dense WDM systems using the OEO architecture.

greater functional flexibility, enabling advanced waveform control. This capability makes it particularly suitable for coherent add–drop multiplexing, allowing individual channels from a multi-channel optical signal to be selectively extracted (dropped) and reinserted (added) at the same spectral position, as conceptually illustrated for an ultra-dense WDM scenario in Fig. 1.1(c).

While the OEO interferometer offers the flexibility to perform coherent add–drop operations even in ultra-dense WDM scenarios, conventional wavelength-selective-switch (WSS) based systems are constrained by finite filter resolution. With a typical resolution of 8–10 GHz, these systems require comparable guard bands between adjacent channels, limiting their effectiveness in spectrally compact multiplexing formats where channels are narrowly separated or overlapping [7]. A notable example is multicarrier offset quadrature amplitude modulation (OQAM), which achieves high spectral efficiency through orthogonal subchannels with overlapping spectra [8–10]. A brief discussion is provided in Appendix B. Under such conditions, conventional multiplexers struggle to achieve precise channel separation without introducing signal degradation.

The OEO-interferometric approach overcomes this limitation by employing coherent detection, DSP-based channel separation, and electro-optic remodulation, enabling operation at baud-rate-spaced or even spectrally overlapping channel configurations. Recent advances in interferometric add–drop multiplexing have also explored alternative strategies, such as all-optical processing via a gated

fast Fourier transform (FFT) [11] or coherent detection followed by frequency conversion in highly nonlinear fiber [12]. While these methods demonstrate the feasibility of interferometric add–drop multiplexing, they remain constrained by hardware complexity, sensitivity to optical path stability, or reliance on nonlinear processes. By contrast, the OEO interferometer provides a more flexible and digitally assisted solution, building on its original proposal in [13, 14] and subsequent numerical studies in [15].

To extend this concept, this work presents the first experimental demonstration of the OEO interferometer as a coherent add–drop multiplexer. The study establishes a generalized system architecture, develops DSP algorithms and phase-control loops for real-time operation on a field-programmable gate array (FPGA), and validates performance in single- and multi-channel WDM systems. The feasibility of integrated solutions is further examined through experimental validation of a partially integrated interferometer module. The results are supported by bit-error ratio (BER) measurements, spectral analysis, and extinction ratio assessments. Collectively, these findings demonstrate that OEO-based processing can bridge the optical and electronic domains, enabling flexible, high-performance coherent multiplexing under dense spectral conditions, and paving the way for next-generation ROADM<sup>s</sup> with enhanced spectral efficiency. Beyond optical networking, OEO-interferometric superposition may extend to optical computing applications, such as coherent Ising machines, where phase-coherent feedback is essential [16].

The remainder of this thesis is organized as follows. Chapter 2 introduces the principles of the OEO interferometer, addressing its operating constraints and phase-control requirements. Chapter 3 presents the digital signal processing algorithms developed for coherent add–drop operation, with emphasis on their adaptation to real-time FPGA implementation. Chapter 4 reports the experimental demonstrations, progressing from proof-of-concept systems to advanced WDM scenarios and integrated-module validation. Finally, Chapter 5 summarizes the key contributions and discusses directions for future work.

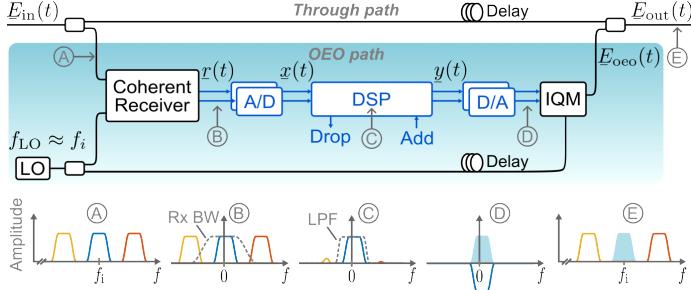


# 2 Fundamentals of Optic-Electronic-Optic Interferometers

This chapter outlines the theoretical principles and technical aspects of optic–electronic–optic (OEO) interferometers, particularly in their application as optical add–drop multiplexers. After introducing the operation principle and the necessary digital signal processing (DSP) functions for coherent reception, key system impairments are discussed. The final section highlights the critical role of optical phase stabilization and presents a dither-based approach as a practical method to achieve robust and reliable operation.

## 2.1 Concept

The core components of an OEO Mach-Zehnder interferometer (MZI) are depicted in Fig. 2.1. In contrast to conventional MZIs, one arm of the OEO configuration performs full optic-to-electronic-to-optic conversion. The lower path in the structure, therefore, includes coherent reception, DSP, and in-phase and quadrature (I/Q) modulation. Through the use of the same laser as a local oscillator (LO) for coherent reception and remodulation, full optical field coherence is maintained across the entire processing path. The insets show characteristic amplitude spectra at various stages of the signal path, with the exemplary objective of replacing an optical channel at carrier frequency  $f_i$  with a different signal at the same frequency while keeping the neighboring channels unaffected.



**Fig. 2.1:** Illustration of the optic–electronic–optic (OEO) interferometer architecture with coherent reception, DSP, and I/Q modulation in the lower processing path. Insets depict representative amplitude spectra at key stages: (A) input WDM signal, (B) baseband after coherent reception, (C) after digital lowpass filtering (LPF), (D) regenerated electrical signal including the new waveform (shaded) and the inverted original (solid), and (E) final optical signal after the add–drop operation. The bandwidths of the receiver and LPF are indicated by gray dashed lines.

Consider a WDM signal input to the OEO interferometer, with the optical field expressed as

$$E_{\text{in}}(t) = \sum_k a_k(t) e^{j[2\pi f_k t + \phi_k(t)]}$$

where  $a_k(t)$  represents the information-carrying complex amplitude of channel  $k$ ,  $f_k$  denotes its carrier frequency, and  $\phi_k(t)$  accounts for the associated laser phase noise. At the input of the interferometer, this signal is split into an optically transparent upper path and an optically opaque lower path. These are referred to as the *through path* and the *OEO path*, respectively. In the OEO path, the frequency of a free-running local oscillator (LO) laser is tuned to channel  $i$  of the WDM system, i.e.,  $f_{\text{LO}} \approx f_i$ , and a coherent receiver is used to detect the I/Q components of the input optical field as

$$r(t) \propto \left( E_{\text{in}}(t) e^{-j[2\pi f_{\text{LO}} t + \phi_{\text{LO}}(t)]} \right) * h_{\text{crx}}(t), \quad (2.1)$$

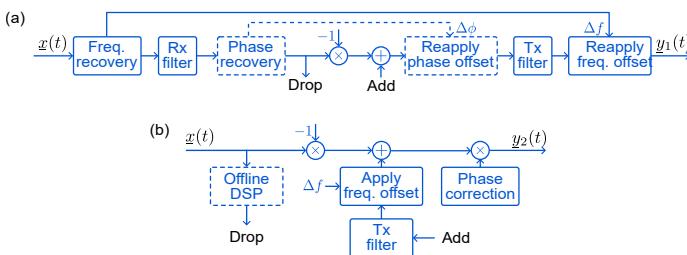
where  $\phi_{\text{LO}}(t)$  is the LO phase noise, and  $h_{\text{crx}}(t)$  represents the impulse response of the bandwidth-limited coherent receiver. The symbol  $*$  denotes the convolution operation. To suppress spectral components from neighboring channels, the digitized signal is passed through a low-pass filter. Considering that the coherent

receiver has unit gain within the frequency content of subchannel  $i$ , the resulting electrical signal after the low-pass filtering can be expressed as,

$$x(t) \propto \hat{a}_i(t) e^{j[2\pi\Delta f t + \Delta\phi(t)]},$$

where  $\hat{a}_i(t)$  is the received complex amplitude of subchannel  $i$ ,  $\Delta f = f_i - f_{\text{LO}}$  denotes the frequency offset, and  $\Delta\phi(t) = \phi_i(t) - \phi_{\text{LO}}(t)$  is the phase noise difference. The resulting signal is then processed through a series of DSP operations to demodulate the ‘drop’ data and to modulate a new ‘add’ data signal. Figure 2.2 (a) illustrates a general DSP framework for the add-drop operation in an OEO interferometer. The first step performs a coarse compensation of the frequency offset  $\Delta f$ . Then, a receive (Rx) filter with an impulse response  $h_{\text{rx}}(t)$  is applied to suppress any residual image from the adjacent channels and to downsample the signal to one sample per symbol. While these operations, including  $h_{\text{rx}}(t)$ , are inherently discrete-time in nature, a continuous-time notation is adopted here for simplicity and consistency across the subsequent DSP steps. Following this, the phase offset  $\Delta\phi$  is estimated and corrected, and the recovered noisy symbol sequence is directed to a local drop output for demodulation. Simultaneously, a sign-inverted copy is combined with a locally generated sequence of ‘add’ symbols. The resulting signal is then processed through a transmit (Tx) filter with an impulse response  $h_{\text{tx}}(t)$  to upsample and filter the signal, and the resulting I/Q components are

Next, the phase offset  $\Delta\phi$  is reapplied, followed by upsampling and filtering through a transmit (Tx) filter with an impulse response  $h_{\text{tx}}(t)$ . Subsequently, the recovered frequency offset  $\Delta f$  is reapplied, and the resulting I/Q components are



**Fig. 2.2:** Typical sequence of DSP steps in an optic-electronic-optic interferometer (a), and a simplified version implemented in Sec. 4.2(b).

passed to D/As. In case there is no spectral overlap between the neighboring channels, both the phase recovery and phase modulation steps can be bypassed from the DSP path as indicated by the dashed rectangles in Fig. 2.2(a).

For the experimental setup presented in Sec. 4.2, we first adopt a simplified DSP steps (see Fig. 2.2(b)), to focus exclusively on the transmitter-side DSP. Here, we directly subtract the digitized signal  $\underline{x}(t)$  from the frequency-shifted add signal, where the frequency offset is manually adjusted. The final output signal, after the full DSP chain (Fig. 2.2 (a)), can be expressed as

$$\underline{y}_1(t) = \left[ a_{\text{add}}(t) e^{j\Delta\phi(t)} * h_{\text{tx}}(t) \right] e^{j2\pi\Delta f t} - \underline{x}(t) * h_{\text{tx}}(t). \quad (2.2)$$

Here, the combined filter response,  $h_{\text{tx}}(t) = h_{\text{rx}}(t) * h_{\text{tx}}(t)$ , is essential for suppressing out-of-band noise and for subchannel selection in case of (orthogonal) frequency-division or wavelength-division multiplexing. Alternatively, the transmit filter defines the pulse shape of the add signal. For the simplified DSP chain, the output signal reduces to

$$\underline{y}_2(t) = \left[ a_{\text{add}}(t) * h_{\text{tx}}(t) \right] e^{j2\pi\Delta f t} - \underline{x}(t).$$

Following D/A conversion, the signal  $\underline{y}(t)$  (either  $\underline{y}_1$  or  $\underline{y}_2$ ) is modulated onto a copy of the LO laser, using an electro-optic I/Q modulator with a lowpass response of  $h_{\text{iqm}}(t)$ . This remodulated optical field can be expressed as

$$\underline{E}_{\text{oeo}}(t) \propto \left[ \underline{y}(t) * h_{\text{iqm}}(t) \right] e^{j[2\pi f_{\text{LO}} t + \phi_{\text{LO}}(t)]}.$$

To simplify the above expression, we first assume an ideal response from the I/Q modulator, i.e.,  $h_{\text{iqm}}(t) = \delta(t)$ . Furthermore, since the phase deviation  $\Delta\phi(t)$  in Eq. 2.2 varies slowly (in the kHz range) relative to the bandwidth of  $h_{\text{tx}}(t)$  (in the GHz range), it can be considered approximately constant throughout the impulse response. This allows  $\Delta\phi(t)$  to be taken outside the convolution. The resulting

simplified expression for the remodulated signal after the complete DSP chain becomes

$$E_{\text{oeo}}(t) \propto [a_{\text{add}}(t) * h_{\text{tx}}(t) - \hat{a}_i(t) * h_{\text{trx}}(t)] e^{j[2\pi f_i t + \phi_i(t)]}. \quad (2.3)$$

At the output coupler, the remodulated signal from the OEO path is superimposed on the through path signal. For this analysis, we assume that both interferometer arms are matched in amplitude, polarization, and group delay. Based on these assumptions, the optical signals at the interferometer output for the typical DSP steps can be expressed as

$$E_{\text{out},1}(t) = \sum_k a_k(t) e^{j[2\pi f_k t + \phi_k(t)]} + [a_{\text{add}}(t) * h_{\text{tx}}(t) - \hat{a}_i(t) * h_{\text{trx}}(t)] e^{j[2\pi f_i t + \phi_i(t)]}.$$

Whereas, for the simplified DSP steps, the expression becomes

$$E_{\text{out},2}(t) = \sum_k a_k(t) e^{j[2\pi f_k t + \phi_k(t)]} + [a_{\text{add}}(t) * h_{\text{tx}}(t) e^{j\Delta\phi(t)} - \hat{a}_i(t)] e^{j[2\pi f_i t + \phi_i(t)]}.$$

The derived expressions highlight that a coherent add-drop operation is subject to several critical constraints. To effectively erase the ‘drop’ channel at the interferometer output, a phase-inverted replica of the original signal must be synthesized. This regenerated signal must match the original in carrier frequency and phase, taking into account the combined effects of the coherent receiver  $h_{\text{crx}}(t)$ , the DSP chain  $h_{\text{trx}}(t)$ , and the I/Q modulator response  $h_{\text{iqm}}$ . For the ‘add’ operation, in case of non-overlapping spectral multiplexing, at least an appropriate frequency offset must be applied to ensure proper spectral alignment.

The proposed OEO interferometer architecture can be extended to accommodate dual-polarization transmission systems. This would involve incorporating an adaptive multiple-input multiple-output (MIMO) equalizer, where the equalizer coefficients are inverted and applied to the ‘add’ signal. However, strong

polarization-dependent loss could present challenges in practical implementations.

This section outlines the core signal processing steps required to perform coherent add-drop multiplexing using an OEO interferometer under idealized conditions. In the following section, we expand the analysis to account for practical impairments, including differential path delays and laser phase noise, to identify the critical conditions required for effective signal cancellation.

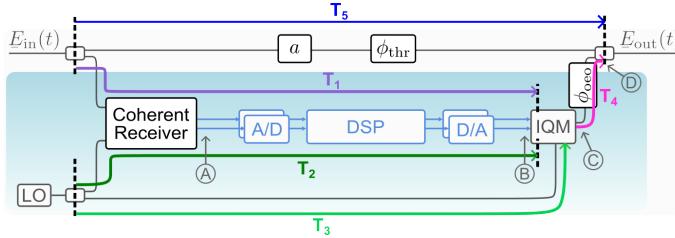
## 2.2 Interferometer Impairments

In the previous section, we examined the add-drop functionality of the OEO interferometer under idealized conditions, assuming perfectly matched path lengths and neglecting random phase fluctuations. In this section, we extend the analysis to incorporate practical impairments, including differential path delays, random phase fluctuations, and laser phase noise. The goal is to identify the necessary conditions for achieving effective destructive signal cancellation.

Figure 2.3 highlights the various time delays along the signal paths. The delay in the upper, purely optical path of the interferometer is denoted as  $T_5$ . In the OEO path, the signal propagation delay from the interferometer input coupler through the DSP chain to the RF input of the modulator is labeled as  $T_1$ . From the LO output, one path incurs a delay of  $T_2$  through a combined optical-electrical route, whereas another path with a delay  $T_3$  brings the LO as an optical carrier to the modulator. The final segment, from the modulator to the output coupler, is associated with a delay  $T_4$ .

Coherent detection of the input optical signal in the OEO path results in a beat term as shown in Eq. 2.1. To focus solely on the influence of time delays, we assume an ideal coherent receiver with an impulse response  $h_{\text{crx}}(t) = \delta(t)$ , implying that it does not distort the input signal. Based on this assumption, the beat term reduces to

$$\underline{s}_A(t) = \underline{E}_{\text{in}}(t) e^{-j[2\pi f_{\text{LO}} t + \phi_{\text{LO}}(t)]},$$



**Fig. 2.3:** Typical signal propagation delays and impairments in the OEO interferometer highlighted along the signal paths.

where  $E_{\text{in}}(t)$  is the input optical field. Now, inserting the time delay  $T_1$  for the input signal, and the  $T_2$  for the local laser path while acting as LO, the electrical signal at the modulator RF input port (labeled as B in the figure) can be written as

$$s_B(t) = \hat{E}_{\text{in}}(t - T_1) e^{-j[2\pi f_{\text{LO}} \cdot (t - T_2) + \phi_{\text{LO}}(t - T_2)]}.$$

Here  $\hat{E}_{\text{in}}$  represents the baseband-equivalent version of the input signal following coherent detection and DSP. This electrical signal then modulates a copy of the LO field, which experiences a time delay  $T_3$  along its optical path to the modulator. The resulting optical field at the modulator output (indicated as C) becomes

$$E_C(t) = \hat{E}_{\text{in}}(t - T_1) e^{-j[2\pi f_{\text{LO}} \cdot (t - T_2) + \phi_{\text{LO}}(t - T_2)]} e^{j[2\pi f_{\text{LO}} \cdot (t - T_3) + \phi_{\text{LO}}(t - T_3)]}.$$

Finally, this remodulated optical signal traverses an additional delay  $T_4$  from the modulator output to the interferometer output coupler. To account for random phase fluctuations arising from environmental disturbances or other time-varying factors along the optical section of the OEO path, we define a phase shift term  $\phi_{\text{oeo}}(t)$ . The corresponding remodulated optical field (marked as D) is given by

$$E_D(t) = \hat{E}_{\text{in}}(t - T_1 - T_4) e^{-j[2\pi f_{\text{LO}} \cdot (t - T_2 - T_4) + \phi_{\text{LO}}(t - T_2 - T_4)]} \\ e^{j[2\pi f_{\text{LO}} \cdot (t - T_3 - T_4) + \phi_{\text{LO}}(t - T_3 - T_4) + \phi_{\text{oeo}}(t)]}.$$

Next, this remodulated optical signal is combined with the signal from the upper path. To account for any residual amplitude imbalance and phase fluctuations in

the through path, an amplitude scaling factor  $a$  and a time-dependent phase term  $\phi_{\text{thr}}(t)$  are introduced, capturing variations due to environmental perturbations and thermal drift. Taking into account a signal propagation delay of  $T_5$  along the upper path, the resulting superimposed optical field is expressed as

$$\begin{aligned} E_{\text{out}}(t) = & a E_{\text{in}}(t - T_5) e^{j\phi_{\text{thr}}(t)} - \hat{E}_{\text{in}}(t - T_1 - T_4) e^{j\phi_{\text{oeo}}(t)} \\ & \times e^{-j[2\pi f_{\text{LO}} \cdot (t - T_2 - T_4) + \phi_{\text{LO}}(t - T_2 - T_4)]} \\ & \times e^{j[2\pi f_{\text{LO}} \cdot (t - T_3 - T_4) + \phi_{\text{LO}}(t - T_3 - T_4)]}. \end{aligned}$$

When the two path delays  $T_2$  and  $T_3$  taken by the LO laser are within its coherence time, the phase noise difference between the time instances  $\phi_{\text{LO}}(t - T_2 - T_4)$ , and  $\phi_{\text{LO}}(t - T_3 - T_4)$  can be considered as quasi-stationary. With the constant LO phase noise difference denoted as  $\delta\phi_{\text{LO}}$ , the above electric field simplifies to

$$\begin{aligned} E_{\text{out}}(t) = & a E_{\text{in}}(t - T_5) e^{j\phi_{\text{thr}}(t)} - \hat{E}_{\text{in}}(t - T_1 - T_4) e^{j\phi_{\text{oeo}}(t)} \\ & \times e^{j[2\pi f_{\text{LO}} \cdot (T_2 - T_3) + \delta\phi_{\text{LO}}(T_2 - T_3)]} \end{aligned}$$

From the above equation, it can be summarized that optimum destructive interference is obtained under the following conditions:

- $a = 1$ , i.e., the signals from the two interferometer paths have equal amplitudes.
- $\phi_{\text{thr}}(t) = \phi_{\text{oeo}}(t)$ , i.e., the optical phase of the two interferometer paths is synchronized.
- $T_5 = T_1 + T_4$ , i.e., the delay for the signal in the combined OEO path should match the delay from the through path.
- $T_2 = T_3$ , the delay for the two paths taken by the LO laser, either acting as an LO for coherent detection or acting as a carrier for remodulation, is equal. In general, the delay difference should be much smaller than the laser coherence time, which will result in a stationary phase noise difference that can be compensated using a phase-locked loop as discussed in the next section.

- $E_{\text{in}}(t) = \hat{E}_{\text{in}}(t)$  implies that the OEO-regenerated optical signal retains the same amplitude and phase characteristics as the field from the through path across all relevant time-frequency components.

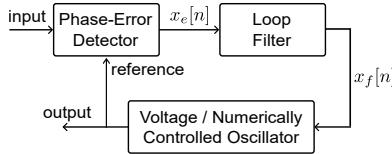
Imperfect fulfillment of the ideal interference conditions results in a residual of the drop channel at the interferometer output, which degrades system performance due to in-band crosstalk. Under typical operating conditions, amplitude balance and delay alignment between the interferometer paths are inherently stable and do not require dynamic control. In contrast, the relative optical phase is subject to continuous drift due to external influences, such as thermal fluctuations and mechanical disturbances. Consequently, active phase stabilization is essential to preserve coherent interference and ensure reliable signal processing. A detailed analysis of phase alignment criteria and stabilization strategies is presented in the following section.

## 2.3 Phase Stabilization

The performance of any interferometric system critically depends on the stability of the relative optical phase between the signal paths. Due to the inherent sensitivity of the optical phase in a fiber or waveguide to environmental factors such as temperature fluctuations and vibrations, active stabilization mechanisms are essential. This section presents the phase alignment criteria and describes the phase-locked loop (PLL) architecture implemented in this thesis.

The typical structure of a PLL is shown in Fig. 2.4. At the core is a phase-error detector, which computes an error signal based on some function  $f\{\cdot\}$  of the phase difference between the input and reference signals. This error signal is passed through a loop filter that generates a correction signal. Depending on the implementation, this correction signal either tunes a voltage-controlled oscillator (VCO) in analog systems or a numerically controlled oscillator (NCO) in digital systems to adjust the phase of the reference signal accordingly. In digital communication synchronization tasks, PLLs are often implemented entirely in

the digital domain, as with the coarse frequency-offset correction used in this work. However, interferometer phase stabilization relies on a hybrid analog-digital design, with the phase-error detector and the reference oscillation correction distributed over both analog and digital circuitry.



**Fig. 2.4:** Basic building blocks of a phase-locked loop (PLL).

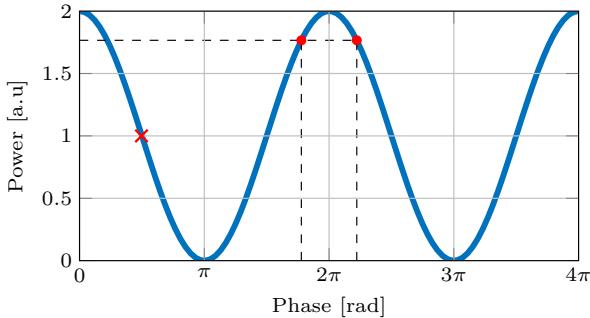
### 2.3.1 Phase Error Detector

Most interferometer stabilization techniques typically rely on directly measuring the interference power variations using a photodetector to generate an error signal. The optical power variation resulting from the superposition of two optical fields with the same center frequency, when detected by a photodetector, can be expressed as

$$P = P_1 + P_2 + 2\sqrt{P_1 P_2} \cos(\Delta\phi).$$

Where  $P_1$  and  $P_2$  are the optical powers associated with the two interferometer paths, and  $\Delta\phi = \phi_1 - \phi_2$  represents the relative phase difference between them. The dependence of the output optical power on the phase difference  $\Delta\phi$  is illustrated in Fig. 2.5.

Two primary challenges arise when the photodetector signal is directly used to extract phase information. First, due to the cosine dependence, the photodetector response is nonunique, i.e., multiple phase values yield the same output power as indicated by the example markers (solid circles) in Fig. 2.5. Consequently, the measurement becomes ambiguous whether the phase is monotonically increasing or decreasing, particularly near the extrema, where the slope of the power variation



**Fig. 2.5:** Variation of interference power with respect to phase difference. The marker ‘ $\times$ ’ indicates a phase value around which the power response exhibits linear behavior. Circular markers identify two phase values with identical interference power, illustrating the ambiguity in phase retrieval from direct power measurement.

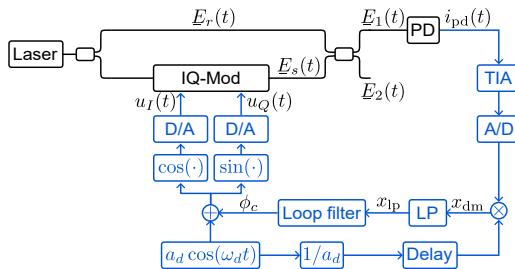
approaches zero. This ambiguity limits the ability to continuously track the phase evolution solely based on photodetector readings of interference power.

Second, the region of the interference curve with the highest linearity is centered around  $\Delta\phi = \pi/2$ . This linear operating point is commonly exploited in PLL implementations, as it enables more accurate and stable feedback control. This phase-locking strategy is similarly employed in communication systems, where PLLs are widely used for various synchronization tasks, such as aligning the local oscillator with the carrier frequency (carrier phase synchronization) or synchronizing the sampling clock with the symbol rate (symbol timing recovery). However, in the context of the OEO interferometer scheme, phase locking must occur near the extrema of the interference curve. This requirement complicates the use of traditional PLL approaches that rely on linear operation around  $\pi/2$ .

To address this challenge, a dither-based technique is employed to extract a phase error signal corresponding to the derivative of the interference power variation. This approach enables phase locking at the extrema, while allowing the use of a symmetric  $180^\circ$  optical coupler and an AC-coupled front-end. The following section describes the principle and implementation of the dither-based phase error extraction method in detail.

## Dither Based Phase Error Detection

In the following, we explain the principle of extracting a phase-error signal by applying a deterministic phase modulation in one arm of an interferometer. A simplified interferometer configuration, as shown in Fig. 2.6, is used to illustrate the concept. A continuous-wave (CW) laser output is split into two optical paths. In the lower path, the optical field is sinusoidally phase modulated using an I/Q modulator. In the upper path, optical delay and polarization are considered to match those of the lower path. The two optical signals are then recombined using a symmetric 3-dB coupler. The superimposed signal is then detected by a photodetector (PD) and digitized using an A/D converter for further analysis.



**Fig. 2.6:** Schematic of a Mach-Zehnder interferometer structure implementing a dither-based phase-locked loop. An I/Q modulator serves as an optical voltage-controlled oscillator, applying both a dither phase modulation and the required phase correction in one interferometer arm. Optical paths are shown in black, while electrical signal paths are indicated in blue.

We now present the mathematical steps for extracting the phase error in the dither-based PLL configuration. The optical field in the upper arm is defined as

$$E_r(t) = \sqrt{P_r} \cdot e^{j[\omega_0 t + \phi_r(t)]},$$

where  $P_r$  denotes the optical power,  $\omega_0 = 2\pi f_0$  is the angular frequency of the laser, and  $\phi_r(t)$  represents phase fluctuations. For simplicity and to focus on the derivation of the phase error term, laser phase noise and relative intensity noise are neglected in this analysis. In the lower path, a phase modulation signal is

applied to the I/Q modulator, where the in-phase and quadrature drive signals are defined as

$$u_I(t) = \cos[a_d \cos(\omega_d t) + \phi_c(t)],$$

$$u_Q(t) = \sin[a_d \cos(\omega_d t) + \phi_c(t)].$$

Here  $a_d$  is the dither phase amplitude,  $\omega_d$  is the dither angular frequency, and  $\phi_c(t)$  is the phase correction term provided by the loop filter. The dither signal can be rewritten using the complex exponential form as

$$\underline{u}(t) = e^{j[a_d \cos(\omega_d t) + \phi_c(t)]}.$$

Assuming small-signal modulation and biasing the IQ-Mod at its null point, the modulated optical field after the IQ-Mod can be expressed as

$$\underline{E}_s(t) = \sqrt{P_s} \cdot e^{j[\omega_0 t + \phi_s(t)]} \cdot \underline{u}(t),$$

$$= \sqrt{P_s} \cdot e^{j[\omega_0 t + \phi_s(t) + \phi_c(t)]} \cdot e^{j[a_d \cos(\omega_d t)]}.$$

Where  $P_s$  and  $\phi_s$  represent the optical power and phase fluctuations, respectively, in the lower path. The phase modulation exponential term  $e^{j[a_d \cos(\omega_d t)]}$  can be expanded using the Jacobi-Anger expansion given by [17]

$$e^{j[z \cos(\theta)]} = \sum_{n=-\infty}^{\infty} j^n J_n(z) e^{jn\theta}$$

$$= J_0(z) + 2 \sum_{n=1}^{\infty} j^n J_n(z) \cos(n\theta),$$

here,  $J_n(\cdot)$  denotes the Bessel function of the first kind of order  $n$ , and the identity  $J_{-n}(z) = (-1)^n J_n(z)$  is applied. For small values of  $z$ , the first-order Bessel function  $J_1(z)$  dominates, whereas the higher-order terms rapidly diminish. Thus, under the small-amplitude condition  $a_d \ll 1$ , the exponential term  $e^{j[a_d \cos(\omega_d t)]}$  can be approximated by retaining only the dominant first-order terms as

$$e^{j[a_d \cos(\omega_d t)]} \approx J_0(a_d) + 2j J_1(a_d) \cos(\omega_d t),$$

To simplify the notation in subsequent derivations, arguments  $t$  and  $a_d$  are omitted hereafter. Under this convention, the electric field emerging from the IQ modulator can be written as

$$\underline{E}_s \approx \sqrt{P_s} \cdot e^{j[\omega_0 t + \phi_s + \phi_c]} \cdot [J_0 + 2j J_1 \cos(\omega_d t)]. \quad (2.4)$$

The power associated with the electric field  $\underline{E}_s$  can be determined using

$$\begin{aligned} |\underline{E}_s|^2 &= \underline{E}_s \cdot \underline{E}_s^* \\ &= \left\{ J_0 \sqrt{P_s} e^{j[\omega_0 t + \phi_s + \phi_c]} + 2j J_1 \sqrt{P_s} \cos(\omega_d t) e^{j[\omega_0 t + \phi_s + \phi_c]} \right\} \\ &\quad \cdot \left\{ J_0 \sqrt{P_s} e^{-j[\omega_0 t + \phi_s + \phi_c]} - 2j J_1 \sqrt{P_s} \cos(\omega_d t) e^{-j[\omega_0 t + \phi_s + \phi_c]} \right\} \\ &= J_0^2 P_s - 2j J_0 J_1 P_s \cos(\omega_d t) + 2j J_0 J_1 P_s \cos(\omega_d t) + 4J_1^2 P_s \cos^2(\omega_d t) \\ &= J_0^2 P_s + 2J_1^2 P_s + 2J_1^2 P_s \cos(2\omega_d t). \end{aligned} \quad (2.5)$$

In the third line of the above equation, the trigonometric identity  $2 \cos^2(\theta) = 1 + \cos(2\theta)$  is applied. The optical fields  $\underline{E}_s$  and  $\underline{E}_r$  are subsequently combined via a symmetric 3-dB coupler, yielding the output electric fields

$$\begin{aligned} \underline{E}_1 &= \frac{1}{\sqrt{2}} (\underline{E}_s + \underline{E}_r) \\ \underline{E}_2 &= \frac{1}{\sqrt{2}} (\underline{E}_s - \underline{E}_r). \end{aligned}$$

The field  $\underline{E}_1$  is detected using a PD with responsivity  $R$ , and the photocurrent is given by

$$\begin{aligned} i_{pd} &= R \cdot |\underline{E}_1|^2 \\ &= R [\underline{E}_1 \cdot \underline{E}_1^*] \\ &= \frac{R}{2} [(E_s + E_r) \cdot (E_s^* + E_r^*)] \\ &= \frac{R}{2} [|\underline{E}_s|^2 + |\underline{E}_r|^2 + 2\Re\{\underline{E}_s \underline{E}_r^*\}]. \end{aligned} \quad (2.6)$$

The product term  $\{E_s E_r^*\}$  can be found as

$$\begin{aligned} \underline{E}_s \underline{E}_r^* &= \left[ J_0 \sqrt{P_s} e^{j[\omega_0 t + \phi_s + \phi_c]} + 2j J_1 \sqrt{P_s} \cos(\omega_d t) e^{j[\omega_0 t + \phi_s + \phi_c]} \right] \cdot \sqrt{P_r} e^{-j[\omega_0 t + \phi_r]} \\ &= J_0 \sqrt{P_s P_r} e^{j\Delta\phi} + 2j J_1 \sqrt{P_s P_r} \cos(\omega_d t) e^{j\Delta\phi}. \end{aligned}$$

Here,  $\Delta\phi = \phi_s - \phi_r + \phi_c$  is the residual phase error. Finally, the real part of  $\{E_s E_r^*\}$  is given by,

$$\Re\{E_s E_r^*\} = J_0 \sqrt{P_s P_r} \cos(\Delta\phi) - 2J_1 \sqrt{P_s P_r} \sin(\Delta\phi) \cos(\omega_d t). \quad (2.7)$$

By substituting the expressions for  $|E_s^2|$  and  $\Re\{E_s E_r^*\}$  from Eq. 2.5 and Eq. 2.7, respectively, into Eq. 2.6 the photocurrent becomes,

$$\begin{aligned} i_{pd} &= \frac{R}{2} \left[ J_0^2 P_s + 2J_1^2 P_s + 2J_1^2 P_s \cos(2\omega_d t) + P_r \right. \\ &\quad \left. + 2J_0 \sqrt{P_s P_r} \cos(\Delta\phi) - 4J_1 \sqrt{P_s P_r} \sin(\Delta\phi) \cos(\omega_d t) \right]. \quad (2.8) \end{aligned}$$

From the above expression, the photocurrent terms (excluding the scaling factor  $\frac{R}{2}$ ) can be grouped according to their functional form and frequency content as

$$\begin{aligned} \text{Constant DC terms :} & \quad J_0^2 P_s + 2J_1^2 P_s + P_r \\ \text{Interference terms :} & \quad 2J_0 \sqrt{P_s P_r} \cos(\Delta\phi) - 4J_1 \sqrt{P_s P_r} \sin(\Delta\phi) \cos(\omega_d t) \\ \text{2nd harmonic :} & \quad 2J_1^2 P_s \cos(2\omega_d t) \end{aligned}$$

The first group represents the constant DC components arising from the average optical power in each interferometer path. The interference terms capture the phase-sensitive interaction between the two fields. The first interference term varies with the cosine of the phase difference  $\Delta\phi$ , as in the non-dithered case, while the second term oscillates at the dither frequency with the amplitude varying according to the sine of  $\Delta\phi$ . The final term is the second-harmonic component, which is independent of the interference phase difference  $\Delta\phi$ , since the phase-amplitude  $a_d$  is assumed to be sufficiently small to retain only the first-order terms.

Using a transimpedance amplifier (TIA), the photocurrent is converted into a voltage according to  $u_{\text{pd}} = R_T i_{\text{pd}}$ , where  $R_T$  is the TIA gain factor in ohms. In an AC-coupled A/D system, the constant DC terms and the slowly varying interference term are suppressed. Consequently, the resulting digital signal (still described in the continuous-time domain) becomes

$$u_{\text{pd}} = RR_T \left[ -2J_1 \sqrt{P_s P_r} \sin(\Delta\phi) \cos(\omega_d t) + J_1^2 P_s \cos(2\omega_d t) \right].$$

This signal is then synchronously demodulated in DSP by multiplying with the reference dither tone  $\cos(\omega_d t)$ . The resulting signal can be written as

$$\begin{aligned} x_{\text{dm}} &= B \cos^2(\omega_d t) + C \cos(2\omega_d t) \cos(\omega_d t) \\ &= \frac{1}{2}B + \frac{1}{2}B \cos(2\omega_d t) + \frac{1}{2}C \cos(\omega_d t) + \frac{1}{2}C \cos(3\omega_d t) \end{aligned}$$

here  $B = -RR_T 2J_1 \sqrt{P_s P_r} \sin(\Delta\phi)$  and  $C = RR_T J_1^2 P_s$ . The derivation makes use of standard trigonometric identities, namely  $2 \cos^2(a) = 1 + \cos(2a)$ , and  $2 \cos(a) \cos(b) = \cos(a + b) + \cos(a - b)$ . The dither frequency  $\omega_d$  and its harmonics are suppressed by applying a lowpass filter (LP). After this filtering and by introducing the argument  $a_d$  again, the output signal simplifies to

$$x_{\text{LP}} = -RR_T J_1(a_d) \sqrt{P_s P_r} \sin(\Delta\phi)$$

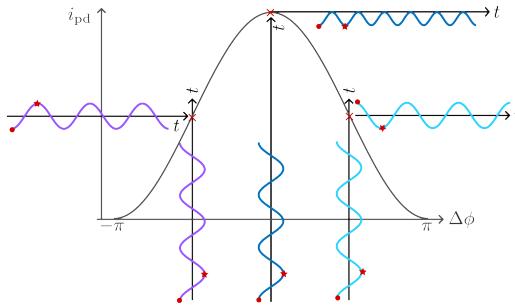
Further simplification is possible by applying the small-angle approximation  $\sin(z) \approx z$  [17]. Using this, the lowpass filtered signal can be approximated as

$$x_{\text{LP}} \approx -RR_T J_1(a_d) \sqrt{P_s P_r} \Delta\phi, \quad (2.9)$$

which provides a linear estimate of the residual phase error  $\Delta\phi$ . The coefficient preceding  $\Delta\phi$  in this expression defines the phase-error detector gain  $K_e$  of the PLL. This signal serves as the error input to a control loop. In this dither-based

PLL configuration, phase detection is distributed across the analog-digital opto-electronic chain. The combined use of phase dithering and synchronous demodulation allows the system to determine the direction of phase deviation, thereby enabling stabilization around the extrema of the interference power variation.

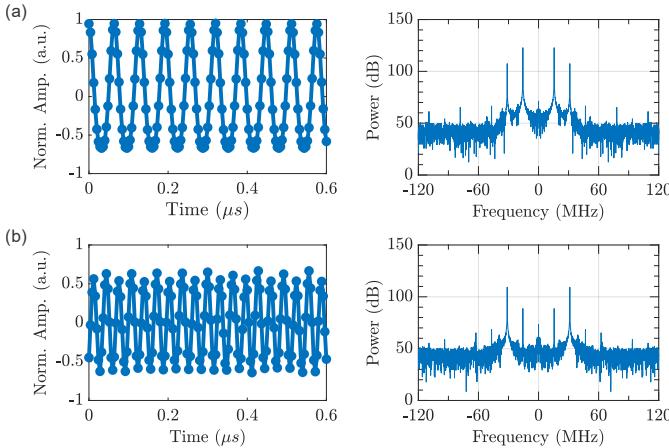
The effect of applying a small phase dither signal on the photocurrent is visualized in Fig. 2.7. Small sinusoidal phase modulation signals are shown vertically in



**Fig. 2.7:** Schematic illustration of phase dithering effects on interference power detection. Photocurrent variations for a sinusoidal dither are illustrated at phase offsets  $-\pi/2$ ,  $0$ , and  $\pi/2$  (marked with  $\times$ ). The progression of the dither phase is indicated by circular and star markers.

purple, blue, and cyan at three distinct phase offset values  $-\pi/2$ ,  $0$ , and  $\pi/2$ . The corresponding variations in the photocurrent are shown using matching colors. Circle and star markers indicate phase evolution related to the dither signal. At zero phase offset, the photocurrent oscillates at twice the dither frequency. In contrast, at phase offsets of  $-\pi/2$  and  $\pi/2$ , the photocurrent oscillates at the fundamental dither frequency. Notably, the oscillation around  $\pi/2$  is in-phase with the dither signal, while the oscillation around  $-\pi/2$  is in quadrature (i.e., phase shifted by  $90^\circ$ ).

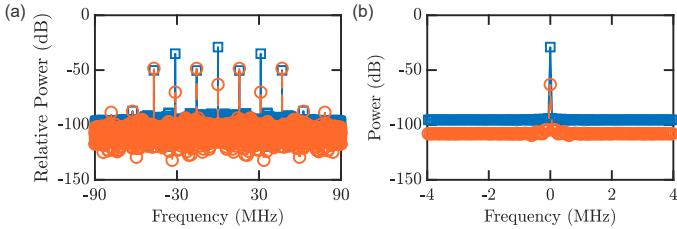
Figure 2.8 illustrates the characteristics of the photocurrent for two different phase offset conditions measured in a practical setup operating at a dither frequency of 15.63 MHz, with the control loop disabled (i.e.,  $\phi_c = 0$ ). In subplot (a), the time-domain signal (left) shows large oscillations, indicating a phase difference near  $\pi/2$ . The corresponding spectrum (right) reveals a dominant first-harmonic



**Fig. 2.8:** Photodetector output over time (left) and corresponding spectra (right) for two different phase offset scenarios in (a) and (b) obtained with the setup shown in Fig. 2.6.

component, consistent with the expected behavior of the photocurrent model in Eq. 2.8. In contrast, subfigure (b) exhibits reduced oscillation amplitude in the time-domain plot (left) and suppressed first harmonic in the spectral profile (right), indicating a phase difference near an extrema. In both subfigures, the second-harmonic peak power in the spectral plots is invariant to the phase offset. Additional spectral lines at higher harmonics (third and fourth) are attributed to minor bias drift of the I/Q modulator.

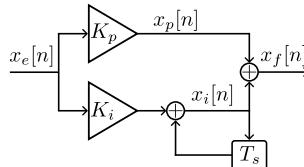
Figure 2.9 (a) presents the spectra of the multiplier output corresponding to the two photocurrent scenarios above. Distinct peaks are visible at harmonics of the dither frequency. As a result of mixing with the reference tone, the first harmonic component from the photocurrent now appears at both DC and the second harmonic. For the case with strong oscillation at  $\omega_d$  (see Fig. 2.8 (a)), the multiplier output exhibits a prominent DC peak (blue), while in the second case, where the oscillation at  $\omega_d$  is weaker (Fig. 2.8 (b)), a smaller DC peak (orange) is observed. Figure 2.9 (b) displays the corresponding spectra of the lowpass-filtered signal, where all higher-order harmonics are effectively suppressed and only the DC component remains.



**Fig. 2.9:** Spectra of the multiplier output (a) and the lowpass-filtered signal (b) corresponding to the two photocurrent cases shown in Fig. 2.8.

### 2.3.2 Loop Filter

The error signal generated by the phase detector is passed to a loop filter, which shapes it into a suitable control signal for driving the NCO. In the case of the interferometer phase stabilization, this control signal ultimately adjusts the phase (or frequency) of the reference oscillator, corresponding to the optical field in the interferometer path. A proportional–integral (PI) loop filter is most commonly employed for this purpose due to its balance of fast response and steady-state accuracy.



**Fig. 2.10:** Structure of the discrete-time proportional–integral (PI) loop filter. The symbol  $T_s$  indicates a delay corresponding to one sampling interval.

The proportional term applies a gain factor  $K_p$  directly to the instantaneous error, providing an immediate corrective response. The integral term, with gain  $K_i$ , accumulates the past error over time, ensuring long-term phase alignment and eliminating residual steady-state offsets. A block diagram of the PI loop filter

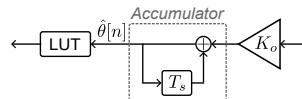
is shown in Fig. 2.10. In discrete time, the proportional contribution  $x_p[n]$ , the integral contribution  $x_i[n]$ , and the overall filter output  $x_f[n]$  are given by

$$\begin{aligned} x_p[n] &= K_p x_e[n], \\ x_i[n] &= x_i[n - 1] + K_i x_e[n], \\ x_f[n] &= x_p[n] + x_i[n], \end{aligned}$$

where  $x_e[n]$  is the error signal from the phase-error detector. The transfer function of this second-order loop filter, and its role in PLL stability and dynamics, are well established and can be found in standard references such as Gardner's Phaselock Techniques [18].

### 2.3.3 Numerically Controlled Oscillator

A numerically controlled oscillator (NCO) generates a discrete-time sinusoidal waveform whose instantaneous phase or frequency is determined by a digital control input. In this work, the control input is provided by the output of the loop filter, which adjusts the phase and frequency of the oscillator output. For the purpose of interferometer phase stabilization, the NCO output is converted to the analog domain using a D/A and subsequently applied to a phase shifting device, implemented here using an I/Q modulator, to correct the phase of the optical field. Figure 2.11 illustrates the core components of an NCO, comprising



**Fig. 2.11:** Block diagram of the numerically controlled oscillator for phase and frequency synthesis. The accumulator integrates the input phase with gain  $K_0$  and feeds the LUT to generate the sinusoidal waveform.  $T_s$  denotes the unit sample delay.

a phase accumulator and a look-up table (LUT). The accumulator output serves as an index to the LUT, which stores discrete samples of the desired waveform

typically a sinusoidal. The accumulator output, representing the instantaneous phase of the waveform, is expressed as

$$\hat{\theta}[n] = \hat{\theta}[n-1] + K_o x_f[n] \bmod 2\pi,$$

where,  $x_f[n]$  is the loop filter output and  $K_o$  is the NCO gain. In most digital implementations  $K_o$  is set to unity. This accumulation of phase then creates the sinusoidal oscillatory waveform. While conventional NCOs rely on phase accumulation to generate oscillations, the random phase fluctuations of the interferometer is typically around a zero-mean frequency. Therefore, for phase control algorithm the accumulator is bypassed, and the loop filter output is directly connected to the LUT.

### Frequency of the NCO Waveform

The real-time implementation of the NCO relies upon fixed-point integer arithmetic. In this work, the bit-width of the accumulator and the input to the LUT are the same, denoted as  $N_{\text{ACC}}$ . The accumulator input, which defines the phase increment, is denoted as  $\phi_{\text{step}}$  and has a bit-width of  $N_{\text{ACC}} - 1$  bits. For  $N_{\text{sa}}$  parallel samples, the frequency of the NCO output,  $f_o$  is given by

$$f_o = \frac{f_{\text{sa}} N_{\text{sa}} \phi_{\text{step}}}{2^{N_{\text{ACC}}}}. \quad (2.10)$$

The smallest frequency step, corresponding to the NCO frequency resolution occurs for  $\phi_{\text{step}} = 1$ ,

$$f_{o,\text{min}} = \frac{f_{\text{sa}} N_{\text{sa}}}{2^{N_{\text{ACC}}}}. \quad (2.11)$$

The maximum frequency that the NCO can generate is achieved for the maximum value of  $\phi_{\text{step}} = 2^{N_{\text{ACC}}-1}$ , consistent with the Nyquist limit:

$$f_{o,\text{max}} = \frac{f_{\text{sa}} N_{\text{sa}}}{2}. \quad (2.12)$$

### 2.3.4 PLL Parameter Design

The PLL output response is characterized by two key parameters: the damping factor  $\zeta$  and the natural frequency  $\omega_n$ . The equivalent noise bandwidth  $B_n$ , which serves as a practical measure of the PLL bandwidth is related to these parameters as [19]

$$B_n = \frac{\omega_n}{2} \left( \zeta + \frac{1}{4\zeta} \right) \quad (2.13)$$

For a given phase-error detector gain  $K_e$  and an NCO normalized gain  $K_o$ , when the equivalent loop bandwidth is small relative to the sampling frequency,  $B_n T_s \ll 1$ , the loop filter constants can be well approximated related to  $\zeta$  and  $\omega_n$  as follows [19]

$$\begin{aligned} K_o K_e K_p &\approx 2\zeta\omega_n \\ K_o K_e K_i &\approx \omega_n^2 \end{aligned} \quad (2.14)$$

Since, the NCO gain  $k_0$  is normalized to unity, the loop filter coefficients can be expressed as

$$\begin{aligned} K_i &= \frac{\omega_n^2}{K_e} \\ K_p &= 2\zeta \sqrt{\frac{K_i}{K_e}} \end{aligned} \quad (2.15)$$

In most practical applications, the phase-error detector is the most complicated component in the loop and its gain  $K_e$  is not easily adjusted. So for a given phase error detector design  $K_e$  is considered fixed, and the loop filter coefficients are tuned to achieve desired loop dynamics.

In summary, this chapter has presented the fundamental principles and technical considerations of OEO interferometers as optical add–drop multiplexers. Key aspects, including the operating principle, system impairments, and the importance of optical phase stabilization, have been discussed. In particular, dither-based

phase control has been highlighted as a practical approach to ensure robust operation. These insights establish the system-level context and requirements that are addressed in the subsequent chapter through the design and implementation of DSP algorithms.



# 3 DSP Algorithms

This chapter focuses on the analysis, simulation, and hardware implementation of the DSP algorithms required for the communication system and the interferometric add-drop operation. The sections are structured in chronological order, beginning with the transmitter side, such as the parallel FIR filter and pulse shaping modules. The discussion then proceeds to the receiver side signal processing, following the sequence of experimental validation.

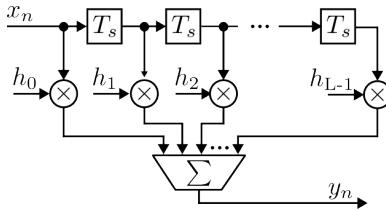
## 3.1 FIR Filter

This section introduces the implementation of finite impulse response (FIR) filters, with an emphasis on architectures that support parallel input and output samples, as used throughout this thesis. An FIR filter has an impulse response of finite duration. In the digital domain, the impulse response is represented by a discrete-time sequence, commonly referred to as the filter coefficients.

Designing an FIR filter involves determining the appropriate values of these coefficients to achieve a desired frequency response. With fixed coefficients, an FIR filter behaves as a linear time-invariant (LTI) system, where the output is given by the convolution of the input signal  $x[n]$  with the filter impulse response  $h[n]$ . For an FIR filter of length  $L$ , the output can be expressed as

$$y[n] = \sum_{m=0}^{L-1} h[m]x[n-m] \quad (3.1)$$

A block diagram of an FIR filter implementation is shown in Fig. 3.1. The convolution operation is built using multipliers, adders, and delay elements. Each delay element introduces one sample delay, denoted by the symbol  $T_s$ . As shown in the figure, an FIR filter with  $L$  taps requires  $L - 1$  delay elements,  $L$  multipliers, and  $L$  adders. The number of arithmetic operations per clock cycle grows linearly with the number of taps, and this growth is scaled linearly again when parallel input samples are processed. Although such an approach may still be functionally valid, it is often not preferred in practice. A long chain of arithmetic operations between input and output registers can result in timing violations, making the design less robust at higher clock speeds.



**Fig. 3.1:** Block diagram of a direct form FIR filter.

In the following section, we examine the architecture of FIR filters designed for parallel input and output processing, followed by a discussion of their practical implementation strategies.

### 3.1.1 Parallel FIR Filter

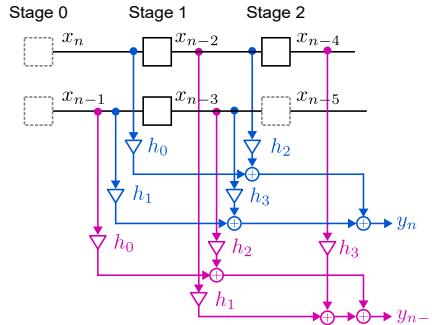
Real-time processing of high-speed signals in optical communication systems requires FIR filters capable of operating at several gigasamples per second. Since typical FPGAs operate at a few hundred megahertz clock frequency, the DSP algorithms must be parallelized to process several samples simultaneously. Here, we explore parallel FIR filter structures suitable for such high-throughput scenarios.

To support flexible design configurations, we formulate a generic FIR filter structure that accepts a variable number of coefficients and parallel input samples. We illustrate the general computation pattern through a representative example. For a number of coefficients,  $N_{\text{coef}} = 4$  and a number of parallel samples,  $N_{\text{sa}} = 2$ . The output of the filter can be written as follows

$$\begin{aligned} y_n &= x_n h_0 + x_{n-1} h_1 + x_{n-2} h_2 + x_{n-3} h_3 \\ y_{n-1} &= x_{n-1} h_0 + x_{n-2} h_1 + x_{n-3} h_2 + x_{n-4} h_3 \end{aligned}$$

Figure 3.2 illustrates the hardware structure of the example parallel-input parallel-output FIR filter. The buffer registers at the input (dashed gray box) are optional and included to simplify data alignment or pipelining. To compute  $N_{\text{sa}}$  outputs sample simultaneously in one clock cycle, a total of  $N_{\text{sa}} + N_{\text{coef}} - 1$  present and past samples are required. The required number of register stages  $N_r$  to store the necessary past samples, including the input buffer stage, is given by

$$N_r = \left\lceil \frac{N_{\text{sa}} + N_{\text{coef}} - 1}{N_{\text{sa}}} \right\rceil = \left\lceil \frac{5}{2} \right\rceil = 3$$



**Fig. 3.2:** Parallel-input, parallel-output FIR filter structure with  $N_{\text{coef}} = 4$ , processing  $N_{\text{sa}} = 2$  samples per clock cycle.

In the hardware implementation, delay elements are realized using a one-dimensional register array, which simplifies data movement and indexing. Each register element is identified by an index of the form  $R(kN_{\text{sa}} + n)$ , where  $k$  is the delay stage index ranging from  $\{0, 1, \dots, N_r - 1\}$ , and  $n \in \{0, 1, \dots, N_{\text{sa}} - 1\}$  refers to the parallel sample index.

At every rising clock edge,

- The current input samples  $\{x[0], x[1], \dots, x[N_{\text{sa}} - 1]\}$  are loaded to the registers with index ranging from  $R[0], R[1], \dots, R[N_{\text{sa}} - 1]$ ,
- The previous contents of the registers  $R[0], R[1], \dots, R[N_{\text{sa}} - 1]$  is shifted to the registers  $R[N_{\text{sa}}], R[N_{\text{sa}} + 1], \dots, R[2N_{\text{sa}} - 1]$ ,
- This procedure continues until the last stage  $k = N_r - 1$  is updated with the contents from the stage  $k = N_r - 2$ .

Since all arithmetic operations in the hardware implementation are carried out using fixed-point integers, each coefficient  $h[n]$  can be expressed as a sum of powers of two as

$$h[n] = \sum_{k=0}^m b_k \cdot 2^k, \quad b_k \in \{0, 1\},$$

where  $b_k$  denotes the binary representation of the coefficient. Accordingly, the product of an input sample  $x[n]$  with a coefficient  $h[n]$  can be expressed as

$$x[n] \cdot h[n] = \sum_{k=0}^m b_k \cdot (x[n] \cdot 2^k)$$

In this formulation, each term  $x[n] \cdot 2^k$  corresponds to a left-shift operation of  $x[n]$  by  $k$  bits. Consequently, multiplication in hardware is realized through a combination of shift operations and additions, eliminating the need for dedicated multipliers. This approach significantly reduces hardware complexity and enables better pipelining by splitting the convolution process into partial shifts and accumulations over several stages, with the final output obtained by summing the intermediate results.

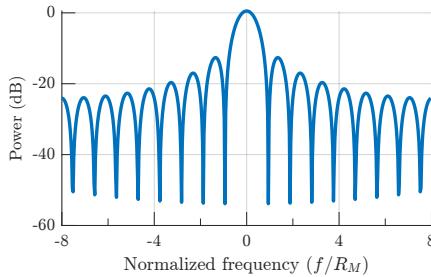
## 3.2 Pulse Shaping

The fundamental objective of a digital communication system is to enable the reliable transmission of digital information across an analog channel. At the transmitter, a binary data stream generated by the information source is first mapped onto modulation symbols (e.g., QPSK or 16-QAM). These discrete symbols must then be transformed into a continuous-time waveform suitable for physical transmission. This transformation is accomplished through pulse shaping, a process that ensures both spectral efficiency and minimal inter-symbol interference (ISI). Let  $a[i]$  denote the discrete-time sequence of modulation symbols, and let  $p(t)$  represent the pulse shaping function. The transmitted signal can be expressed as

$$s(t) = \sum_i a[i]p(t - iT_M),$$

where  $T_M$  is the symbol duration. The simplest pulse shape is the rectangular pulse, which maintains a constant amplitude over the symbol interval. This pulse is more commonly referred to as the non-return-to-zero (NRZ) format. A key advantage of the NRZ pulse is its strict confinement of each symbol to its respective time slot, ensuring the absence of ISI in an ideal, distortion-free, and dispersion-free channel. However, the frequency-domain characteristics are less favorable. The Fourier transform of a rectangular pulse yields a sinc-shaped spectrum with slowly decaying sidelobes, as illustrated in Fig. 3.3. These sidelobes cause poor spectral containment, rendering NRZ pulses unsuitable for bandwidth-constrained systems.

Despite this limitation, NRZ pulse shaping remains attractive in certain applications. In particular, it is widely employed in intensity modulation (IM) and direct detection (DD) systems, especially for short-reach and cost-sensitive optical communication links, where its simplicity and low implementation cost outweigh its spectral inefficiency.



**Fig. 3.3:** Spectrum of a rectangular pulse shape for 16 samples/symbol.

To improve spectral efficiency while eliminating ISI, the raised cosine (RC) filter is widely adopted. It satisfies the Nyquist no-ISI criterion, which ensures zero intersymbol interference under ideal sampling conditions. The frequency response of the RC filter is defined as [20]

$$H_{\text{rc}}(f) = \begin{cases} T_M & 0 \leq |f| \leq \frac{1-\beta}{2T_M} \\ \frac{T_M}{2} \left[ 1 + \cos \left( 2\pi \cdot \frac{T_M}{2\beta} \left( |f| - \frac{1-\beta}{2T_M} \right) \right) \right] & \frac{1-\beta}{2T_M} \leq |f| \leq \frac{1+\beta}{2T_M} \\ 0 & |f| \geq \frac{1+\beta}{2T_M} \end{cases}$$

here,  $\beta$  is called the roll-off factor and defined in the range  $[0, 1]$ . Recalling that the minimum Nyquist bandwidth is  $1/(2T_M)$ , the factor  $\beta$  specifies the frequencies beyond this minimum bandwidth. As can be seen from the above equation, the RC shape in the frequency domain has three distinct frequency regions:

- A constant value within the frequency range  $-\frac{1-\beta}{2T_M} \leq f \leq \frac{1-\beta}{2T_M}$
- A half cosine oscillation (overall duration in frequency  $\beta/T_M$ , compared to a full oscillation frequency period  $2\beta/T_M$ ) raised by a constant to have only positive values and scaled by a factor  $T_M/2$  to have a peak value of  $T_M$  within both the positive and negative frequency range  $\frac{1-\beta}{2T_M} \leq |f| \leq \frac{1+\beta}{2T_M}$ .
- In all other frequencies has zero values.

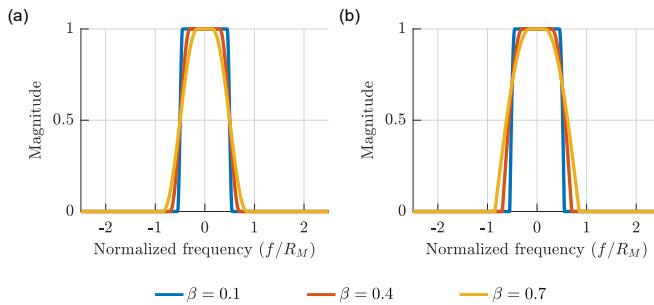
To eliminate ISI using RC filtering, the filter is typically realized in a split form across transmitter and receiver by means of matched filtering. In this configuration, the receive filter is the time-reversed replica of the transmit filter. The filtering of the pulse shaping function with its time-inverted counterpart results in its autocorrelation, expressed as

$$r_p(t) = p(t) * p(-t), \quad R_p(f) = |P(f)|^2 \implies P(f) = \sqrt{R_p(f)}.$$

Accordingly, the individual filter applied at the transmitter and receiver has a frequency response equal to the square root of the RC spectrum. This filter is referred to as the square-root raised cosine (RRC) filter, with frequency response,

$$H_{\text{rrc}} = \begin{cases} \sqrt{T_M} & 0 \leq |f| \leq \frac{1\beta}{2T_M} \\ \sqrt{T_M} \left[ \cos \left( 2\pi \cdot \frac{T_M}{4\beta} \left( |f| - \frac{1-\beta}{2T_M} \right) \right) \right] & \frac{1-\beta}{2T_M} \leq |f| \leq \frac{1+\beta}{2T_M} \\ 0 & |f| \geq \frac{1+\beta}{2T_M}. \end{cases}$$

Figure 3.4 illustrates the frequency responses of RC and RRC filters for varying roll-off factors.



**Fig. 3.4:** Raised cosine frequency response (left) and square-root raised cosine frequency response (right) for various roll-off.

### 3.2.1 RRC Filter Design

The RRC pulse shaping filter implemented in this work is designed to meet real-time hardware constraints. For symbol rates of 1 GBd and 2 GBd, filters with roll-off factors of 0.1 and 0.4 are designed, respectively. Given a D/A sampling rate of 4 GSa/s, the required upsampling factors are 4 for the 1 GBd and 2 for the 2 GBd. The discrete-time impulse response of an RRC filter with unit energy, for an oversampling factor  $L$ , is given as [20]

$$h[n] = \begin{cases} \frac{1}{\sqrt{L}} \cdot \left(1 - \beta + \frac{4\beta}{\pi}\right) & n = 0, \\ \frac{\beta}{\sqrt{2L}} \left[ \left(1 - \frac{2}{\pi}\right) \cos\left(\frac{\pi}{4\beta}\right) + \left(1 + \frac{2}{\pi}\right) \sin\left(\frac{\pi}{4\beta}\right) \right] & n = \pm \frac{L}{4\beta}, \\ \frac{1}{\sqrt{L}} \cdot \frac{\sin[\pi n(1-\beta)/L] + \frac{4\beta n}{L} \cos[\pi n(1+\beta)/L]}{\pi n/L \left[1 - (4\beta n/L)^2\right]} & \text{otherwise,} \end{cases}$$

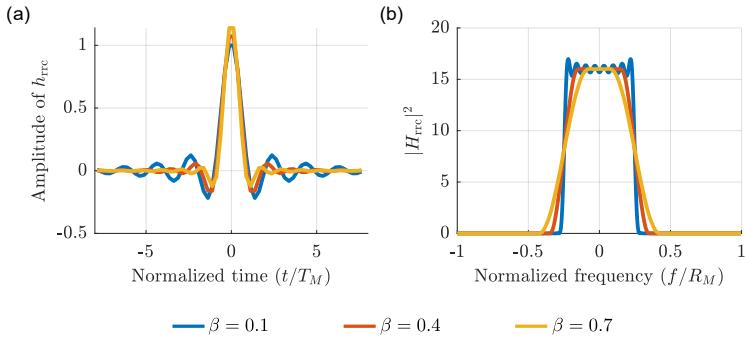
Since this ideal response extends infinitely, it must be truncated to a certain number of symbols for practical realization. A 63-tap implementation is adopted in this work, balancing FPGA resource usage with filter performance.

Figure 3.5 shows the impulse and corresponding frequency responses of a 63-tap RRC filter for  $L = 4$  with roll-off factors of 0.1, 0.4, and 0.7. To enable efficient polyphase implementation, the filter length is extended to 64 by appending one zero, making the total number of taps divisible by  $L$ . In the 1 GBd case, this yields four subfilters of 16 coefficients each.

### Coefficient Bit-Width Analysis

For FPGA implementation, the filter coefficients are represented using signed fixed-point integers. Given that the D/A supports 14-bit resolution and the filter output must accommodate both positive and negative values, a signed 14-bit word length is chosen for the filter output.

The filter coefficients are first computed in MATLAB as high-precision floating-point values. Subsequently, these values are scaled to fixed-point integers. In



**Fig. 3.5:** RRC impulse response (left) and the corresponding frequency response (right) for 63 filter taps with 4 samples/symbol for various roll-off.

in this work, QPSK modulation is primarily employed, where two independent bit streams form the I and Q components of the signal. Therefore, each component only contains two possible amplitude levels of +1 or -1, corresponding to a symbol bit-width of  $N_{\text{b,sym}} = 2$ . For comparison, in a 16-QAM modulation format, considering independent bit streams for the I and Q branches, each component can take one of four amplitude levels (-3, -1, +1, +3), which requires a symbol bit-width of  $N_{\text{b,sym}} = 3$ .

Let the filter be defined by  $N_{\text{tap}}$  coefficients, each represented using a signed fixed-point word of  $N_{\text{b,coef}}$  bits. The key design objective is to select  $N_{\text{b,coef}}$  such that the maximum possible filter output remains within the dynamic range of the 14-bit D/A. The worst-case absolute maximum output occurs when all input samples align in sign with the respective filter coefficients, such that each multiplication contributes positively to the output sum. Each multiplication result requires at least  $N_{\text{b,coef}} + N_{\text{b,sym}} - 1$  bits, and the accumulation of  $N_{\text{tap}}$  such terms leads to an additional bit-growth of  $\lceil \log_2(N_{\text{tap}}) \rceil$ . Thus, the required bit-width to represent the worst-case filter output can be expressed as

$$N_{\text{b,out}} = N_{\text{b,coef}} + N_{\text{b,sym}} - 1 + \lceil \log_2(N_{\text{tap}}) \rceil \leq N_{\text{DAC}}$$

For QPSK modulation and  $N_{\text{tap}} = 16$  with a 14-bit D/A converter, this condition implies  $N_{\text{b,coef}} \leq 9$ . However, since multiplication with symbol amplitude  $\pm 1$  can

be implemented without any bit-growth,  $N_{b,\text{coef}} = 10$ -bit fixed-point representation is used for the coefficients in this thesis.

### 3.3 Hilbert Transform and Analytic Signal Generation

The Hilbert Transform (HT) is a mathematical operation that converts a real-valued signal into another real-valued signal with a  $90^\circ$  phase shift. When the original signal is combined with its HT, the result is a complex analytic signal, where the original signal represents the real part and the HT provides the imaginary part. In this work, the HT is applied to an intermediate-frequency signal to construct its analytic representation, which is then used to realize single-sideband (SSB) modulation.

The HT is most conveniently described in the frequency domain. It applies a  $-90^\circ$  phase shift to the positive frequencies and a  $+90^\circ$  phase shift to the negative frequencies. The ideal frequency response can be expressed as

$$H(f) = \begin{cases} -j & \text{for } f > 0 \\ +j & \text{for } f < 0 \end{cases}$$

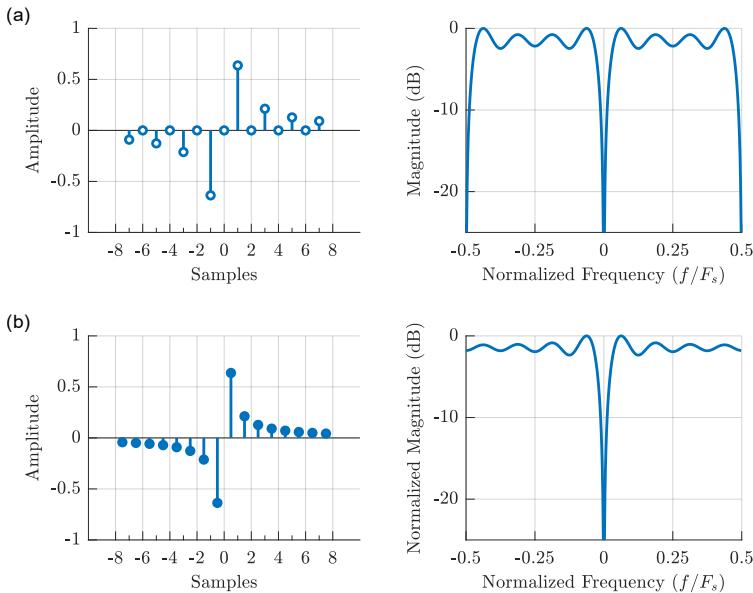
In the time domain, the corresponding impulse response of the HT is infinite in duration. For a normalized sampling frequency, the ideal impulse response is given by [21]

$$h[n] = \begin{cases} \frac{2}{\pi n} \sin^2\left(\frac{\pi n}{2}\right) & n \neq 0 \\ 0 & n = 0. \end{cases} \quad (3.2)$$

The HT can be implemented in both time and frequency domains. For real-time applications on platforms such as FPGAs, this thesis adopts a time-domain FIR implementation due to its lower complexity. Since the ideal HT impulse response is infinite in length and non-causal, it must be truncated for practical digital

realization. The characteristics of the resulting FIR filter depend on whether the number of coefficients is odd or even.

Figure 3.6 illustrates the impulse (left) and frequency responses (right) for odd-tap and even-tap implementations, respectively. When an odd number of taps is used, the resulting filter is classified as a Type-III FIR filter, characterized by an anti-symmetric impulse response (see Fig. 3.6 (a), left) with zero-valued coefficients at all even indexed positions. In contrast, an even-tap implementation known as a Type-IV FIR filter, which also has an anti-symmetric impulse response (see Fig. 3.6 (b), left) but contains no zero-valued coefficients. The Type-III



**Fig. 3.6:** Impulse (left) and frequency (right) responses of FIR Hilbert transform filters. (a) Type-III filter with odd length, exhibiting an impulse response with all even-indexed samples equal to zero and a bandpass spectrum. (b) Type-IV filter with even length, showing an impulse response with no non-zero samples and a wider passband.

structure is well-suited for hardware, as it lowers computational effort by omitting every second coefficient. Additionally, it exhibits an integer-valued group delay,

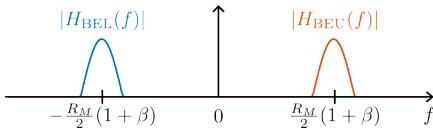
simplifying temporal alignment with the input signal. The Type-IV filter, on the other hand, introduces a fractional group delay, necessitating resampling or fractional delay correction to maintain alignment with the original real-valued signal.

In the frequency domain, the type-III spectrum (see Fig. 3.6(a) right) exhibits zero magnitude response at both DC and the Nyquist frequency, resulting in a bandpass-like characteristic. In contrast, the Type-IV filter response (see Fig. 3.6(b) right) has a spectral null only at DC, offering a closer approximation to the ideal HT over a wider frequency range. However, given that the Hilbert Transform is applied in this thesis to signals centered at an intermediate frequency well above DC, the reduced accuracy of the Type-III filter near DC is of minimal consequence. Consequently, the Type-III configuration is adopted due to its lower computational demand, predictable integer delay, and straightforward implementation, all of which are advantageous in FPGA-based real-time systems.

### 3.4 Carrier Frequency Offset Estimation Using Band-Edge Filters

In digital coherent receivers, a carrier frequency offset (CFO) arises when the transmitter and LO lasers operate independently, with frequency deviations that may reach several gigahertz. In the context of the OEO interferometer, this offset must be preserved in the remodulating signal to ensure that, after modulation, the optical output remains aligned with the carrier frequency, as described in Sec. 2.1. To achieve this, a band-edge filter technique is employed for CFO acquisition. The method is attractive because it avoids reliance on prior symbol timing recovery, operates reliably with a sampling rate as low as twice the symbol rate, and remains applicable in overlapping spectral multiplexing scenarios. CFO estimation is obtained by exploiting the transition regions of the transmitted signal spectrum, where the filter response is particularly sensitive to frequency deviations. The filter design is determined by the system's symbol rate ( $R_M$ ), pulse-shaping scheme, and roll-off factor ( $\beta$ ).

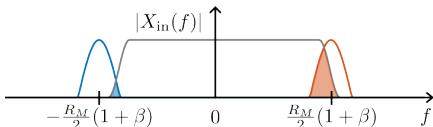
Figure 3.7 illustrates the frequency response of an exemplary band-edge filter designed for an RRC pulse-shaped signal. The response centered at the positive band edge, denoted as  $H_{BEU}(f)$  and shown in red, is referred to as the upper band-edge filter. Conversely, the response centered at the negative band edge, denoted as  $H_{BEL}(f)$  and shown in blue, is referred to as the lower band-edge filter. A detailed description of the filter shape formation is provided in Sec. 3.4.3. These complementary filter responses form the foundation for detecting carrier frequency offsets in the received waveform and are subsequently used to construct the frequency error detector.



**Fig. 3.7:** Magnitude responses of the upper and lower band-edge filters used for carrier frequency offset detection.

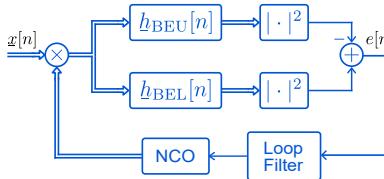
### 3.4.1 Frequency Error Detector Based on Band-Edge Filtering

The upper and lower band-edge filters can be used to construct a frequency error detector (FED). Figure 3.8 illustrates this concept with a received signal  $X_{in}(f)$  exhibiting a positive frequency offset. The shaded areas under the upper and lower filter responses indicate the relative energy in each band. A larger red area compared to the blue area reflects the positive frequency shift, forming the basis of the FED measurement.

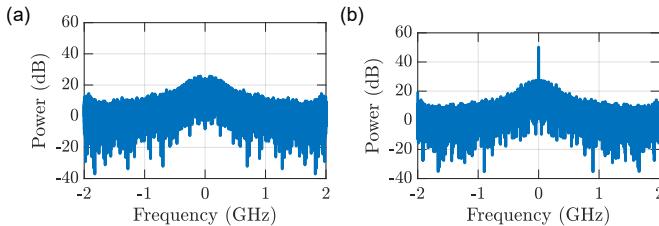


**Fig. 3.8:** Illustration of frequency error detection using band-edge filters. The relative energy captured by the upper (red) and lower (blue) filters reflects the sign and magnitude of the frequency offset.

Building on the principles described above, Fig. 3.9 presents a block diagram of a frequency-locked loop (FLL) implemented using the upper and lower band-edge filters. The architecture consists of two parallel branches, each incorporating one of the band-edge filters. The energy difference between the outputs of the upper and lower filters is used to generate an error signal, which is fed through a loop filter to control the NCO. Through this feedback, the NCO is adaptively steered to minimize the frequency error between the incoming signal and the local reference.



**Fig. 3.9:** Block diagram of a frequency-locked loop (FLL) employing upper and lower band-edge filters. The error signal, derived from the energy difference between the filter outputs, is fed back to a numerically controlled oscillator (NCO) via a loop filter. Double arrows indicate complex signals, while single arrows indicate real signals.



**Fig. 3.10:** Spectrum of the FLL error signal for an input signal with zero frequency offset (a), and with a 100 MHz frequency offset (b).

Figure 3.10 shows the spectra of the error signal for two exemplary frequency offsets. The input signal, with a symbol rate of 2 GBD, RRC pulse shaping (roll-off  $\beta = 0.1$ ), and sampled at 4 GSa/s, is processed using 15-tap band-edge filters. As the frequency offset increases, a pronounced DC peak appears in the error

spectrum, whereas the DC component vanishes when the offset is zero. This behavior illustrates the fundamental operating principle of the frequency error detector. The following subsection presents an efficient implementation of the band-edge filters using even and odd symmetry.

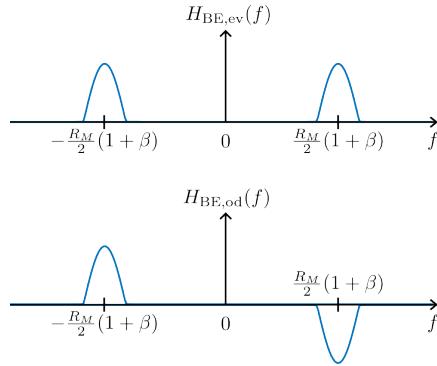
### 3.4.2 Efficient Implementation with Even and Odd Filter Symmetry

In the FLL shown in Fig. 3.9, the conventional error signal is obtained from the energy difference of the upper and lower band-edge filter outputs, which requires an absolute-square operation. While simple to implement in software such as MATLAB, this operation requires multiple multipliers on an FPGA, increasing resource usage and latency. This can be mitigated by forming two additional band-edge filters with even and odd symmetry from the existing upper and lower filters. The FLL error signal can then be expressed as

$$e[n] = \Re \{ z_{\text{BE,ev}}[n] z_{\text{BE,od}}^*[n] \}.$$

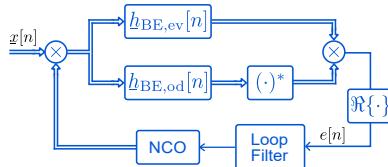
Here,  $z_{\text{BE,ev}}$  and  $z_{\text{BE,od}}$  are the outputs of the even and odd band-edge filters,  $\{\cdot\}^*$  denotes complex conjugation, and  $\Re\{\cdot\}$  extracts the real part of a complex value. This eliminates the need to explicitly calculate the energy of each filter output, reducing the number of multipliers and, consequently, the latency of the FLL computation. A detailed derivation demonstrating the equivalence of this method with the conventional energy-based approach is provided in Appendix A.

The even-symmetric filter response is obtained by summing the upper and lower band-edge filter responses, while the odd-symmetric response is formed by taking their difference. These filters are referred to as the even band-edge and odd band-edge filters, with frequency responses denoted by  $H_{\text{BE,ev}}$  and  $H_{\text{BE,od}}$ , as illustrated in Fig. 3.11. By using these filters, the FLL error signal can be generated efficiently in real time, maintaining the same functionality as the conventional approach while reducing hardware resource usage.



**Fig. 3.11:** Magnitude responses of the even (top) and odd (bottom) band-edge filters, obtained by respectively summing and subtracting the original upper and lower band-edge filter responses shown in Fig. 3.7.

Figure 3.12 shows the corresponding FLL architecture using the even and odd band-edge filters. The error signal is generated by multiplying the filter outputs, and its real part drives the loop. This approach reduces the number of multiplications compared to the earlier structure shown in Fig. 3.9, improving computational efficiency.



**Fig. 3.12:** Block diagram of an FLL employing even and odd band-edge filters. Double arrows indicate complex signals, while single arrows indicate real signals.

### 3.4.3 Impulse Response Characteristics of Band-Edge Filters

In the previous section, the formation of a frequency error detector was introduced using the frequency-domain characteristics of band-edge filters. To gain further insight into the practical implementation, it is useful to examine the corresponding impulse responses.

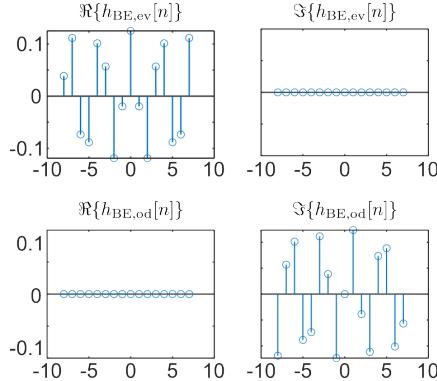
The construction begins with a baseband version of the band-edge spectral lobe, which has a half-cosine shape in the frequency domain with a width of  $2\beta/T_M$ , where  $T_M = 1/R_M$  denotes the symbol period. Consequently, the full cosine period in the frequency domain is  $4\beta/T_M$ , leading to the mathematical form:

$$H_{\text{BE,bb}} = \begin{cases} \cos\left(2\pi \frac{T_M}{4\beta} f\right) & |f| \leq \frac{\beta}{T_M}, \\ 0 & \text{otherwise.} \end{cases}$$

Applying the inverse Fourier transform then yields the baseband impulse response  $h_{\text{BE,bb}}(t)$ . Multiplying this impulse response by complex sinusoids at frequencies  $\pm(1 + \beta)/(2T_M)$  introduces a frequency-domain shift, resulting in the lower and upper band-edge impulse responses. The even and odd responses are then formed by combining these through addition and subtraction. The resulting impulse responses are shown in Fig. 3.13. A key observation is that the imaginary part of the even response and the real part of the odd response vanish. This symmetry eliminates two convolution operations, making the FLL structure in Fig. 3.12 more efficient than the conventional design in Fig. 3.9.

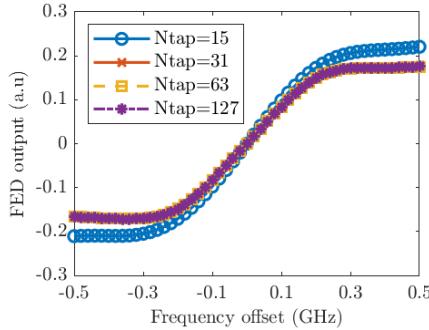
### 3.4.4 Design Considerations and Parameter Selection

This subsection discusses the key design considerations and parameter choices for the band-edge filter-based FED. The effects of filter length, sampling resolution, and fixed-point bit width on detector performance are analyzed to guide the implementation for real-time FPGA operation.



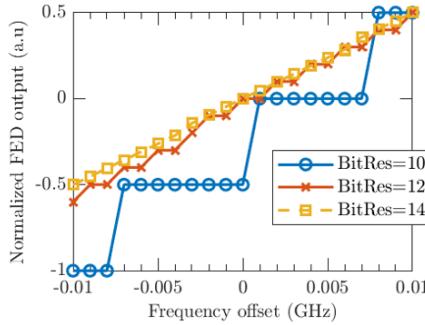
**Fig. 3.13:** Impulse responses of the even (top row) and odd (bottom row) band-edge filters, with real parts shown on the left and imaginary parts on the right.

Figure 3.14 presents the FED output for varying frequency offsets with 20 MHz steps and different numbers of filter taps ( $N_{\text{tap}}$ ), simulated for a symbol rate of 2 GBd with an RRC roll-off of  $\beta = 0.1$ . The linear response occurs only within the excess bandwidth, i.e.,  $\pm\beta/T_M$  ( $\pm 200$  MHz), while outputs saturate beyond this range. For a resolution of 20 MHz, 15 filter taps are sufficient to preserve linearity.



**Fig. 3.14:** Simulated frequency-error detector (FED) output versus frequency offset for different numbers of filter taps.

To evaluate fine-resolution performance, the frequency offset is varied within  $\pm 10$  MHz in 1 MHz steps. Using  $N_{\text{tap}} = 15$ , the FED output is simulated for bit resolutions of 10, 12, and 14 bits. As shown in Fig. 3.15, higher bit resolutions enhance the detector's sensitivity to small frequency changes, enabling finer frequency discrimination. For the chosen 12-bit resolution with 15 taps, the resulting frequency resolution is approximately 2 MHz, which is adopted in the final implementation.



**Fig. 3.15:** Simulation of FED output for various frequency offset for various fixed-point bit resolution.

The NCO, whose operating principle is discussed in Sec. 2.3.3, must be configured consistently with the FED characteristics to ensure proper operation of the FLL. To achieve a minimum NCO frequency close to 2 MHz, with a 250 MHz system clock and 16 parallel samples, the LUT bit-width is set to 11. Using Eq. 2.11, this gives

$$f_{\text{o,min}} = \frac{250 \cdot 10^6 \cdot 16}{2^{11}} \approx 1.95 \text{ MHz.}$$

Similarly, the maximum NCO frequency must span at least the detectable range of the FED, considering the designed symbol rate and pulse-shaping roll-off, while avoiding excessively large values that could induce oscillations under large error

conditions. By constraining the loop filter output to a 9-bit signed representation (maximum positive value 255), Eq. 2.12 yields

$$f_{o,\max} = \frac{250 \cdot 10^6 \cdot 16 \cdot 255}{2^{11}} \approx 498 \text{ MHz.}$$

This configuration ensures that the NCO operates reliably across the full range of expected frequency offsets while maintaining the resolution determined by the FED design. By aligning the FED bit resolution, number of filter taps, and NCO parameters, the FLL achieves accurate and stable frequency tracking, balancing both sensitivity and hardware resource efficiency.

### 3.5 Moving Average Filter

Moving average (MA) filters are among the most widely used lowpass filters in DSP due to their simplicity, linear phase response, and ease of implementation. MA filters are particularly suitable for applications where precise passband flatness or deep stopband attenuation is not required, providing basic lowpass filtering functionality for tasks such as smoothing white noise.

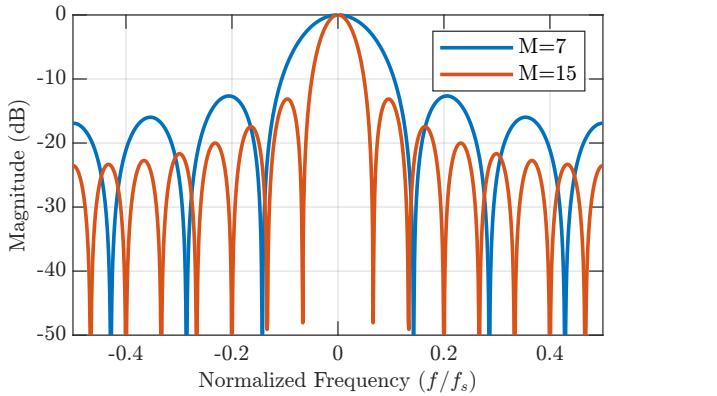
A length- $M$  moving average filter computes each output sample as the arithmetic mean of the most recent  $M$  input samples. The operation can be expressed using the following difference equation as

$$y[n] = \frac{1}{M} \sum_{m=0}^{M-1} x[n-m],$$

where,  $x[n]$  denotes the input signal. The impulse response of an MA filter is a rectangular pulse of amplitude  $\frac{1}{M}$  and length  $M$ , yielding the frequency response

$$H(f) = \frac{\sin(\pi M f)}{\pi M f}$$

The magnitude response for various averaging lengths is shown in Fig. 3.16. The

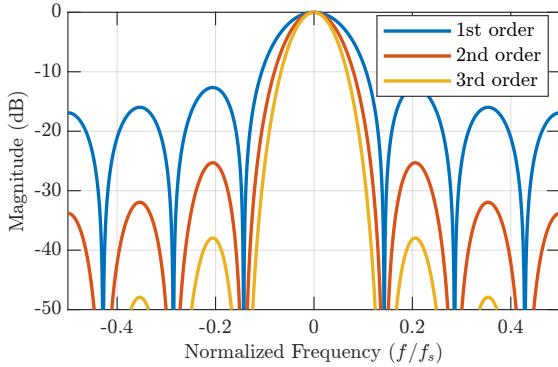


**Fig. 3.16:** Magnitude response of MA filters illustrating the effect of different filter lengths.

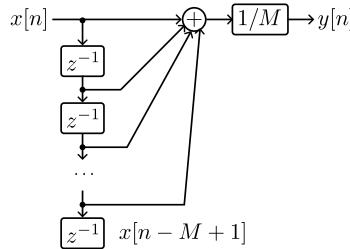
Spectral nulls occur at integer multiple of the frequency at  $f = k \cdot \frac{f_s}{M}$ , where  $k = \{\pm 1, \pm 2, \dots\}$ . Thus, giving  $M$  evenly spaced such spectral nulls within the Nyquist band of  $\pm 0.5f_s$ . Increasing  $M$  narrows the mainlobe and improves low-pass selectivity, though sidelobe attenuation remains fixed at approximately 13.3 dB for the first sidelobe. A straightforward method to increase sidelobe suppression is to cascade multiple MA stages. The magnitude response of the cascade is the single-stage response raised to the power of number of stages, providing improved stopband rejection without increasing design complexity. (Fig. 3.17).

### 3.5.1 Hardware Implementation Architecture

The straightforward implementation of an MA filter is its non-recursive form, which requires  $M - 1$  addition operations and a single multiplication per output sample (Fig. 3.18). While simple to implement, the number of additions grows linearly with  $M$ , which may lead to timing challenges in hardware realizations for high-throughput systems. As an illustrative example, an MA filter with  $M = 1024$  at an FPGA logic clock of 250 MHz, as used in this work, demands careful design considerations to avoid timing violations. A more efficient realization is the



**Fig. 3.17:** Magnitude response of multiple cascaded moving average (MA) filters, showing enhanced sidelobe attenuation.



**Fig. 3.18:** MA filter non-recursive implementation.

recursive running-sum form, formulated from the original MA as

$$\begin{aligned}
 y[n] &= \frac{1}{M} (x[n] + x[n-1] + \dots + x[n-M+1]) \\
 &= \frac{1}{M} (x[n] + x[n-1] + \dots + x[n-M+1] + x[n-M] - x[n-M]) \\
 &= y[n-1] + \frac{1}{M} (x[n] - x[n-M]),
 \end{aligned}$$

which reduces the number of additions to two per output samples, at the cost of increasing the delay line to  $M + 1$  samples as shown in Fig. 3.19. For high-throughput designs, this reduction in arithmetic complexity is significant.

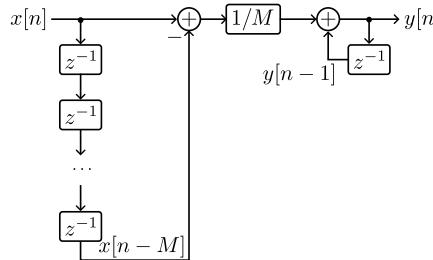


Fig. 3.19: MA filter recursive implementation.

### 3.5.2 Register Bit-Width Considerations

Although the moving average (MA) filter is computationally efficient, correct hardware implementation requires careful consideration of register bit widths to ensure mathematically accurate results. In fixed-point arithmetic using two's complement representation, the initial subtraction stage results in a bit growth of one. Subsequently, the accumulation stage requires an additional bit growth of  $\lceil \log_2(M) \rceil$ . When  $M$  is constrained to be an integer power of two, the final division operation can be efficiently implemented as a right-shift by  $\log_2(M)$  bits, thereby eliminating the need for a hardware multiplier or divider. An example hardware implementation is illustrated in Fig. 3.20, showing an 8-bit input signal processed with an averaging length of  $M = 8$  samples. The corresponding register bit widths for each stage of the processing chain are indicated in the diagram, highlighting the bit growth at both the subtraction and accumulation stages.

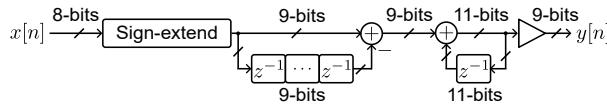


Fig. 3.20: Example hardware implementation of an MA filter with an 8-bit input signal and an averaging length of  $M = 8$ , illustrating register bit-width requirements at each processing stage.

## 3.6 Kaiser-Window-Based Lowpass Filter Design

While the MA filter is simple and efficient to implement, it suffers from poor spectral characteristics, particularly in terms of passband ripple and stopband attenuation. Although adequate for simple averaging tasks such as smoothing the error signal in a control algorithm, its performance is inadequate for high-fidelity signal processing tasks in the GHz frequency range. Consequently, this work adopts window-based FIR lowpass filter designs to improve spectral fidelity. Among the available options, the Kaiser window is favored due to its adjustable parameters that allow an effective balance between mainlobe width and sidelobe attenuation.

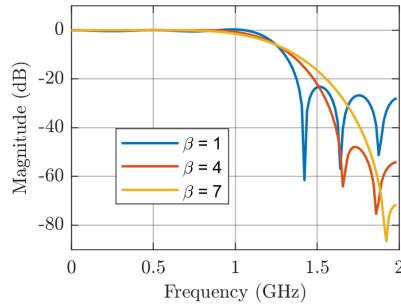
The Kaiser window is particularly advantageous because it introduces a shape parameter, commonly denoted by  $\beta$ , which enables independent control over the filter's transition bandwidth and sidelobe suppression. This makes it well-suited for applications requiring precise control over spectral leakage and filter sharpness. In this work, a Kaiser-window-based lowpass FIR filter is used to suppress unwanted spectral components from adjacent channels in a WDM received signal. The coefficients of a Kaiser window of length  $N + 1$  can be computed using the following expression as [21]

$$w[n] = \frac{I_0\left(\beta\sqrt{1 - \left(\frac{n-N/2}{N/2}\right)^2}\right)}{I_0(\beta)}, \quad 0 \leq n \leq N,$$

where  $I_0(\cdot)$  denotes the zero-th order modified Bessel function of the first kind. The parameter  $\beta$  determines the shape of the window, with higher values resulting in improved sidelobe suppression and a corresponding increase in main lobe width.

Figure 3.21 illustrates the frequency response of a low-pass FIR filter designed using the Kaiser window for various values of the shape parameter  $\beta$ . In this example, the filter is designed with a sampling rate of 4 GSa/s and a cutoff frequency

of 1.25 GHz. As shown, increasing  $\beta$  results in greater sidelobe suppression, but also leads to a wider main lobe. This demonstrates the inherent trade-off between transition bandwidth and spectral leakage in window-based FIR filter design.



**Fig. 3.21:** Frequency response of a Kaiser-window-based lowpass FIR filter, illustrating the effect of varying shape factors ( $\beta$ ) on main lobe width and sidelobe attenuation, for a cutoff frequency of 1.25 GHz and a sampling rate of 4 GSa/s.

This chapter has detailed the key DSP algorithms forming the core of the system, including band-edge filters, moving average and window-based lowpass filters, and frequency-locked loops. Design choices, such as filter parameters, bit resolution, and efficient hardware implementation strategies, were discussed to ensure practical feasibility. The next chapter focuses on the experimental implementation, demonstrating how these algorithms are applied in the physical system.



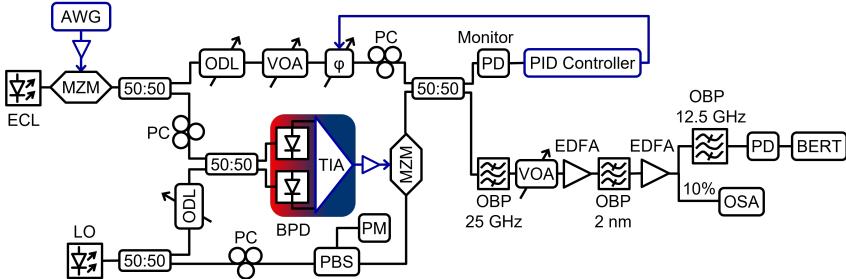
# 4 Experimental Implementations

This chapter presents the experimental realization of the OEO interferometer through four progressively advanced case studies. First, a proof-of-concept experiment using heterodyne detection with analog electronic processing validates the interferometric cancellation of an intensity modulated input signal. Second, the setup is adapted to a digital processing path and coherent remodulation showcasing coherent add-drop operation for a QPSK-modulated signal. Third, this setup is extended to evaluate a partially integrated interferometer module. Finally, an intradyne detection based configuration is introduced with necessary DSP chain to achieve add-drop functionality in a WDM system with small guard band.

## 4.1 Fiber-Based System with Heterodyne Detection and Analog Processing

This section describes a proof-of-concept OEO interferometer employing heterodyne detection, analog electronic processing and subsequent amplitude remodulation. The implementation demonstrates interferometric cancellation of an intensity-modulated signal and provides valuable insights into the core operating principle, fiber-length alignment procedure and phase stabilization limitations. The content of this chapter was presented at the *Conference on Lasers and Electro-Optics (CLEO)* in 2020 [C1]. The material from the publication has been adapted to comply with the layout and the structure of this thesis.

The experimental setup is depicted in Fig. 4.1. An optical carrier is generated by an external-cavity laser (ECL) with a linewidth of 100 kHz. This carrier



**Fig. 4.1:** Experimental setup of the optic-electronic-optic (OEO) interferometer with heterodyne detection and analog electronic processing path.

is intensity-modulated using a push-pull Mach-Zehnder modulator (MZM) to generate a 5 Gbit/s on-off keying (OOK). As a data signal, a pseudo-random binary sequence (PRBS) of length  $2^{11}$  is produced by an arbitrary waveform generator (AWG) and amplified using an RF amplifier.

At the input of the OEO interferometer, the transmitted signal is equally split into two paths using a 50:50 splitter. The upper path is optically transparent and called the *through* path. The lower path of the interferometer is the signal processing arm and is called the *OEO* path. In the OEO path, first heterodyne detection is performed using a balanced photodetector module (BPD, Optilab, BPR-20-M) incorporating a transimpedance amplifier (TIA). The local oscillator (LO) laser for coherent detection operates as free-running and the wavelength is tuned to achieve a 10 GHz frequency offset from the signal carrier. Two different types of LO lasers, a fiber-laser with kilohertz-class linewidth and an ECL with typical 100 kHz linewidth is used to evaluate their impact on the system performance. The detected RF signal is subsequently amplified and remodulated onto a copy of the LO using a second MZM, which is biased at the null point to achieve amplitude modulation. The propagation delay through the electronics path is around 12.5 ns. Finally, the resulting optical signal is superimposed in the output coupler with the signal from the through path.

To achieve maximum-contrast interference, the two interferometer paths must be carefully matched in terms of group delay, polarization, amplitude, and phase.

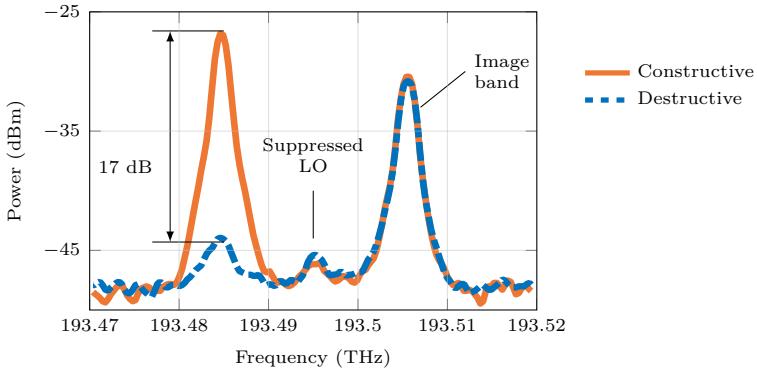
Coarse delay alignment is achieved using patch fibers of customized lengths, while fine-tuning is carried out using a variable optical delay line (ODL). A manual polarization controller (PC) is used to align the states of polarization, and a variable optical attenuator (VOA) is employed to balance the optical power levels. The relative phase difference between the two paths, which can fluctuate due to temperature variations and vibrations, is actively stabilized using a fiber-based piezoelectric phase shifter ( $\varphi$ , General Photonics, GPC-FPS-001) driven by a feedback control system. The interference power is monitored by a low-speed photodetector (PD), and the resulting signal is processed by a proportional–integral–derivative (PID) controller (LaseLock, TEM Messtechnik). The controller output voltage (0–10 V) is amplified by a high-voltage amplifier to produce the 0–150 V range required by the phase shifter, enabling a total phase tuning range of approximately 0 –  $8\pi$ .

The second port of the output coupler is used for assessing system performance. First, the image band (see Fig. 4.2) is suppressed using an optical bandpass filter (OBP) with 25 GHz bandwidth. Next, through a cascade of Erbium-doped fiber amplifiers (EDFAs) and an OBP, amplified spontaneous emission (ASE) noise is added to the signal to vary the optical-signal-to-noise ratio (OSNR). Finally, the signal is directly detected using a PD, and the bit-error ratio (BER) is measured using a BER tester (BERT, Anritsu, MP1776A).

### 4.1.1 Results and Analysis

Figure 4.2 shows the optical spectrum for both constructive (solid) and destructive interference (dashed line) measured at the output coupler. At the signal carrier frequency of 193.485 THz, an extinction ratio of  $\approx 17$  dB is achieved between the two interference cases. The LO carrier at 193.495 THz is well suppressed due to the null-point biasing of the MZM in the OEO path. The image band arising from the heterodyne detection is observed at 193.505 THz.

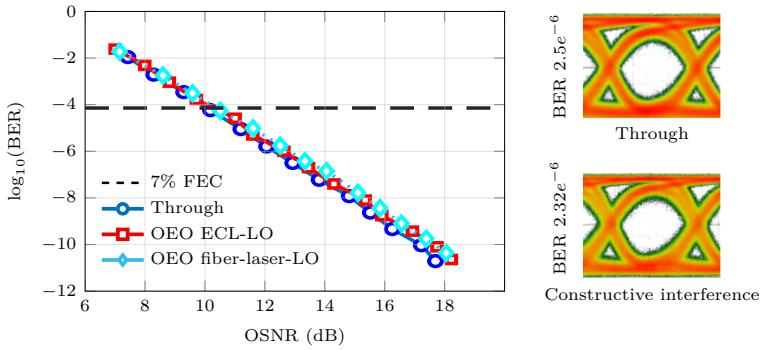
To characterize the performance of the OEO interferometric process, the controller is set to maintain the phase condition for constructive interference. Figure 4.3 shows the measured BER over a range of OSNR levels. The measurement using



**Fig. 4.2:** Measured optical spectra corresponding to constructive and destructive interference conditions, obtained using a resolution bandwidth of 20 MHz.

only the through path of the interferometer serves as the benchmark and is shown in solid blue with circle markers. For the constructive interference case, results are obtained using either an ECL (red squares) or a fiber laser (cyan diamonds) as the local oscillator (LO). The two types of LO lasers exhibit comparable performance, indicating that the two LO paths are well matched, allowing partial cancellation of LO phase noise by the remodulation. At low BER values, a small penalty of about 1 dB is observed compared to the through path. This can be attributed to the situations where the phase shifter reaches its limit and has to be reset by the controller. The corresponding eye diagrams at an OSNR of 15 dB are shown to the right of Fig. 4.1.

This section presented a proof-of-concept of OEO interferometer with optic-electronic-optic conversion in its processing path. The system demonstrated interference cancellation with 17 dB extinction ratio achieved using a fiber-based piezo phase shifter. For constructive interference, only a small OSNR penalty for a 5 Gbit/s OOK signal is observed, validating the practical viability of the approach. These findings establish a foundation for further development, where the integration of real-time digital signal processing techniques could enable enhanced and reconfigurable functionalities.



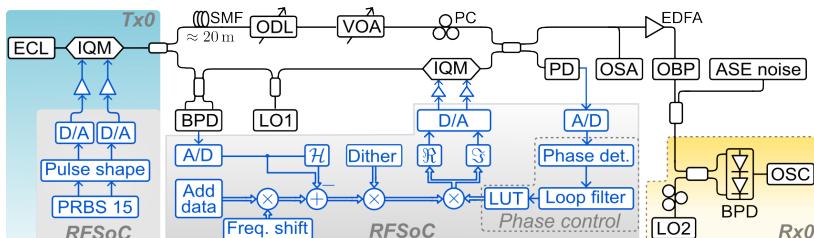
**Fig. 4.3:** Bit-error ratio (BER) as a function of optical signal-to-noise ratio (OSNR) for the individual through-path (blue circles) and for constructive OEO interference using either an ECL (red squares) or a fiber laser (cyan diamonds) as the local oscillator (LO) for a 5 Gbit/s OOK signal. The corresponding measured eye diagrams for the interference and non-interference cases are shown to the right.

## 4.2 Fiber-Based System with Heterodyne Detection and Digital Processing

The section presents the experimental realization of an OEO interferometer incorporating digital processing and coherent remodulation, demonstrating the add-drop operation of coherently modulated signals. The primary goal is to validate the core DSP framework needed for real-time operation, focusing on receiver-side analytic signal formation, transmitter-side signal generation for the added channel, and digital phase stabilization. As illustrated in Fig. 4.4, the experimental configuration comprises of three main subsystems: a transmitter (Tx0) generating the initial optical transmit signal, the central OEO interferometer responsible for the add-drop operation, and a coherent receiver (Rx0) used for signal analysis and performance evaluation. The content of this chapter was presented at the *Conference on Lasers and Electro-Optics (CLEO)* in 2023 [C2]. The material from the publication has been adapted to comply with the layout and the structure of this thesis.

A 1-GBd QPSK signal is synthesized within the FPGA fabric of a radio-frequency system-on-chip (Xilinx RFSoC ZCU111). The process involves generating two delay-decorrelated pseudorandom binary sequences (PRBSs) of length  $2^{15} - 1$ , mapping them to QPSK symbols, and applying a pulse-shaping filter using a root-raised-cosine frequency response with a roll-off factor of 0.4. Afterwards, the signal is converted to an analog waveform using two integrated 4-GHz D/A converters, sampling at a rate of 4 GSa/s. After amplification, the signal modulates an optical carrier at 193.489 THz provided by an external-cavity laser (ECL) with a linewidth of less than 100 kHz using a LiNbO<sub>3</sub> I/Q modulator (IQM).

At the interferometer input coupler, a 50/50 coupler splits the transmitted signal power into two distinct paths. In the lower path referred to as the OEO path, we perform balanced heterodyne detection utilizing a balanced photodetector module (BPD, Optilab BPR-20-M) and a free-running fiber-laser (NKT) operating at 193.490 THz with 10 kHz linewidth serving as a local oscillator (LO1). The detected electrical signal is digitized using an A/D converter sampling at 4 GSa/s with an electrical 3-dB bandwidth of 4 GHz. From this real-valued digital signal, we form a complex-valued analytic signal by generating the imaginary component using the Hilbert transform ( $\mathcal{H}$ ). The Hilbert transform is implemented by approximating it as a finite impulse response (FIR) filter in the time domain as outlined in [21, 22].



**Fig. 4.4:** Experimental setup of the coherent add-drop interferometer. The optical and electrical signal paths are visualized in black and blue, respectively. Within the DSP block (gray-shaded area), complex signals are indicated by a double arrow, while real-valued signals are shown with a single-line arrow.  $\mathcal{H}$ : Hilbert transform,  $\Re$ ,  $\Im$ : real and imaginary part, respectively.

The analytic signal is next subtracted from a digitally frequency-shifted newly generated data signal, referred to as "Add data". The "Add data" is also a 1-GBd RRC pulse-shaped QPSK waveform generated following the same process as before. In this implementation, we apply a fixed frequency shift of 1 GHz to nominally match the frequency difference of Tx0 and LO1. However, with the implementation of a real-time carrier recovery algorithm [23–26], the estimated carrier phase and frequency offset can be directly imposed onto the newly generated data signal.

Subsequently, a small-amplitude sinusoidal dither signal at a frequency of 15.6 MHz is applied, where the dither amplitude is quantized with 3-bit resolution compared to the 12-bit resolution of the received signal. The phase correction value, obtained from the look-up table (LUT) of the phase-control DSP block, is then applied to this resulting signal to compensate for the random phase fluctuations between the two interferometer paths. Additional details on the phase control mechanism are discussed later in this section. Finally, the real ( $\Re$ ) and imaginary ( $\Im$ ) components of the signal are fed to two D/A converters, amplified, and used to modulate a portion of LO1 via a second LiNbO<sub>3</sub> IQM. The resulting remodulated optical signal is then combined with the signal from the upper path using another 50/50 coupler.

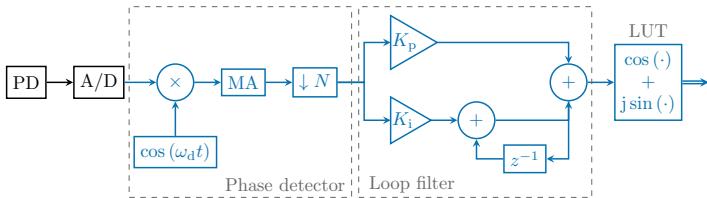
The superimposed signal from the upper output of this coupler is used for data evaluation and BER measurements. First, the signal is amplified using an Erbium-doped fiber amplifier (EDFA), filtered using an optical bandpass filter (OBP) of bandwidth 10 GHz to reduce out-of-band amplified spontaneous emission (ASE) noise. An ASE noise source is then used to variably add ASE noise and vary the optical-signal-to-noise-ratio (OSNR). Another coherent receiver, denoted as Rx0, then performs balanced heterodyne detection of the signal. The receiver uses a free-running ECL (100 kHz linewidth) as a tunable local oscillator (LO2) and a 5 –GHz bandwidth BPD (Thorlabs BDX3BA). The electrical signal is then sampled at 6.25 GSa/s using an oscilloscope (OSC, Tektronix DPO70808B) for offline evaluation. The recorded waveforms are first normalized and resampled to two samples per symbol. After that, symbol timing synchronization is achieved by applying a feedforward clock recovery [C3]. Channel distortions are corrected

using an adaptive equalizer based on a constant-modulus algorithm [27, 28]. This is followed by carrier recovery with the Viterbi & Viterbi algorithm before hard-decision demodulation [29].

For maximum suppression of the original signal through destructive interference, both interferometer paths must be well-matched in terms of group delay, polarization, amplitude, and phase. In our setup, we begin by coarsely adjusting the delay in the through path with roughly 20 m of single-mode fiber (SMF). A variable optical delay line (ODL) is then used for fine adjustments. Amplitude and polarizations are controlled using a variable optical attenuator (VOA) and a polarization controller (PC), respectively.

Despite these calibrations, the phase difference between the two paths fluctuates over time due to external disturbances, such as vibrations, temperature variations, and/or phase noise differences between the lasers in Tx0 and LO1. Consequently, active phase stabilization is required to maintain long-term stability. However, directly using interference-induced power variations as an error signal in a control loop leads to phase locking only within a limited range (0 to  $\pi$  or  $\pi$  to  $2\pi$ ) due to phase ambiguity, as power and phase do not have a one-to-one mapping (see Sec. 2.3.1). However, for proper operation of the OEO interferometer, it is essential to lock the phase at the interference extrema (maximum or minimum). To resolve this, we employ a dither-based [30, 31] approach. A small periodic phase modulation is introduced into one interferometer arm, and synchronous demodulation is used to extract the corresponding power variation derivative (see Sec. 2.3.1). The required phase correction is then applied via the second IQ modulator (IQM) in the OEO path, enabling continuous phase adjustment without range limitations [32, 33].

Figure 4.5 depicts the steps of computing the phase correction value in the PLL. First, a low-bandwidth photodetector (PD, DC - 200 MHz) converts interference power variations into an electrical signal, serving as a feedback signal. Next, the signal is digitized by an A/D converter (bandwidth: 10 MHz to 1 GHz), and then multiplied by the cosine component of the reference dither signal. The resulting output contains three frequency components: a DC term, a component at the



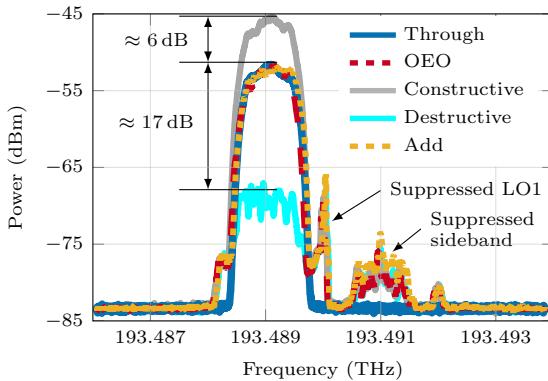
**Fig. 4.5:** Schematic of the phase control structure consisting of a phase error detector, a loop filter, and a look-up table (LUT). The control loop includes a photodiode (PD) and an analog-to-digital converter (A/D) to detect the interference power variation due to random phase drifts. An error signal around zero frequency is obtained by mixing with the reference dither and filtering the harmonics using a moving average (MA) filter. After downsampling ( $\downarrow N$ ), the signal is fed into a proportional-integral (PI) loop filter to converge to the correct phase. The LUT converts the phase to a complex sinusoidal.

dither frequency  $\omega_d$ , and/or a component at  $2\omega_d$ . A moving average (MA) filter suppresses the oscillatory terms, thereby passing only the DC term, which serves as the phase error value. The phase error signal is downsampled by a factor of 1024 relative to the FPGA clock of 250 MHz and then fed to a proportional-integral (PI) controller (loop filter) [18]. The controller parameters are optimized using the Ziegler–Nichols method [34]. Finally, the loop filter output is mapped to a look-up table (LUT) that provides the complex-valued phase correction. The LUT functions as a numerically controlled oscillator around zero frequency, and due to its inherent modulo operation on the input index, continuous phase adjustment is achieved across the entire range of 0 to  $2\pi$ .

## 4.2.1 Results and Analysis

In the following, we evaluate the performance of the OEO interferometric system for channel suppression and reinsertion of a new data signal on the same channel, based on optical spectra and BER measurements.

Figure 4.6 shows optical spectra measured with a 20 MHz resolution bandwidth at the output coupler for five different scenarios. The solid blue trace represents the spectrum when only the through path is connected, while keeping the OEO path open. In contrast, the dashed red line corresponds to the OEO path spectrum

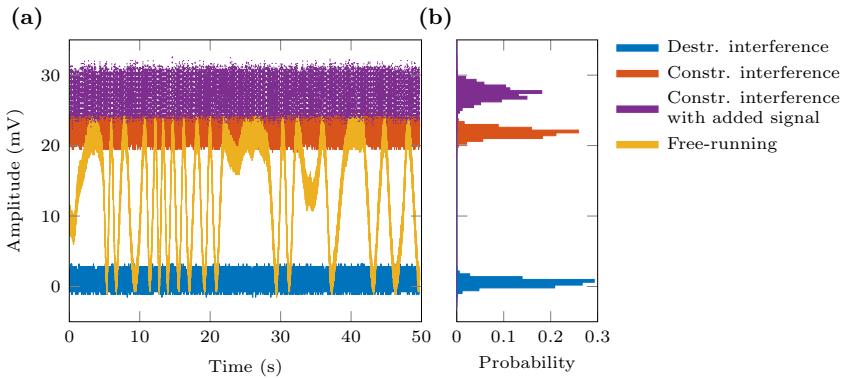


**Fig. 4.6:** Measured optical spectra (20 MHz resolution bandwidth) recorded at the interferometer output coupler for the upper (through) path and lower (OEO) path without any interference, for constructive and destructive interference, and for the case where the former signal is dropped and a new signal is added (Add).

with the through path open. At the signal carrier frequency of 193.489 THz, the optical power levels are adjusted to achieve comparable spectral intensity in both paths. It can be observed that the OEO path regenerates the original signal without any noticeable distortion. However, at 193.49 THz, the residual carrier from LO1 is visible alongside minor spectral broadening of the signal spectra caused by modulator nonlinearity. The digital Hilbert transform effectively suppresses the upper sideband near 193.491 THz by approximately 25 dB relative to the lower sideband. When both interferometer paths are simultaneously connected and the controller is tuned for constructive interference (solid gray), the signal power increases by 6 dB, verifying phase coherence. Conversely, setting the controller to destructive interference yields the solid cyan spectrum, where the signal is suppressed by approximately 17 dB relative to the through-path-only scenario. Finally, during the add operation, the introduction of a new data signal over the residual destructive interference spectrum produces the dotted orange trace. This trace exhibits a slight frequency shift, attributed to manual LO1 tuning and inherent laser frequency drift.

Figure 4.7 (a) presents the temporal evolution of the monitor PD output voltage resulting from interference-induced power variation. The yellow trace corresponds

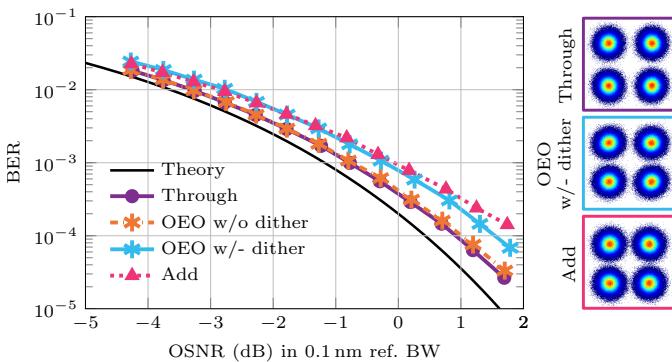
to the unstabilized interference condition, where the output voltage randomly oscillates between upper and lower extremes. The blue and red traces represent the actively stabilized PD output under destructive and constructive interference, respectively. Introducing the add-signal into the OEO path while maintaining constructive interference yields the purple trace, which corresponds to the ‘add’ spectrum depicted in Fig. 4.6. Since the two interferometer outputs have a  $180^\circ$  phase offset, a destructive interference in the upper output corresponds to constructive interference in the lower output. The related histograms for the various voltage levels are displayed in Fig. 4.7(b).



**Fig. 4.7:** Measured photodiode voltage over time (a) and corresponding histograms of the measured voltage signal (b).

The BER performance of the add-drop process is examined under varying OSNR conditions. Amplified spontaneous emission (ASE) noise is injected after the OEO interferometer, and OSNR is determined within 0.1 nm reference bandwidth. BER is measured for four distinct cases and compared with a theoretical benchmark (solid black), which is derived analytically for a 1 GBd QPSK signal over an additive white Gaussian noise (AWGN) channel, as plotted in Fig. 4.8. Due to ASE noise folding from the image band in heterodyne reception, an additional 3 dB penalty is included, consistent with prior studies [35–38].

The BER measured using only the through path (solid purple line, circle marker) establishes a baseline for optical back-to-back characterization. BER measurements for the OEO path alone are first obtained without dither (dashed orange) and then with dither enabled (solid cyan), showing a sensitivity penalty of approximately 0.5 dB at a BER of  $10^{-3}$ . This penalty could potentially be mitigated by refining the bit resolutions of DSP signals and/or reducing the dither frequency (see Fig. 4.4). When the new add-signal is inserted (dotted magenta, triangle marker) in place of the dropped channel, an additional 0.1 dB penalty is observed due to linear crosstalk from the residual drop signal. Consequently, the total OSNR penalty introduced by the add-drop process, including both dither tone and crosstalk effects, is around 0.6 dB for QPSK modulation.



**Fig. 4.8:** BER measurements with varying OSNR for the transmitted QPSK signal before and after interferometric add-drop operation. The insets show the corresponding constellations ( $10^5$  symbols plotted) for the cases of through, OEO with dither, and after add-drop operation (Add).

The constellation diagrams shown to the right, obtained at an OSNR of 1.7 dB, correspond to the BER performance described earlier. From top to bottom, the diagrams represent the through path, the OEO path with dither, and the add-drop scenario, respectively. These results demonstrate that the system can replace an existing channel with a new signal while incurring minimal performance penalty, highlighting its potential for use in future high-capacity optical networks.

## 4.3 Integrated Module with Heterodyne Detection and Digital Processing

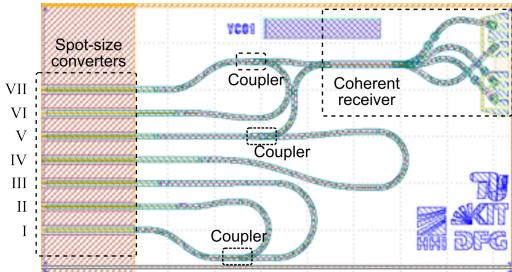
In this section, the performance of an integrated OEO interferometer module is experimentally characterized. The core photonic-integrated circuit (PIC) implements partial integration of the OEO interferometer, comprising primarily of passive waveguides routing combined with an on-chip coherent photodetector. The device is presented in its fully packaged form and subsequently employed in the coherent add-drop experiment. Some of the results and discussions in this section were originally presented at the *Conference on Lasers and Electro-Optics (CLEO)* in 2024 [C4]. The content has been modified to fit the thesis framework and provide a cohesive narrative.

### 4.3.1 PIC Design Features

The PIC was fabricated on an indium phosphide (InP) platform using the Fraunhofer Heinrich-Hertz-Institute (HHI) multi-project wafer (MPW) process. A top-view photograph of the designed circuit is shown in Fig. 4.9. For efficient fiber-to-chip coupling, the PIC incorporates single-mode fiber spot-size converters. The optical interface is labeled from I to VII. It also integrates three multi-mode interference (MMI) couplers and a coherent photodetector. The coherent photodetector is implemented using a  $2 \times 4$  MMI coupler to form a  $90^\circ$  optical hybrid (OH), followed by four photodiodes. This implementation serves as an intermediate step towards a fully-integrated version.

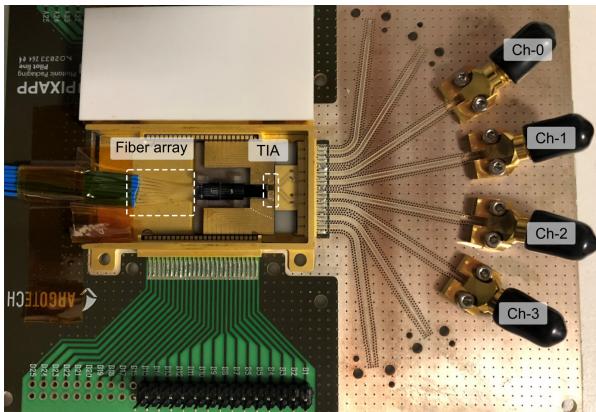
### 4.3.2 Module Packaging and Interface Characterization

Figure 4.10 shows the final packaged module mounted on the evaluation board. The module is housed in a generic enclosure provided by the EU PIXAPP project, designed for photonic integrated circuit packaging. Inside the housing, a polarization-maintaining eight-channel fiber array (which is one channel



**Fig. 4.9:** Top-view image of the partially integrated OEO interferometer PIC with highlighting the coherent receiver, three couplers, and spot-size converters.

more than the number of optical interfaces shown in Fig. 4.9) is actively aligned and edge-coupled to the chip facets to ensure optimal optical coupling efficiency. The interferometer PIC and a commercially available trans-impedance amplifier (TIA) are mounted together on a ceramic substrate. The TIA is wire-bonded to the on-chip coherent receiver pads, providing differential electrical outputs that are routed to V-connectors for high-frequency measurements. Both the DC and RF pads of the TIA are electrically connected to corresponding interfaces within the housing. In the OEO interferometer setup, this module functions as the coherent



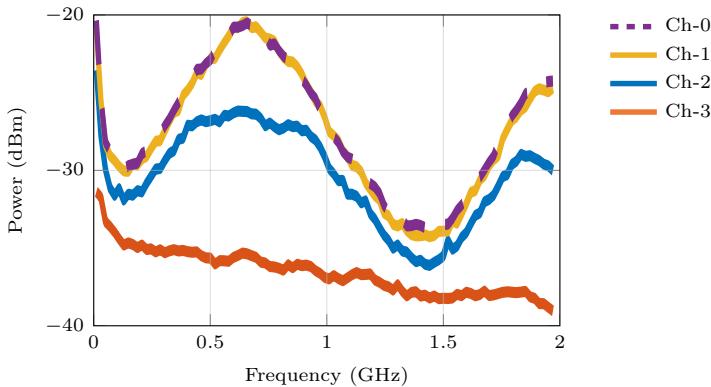
**Fig. 4.10:** A photograph of the packaged module with evaluation board showing the fiber array edge-coupled to the chip. The four differential electrical outputs of the coherent receiver are labeled from Ch-0 to Ch-3.

receiver. The electrical interfaces are labeled ch-0 through ch-3 in the figure, corresponding to the four photodiode channels of the coherent receiver.

To quantify the insertion loss through the optical interface, a continuous-wave (CW) laser output power of 0 dBm is fed to one input port (e.g., interface I in Fig. 4.9) via a polarization controller and the attached PM fiber. The output power through the corresponding output port is measured using an optical power meter. Table 4.1 summarizes the measured insertion loss for several input-output port combinations. These measurements include coupling losses at the fiber–chip interfaces and the inherent 3 dB loss from the MMI couplers. The reference power level was measured with a direct fiber–fiber connection, yielding an insertion loss uncertainty of approximately  $\pm 0.2$  dB.

Interface in to out	Insertion loss (dB)
I to II	$\approx 7$
I to III	$\approx 7$
V to IV	$\approx 8.3$
VII to VI	$\approx 7$

**Table 4.1:** Measured insertion loss of the packaged module through various optical input and output interfaces indicated as in Fig. 4.9.

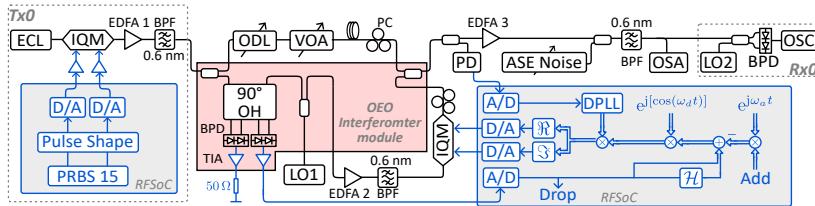


**Fig. 4.11:** Electrical bandwidth characterization of all four channels of the coherent detector output in the packaged module (see Fig. 4.10).

A heterodyne bandwidth measurement is then carried out using an electrical spectrum analyzer (ESA) (Fig. 4.11). The measurement used TE-polarized light at a wavelength of 1550 nm. The heterodyne signal is generated by inserting two CW laser outputs through the optical ports VII and V, with sweeping one laser's carrier frequency to produce a frequency offset from 0 to 2 GHz. Channels labeled Ch-0 and Ch-1 in Fig. 4.10 exhibit nearly identical responses, whereas the responses from ch-2 and ch-3 diverged significantly within the tested frequency span, which later influenced the channel selection in the subsequent experiment.

### 4.3.3 Experimental Setup

The experimental setup, which includes the photonic module along with external off-chip delay and remodulation paths, is shown in Fig. 4.12. The components of the integrated module are highlighted within a red-shaded area. The transmit signal generation follows the same approach as described in Sec. 4.2. A Xilinx RFSoC (ZCU111) with integrated 4 GSa/s D/A converters produces an 1 GBd QPSK waveform, shaped by a root-raised cosine filter with a roll-off  $\beta = 0.4$ . This waveform then modulates an external cavity laser (ECL) using an IQ modulator (IQM).



**Fig. 4.12:** Experimental setup using the integrated OEO interferometer module. ODL: Optical delay line, VOA: Variable optical attenuator, PC: Polarization controller, OBP: Optical bandpass filter.

The transmitted optical signal is amplified and then fed into the integrated module. Inside the PIC, this signal is split into two paths: a through path exiting the PIC and an OEO path directed to the on-chip coherent receiver. A free-running laser

(LO1) with a linewidth below 10 kHz is also split within the PIC. One part of the laser light is routed to the coherent receiver, while the other exits the PIC. Since balanced heterodyne detection is performed in this experiment, only one channel of the BPD/TIA output is used while the other channel is terminated by a matched  $50\Omega$  load. The resulting electrical signal is digitized by a 4 GSa/s A/D converter on the RFSoC.

Building on the previously described DSP processing, we apply the Hilbert Transform ( $\mathcal{H}$ ) to the received electrical signal and generate an analytic signal. A 1 GBd QPSK signal labeled as "Add" is digitally frequency shifted by multiplying with a complex exponential  $\exp[j\omega_a t]$  and the resulting signal is subtracted from the analytic signal. The frequency shift  $f_a = \omega_a/2\pi$  is roughly 1 GHz, similar to the implementation in Sec 4.2.

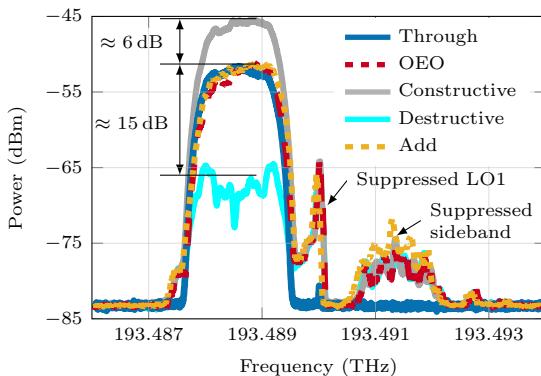
Next, the resulting difference signal is multiplied by a phase dithering term  $\exp[j \cos(\omega_d t)]$ , followed by multiplication with the output of the digital phase-locked loop (DPLL). The real and imaginary components of this signal are then used to modulate a portion of LO1 via a second IQM. Both the remodulated optical signal and the through-path signal are inserted back into the PIC, where they are superimposed and coupled out of the chip. The superimposed signal output from the module is then split into two paths: one path is directed to a coherent receiver (Rx0) for BER analysis through offline DSP, while the other is detected using a low-bandwidth photodetector (PD) with a bandwidth from DC - 200 MHz, producing a feedback signal for phase stabilization. Using a lock-in technique described in the previous section, the phase-error signal is extracted by the DPLL, and phase correction values are calculated by a PI controller. In the external delay path, coarse group delay matching between the two interferometer arms is achieved with patch cords, while fine adjustment is performed using a variable optical delay line (ODL). A variable optical attenuator (VOA) and polarization controller (PC) are then used to optimize the interference amplitude and polarization state.

### 4.3.4 Results and Analysis

Following the methodology outlined earlier, we evaluate the performance of the interferometric add-drop operation using optical spectral analysis and BER measurements.

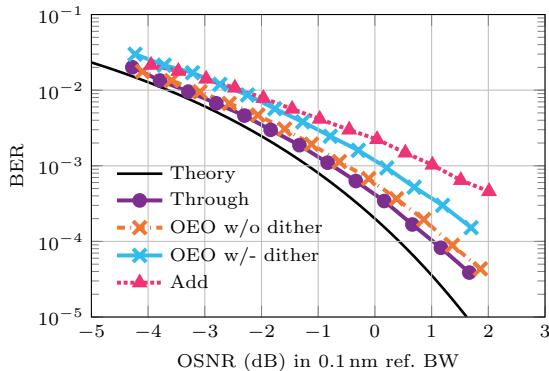
Figure 4.13 presents the optical spectra obtained under five distinct conditions, with a portion of the PD input tapped for measurement. The solid blue and dashed red traces represent the spectra of the individual interferometer through and OEO paths, respectively. The solid gray and solid cyan traces represent constructive and destructive interference, leading to a 6 dB power enhancement and an extinction ratio of 15 dB, respectively, compared to the individual paths. The dashed yellow trace represents the spectrum following the add process. Similar to the measurements in the earlier section, all spectra, except for the interferometer through path, exhibit suppression of LO1 near 193.49 THz and effective attenuation of the upper sideband near 193.491 THz, an effect of the digital Hilbert transform.

Figure 4.14 illustrates the measured BER as a function of OSNR for this integrated module-based setup. While the overall trends align with the previous full-fiber-based setup measurements, a slight increase in BER penalties is observed. The theoretical curve obtained analytically for an AWGN channel is shown in solid



**Fig. 4.13:** Measured optical spectra (20 MHz resolution bandwidth) for individual through path and OEO path, for constructive and destructive interference and for the add-drop operation (Add).

black. The through path (circle marker) again serves as the baseline measurement. The OEO path without dithering (dash-dotted orange) exhibits a 0.2 dB penalty, while enabling the dither signal (solid cyan) introduces an additional 0.6 dB penalty at a BER of  $10^{-3}$ . Both penalties are slightly higher than those observed in the fiber-based measurement. For the add operation (dotted line with triangle marker), the overall penalty amounts to 1.3 dB, which correlates with the 2 dB lower extinction ratio compared to the full-fiber-based implementation. The increased penalty may result from length mismatch and polarization misalignment introduced during fiber-to-chip coupling, particularly due to the off-chip single-mode fiber delay in the through path.



**Fig. 4.14:** Measured BER curves over varying OSNR with the integrated module, illustrating the performance impact of the interferometric add–drop operation.

In summary, we have demonstrated a functional OEO interferometer module based on an InP PIC incorporating passive waveguides and a coherent receiver. The module achieves a coherent add-drop operation of 1-GBd QPSK signals with only a slight penalty increase compared to the fiber-based setup. This small additional penalty, caused by fiber-to-chip coupling issues, can be mitigated with careful system optimization. With further refinement, such integrated solutions offer a promising path toward compact, scalable, and fully integrated interferometric optical add-drop multiplexing systems.

## 4.4 Fiber-Based System with Intradyne Detection for WDM Signals

Building upon the single-channel heterodyne detection experiment, which enabled the development of minimal receiver-side DSP and a robust phase control algorithm, the setup is now extended to support multicarrier WDM operation using coherent intradyne detection. Heterodyne detection, while suitable for initial proof-of-concept demonstrations, is inherently unsuited for WDM reception due to channel spacing and filtering constraints. In the new configuration, the transmitter-side add process and the phase control mechanism from the previous implementation are retained, while additional DSP functions are introduced at the receiver to enable multichannel processing. The use of intradyne detection also allows the symbol rate to be increased to 2 GBd, given the available 4 GSa/s sampling rate. Some of the results and discussions in this section have been originally submitted as a book chapter to Springer in 2025 [B1].

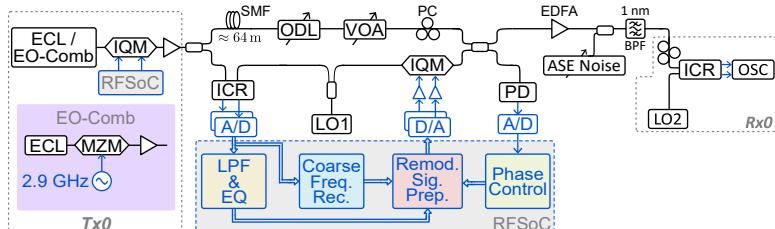
The experimental configuration is illustrated in Fig. 4.15. The transmitter (Tx0) now features an electro-optic frequency comb (EO-COMB) implemented using a Mach-Zehnder modulator (MZM), as detailed in the inset. The MZM is driven in a push-pull configuration by a 2.9 GHz sinusoidal RF tone from a synthesizer. The drive voltage is tuned to produce only three spectral lines, the carrier ( $0^{\text{th}}$  order) and the first-order sidebands ( $\pm 1^{\text{st}}$ ). The MZM bias is further adjusted to equalize the power of these three spectral lines.

Each comb line is subsequently modulated with a 2-GBd QPSK waveform that is pulse-shaped using an RRC frequency response with a roll-off factor of 0.1. As in previous implementations, the transmit signal is split into an upper through path and a lower OEO path. In the OEO path, coherent intradyne detection is performed using an integrated coherent receiver (ICR, Fujitsu FIM24902) together with a narrow-linewidth (10 kHz) fiber laser (LO1) serving as the local oscillator. The resulting I/Q signals are digitized using two A/D converters operating at 4 GSa/s, and processed through a series of DSP stages. These operations are organized into three functional blocks: lowpass filtering (LPF) & equalization

(EQ), coarse frequency recovery (Coarse Freq. Rec.), and remodulation signal preparation (Remod. Sig. Prep.). The remodulation block produces a tailored waveform that drives an I/Q modulator to modulate a portion of LO1 for further interferometric processing. The structure and operational principles of each DSP stage are examined in detail later in this section.

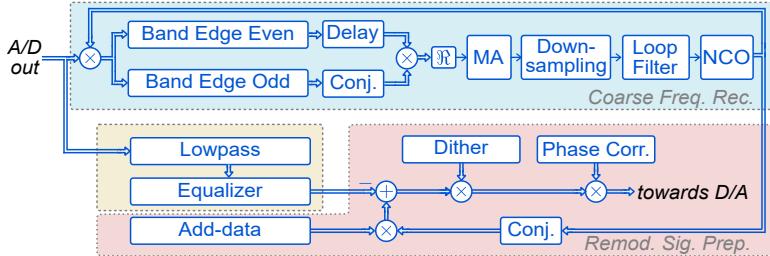
A fiber delay of approximately 64 m, implemented using several custom-length single-mode fiber (SMF) patch cords, is inserted into the through path to achieve coarse group delay alignment with the OEO path. Following the approach of previous implementations, one interferometer output is fed to a PD for phase control. The other output is directed to a receiver (Rx0) that uses a separate ECL (100 kHz linewidth) as the LO (LO2) and an ICR. After ASE noise loading, the signal is sampled at 4 GSa/s using an oscilloscope (OSC) and processed offline as described in Section 4.2.

The DSP architecture implemented in the OEO path is illustrated in Fig. 4.16, with the corresponding filter responses shown in Fig. 4.17. The received I/Q signal is processed along two parallel branches, each addressing different signal conditioning tasks. In the first branch, a coarse frequency offset compensation algorithm is employed. A 15-tap band-edge filter, whose frequency response is shown in Fig. 4.17(a), is used to estimate the frequency offset between Tx0 and LO1 [20]. For efficient implementation, the filter response is decomposed into even and odd components, taking advantage of the properties that the imaginary



**Fig. 4.15:** Experimental setup of the coherent add-drop interferometer based on intradyne reception for WDM operation. Optical and electrical signal paths are represented by black and blue lines, respectively. Within the gray-shaded DSP block, complex-valued signals are denoted by double arrows, and real-valued signals by single-line arrows. ECL: External cavity laser, ODL: optical delay line PC: polarization controller, ICR: integrated coherent receiver.

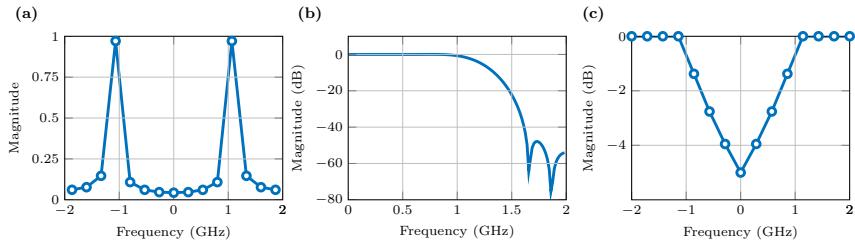
part of the even filter and the real part of the odd filter are zero. The even filter output is delayed and multiplied by the conjugate of the odd filter output.



**Fig. 4.16:** Block diagram of the DSP workflow in the OEO path supporting add-drop operation for WDM signals. Functional blocks for coarse frequency offset recovery, received signal equalization, and remodulation signal synthesis are highlighted with blue, yellow, and red shading, respectively.

The real part of the resulting product provides the frequency error estimate. This error signal is first smoothed using a moving average (MA) filter, then downsampled, and finally processed through a PI loop filter. The output of this loop filter drives a numerically controlled oscillator (NCO), which synthesizes a complex exponential corresponding to the estimated frequency offset. The NCO output is applied to the received I/Q waveform to complete the feedback path, while its conjugate is simultaneously used to impose the corresponding frequency shift on the add-data signal.

In the second branch, the received signal is filtered using a Kaiser-windowed lowpass filter (Fig. 4.17(b)) to suppress out-of-band spectral components. This is followed by an equalizer, designed to mitigate spectral distortion introduced by the ICR and the second transmitter. The equalizer employs a 15-tap inverse-triangle spectral response, shown in Fig. 4.17(c). The equalized signal is then subtracted from the frequency-shifted add-data signal. Following this, a phase-dither signal and a phase correction signal from the phase control module (see Fig. 4.5) are applied. Finally, the real and imaginary components are routed to D/As to drive an I/Q modulator for signal regeneration.

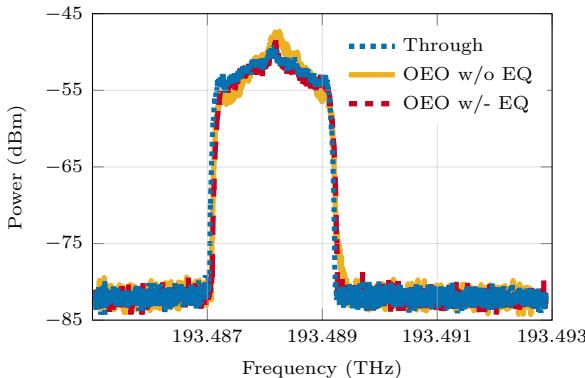


**Fig. 4.17:** Frequency responses of FIR filters used in the DSP chain: (a) 15-tap band-edge filter for frequency offset recovery; (b) lowpass filter designed using a Kaiser window; (c) 15-tap inverted-triangle filter response used for spectral shaping.

## 4.4.1 Results and Analysis

### Single-Carrier Signal

To assess the performance of the intradyne-based OEO interferometer, we first use a single-carrier signal. This enables the evaluation of ICR performance and allows careful optimization of the OEO path's DSP operations, particularly the equalizer, phase-locked loop, and frequency-locked loop.



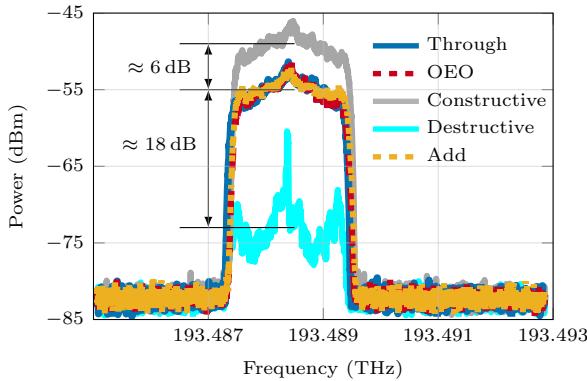
**Fig. 4.18:** Comparison of optical spectra for the through path (blue), the OEO path without equalization (yellow), and with the equalizer (red), measured with a resolution bandwidth of 20 MHz.

Figure 4.18 illustrates optical spectra at the interferometer output coupler for the individual through and OEO paths, with and without equalization (EQ). The dotted blue trace corresponds to the through path and reflects only the spectral response of Tx0. A linear reduction in spectral power from the center peak toward the band edges produces a characteristic triangular spectral envelope. The nonuniform low-frequency response of the D/A and the RF amplifier likely causes this spectral shape. The solid yellow trace shows the OEO path spectrum without equalization, which exhibits a noticeably steeper decline in spectral power across the signal bandwidth. This spectrum reflects the combined frequency response of Tx0, the ICR, and the transmitter in the OEO path. The steeper roll-off is attributed to the cascaded effect of the two transmitters and the contributions from the elevated baseband noise introduced by the ICR's TIA. When the equalizer is enabled (dashed red trace), the OEO spectrum exhibits effective compensation for these distortions, resulting in a spectral shape comparable to that of the through path.

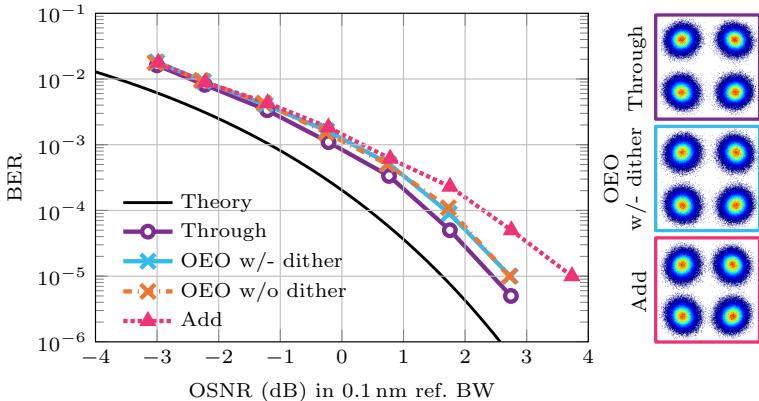
Figure 4.19 illustrates optical spectra, measured with the complete OEO DSP chain enabled in the intradyne configuration. The solid blue curve corresponds to the through path alone, whereas the dashed red curve corresponds to the OEO path. As in the heterodyne case, the signal powers of both paths are carefully adjusted to yield comparable spectral power levels within the signal band. When both interferometer arms are connected and the phase controller is tuned for constructive interference (solid gray trace), a power enhancement of roughly 6 dB is observed, indicating phase coherence. In contrast, the solid cyan trace represents the destructive interference case, where the signal is suppressed by about 18 dB relative to the through-path-only case. These relative power levels are estimated by averaging power within a 2 GHz spectral window centered at the peak. Residual leakage of LO1 is also evident at the center of the signal band. The attenuation exhibits a slight frequency dependence, being lowest near DC, which can be attributed to increased TIA noise and LO1 leakage arising from gradual bias drift in the IQ modulator. At the outer edges of the signal band, a similar reduction in attenuation is also evident. Lastly, introducing the add-data waveform while the controller is tuned to destructive interference produces the

dotted yellow spectrum. Here, the add-data signal is digitally scaled to match the power levels of the individual paths.

The BER performance of the single-carrier intradyne detection configuration is presented in Fig. 4.20. As in the heterodyne case, BER values are measured for four distinct cases, and OSNR is evaluated within a 0.1 nm reference bandwidth.



**Fig. 4.19:** Optical spectra (20 MHz resolution) of a 2 GBd QPSK signal recorded at the interferometer output for individual through/OEO paths, constructive/destructive interference, and add operation.



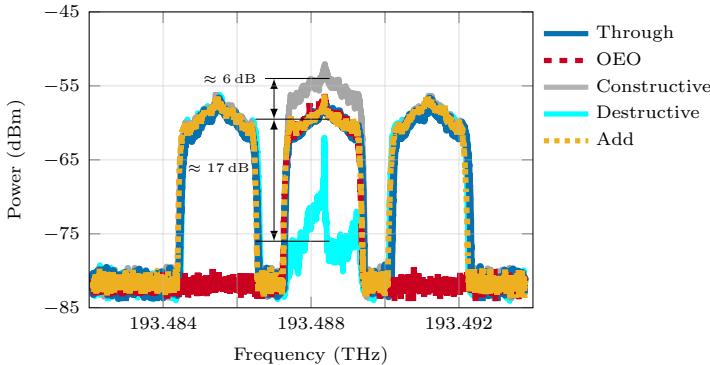
**Fig. 4.20:** BER vs OSNR for intradyne-detected single-carrier signal with corresponding constellations at 2.7 dB OSNR.

The analytical BER curve for a 2 GBd QPSK signal in an AWGN channel is plotted as a solid black line. The solid purple line with circular marker shows the BER for the through path alone, serving as an optical back-to-back reference. The OEO path without dither (dashed orange) and with dither (solid cyan) both exhibit a small 0.3 dB OSNR penalty at a BER of  $10^{-3}$ , attributed to the optic–electronic–optic conversion steps. Notably, after careful optimization of the digital scaling parameters within the DPLL, the inclusion of the dither signal produces no measurable additional penalty. When the add-data signal is enabled (dotted magenta) in place of the dropped channel, a further penalty of 0.1 dB is observed, attributed to linear crosstalk from the residual drop signal. Overall, the total OSNR penalty from the complete add–drop process, accounting for both OEO conversion and crosstalk effects, is approximately 0.4 dB. The inset presents constellation diagrams measured at an OSNR of 2.75 dB, arranged from top to bottom for the through path, the OEO path with dither, and the add-data case.

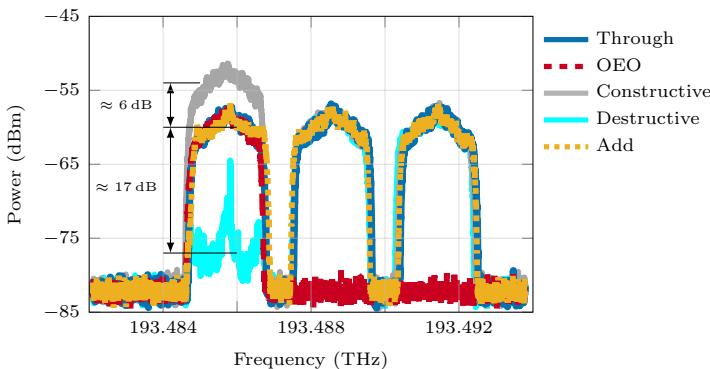
## Multi-Carrier WDM Signal

Figure 4.21 presents the measured optical spectra for a three-channel WDM signal with 2.9 GHz channel spacing. The blue trace corresponds to the spectrum obtained from the through path alone, while the dashed red line shows the spectrum from the OEO path alone with the center channel reinserted via OEO remodulation. When both paths are combined with the controller tuned for constructive interference, the resulting spectrum (solid gray) shows a 6 dB increase in the peak power of the center channel, consistent with earlier single-channel results. Destructive interference is illustrated by the solid cyan curve, exhibiting approximately 17 dB suppression of the center channel relative to the individual paths. This suppression is quantified as the average power reduction within a 2 GHz bandwidth centered around the peak spectral power of the center channel. The outcome of the add operation applied to the center channel is shown by the dotted yellow trace. For comparison, Fig. 4.22 and Fig. 4.23 display the corresponding spectra when the add-drop functionality is applied to the left and right WDM channels, respectively. For the right channel, the destructive interference

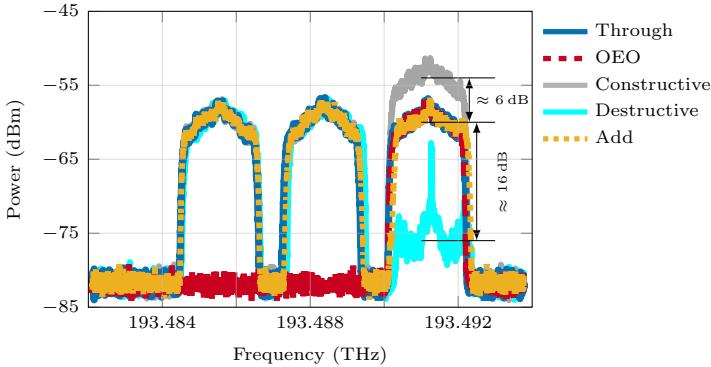
condition (Fig. 4.23) exhibits 1 dB less extinction compared to the left or center channels. This reduction is attributed to increased residual leakage from LO1, likely stemming from bias drift in the IQ modulator of the OEO path.



**Fig. 4.21:** Optical spectra at the interferometer output for the three channel WDM signal with add-drop of the center channel (20 MHz resolution bandwidth).

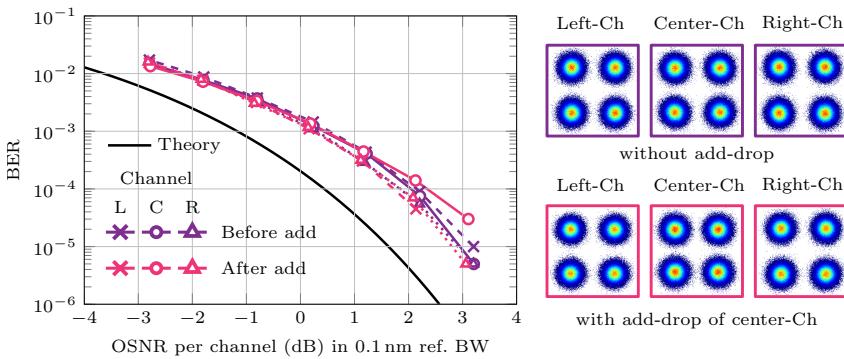


**Fig. 4.22:** Optical spectra at the interferometer output for the three channel WDM signal with add-drop of the left channel. The resolution bandwidth is 20 MHz.



**Fig. 4.23:** Optical spectra at the interferometer output for the three channel WDM signal with add-drop of the right channel. The resolution bandwidth is 20 MHz.

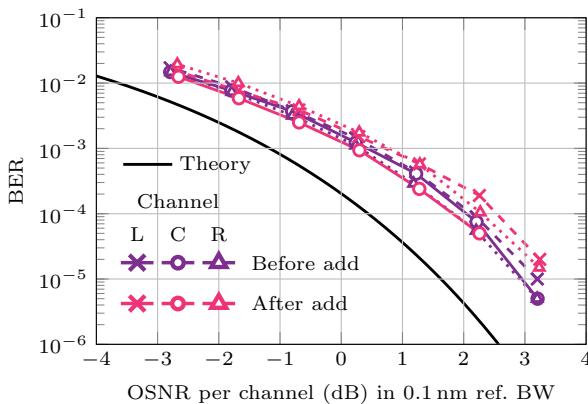
BER measurements for all three WDM channels were conducted before and after performing an add-drop operation on the center channel. The EO-Comb was adjusted to ensure equal peak power across all channels, and the optical spectrum analyzer (OSA) resolution bandwidth was set to 0.1 nm, wide enough to contain all three channels of the WDM signal. The results are depicted in Fig. 4.24 alongside the analytical BER curve for 2 GBd QPSK signal in an AWGN channel. The measurement labeled as “before add” (purple curve) corresponds to the case



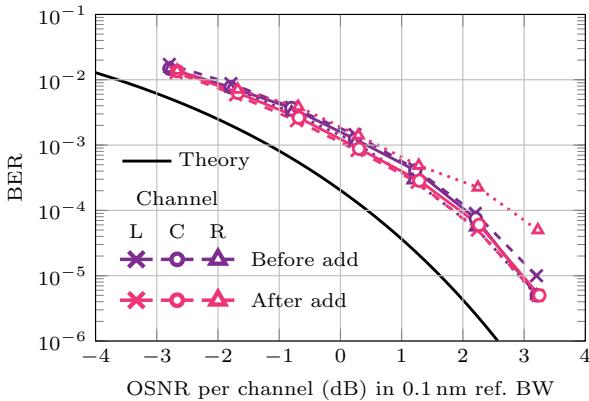
**Fig. 4.24:** BER measurements for three WDM channels before and after add-drop of the central channel (left). Corresponding constellations at 3 dB OSNR (right).

where only the through path was active. The “after add” operation case (magenta curve) represents the scenario in which a new data signal is inserted at the central wavelength channel using the OEO interferometer. At BER values above  $10^{-3}$ , all three channels exhibit comparable BER performance before and after the *add* operation. A minor penalty of approximately 0.4 dB is observed at lower BER values (e.g., at  $10^{-4}$ ) for the central channel after the add operation, attributed primarily to residual crosstalk from incomplete suppression during the drop stage. This BER performance is consistent with the constellation diagrams shown on the right of Fig. 4.24. These constellations, captured at an OSNR of 3 dB, illustrate the signal quality for the three WDM channels without (top) and with (bottom) the add-drop operation.

The same performance trend is observed when the add-drop operation is applied to the left and right WDM channels, as shown in Fig. 4.25 and Fig. 4.26, respectively. For the right channel, a slightly elevated BER is noted after the add-drop operation at OSNR levels above 2 dB, correlating with the reduced extinction (by approximately 1 dB) during the drop stage, as seen in Fig. 4.23. These results confirm the scalability of the OEO-based add-drop architecture to multi-channel WDM systems, maintaining consistent performance across all channels with only minor and manageable crosstalk penalties. This chapter presented a systematic



**Fig. 4.25:** BER measurements for three WDM channels before and after add-drop of the left channel.



**Fig. 4.26:** BER measurements for three WDM channels before and after add-drop of the right channel.

experimental investigation of the OEO interferometer through four progressively advanced implementations. The initial proof-of-concept experiment, based on heterodyne detection with analog processing, demonstrated only the interferometric cancellation of an intensity-modulated signal. The subsequent experiment incorporated DSP while still using heterodyne detection, enabling full coherent add-drop operation for a single-carrier 1 GBd QPSK signal. The third study evaluated a partially integrated interferometer module, showing that a compact, packaged implementation is feasible while maintaining coherent add-drop functionality. The substantial DSP-induced delays required the through-path delay to be implemented off-chip. This experiment confirmed that the phase control structure developed in this thesis continues to provide stable operation and preserves optimal phase alignment even with off-chip delays.

Finally, the intradyne detection configuration extended the system to a WDM input with 2 GBd QPSK channels. This setup revealed noticeable spectral deformation in the OEO path due to successive OEO conversions, primarily resulting from the non-uniform response of the DAC, RF amplifier, and ICR near DC. Equalization was necessary to restore the spectral shape and achieve reasonable spectral suppression. Careful optimization of the digital scaling in the DPLL eliminated the

OSNR penalty previously observed with the dither signal in the heterodyne DSP experiment. Across all experiments, extinction ratios remained within 16–18 dB.

Overall, these experiments validate the OEO-based architecture for flexible coherent add-drop applications. They demonstrate phase-coherent operation, minimal OSNR penalties, and manageable crosstalk across single-channel and multi-channel scenarios. Furthermore, the studies provide practical insights into DSP design, phase control, and module integration, establishing a solid foundation for the further development of integrated OEO interferometers.



# 5 Summary and Outlook

## 5.1 Summary

The research presented in this thesis reports the first experimental demonstration of an optic-electronic-optic (OEO) interferometer performing coherent add–drop operation on wavelength-division multiplexing (WDM) signals with narrow guard bands. The system is implemented on an radio-frequency system-on-chip (RF-SoC) platform with FPGA-based real-time digital signal processing (DSP). The final WDM experiment validates coherent add–drop operation on a three-channel WDM signal, where each channel carries a 2 GBd QPSK signal with a 2.2 GHz passband and a 0.7 GHz guard band. These results highlight the system’s ability to manipulate spectrally compact signals with high fidelity.

Across all experiments, the OEO interferometer consistently achieved an extinction ratio of approximately 18 dB. The dither-based phase stabilization introduced no additional penalties beyond the intrinsic effects of the OEO conversion process. In the final WDM experiments, only a minor optical signal-to-noise ratio (OSNR) penalty of 0.4–0.5 dB was observed at a bit-error ratio (BER) of  $10^{-4}$ , confirming the effectiveness of coherent add–drop operation under practical conditions.

The work further explores the path toward photonic integration. An initial integrated module, incorporating the passive waveguides and a coherent receiver, provided notable compactness compared to the discrete setup. Experimental results with the integrated module confirmed reliable phase and polarization stability equivalent to the discrete implementation, and the dither-based phase-locked loop operated seamlessly, unaffected by the off-chip delay. Collectively, the experiments demonstrate that the OEO approach meets the key performance

requirements for coherent add–drop operation in spectrally compact WDM systems, while offering a clear path toward more compact and scalable integrated implementations.

## 5.2 Outlook

The experimental results presented in this thesis provide a solid foundation for future investigations and enhancements of OEO-based coherent add–drop multiplexers. Several directions can be pursued to extend the performance and applicability of this technology:

### **Higher Data Rates and Advanced Modulation Schemes:**

In this work, the current symbol rate is limited by the bandwidth of the RFSoC’s data converters. Future experiments will leverage faster synchronous D/A and A/D converters interfaced with real-time FPGA hardware to achieve higher symbol rates. Moreover, exploring higher-order modulation formats such as 16-QAM will allow the evaluation of OEO performance under more spectrally efficient signaling conditions.

### **Impact of ECL-based LO on Performance:**

In this thesis, a kHz-linewidth fiber laser is used as the local oscillator (LO). Future studies will investigate the use of an external cavity laser (ECL) with a typical linewidth of 100 kHz as the LO in the OEO path. Such implementation will require precise matching of the LO paths, with tolerances on the order of roughly 10 cm [15], and will support a more compact module through photonic integration.

### **Photonic Integration and Compactness:**

The partially integrated OEO interferometer demonstrates that integration preserves system performance. Since the DSP operations introduce a significant processing delay, a corresponding optical delay on the order of 60–100 m is required, making a fiber-based off-chip delay line essential. Moving towards a fully integrated module, including the LO laser and an in-phase/quadrature (I/Q)

modulator, will necessitate an off-chip delay path for the LO. These fiber-based delays can be coiled to maintain a compact footprint. Full integration is expected to substantially reduce the system footprint and enhance robustness, providing a pathway toward scalable coherent optical network nodes.

### **Overlapping Spectral Multiplexing:**

To handle overlapping spectral formats, such as multi-carrier offset-QAM, the OEO interferometer will require additional real-time DSP algorithms. These algorithms must support symbol-level demodulation, with precise frequency and phase offset estimation and compensation to maintain signal integrity in dense multiplexing scenarios. A description of offset-QAM and its relevance to this work is provided in the Appendix B. These studies will build directly on the DSP framework developed for WDM operation in this thesis.

### **Dual-Polarization Systems:**

Future experiments will explore dual-polarization OEO architectures. Achieving high-performance coherent operation in such systems will require multiple-input multiple-output (MIMO) equalization strategies, which can be integrated into the DSP framework developed in this work.

### **Applications Beyond Communication:**

Beyond WDM networks, the OEO approach may find applications in photonic sensing, computing (such as Ising machines), and coherent feedback systems. Its ability to bridge optical and electronic domains with high-fidelity waveform control positions it as a versatile platform for emerging photonic technologies.

Taken together, these directions demonstrate that OEO-based interferometric systems can provide scalable, flexible, and high-performance solutions for next-generation coherent optical networks and a broad range of emerging photonic applications.



# Appendices



# A Equivalence of Band-Edge Filtering Approaches for Frequency Offset Error Signals

In the following, the formation of even and odd band edge filters from the upper and lower band edge frequency response is explained. It is also mathematically shown how the even and off filter results in the same error value as with the use of the upper and lower band edge filter.

$$H_{\text{BE,ev}}(f) = H_{\text{BEL}}(f) + H_{\text{BEU}}(f),$$
$$H_{\text{BE,od}}(f) = H_{\text{BEL}}(f) - H_{\text{BEU}}(f),$$

The outputs of even and odd band edge filters as,

$$z_{\text{BE,ev}}(nT_s) = z_{\text{BEL}}(nT_s) + z_{\text{BEU}}(nT_s),$$
$$z_{\text{BE,od}}(nT_s) = z_{\text{BEL}}(nT_s) - z_{\text{BEU}}(nT_s), \quad (\text{A.1})$$

where  $z_{\text{BEL}}(nT_s)$  and  $z_{\text{BEU}}(nT_s)$  are the outputs of the upper and lower band edge filters respectively.

## Formation of the error signal

So the frequency error from the band edge even and odd filter can then be defined as,

$$e[n] = \Re\{z_{\text{BE,ev}}(nT_s) \cdot z_{\text{BE,od}}^*(nT_s)\}$$

Pluggin in the definition of even on odd band edge filter form Eq. A.1, the error signal becomes,

$$\begin{aligned}
e[n] &= \Re \left\{ (z_{\text{BEL}}(nT_s) + z_{\text{BEU}}(nT_s)) (z_{\text{BEL}}(nT_s) - z_{\text{BEU}}(nT_s))^* \right\} \\
&= \Re \left\{ z_{\text{BEL}}(nT_s) z_{\text{BEL}}^*(nT_s) - z_{\text{BEU}}(nT_s) z_{\text{BEU}}^*(nT_s) - \right. \\
&\quad \left. z_{\text{BEL}}(nT_s) z_{\text{BEU}}^*(nT_s) + z_{\text{BEU}}(nT_s) z_{\text{BEL}}^*(nT_s) \right\} \quad (\text{A.2}) \\
&= \Re \left\{ |z_{\text{BEL}}(nT_s)|^2 - |z_{\text{BEU}}(nT_s)|^2 + \right. \\
&\quad \left. z_{\text{BEU}}(nT_s) z_{\text{BEL}}^*(nT_s) - (z_{\text{BEU}}(nT_s) z_{\text{BEL}}^*(nT_s))^* \right\}
\end{aligned}$$

The first two terms are the magnitude squared values and hence have no quadrature component. The last two terms are the difference of two complex signals, where one is the conjugate of the other which results in only the imaginary component. Thus taking only the real part of the Eq. gives the error signal becomes,

$$e[n] = |z_{\text{BEL}}(nT_s)|^2 - |z_{\text{BEU}}(nT_s)|^2 \quad (\text{A.3})$$

So it can be seen from the above derivation that the error signal derived from the even and odd band edge filter is similarly a measure of the energy difference between the outputs of lower and upper band edge filters.

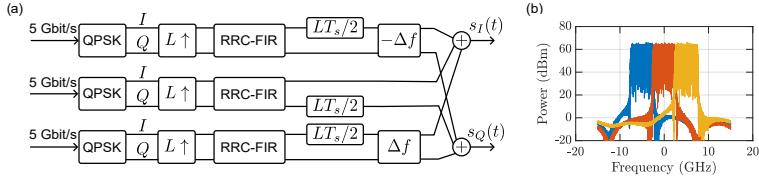
## B Offset QAM

Multi-carrier offset quadrature amplitude modulation (offset-QAM) is a promising technique that enables symbol-rate spacing with inter-symbol interference (ISI)-free transmission while maintaining relatively low implementation complexity. Historically, offset-QAM was introduced in wireless communications to mitigate spectral regrowth caused by nonlinear power amplifiers, by offsetting the transitions of the in-phase (I) and quadrature (Q) components by half a symbol period [19, 40]. In the single-channel case, this offset prevents simultaneous I/Q transitions that would otherwise introduce a  $\pi$  phase shift. When extended to multi-carrier systems, the alternating half-symbol delay across I and Q components of adjacent subcarriers relaxes the orthogonality condition and suppresses crosstalk, even under practical pulse-shaping constraints. The resulting transmit waveform can be expressed as

$$s(t) = \sum_{n=-N}^N \sum_{k=-\infty}^{\infty} \left[ a_n(k) h\left(t - kT_m - \frac{\alpha_n T_m}{2}\right) + j b_n(k) h\left(t - kT_m - \frac{(1 - \alpha_n) T_m}{2}\right) \right] \exp\left(j \frac{2\pi n t}{T_m}\right) \quad (B.1)$$

where  $h(t)$  is the pulse shape,  $a_n(k)$  and  $b_n(k)$  are the real and imaginary parts of the  $k$ -th symbol in the  $n$ -th subcarrier (SC). The coefficient  $\alpha_n$  equals 0 for even  $n$  and 1 for odd  $n$ , indicating that the imaginary part is delayed for even subcarriers, whereas the real part is delayed for odd subcarriers by half a symbol period.

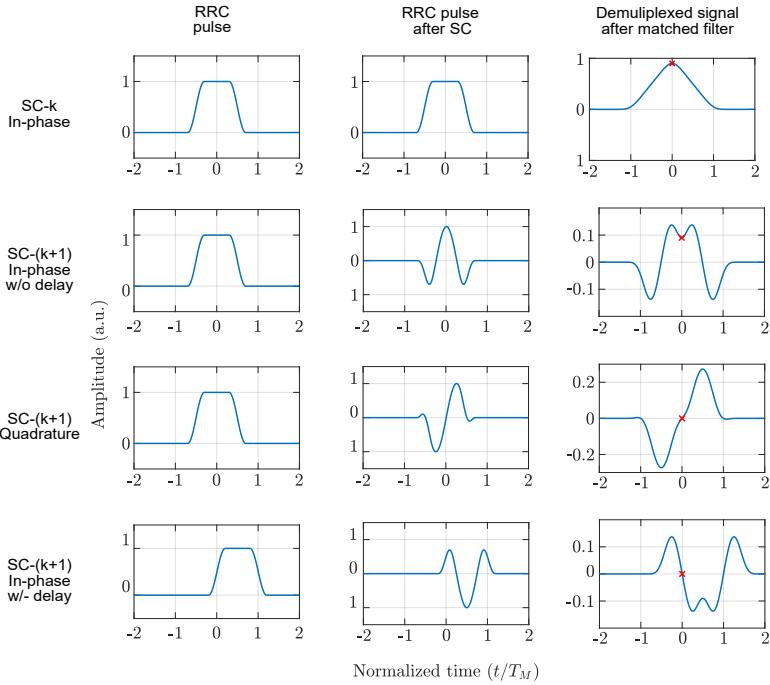
The simulation model of an offset-QPSK transmitter with three subcarriers is shown in Fig. B.1(a). Each subcarrier carries a QPSK symbol stream, which



**Fig. B.1:** Simulation setup to generate the offset-QPSK transmit signal

is upsampled and shaped using an RRC pulse. In the central subcarrier, the imaginary (Q) component is delayed by half a symbol period. In contrast, for the adjacent subcarriers, the real (I) component is delayed. These SCs are then frequency shifted to  $-\Delta f$  and  $+\Delta f$ , respectively. Finally, the real and imaginary components from all subcarriers are combined to form the composite transmit signal  $s(t)$ . Figure B.1(b) illustrates the corresponding spectrum of the transmitted signal, where the subcarriers are spaced at the symbol rate, i.e.,  $\Delta f = R_M/2$ .

Figure B.1 illustrates a simulation model to generate an offset-QPSK transmitter with three subcarriers. For all subcarriers, QPSK symbol sequence is upsampled and pulse shaped using RRC pulse shape. In the center subcarrier denoted as the 0-th the imaginary part is delayed by half-symbol period. While for the -1th and +1th subcarrier the real part is delayed. The -1th and +1th subcarrier is then frequency shifted to  $-\Delta f$  and  $\Delta f$  accordingly by multiplying with a complex exponential of that frequency. Next the real and imaginary part of the subcarriers are combined to form real and imaginary of the transmit signal  $s(t)$ . Figure XX (a), (b) shows the spectra of the individual subcarriers after the frequency shift and the final transmit signal, respectively. To illustrate the principle of inter-symbol and inter-carrier interference-free transmission in multi-carrier OQAM, Fig. XX demonstrates how applying a half-symbol delay to alternate components of adjacent subcarriers ensures orthogonality even at symbol-rate spacing. The figure is structured into three columns. The first column illustrates one symbol period of RRC shaped pulses in the time-domain. The top row corresponds to the I component of the  $k$ -th SC, followed by the I component of the  $(k+1)$ -th SC without delay, its Q component, and finally the I component of the  $(k+1)$ -th SC with a half-symbol delay.

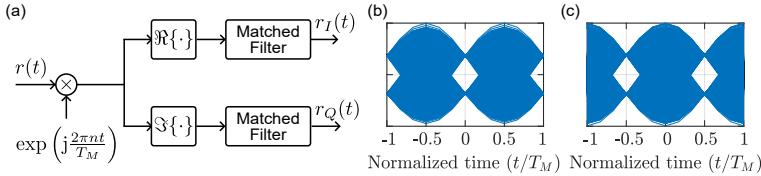


**Fig. B.2:** Illustration of crosstalk in a multi-carrier OQAM using RRC pulses (roll-off 0.4) normalized to the symbol period. The first column shows the time-domain pulses for the I component of the  $k$ -th subcarrier, the I component of the  $(k + 1)$ -th subcarrier without delay, its Q component, and the I component of the  $(k + 1)$ -th subcarrier with a half-symbol delay. The second and third columns depict the corresponding signals after subcarrier modulation and after demultiplexing of the  $k$ -th subcarrier, respectively.

The second column presents the same pulses after subcarrier modulation. The  $k$ -th subcarrier, centered at baseband, exhibits no oscillation. In contrast, the  $(k + 1)$ -th subcarrier shows a single oscillation of the cosine-modulated I component (second row), the sine-modulated Q component (third), and the half-symbol delayed cosine oscillation (fourth row), each shaped by the RRC pulse.

Finally, the third column displays the matched filter outputs for the  $k$ -th subcarrier after demultiplexing. Here, the matched filter is again an RRC pulse. At the zeroth symbol instant, the non-delayed I component of the  $(k + 1)$ -th subcarrier

(second row) produces a nonzero contribution, which would cause interference. However, when a half-symbol delay is introduced (fourth row), this contribution goes to zero, thus ensuring orthogonality. The quadrature component (third row) inherently contributes zero interference at the sampling instant due to its sine carrier modulation.



**Fig. B.3:** Receiver model for multi-carrier offset-QAM detection. (a) Schematic of subcarrier down-conversion and matched filtering. (b,c) Eye diagrams of the in-phase (I) and quadrature (Q) components, illustrating the half-symbol delay in the Q component and the corresponding optimum sampling instants.

Figure B.3 illustrates a receiver model for the detection of a subcarrier-multiplexed offset-QAM signal. The target subcarrier is first downconverted to baseband by multiplication with a complex exponential, followed by matched filtering. The corresponding eye diagrams of the received in-phase (I) and quadrature (Q) components reveal the inherent half-symbol delay of the Q component, highlighting the shift in the optimum sampling instants for accurate symbol detection.

This illustration highlights the key property of multi-carrier OQAM. The use of alternating half-symbol delays together with quadrature carriers ensures adjacent subcarriers are orthogonal, enabling efficient symbol-rate multiplexing without ISI or ICI.

# C Real-Time Hardware Platform

This chapter gives an overview of the hardware platform used for implementing the DSP algorithms. The first section describes the main features of the data converters, while the second introduces PYNQ, an open-source framework for hardware–software co-design.

The experiments in this work use the Zynq UltraScale+ RFSoC ZCU111 board from AMD Xilinx, a high-performance evaluation kit for RF applications. The System-on-Chip (SoC) integrates A/D and D/A converters, FPGA fabric, and processing systems, including a quad-core Arm Cortex-A53 and a dual-core Cortex-R5. An FMC XM500 balun transformer card provides high- and low-frequency baluns with SMA connectors for direct access to the signal converters.

## C.1 RF Data Converters

The ZCU111 board integrates eight 12-bit A/D channels (up to 4 GSa/s) and eight 14-bit D/A channels (up to 6.544 GSa/s). Interfacing is provided through the XM500 add-on card, which offers SMA connectors with high-speed, low-speed, and bandpass baluns. Four A/Ds and four D/As use high-speed baluns (differential), two A/Ds and two D/As use low-speed baluns, and the remaining channels use bandpass baluns. Since the differential A/D inputs require DC-free signals, DC blocks are added at their inputs.

The converters are configured in Vivado using the RF Data Converter IP core. In this work, both A/D and D/A channels are set to 4 GSa/s. The A/Ds, when operated at this rate, are clocked from a 500 MHz PLL that provides 8× parallel

samples. A custom VHDL design combines two cycles, yielding 16 parallel samples at a 250 MHz FPGA clock. Data exchange with the FPGA fabric uses the AXI bus protocol with 16-bit samples, where A/D and D/A data are MSB-aligned to match their resolutions.

## C.2 PYNQ Framework

PYNQ (“Python Productivity for Zynq”) is an open-source framework that makes it easier to use Zynq devices. It is based on Python and simplifies the hardware–software co-design process.

In this work, PYNQ is installed on an SD card as a Linux bootable image. During startup, the Arm processor loads this image. The board can then be programmed directly in Python through Jupyter Notebook, a browser-based interactive environment.

Hardware designs are loaded into the FPGA using overlays. An overlay consists of: a bitstream file (.bit) to configure the programmable logic (PL), and a hardware handoff file (.hwh) that describes the hardware design.

For simple control tasks, up to 64 GPIO pins can be used with the GPIO class, which allows assigning high or low levels. Example code is given in Listing A.6. To read or write data directly from PL BRAMs, the MMIO (memory-mapped I/O) class is used.

In this work, PYNQ is used to: provide GPIO inputs to hardware (e.g., PI coefficients, controller on/off, digital delay tuning, phase-lock point selection), enable/disable writing to BRAM, and read data back from BRAM for evaluation.

# D FPGA Arithmetic

## D.1 Fixed-Point Number Representation

Fixed-point representation is a method of expressing fractional numbers with a finite bit-width, where the number of bits allocated to the integer and fractional parts remains constant. In this work, all arithmetic operations implemented on the FPGA were performed using fixed-point values. The following provides an overview of the conversion process from floating-point to fixed-point representation.

Let the fixed-point integer representation of a floating-point number  $x$  be denoted by  $x_f$ . The binary representation of  $x_f$ , commonly referred to as a binary word, is divided into an integer part and a fractional part. The number of bits assigned to these two parts is denoted by  $N_I$  and  $N_F$ , respectively. For a two's complement representation, using 1-bit for sign, the total bit-width is given by

$$N = 1 + N_I + N_F$$

The representable range of numbers is then from  $-2^{N_I}$  to  $2^{N_I} - 2^{-N_F}$  with a resolution (or step size) of  $2^{-N_F}$ . The conversion from a floating-point number  $x$  to its fixed-point integer representation is performed as

$$x_f = \lfloor x \cdot 2^{N_F} \rfloor,$$

where, the symbol  $\lfloor \cdot \rfloor$  denotes the floor operation. Alternatively rounding to nearest integer may also be employed. The quantized fixed-point approximation of  $x$  is then obtained as

$$x_q = x_f / 2^{N_F} = \lfloor x \cdot 2^{N_F} \rfloor / 2^{N_F}$$

In practice, quantization introduces an error bounded by  $|x - x_q| < 2^{-N_f}$ .

Another commonly used shorthand notation for fixed-point representation is the Q-format, expressed as  $Q(N_I + 1.N_F)$ , where the first term accounts for the integer and sign bits, and the second term specifies the fractional bits.

### Design Example:

The choice of bit allocation between the integer and fractional parts depends on the specific design requirements. For example, in the implementation of the Kaiser-window low-pass filter in this work, the coefficients are first computed in floating-point form, with the maximum absolute value among the fifteen coefficients equal to 0.6252. To meet the target of a 12-bit resolution for the coefficients, one bit is assigned for the sign, with  $N_I = 0$  (no integer bits) and  $N_F = 11$  fractional bits. Consequently, the floating-point coefficients are scaled by a factor of  $2^{11}$ , and the resulting values are then quantized to integers using either rounding or the floor operation.

As another example, consider representing the floating-point value 5.6349 in 12-bit fixed-point format. Since the value lies between  $2^2$  and  $2^3$ , at least  $N_I = 3$  integer bits are required, along with one sign bit. Allocating the remaining  $N_F = 8$  for the fractional part yields a scaling factor of  $2^8$ . The fixed-point integer representation is then obtained as

$$\text{round}(5.6349 \cdot 2^8) = 1443.$$

## D.2 Division Operation in FPGA Hardware

Basic arithmetic operations such as addition, subtraction, and multiplication are typically available as pre-verified IP cores provided by FPGA vendors. In recent years, most vendors have also started supplying IP cores for division. Alternatively, algorithms such as CORDIC can be used to implement division. However, both approaches are resource-intensive and require multiple clock cycles to execute.

In practice, when the divisor has moderate precision (e.g., fewer than 14 bits), dedicated division IPs are often avoided in favor of more efficient alternatives. A common approach is to reformulate division as multiplication by a precomputed reciprocal, with the reciprocal values stored in a lookup table (LUT). In this work, division is required for the coefficients of the PI loop filter, which are typically less than one and must be tuned for stable operation. Since loop stability is sensitive to latency, the reciprocal-based approach is adopted. The reciprocal values are computed in software (PYNQ) and passed to the FPGA fabric through GPIO inputs. The following explains the process.

To illustrate, consider the division of two fixed-point integers  $x_f$  and  $y_f$  (with  $y_f$  being a positive integer represented using  $N_y$  bits). Instead of directly computing the division, first the fixed-point reciprocal of  $y_f$  is represented using  $2^{N_{\text{rep}}}$  as

$$y_{\text{rep},f} = \text{round}\left(\frac{1}{y_f} \cdot 2^{N_{\text{rep}}}\right), \quad y_f = 1, 2, \dots, 2^{N_y} - 1.$$

This reciprocal can either be precomputed and stored in a LUT, or, as in this work, calculated in software (PYNQ) and supplied to the FPGA via GPIO pins. To ensure rounding accuracy,  $N_{\text{rep}}$  must be chosen greater than  $N_y$ , often about twice its value. The division operation in the FPGA is then implemented as

$$\frac{x_f}{y_f} \approx \left[ x_f \cdot \text{round}\left(\frac{1}{y_f} \cdot 2^{N_{\text{rep}}}\right) \right] / 2^{N_{\text{rep}}}$$

The final division can be performed by the shift-right operation of  $N_{y_{rep}}$  bits. However, such an implementation inherently behaves as a floor function, which may introduce a systematic underestimation of the result. A common remedy is to add an offset of  $2^{N_{y_{rep}}-1}$ , which is equivalent to 0.5 in fixed-point arithmetic, before the final division by shift-right.

For example, with  $x_f = 100$  and  $y_f = 6$ , and parameters  $N_y = 3$  and  $N_{y_{rep}} = 6$ , the computation gives

$$\lfloor 100 \cdot \text{round} \left( 1/6 \cdot 2^6 \right) \rfloor / 2^6 = 17,$$

while the exact value is 16.667. This demonstrates the effectiveness of reciprocal-based division in FPGA designs.

# Glossary

## List of abbreviations

A/D	Analog-to-digital converter
ASE	Amplified spontaneous emission
ASIC	Application-specific integrated circuit
AWG	Arbitrary waveform generation
AWGN	Additive white Gaussian noise
BER	Bit-error ratio
BPD	Balanced photodetector
BPF	Bandpass filter
CW	Continuous wave
D/A	Digital-to-analog converter
DC	Direct current
DPSK	Differential phase-shift-keying
DSP	Digital signal processing
ECL	External-cavity laser
EDFA	Erbium-doped fiber amplifier

EO	Electro-optic
FFT	Fast Fourier Transform
FIR	Finite impulse response
FPGA	Field-programmable gate array
IM/DD	Intensity modulation and direct detection
InP	Indium-phosphide
I/Q	In-phase and quadrature
IQM	In-phase and quadrature modulator
LF	Loop filter
LO	Local oscillator
LP	Low pass
LUT	Look-up table
MIMO	Multiple-input multiple-output
MZI	Mach-Zehnder interferometer
NRZ	Non-return-to-zero
OBPF	Optical bandpass filter
ROADM	Reconfigurable optical add-drop multiplexer
OH	Optical hybrid
OOK	On-off keying
OSA	Optical spectrum analyzer
Osc.	Oscilloscope
OSNR	Optical signal-to-noise ratio

OQAM	Offset quadrature amplitude modulation
PC	Polarization controller
PD	Photodetector
PI	Proportional integral
PIC	Photonic integrated circuit
PLL	Phase-locked loop
PRBS	Pseudorandom binary sequence
QAM	Quadrature amplitude modulation
RC	Raised-cosine
RFSoC	Radio-frequency system-on-chip
RRC	Root-raised-cosine
Rx	Receiver
SMF	Single-mode fiber
TIA	Transimpedance amplifier
VOA	Variable optical attenuator
WDM	Wavelength-division multiplexing
WSS	Wavelength-selective switch

## **List of mathematical symbols**

### **Uppercase Latin symbols**

$B$	Signal bandwidth
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$B_{\text{ref}}$	Reference bandwidth for OSNR measurements (0.1 nm)
$E(t)$	Electric field
$\tilde{H}$	Amplitude response = magnitude of transfer function
$L$	Number of coefficients of an equalizer or impulse response
$N$	Number of elements, e.g., vector elements or spectral tributaries
$P(t)$	Power
$P_{\text{LO}}$	LO power
$P_s$	Signal power
$R$	Responsivity
$T_s$	Sampling period
$T_M$	Symbol duration

### Lowercase Latin symbols

$f$	Frequency
$f_{\text{clk}}$	Clock rate
$f_o$	Optical carrier frequency
$f_s$	Sampling rate
$h$	Impulse response
$i(t)$	Current, e.g., photocurrent
$n$	Index of discrete-time elements

## Greek symbols

$\lambda$	Wavelength
$\beta$	Roll-off factor
$\sigma$	Standard deviation
$\phi, \Phi, \theta$	Phase
$\Delta\phi$	Phase offset
$\omega$	Angular frequency

## Mathematical symbols

e	Euler's number, 2.71828...
$\mathcal{F}\{\cdot\}$	Fourier transform
$\mathcal{H}\{\cdot\}$	Hilbert transform
$\Im\{\cdot\}$	Imaginary part
j	Imaginary unit
$\Re\{\cdot\}$	Real part

## Mathematical functions

$\cos(\cdot)$	Cosine function
$\exp(\cdot)$	Natural exponential function
$\ln(\cdot)$	Natural logarithm
$\operatorname{sgn}(\cdot)$	Sign function

$\sin(\cdot)$  Sine function

$\text{sinc}(\cdot)$  Cardinal sine function

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# Acknowledgments

The research presented in this dissertation was conducted at the Institute of Photonics and Quantum Electronics (IPQ) at the Karlsruhe Institute of Technology (KIT). The underlying scientific work was generously funded by the German Research Foundation (Deutsche Forschungsgemeinschaft, DFG) within the projects *Interfere-1* and *Interfere-2*.

I am profoundly grateful to my doctoral supervisor, Prof. Dr. Sebastian Randel, for granting me the opportunity to pursue this research and for the trust, guidance, and support he provided throughout this journey. In addition, I would like to thank Prof. Dr. Christian Koos for his insightful comments and constructive feedback on my publications.

I thank my current and former colleagues at IPQ for fostering a supportive and stimulating research environment. This work was shaped by our rigorous scientific discussions in the lab and during seminars, as well as by the countless coffee breaks that offered much-needed moments of relief.

I am sincerely thankful to Christoph Füllner and Md. Mosaddek Hossain Adib for the continuous exchange of ideas that enriched each day. The years we worked together in the same office were marked by an inspiring and steady flow of scientific discussion. My special thanks go to Patrick Matalla, my closest collaborator, whose frequent and profound discussions on FPGA design were central to the development of this work. I am also indebted to Jonas Krimmer, whose patient and skillful guidance through complex mathematical and IT challenges proved indispensable. Finally, I thank Joel Dittmer for his important assistance in translating the preface of this dissertation into an excellent German *Zusammenfassung*, and

for his much-appreciated role as our barista, ensuring a steady supply of coffee during many productive days

I would also like to express my gratitude to the technical staff, namely Steffen Pfeifer, Lisa Nolte, Volker Bös, Thorsten Fux, and Damian Wagner, for their essential and often unseen support. My thanks also go to the office staff, including Maria-Luise Koch, Bettina Rasche, and Alina Lauinger, for their assistance with administrative procedures and for coordinating social activities.

Finally, I extend my deepest appreciation to my family. I am profoundly grateful to my parents for their unwavering support throughout my academic journey. My heartfelt gratitude goes to my wife, Rimi. Her encouragement, patience, and steady presence sustained me through the most demanding phases of this work. The arrival of our daughter Inayah shortly after the defense brought immeasurable joy and marked a beautiful beginning to the next chapter of our lives. I also wish to thank my friends in Karlsruhe, including Sakib, Hisan, Romel, Rabia, Nahid, and Marufa, whose companionship, support, and many shared moments provided balance and motivation during these years. Without the support of all of them, this dissertation would not have been possible.

# List of Publications

## Book Chapters

[B1] **M. S. Mahmud**, A. Schindler, P. Runge, M. Schell, and S. Randel, “Optic-electronic-optic interferometers for ultrabroadband arbitrary digital signal processing”, in *Electronic-Photonic Integrated Systems for Ultrafast Signal Processing*, S. Pachnicke, Ed. Springer, submitted on 30 July 2025.

## Journal Publications

[J1] **M. S. Mahmud**, P. Matalla, J. Dittmer, C. Koos, and S. Randel, “Optic-electronic-optic (oeo) interferometer enabling coherent optical add-drop multiplexing”, *Opt. Express* **33**(4), pp. 6885–6893 (Feb. 2025). DOI: [10.1364/OE.532854](https://doi.org/10.1364/OE.532854).

## Conference Publications

[C1] **M. S. Mahmud**, J. N. Kemal, M. Adib, C. Fullner, A. Schindler, P. Runge, M. Schell, W. Freude, C. Koos, and S. Randel, “Optic-electronic-optic interferometer: A first experimental demonstration”, in *Conference on Lasers and Electro-Optics*, Optica Publishing Group, (2020), SF1L.1. DOI: [10.1364/CLEO\\_SI.2020.SF1L.1](https://doi.org/10.1364/CLEO_SI.2020.SF1L.1).

- [C2] **M. S. Mahmud**, P. Matalla, M. M. H. Adib, C. Koos, and S. Randel, “Coherent add/drop multiplexing using an optic-electronic-optic interferometer”, in *CLEO 2023*, Optica Publishing Group, (2023), SM2I.6. DOI: [10.1364/CLEO\\_SI.2023.SM2I.6](https://doi.org/10.1364/CLEO_SI.2023.SM2I.6).
- [C3] P. Matalla, **M. S. Mahmud**, C. Füllner, C. Koos, W. Freude, and S. Randel, “Hardware comparison of feed-forward clock recovery algorithms for optical communications”, in *Opt. Fiber Comm. Conf. (OFC (2020))*, (2020), paper Th1A.10-1. DOI: [10.1364/OFC.2021.Th1A.10](https://doi.org/10.1364/OFC.2021.Th1A.10).
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- [C7] M. M. H. Adib, P. Marin-Palomo, J. N. Kemal, C. Füllner, **M. S. Mahmud**, A. Ramdane, C. Koos, W. Freude, and S. Randel, “Coherent TWDM-PON downstream architecture based on a chip-scale QD-MLLD”, in *Advanced Photonics Congress (Networks) (APC (2020))*, (2020), paper NeTu2B.5. DOI: [10.1364/NETWORKS.2020.NeTu2B.5](https://doi.org/10.1364/NETWORKS.2020.NeTu2B.5).
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## Preprint Publications

[P1] P. Matalla, J. Dittmer, **M. S. Mahmud**, C. Koos, and S. Randel, “Elastic buffer design for real-time all-digital clock recovery enabling free-running receiver clock with negative and positive clock frequency offsets” (2025). arXiv: [2507.13748](https://arxiv.org/abs/2507.13748) [eess.SP]. [Online]. Available: <https://arxiv.org/abs/2507.13748>.