



Full Length Article

AstroPix: A pixelated HVCMOS sensor for space-based gamma-ray measurement

Amanda L. Steinhebel ^{a,b}, Daniel P. Violette ^{a,b}, Regina Caputo ^b, Anthony Affolder ^c, Autumn Bauman ^{d,e}, Carolyn Chinatti ^{f,g}, Aware Deshmukh ^c, Vitaliy Fadayev ^c, Yasushi Fukazawa ^h, Manoj Jadhav ⁱ, Carolyn Kierans ^b, Bobae Kim ⁱ, Jihee Kim ⁱ, Henry Klest ⁱ, Olivia Kroger ^c, Kavic Kumar ^{j,b}, Shin Kushima ^k, Jean-Marie Lauenstein ^b, Adrien Laviron ^{a,b}, Richard Leys ^l, Forest Martinez-Mckinney ^c, Jessica Metcalfe ⁱ, Zachary Metzler ^{j,b}, John W. Mitchell ^b, Norito Nakano ^h, Jennifer Ott ^c, Ivan Peric ^l, Jeremy S. Perkins ^b, Max R. Rudin ^{m,g}, Taylor (K.W.) Shin ^c, Grant Sommer ^{n,b}, Nicolas Striebig ^l, Yusuke Suda ^h, Hiroyasu Tajima ^{k,o}, Janeth Valverde ^{p,b}, Maria Zurek ⁱ

^a NASA Postdoctoral Program Fellow, USA

^b NASA Goddard Space Flight Center, 8800 Greenbelt Rd, Greenbelt, MD 20771, USA

^c Santa Cruz Institute for Particle Physics (SCIPP), University of California Santa Cruz, 1156 High Street, Santa Cruz, CA 95064, USA

^d University of Colorado Denver, 1201 Larimer St., Denver, CO 80204, USA

^e NASA Office of STEM Engagement, 300 E. St. SW, Washington, DC 20546, USA

^f Carleton College, North College St., Northfield, MN 55057, USA

^g Center for Research and Exploration in Space Science and Technology, College Park, MD 20742, USA

^h Physics Program, Graduate School of Advanced Science and Engineering, Hiroshima University, 1-3-1

Kagamiyama, Higashihiroshima, 739-8526, Hiroshima, Japan

ⁱ Argonne National Laboratory, 9700 S. Cass Avenue, Lemont, IL 60439, USA

^j University of Maryland, College Park, MD 20742, USA

^k Institute for Space-Earth Environmental Research, Nagoya University, Furo-cho, Chikusa-ku, Nagoya, 464-8602, Aichi, Japan

^l ASIC and Detector Laboratory, Karlsruhe Institute of Technology, Hermann-von-Helmholtz-Platz 1, Karlsruhe, D-76344, Baden-Wuerttemberg, Germany

^m Rice University, 6100 Main St., Houston, TX, 77005, USA

ⁿ The George Washington University, 2121 I St. NW, Washington, DC 20052, USA

^o Kobayashi-Maskawa Institute for the Origin of Particles and the Universe, Nagoya University, Furo-cho, Chikusa-ku, Nagoya, 464-8601, Aichi, Japan

^p Department of Physics and Center for Space Sciences and Technology, University of Maryland Baltimore County, 1000 Hilltop Cir., Baltimore, MD 21250, USA

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ABSTRACT

A next-generation medium-energy gamma-ray telescope targeting the MeV range would address open questions in astrophysics regarding how extreme conditions accelerate cosmic-ray particles, produce relativistic jet outflows, and more. One concept, AMEGO-X, relies upon the mission-enabling CMOS Monolithic Active Pixel Sensor silicon chip AstroPix. AstroPix is designed for space-based use, featuring low noise, low power consumption, and high scalability. Desired performance of the device include an energy resolution of 5 keV (or 10% FWHM) at 122 keV and a dynamic range per-pixel of 25–700 keV, enabled by the addition of a high-voltage bias to each pixel which supports a depletion depth of 500 μm . This work reports on the status of the AstroPix development process with emphasis on the current version under test, version three (v3), and highlights of version two (v2). Version 3 achieves energy resolution of $10.4 \pm 3.2\%$ at 59.5 keV and $94 \pm 6 \mu\text{m}$ depletion in a low-resistivity test silicon substrate.

1. Introduction

Over the past several decades, silicon strip detectors (SSDs) have been a key detector technology used in gamma-ray and cosmic-ray

telescopes such as the *Fermi* Large Area Telescope (LAT) [1], the Alpha Magnetic Spectrometer (AMS) [2], and Dark Matter Particle Explorer (DAMPE) [3]. Breakthroughs in particle physics instrumentation have

* Correspondence to: Oak Ridge National Laboratory, TN, USA.

E-mail addresses: steinhebel@ornl.gov (A.L. Steinhebel), daniel.p.violette@nasa.gov (D.P. Violette), regina.caputo@nasa.gov (R. Caputo).

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Table 1

Measurements for ATLASPix and AstroPix versions 1, 2, and 3. The energy resolution was measured using cadmium-109, cobalt-57, americium-241, and barium-133. AstroPix was not thinned to the thickness of the chips is the thickness of the wafer. The depletion (Dep.) was not measured (N.M.) for versions 1 and 2.

*Analog data only \diamond Median of full array response \blacksquare Theoretical value from pn junction model \triangle Do not expect full depletion with test chips. See Section 5.2.

	ATLASPix [5,6]	v1 [7]	v2 [7,8]	v3 [9–11]	Goal [12]
E_{res} [keV] (FWHM) at 30.1	$7.3 \pm 1.2\%$ at 30.1	$20 \pm 7.4\%^*$ at 30.1	$15 \pm 3\%$ at 30.1	$10.4 \pm 3.2\%^\diamond$ at 59.5	10% at 122
Pitch [μm]	150×50	175×175	250×250	500×500	500×500
Thick [μm]	100	725	725	725	525
Dep. [μm]	48 \blacksquare	N.M.	N.M.	$94 \pm 6^\triangle$	500
Range [keV]	5-32	14-122	14-80	22-200	25-700
Analog [mW/cm ²]	120	14.7	3.4	1.06	1.0
Digital [mW/cm ²]	40	9.9	3.75	3.06	0.5

enabled the development of High Voltage-CMOS (HVC MOS) Monolithic Active Pixel Sensors (MAPS) [4], which have the potential to offer significant advantages over other silicon-based detectors (such as SSDs).

MAPS have signal amplification and readout circuits embedded in the sensor, without the need for a separate Application Specific Integrated Circuit (ASIC), providing a more compact and scalable design. MAPS are traditionally low power devices, and they have by design a reduced overall mass with limited passive material in the active area of the detector. The two-dimensional hit location information provided by these pixelated detectors is an imperative feature for soft gamma-ray detection (<10 MeV). These detector capabilities make them a particularly compelling technology for future gamma-ray telescopes (see Refs. [5,12] for more details).

AstroPix is a HVC MOS MAPS being developed for space-based mission concepts such as the All-sky Medium Energy Gamma-ray Observatory eXplorer (AMEGO-X) [12]. Inspiration is drawn from the ATLASPix chip, which was designed to detect charged particles in the inner detector of the ATLAS Experiment [6,13]. The AstroPix project has subsequently coordinated incremental development away from the ATLASPix designs toward a final version which will be optimized for a space environment (see Table 1). The device under test and subject of this work is the third iteration, or AstroPix_v3. The performance of AstroPix_v1 and AstroPix_v2 has been documented in Refs. [7–9,14].

In addition to reviewing AstroPix_v3 operation and functionality, this work will overview noise and energy resolution performance. Current-voltage and capacitance-voltage curves are presented with discussion of sensor noise and depletion. AstroPix_v3 will be the first flight-tested AstroPix chip as the main component of a sounding rocket payload, the Astropix Sounding rocket Technology dEmonstration Payload (A-STEP) (see Section 7). As such, operation and characterization results relevant for this upcoming flight will be emphasized.

AstroPix has been tested in multiple beam environments, including with a 120 GeV proton beam at the Fermilab Test Beam Facility. A detailed report of this testing and results including the measurement and identification of minimum ionizing particles, alternate energy calibration method, and alternate measurement of depletion depth will be reported in an upcoming independent publication.

The paper is outlined as follows: Section 2 describes the AstroPix_v3 chips; Section 3 illustrates the benchtop test setup; Section 4 describes measurements and impact of noise and dark count rate; Section 5 details the AstroPix_v3 characterization, including calibration, energy resolution, and depletion depth; Section 6 summarizes radiation testing of AstroPix_v2 in a heavy ion beam; and finally Section 7 summarizes the work and outlines future outlook and applications of AstroPix.

2. AstroPix_v3

HVC MOS MAPS detectors were developed by I. Peric more than a decade ago [4] as a novel technology primarily for particle physics applications. His group at the Karlsruhe Institute of Technology (KIT) ASIC and Detector Laboratory (ADL), with many more collaborators, has continued this work, advancing the technology forward [15–17]. ADL's experience with chips such as MuPix and ATLASpix inform the development of AstroPix. The design evolution over the course of several iterations has culminated in the first full-scale flight prototype chip: AstroPix_v3. An illustration of key properties of each AstroPix version is shown in Table 1. For the first time, AstroPix_v3 uses the full $2 \times 2 \text{ cm}^2$ reticle and features a 35×35 pixel matrix with a pixel pitch of $500 \times 500 \mu\text{m}^2$. A $300 \times 300 \mu\text{m}^2$ high voltage deep n -well (DNW) protects the embedded CMOS circuits and creates a bias junction with the p -type bulk silicon, leading to a depletion region with high voltage (HV) application (see Fig. 1). HV is applied as a negative voltage to the p^+ ring near the chip edge. In-pixel collection diodes are biased to 1.8 V. Fabrication uses a standard high voltage CMOS process with a deep n -well and unthinned bulk silicon wafers with a thickness of 720 μm .

All iterations of AstroPix were fabricated using TSI Semiconductors' 180 nm process¹ and AstroPix_v3 was delivered in October 2022. The final design must deplete 500 μm and thus a global HV bias is applied to the chip top side (Fig. 1). A backside bias is not utilized in order to simplify chip processing and eventual integration into large format structures. Full depletion will be achieved with a high-resistivity ($> 5 \text{ k}\Omega \cdot \text{cm}$) silicon wafer thinned to 525 μm . Neighboring pixels are isolated by a p -stop isolation ring (blue in Fig. 1), separated by a distance of 100 μm . The metal DNW guard ring (dark green in Fig. 1) is connected to each pixel DNW and overhangs the DNW and silicon bulk by 4 μm on each side. It acts as a field plate to reduce the electrical field strength at the implant edges, thus improving breakdown voltage. The large separation between the DNW guard ring and the isolation p -stop allows for operation at high voltages with breakdown occurring at $\sim 400 \text{ V}$. The bulk substrate between implants sustains the high voltage, creating a smooth depletion layer through the bulk without introducing inter-pixel dead space. The 600 μm distance between edge pixels and the chip edge, as well as the final p -well block, is to ensure that the depletion region does not touch the chip edge.

Chips were fabricated on three different wafers with low, medium, and high resistivity (see Table 2). The medium-resistivity Wafer 2 is the

¹ TSI Semiconductors has subsequently been acquired by Bosch Semiconductor LLC and the foundry business has ceased. Subsequent iterations of AstroPix will be fabricated at a different foundry such as AMS in Austria or LFoundry in Italy.

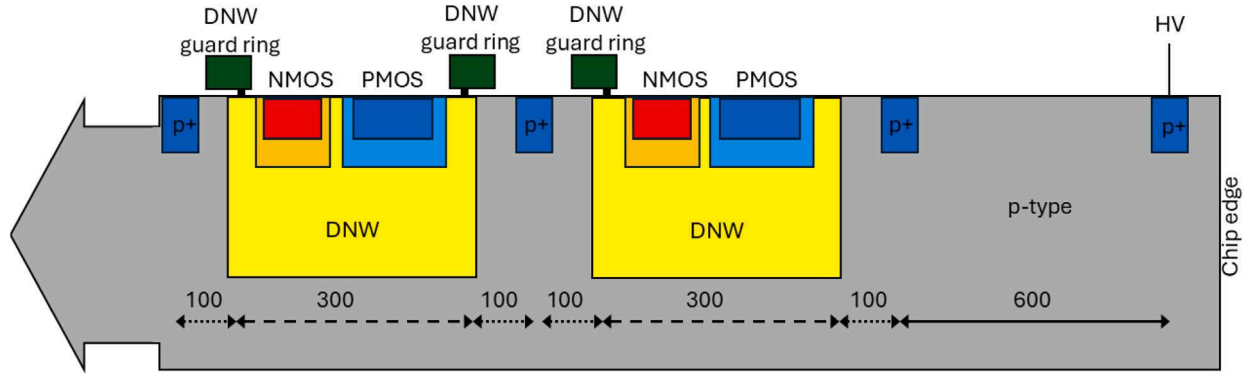


Fig. 1. Cartoon of AstroPix_v3 structure, including DNWs (yellow), CMOS components (structures within DNWs), inter-pixel isolation p -stop (blue), and DNW guard rings (dark green). HV is delivered on the frontside of the chip. Drawing not to scale. Units displayed in μm .

Table 2

Properties of silicon wafers. The medium-resistivity Okmetic wafer, hereafter referred to by its number 2, is the focus of this work.

Wafer	1	2	3
Resistivity [$\Omega \cdot \text{cm}$]	20	200–400	20 900–28 900
Manufacturer	TSI	Okmetic	Topsil
Notes	Fabricator test wafer with poorly quantified resistivity	Focus of this work, used to populate Table 1, full depletion not expected	Tested in this work to explore the goal depletion depth

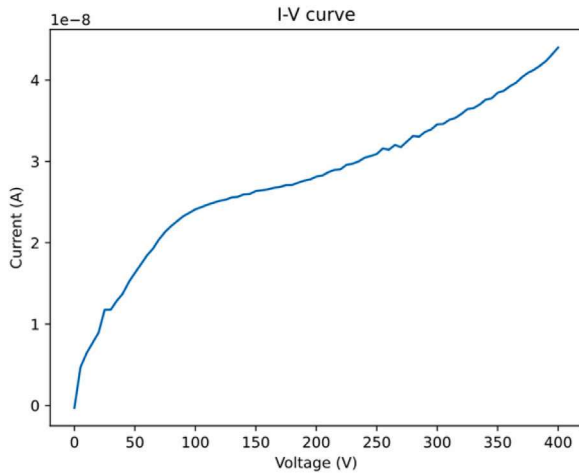


Fig. 2. IV curve for AstroPix_v3 wafer 2 chip (200–400 $\Omega \cdot \text{cm}$).

emphasis of this work. Further details of AstroPix characterization can be found in Refs. [9–11].

A current–voltage (IV) curve of the biasing HV used to deplete the substrate for a representative wafer 2 chip is shown in Fig. 2. The DNW guard rings are electrically coupled to the DNW for this measurement. Breakdown occurs between -380 V and -400 V in wafer 2 and around -200 V in wafer 1. Applications of AstroPix require low power draw and a bias leakage current less than $1 \mu\text{A}$, allowing operation of a wafer 2 chip up to -400 V. A larger bias enables more complete depletion (more details in Section 5.2), so the energy calibration reported in Section 5.1 uses a bias of -350 V which incorporates a safety margin with respect to the breakdown voltage. Otherwise, a stable bias of -150 V can be assumed for the remainder of the studies in this paper unless explicitly stated.

A simplified schematic for pixel operation and timestamp generation is shown in Fig. 3. Each pixel contains a charge-sensitive amplifier (CSA), bandpass filter, and comparator. For testing and comparison purposes, the first three columns feature a PMOS amplifier whereas the

rest implement the standard NMOS amplifiers. These PMOS columns were found to impair data quality with higher noise rates than NMOS columns, and are not considered in this work’s analysis or for future design iterations.

Each pixel contains a band pass filter to mitigate thermal and flicker noise (see Section 4). The in-pixel comparator (‘comp’ in Fig. 3) enables self-triggering, so no external trigger signal is required for readout and the device only returns data when an event occurs. This reduces the data footprint as pixels with no measured charge do not return zero or empty counts. A Time Over Threshold (ToT) measurement provides a measurement of the deposited charge by recording the duration of the signal amplitude while it remains above a user-defined threshold. The timing of this signal is set by an external global timestamp (TS). In AstroPix_v3, a global comparator threshold value is set for the full array. AstroPix_v4 and subsequent versions include Tune DACs to enable individual pixel threshold setting [18].

The full signal path is shown in Fig. 4. When a pixel comparator passes a signal that exceeds the threshold, the chip processes this information and lowers an ‘interrupt’ signal. To keep the number of readout channels low, and therefore reduce power consumption, the pixel comparator outputs per row and column are OR wired (Fig. 4). A low ‘interrupt’ signal indicates that data is ready for collection to a Field Programmable Gate Array (FPGA) which receives and stores data then transmitted to a software-based data acquisition (DAQ) system (see Section 3). The comparator threshold is set to achieve maximal detector efficiency by setting the lowest possible detector threshold while still minimizing triggering from noise fluctuations.

The matrix digitization is done via 12 bit counters driven by a 200 MHz ToT clock, implemented both per row and per column (Fig. 4). Resulting ToT values fall within the μs range, therefore the ns-scale resolution from this clock is much smaller than the ToT noise. An 8 bit time of arrival (ToA) timestamp is driven by a 2 MHz clock.

Once collected at the pixel level, the digital signal is stored in a hit buffer and ultimately read out over SPI (Fig. 4). Each digitized signal returns a 5-byte data packet - a 4 bit header for data integrity, 11 bit pixel address, 12 bit ToT, and 8 bit ToA.

In addition to digitized output, an “analog” output can also be accessed. This is sent from the in-pixel amplifier prior to the standard digitization readout path (including the in-pixel comparator) and can

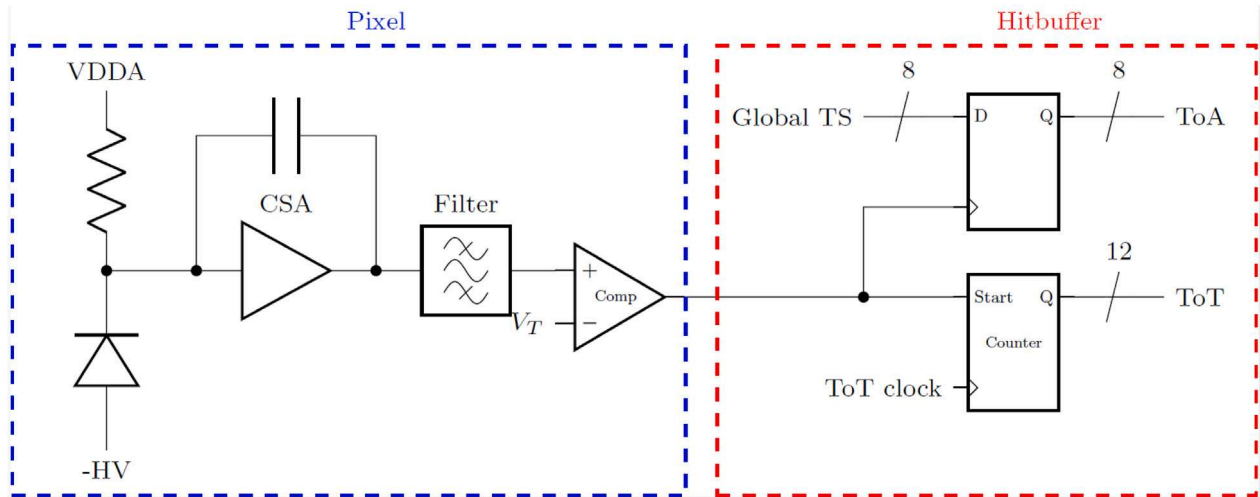


Fig. 3. Simplified operational schematic illustrating electronics within each pixel and timestamp generation within pixel buffers.

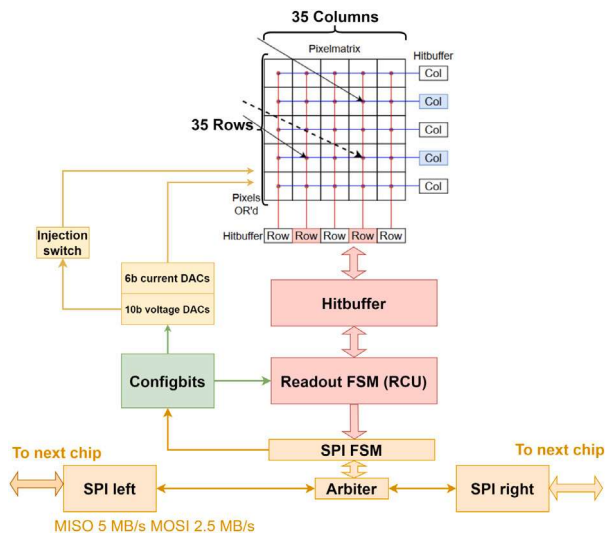


Fig. 4. AstroPix_v3 signal chain with all basic blocks showing the full readout path. Hitbuffer signals interface with a readout control unit (RCU) which includes a finite state machine (FSM).

be read from a single pixel at a time from the bottom row of pixels (row0). The analog output signal provides an important cross-check on the energy resolution of the detector and front-end amplifier because it is not limited by the digital resolution of the readout.

Power consumption has decreased with each chip version (see Table 1). Strategies such as limiting clock distribution to the matrix periphery, optimizing the bias circuits, and increasing pixel size account for some power saving. Analog power consumption has been the emphasis of past design iterations, where 97% analog power reduction was achieved from AstroPix_v1 to the current 1.06 mW/cm² draw of AstroPix_v3. Future versions of AstroPix [18] will continue this trend of reduced power consumption with a renewed focus on the digital power draw. A brief discussion of the planned path forward is included in Section 7.

Fig. 5 (left) shows a single AstroPix_v3 chip mounted to a carrier board. Chips are diced from the wafer as single arrays and in a 2 × 2-array configuration called a quad chip, shown in Fig. 5 (right) with a total area of 3.81 × 3.93 cm². This quad chip, utilizing four independent AstroPix arrays, will be the building block of larger AstroPix-based structures including A-STEP [19]. 18% of fabricated chips (180 chips)



Fig. 5. (left) One 2 × 2 cm² AstroPix_v3 chip mounted on a custom carrier board (right) One ~4 × 4 cm² AstroPix_v3 quad chip, comprised of an array of four individual chips. The top two chips are connected via a flex cable glued on top of the chips.

underwent Quality Control testing following fabrication, dicing from the wafer, mounting to a carrier board, and wirebonding. Individual chips were tested with an IV measurement, visual inspection for physical damage, and metrology for dimension and mass. Passing chips displayed no physical damage inside guard rings and a sufficiently high breakdown voltage around −375 V. 97.1% of wafer 2 chips passed the Quality Control testing, with the few failures due mostly to low breakdown voltage. No ASIC readout testing was conducted at this stage, however this is planned in the future as active work is underway to commission the necessary infrastructure and develop a test procedure. This chip yield exemplifies the scalability that AstroPix is designed for, where the formation of large format structures with straightforward integration, operation, and readout is achievable. Power is delivered to each chip in a quad-chip via custom-designed bus bars to supply the chips in parallel. Data are sent between arrays via wirebonds that enable a daisy chain and is delivered off-chip with a quasi-Serial Peripheral Interface (SPI). Quad chips of AstroPix_v3 are also under test with a suite of software and firmware developed for the readout of large arrays and multiple layers.² Larger instrument designs can daisy chain up to 32 chips to one SPI bus, limited by available chip identification bits. The chip-to-chip transfer latency is expected to be 800 ns total with 200 ns/byte and assuming 4 idle bytes per hop. The 2 MHz timestamp clock turns over after 128 μs, so the latency does not impact timing resolution.

² <https://github.com/AstroPix/astep-fw>

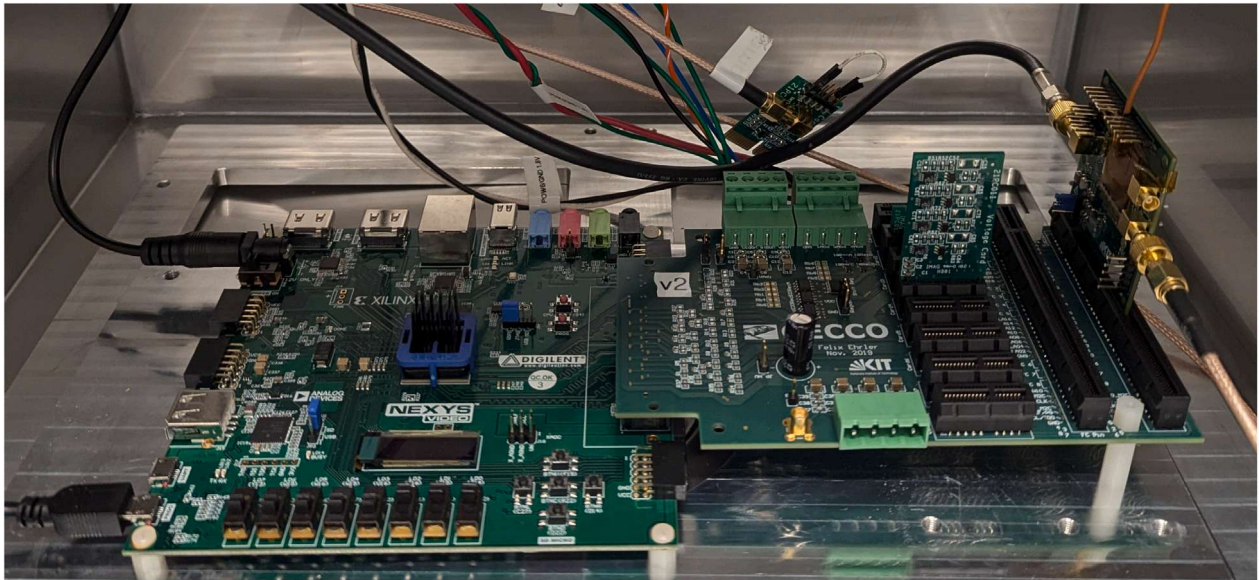


Fig. 6. Experimental setup of AstroPix_v3 and supporting electronics. The chip is mounted on the rightmost board, facing the left.

3. Experimental setup and sensor operation

The equipment used to test AstroPix, as shown in Fig. 6, includes a custom built GEneric Configuration and CONTROL (GECCO [20]) Data Acquisition System, a NexysVideo (Xilinx Artix-7) FPGA, and a carrier board for the integration of the chips into the GECCO system, along with an oscilloscope and power supplies. Data is read off the sensor by a software-based DAQ system.

In-pixel circuitry operation can be fine-tuned through user-definable values configured through in-chip Digital-to-Analog Converters (DACs). Currents, such as that fed to the source follower which sets the amplifier operating point, and voltages, such as comparator voltage baseline, impact signal shaping and power consumption. Initial values are set from simulation and were further optimized for performance while on the bench. Shaping the pulse width via the in-pixel band pass filter was a focus of optimization studies, to not limit the operational range given by the maximum measurable value of $\sim 20.5 \mu\text{s}$ by the 12 bit 200 MHz ToT counter. Following optimization, all testing utilizes the same set of DAC values. This can be assumed for all the results explored in this work.

The chip can operate in “high gain” or “high dynamic range” mode, which impacts the in-pixel CSA gain. The studies in this work all operate in “high dynamic range” mode which causes bilinear output from the CSA. Therefore, a linear response through the full operational range is not expected.

Custom firmware³ and software⁴ allow for interfacing with the chip, properly setting clocks and configuring chip operational settings, and executing data collection and storage.

All studies in this work exclusively consider this digital data. The row- and column-wise OR wiring results in the data from a pixel being separated in two hits containing the row and column information. Events are considered for data analysis only if a pair of row and column hits record a timestamp within 1 clock count (200 ns) and ToT values within $0.15 \mu\text{s}$. In this way, the response of individual pixels can be considered.

The work presented in this paper is a collection of results from a dedicated international collaboration with worldwide testing campaigns. As such, minor differences in experimental setup may be present

Table 3

Standard run settings for the studies reported in this work.

Wafer identifier	Wafer brand	Resistivity [$\Omega \cdot \text{cm}$]	Comparator Thresh. [mV]	Bias [-V]	Max. dark count rate [Hz]
2	Okmetic	200–400	200	150	2

for different tests presented here. Unless explicitly stated in a section, the settings in Table 3 can be assumed for all studies in this work.

Additional settings include operation in ‘high dynamic range’ gain mode, optimized voltage and current DAC settings, and disabling of the first three pixel columns with PMOS amplifiers.

4. Noise studies

‘Noise’ hits occur when particles from background sources interact with the detector, such as cosmic ray interactions or naturally occurring background radiation. Electronic fluctuations can trigger a comparator readout even without a particle interaction, and detector noise from leakage current can contribute to underlying noise levels. The goal of these studies is to quantify the impact of noise through electronics and detector noise sources by determining the percentage of pixels which are sensitive within the operational range, understand the noise rate at different thresholds, and setting an optimized threshold voltage such that the impact of noise is minimized.

The analog baseline, as read off the amplifier from selected pixels, shows random fluctuations up to 50 mV over a nearly constant baseline. This constant noise floor is due to detector electronics and consists of shot noise from the sensor diode and thermal and flicker noise from the electronics. Shot noise is not dominant as AstroPix application is in low-radiation environments, though the chip’s digital periphery is robust against catastrophic radiation damage (see Section 6.2). Thermal and flicker noise are controlled due to the use of in-pixel low- and high-pass filtering respectively (Fig. 3). This filtering helps mitigate their dependence on pixel capacitance, as the pixel capacitance is roughly 1 pF. Pixel capacitance is dominated by the capacitance of metal traces over each pixel and not by the diode capacitance. The trace routing will be optimized in further versions of AstroPix and is expected to decrease to 500 fF per pixel. The HVCMOS nature of the AstroPix design necessarily carries higher capacitance values than standard CMOS pixels, however the optimized future design is aligned with other HVCMOS chips.

³ <https://github.com/AstroPix/astropix-fw>

⁴ <https://github.com/AstroPix/astropix-python>

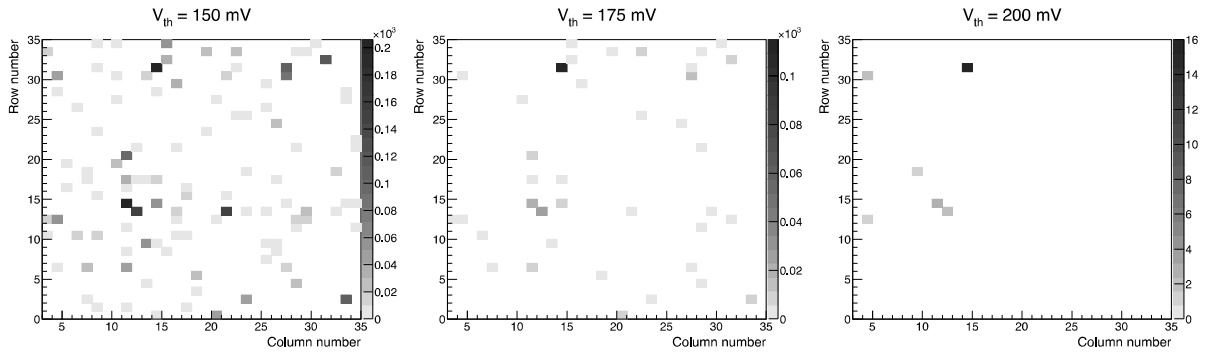


Fig. 7. Dark count hit map for a wafer 2 chip at different comparator thresholds with no disabled pixels. The z-axis shows the number of hits per pixel over 5 s integration time.

Large fluctuations with a low rate are likely noise from the environment in which the sensor is operated. The dark count rate can be mitigated during data collection by setting the comparator threshold higher than 50 mV above baseline. A 22.1 keV photopeak from cadmium-109 is visible in measurements made in Section 5 with a 200 mV threshold, so the 50 mV fluctuations can be disregarded and do not impact the operational range. The impact of increasing threshold on noise is shown in Fig. 7.

Threshold values of 200 mV allow the detection of 25 keV signals as required in Table 1 (see Section 5 for details). As shown in Section 5, a 22 keV photopeak from cadmium-109 is visible with a 200 mV threshold, so that the electronics fluctuations do not impact the operational range. With nominal operational settings (see Table 3), < 0.5% of pixels per array are too noisy for data collection and must be masked (their comparators disabled).

The variation in dark count rate also illustrates a degree of variation between pixels within the same array. Process variations and device mismatch lead to this natural variation in amplifier gain which cause some pixels to be sensitive to noise which remains below threshold in other pixels. This leads to pixel responses varying 20 – 35% relative to one another.⁵ Individual-pixel calibration therefore is required to correct for this variation. Section 5 outlines this calibration strategy and its results.

The in-pixel comparator does not collect sub-threshold hits. AstroPix_v3 is designed to reduce charge sharing, or signal splitting between neighboring pixels due to ionizing particle positioning. Improperly accounting for charge sharing could reduce the measured energy resolution of the device, as there is unmeasured (sub-threshold) charge in the shared pixels. Studies in Ref. [5] show that any potential charge sharing between pixels does not induce above-threshold hits in neighboring pixels. However, the threshold is set to maximize the operational range and has been shown (in Section 5) to enable measurement below the 25 keV requirement. In this way, some degree of charge splitting can be accounted for provided that there is enough to trigger a neighboring comparator operating at this low global threshold. Simulation studies are planned to investigate the potential impact of charge sharing and its effect on energy resolution.

The studies of this section illustrate that noise can be reduced to tolerable rates with AstroPix devices. This can be done by carefully setting a global threshold which minimizes noise while still providing measurements within the required operational range of 25–700 keV and identifying and masking noisy pixels with large noise rates. These noisy pixels have no geometric dependence within the array and have

not shown induced charge sharing. With the optimal operation described here and standard run settings from Table 3, a single array measures a total noise rate below 2 Hz. This measured rate is acceptable for future AstroPix applications including A-STEP and large-format future-observatories such as AMEGO-X.

5. Energy resolution

A high bias voltage enables more complete depletion and in general more efficient charge collection. Here we consider an energy calibration conducted at –350 V bias, as described in Ref. [10]. The current drawn off the bias line is ~ -38 nA (Fig. 2).

5.1. Energy calibration and resolution

The energy calibration procedure is described in detail in Ref. [10], and is applied to one wafer 2 chip. After masking 8 noisy pixels, measurements of radioactive sources including Cd-109, Ba-133, Am-241, and Co-57 were made. Calibration curves for each pixel relate the expected photopeak energy and the mean measured ToT with a function of the form

$$y = a * E + b * [1 - \exp(-E/c)] + d,$$

where E is the true photopeak energy and y is the uncalibrated ToT value. The functional form involves a low-energy linear component and higher-energy exponential decay. This form is motivated by the in-pixel charge-sensitive amplifier which utilizes two feedback capacitances which manifest as different gain regimes, creating a bilinear gain structure.

Fig. 8 shows the application of these calibration curves to spectra for all calibrated pixels after individual pixel calibration. The 22 keV photopeak of Cd-109 is clearly visible, indicating that the necessary 25 keV threshold is achieved.

Calibration precision is reflected in Fig. 9 where the full width half max (FWHM) of a given photopeak is shown for each calibrated pixel. This is illustrated as a function of photopeak energy in Fig. 10.

The median FWHM value for each photopeak is used to calculate energy resolution, defined as the ratio of the FWHM to the expected photopeak energy. This energy resolution dependence on energy can be found in Ref. [10].

When considering one 35×35 array, 92.4% of pixels achieve the low-energy floor requirement of 25 keV sensitivity. 44% of pixels meet the energy resolution requirement of 5.9 keV at 59.5 keV with a median full-width half-max (FWHM) of 6.2 keV (10.4%). The lack of a confident Compton edge feature identification at ~ 220 keV makes the measured operational range 14–200 keV.

The high-end of the operational range is hindered due to incomplete depletion (see Section 5.2) and amplifier saturation. Simulations of the amplifier in “high dynamic range” mode showed that its output amplitude saturates at ~ 250 keV. This is consistent with Fig. 8 where the

⁵ The variation is calculated by identifying a photopeak from a spectrum and fitting a Gaussian function to the histogram of all pixel responses to that photopeak. The reported pixel variation is the 68% confidence interval associated with the fit. See Fig. 9.

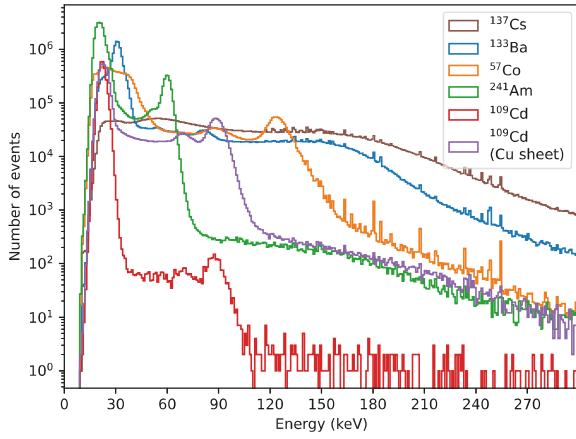


Fig. 8. Stacked calibrated spectra from all 996 calibrated pixels. ‘Cd-109 (Cu sheet)’ is a measurement with the same Cd-109 source as used in the designated line but with a Copper sheet placed between the source and the sensor to limit low-energy interactions.

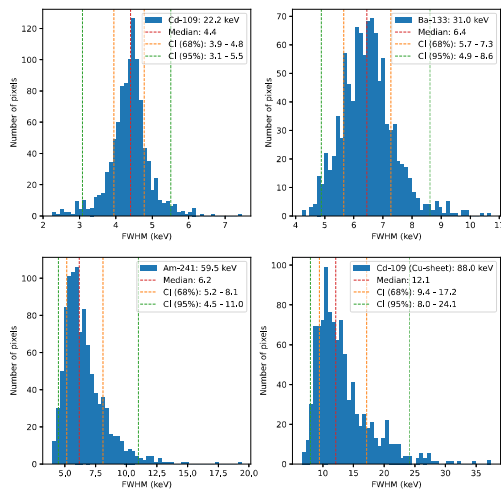


Fig. 9. Full Width Half Max (FWHM) distributions of individual pixel calibrated responses to a photopeak.

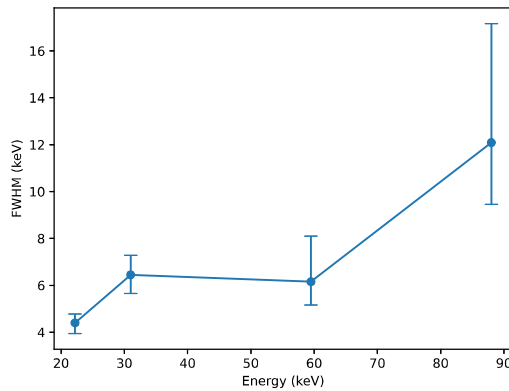


Fig. 10. Full Width Half Max (FWHM) measurements as a function of photopeak energy.

Cs-137 spectrum is terminated around 260 keV. A subsequent iteration of AstroPix implements test pixels with a dynamic feedback capacitance realized with an NFET device [21] to enable higher measurements before saturation. Additionally, more ToT bits are allotted to prevent an

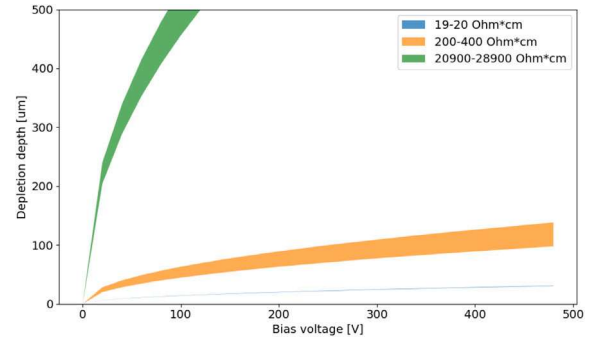


Fig. 11. Theoretical achievable depletion of AstroPix_v3 substrates [22].

operational range loss due to overflow in the digitization step in future versions.

5.2. Depletion depth measurements

The highest-resistivity AstroPix_v3 design ($25 \pm 8 \text{ k}\Omega \cdot \text{cm}$ in wafer 3) was targeted for exploring the goal depletion depth of $500 \mu\text{m}$ within a -100 V bias range. The two other resistivities are included for comparison with previous generations and consideration for further studies. The different depletion depths expected for each wafer resistivity are shown in Fig. 11.

However, this high-resistivity substrate could not be thoroughly tested due to a high leakage current. An inherent voltage gradient coupling through conductive mounting to the test board contributes to a low breakdown voltage of $< -1 \text{ V}$, but isolating the backside does not resolve the high current. The cause of this current is an active area of investigation.

Detector capacitance plays an important role in the readout system performance. By design, it is connected to the input of the charge-sensitive amplifier. The amplifier noise is a monotonically increasing function of the capacitance. Therefore, reducing the capacitance through higher bias reduces noise, in addition to increasing the ionization efficiency by augmenting the depletion region.

A capacitance-voltage (CV) curve of the $200\text{--}400 \Omega \cdot \text{cm}$ wafer 2 substrate is shown in Fig. 12. Notably, the function shape at low voltages is different from the linear dependence of $1/C^2$ on bias voltage. We attribute this to the depletion area development. At near-zero bias the depleted regions starts to grow from the implants, therefore the depleted area is smaller than the full chip size. For this reason, we expect $1/C^2$ first to grow sub-linearly with the bias voltage until the depleted region between neighboring pixels reconnect. Indeed, the shape of the CV curve indicates a reduction of the slope below -25 V with quasi-linear dependence above this voltage. The other feature is a sharp capacitance change around -150 V . It is dependent on the test frequency, indicating a possible relation to surface charge. Both features are under further investigation, however the functional shape of the CV curve suggests under-depletion and isolated depleted regions under each implant in the voltage range tested.

Estimations of the depletion depth that wafer 2 chips can achieve was tested in Ref. [10] by measuring the count rates of X-ray sources. This indirect measurement results in $60 \pm 3 \mu\text{m}$ depletion at -150 V bias and $94 \pm 6 \mu\text{m}$ depletion at -350 V bias, which agrees with the PN junction model curve with the uncertainty in the resistivity. Fitting a PN junction model to the data reproduces a resistivity of $236.8 \pm 2.4 \Omega \cdot \text{cm}$.

A direct measurement of depletion depth from the same wafer using the Edge Transition Current Technique [23] was conducted at the Santa Cruz Institute for Particle Physics in November 2023. Current results from this study are detailed in Ref. [22] and Ref. [11]. These preliminary studies estimate depletion depths of $\sim 275 \mu\text{m}$ at -150 V which over-estimates the theoretically expected value from Fig. 11.

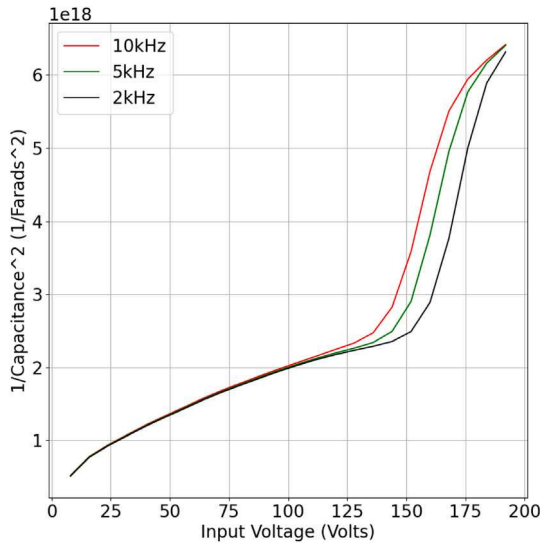


Fig. 12. CV curve for a wafer 2 chip tested at different frequencies. The device is reverse biased. [11].

Unaccounted for sources of error including reflections in the measurement setup, relative angle between the chip and the beam, and charge sharing could all account for the difference. Further analysis of these data is ongoing.

6. Heavy-ion radiation testing

AstroPix has been targeted for use in γ -ray detectors in low-Earth orbits at low inclination or outside Earth's radiation belts, requiring resilience to heavy-ion radiation environments. A previous iteration of AstroPix, AstroPix_v2, was tested for radiation hardness to single-event effects (SEEs). While minor changes in design or processing of CMOS semiconductor chips can have unintended consequences for SEE susceptibility, this experiment provides some indication for expected SEE response in future AstroPix revisions. Two classes of SEE were monitored:

1. **Catastrophic Single-event latchup (SEL)**, a destructive event leading to runaway power draws due to parasitic switching of the CMOS transistors [24], and
2. **Single-event upset (SEU)**, a temporary state where radiation causes bit flips which may degrade data or configuration. In the case of a single-event functional interrupt (SEFI), a system reset can restore nominal operation.

The design of the on-chip digital periphery, the most susceptible detector region, is identical in AstroPix_v2 and AstroPix_v3, and both chips were fabricated on a wafer 2 silicon substrate.

6.1. Experimental setup

The radiation tolerance of AstroPix_v2 was tested in June 2022 at the Lawrence Berkeley National Laboratory (LBNL) Berkeley Accelerator Space Effects (BASE) Facility 88" cyclotron [25]. The beam provides a cocktail of ions with 16 MeV/amu tune shown in Table 4. Four ion species with differing atomic masses provide a range of linear energy transfers (LETs), and tilting the detector plane relative to the ion beam direction of propagation provided additional effective LETs (the surface-incident LET in silicon at normal incidence divided by the cosine of the detector tilt angle). Surface energy was calculated with the SRIM-2013 code [26]. The effective range reported is the penetration depth of the ion species in silicon (multiplied by the cosine of the detector angle from the ion beam perpendicular when tilting).

Table 4

Ion beam properties from June 2022 radiation testing.

Ion	E_{initial} [MeV]	Air gap [mm] & Sensor tilt	E_{surface} [MeV]	Eff. LET [MeV·cm ² /mg]	Eff. range [μm]
⁴⁰ Ar ⁺¹⁴	642	20 : 0 ° 45 : 23 °	555 ± 1.0 737 ± 1.9	8.0 21	206 115
⁶³ Cu ⁺²²	1007	20 : 0 ° 45 : 23 °	805 ± 1.1 921 ± 3.0	19 32	141 107
⁷⁸ Kr ⁺²⁸	1317	20 : 0 ° 45 : 23 °	1021 ± 2.9 1216 ± 4.9	28 64	132 82
¹²⁴ Xe ⁺⁴³	1975	20 : 0 ° 35 : 23 °	1341 ± 4.6 1216 ± 4.9	57 64	98 82

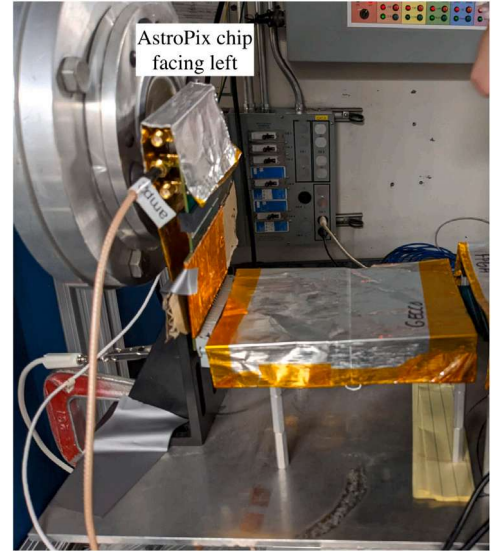


Fig. 13. AstroPix_v2 at the 88" Cyclotron (beam pipe on the left). AstroPix boards and auxiliary boards are covered to protect from stray ions.

Fig. 13 shows the experimental beamline set-up with AstroPix_v2 on the left, 20 mm away from the beam pipe. The AstroPix chip carrier board and auxiliary boards are covered with aluminum to protect active electronic components from recoil ions. Digitized event data was collected from the full pixel array (with 35% of pixels masked to reduce noise), as well as a diagnostic analog signal from a single pixel, and monitored in real-time for non-destructive SEEs. Four input voltage rails (analog 1.2 V and 1.8 V supplies, a 1.8 V supply for the chip's digital periphery, and a 2.7 V supply for the auxiliary readout boards) and the high voltage bias were also recording during irradiation for destructive and non-destructive SEEs.

Spaceflight standards [27] require instruments to be robust against catastrophic latchup up to a LET between 60–75 MeV·cm²/mg. Accurate flux measurements are provided from BASE through calibration of a set of four photomultiplier tubes (PMTs) to a centered PMT that is then removed before the beam run. Data were recorded for each beam exposure, beginning before the beam was on and ending shortly after the beam was shuttered. Each beam exposure was run to an 1×10^7 cm⁻² effective fluence, or until a SEFI event was recorded. For all effective LETs, a minimum of one beam exposure was performed to the full 1×10^7 cm⁻² effective fluence to test for destructive SELs, ignoring any SEFIs. Both high- ($\leq 4 \times 10^4$ cm⁻²s⁻¹) and low-flux (≤ 125 cm⁻²s⁻¹) beam exposures were performed after it was noted that the higher beam exposure flux was overwhelming the digital readout.

6.2. Radiation results

In total, data from 21 beam exposures were collected across four ion species and two incident angles. Two chips were tested with one

Table 5

Table of BASE cyclotron beamline runs listed by LET and recording fluence cross section, SEE class, and detector under test (DUT).

LET [MeV·cm ² /mg]	Avg Beam Flux [cm ⁻² s ⁻¹]	Min Fluence [cm ⁻²]	Cross Section [cm ²]	SEE Class	DUT
8	2.22 × 10 ⁴	1.00 ± .05 × 10 ⁷	≤ 9.99 × 10 ⁻⁸	None	1
19	2.34 × 10 ⁴	1.00 ± .05 × 10 ⁷	≤ 9.99 × 10 ⁻⁸	None	1
21	1.69 × 10 ⁴	6.61 ± .03 × 10 ⁶	1.51 ± 0.01 × 10 ⁻⁷	A	1
28	2.88 × 10 ⁴	5.24 ± .06 × 10 ⁶	1.91 ± 0.02 × 10 ⁻⁷	B	1
28	7.35 × 10 ³	8.23 ± .01 × 10 ⁶	1.21 ± 0.02 × 10 ⁻⁷	A	1
32	1.94 × 10 ⁴	9.97 ± .04 × 10 ⁶	1.00 ± 0.01 × 10 ⁻⁷	C	1
57	18.3	1.73 ± .06 × 10 ³	5.79 ± 0.10 × 10 ⁻⁴	B	1
57	3.48 × 10 ⁴	4.29 ± .07 × 10 ⁶	2.33 ± 0.04 × 10 ⁻⁷	A	1
57	111.8	8.02 ± .02 × 10 ⁴	1.25 ± 0.01 × 10 ⁻⁵	B	2
64	5.32 × 10 ⁴	5.76 ± .10 × 10 ⁶	1.74 ± 0.03 × 10 ⁻⁷	B	2

device used for 18 exposures and the second used for the final three runs at the highest LETs for confirmation of results. During testing, three potential classes of non-destructive events were identified. The first type (“Class A”) is likely a SEFI caused by flipped bits in the on-chip configuration registers. Class A events were characterized by a loss of both digital data and diagnostic analog signal coupled with a drop in supplied 1.8 V digital power to pre-configuration levels. Class A events were corrected with a digital chip reconfiguration without power cycling, and later replicated using a 1016 nm infrared laser to stimulate the digital periphery.

The other two types of non-destructive event (“Class B” and “Class C”) involved the processing of the detector’s digital data. Class B events were characterized by the off-chip digital decoder software failing to process unexpected data structure in the bitstream and crashing. Modifications to the digital decoder software during later analysis dramatically reduced the rate of decoder failures, but the underlying cause of the unexpected bitstream structure is unresolved. Event pileup due to high beam flux, issues with data encoding in the frontend firmware, or a true SEFI could all be potential culprits. A conservative approach has been taken to treat all Class B events as SEFIs for this analysis. Class C events are characterized by a bit flip that modified the leading byte of each digitized event data packet. This behavior would occasionally correct or restart itself during the run. Power cycling of the 1.8 V analog input to the detector would correct the behavior. Class C event behavior was observed in pre-beam baseline noise data, but was not reproducible in later testing.

Table 5 catalogs the beam exposure runs by effective LET and the resulting SEFI class of the run if any occurred. No Class A SEFIs occurred below an LET of 21 MeV·cm²/mg. Combined uncertainty arising from fluence and cross section uncertainties is estimated to 2 s of beam flux. In the case of multiple runs at the same LET, the lowest fluence until SEE is recorded.

A cross section of ≤ 9.99 × 10⁻⁸ cm² indicates no observed SEFIs. It was observed that Class B events occurred much more frequently at low beam flux. At high flux it is believed that the detector digital output was likely overrun and not returning all event data.

CREME96 [28], an engineering tool to calculate a worst-case galactic cosmic ray environment at solar minimum, was used to determine an on-orbit SEFI rate. For inputs into this tool, the SEFI cross-section as a function of LET was fit with a Weibull curve [29] of the form

$$F(x) = A \left(1 - e^{-[(x-x_0)/w]^s} \right), \quad (1)$$

where x is the effective LET, A is the limiting or plateau cross section, x_0 is an onset parameter such that $F(x) = 0$ for $x < x_0$, w is a width parameter, and s is a dimensionless exponent. All three described classes of observed detector behavior were treated as SEFIs. The data, due to limited LET test points and the different LET-based behavior of the three event classes, does not lend itself to a Weibull fit. However, for the sake of a conservative parameter inputs for the CREME96 model, we apply an over-constrained fit assuming worse possible factors to conservatively bound the on-orbit rate.

Table 6

Weibull parameters.

Curve	Saturation Cross Section [cm ²]	Onset LET [MeV·cm ² /mg]	Power (s)	Width (w)
1	3.00 × 10 ⁻⁷	18	5	1
2	6.00 × 10 ⁻⁴	31	5	7

Table 7

Worst-case SEFI rate for interplanetary space at solar minimum.

SEFI rate per day	SEFI rate per year
2.386 × 10 ⁻⁴	8.717 × 10 ⁻²

To account for these worst-case flux effects when calculating an upper bound on-orbit SEFI rate, the data have been fit with two Weibull curves and event rates summed. One curve was fit to all data below LET < 35 MeV·cm²/mg and data from the high-flux runs above LET > 35 MeV·cm²/mg. The second curve was added to include the low flux results at high LET that have high cross section, and using a conservative onset LET of 31 MeV·cm²/mg, as SEE cross section established at LETs of 21, 28, and 32 MeV·cm²/mg remained level. The fits are intentionally worst-case with steep increases and saturation levels at the highest cross section data point as opposed to an average. Corresponding Weibull parameters are given in Table 6.

The sensitive volumes defined in CREME96 had x- and y-dimensions equal to the square root of the saturated cross section; each volume was assigned a depth of 2 μm. The CMOS circuitry that is potentially responsible for the SEFIs have a shallow sensitive volume relative to chip thickness. Within CREME96, this shallower volume yields higher event rates than would a deeper sensitive volume designation, conservatively bounding the rate. Total event rates for the worst-case assumptions described above are given in Table 7.

After completing beam exposures at all effective LETs, no destructive high-current events occurred, suggesting AstroPix_v2 has a destructive SEL threshold greater than 64 MeV·cm²/mg. The device is susceptible to recoverable soft errors with a LET threshold above 19 MeV·cm²/mg. The onset LET above 19 MeV·cm²/mg indicates proton-induced secondary ions are unlikely to cause on-orbit SEEs. This result is unique to AstroPix_v2, though the digital block of AstroPix_v2 is identical to that of AstroPix_v3. The satisfactory results raise confidence in future designs. Future AstroPix versions will be tested in a similar manner to ensure continued compliance with spaceflight standards.

7. Conclusion and outlook

The AstroPix design program is strong and robust as advances in the design are consistently made toward realizing a final version. AstroPix v1 through v3 show consistent improvements in key metrics such as power consumption and energy resolution, as shown in Table 1 however the design process is ongoing.

This paper has presented an overview of AstroPix_v3 HVCMOS design and benchtop operation. Current-voltage measurements illustrated chip properties, including high-voltage breakdown between $-380 - 400$ V. An overview of energy resolution studies and results from Ref. [10] were presented, where $10.4 \pm 3.2\%$ FWHM energy resolution at 59.5 keV was achieved using a medium-resistivity $200-400 \Omega \cdot \text{cm}$ substrate. The measured $94 \pm 6 \mu\text{m}$ depletion of this substrate is discussed, and plans for increasing this depletion depth to the designed $500 \mu\text{m}$ were presented. Radiation testing with a cocktail of ions was performed with AstroPix_v2 which shares an identical digital bloc to AstroPix_v3, and no catastrophic events were detected. Single event functional interrupt rates were estimated to be at the order of 10^{-4} per day in the planned AMEGO-X orbit, which is a tolerable rate.

The first space-based test of AstroPix will be the Astropix Sounding rocket Technology dEmonstration Payload (A-STEP), featuring three AstroPix_v3 quad chips to be flown on a sounding rocket in 2026 [30]. The first large-format test of AstroPix is the AMEGO-X prototype tower ComPair2 [31], which is intended to fly on a high-altitude balloon. The other AMEGO-X subsystems and operations team take heritage from the 2023 ComPair flight [32]. ComPair2 features 10 tracker layers with 380 AstroPix chips per layer, which will interact with a unified trigger system to return science data. The results from this publication serve as a baseline for AstroPix_v3 operation, and will provide the basis for A-STEP design, optimization, calibration, and analysis.

At the time of writing, AstroPix_v4 has been fabricated and is undergoing preliminary testing [18]. This testing has informed the submission of AstroPix_v5 during the 2025 calendar year. Continued improvements in power consumption and operational range are expected with the elimination of an external fast 200 MHz clock and addition of dynamic feedback capacitance.

The AstroPix project benefits from the expertise of international collaborators in multiple fields of physics and engineering. Though not currently a final design, each AstroPix version improves upon the previous. The ultimate design will revolutionize γ -ray astronomy, especially in the elusive MeV range.

CRediT authorship contribution statement

Amanda L. Steinhebel: Writing – review & editing, Writing – original draft, Validation, Supervision, Software, Formal analysis, Conceptualization. **Daniel P. Violette:** Writing – review & editing, Validation, Supervision. **Regina Caputo:** Writing – review & editing, Validation, Supervision, Resources, Project administration, Investigation, Funding acquisition, Conceptualization. **Anthony Affolder:** Investigation. **Autumn Bauman:** Investigation. **Carolyn Chinatti:** Investigation. **Awake Deshmukh:** Investigation. **Vitaliy Fadayev:** Validation, Supervision, Investigation. **Yasushi Fukazawa:** Supervision, Investigation. **Manoj Jadhav:** Writing – review & editing, Supervision, Software, Investigation, Formal analysis. **Carolyn Kierans:** Investigation. **Bobae Kim:** Visualization, Validation, Formal analysis. **Jihee Kim:** Investigation. **Henry Klest:** Investigation. **Olivia Kroger:** Visualization, Investigation, Formal analysis. **Kavic Kumar:** Investigation, Formal analysis. **Shin Kushima:** Investigation. **Jean-Marie Lauenstein:** Writing – review & editing, Supervision, Methodology, Formal analysis. **Adrien Laviron:** Investigation. **Richard Leys:** Validation, Software, Investigation. **Forest Martinez-Mckinney:** Investigation. **Jessica Metcalfe:** Validation, Supervision, Project administration, Funding acquisition. **Zachary Metzler:** Investigation. **John W. Mitchell:** Investigation. **Norito Nakano:** Investigation, Formal analysis. **Jennifer Ott:** Validation, Supervision, Methodology, Formal analysis. **Ivan Peric:** Supervision, Resources, Investigation. **Jeremy S. Perkins:** Investigation. **Max R. Rudin:** Investigation. **Taylor (K.W.) Shin:** Investigation. **Grant Sommer:** Investigation, Formal analysis. **Nicolas Striebig:** Writing – review & editing, Resources, Investigation, Conceptualization. **Yusuke Suda:** Writing – review & editing, Visualization, Supervision, Formal analysis. **Hiroyasu Tajima:** Writing – review & editing, Supervision, Investigation. **Janeth Valverde:** Investigation. **Maria Zurek:** Investigation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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