Versatile Converter Impedance Modeling with Matrix Signal Flow Graphs to Include Frequency Coupling

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***Abstract*—The behavior of grid-connected converters is defined by their control systems over a wide frequency band. Understanding the impact of the control design on the converter output impedance is thus essential. In the lower frequency range, asymmetric control elements such as the phase-locked loop (PLL) or DC link control introduce frequency coupling, resulting in a multiple-input multiple-output (MIMO) system structure. Deriving the MIMO converter impedance model can be a complex and demanding task. This paper presents a structured approach to model the converter output impedance based on its signal-flow graph that accounts for asymmetric control loops and frequency coupling. The technique is applied to analyze the impedance of a real converter system, focusing on the low-frequency range. The obtained analytical impedance curves are validated by experimental impedance measurements that capture frequency coupling. Finally, the validated converter impedance matrix is used to assess and mitigate a low-frequency instability observed in a power hardware-in-the-loop (PHIL) setup.**

***Index Terms*—Converter control, stability analysis, harmonic stability, converter impedance measurement, frequency coupling**

I. Introduction

The ongoing energy transition includes a shift towards more power electronic components in the electrical grid. This affects both the generation and the load side, as well as the integration of storage systems. All of these new installations contain control systems that have been found to interact with each other and with the grid under certain circumstances [1]. The impedance-based stability criterion is used to assess unstable system conditions and has already been studied extensively [2], [3]. Knowledge about the converter output impedance and how it is affected by the control system is therefore highly relevant. As the converter controls act on multiple timescales with different control loops, oscillations may occur in a wide frequency range [1]. In the high-frequency range, the converter impedance is defined by the grid filter components and the current controller. These elements show symmetric behavior in the dq-frame and can be transformed into decoupled positive and negative sequence impedances [4]. In contrast, the phase-locked loop (PLL) and the DC link voltage control are asymmetric control elements that impact the impedance in the low-frequency range. This results in a converter impedance that introduces couplings between the positive and negative sequences at different frequencies. Hence, the converter impedance needs to be described using a transfer matrix to model the sequence and frequency coupling [5]. In previous works, the impedance matrix is derived by first formulating a state-space model [6], by reformulation and substitution of the system equations [5], or directly derived from the control structure without further detail [7]. All of these methods result in valid converter impedances, but may be complex to use without sufficient experience and without clear instructions on how they need to be adapted according to the investigated system. Related works have shown the benefit of using signal-flow graphs (SFG) to determine converter impedances and system transfer functions in the single-input single-output case [8]–[10]. However, when sequence and frequency couplings in the converter impedance are considered, these techniques are no longer valid.

The contribution of this paper is a structured approach to model the converter impedance based on its signal-flow graph. The method lists explicit step-by-step instructions and results in an impedance matrix that models the frequency coupling. The procedure is applied to derive the impedance for a 50 kHz SiC grid-connected converter with a focus on the low-frequency range with asymmetric outer control loops. The obtained impedance matrix is then validated with experimental impedance measurements that capture the frequency

coupling. Finally, the validated impedance matrix is utilized to assess and mitigate a low-frequency instability observed in a laboratory PHIL setup.

II. Converter Impedance Model

A. Converter System and Signal-Flow Graph

The converter system considered in this paper is depicted in Fig. 1. It consists of a two-level converter connected to the grid using an LCL filter. Relevant system parameters are listed in Table I. The investigated converter control implemented in the grid-aligned *dq*-frame is shown in Fig. 2. The park transform is applied using the grid phase angle θ identified by the PLL. The DC link voltage controller $G_{\mathrm{vc}}(s) = k_{\mathrm{vc,p}} + k_{\mathrm{vc,i}}/s$ defines the d-component of the current setpoint $i_{\mathrm{set,d}}$, while the q-component $i_{\mathrm{set,q}}$ can be selected as desired for reactive power exchange. The setpoints for the grid current i_{g} are tracked by the current controller $G_{\mathrm{cc}}(s) = k_{\mathrm{cc,p}} + k_{\mathrm{cc,i}}/s$, which for the sake of simplicity does not include decoupling terms. Additionally, a proportional PCC voltage feed-forward with $G_{\mathrm{ff}} = k_{\mathrm{ff}}$ is added to the current controller output in the stationary $\alpha\beta$-frame. The resulting voltage output is affected by the control and PWM delay $G_{\mathrm{d}}(s) = e^{-T_{\mathrm{d}}s}$.

In Fig. 3, the signal-flow graph of the presented control structure is shown. The graph also includes the LCL filter and DC link dynamics. Note that the path gains are 2x2 transfer matrices to describe the couplings between the d- and q-components, as well as control parts that do not act symmetrically on both components. These include the PLL effects on the park transform in both directions, which are modeled according to [5], and the DC link dynamics:

$$G_{\mathrm{DC}}(s) = \begin{bmatrix} 1/(s\,C_{\mathrm{DC}}) & 0 \\ 0 & 0 \end{bmatrix} g_{\mathrm{DC}} \tag{1}$$

$$G_{\mathrm{PLL}}(s) = \begin{bmatrix} 0 & -H_{\mathrm{PLL}}(s) I_{\mathrm{q,op}} \\ 0 & H_{\mathrm{PLL}}(s) I_{\mathrm{d,op}} \end{bmatrix} \tag{2}$$

$$\tag{3}$$

$$Y_{\mathrm{PLL}}(s) = \begin{bmatrix} 0 & -H_{\mathrm{PLL}}(s) V_{\mathrm{cq,op}} \\ 0 & H_{\mathrm{PLL}}(s) V_{\mathrm{cd,op}} \end{bmatrix} \tag{4}$$

$$H_{\mathrm{PLL}}(s) = \frac{G_{\mathrm{PI,PLL}}(s)}{s + G_{\mathrm{PI,PLL}}(s)} \tag{5}$$

$$G_{\mathrm{PI,PLL}}(s) = k_{\mathrm{PLL,p}} + \frac{k_{\mathrm{PLL,i}}}{s} \tag{6}$$

$I_{\mathrm{dq,op}}$ are the steady-state operating point values of the grid current and $V_{\mathrm{cdq,op}}$ the steady-state control output voltages.

TABLE I
Relevant System Parameters

Parameter	Symbol	Value
Converter-side LCL inductance	L_{fi}	100 µH
Grid-side LCL inductance	L_{fg}	50 µH
LCL filter capacitance	C_{f}	13.5 µF
DC link capacitance	C_{DC}	1.4 mF
DC link voltage setpoint	$v_{\mathrm{DC,set}}$	650 V
Switching and sampling frequency	f_{sw}	50 kHz

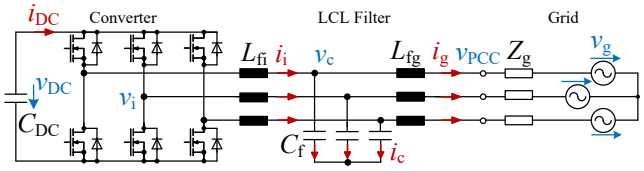

Fig. 1. Converter with LCL filter and DC link

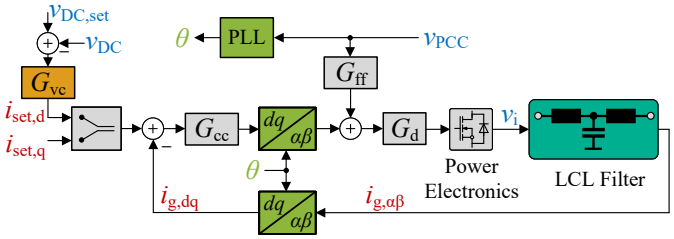

Fig. 2. Converter control structure

Note that this control output voltage differs from the steady-state grid voltage when using PCC voltage feed-forward. To model the DC link dynamics, the steady-state q-component of the grid voltage $V_{\mathrm{PCC,q}}$ is assumed to be zero such that the DC current is linearized to

$$i_{\mathrm{DC}} = g_{\mathrm{DC}}\, i_{\mathrm{i,d}} \text{ with } g_{\mathrm{DC}} = \frac{3}{2}\frac{V_{\mathrm{PCC,d}}}{v_{\mathrm{DC,set}}}. \tag{7}$$

B. Impedance Derivation using Matrix Signal-Flow Graph

Mason's gain formula provides a convenient way to determine transfer functions based on a signal-flow graph, especially for systems with multiple and nested loops. For MIMO systems, the noncommutative property of the transfer matrices requires a generalized form called *forward return loop (FRL)* method [11], [12]. It consists of the following steps to determine the desired transfer matrix T:

1) Collect all forward paths from the input node a to the output node b.
2) Determine the loop gain S_i^k for each node i along path k. First, split all nodes on path k between node i and the output node b. The loop gain S_i^k is thus path-dependent. Then split node i into an input and output node and recursively compute the transfer matrix between them.
3) Determine the node factors along each path k to $N_i^k = (I - S_i^k)^{-1}$

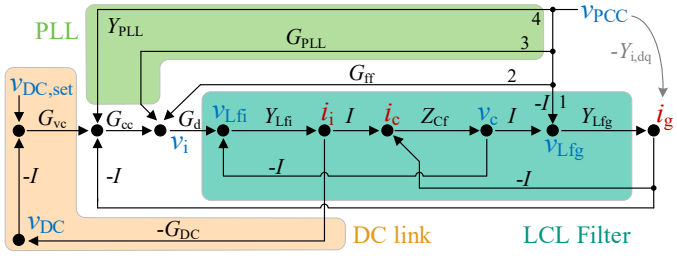

Fig. 3. Signal-flow graph of converter control and dynamics

4) Form the path product P_k. Starting at the output node, form the product using the SFG edge matrices and the node factors.
5) Obtain T as the sum all path products P_k.

The procedure can be formally described as:

$$T = \sum_k P_k \text{ with } P_k = \prod_{i=L}^{1} N_i^k A_i^k \text{ and } N_i^k = (I - S_i^k)^{-1},$$

where A_i^k is the i$^{\text{th}}$ transfer matrix on path k with length L.

The FRL method is now applied to the SFG shown in Fig. 3 with $T = -Y_{\mathrm{i,dq}}$ from node v_{PCC} to node i_g:

$$P_1 = N_{ig} Y_{Lfg} (-I) \tag{8}$$
$$P_2 = N_{ig} Y_{Lfg} N_{vc}\, Z_{Cf}\, N_{ii}\, Y_{Lfi}\, G_\mathrm{d}\, G_\mathrm{ff} \tag{9}$$
$$P_3 = N_{ig} Y_{Lfg} N_{vc}\, Z_{Cf}\, N_{ii}\, Y_{Lfi}\, G_\mathrm{d}\, G_\mathrm{PLL} \tag{10}$$
$$P_4 = N_{ig} Y_{Lfg} N_{vc}\, Z_{Cf}\, N_{ii}\, Y_{Lfi}\, G_\mathrm{d}\, G_\mathrm{cc}\, Y_\mathrm{PLL} \tag{11}$$

$$N_{ii} = (I - Y_{Lfi}\, G_\mathrm{d} G_\mathrm{cc} G_\mathrm{vc} G_\mathrm{DC})^{-1} \tag{12}$$
$$N_{vc} = (I + Z_{Cf}\, N_{ii} Y_{Lfi})^{-1} \tag{13}$$
$$N_{ig} = (I + Y_{Lfg}\, N_{vc} Z_{Cf} N_{ii} Y_{Lfi} G_\mathrm{d} G_\mathrm{cc} + Y_{Lfg}\, N_{vc} Z_{Cf})^{-1} \tag{14}$$

In this case, the node factors N_i^k are identical for all forward paths. The converter output impedance $Z_{\mathrm{i,dq}}$ is then determined to

$$Z_{\mathrm{i,dq}} = Y_{\mathrm{i,dq}}^{-1} \quad \text{with} \quad Y_{\mathrm{i,dq}} = -(P_1 + P_2 + P_3 + P_4).$$

C. Reference Frame Transformations

The converter controls and thus also the signal-flow graph in Fig. 3 are formulated in the *dq*-frame. The transfer matrices for the passive components Y_{Lfi}, Z_{Cf} and Y_{Lfg} are defined in the $\alpha\beta$-frame and need to be transformed into the *dq*-frame. Similarly, this paper considers the converter output impedance in the stationary $\alpha\beta$-frame. To this end, the reference frame transformations described in [4], [5] are applied:

$$Z_{\mathrm{i,pn}}(s) = A_\mathrm{Z}\, Z_{\mathrm{i,dq}}(s)\, A_\mathrm{Z}^{-1} \text{ with } A_\mathrm{Z} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & j \\ 1 & -j \end{bmatrix} \tag{15}$$

This results in the impedance definition

$$\begin{bmatrix} V_\mathrm{p}(s_+) \\ V_\mathrm{n}(s_-) \end{bmatrix} = \underbrace{\begin{bmatrix} Z_\mathrm{pp}(s) & Z_\mathrm{pn}(s) \\ Z_\mathrm{np}(s) & Z_\mathrm{nn}(s) \end{bmatrix}}_{Z_{\mathrm{i,pn(s)}}} \begin{bmatrix} I_\mathrm{p}(s_+) \\ I_\mathrm{n}(s_-) \end{bmatrix}, \tag{16}$$

with $s_+ = s + \omega_0$, $s_- = s - \omega_0$ and ω_0 as the fundamental frequency. In this notation, the sequence and frequency coupling become apparent with the off-diagonal entries $Z_\mathrm{pn}(s)$ and $Z_\mathrm{np}(s)$. A drawback of this notation is the possibility of a negative sequence with a negative frequency, which is equal to a positive sequence at the same frequency [5]. This implies that a positive sequence at frequency ω below twice the fundamental frequency ω_0 will result in another positive sequence at the mirror frequency $2\omega_0 - \omega$.

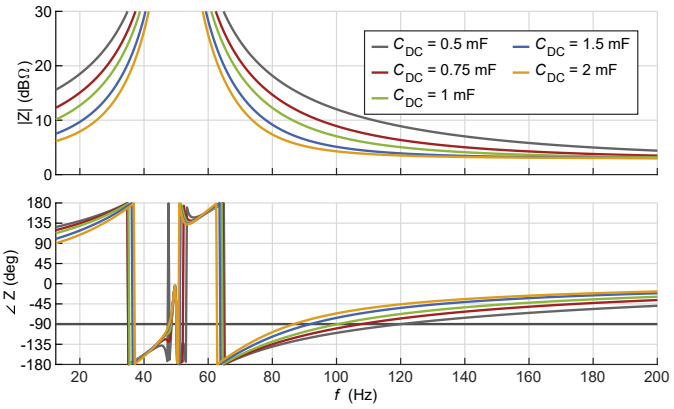

Fig. 4. Impact of DC link capacitance on analytical positive sequence converter impedance Z_pp

D. Parameter Influence on Analytical Converter Impedance

The derived converter impedance model can be used to investigate the impact of selected control or hardware parameters. For example, Fig. 4 shows the influence of the DC link capacitance C_DC on the positive sequence impedance. This influence is of interest, as other devices connected to the DC bus will change the total capacitance and therefore the converter output impedance Z_i seen from the AC side.

III. Measurement Validation

This section validates the impedance model derived using the presented method through impedance measurements that account for frequency coupling effects. Furthermore, instabilities predicted by the model are confirmed in a PHIL setup and mitigated by control adjustments.

A. Measurement Setup and Impedance Measurement

The measurement setup is shown in Fig. 5. An Egston Power CSU100 grid emulator provides a 400 V / 50 Hz grid. Additionally, the voltage contains a superimposed excitation at the investigated frequencies from 12.5 Hz to 200 Hz in both the positive and negative sequence with an amplitude of $V_\mathrm{e} = 3\,\mathrm{V}$. The converter system to be measured is connected to the emulator, where the control structure shown in Fig. 2 is implemented on an Artix™-7 FPGA. The investigated control parameters can be tuned online to enable subsequent measurement runs without reprogramming the FPGA.

The converter impedance is determined based on the converter current response to voltage excitations. The frequency coupling property requires also considering the relevant mirror frequency response in the correct sequence. This is demonstrated in Fig. 6, where the operating point is set to $I_\mathrm{d,op} = I_\mathrm{q,op} = 0\,\mathrm{A}$ and a positive sequence component at 125 Hz is excited. It results in a positive sequence current response at the frequency, but also a negative sequence component visible in the peaks ($i_\mathrm{c} \rightarrow i_\mathrm{b} \rightarrow i_\mathrm{a}$) at 25 Hz as predicted by the impedance model in (16). With two orthogonal excitation vec-

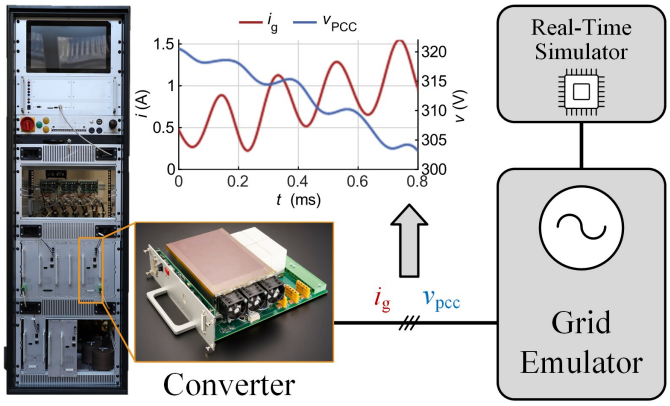

Fig. 5. Impedance measurement and PHIL setup

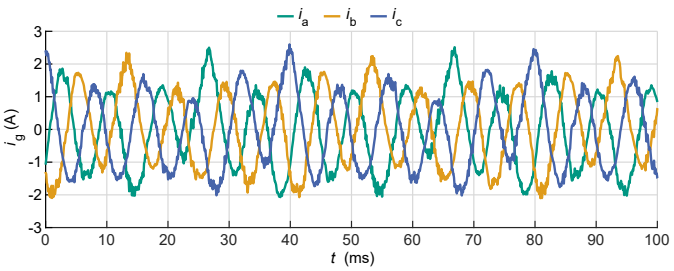

Fig. 6. Current response to voltage excitation with frequency coupling

tors for every frequency and the definitions from Section II-C, the converter impedance matrix is calculated as

$$Z_{\mathrm{i,pn(s)}} = \begin{bmatrix} Z_{\mathrm{pp}}(s)\, Z_{\mathrm{pn}}(s) \\ Z_{\mathrm{np}}(s)\, Z_{\mathrm{nn}}(s) \end{bmatrix} = \begin{bmatrix} V_{\mathrm{p1}}(s_+)\, V_{\mathrm{p2}}(s_+) \\ V_{\mathrm{n1}}(s_-)\, V_{\mathrm{n2}}(s_-) \end{bmatrix} \begin{bmatrix} I_{\mathrm{p1}}(s_+)\, I_{\mathrm{p2}}(s_+) \\ I_{\mathrm{n1}}(s_-)\, I_{\mathrm{n2}}(s_-) \end{bmatrix}^{-1}. \tag{17}$$

For the following impedance measurements, the default control parameters and operating point values from Table II are used, if not otherwise specified. Results for the extracted converter impedances are shown in Fig. 7, where the bandwidth of the PLL is varied. The impedance model is depicted by solid lines and is in good agreement with the impedance measurements represented by markers, both in phase and in magnitude for all considered PLL bandwidths. At 50 Hz, the

TABLE II
RELEVANT CONTROL AND OPERATING POINT PARAMETERS

Parameter	Symbol	Value
Current control proportional gain	$k_{\mathrm{cc,p}}$	1
Current control integral gain	$k_{\mathrm{cc,i}}$	75
PCC voltage feed-forward gain	k_{ff}	0
DC link control proportional gain	$k_{\mathrm{vc,p}}$	1.5
DC link control integral gain	$k_{\mathrm{vc,i}}$	256
PLL proportional gain	$k_{\mathrm{PLL,p}}$	0.785
PLL integral gain	$k_{\mathrm{PLL,i}}$	3.14
Operating point currents	$I_{\mathrm{d,op}}, I_{\mathrm{q,op}}$	0 A
PCC voltage	$V_{\mathrm{PCC,d}}$	326 V

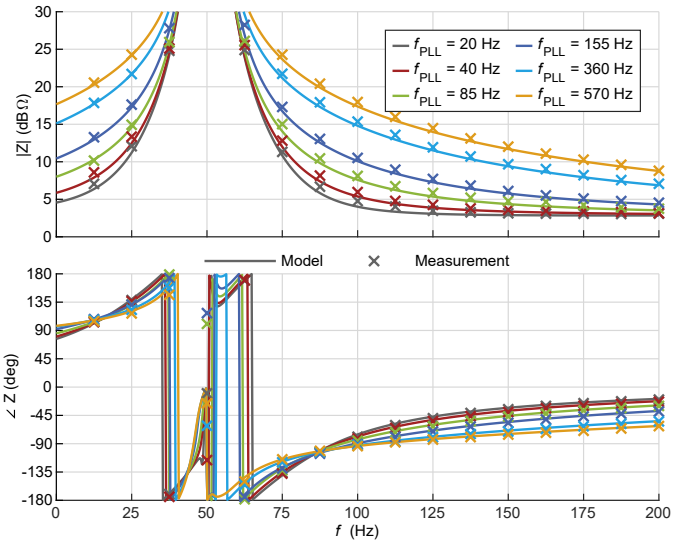

Fig. 7. Measured and modeled positive sequence impedance Z_{pp} with variation of the PLL bandwidth f_{PLL}

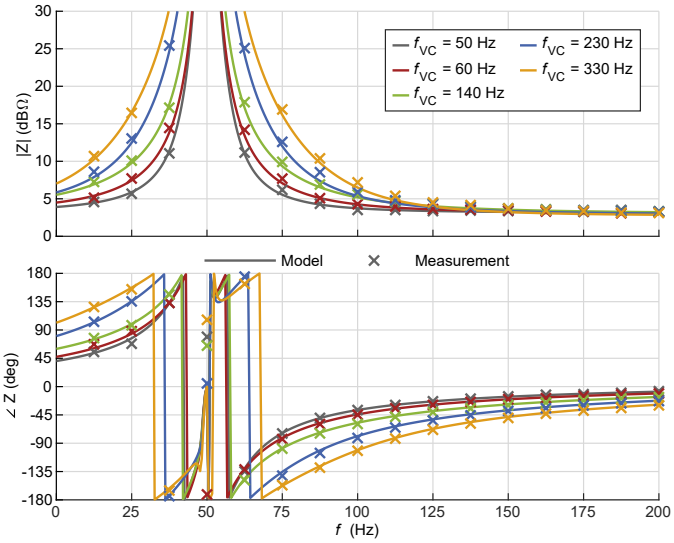

Fig. 8. Measured and modeled positive sequence impedance Z_{pp} with variation of the voltage controller bandwidth f_{VC}

integral part of the current controller G_{cc} results in a high impedance magnitude and multiple phase wraps.

In Fig. 8, the bandwidth of the DC link voltage controller G_{vc} is varied. Again, the measured positive sequence impedance shows a good match with the impedance model. The analytical model and the measurements show the strong influence of the considered control elements on the output impedance. In both cases, increasing the bandwidth raises the magnitude and lowers the phase of the positive sequence impedance Z_{pp}.

B. Instability Assessment and Mitigation in a PHIL setup

In the following, the converter impedances obtained by analytical modeling and impedance measurements will be

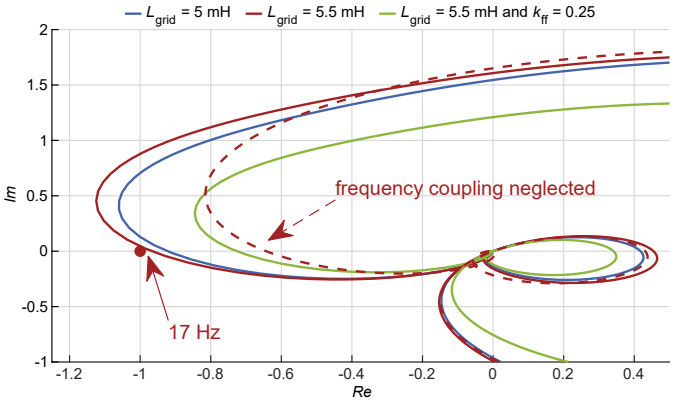

Fig. 9. Nyquist diagrams for the eigenvalues of $L = Z_{\text{grid}} Z_{\text{i}}^{-1}$ with variations in grid and control parameters

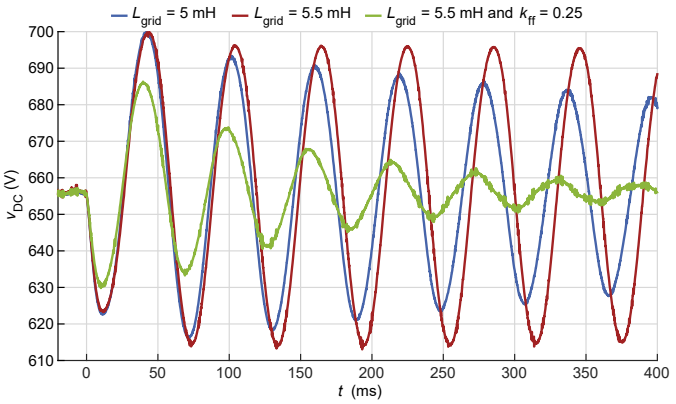

Fig. 10. Measured DC link voltage v_{DC} for grid voltage steps in critical stability scenarios

used to assess and mitigate an instability in a PHIL setup. In case the positive and negative sequence impedances can be approximated to be decoupled, impedance curves in the positive and negative sequence as given in the preceding section suffice for a stability assessment. Due to the asymmetric controls described in section II-A and the resulting frequency coupling, this is not valid for the investigated converter system. To assess the stability of a MIMO system, the generalized Nyquist criterion (GNC) is used [3]. In a simplified form and applied to the considered grid-converter system, it states that the system is stable if the traces of the frequency-dependent eigenvalues of $L(s) = Z_{\text{grid,pn}}(s) Z_{\text{i,pn}}^{-1}(s)$ do not encircle the critical point $(-1, 0)$. Fig. 9 shows the Nyquist diagram for such eigenvalues, assuming an inductive grid. A resistance of $R_{\text{grid}} = 4\,\Omega$ is placed in parallel to the grid inductance to avoid instabilities in the PHIL setup. The converter DC link voltage controller G_{vc} is parametrized for a bandwidth of $f_{\text{VC}} = 50\,\text{Hz}$. The plot shows that the controller parameters provide low damping for $L_{\text{grid}} = 5\,\text{mH}$, which further deteriorates for $L_{\text{grid}} = 5.5\,\text{mH}$. The eigenvalue trace is closest to the critical point at a frequency of $f_{\text{crit}} = 17\,\text{Hz}$ using the notation in (16). Enabling partial PCC voltage feed-forward with $k_{\text{FF}} = 0.25$ significantly improves the system stability at the same grid inductance. Also shown in Fig. 9 is the influence of frequency coupling effects. For the critical configuration, the dashed red line shows the resulting eigenvalue trace when neglecting the frequency coupling by setting the off-diagonal terms in $Z_{\text{i,pn}}(s)$ to zero. The curve erroneously indicates a stable system and highlights the need to include frequency coupling for the stability assessment.

The stability assessments for the grid and control configurations investigated analytically in Fig. 9 are validated in a PHIL setup. An Opal-RT OP4510 real-time simulator connected to the grid emulator is used to emulate the grid impedance. To excite the system, the grid voltage is stepped down by $30\,\text{V}$ at $t = 0\,\text{ms}$. Fig. 10 shows associated measurements for the considered scenarios. The system response in the DC link voltage v_{DC} confirms the stability assessments using the GNC. Increasing the grid inductance to the critical value of $L_{\text{grid}} = 5.5\,\text{mH}$ results in oscillations with near-zero damping at $f_{\text{crit}} = 17\,\text{Hz}$. The oscillations are effectively damped when enabling partial PCC voltage feed-forward with $k_{\text{ff}} = 0.25$.

IV. Conclusion

This paper presents a structured approach to derive the analytical converter output impedance. Importantly, this method is applicable to control structures with asymmetric elements, that result in a MIMO control structure. The proposed impedance derivation is well suited to systems with multiple forward paths and feedback loops, formed by passive components, control loops and indirect effects such as the PLL influence. While the presented method can result in complex analytical terms, this is inevitable for MIMO systems with multiple feedback loops and is effectively handled by computer algebra systems. The system description based on a signal-flow graph enables versatile integration of modifications to the control structure such as an additional feed-forward path. By following the outlined step-by-step instructions, the desired converter impedances are obtained. Impedance measurements that include frequency coupling are in good agreement with the analytical converter impedances both in magnitude and in phase over the investigated frequency range and for control parameter variations. The analysis and mitigation of an instability in a PHIL setup further validate the derived analytical converter impedance and its frequency coupling characteristics, as well as highlighting the necessity of considering these coupling effects.

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