Power Loss Comparison of Different Operation Modes of a Medium Voltage Solid-State Transformer

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***Abstract*—This paper focuses on optimized operation modes to reduce the overall power losses of a modular three-phase Solid-State Transformer (SST) for an AC-DC grid coupling. The topology of the investigated SST is a Cascaded H-Bridge structure, consisting of a series connection of Dual Active Bridges (DAB) to provide a multilevel phase voltage. This structure inherently has several degrees of freedom to distribute the transmitted power between the modules. Using different approaches to distribute power among the DABs offers significant potential for reducing power losses. Extrapolated values for an SST phase, derived from experimental results of a 450 kW, 720 V to 1800 V DAB, indicate a possible reduction of up to 20%.**

***Index Terms*—Solid-State Transformer, Efficiency, Dual Active Bridge, Cascaded H-Bridge, Optimization.**

I. Introduction

In recent years, significant research has been conducted to mitigate the disadvantages and enhance the advantages of Solid-State Transformer (SST) compared to state-of-the-art step-down line frequency transformers combined with an additional converter stage. However, both technologies remain relevant depending on the application and boundary conditions [1]–[6]. If an SST is used, a suitable topology for connecting the medium voltage (MV) AC to a low voltage (LV) DC grid is the input serial output parallel (ISOP) structure of an SST. This topology comprises identical and modular power modules arranged in a Cascaded H-Bridge (CHB) stage. The power modules can transfer power to either the MV or LV side, depending on the desired direction of power flow. In this context, the MV side is also referred to as the secondary side, while the LV side is considered the primary side. In addition to bidirectional power flow capability, these modules must meet further requirements such as galvanic isolation, high power density, and efficient buck and boost operation of the output voltage. Among the available options, the CLLC and the Dual Active Bridge (DAB) topologies are valid candidates. However, the DAB is preferred in this investigation due to its superior controllability for varying, bidirectional power flow in buck and boost operation [7].

In addition to low costs, high gravimetric and volumetric power density, a low device count of the AC to DC conversion system and the efficiency are key factors that influence the topology and design decisions. One effective way to improve the overall efficiency of the SST is by enhancing the efficiency of the individual DAB modules. This approach has been widely investigated in previous studies on SST design [8]–[11], as well as in research focusing on advanced modulation schemes for the DAB across various operating conditions [12]–[14]. In contrast, this publication presents a different approach by using a degree of freedom inherent in the modular SST: the improved distribution of setpoints among individual modules. This work builds upon the concepts outlined in [15]. Starting with measured and fitted losses from a single unscaled MV DAB, a power loss model for the individual phases of the SST is developed and investigated. By applying different current setpoints of the individual DABs within a phase, the model calculates and predicts the phase's power losses for the next operation point (OP). This predictive approach allows for optimizing the current setpoints of the DABs, achieving significant reductions in total phase and therefore system losses.

This publication is structured as follows: Section II introduces the SST topology and the DAB power module of the investigated system. Section III outlines the different concepts of the operation modes (OM)s. The MV DAB power module and the SST setup are described in Section IV. Section V presents calculated results for the SST, based on experimental data from the DAB, leading to the conclusion of both the reduction in power losses and the effectiveness of the proposed OMs. Finally, Section VI summarizes the main achievements.

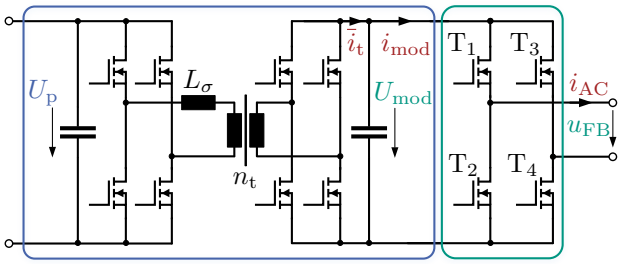


Fig. 1: Power module with DAB stage for power supply (blue) and CHB cell output stage (green).

TABLE I
Switching states of the CHB cell

State	Conducting	Output voltage u_FB	Module current i_mod
Positive	$\mathrm{T}_1, \mathrm{T}_4$	U_mod	i_AC
Negative	$\mathrm{T}_2, \mathrm{T}_3$	$-U_\mathrm{mod}$	$-i_\mathrm{AC}$
Bypass 1	$\mathrm{T}_1, \mathrm{T}_3$	0 V	0 A
Bypass 2	$\mathrm{T}_2, \mathrm{T}_4$	0 V	0 A

II. Topology

The topology that is investigated is a three-phase modular CHB-based SST in star connection. Each cell is powered individually by a galvanically isolated DAB. A single power module, comprising a DAB stage and a CHB cell, is shown in Fig. 1. The DAB, highlighted in blue, facilitates unrestricted bidirectional power flow and can operate in unity gain, buck, or boost mode. The CHB cell, highlighted in green, provides the AC output voltage u_FB for each module. The overall topology of the prototype is depicted in Fig. 2. The DAB stages on the left-hand side of the figure are connected in parallel and powered by a bidirectional DC voltage source with an output voltage U_p. The converter's AC output voltages $u_{\mathrm{AC},x}$, with $x \in \{\mathrm{U}, \mathrm{V}, \mathrm{W}\}$, are generated by the series connection of m_ph CHB cells. Each CHB cell, consisting of four MOSFETs T_1 to T_4, can generate three output voltage levels based on the MOSFET switching states. Table I shows these states along with the resulting output voltage u_FB and module current i_mod as a function of the phase current $i_{\mathrm{AC},x}$.

III. Operation Modes

In the following sections, first, the mathematical model of the power losses of the DAB and SST phase is derived, then three different OMs are described and compared with regard to their advantages and disadvantages.

A. Mathematical models of the DAB's and SST phase's power losses

To develop a mathematical model for the power losses of a DAB, measurements with a constant voltage source are conducted using a power meter. The measured losses $P_{\mathrm{losses,DAB,meas}}(\bar{i}_\mathrm{t})$ are approximated by two polynomial functions, one for positive and one for negative currents $\bar{i}_\mathrm{t}$, c.f. Fig. 4. Since the test setup was a constant voltage power

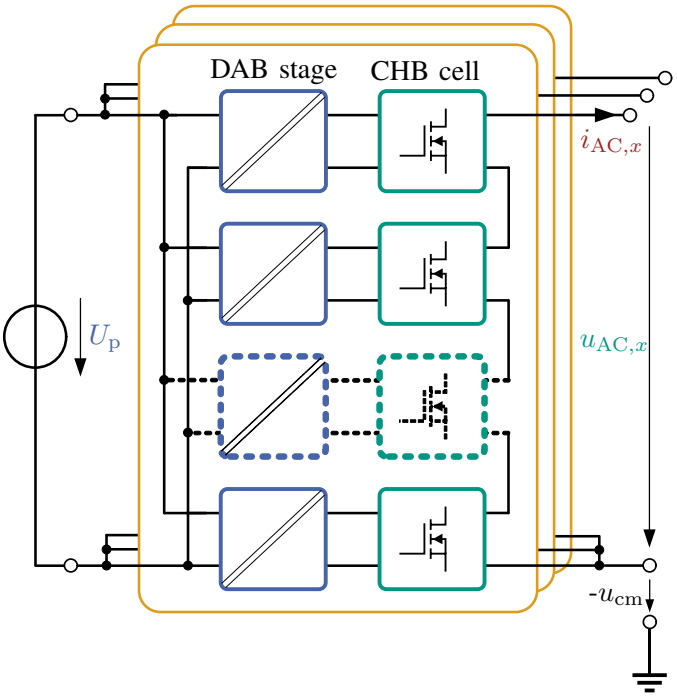


Fig. 2: Three phase modular ISOP SST for AC/DC grid coupling. The dotted module means that there can be multiple modules.

sink, the transmitted rectified transformer current $\bar{i}_\mathrm{t}$ equals the module current i_mod. The general shape of the resulting loss function of a single DAB defines the potential for optimizing the setpoint vector for all DABs $\bar{\boldsymbol{i}}_\mathbf{t}^* = \left(\bar{i}_{\mathrm{t},1}^*, \bar{i}_{\mathrm{t},2}^*, ..., \bar{i}_{\mathrm{t},k}^*\right)^T$ with $k \in \{1, 2, ..., m_\mathrm{ph}\}$. This single-module loss function can be extended to (1) to estimate the total losses of an SST phase, $P_\mathrm{losses}(\bar{\boldsymbol{i}}_\mathbf{t}^*)$, comprising all m_ph modules. For phase loss calculations, it is assumed that the SST phase operates with level shifted pulse width modulation (LSPWM), meaning that only one module per phase is controlled by pulse width modulation (PWM), while the others are constantly switched on or off over a switching period [16]. To prevent a static temperature drift of the modules when using this modulation scheme, a flexible carrier permutation method, sorted by cell temperature, as proposed in [17], can be employed. This approach enhances the thermal management and reliability of the SST.

$$P_\mathrm{losses}\left(\bar{\boldsymbol{i}}_\mathbf{t}^*\right) = \sum_k P_{\mathrm{losses,DAB}}\left(\bar{i}_{\mathrm{t},k}^*\right) \tag{1}$$

Depending on the setpoints for the DABs, a different amount of power losses occur. For simplicity, it is assumed that the actual transmitted current $\bar{i}_{\mathrm{t},k}$ matches the current setpoint $\bar{i}_{\mathrm{t},k}^*$ of the k^th DAB, since current controllers are in use. Furthermore, the phase index x is omitted for readability.

The setpoint generation schemes are based on a voltage controlled operation mode (VCOM), a current controlled operation mode (CCOM) or an optimized current controlled operation mode (OCCOM). These three modes consider only continuous operation of the DABs without taking non-switching

DABs in intermittent mode into account. However, the overall power losses can be further reduced by implementing an intermittent operation mode of the DAB, as suggested in [18].

B. Voltage Controlled Operation Mode (VCOM)

With the VCOM, the DABs maintain a fixed voltage across the DC link capacitors, meaning $\bar{i}_{\mathrm{t},k} \approx i_{\mathrm{mod},k}$, providing the advantage of negligible voltage ripple of the module voltage $U_{\mathrm{mod},k}$. This is achieved with precise feedforward control of the estimated output power and a linearization of the transfer characteristic of the DAB [19]–[21]. However, this mode also suffers from certain drawbacks, including the requirement for highly dynamic voltage control and the presence of a ripple in the instantaneous power transmitted by the DABs. The VCOM ensures that only the minimum required number of DABs are active and transmitting power simultaneously. The number of active modules is determined by the ratio of the current phase voltage u_{AC} to the average module voltage $\overline{U}_{\mathrm{mod}}$ of this phase. The absolute value of the integer part of this ratio $|n_{\mathrm{fix}}|$, calculated with (2), corresponds to the number of modules conducting the full phase current $i_{\mathrm{mod},l} = \mathrm{sign}\,(u_{\mathrm{AC}}) \cdot i_{\mathrm{AC}}$ with $l \in \{0, ..., |n_{\mathrm{fix}}|\}$. The function 'trunc' is a truncation which means rounding to the next integer in the direction of zero. One further module with index $d = |n_{\mathrm{fix}}| + 1$ provides the residual voltage and therefore conducts the fractional part $i_{\mathrm{mod},d} = a_{\mathrm{dc}} \cdot i_{\mathrm{AC}}$, with a_{dc} calculated with (3). All other modules $r \in \{d+1, ..., m_{\mathrm{ph}}\}$ remain in idle mode, i.e. $i_{\mathrm{mod},r} = 0\,\mathrm{A}$ since their CHB cell is in bypass state. Therefore, (4) defines the resulting setpoint vector $\bar{\boldsymbol{i}}^{*}_{\mathbf{t,cv}}$ for operation in constant voltage mode (cv).

$$n_{\mathrm{fix}}(u_{\mathrm{AC}}) = \mathrm{trunc}\left(\frac{u_{\mathrm{AC}}}{\overline{U}_{\mathrm{mod}}}\right) \tag{2}$$

$$a_{\mathrm{dc}}(u_{\mathrm{AC}}) = \frac{u_{\mathrm{AC}}}{\overline{U}_{\mathrm{mod}}} - n_{\mathrm{fix}}(u_{\mathrm{AC}}) \tag{3}$$

$$\bar{\boldsymbol{i}}^{*}_{\mathbf{t,cv}} = \mathrm{sign}\,(u_{\mathrm{AC}})\,(\underbrace{i_{\mathrm{AC}}, ..., i_{\mathrm{AC}}}_{|l| \text{ entries}}, \underbrace{a_{\mathrm{dc}} i_{\mathrm{AC}}}_{1 \text{ entry}}, \underbrace{0\,\mathrm{A}, ..., 0\,\mathrm{A}}_{|r| \text{ entries}})^{T} \tag{4}$$

C. Current Controlled Operation Modes (CCOM)

Using CCOM, the DABs of each phase receive their setpoints $\bar{\boldsymbol{i}}^{*}_{\mathbf{t,ip}}$ based on the instantaneous power (ip) p_{AC} of the respective phase, as defined in (5), where $\mathbb{1}_{\mathrm{m_{ph}}}$ denotes a vector of ones with m_{ph} rows. As a consequence, each module within the same phase always delivers the same amount of power. With CCOM the setpoint vector for the transmitted currents $\bar{\boldsymbol{i}}^{*}_{\mathbf{t,ip}}$ depends not only on the phase current i_{AC} but also on the phase voltage u_{AC}.

$$\bar{\boldsymbol{i}}^{*}_{\mathbf{t,ip}} = \frac{p_{\mathrm{AC}}}{\overline{U}_{\mathrm{mod}} \cdot m_{\mathrm{ph}}} \cdot \mathbb{1}_{\mathrm{m_{ph}}} = \frac{u_{\mathrm{AC}} \cdot i_{\mathrm{AC}}}{\overline{U}_{\mathrm{mod}} \cdot m_{\mathrm{ph}}} \cdot \mathbb{1}_{\mathrm{m_{ph}}} \tag{5}$$

Instantaneous power control allows simple and straightforward setpoint calculation but requires buffering the 100 Hz AC power ripple in the DC link capacitors, resulting in a significant amount of stored energy. Voltage balancing of these capacitors must be managed by the AC voltage modulator, since the transmitted power is not equal to the power delivered to the grid, i.e., $\bar{i}^{*}_{\mathrm{t},k} \neq i_{\mathrm{mod},k}$. This increases the system's control complexity, requiring a full sorting algorithm and potentially causing frequent reordering of switching events in the CHB stage.

Another mode that considers active power (ap) for setpoint calculation is CCOM-AP. In this mode, all DABs across the three phases of the SST are assigned the same current setpoint $\bar{\boldsymbol{i}}^{*}_{\mathbf{t,ap}}$, which is derived from the active power transfer between the DC and AC grids, $P_{\mathrm{DC}} = P_{\mathrm{AC}}$, and calculated according to (6).

$$\begin{aligned}\bar{\boldsymbol{i}}^{*}_{\mathbf{t,ap}} &= \frac{P_{\mathrm{AC}}}{\overline{U}_{\mathrm{mod}} \cdot 3m_{\mathrm{ph}}} \cdot \mathbb{1}_{\mathrm{m_{ph}}} \\ &= \frac{\sqrt{3} \cdot U_{\mathrm{AC}} \cdot I_{\mathrm{AC}} \cdot \cos(\varphi)}{\overline{U}_{\mathrm{mod}} \cdot 3m_{\mathrm{ph}}} \cdot \mathbb{1}_{\mathrm{m_{ph}}}\end{aligned} \tag{6}$$

The only advantage of CCOM-AP is its simplified setpoint calculation. However, it inherits all disadvantages of CCOM and additionally increases the power ripple in the DC link capacitors. Therefore, it is not considered further.

D. Optimized Current Controlled Operation Mode (OCCOM)

The OCCOM aims to minimize the overall power losses P_{losses} of the DABs of an SST phase, by calculating the optimal setpoint distribution $\bar{\boldsymbol{i}}^{*}_{\mathbf{t,op}}$ in real time. This requires solving (7) with respect to (8) and (9) for each modulation step to ensure stable operation. The primary advantage of this approach lies in its guaranty to achieve the lowest possible overall DAB losses, thereby improving the system's efficiency. However, this mode introduces several challenges, including the complexity of real-time optimization, the tendency for increased voltage ripple in the DC link capacitors, since $\bar{i}_{\mathrm{t},k} \neq i_{\mathrm{mod},k}$, and circulating power between the DABs on the DC side. Furthermore, voltage balancing must be managed by the AC voltage modulator. Hence, as with the CCOM, a voltage sorting algorithm is required, and frequent switching events in the CHB stage may be necessary, potentially resulting in higher switching losses.

$$\bar{\boldsymbol{i}}^{*}_{\mathbf{t,op}} = \arg\min\left(P_{\mathrm{losses}}\left(\bar{\boldsymbol{i}}^{*}_{\mathbf{t}}\right)\right) \tag{7}$$

$$p_{\mathrm{AC}} = \sum_{k} \overline{U}_{\mathrm{mod}} \cdot \bar{i}^{*}_{\mathrm{t},k} \tag{8}$$

$$|\bar{i}^{*}_{\mathrm{t},k}| \leq |i_{\mathrm{AC}}| \tag{9}$$

IV. System Setup

To provide practical examples of the theory outlined in section III, this chapter details the hardware implementation of the Power Electronic Building Block (PEBB) and the software configuration of the SST.

A. Hardware of PEBB

Fig. 3 illustrates two PEBBs of the SST. Constructing a complete, full-scale MV SST with several megawatts of power is both expensive and space-intensive. Consequently, only the DAB stage and the control system of the modules have been physically implemented. The CHB cell is not

Fig. 3: Two 450 kW DABs configured in a back-to-back (B2B) setup.

TABLE II
Parameters of the MV DAB referred to the primary side

Parameter	Symbol	Value
Nominal output power	P_{nom}	450 kW
Primary voltage	U_{p}	720 V
Maximum module voltage	$U_{\mathrm{mod,max}}$	2000 V
Maximum module output current	$i_{\mathrm{mod,max}}$	±250 A
DAB switching and control frequency	$f_{\mathrm{sw}} = f_{\mathrm{con}}$	15 kHz
Transformer winding ratio	n_{t}	1 : 2.5
Leakage inductance	L_{σ}	1.44 µH
Magnetizing inductance	L_{h}	600 µH

TABLE III
Setup for the SST calculation

Parameter	Symbol	Value
Modules per phase	m_{ph}	11
Module (secondary) voltage	U_{mod}	1800 V
CHB switching frequency	f_{CHB}	15 kHz
Maximum phase current	$\hat{i}_{\mathrm{AC}}$	±250 A
Nominal power of SST	P_{SST}	6.1 MW
AC grid voltage	U_{N}	20 kV
Grid frequency	f_{grid}	50 Hz

included, as the knowledge gained from its integration is marginal relative to the associated costs of four additional MV semiconductors. Therefore, the losses of the full-scale SST are extrapolated using experimental data obtained from these PEBBs. This extrapolation method seems to be valid as shown in [15]. Each PEBB is housed in a single cabinet, containing the power stage, the medium-frequency transformer (MFT), measurement and control electronics, and auxiliary devices.

1) Power stage: Each full bridge consists of two Silicon Carbide (SiC) half-bridge modules by *MITSUBISHI ELECTRIC*. For the LV side 1200 V/1200 A modules are utilized [22], while 3300 V/750 A modules are used for the MV side [23]. The switching frequency is set to $f_{\mathrm{sw}} = 15\,\mathrm{kHz}$, providing a balance between controllability, power density, switching losses, and a limitation of parasitic effects.

2) Transformer: The medium-frequency transformer serves as the electromagnetic coupling component of the DAB. It features a winding ratio of $n_{\mathrm{t}} = 1 : 2.5$ and is manufactured by *Schmidbauer Transformatoren- und Gerätebau GmbH*. The leakage inductance of the transformer, including the connection wires to the semiconductors, is approximately $L_{\sigma} \approx 1.44\,\mu\mathrm{H}$, while the magnetizing inductance is $L_{\mathrm{h}} \approx 600\,\mu\mathrm{H}$. Both values refer to the primary side.

3) Control and auxiliary System: The DAB is managed by a modular signal processing platform, the ETI-System-on-Chip System (SoC-System), which combines two ARM-core processors and an field-programmable gate array (FPGA) operating at a clock frequency of $f_{\mathrm{FPGA}} = 150\,\mathrm{MHz}$. The control frequency of the DAB is set to $f_{\mathrm{con}} = 15\,\mathrm{kHz}$. A detailed description of the ETI-SoC-System system is provided in [24].

4) Setup and Summary of test bench: Both DABs are connected in a B2B setup. While one DAB, the Voltage Controlled DAB (VC-DAB), controls the LV side voltage U_{p}, the Current Controlled DAB (CC-DAB) controls the rectified transformer current on the MV side $\bar{i}_{\mathrm{t}}$ and, consequently, the transmitted power $P_{\mathrm{mod}} = \bar{i}_{\mathrm{t}} \cdot U_{\mathrm{mod}}$. The voltage controller of the VC-DAB is a combination of an operation point-dependent feedforward controller and a PI-controller, as described in [25]. The MV DC link voltage U_{mod} is stabilized by a 120 kW power supply which provides the power losses of the system. A Gen7tA power meter from *HBK - Hottinger Brüel & Kjaer GmbH* is used to measure the quasi-stationary input and output currents and voltages. This enables precise calculation of losses and efficiency for each DAB. Table II summarizes the most relevant data of the DABs.

B. SST calculation setup

The calculation results presented in section V are generated by using the system summarized in table III. To have one redundant module in each SST phase for a MV grid with nominal voltage of $U_{\mathrm{N}} = 20\,\mathrm{kV}$ according to the Technical Connection Rules Medium Voltage VDE-AR-N 4110 (TCR Medium Voltage) standard, a total number of $m_{\mathrm{ph}} = 11$ modules are implemented. The resulting nominal power of the SST is about $P_{\mathrm{SST}} = 6.1\,\mathrm{MW}$.

V. Results

First, the experimental results of the DAB are presented. Based on these results, a phase loss model of the SST is derived to determine the losses of all DABs of this phase as a function of the presented OMs. The calculated results using OCCOM are obtained in Matlab with the `fmincon` function and the interior-point algorithm.

A. Experimental results

Fig. 4 presents the measured power losses $P_{\mathrm{losses,DAB,meas}}$ at OPs with a primary voltage of $U_{\mathrm{p}} = 720\,\mathrm{V}$ and a module voltage of $U_{\mathrm{mod}} = 1800\,\mathrm{V}$, represented by black circles. The results indicate an asymmetry between positive and negative module currents $\bar{i}_{\mathrm{t}} = i_{\mathrm{mod}}$. The fifth-order polynomial fits for positive and negative currents are highlighted in blue and green, respectively. As expected, the power losses of the DAB increase approximately quadratically with higher absolute transmitted currents $\left|\bar{i}_{\mathrm{t}}\right| > 100\,\mathrm{A}$. This behavior is primarily

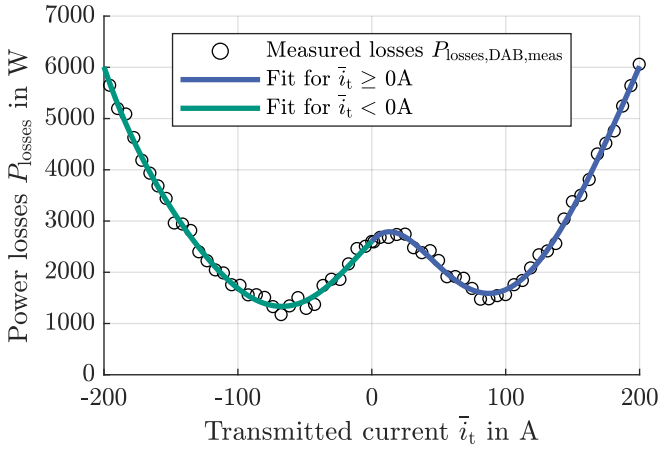


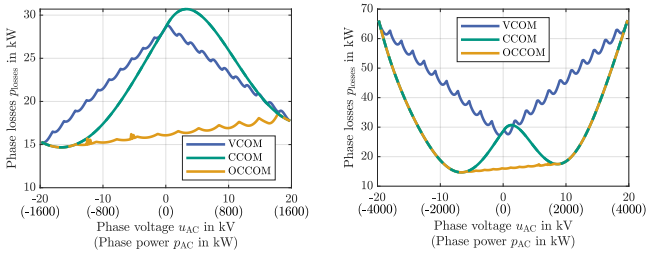
Fig. 4: Measured and fitted power losses of a DAB with $U_{\text{p}} = 720\,\text{V}$ and $U_{\text{mod}} = 1800\,\text{V}$.

due to ohmic losses of the semiconductors, the litz wires and the transformer. Counterintuitively, the losses at $\bar{i}_{\text{t}} \approx 0\,\text{A}$ are significantly higher compared to the two local minima at $\bar{i}_{\text{t}} \approx -65\,\text{A}$ and $\bar{i}_{\text{t}} \approx 90\,\text{A}$. This phenomenon is attributed to the absence of zero voltage switching (ZVS) of the MOSFETs, which is not inherently guaranteed at low switching currents and is only achieved beyond the aforementioned current levels. Due to the significant influence of commutation effects at low switching currents [26], combined with almost constant transformer core losses, the power losses at low module currents $\bar{i}_{\text{t}} \approx 0\,\text{A}$ exhibit a local maximum. The asymmetry between positive and negative currents, however, is caused by the differing semiconductor and gate driver characteristics on the primary (LV) and secondary (MV) sides.

B. Calculation results

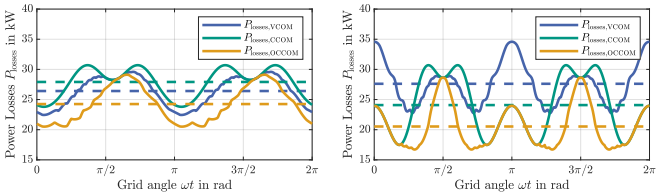
In Fig. 5, two representative phase loss characteristics as a function of the phase voltage u_{AC}, and thus different instantaneous phase powers p_{AC}, are shown for the three investigated OMs. The results are presented for two fixed phase currents: $i_{\text{AC}} = 80\,\text{A}$ in Fig. 5a and $i_{\text{AC}} = 200\,\text{A}$ in Fig. 5b. The comparison of VCOM and CCOM shows that the preferable OM depends on the phase voltage u_{AC} and the phase current i_{AC}. In general, it also depends on the shape of the power loss characteristic of the DAB itself. However, the OCCOM combines all advantages of both modes and allows unrestricted power distribution between modules. As a result, it always yields the lowest instantaneous power losses p_{losses}. For higher requested phase voltages, the optimal OP tends towards the solution for CCOM. For zero phase current $i_{\text{AC}} = 0\,\text{A}$ (which is not shown) or maximum phase voltage in either direction, positive or negative (c.f. $\pm 19.8\,\text{kV}$ of Fig. 5), no optimization is possible since all modules are at their limits. Thus, all OMs yield the same outcome.

To allow a comprehensive comparison of the instantaneous power losses during operation over a full grid period for each OM, Fig. 6 presents the calculated results. In both cases, the peak phase voltage is $\hat{u}_{\text{AC}} = \frac{\sqrt{2}\cdot 20\,\text{kV}}{\sqrt{3}} \approx 16.33\,\text{kV}$, while



(a) Phase current $i_{\text{AC}} = 80\,\text{A}$. **(b)** Phase current $i_{\text{AC}} = 200\,\text{A}$

Fig. 5: Power losses P_{losses} of a single phase for different OMs and phase currents i_{AC} in dependence of the phase voltage u_{AC} or phase power p_{AC}.



(a) $\hat{i}_{\text{AC}} = 60\,\text{A}$, $\cos(\varphi) = 0.95$, $\overline{P}_{\text{losses,VCOM}} \approx 26.4\,\text{kW}$, $\overline{P}_{\text{losses,CCOM}} \approx 27.9\,\text{kW}$, $\overline{P}_{\text{losses,OCCOM}} \approx 24.3\,\text{kW}$

(b) $\hat{i}_{\text{AC}} = 150\,\text{A}$, $\cos(\varphi) = 1$, $\overline{P}_{\text{losses,VCOM}} \approx 27.6\,\text{kW}$, $\overline{P}_{\text{losses,CCOM}} \approx 24.1\,\text{kW}$, $\overline{P}_{\text{losses,OCCOM}} \approx 20.5\,\text{kW}$

Fig. 6: Single phase power loss P_{losses} comparison for different OMs during a grid period. The peak voltage of both is $\hat{u}_{\text{AC}} = 16.33\,\text{kV}$. The dashed lines are the corresponding average power losses of each OM.

the peak current and the power factor are set to $\hat{i}_{\text{AC}} = 60\,\text{A}$, $\cos(\varphi) = 0.95$ in Fig. 6a and $\hat{i}_{\text{AC}} = 150\,\text{A}$, $\cos(\varphi) = 1$ in Fig. 6b, respectively.

Since the optimization goal of the OCCOM is to minimize power losses, it consistently achieves both the lowest instantaneous and therefore, the lowest average power losses $\overline{P}_{\text{losses,OCCOM}}$. However, due to the complexity of the OCCOM optimization problem, it is easier to implement either CCOM or VCOM. The two examples presented in Fig. 6a and Fig. 6b illustrate that the preferable choice between these two modes depends on the specific OP of the SST. As a general guideline, if real-time optimization using OCCOM is not feasible, CCOM tends to outperform VCOM when the phase currents exceed the threshold required for achieving ZVS in the DABs (here: $\left|\hat{i}_{\text{AC}}\right| > 100\,\text{A}$). Conversely, when the AC peak current $\hat{i}_{\text{AC}}$ is lower, VCOM becomes the more efficient choice. On top of that, combinations and further modifications of the OMs are also possible. Beyond power loss reduction, other advantages and disadvantages discussed in Section III must also be considered when selecting the appropriate OM. If chosen correctly, loss reductions of approximately $10\,\%$ to $20\,\%$ can be achieved with the investigated OMs.

VI. Conclusion

This paper investigates various OMs for modular SSTs based on DABs, aiming to reduce power losses and thus increasing efficiency. Three basic OMs, VCOM, CCOM, and OCCOM, are analyzed and compared regarding their impact on total SST phase losses, with a particular focus on the

trade-off between power loss reduction and control complexity. Starting from the measured losses of a single DAB, a phase loss model for the SST is developed, allowing for the evaluation of the power losses under various operating conditions. The results show that while OCCOM achieves the lowest power losses, it requires complex real-time optimization. When this is not feasible, the choice between VCOM and CCOM depends on the phase current: CCOM is preferable for currents exceeding the ZVS threshold of the DAB, whereas VCOM performs better at lower currents. Overall, a proper selection of the OM can reduce power losses by up to $20\,\%$, highlighting the potential for improved SST operation modes through advanced control strategies. Future research should further explore the impact of these OMs on capacitor design, thermal management, and CHB switching losses.

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