Converter-Based Fault Interruption: A Pathway to Effective DC Protection

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***Abstract*—The interruption of DC faults remains a major obstacle to the widespread deployment of DC grid technologies. The rapid rise of fault currents and the absence of natural current zero-crossing points in DC systems have limited the performance and cost-effectiveness of conventional protection strategies, especially when compared to their AC counterparts. This has led to a growing interest in rethinking traditional protection paradigms, particularly the dependence on dedicated circuit-breaking devices. This paper investigates the feasibility of converter-integrated or breaker-less protection approaches for basic DC-DC converter topologies. By introducing structural modifications, specifically the integration of additional switching components, these converters are adapted to autonomously detect and clear faults on the grid side. Although these modifications may not directly improve efficiency or reduce cost, they can significantly enhance fault response time and the practicality of integrated protection schemes. The study begins with an analysis of conventional DC-DC converter behavior under pole-to-pole short-circuit conditions, followed by simulation-based validation of the proposed modifications. Results demonstrate that the modified converters can effectively interrupt fault currents, highlighting the potential of power electronic converters to serve dual roles in both energy conversion and system protection.**

Keywords—breaker-less, converter-based, DC microgrid, protection, short-circuit

I. Introduction

The rapid proliferation of renewable DC energy sources, storage, and DC loads including electric vehicles, and data centers has revitalized interest in DC grids. DC grids are capable of achieving higher efficiency compared to AC networks due to fewer conversion stages and lower effective resistance. Moreover, the absence of reactive power in DC systems diminishes the size of conductors and the volume of copper required to transmit a specific amount of active power, thereby enhancing the sustainability of future power grids [1]-[2]. This is particularly beneficial for microgrids, where solar DC generation is typically proximate to consumption, making DC grids a preferable choice over AC microgrids.

While DC power systems offer numerous operational and efficiency advantages, the protection of such systems remains a significant technical challenge. One of the primary concerns is the rapid rate of fault current rise, which can reach up to 1000 A/µs depending on the fault location and its proximity to voltage sources or power electronic converters. This high di/dt necessitates the integration of inductive fault current limiters (FCLs) in many DC circuit breaker designs [3]. Although these inductive elements do not introduce substantial voltage drops, they considerably increase the overall mass of the breaker and adversely affect the dynamic response of the network. In scenarios where the addition of inductance is impractical or undesirable, manufacturers are often forced to design breakers with interruption capabilities significantly exceeding the system's nominal current [4]. For example, solid-state circuit breakers may require semiconductor devices rated for multiple times the nominal current to ensure reliable operation under fault conditions.

An alternative mitigation strategy involves minimizing the fault detection and interruption time. In certain cases, the fault detection latency surpasses the actual isolation time. By reducing the detection time, the peak amplitude of the fault current can be significantly limited, thereby reducing the stress on the breaker and potentially eliminating the need for bulky fault limiting components.

Fault detection methodologies in DC systems can generally be categorized in two distinct ways based on their underlying objectives [5]. The first categorization is based on the signal processing techniques employed for fault analysis, which may involve the use of instantaneous signal values or the application of transformation methods such as the Fourier or wavelet transforms. These processed signals are then analyzed using either conventional computational algorithms or advanced artificial intelligence (AI) techniques to support decision-making. The second categorization pertains to the type of fault indicator utilized. The majority of existing studies rely exclusively on three primary indicators: the fault current, the time derivative of the fault current, and the voltage drop across the DC bus. However, with the development of novel protection system configurations, there is growing interest in identifying alternative fault indicators that can provide faster and more sensitive responses to fault events, potentially enhancing the overall responsiveness of DC protection schemes.

One novel protection configuration involves leveraging power electronic converters to isolate faults on the power grid side. The core idea stems from the fact that these converters inherently contain switching elements, which, in principle, should be capable of interrupting the faults and isolating the

output side from the input. However, as will be discussed later, this assumption is often overly optimistic, as many commonly used converter topologies are highly vulnerable to faults occurring on the network side. Nevertheless, if power electronic converters can be modified to assume a protective role, several advantages may be realized. First, if fault isolation is performed within the converter, it becomes possible to define new fault indicators internal to the converter. For example, the current through the input or output DC-link capacitors may exhibit a faster response to fault events. Second, the converter's existing measurement signals, originally intended for monitoring or control, can be repurposed for fault detection. Furthermore, if the converter's semiconductor switches are used for fault interruption, existing protection mechanisms such as DESAT protection can be extended to contribute to network-level fault protection. Third, many researchers envision power electronic converters as enablers of distributed intelligence in future energy networks. These converters are often equipped with communication capabilities for power-sharing applications. If they can independently detect and interrupt faults, they could facilitate the implementation of more advanced protection schemes, such as differential protection.

The primary objective of this study is then to modify fundamental DC-DC converter topologies, specifically buck, boost, and buck-boost converters, such that they are capable of detecting and clearing power system faults occurring at either their input or output terminals. To achieve this, the first step involves analyzing the impact of grid-side faults on the converter, including the fault propagation stages and their respective effects on both the converter and the DC grid. Subsequently, the study explores the integration of additional semiconductor devices into the converter architecture to enable fault interruption at all stages of fault development. It is important to note that the proposed modified converter structures are not necessarily optimized for efficiency or cost. Rather, the focus is on evaluating the feasibility of combining protection functionality with energy conversion within power electronic converters.

The remainder of this paper is organized as follows. Section II presents an analysis of short-circuit faults occurring at the output side of DC-DC converters. Section III introduces the proposed modifications applied to the buck, boost, and buck-boost converter topologies to enable fault detection and interruption capabilities. Section IV discusses the simulation results and provides a detailed evaluation of the modified converters performance under fault conditions. Finally, Section V concludes the paper by summarizing the key findings and outlining potential directions for future research.

II. Short-circuit Fault Analysis

Most DC-DC converters, both isolated and non-isolated, are based on three fundamental topologies: buck, boost, and buck-boost (Fig. 1). These converters have similar structures, where the position of an inductor changes between two semiconductor devices and the converter's input and output. Two capacitors are also typically employed at both the input and output terminals of the converter, which initiate the main complexity of DC protection. In the following, the progression of a pole-to-pole fault on the output side of the three basic DC-DC converters through three distinct stages has been analyzed [6]:

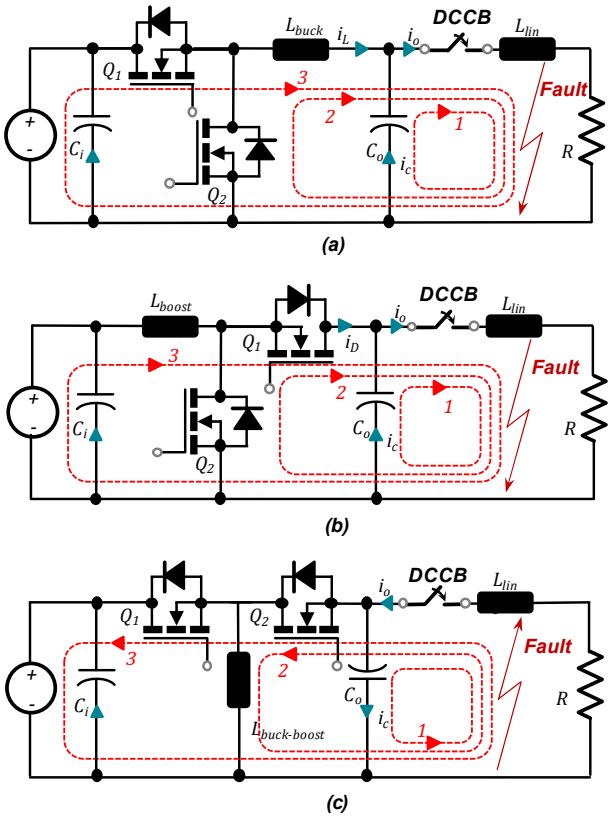

Fig. 1. Short-circuit fault path through a) buck, b) boost, and c) buck-boost converters.

1) DC-link Capacitor Discharge Stage

At the initial moment following the fault occurrence, in all three topologies, the output DC-link capacitor discharges through the fault inductor and resistance, forming an RLC circuit, as illustrated in Fig. 1 (a, b, and c) path 1. This results in a rapid increase in the line current. Neglecting the capacitor's equivalent series resistance, the loop voltage equation can be expressed as (1).

$$L_f C \frac{d^2 V_c}{dt^2} + R_f C \frac{dV_c}{dt} + V_c = 0 \tag{1}$$

L_f, R_f, and V_c are the fault loop inductance, and resistance and capacitor voltage respectively. Consequently, the capacitor voltage and fault current can be calculated as follows:

$$V_c = e^{-\alpha t}\left(V_{c0}\frac{\omega}{\omega_d}\sin(\omega_d t + \beta) - \frac{I_{f0}}{\omega_d C}\sin(\omega_d t)\right) \tag{2}$$

$$I_f = -C\frac{dV_c}{dt} = e^{-\alpha t}\left(-I_{f0}\frac{\omega}{\omega_d}\sin(\omega_d t - \beta) + \frac{V_{c0}}{\omega_d L_f}\sin(\omega_d t)\right) \tag{3}$$

Where $\alpha = \frac{R_f}{2L_f}$, $\omega_d^2 = \frac{1}{L_f C} - \alpha^2$, $\omega^2 = \omega_d^2 + \alpha^2$, and $\beta = tg^{-1}\left(\frac{\omega_d}{\alpha}\right)$, and V_{c0} and I_{f0} are the capacitor initial voltage and

line initial current when fault happens. This stage is the primary cause of the drastic escalation of fault current, which can be mitigated by increasing the line inductance using an FCL.

2) Freewheeling Diodes Conduction Stage

The capacitor discharge stage in a boost converter concludes when the capacitor voltage reaches zero. In buck or buck-boost converters, the first stage persists until the fault inductor current equals the converter inductor current. Following this moment, the fault current continues to flow through the free-wheeling diodes, forming an RL circuit as illustrated in Fig. 1 (a, b, and c) path 2. Assuming this stage starts at t_1 and the initial value of fault current in this stage is $I_{f,t1}$, fault current in this stage can be expressed as:

$$I_f = I_{f,t1} e^{-\frac{R_f}{L_f}(t-t_1)} \quad (4)$$

For the boost topology, L_D is equal to the fault inductance. However, in buck and buck-boost converters, L_D is the sum of the converter inductor inductance and the fault inductance.

3) Source Current Feeding Stage

In buck and boost converters, if an appropriate circuit breaker is not implemented or the converter switch cannot interrupt the fault, the fault current may escalate depending on the fault resistance and the DC source's capacity to supply current. This escalation could potentially occur even before the second stage. During this stage, the fault current increases to its final value, and the DC source continues to supply the fault (Fig. 1 (a, and b) path 3) until the circuit breaker intervenes. However, in buck-boost converters, since the output has a different polarity compared to the DC supply, this stage may never occur. However, if it does happen, it will diminish the fault current.

The analysis of fault behavior shows that the sharp rise in fault current is mainly caused by the fast discharge of the DC-link capacitor. This discharge happens much more quickly than the other two fault stages. Therefore, placing a fast current interruption device in series with the DC-link capacitor could help stop the first two stages from fully developing. In addition, modifying or rearranging the converter's semiconductor devices could allow the converter to interrupt the remaining stages of the fault current on its own.

III. Proposed Modification for Basic DC-DC Topologies

The core concept of the breaker-less or converter-based approach entails substituting the primary circuit breakers, which are conventionally installed in series with transmission line feeders, with alternative switching devices that possess equivalent fault interruption capabilities. As depicted in Fig. 2 and grounded in fundamental electrical circuit theory, the traditional circuit breaker in series with the transmission line can be replaced by two switching devices situated in separate branches that converge at a common node.

Based on this concept, a dedicated circuit breaker can be employed specifically to interrupt the capacitor discharge current. Additionally, by modifying the converter structure or incorporating new semiconductor devices, it is possible to interrupt fault currents in the second and third stages. It is important to note that faults in the first and second stages are inevitable due to fault detection delays. Regardless of how quickly the capacitor discharge current is interrupted, the delay in fault detection and the reaction time of the capacitor breaker will result in the line inductor becoming energized.

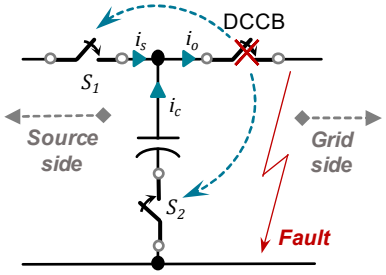

Fig. 2. Breaker-less or converter-based fault interruption main concept

The objective of the proposed modification is to redesign the topologies in a way that enables isolation of faults occurring on both the input and output sides, thereby preventing damage to the converter. This modification is made under the assumption that the converters are bidirectional and equipped with filter capacitors at both the input and output terminals.

A. Modification for Buck Topology

As illustrated in Fig. 1(a), if a fault occurs on either the input or output side, the corresponding input or output capacitor will immediately discharge through the fault resistance in the first stage. In the case of an output-side fault, the fault current in the second stage flows through the anti-parallel diode of switch Q_2 and the buck inductor. Conversely, if the fault occurs on the input side, the current path is formed through the anti-parallel diodes of both switches Q_2 and Q_1.

To interrupt the fault current passing through the anti-parallel diode of Q_2, it is necessary to place an additional switch in anti-series configuration with Q_2. If the buck converter is unidirectional, adding only an output capacitor breaker and the anti-series switch with Q_2 is sufficient to clear the fault, as switch Q_1 can interrupt the fault current in the third stage and isolate the output from the input.

However, for bidirectional fault interruption, an additional switch must be placed in series with Q_1 but oriented in the opposite direction to block the reverse current path from the secondary to the primary side. It is worth noting that the switching speed of these devices can be adjusted based on the time constant of each stage. For instance, the switch added to interrupt the third-stage fault can operate more slowly than the capacitor breaker.

An alternative configuration involves placing a switch in series with the buck inductor instead of in series with Q_2. However, since the inductor carries a higher effective current than the Q_2 branch, this approach results in greater power losses. Therefore, the initial proposed configuration, adding two anti-series switches with Q_2 and Q_1, along with two breakers for the capacitors, offers the most effective solution for enabling the buck converter to interrupt faults on both the input and output sides. The proposed modified Buck configuration is shown in Fig. 3(a).

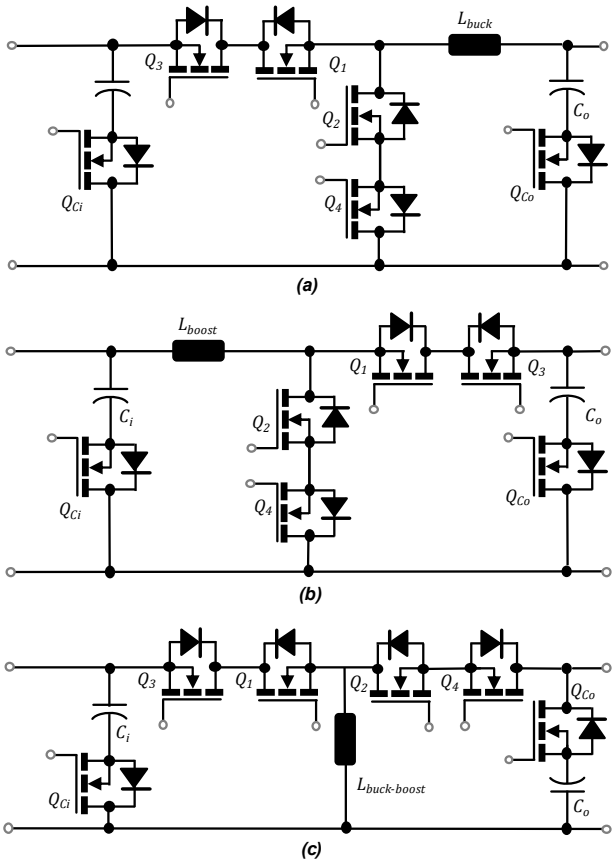

Fig. 3. Modified topologies of a) buck, b) boost, and c) buck-boost converters for autonomous fault interruption.

B. Modification for Boost Topology

As shown in Fig. 1(b), if a fault occurs on the output side, the fault current flows through the anti-parallel diodes of switches Q_2 and Q_1. If the fault occurs on the input side, the fault current in the second stage flows through the anti-parallel diode of switch Q_2 and the boost inductor. Bidirectional buck and boost converters exhibit similar behavior when facing faults on either the input or output side.

The proposed fault-tolerant structure for the bidirectional boost converter involves modifications analogous to those applied to the buck converter. Specifically, two anti-series switches should be added in series with switches Q_2 and Q_1, along with two breakers for the input and output capacitors. In the unidirectional configuration, it is sufficient to include one breaker for the output capacitor and another breaker connected in anti-series with Q_1 to block the fault current in the second and third stages.

C. Modification for Buck-boost Topology

In the buck-boost topology (Fig. 1(c)), if a fault occurs at either the input or output, the anti-parallel diodes of switches Q_1 and Q_2 may conduct in the second stage and become susceptible to damage. However, due to the inherent polarity inversion between the input and output in this topology, the fault current magnitude in the third stage is naturally reduced. Consequently, although the converter switches are capable of interrupting faults on both the input and output sides during the third stage, to prevent damage to the anti-parallel diodes, it is necessary to add two anti-series switches in parallel with Q_2 and Q_1.

It is important to note that these modifications are based on the assumption that the capacitor breaker may have a relatively long reaction time and that the overcurrent tolerance of the anti-parallel diodes conducting in the second stage is very limited. Nevertheless, diodes typically exhibit a significant capability to withstand pulsed currents. Therefore, if the capacitor breaker operates rapidly and prevents the line inductor from charging quickly, the need for the additional fault-blocking switches for the second stage may be eliminated altogether.

IV. Simulation Results and Discussion

In this section, the fault interruption performance of the modified topologies is evaluated through simulation. For all three topologies, a short-circuit fault is introduced on the secondary side of the converter to analyze the fault current path through the semiconductors and assess the system's fault-clearing capability. The simulations were conducted using MATLAB-Simulink.

To ensure realistic modeling, fault detection delay and fault signal transmission time are also considered. Specifically, in all simulations, the capacitor breaker delay is modeled using a realistic driver model. For the main converter semiconductors, a longer delay of 10 microseconds is applied. Although significantly shorter reaction times are technically achievable, a 10-microsecond delay is assumed as the maximum fault detection time in an electronic fault detection system, accounting for potential complexities in real-world fault identification. The detailed specifications of the three simulated models, as well as the characteristics of the applied fault, are presented in Table I.

TABLE I. SPECIFICATIONS OF THE SIMULATED TOPOLOGIES AND FAULT

Specification	Value
Buck Topology	
Input voltage	380V
Output voltage -power	220V -1kW
Switching Frequency	100kHz
Buck inductor inductance -resistance	620µH -5mΩ
Output capacitors capacitance	47µF
Snubbers	RCD -1mF & 40Ω
Reaction delay of converter switches	10µs
Boost Topology	
Input voltage	220V
Output voltage -power	380V -2kW
Switching Frequency	20kHz
Boost inductor inductance -resistance	1.7mH -10mΩ
Output capacitors capacitance	33µF
Snubbers	RCD -1mF & 40Ω
Reaction delay of converter switches	10µs
Buck-boost Topology	
Input voltage	380V
Output voltage -power	220V -1kW
Switching Frequency	100kHz
Inductor inductance -resistance	1.1mH -7mΩ
Output capacitors capacitance	33µF
Snubbers	RCD -1mF & 40Ω
Reaction delay of converter switches	10µs
Fault Specification	
Fault inductance -resistance	100µH -0.1Ω

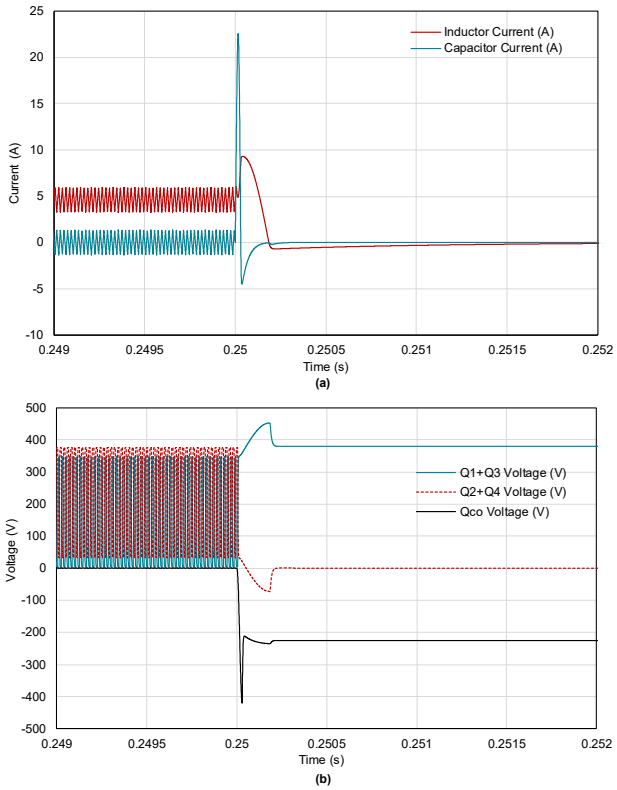

Fig. 4. Fault interruption capability of modified buck topology a) buck inductor and output capacitor currents, b) semiconductors' voltages.

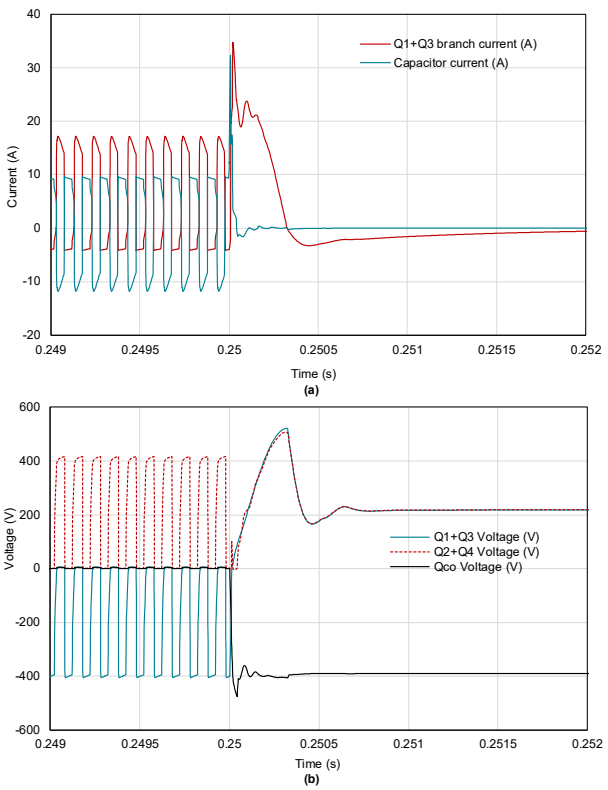

Fig. 5. Fault interruption capability of modified boost topology a) $Q_1 + Q_3$ branch and output capacitor currents, b) semiconductors' voltages.

A. Modified Buck Topology

In evaluating the performance of the modified topologies in successfully interrupting fault current, two critical aspects must be considered. First, the increase in fault current resulting from capacitor discharge should not propagate to the main converter semiconductors. Second, the voltage stress across the semiconductors must remain within acceptable limits, ideally not exceeding twice the nominal voltage, when using reasonably sized snubber circuits.

In this part of the simulation study, the fault interruption performance of a modified buck converter, as shown in Fig. 3(a), is assessed under a secondary-side fault condition. All semiconductors in the simulation are equipped with an RCD snubber circuits, with specifications provided in Table I. While the use of these snubbers may prolong the fault current settling time due to oscillations with the line inductance, hybrid snubber circuits incorporating metal-oxide varistors (MOVs) can also be employed to mitigate this effect.

Fault detection in the proposed system is performed by monitoring the capacitor current. Due to its inherently AC nature, the capacitor current exhibits the fastest response to fault events. This rapid detection capability reduces the peak current that must be interrupted, thereby minimizing the need for oversized semiconductor devices.

As illustrated in Fig. 4(a), a sharp increase in the capacitor branch current occurs immediately after the fault event at t = 0.25 s. This surge corresponds to the charging current of the snubber capacitor. The magnitude of this current is influenced by the type of snubber used; however, it is ultimately dissipated during the fault and does not propagate toward the converter semiconductors.

Fig. 4(b) presents the voltage profiles of the converter semiconductors and the snubber capacitor breaker. The results indicate that the peak voltage remains below twice the open-circuit voltage, confirming the proper operation of the snubber circuits. Nevertheless, further optimization using hybrid snubber structures, such as combinations of MOV and RCD networks, can yield significantly improved performance in both current limiting and voltage clamping.

B. Modified Boost Topology

Fig. 5 presents analogous signals for the boost converter topology. The specifications of the simulated boost converter are provided in Table I. Fault detection is again based on monitoring the capacitor current, similar to the previously discussed topology. In Fig. 5(a), the currents in the capacitor and $Q_1 + Q_3$ branches are shown. Although the sharp rise in the capacitor current may appear to be transferred to the converter semiconductors, it is important to note that the semiconductor current is interrupted very rapidly. The observed current spike in the figure primarily flows through the snubber circuits.

Fig. 5(b) demonstrates that the snubbers, designed according to the parameters listed in Table I, effectively limit the voltage overshoot across the semiconductor devices. This confirms the adequacy of the snubber design in protecting the converter components during fault conditions.

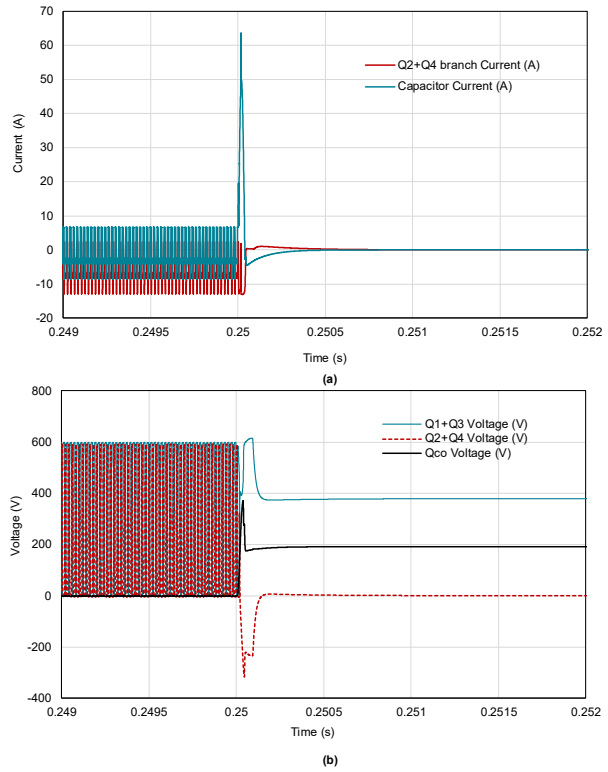

Fig. 6. Fault interruption capability of modified buck-boost topology a) $Q_2 + Q_4$ branch and output capacitor currents, b) semiconductors' voltages.

C. *Modified Buck-boost Topology*

Figure 6 presents similar signals for the buck-boost topology. The specifications of the simulated topology are also provided in Table I. As shown in Fig. 6(a), despite a significant current spike in the capacitor branch, there is almost no noticeable current increase in the adjacent branch containing the converter semiconductors. This observation suggests that, in a buck-boost converter, it may be possible to isolate a secondary-side fault simply just by incorporating a capacitor breaker.

Fig. 6(b) further demonstrates that, with snubbers designed according to the specifications listed in Table I, it is feasible to limit the voltage transients across the semiconductors to twice their off-state voltage. It is worth noting that RCD snubbers were employed for this purpose, as they are commonly used in switching applications. However, the use of hybrid-structured snubbers, at least for the capacitor breaker, could significantly reduce the current spike during fault events. This is because a substantial portion of the capacitor branch current during a fault is diverted to charge the snubber capacitor.

V. Conclusion

This study highlights the potential of utilizing power electronic converters for clearing short-circuit faults in DC networks. Although the analysis was limited to basic DC-DC converter topologies, the findings do not preclude the possibility of adapting other converter types for similar protective functions. It is acknowledged that implementing such adaptations may not yield favorable results for all converter types and could, in some cases, lead to significant cost increases. Nevertheless, certain topologies may exhibit unique characteristics that make them particularly well-suited for fault-clearing applications and thus merit further investigation. Overall, the preliminary results suggest that adapting power electronic converters for DC network protection is feasible, but additional research is required to identify and optimize the most effective topologies for this purpose.

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