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Direct observations of nucleation and early-stage growth of Au-catalyzed GaAs nanowires on Si(111)

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Abstract

Developing a reliable procedure for the growth of III–V nanowires (NW) on silicon (Si) substrates remains a significant challenge, as current methods rely on trial-and-error approaches with varying interpretations of critical process steps such as sample preparation, Au–Si alloy formation in the growth reactor, and NW alignment. Addressing these challenges is essential for enabling high-performance electronic and optoelectronic devices that combine the superior properties of III–V NW semiconductors with the well-established Si-based technology. Combining conventional scalable growth methods, such as metalorganic chemical vapor deposition (MOCVD) with *in situ* characterization using environmental transmission electron microscopy (ETEM-MOCVD) enables a deeper understanding of the growth dynamics, if that knowledge is transferable to the scalable processes. We report on successful epitaxial growth of Au-catalyzed GaAs NWs on Si(111) substrates using micro-electromechanical system chips with monocrystalline Si-cantilevers in both conventional MOCVD and ETEM-MOCVD systems. The conventional MOCVD provided a framework for initial parameter tuning, while ETEM-MOCVD offered valuable insights into early nucleation and catalyst-substrate interactions. Our findings show that nucleation is significantly influenced by the removal of native oxide layers and the initial formation of the Au–Si alloy. Our *in situ* studies revealed different NW-substrate interfaces, essential for optimizing the epitaxial growth process.

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We identified three typical configurations of NW 'roots', each impacted by growth conditions and preparation steps, affecting the structural and potentially the optical properties of the NWs. Similarly, doping from the Si-substrate may affect both optical and electrical properties; however, compositional analysis revealed no traces of Si in NWs post-nucleation and a small amount in the catalytic droplet. Our research highlights the importance of *in situ* studies for a comprehensive understanding of nucleation mechanisms, paving the way for optimizing III–V NW growth on Si substrates and developing high-performance III–V/Si devices.

Supplementary material for this article is available online

Keywords: GaAs nanowires, Si, ETEM, MOCVD, nucleation mechanisms

1. Introduction

The integration of III–V semiconductors on silicon (Si) substrates has been a long-standing research goal to leverage the direct band gaps and high electron mobilities of these materials within well-established Si-based technology. However, epitaxial growth of monolithic III–V semiconductor layers transferring the crystallographic orientations of the Si substrates faces fundamental challenges such as the mismatch in lattice constants [1], the difference in thermal expansion coefficients [2], and the polar crystal structure enabling the formation of antiphase boundaries (APBs) [3, 4]. Nanowire (NW) growth using nanoparticle-catalyzed vapor–liquid–solid (VLS) methods mitigates these issues in two ways: Firstly, by relieving the lattice stress at the surface of the NW sidewalls and, secondly, by minimizing the probability of APBs due to the small growth area. An additional material, typically gold (Au), can make up the catalyst droplet stabilizing the liquid phase of the subspecies for VLS-growth and increase the growth rate forming these NWs rather than thin films covering the substrate surface [5, 6]. Nonetheless, initiating growth of defect-free compound semiconductors requires carefully tuned growth parameters.

Different procedures to achieve successful growth of III–V semiconductors on Si have been reported using conventional standalone growth systems [1, 7–14]. Such procedures are typically developed through trial-and-error and extensive efforts have been made to interpret the importance of process steps retroactively. However, in the absence of direct observations of the nucleation and growth process, these interpretations vary significantly in understanding of the limiting steps, making it very difficult to transfer successful results between different growth systems. Studies have pointed to the importance of a proper sample preparation since the initial surface contamination, including residual oxides and carbon, has a significant impact on the NW growth direction and defect formation [7–10]. Other aspects are the formation of an Au–Si alloy and the nucleation process, as they affect interface roughness and NW alignment, which are crucial for the Si-to-III–V interface quality, which in turn is important for the electrical properties [10]. Finally, transition mechanisms from lateral traces to vertical NWs can potentially be influenced by the interface energies and growth conditions [2]. Understanding these transition mechanisms is essential, as defects formed during initial nucleation stages can impact the optical properties of the resulting NWs [8, 15, 16]. To date, no literature has provided direct observations of the early stages of III–V NW nucleation and growth on Si-substrates with respect to the suggested effect of the individual steps such as Au–Si alloy formation, precursor absorption, and NW alignment.

Recently, environmental transmission electron microscopes (ETEMs) have been used for direct observations of the early stages of single crystalline NW growth including Si [17, 18], GaN [19] and GaAs [20] on amorphous substrates, as well as homoepitaxial growth of Si NWs on monocrystalline Si [21]. These observations are crucial for understanding the supersaturation of the catalyst [18], initial formation of NW facets [19] and preferred growth direction [20]. NWs nucleated in the ETEM, or transferred from standalone growth chambers into the ETEM, can be analyzed to investigate later stages of development such as controlling and understanding the atomic step flow [22, 23], crystal phase formation [24–26] and droplet kinetics [27]. However, for a detailed understanding of the initial stages of heteroepitaxial nucleation and the dynamic processes involved, as well as to prevent contamination from transferring samples between growth chambers, it is essential to study NW growth *in situ* in its entirety.

In this study, we detail a procedure for initiating epitaxial growth of Au-catalyzed GaAs NWs on Si(111) using both a conventional growth chamber and an ETEM. We provide direct TEM observations of the nucleation process, focusing on sample preparation, the GaAs–Si NW-substrate integration and the resulting NW structure and composition. This paper is organized as follows: section 2 describes the preparation of the micro-electromechanical system (MEMS) chips with monocrystalline Si-cantilevers, used as a substrate in both the standalone metalorganic chemical vapor deposition (MOCVD) chamber, and the ETEM with an integrated MOCVD system (ETEM-MOCVD). Section 3 presents the growth procedures and environments for both growth systems and discusses the results of the procedures. While the ETEM-MOCVD procedure allows direct observations of nucleation and growth, the conventional MOVCD procedure in tandem provides the necessary information to transfer knowledge between the systems and to compare with other conventional studies. Furthermore, the conventional MOCVD and ETEM-MOCVD procedures can be compared as we use the

same chip design striving to get compatibility between the systems. Section 4 presents and discusses the observations of the individual steps in the preparation and growth process including formation of Au–Si alloy and GaAs–Si integration. We identify three distinct types of NW morphologies resulting from these growth processes. Finally, section 5 concludes with insights into the significance and future applications of ETEM-MOCVD growth techniques for optimizing NW properties.

2. Sample preparation

A clean, single crystalline substrate is crucial to ensure a high yield of epitaxial growth of GaAs- NWs on Si as mentioned above. In this study, the sidewall of Si-cantilevers on a MEMS-chip served as substrate with a <111> crystal orientation. The following describes the design and preparation of the cantilevers, the procedure for depositing the Au-catalyst particles, and cleaning of the sample before loading into the growth chambers.

2.1. Chip design

The MEMS-chips were designed with two adjacent U-shaped Si-cantilevers at the center as shown in figure 1. The crystal orientation of the Si-cantilever sidewalls is <111>, allowing NWs to grow either perpendicular to the sidewall or at a 70° angle depending on sidewall facet orientation. Monocrystalline (110) silicon-on-insulator wafers were used for the MEMS-chips with a 4 μm thick device layer on top of a 0.5 μm insulating SiO_2 layer and a 300 μm handle layer, a microfabrication process that has previously been reported [26]. After fabrication, a layer of 10 μm protective photoresist was deposited on top of the device layer to prevent contamination before use, as illustrated in figures 2(a) and (b). The cantilevers were formed from the device layer, resting solely on the insulating SiO_2 layer, which acted as a temporary suspended protective membrane supporting the cantilevers before use (figure 2(c)).

2.2. Adding catalysts

The first step in adding catalyst particles to the cantilever device was to remove the protective photoresist from the device layer. The process involved soaking the chips twice in Acetone (60 ml) for 5 min and then twice in Isopropan-2-ol [IPA] (60 ml) for 5 min each (figures 2(b) and (c)). The visual color of the chips shifted from brown to gray, revealing that the removal was successful (figures 2(h) and (i)). The cleaning procedure was finished by drying the cantilever using a N_2 (g) spraygun.

HF vapor etch was then used to remove the native oxide, SiO_x, as well as the SiO_2 membrane supporting the cantilevers (figures 2(c) and (d)). This was achieved by placing the devices over a beaker containing 48 wt% HF for 3–8 min until the SiO_2-membrane at the center of the chips was etched, but no longer to avoid underetching the insulating SiO_2 layer. The edge of the hole changed from purple to grey, indicating the removal of the 0.5 μm membrane and the exposure of the bare handle layer (figure 2(i)). The etching was then continued for an additional 30–60 s to ensure full removal of the oxide on the cantilevers. After etching, the chips were rinsed in deionised water in two consecutive beakers and carefully blow-dried with N_2.

Au-catalysts were deposited onto the bare Si-cantilevers in the form of Au-nanoparticles using an aerosol system within a glove box with an N_2 atmosphere (figures 2(d) and (e)), which allows precise control over the diameter and density of the catalyst particles [28]. The deposition was done immediately after the HF etch to minimize the formation of new SiO_x on the cantilevers. For these studies, the deposited particles had a diameter of approximately 30 nm and a nominal areal density of 2.5 μm^{-2} (figure 2(j)).

2.3. Preparing for growth

After the Si-cantilevers were brought out of the inert gas environment used for depositing the catalysts, a native SiO_x layer formed on both the cantilever sidewalls and the Au-nanoparticles [30]. This layer had to be removed right before loading the Si-cantilever chips into the MOCVD chambers to ensure two things: (1) good contact between the Au-nanoparticles and the Si-substrate and (2) good contact between the Au-nanoparticles and the precursor gases.

For conventional MOCVD growth, the chips were dipped and stirred in a buffered oxide etch (BOE) (1:10) solution for 4 min right before loading into the growth chamber. While the cantilevers were heated uniformly along with the surrounding bulk substrate in the conventional MOCVD, they were locally heated from resistive heating in the ETEM-MOCVD with the temperature calibration described elsewhere [26]. To enable resistive heating with good electrical contact, a layer of Au/Ti was lift-off patterned with e-beam deposition during microfabrication on the electrode pads of the MEMS-chips used in the ETEM (figures 2(e) and (g)). Rather than using BOE etching, as this is known to etch the electrical contact material (Ti) [31], the chips for the ETEM-MOCVD were prepared by HF vapor etching for 0.5–6 min before being loaded in the TEM. This was done by placing the chips on a Teflon lid with a hole in the chip center, where the cantilevers were located.

3. Nucleation

After the sample preparation, the chips were loaded into the growth chambers. These were either the standalone MOCVD growth chamber, where the pressure was maintained constant at 10 kPa using a throttle valve, with a constant flow of H_2 and the precursor gases, or the microscope column in the ETEM-MOCVD with a variable pressure solely regulated by the precursor flows. Differences in pressure, precursor conditions, and temperature regulation (section 2.3) between the two chambers necessitated distinct approaches for nucleation. The nucleation procedures within the different growth chambers are summarized in figure 3 and described in detail in

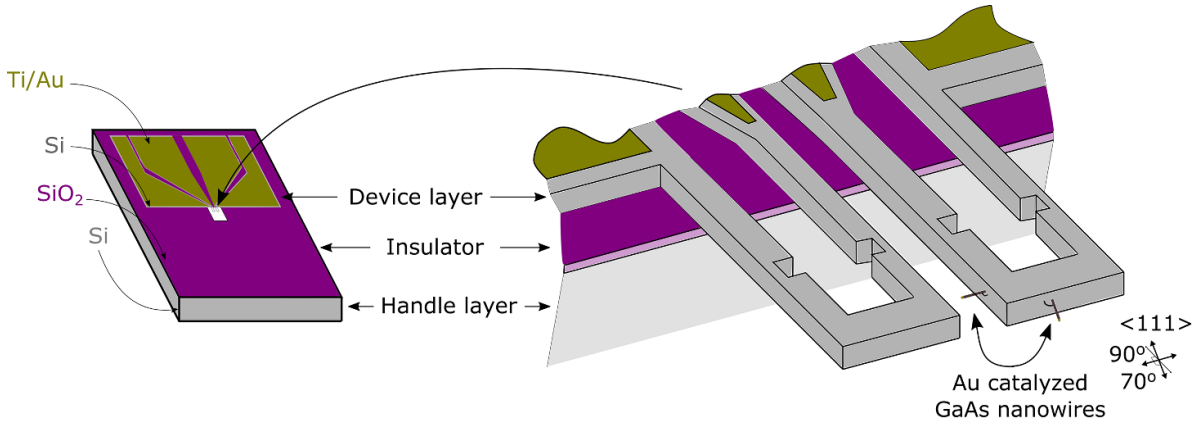

Figure 1. Overview of chip design with device, insulating and handle layers indicated. Nanowires and their orientation on cantilever sidewalls are also indicated at the chip center to the right hand side of the illustration.

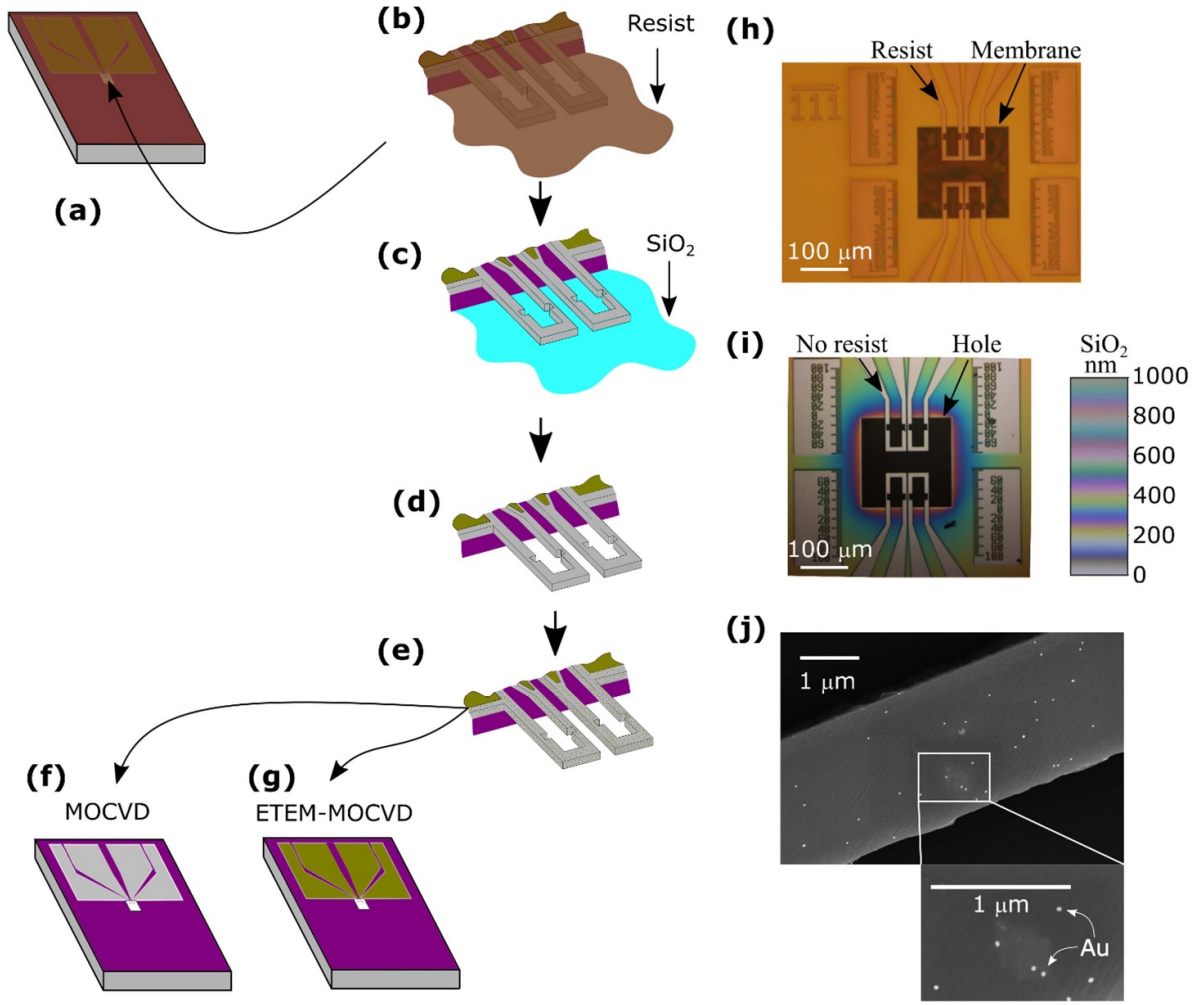

Figure 2. The preparation process of a Si-cantilever chip, focusing on the cantilever region, from removal of protective resist (a–b), removal of the protective membrane (c)–(d), and catalyst deposition (e) illustrating the resulting chips for conventional MOCVD (f) and ETEM-MOCVD (g) growth. The process steps are also illustrated by images from optical light microscopy (h)–(i) and scanning electron microscopy (j). The thickness of the oxide thin film is indicated by the color scale (i). Adapted with permission from [29] © Optical Society of America.

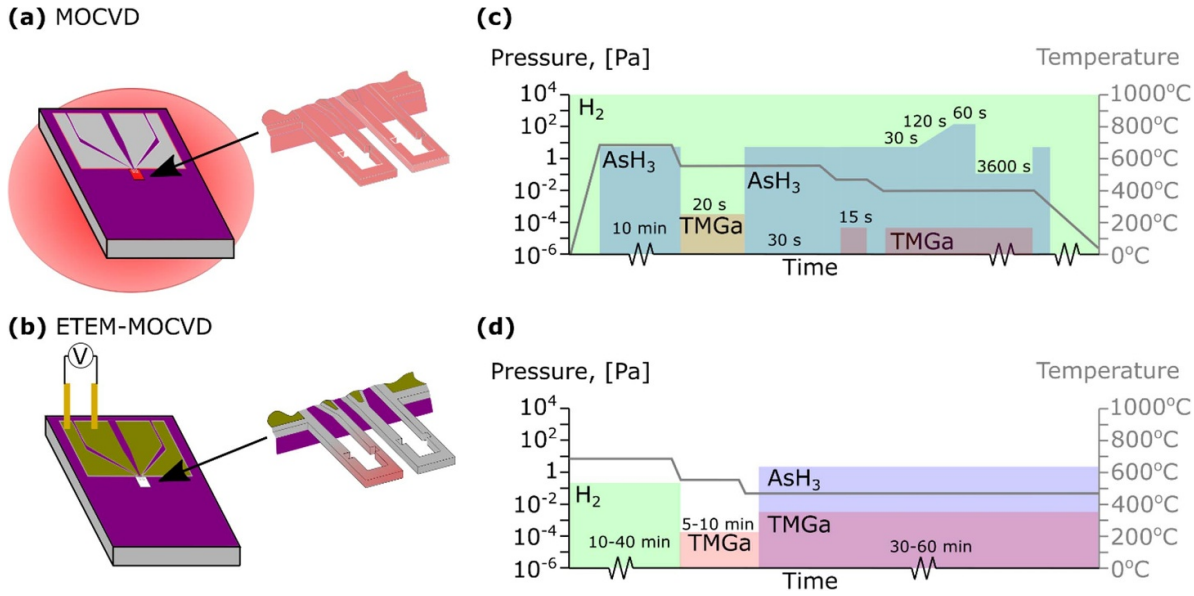

Figure 3. Illustration of the bulk heating in standalone MOCVD (a) and the resistive heating in ETEM-MOCVD (b). The precursor partial pressure and the sample temperatures are likewise illustrated in the standalone MOCVD (c) and in the ETEM-MOCVD (d), respectively.

the following sections. Despite the differences, the conceptual challenges for initiating growth were similar: removing native oxide from the substrate and particle, forming a eutectic melt, and absorbing the group-III and group-V species. The successful procedures described in the following were developed involving trial-and-error with new MEMS chips for each iteration to optimize the growth parameters and reach a high, reproducible yield of epitaxially growing III–V NWs on the Si-cantilevers.

3.1. MOCVD nucleation recipe and results

For the growth in the standalone MOCVD chamber, the samples (both the MEMS chips and reference GaAs(111B) substrates with similar deposited Au particles) were heated up in an H_2 atmosphere to a set temperature of 680 °C and annealed for 10 min at a partial pressure of 7.4 Pa AsH_3, with H_2 as a carrier gas to reduce any oxides. The temperature was then lowered to 550 °C where 5.6×10^{-4} Pa of TMGa were supplied for 20 s while simultaneously stopping the AsH_3 supply, followed by 7.5 Pa AsH_3 for 30 s directly after without a flow of TMGa. Initial growth of the NWs was obtained by reducing temperature further to 475 °C while supplying 7.5 Pa AsH_3 to protect the NWs from decomposing, and then growing GaAs NWs for 15 s by supplying 5.6×10^{-4} Pa TMGa and 7.5 Pa AsH_3 simultaneously. Regular growth of the full NW length was developed to form the cubic zincblende (ZB) structure as described below. This was obtained by lowering temperature to 400 °C supplying 7.5 Pa AsH_3, and then supplying both precursors with a constant TMGa flow with a partial pressure of 5.6×10^{-4} Pa and varying AsH_3 in four steps. These steps were 1) 30 s of 7.4 Pa AsH_3, then 2) increasing it 20 times to 148 Pa AsH_3 during 120 s to avoid kinking, 3) continuing for 60 s at 148 Pa AsH_3 and finally doing overgrowth for 3600 s with 0.175 Pa AsH_3. The growth was stopped by turning off the heat and cooling down to 300 °C with a partial pressure of 7.38 Pa AsH_3. The precursor flow was then turned off and the samples were taken out, when the temperature was below 150 °C. The resulting NWs grown under these conditions were approximately 1.5 μm long. The full procedure is illustrated in figure 3(c).

A high yield from the conventional MOCVD growth, defined as at least half of the deposited catalysts forming epitaxial NWs, was obtained by following the recipe above. Figure 4(a) shows a cantilever with GaAs NWs growing epitaxially from the Si(111) sidewall. The insets show NWs growing consistent with the <111> crystal orientation of the Si-cantilever, both perpendicular to the cantilever tip or at an angle of 70° from the side surface.

The nucleation procedure not only provided a high yield of Au-assisted GaAs NWs on Si-cantilevers, but it could also be applied to GaAs(111B) substrates allowing parameter tuning for growth studies with less expensive substrates. This was concretely used to grow NWs with mainly ZB structure and {112}A side facets following the growth procedure at 400 °C described above. These NWs could be transferred to TEM on the chips for further *in situ* growth studies; however, such studies are not the scope of this paper. An example of NWs grown on GaAs(111B) is shown in figure 4(b).

The procedure reported here provided successful growth, but other procedures have also been reported in literature giving successful growth using different growth conditions including annealing environment, nucleation temperature and the order of the precursor flow supply. The samples from the conventional MOCVD growth presented here were initially annealed in an AsH_3 atmosphere like Roest *et al* [10]. However, other studies report different initial atmospheres such as H_2 [7] and N_2 [8]. When lowering temperature, the

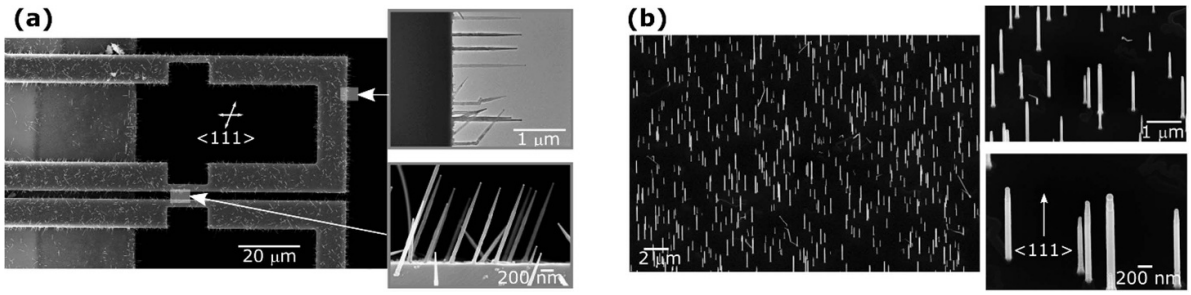

Figure 4. Au-catalyzed GaAs nanowires grown in a conventional MOCVD on Si-cantilevers (a) and (b) on GaAs(111B) substrates following the same growth procedure.

flow of AsH3 was stopped and TMGa was introduced alone to initiate nucleation. Both precursors were subsequently reintroduced to promote NW growth, based on previous experience [24]. In contrast, other studies added the precursors simultaneously immediately after annealing the sample [7, 9, 10]. Finally, the nucleation temperature of 550 °C was higher than the temperature reported in the literature, being 417 °C–455 °C [9] and 450 °C–475 °C [7, 32]. Our results show that a high yield of epitaxial NWs can be achieved with different growth strategies using a trial-and-error approach, but a strict strategy is needed for the specific instrument to achieve a positive result. To understand the effect of the individual growth process steps, *in situ* studies are thus helpful in understanding the underlying processes.

3.2. ETEM-MOCVD nucleation recipe and results

For the *in situ* ETEM-MOCVD growth, MEMS cantilever chips with deposited Au particles were loaded into the microscope within 5 min after the HF vapor etch to minimize reoxidation. A bias was applied to reach a corresponding temperature of approximately 600 °C at 0.17 Pa H_2 and the chip was then annealed for 10–40 min to ensure a stable temperature from the resistive heating. This step was done to reduce any oxides and form the initial AuSi eutectic. The Au–Ga eutectic for the NW growth was observed to form by lowering the temperature to 440 °C–470 °C and supplying 2.1 $\times$ 10^{-4} Pa TMGa for 5–10 min. Nucleation and growth of the GaAs NWs was initiated by supplying both 3.5 $\times$ 10^{-3} Pa TMGa and 2.1 Pa AsH_3 for 30–60 min. A higher yield of NWs between the cantilevers was observed, when annealing the opposing cantilever to similar temperatures. The full procedure is illustrated in figure 3(d).

For ETEM-MOCVD growth, a sufficient yield is considered as five or more epitaxial GaAs NWs per cantilever with an equivalent planar catalyst density of 2.5 μm^{-2}. This is considered as a sufficiently high yield since a single NW can be used for a full study [24, 25, 33]. Figure 5 shows successful nucleation with eight epitaxial NWs between the cantilevers at the lower part of figure 5(a). The lower yield compared to conventional MOCVD could be due to differences in growth environment such as lower pressure, temperature variation from resistive heating and electron beam-induced carbon contamination, all affecting the precursor deposition. More NWs nucleated closer to the cantilever corners, where the diffusive supply and flow velocity are higher than on the flat surfaces. Epitaxial NWs predominantly formed near the tip, where the cantilever was hotter (figure 5(b)). Preparation for ETEM-MOCVD growth involved HF vapor etch instead of BOE, resulting in a rougher surface and less flat substrate as suggested by Bao and coworkers [9], which on the other hand aided imaging the NW-substrate interface.

4. *In situ* observations from sample preparation and NW nucleation

ETEM-MOCVD can provide a deeper understanding of the preparation steps (section 4.1), the effect of the nucleation process on the NW-substrate integration (section 4.2), and the resulting NW structure and composition (section 4.3) from the sample preparation (section 2) and NW growth (section 3).

4.1. Effect of annealing during sample preparation

To optimize the interface between the Au-nanoparticles and the Si-substrate, and to improve the yield of nucleated NWs, different MEMS chips were heated for 0.5–1 min at 300 °C and 400 °C in an inert gas atmosphere (N_2) immediately after the Au aerosol deposition (section 2.2). Figure 6 summarizes the resulting Au-nanoparticles, where annealing at 400 °C led to interaction between Au and Si before the samples were loaded into the ETEM (figures 6(b) and (c)). However, this also caused the formation of a thickened SiO_x layer on both the Si-surface and a uniform coverage SiO_x of the Au-nanoparticles (figure 6(c)) [30]. This thicker oxide layer hindered NW nucleation, requiring longer HF vapor etching to remove the oxide before loading the MEMS chips into the ETEM-MOCVD. Excessive etching, however, resulted in shorted circuits in the cantilevers and chip handle layer, reducing the reliability of the process. Ultimately, cantilevers without Au-catalyst annealing were used for successful epitaxial NW nucleation, as the particles showed only partially oxidized regions on their surface (figure 6(a)). This result highlights the importance of minimizing oxidation rather than improving the Au–Si contact before loading the samples to achieve successful nucleation.

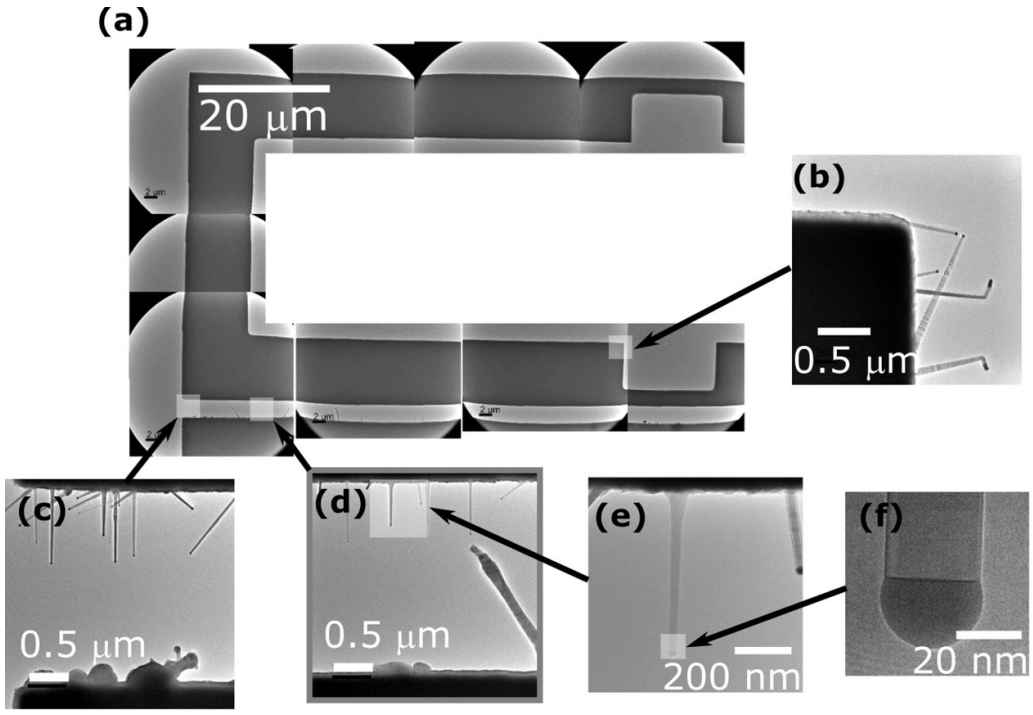

Figure 5. Au-catalyzed GaAs nanowires grown in the ETEM-MOCVD on a Si-cantilever illustrated by joined micrographs at low magnification (a) focusing on three regions of the cantilever with growth at the corner of the notch (b), the corner of the cantilever (c) and along the cantilever sidewall (d). Higher magnifications of one of the nanowires are also illustrated with an overview of the nanowire (e) and the catalyst droplet (f).

4.2. Types of NW-substrate integration

Three distinct types of NW-substrate interfaces were observed from the MOCVD and ETEM-MOCVD growth (figure 7). One type showed broad 'roots' at the GaAs/Si interface formed by the behavior of the Au–Si alloy (figure 7(a)) as elaborated below (section 4.2.1). A second type also showed broad 'roots' at the GaAs/Si interface, but the broadening was rather formed by localized surface roughness and contamination than AuSi-alloy (figure 7(b)). This is elaborated in section 4.2.2. Though the NW-substrate interface was covering larger parts of the Si-surface, GaAs was not covering all of it as reported for MBE growth [2]. A third type exhibited narrower roots, with a diameter at the interface comparable to the NW width at the tip. These NWs had oblique stacking faults with an angle of 70° (figure 7(c)), which starts at the interface of the NW-substrate as shown in section 4.2.3. Notably, the third morphology was consistently observed for NWs grown in conventional MOCVD with narrow roots (figure 7(d)) and stacking faults (figure 7(e)). The three types of NW-substrate interaction and observations of the possible growth process are discussed in the following.

4.2.1. Annealing. Broad roots may be caused by the broadening of the particle-substrate interface area upon the formation of an Au–Si alloy during the initial annealing (figure 7(a)). The Au–Si liquid droplet forms at 363 °C with 18.6 at-% Si increasing to 31 at-% at 700 °C according to the phase diagram (figure 8(a)) [34]. The expansion of the particle-substrate interface area during annealing is illustrated in figure 8(b). When SiO_x surrounds the alloy, the droplet may even form voids and etch the Si surface (figure 8(c), SI Mov2 and SI Mov3). Au is known to catalyze the process of forming volatile SiO from the solid Si-surface and SiO_x [35], underlining the need of a clean substrate. Lowering the temperature reforms a crystalline Si-surface by solidifying Si below the droplet (figures 8(d) and (e)). Hence, the final droplet-substrate integration and broadness of the root depends on the annealing history and nucleation temperature. To minimize the broadness of the roots, the initial annealing temperature should be kept at 600 °C–700°C.

4.2.2. Precursor absorption. Broad roots may also result from surface roughness near the nucleated NW (figure 7(b)) or contamination on the catalyst particle from e.g. native oxide, or carbon formed by electron beam effects. An example of an Au–Si catalyst droplet absorbing Ga is illustrated in figure 9. A solid shell covering parts of the droplet can result in the NW nucleating epitaxially next to the initial droplet position pushing the catalyst liquid outside the shell as GaAs crystal layers are forming at the Si surface. This can be avoided by minimizing the initial oxidation before loading the sample, ensuring sufficient annealing as described in the previous section

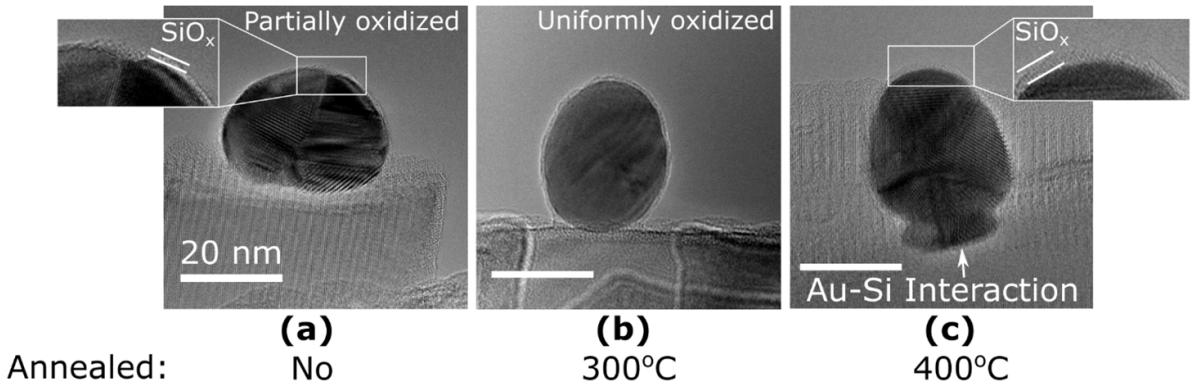

Figure 6. Au-nanoparticles on Si-cantilevers prepared with (a) no annealing, (b) annealing at 300 °C and (c) 400 °C right after the catalyst deposition. Insets for (a) and (c) indicate the SiO_x thickness. The scale bar is the same for (a)–(c).

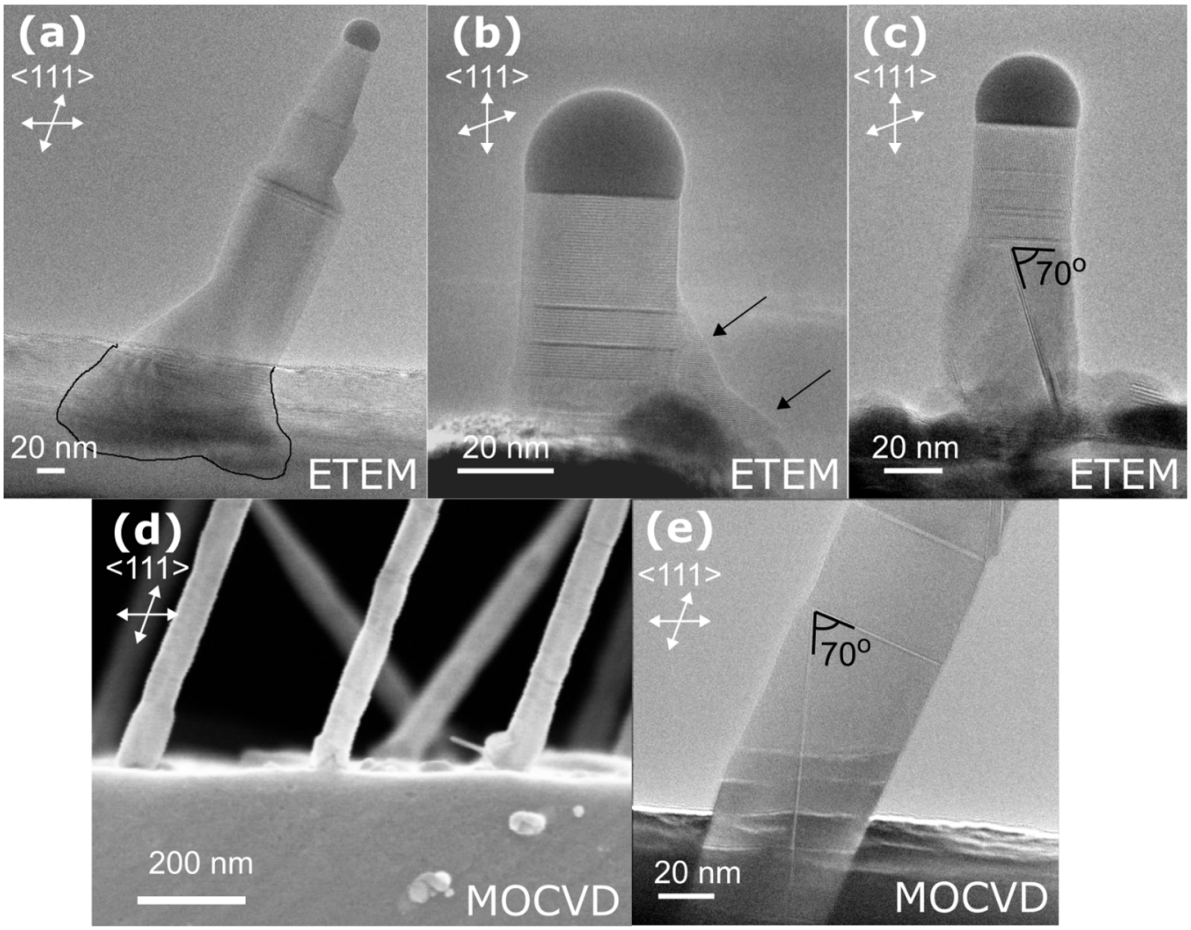

Figure 7. Examples of the nanowire-substrate interface from growth in the ETEM-MOCVD (a)–(c) and conventional MOCVD (d)–(e). The substrate <111> crystal orientation is marked below the labels. Broader regions from the interaction are marked in black (a) and black arrows (b) and oblique stacking faults are marked with their corresponding angle (c),(e). More nanowires from conventional MOCVD are illustrated with images from scanning electron microscopy (d).

and minimizing the carbon formation from electron beam illumination.

4.2.3. Nucleation. The nucleation procedure for NWs with narrower roots using ETEM-MOCVD (figure 7(c)) followed the same steps as those for NWs with broader roots (figures 7(a) and (b)). However, lower annealing temperatures and more effective removal of SiO_x may prevent the droplet-substrate interface from broadening. As the temperature decreases, Si desorbs and solidifies beneath the droplet (figure 10(a)). A constant flow of TMGa leads to the formation of an Au–Ga–Si alloy, which potentially solidifies more Si below the droplet, and the introduction of an AsH_3 flow

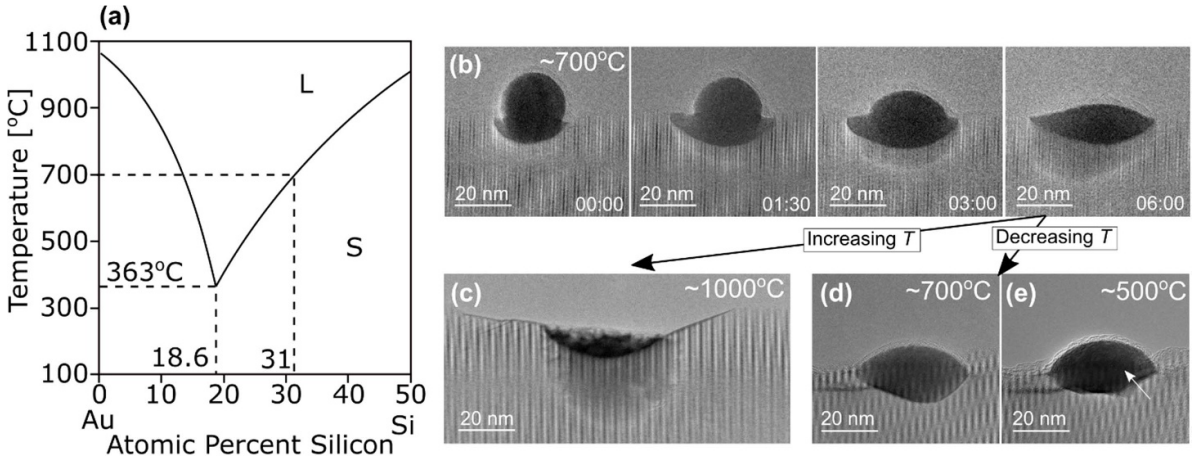

Figure 8. Phase diagram of Au–Si simplified from Okamoto *et al* reproduced with permission from SNCSC (a) with exemplifications from movie (SI Mov1) (b) and images (c)–(e) of different Au–Si interactions at different temperatures starting from approx. 400 °C at 0 s before it is increased to 700 °C after 5 s. Adapted from [34], with permission from Springer Nature.

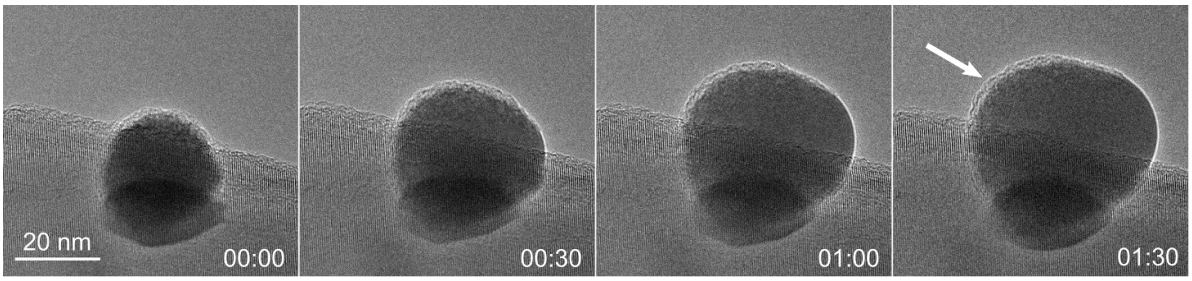

Figure 9. Movie sequence of Au–Si droplet absorbing Ga (See SI Mov4). A solid shell covers parts of the droplet as indicated by the arrow, while the liquid expands through an uncovered region (right side of the particle). The movie starts 15 s after TMGa is added to the microscope column.

initiates GaAs nucleation. Moiré patterns and strain between solidified Si and GaAs are observed at the GaAs–Si interface as marked by the white region in figure 10(a); hence some of the challenges of heteroepitaxy such as the mismatch in lattice constants are not completely overcome with the NW growth as otherwise noted in section 1. During the NW growth, starting from the interface, the crystal layers initially formed in the cubic ZB structure for NWs with both broad and narrow roots. For the NWs with a narrower root (figures 7(c) and (d)) oblique defects were observed along the growth direction at a 70° angle (figure 10(b)). These defects originate during the initial formation of the GaAs NW at the Si surface, possibly induced by the rough Si surface, similar to the behavior of APBs mentioned in section 1. This underlines the importance of further treatment of the Si-cantilevers to achieve a flatter surface e.g. by brief KOH etch of the cantilevers formed from the device layer during microfabrication [26].

4.2.4. Summary on NW morphology and outlook. For all three types of NW-substrate interfaces, the NW morphology may influence the electrical properties and reproducibility of III–V/Si devices. These challenges from Au–Si-alloy formation and broadening to Si roughness and contamination from oxide or carbon need to be addressed by optimizing the temperature, minimizing oxidation and other contamination, and flattening the Si surfaces. Further fine-tuning of these parameters can not only optimize the NW-substrate integration and NW morphology for potential optical and electrical usage, but it can potentially also increase the yield of epitaxial NWs.

4.3. Later growth and compositional results

The successful integration between NW and substrate is not the only important factor for potential use of the III–V-NW applications in III–V/Si devices. General NW properties, such as crystal structure and composition, may also be influenced by nucleation conditions, including the geometry of the Si surface, the formation of the Au–Si alloy, and the precursor flow. Therefore, we also report on the post-nucleation development of the NW crystal structure and its compositional characteristics in this section.

Initially, the NWs formed the cubic ZB structure near the substrate surface (figures 10(a) and (b)) as discussed in the previous section. However, after tens of nanometers of growth, the crystal phase translated to the hexagonal wurtzite structure (WZ) (figure 10(c)). Notably, the oblique defects stopped at the ZB–WZ interface, continuing with transverse stacking faults only for the WZ structure. The crystal phase transition can be explained as follows: Differences in diffusion lengths of precursor species on either the Si substrate or the GaAs

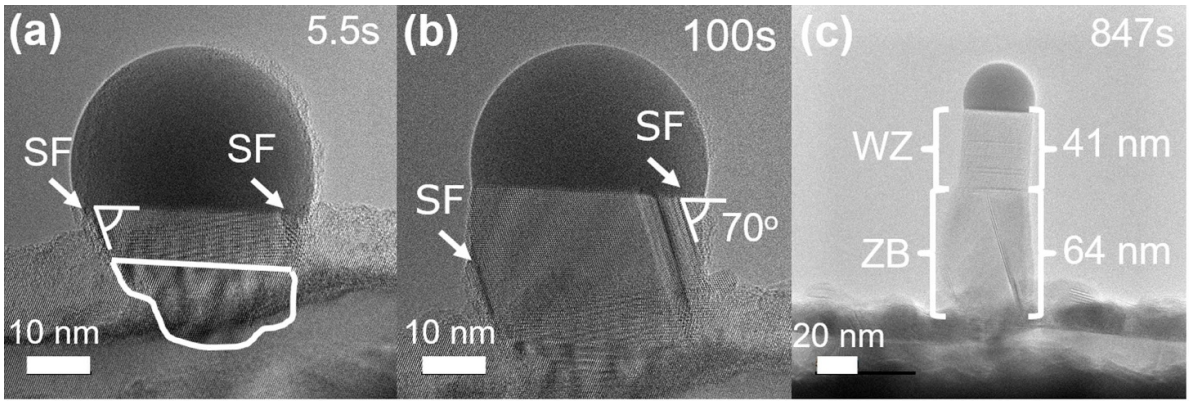

Figure 10. Movie sequence of the early stages of Au-catalyzed GaAs nanowire nucleated on Si (SI Mov5). The patterns of strong contrast changes marked by a white region (a) is considered to be Moiré patterns and strain between solidified Si and GaAs. Oblique stacking faults (SF) are indicated having an angle of 70° to the growth direction (a)–(b). The nanowire changes from a zincblende (ZB) crystal structure to a wurtzite (WZ) structure after approximately 10 min of growth (c).

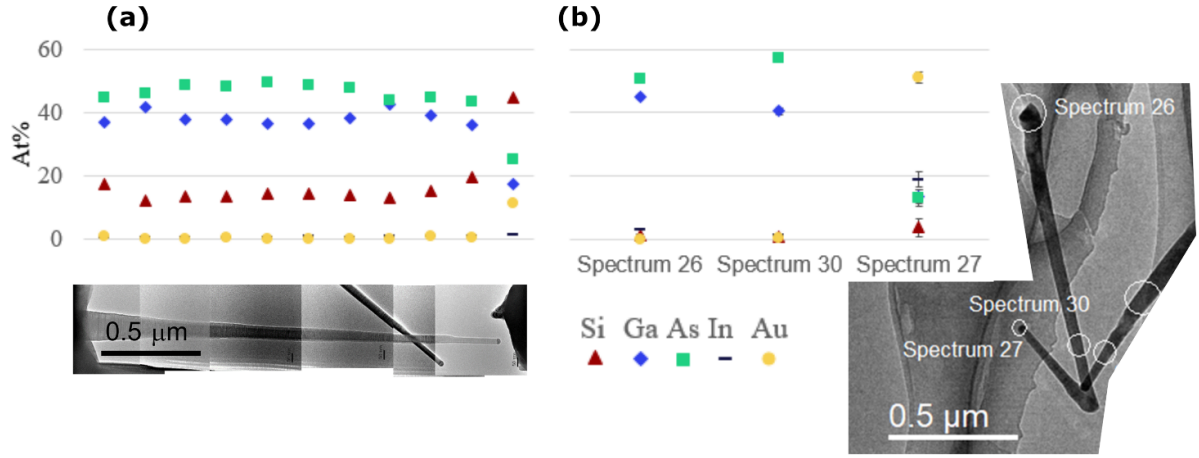

Figure 11. Compositional analysis at different positions of a nanowire on a Si-cantilever (a) and nanowires transferred to a Cu-grid (b).

NW side facets, after they have formed, might have a critical influence on the supersaturation of the seed particle and, thus, affect the preferentially formed crystal phase. Concurrently, the surface energy from the NW side facets, once formed, may have a greater impact on the growth, favoring the WZ crystal phase. A deeper understanding of the mechanisms behind crystal phase formation is outside the scope of this paper and has been addressed in previous studies [26, 36].

In addition to strutural observations, ETEM-MOCVD allows compositional analysis using EDX. This analysis provides valuable insights into the initial growth dynamics and interactions with the growth environment, enhancing the information gained from micrographs. The ternary Au–Ga–Si droplet formed after nucleation is of particular interest, as its composition can help estimate local temperatures [26, 37]. Furthermore, Si may be incorporated into the GaAs NW, potentially influencing its electrical properties, since e.g. Si is known to act as a p-type dopant in Au-catalyzed GaAs NWs grown by the VLS-mechanism [38].

For this study, a Si-signal was observed for the compositional analysis along a NW on a cantilever (figure 11(a)). However, a similar Si signal was also detected in reference spectra taken micrometers into vacuum, away from the specimen and cantilevers, indicating that the signal does not originate from Si within the NW. To clarify this, EDX was performed after mechanically transferring the NWs from the MEMS chips onto carbon laced Cu-grids, which showed no detectable Si within the NWs and small amounts, 4(3) at%, within the catalyst droplet (figure 11(b)). Indium (In) was also detected for the droplet, which is a known contamination artifact from the ETEM-MOCVD system. The elevated Si-signal from the NWs on the MEMS chips is likely due to unintended excitation of the cantilever material during heating, creating a background signal masking any real Si-signal from the NWs during *in situ* EDX. Whether Si is extracted from the GaAs/Si interface into the NW root during the nucleation has not been confirmed from the EDX as this part of the NW is not included in the transferred NWs.

It is concluded that the amount of Si in the droplet and NW is small, and the Si contribution can be ignored when estimating temperature based on droplet composition [26, 37]. The small amount of Si left in the droplet and not adopted in the

NW may be due to the balance of the ternary as observed for Au-assisted $In_xGa_{1-x}As$ NW growth [39]. Dopants in the NW close to the Si-sidewall may still be detectable, and Si doping of the NW may likewise occur further away from the sidewall; however, the signal could not be detected in this study and further investigation needs to be done characterizing the effect on the resulting electrical properties of the NWs. This should be taken into consideration and investigated further when fabricating III–V/Si devices like presented in previous reports on Si-NWs studying droplet deformation by electric fields [40], contact formation [41] and electrical characterization [42].

5. Conclusion

We report the successful epitaxial growth of Au-catalyzed GaAs NWs on Si(111) substrates using both conventional MOCVD and ETEM with an integrated MOCVD system (ETEM-MOCVD) using the same design of Si-cantilever MEMS-chips. The conventional MOCVD growth provided a framework for initial parameter tuning comparable with other growth studies, while *in situ* ETEM studies offered insights into early nucleation and catalyst-substrate interactions. Our findings show that the nucleation process is significantly influenced by the removal of native oxide layers and the formation of the Au–Si alloy. *In situ* studies revealed different NW-substrate interfaces, essential for optimizing the epitaxial growth process. We identified three types of NW-substrate interfaces, each impacted by growth conditions and preparation steps, affecting the structural and potentially the optical properties of the NWs. Compositional analysis using EDX did not reveal any Si incorporated in the NW and only small amounts in the droplet post-nucleation. Our research highlights the value of *in situ* studies for a comprehensive understanding of nucleation mechanisms, paving the way for optimizing III–V NW growth on Si substrates and developing high-performance III–V/Si devices. Future work will focus on refining ETEM-MOCVD growth techniques and exploring the electrical properties of NWs for practical electronic and optoelectronic applications.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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References

[1] Bakkers E P A M, Borgström M T and Verheijen M A 2007 Epitaxial growth of III–V nanowires on group IV substrates *MRS Bull.* **32** 117–22
[2] Breuer S, Hilse M, Trampert A, Geelhaar L and Riechert H 2010 Vapor-liquid-solid nucleation of GaAs on Si(111): growth evolution from traces to nanowires *Phys. Rev.* B **82** 075406
[3] Fang S F, Adomi K, Iyer S, Morkoç H, Zabel H, Choi C and Otsuka N 1990 Gallium arsenide and other compound semiconductors on silicon *J. Appl. Phys.* **68** 31
[4] Ohlsson B J, Malm J O, Gustafsson A and Samuelson L 2002 Anti-domain-free GaP, grown in atomically flat (001) Si sub-μm-sized openings *Appl. Phys. Lett.* **80** 4546–8
[5] Yazawa M, Koguchi M, Muto A, Ozawa M and Hiruma K 1992 Effect of one monolayer of surface gold atoms on the epitaxial growth of InAs nanowhiskers *Appl. Phys. Lett.* **61** 2051
[6] Björk M T, Ohlsson B J, Sass T, Persson A I, Thelander C, Magnusson M H, Deppert K, Wallenberg L R and Samuelson L 2002 One-dimensional heterostructures in semiconductor nanowhiskers *Appl. Phys. Lett.* **80** 1058–60
[7] Mårtensson T, Svensson C P T, Wacaser B A, Larsson M W, Seifert W, Deppert K, Gustafsson A, Wallenberg L R and Samuelson L 2004 Epitaxial III–V nanowires on silicon *Nano Lett.* **4** 1987–90
[8] Khorenko V, Regolin I, Neumann S, Prost W, Tegude F J and Wiggers H 2004 Photoluminescence of GaAs nanowhiskers grown on Si substrate *Appl. Phys. Lett.* **85** 6407–8
[9] Bao X Y, Soci C, Susac D, Bratvold J, Aplin D P R, Wei W, Chen C Y, Dayeh S A, Kavanagh K L and Wang D 2008 Heteroepitaxial growth of vertical GaAs nanowires on Si (111) substrates by metal-organic chemical vapor deposition *Nano Lett.* **8** 3755–60
[10] Roest A L, Verheijen M A, Wunnicke O, Serafin S, Wondergem H and Bakkers E P 2006 Position-controlled epitaxial III–V nanowires on silicon *Nanotechnology* **17** 271–5
[11] Krogstrup P, Popovitz-Biro R, Johnson E, Madsen M H, Nygård J and Shtrikman H 2010 Structural phase control in self-catalyzed growth of GaAs nanowires on silicon (111) *Nano Lett.* **10** 4475–82
[12] Mandl B, Stangl J, Hilner E, Zakharov A A, Hillerich K, Dey A W, Samuelson L, Bauer G, Deppert K and Mikkelsen A 2010 Growth mechanism of self-catalyzed group III–V nanowires *Nano Lett.* **10** 4443–9
[13] Plissard S, Larrieu G, Wallart X and Caroff P 2011 High yield of self-catalyzed GaAs nanowire arrays grown on silicon via gallium droplet positioning *Nanotechnology* **22** 275602
[14] Ihn S G, Song J I, Kim T W, Leem D S, Lee T, Lee S G, Koh E K and Song K 2007 Morphology- and

orientation-controlled gallium arsenide nanowires on silicon substrates *Nano Lett.* **7** 39–44
[15] Novikov B V *et al* 2010 Photoluminescence properties of GaAs nanowire ensembles with zincblende and wurtzite crystal structure *Phys. Status Solidi* **4** 175–7
[16] Hoang T B, Moses A F, Ahtapodov L, Zhou H, Dheeraj D L, Van Helvoort A T J, Fimland B-O and Weman H 2010 Engineering parallel and perpendicular polarized photoluminescence from a single semiconductor nanowire by crystal phase control *Nano Lett.* **10** 2927–33
[17] Hofmann S, Sharma R, Wirth C T, Cervantes-Sodi F, Ducati C, Kasama T, Dunin-Borkowski R E, Drucker J, Bennett P and Robertson J 2008 Ledge-flow-controlled catalyst interface dynamics during Si nanowire growth *Nat. Mater.* **7** 372–5
[18] Kim B J, Tersoff J, Kodambaka S, Reuter M C, Stach E A and Ross F M 2008 Kinetics of individual nucleation events observed in nanoscale vapor-liquid-solid growth *Science* **322** 1070–3
[19] Diaz R E, Sharma R, Jarvis K, Zhang Q and Mahajan S 2012 Direct observation of nucleation and early stages of growth of GaN nanowires *J. Cryst. Growth* **341** 1–6
[20] Maliakkal C B, Jacobsson D, Tornberg M and Dick K A 2022 Post-nucleation evolution of the liquid–solid interface in nanowire growth *Nanotechnology* **33** 105607
[21] Kallesøe C, Wen C Y, Mølhave K, Bøggild P and Ross F M 2010 Measurement of local Si-nanowire growth kinetics using *in situ* transmission electron microscopy of heated cantilevers *Small* **6** 2058–64
[22] Maliakkal C B, Mårtensson E K, Tornberg M U, Jacobsson D, Persson A R, Johansson J, Wallenberg L R and Dick K A 2020 Independent control of nucleation and layer growth in nanowires *ACS Nano* **14** 3868–75
[23] Harmand J-C, Patriarche G, Glas F, Panciera F, Florea I, Maurice J-L, Travers L and Ollivier Y 2018 Atomic step flow on a nanofacet *Phys. Rev. Lett.* **121** 166101
[24] Jacobsson D, Panciera F, Tersoff J, Reuter M C, Lehmann S, Hofmann S, Dick K A and Ross F M 2016 Interface dynamics and crystal phase switching in GaAs nanowires *Nature* **531** 317–22
[25] Panciera F, Baraissov Z, Patriarche G, Dubrovskii V G, Glas F, Travers L, Mirsaidov U and Harmand J-C 2020 Phase selection in self-catalyzed GaAs nanowires *Nano Lett.* **20** 1669–75
[26] Andersen C R Y, Tornberg M, Lehmann S, Jacobsson D, Dick K A and S M K 2024 Microheater controlled crystal phase engineering of nanowires using *in situ* transmission electron microscopy *Small Methods* **9** 2400728
[27] Tornberg M, Jacobsson D, Persson A R, Wallenberg R, Dick K A and Kodambaka S 2019 Kinetics of Au-Ga droplet mediated decomposition of GaAs nanowires *Nano Lett.* **19** 3498–504
[28] Magnusson M H, Deppert K, Malm J O, Bovin J O and Samuelson L 1999 Size-selected gold nanoparticles by aerosol technology *Nanostruct. Mater.* **12** 45–48
[29] Henrie J, Kellis S, Schultz S M and Hawkins A 2004 Electronic color charts for dielectric films on silicon *Opt. Express* **12** 1464–9
[30] Lugstein A, Hyun Y J, Steinmair M, Dielacher B, Hauer G and Bertagnolli E 2008 Some aspects of substrate pretreatment for epitaxial Si nanowire growth *Nanotechnology* **19** 485606
[31] Williams K R and Muller R S 1996 Etch rates for micromachining processing *J. Microelectromech. Syst.* **5** 256–69
[32] Borgström M, Deppert K, Samuelson L and Seifert W 2004 Size- and shape-controlled GaAs nano-whiskers grown by MOVPE: a growth study *J. Cryst. Growth* **260** 18–22
[33] Persson A R, Tornberg M, Sjökvist R and Jacobsson D 2021 Time-resolved compositional mapping during *in situ* TEM studies *Ultramicroscopy* **222** 113193
[34] Okamoto H and Massalski T B 1983 The Au-Si (Gold-Silicon) system *Bull. Alloy Phase Diagr.* **4** 190–8
[35] Bábor P, Duda R, Polčák J, Průša S, Potoček M, Varga P, Čechal J and Šikola T 2015 Real-time observation of self-limiting SiO2/Si decomposition catalysed by gold silicide droplets *RSC Adv.* **5** 101726–31
[36] Mårtensson E K, Lehmann S, Dick K A and Johansson J 2019 Simulation of GaAs nanowire growth and crystal structure *Nano Lett.* **19** 1197–203
[37] Maliakkal C B, Jacobsson D, Tornberg M, Persson A R, Johansson J, Wallenberg R and Dick K A 2019 *In situ* analysis of catalyst composition during gold catalyzed GaAs nanowire growth *Nat. Commun.* **10** 4577
[38] Hijazi H *et al* 2019 Si doping of vapor−liquid−solid GaAs nanowires: n-type or p-type? *Nano Lett.* **19** 28
[39] Sjökvist R, Jacobsson D, Tornberg M, Wallenberg R, Leshchenko E D, Johansson J and Dick K A 2021 Compositional correlation between the nanoparticle and the growing au-assisted $In_xGa_{1-x}As$ nanowire *J. Phys. Chem. Lett.* **12** 7590–5
[40] Panciera F, Norton M M, Alam S B, Hofmann S, Mølhave K and Ross F M 2016 Controlling nanowire growth through electric field-induced deformation of the catalyst droplet *Nat. Commun.* **7** 12271
[41] Alam S B, Panciera F, Hansen O, Mølhave K and Ross F M 2015 Creating new VLS silicon nanowire contact geometries by controlling catalyst migration *Nano Lett.* **15** 6535–41
[42] Alam S B, Andersen C R, Panciera F, Nilausen A A S, Hansen O, Ross F M and Mølhave K 2020 *In situ* TEM modification of individual silicon nanowires and their charge transport mechanisms *Nanotechnology* **31** 494002–13