Real-Time Power Loss Optimized Operation of a Solid State Transformer by Utilizing the Common-Mode Voltage

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***Index Terms*—Analytical loss computation, Cascaded H-Bridge, Dual Active Bridge Converter, Solid-State Transformer**

***Abstract*—This article presents a general methodology and a real-time solvable, analytical model for reducing the total losses of the cells of a Solid-State Transformer (SST). The efficiency is increased with the usage of the online optimized common-mode voltage u_{CM}. Measurements on a $400\mathrm{V_{AC}}$ to $750\mathrm{V_{DC}}$, 45kW SST test bench verify the calculation results and the operating principle of the algorithm. A loss reduction of up to 20% is possible without introducing additional restrictions to the SST.**

I. Introduction

For use as a medium voltage (MV) alternating current (AC) to low voltage (LV) direct current (DC) grid coupling, the Solid-State Transformer (SST) offers significant potential and advantages. These include controlled active and reactive power flow, higher volumetric and gravimetric power density, fewer inverter stages, and active filtering of grid harmonics compared to a conventional low-frequency transformer (LFT) with an additional inverter stage [1]. However, a major drawback of SST is its lower efficiency compared to LFT [2]. To address this limitation, extensive research has focused on reducing the efficiency gap while enhancing existing benefits and overall SST design, including its lifetime [3]. A common topology for connecting a MV AC grid to an LV DC microgrid is the input serial output parallel (ISOP) structure, built with similar power modules. These modules supply energy on either the MV or LV side, depending on the power flow direction. The Dual Active Bridge (DAB) is often used as a galvanically isolating power transmission stage. First introduced in [4], it has since been extensively studied and improved. Its main advantages are high dynamic performance, zero voltage switching (ZVS) capability, and controllable bidirectional power flow. Improving the efficiency of the DABs, and thus the sub-modules, directly enhances the overall efficiency of the SST [5]–[7]. While traditional methods focus on improving the modulation scheme or upgrading hardware, this publication explores a different approach using a degree of freedom inherent in the three-phase system of an SST. Starting from a basic loss function derived from a single DAB, a mathematical loss model is developed for the phases and the entire SST. By applying various common-mode (CM) voltages u_{cm} to this model, the system's power losses for the next operation point (OP) can be predicted. This approach enables significant real-time reduction of total system losses.

In Section II of this paper, the topology and the key components of the investigated system are described. In Section III, the analysis is presented in several steps. First, Section III-A discusses the measured power losses of a single DAB module, showing its loss behavior. Next, Section III-B introduces a cost function for the entire SST, combining losses from all modules. Section III-C explains how the CM voltage u_{cm} can be adjusted to reduce total power losses. In Section III-D, a mathematical optimization method is used to minimize power losses by changing u_{cm}. Finally, Section IV presents calculated and experimental results, confirming the accuracy and effectiveness of the proposed optimization method.

II. Topology

The investigated topology is a three-phase modular Cascaded H-Bridge (CHB)-based SST in a star connection, with each cell individually powered by a galvanically isolated DAB. A single power module, consisting of a CHB cell and a DAB stage, is illustrated in Fig. 1. The DAB, highlighted in blue, enables unrestricted bidirectional power flow and operates at unity gain in this study. The CHB cell, highlighted in green, generates the AC output of each power module. The overall topology of the prototype is depicted in Fig. 2. The DAB stages are connected in parallel and are powered by a bidirectional DC voltage source with an output voltage of U_p. The converter's AC output voltages $u_{\mathrm{AC},x}$, where $x \in \{\mathrm{U}, \mathrm{V}, \mathrm{W}\}$, are produced by a series connection of the CHB cells. Depending on the switching state of the four MOSFETs T_1 to T_4, the CHB cell provides three discrete voltage levels $u_\mathrm{FB} \in \{+U_\mathrm{mod}, -U_\mathrm{mod}, 0\,\mathrm{V}\}$. Each SST phase operates using voltage shifted pulse width modulation (VSPWM) with one switching module per phase. In general the current CM voltage u_cm is calculated as shown in (1). The voltage between the phase and the neutral point of the converter is defined as $u_{\mathrm{AC},x,\mathrm{sp}}$.

$$u_\mathrm{cm} = \frac{1}{3} \cdot \sum_x u_{\mathrm{AC},x,\mathrm{sp}} \tag{1}$$

To enhance voltage utilization of the converter, a triangular-shaped CM voltage $u_{\mathrm{cm,tri}}$ is added to the voltage setpoints of the controller. This triangular CM voltage setpoint is calculated as shown in (2). This degree of freedom is further leveraged by the proposed algorithm described in the following sections. In this publication, the harmonic content of the output voltage is not analyzed in detail. This simplification is justified, as the SST operates as a multilevel converter with many voltage levels per phase and an assumed switching frequency in the kilohertz range. More details on reducing the harmonics is described in [8], [9], for example. In addition, the DAB is set up to transfer enough power to neglect a voltage ripple of the DC link capacitors, and no special voltage suppression method needs to be implemented as in [10].

$$u_{\mathrm{cm,tri}} = -\frac{\min\left(u_{\mathrm{AC,UVW}}\right) + \max\left(u_{\mathrm{AC,UVW}}\right)}{2} \tag{2}$$

The switching states with the resulting output voltages u_FB and the module current i_mod in dependence of the phase current i_AC of the CHB cell is shown in Table I.

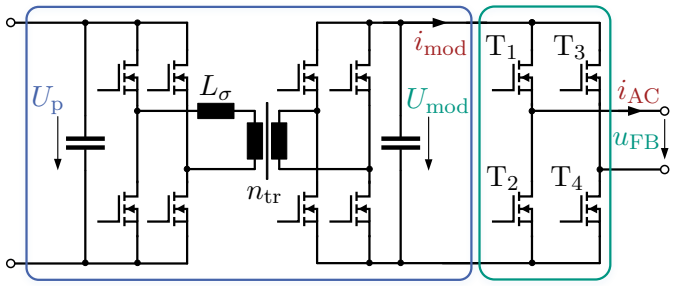


Fig. 1: Power module with DAB stage for power supply (blue) and CHB cell output stage (green).

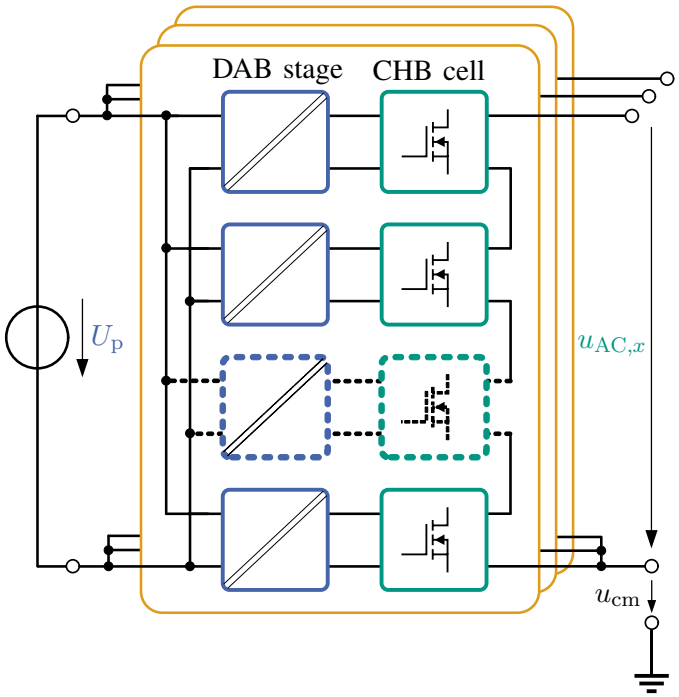


Fig. 2: Three phase modular ISOP SST for AC/DC grid coupling. The dotted module means that there can be several modules.

TABLE I
Switching states of the CHB cell

State	Conducting	Output voltage u_FB	Module current i_mod
Positive	$\mathrm{T}_1, \mathrm{T}_4$	U_mod	i_AC
Negative	$\mathrm{T}_2, \mathrm{T}_3$	$-U_\mathrm{mod}$	$-i_\mathrm{AC}$
Bypass 1	$\mathrm{T}_1, \mathrm{T}_3$	0 V	0 A
Bypass 2	$\mathrm{T}_2, \mathrm{T}_4$	0 V	0 A

III. Proposed optimized operation mode

The proposed power loss-optimized operation mode of the SST aims to reduce overall power losses by considering the individual losses of each DAB at the current OP. Therefore, a mathematical model is developed to analytically describe the power losses of each DAB (Section III-A). Using this model, the power losses of each phase and the entire SST can be predicted based on the current operating conditions (Section III-B). The total losses are then minimized by adjusting the CM voltage u_{cm}, which serves as a degree of freedom in the system (Section III-D). A key requirement when applying the proposed method is ensuring that the setpoints of the superimposed current controller remain unaffected. This is achieved by maintaining the relevant line-to-line voltages of the SST unchanged, even when the CM voltage u_{CM} is modified.

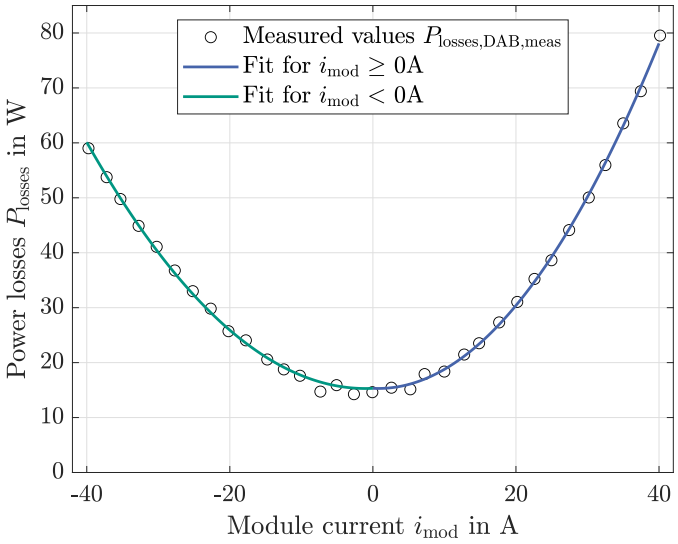


Fig. 3: Measured and fitted power losses of a DAB with $U_{\mathrm{p}} = 750\,\mathrm{V}$ and $U_{\mathrm{mod}} = 53.2\,\mathrm{V}$.

A. Power losses of a single DAB

Firstly, the power losses of the DAB stage of a power module operating at unity gain (cf. the blue box in Fig. 1) are measured using a power meter with fixed primary and secondary voltages U_{p} and U_{mod}. The measured losses are fitted to a function based on the module current i_{mod}. Ohmic losses of the CHB cell are not included, assuming that two of the four semiconductors (T_1 to T_4) always conduct the phase current $i_{\mathrm{AC,x}}$, as shown in Table I. Furthermore, it is assumed that the switching losses of the CHB cells remain within the same range as they would without the proposed method. Figure 3 shows the measured power losses $P_{\mathrm{losses,meas}}$ (black circles). The results reveal an asymmetry between positive and negative module currents. This asymmetry arises from different voltage levels on the primary and secondary sides, leading to varying semiconductor switching behavior. More hardware details are provided in Section IV.

Secondly, to obtain an analytical description of power losses as a function of the module current i_{mod}, the measurement results are used for curve fitting. Due to the observed asymmetry, two separate functions are employed: one for positive output power ($i_{\mathrm{mod}} \geq 0\,\mathrm{A}$) and another for negative output power ($i_{\mathrm{mod}} < 0\,\mathrm{A}$). Since lower-order polynomials are easier to handle and capture the primary loss contributions — quadratic for copper losses, linear for switching losses, and constant for transformer core losses under fixed switching frequency and voltages [11] — a quadratic function is chosen, as shown in (3). If sufficient computational power is available, higher-order polynomials or other function types could be used for more precise real-time optimization.

$$P_{\mathrm{losses,DAB}}(i_{\mathrm{mod}}) = p_{2,\mathrm{k}} \cdot i_{\mathrm{mod}}^2 + p_{1,\mathrm{k}} \cdot i_{\mathrm{mod}} + p_{0,\mathrm{k}} \quad (3)$$

Thirdly, the variables $p_{n,k}$ serve as fitting parameters, where $n \in \{2, 1, 0\}$ represents the coefficients for the quadratic, linear, and constant terms of the loss function. The index $k \in \{\mathrm{pos}, \mathrm{neg}\}$ indicates whether the power flow within a module is positive or negative, respectively. This distinction ensures an accurate representation of the asymmetric power loss behavior observed during the measurements.

Fourthly, due to physical considerations, it is reasonable that the power losses for very small positive and negative currents, close to $0\,\mathrm{A}$, should be similar. This leads to a constant offset and an intersection of the curves, creating a continuous function that may not be continuously differentiable. Consequently, $p_{0,\mathrm{pos}} = p_{0,\mathrm{neg}} = p_0$. The results of the fitting parameters for the investigated scaled prototype are shown in Section IV.

B. Mathematical model of SST phase losses caused by the DABs

The fitted power loss curves of a single DAB are combined into an analytical power loss model for a single phase of the SST, depending on the number of modules per phase, m_{ph}. Figure 4 illustrates the phase power losses as a function of different phase currents i_{AC}. As mentioned earlier, each phase operates with VSPWM. In this mode, only one module is actively

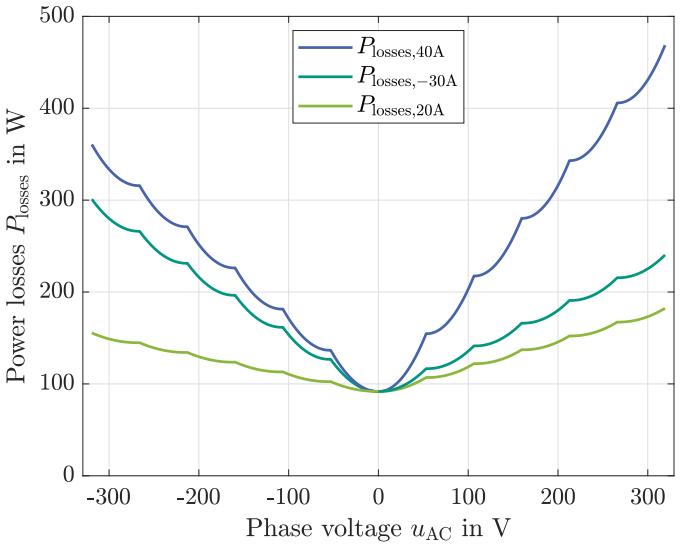


Fig. 4: Calculated power losses of a single phase with six modules for different phase currents and voltages.

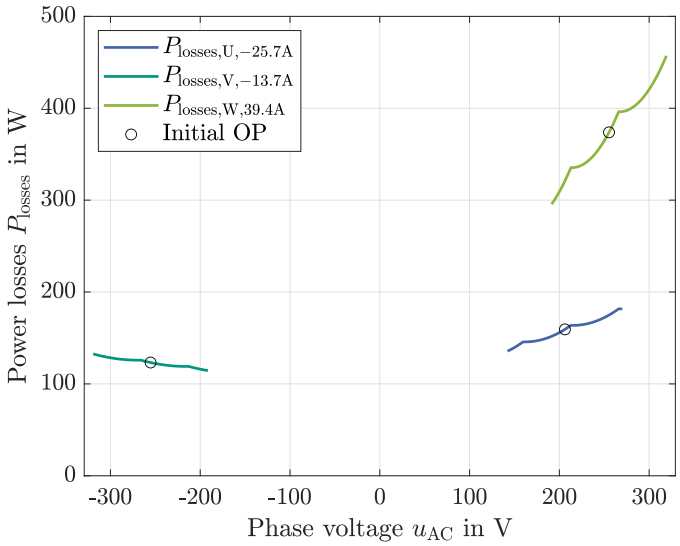


Fig. 5: Calculated power losses of each phase for a specific OP and residual voltage modification range ($\hat{u}_{\text{AC}} = 325\,\text{V}$, $\hat{i}_{\text{AC}} = 40\,\text{A}$, $\varphi = 65°$, $\omega t = 25°$).

switching, while the other modules are either in bypass or in an active state (i.e., positive or negative) to achieve the phase voltage setpoints $u_{\text{AC,x,sp}}$ of the overlaid controller as accurately as possible.

The number of modules in a phase in an active state is an integer value and denoted by $a_{\text{fix},x}$, where $a_{\text{fix},x} \in \mathbb{Z}$ and $-m_{\text{ph}} \leq a_{\text{fix},x} \leq m_{\text{ph}}$. Each DAB stage of a module in a positive state must deliver the corresponding phase current ($i_{\text{mod}} = i_{\text{AC}}$) to maintain a constant module voltage U_{mod}. Modules in a negative switching state have to supply the negative phase current ($i_{\text{mod}} = -i_{\text{AC}}$). Modules in bypass state do not transmit any power in this control cycle ($i_{\text{mod}} = 0\,\text{A}$). The DAB stage of the switching module supplies a portion of the phase current ($i_{\text{mod}} = a_{\text{dc}} \cdot i_{\text{AC}}$), determined by the duty cycle $a_{\text{dc},x}$ with $-1 \leq a_{\text{dc},x} \leq +1$, which is derived from the voltage setpoint of the current controller.

It is evident that smaller phase voltages and currents result in lower phase losses. However, phase currents are not a degree of freedom, as they are defined by the superimposed controller and the grid. The resulting mathematical loss model of a single phase is shown in (4).

$$\begin{aligned} &P_{\text{losses},x}(a_{\text{fix},x}, a_{\text{dc},x}, m_{\text{ph}}, i_{\text{AC},x}) = \\ &p_{2,\text{k}} \cdot \left(|a_{\text{fix},x}| + a_{\text{dc},x}^2\right) \cdot i_{\text{AC},x}^2 + \\ &p_{1,\text{k}} \cdot (a_{\text{fix},x} + a_{\text{dc},x}) \cdot i_{\text{AC},x} + \\ &p_0 \cdot m_{\text{ph}} \end{aligned} \tag{4}$$

Combining (4) for each phase and considering that the change in CM voltage u_{cm} changes $a_{\text{fix},x}$ and $a_{\text{dc},x}$ as shown in (5) and (6) for each phase x leads to (7). The function 'trunc' is a truncation which means rounding to the next integer in the direction of zero.

$$a_{\text{fix},x}(u_{\text{cm}}) = \text{trunc}\left(\frac{u_{\text{AC},x,\text{sp}} + u_{\text{cm}}}{U_{\text{mod}}}\right) \tag{5}$$

$$a_{\text{dc},x}(u_{\text{cm}}) = \frac{u_{\text{AC},x,\text{sp}} + u_{\text{cm}}}{U_{\text{mod}}} - a_{\text{fix},x}(u_{\text{cm}}) \tag{6}$$

$$P_{\text{losses,total}}(u_{\text{cm}}) = \sum_x P_{\text{losses},x}(u_{\text{cm}}) \tag{7}$$

C. *Using the common-mode voltage for optimization*

Since the investigated SST is a three-phase system in a star connection, it inherently offers the opportunity to use the CM voltage u_{cm} for various objectives. Primarily, the CM voltage is typically used to increase the maximum output voltage. However, because the SST does not always operate at its voltage limits, the residual voltage range of the combined phases can be utilized to reduce overall losses. This is achieved by operating more DABs at higher efficiency and fewer at less efficient OP.

Figure 5 illustrates an example OP with the setpoint for the triangular CM voltage at $u_{\text{cm}} = 68.7\,\text{V}$ (black circles). When the CM voltage is modified, all three phase voltages shift in the same direction simultaneously to maintain the same line-to-line voltage. However, the losses in each phase change differently depending on the corresponding phase currents.

To highlight the potential for power loss modification, Fig. 6 shows the power losses of each phase as

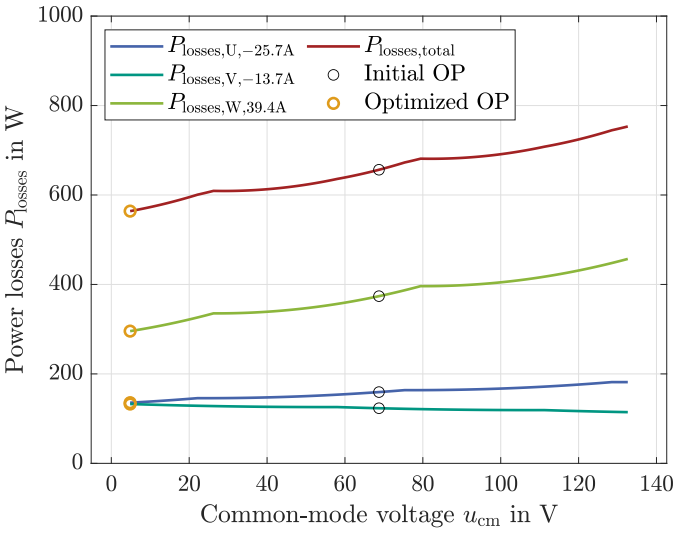


Fig. 6: Losses within each phase and total DAB losses in relation to the residual CM voltage u_{cm} range.

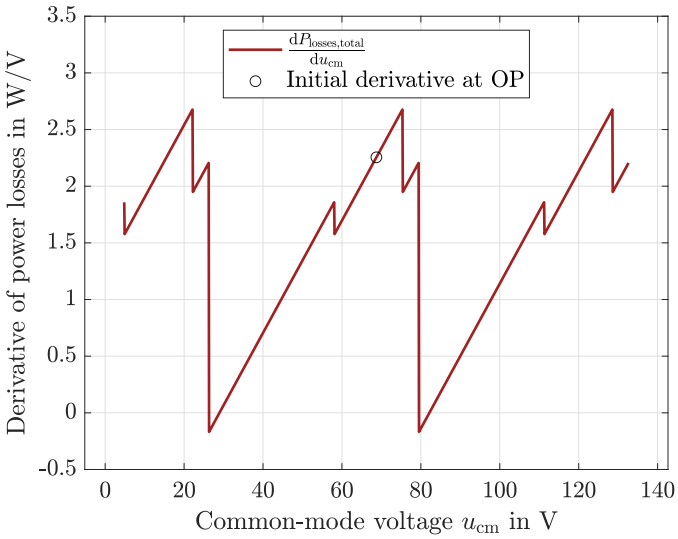


Fig. 7: Derivative of total power losses $\frac{\mathrm{d}P_{\text{losses,total}}}{\mathrm{d}U\text{cm}}$ with respect to CM voltage u_{cm}.

a function of the permissible CM voltage u_{cm} range. Additionally, the sum of the phase losses $P_{\text{losses,total}}$ and the initial OP are displayed. It is evident that in this case, reducing the CM voltage u_{cm} also reduces the total power losses. Hence, the overall efficiency of the SST is increased.

D. Minimizing the overall DAB power losses

Due to the mathematical power loss model of each phase, it is possible to solve this constrained, superimposed optimization problem analytically. Since the power losses are represented by polynomial fitting functions, calculating the local derivatives and setting them to zero to find local minima is simple. Solving (8) for u_{cm} leads to a local and potential global minimum. Given the constraints, the maximum and minimum common-mode voltages must also be tested to identify the global minimum. By evaluating this limited set of potential local minima with the predicted losses from (7), the global minimum of the power losses is determined and applied to the output of the SST phases.

$$\frac{\mathrm{d}P_{\text{losses,total}}}{\mathrm{d}u_{\text{cm}}} = \sum_{x} \frac{\mathrm{d}P_{\text{losses},x}}{\mathrm{d}u_{\text{cm}}} = 0\,\text{W}\,\text{V}^{-1} \tag{8}$$

An upper bound of the amount of potential local minima B_{opt} can be calculated according to (9). It is proportional to the amount of modules per phase m_{ph}. The implementation has to be capable of calculating and comparing all of these B_{opt} potential local minima within one control cycle to be deterministic. However, in reality the absolute number of local minima is smaller, since the valid CM voltage range is reduced because of the actual voltage setpoints of the superimposed current controllers.

$$B_{\text{opt}} = 3 \cdot (2m_{\text{ph}} + 1) \tag{9}$$

In Fig. 7 the overall derivative of the mentioned OP is shown, revealing two local minima. However, the global minimum is found at the minimal CM voltage $u_{\text{cm}} \approx 4.8\,\text{V}$. As a result, the power losses at this particular OP can be reduced from $P_{\text{losses,total,old}} \approx 660\,\text{W}$ to $P_{\text{losses,total,new}} \approx 566\,\text{W}$. The optimized OP is highlighted with the orange circles in Fig. 6.

IV. Results

Both the calculated results and the measurements in the following subsections are generated with the system, described in Table II. The algorithm is implemented on an field-programmable gate array (FPGA) which operates with a frequency of $f_{\text{FPGA}} = 150\,\text{MHz}$. The algorithm is able to calculate the loss optimized common-mode voltage in real-time.

A. Hardware setup

Figure 8 shows a picture of a single power module of the SST. It consists of the DAB stage, the CHB cell, a plug-in FPGA controller board, and current, voltage, and temperature measurement systems. The control of the capacitor's voltage in each power module is managed by a simple PI-controller. The SST is controlled by a modular signal processing platform that incorporates two ARM-core processors and a high-performance FPGA [12]. The control structure of the SST as grid coupling between a 400 V AC and a 750 V DC grid is explained detail in [13].

TABLE II
System specification

Parameter	Symbol	Value
Modules per phase	m_{ph}	6
Module voltage	U_{mod}	53.2 V
Primary/ DC grid voltage	U_{p}	750 V
Transformer winding ratio	n_{tr}	14.11:1
DAB and CHB switching frequency	$f_{\mathrm{DAB}}, f_{\mathrm{CHB}}$	50 kHz
Maximum phase current	$I_{\mathrm{AC,max}}$	60 A
Nominal power of DAB	P_{DAB}	2.5 kW
Nominal power of SST	P_{SST}	45 kW
System control frequency	f_{sys}	50 kHz
AC grid voltage	U_{grid}	400 V
Grid frequency	f_{grid}	50 Hz
Grid filter	L_{filter}	1 mH

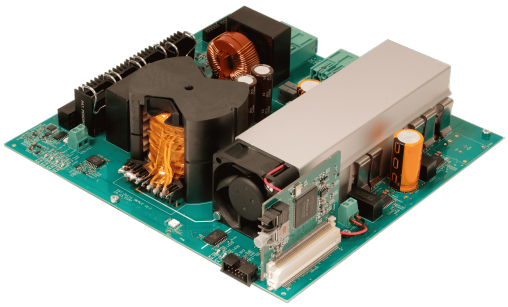


Fig. 8: Hardware of the power module with a DAB stage and the CHB cell.

B. Calculation results

The results of the fitting process for the values shown in Fig. 3 are presented in Table III.

As a reference for the proposed optimization method, indicated with the index opt, the total losses $P_{\mathrm{losses,total}}$ and the resulting CM voltage u_{cm} are compared to the modulation scheme with a maximized output voltage range (triangular shape), indicated by the index tri. It is important to note that the proposed method does not restrict the maximum output voltage. To verify the

TABLE III
Fitting parameters specification

Parameter	Value
$p_{2,\mathrm{pos}}$	$40.8\,\mathrm{mW\,A^{-2}}$
$p_{1,\mathrm{pos}}$	$-61.9\,\mathrm{mW\,A^{-1}}$
$p_{2,\mathrm{neg}}$	$29.5\,\mathrm{mW\,A^{-2}}$
$p_{1,\mathrm{neg}}$	$60.4\,\mathrm{mW\,A^{-1}}$
p_0	15.3 W

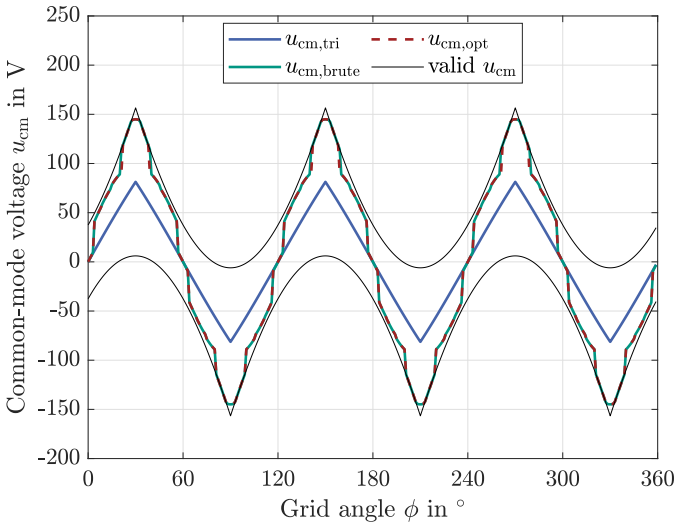


Fig. 9: Comparison of the valid CM voltage u_{cm} for a grid period.

calculation results of the loss-optimized method, a time-consuming, not real-time capable brute-force algorithm is implemented in MATLAB, indicated by the index brute. The OP shown in the following figures (Fig. 9, Fig. 10 and Fig. 11) is $\hat{U}_{\mathrm{AC}} = 325\,\mathrm{V}$, $\hat{I}_{\mathrm{AC}} = 40\,\mathrm{A}$, $\varphi = 0°$. Figure 9 shows that the analytical and the brute-force approach yield the same results, which differ from the triangular shape. The black lines indicate the minimum and maximum CM voltage range for this setup and grid voltages. It can be observed that the optimized CM voltage u_{cm} only matches the reference values at grid angles close to integer multiples of $\omega t = 60°$. The resulting phase voltages of the converter are shown in Fig. 10. Although these phase voltages do not resemble a sinusoidal waveform, the resulting line-to-line voltage between two phases, which is relevant for controlling the sinusoidal currents, is sinusoidal and shown in red.

Fig. 11 shows the calculated power losses P_{losses} for the different calculation methods. It is evident that when the CM voltages u_{CM} are equal, the power losses are equal, too. Hence, the loss-optimized method achieves operating points that result in power losses equal to or lower than those of the reference method, with a reduction in losses occurring in most cases. Consequently, the overall efficiency of the DAB stages is improved. As a result of the optimization of each OP of the SST, the power losses over a full grid period are also reduced.

C. Experimental results

To evaluate the actual power loss reduction, measurements with different setpoint currents for I_{d} and I_{q} are conducted on the grid. As an example Fig. 12 shows the resulting voltage and current of phase U for

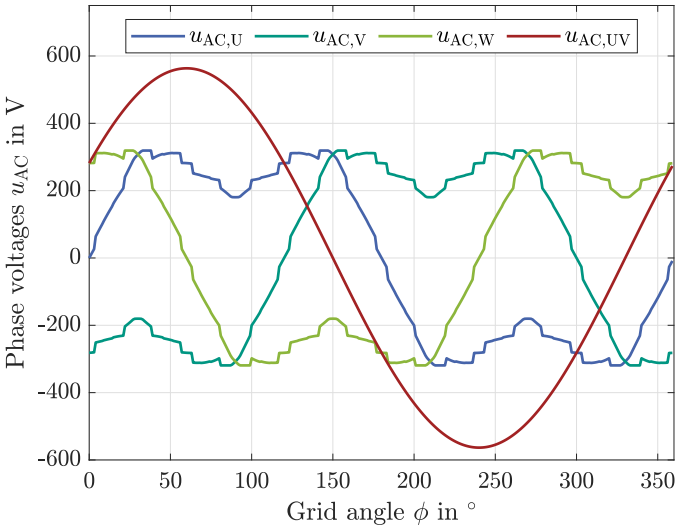


Fig. 10: Resulting calculated, switching period average SST output phase voltages with loss optimized CM voltage. Resulting sinusoidal line-to-line voltage $u_{AC,UV}$ between phases U and V.

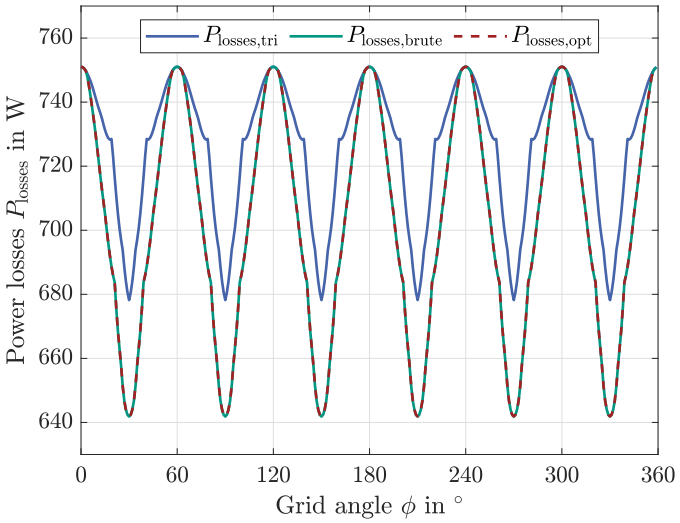


Fig. 11: Comparison of the resulting losses P_{losses} during a grid period.

an OP of $I_d = 0\,A$ and $I_q = 30\,A$. As previously mentioned, the phase current is not affected by the proposed scheme. However, due to the different CM voltage, the phase voltage takes on a different form. The loss reduction over the full operation range of the SST is shown in Fig. 13a. Additionally, a calculation with the same setpoints for voltages and currents is performed to compare the results and assess the accuracy of the model. The calculated results are presented in Fig. 13b. Both the measurements and the calculations show high accordance with a reduction in power losses of more than 160 W, even though the calculation does not consider harmonic voltages of the grid. However, there

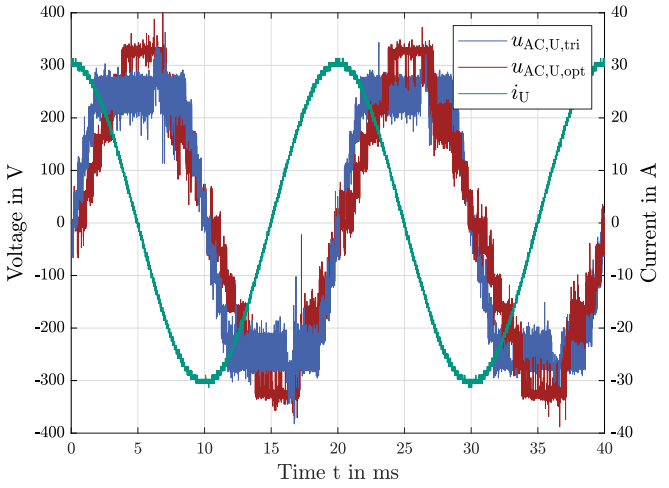
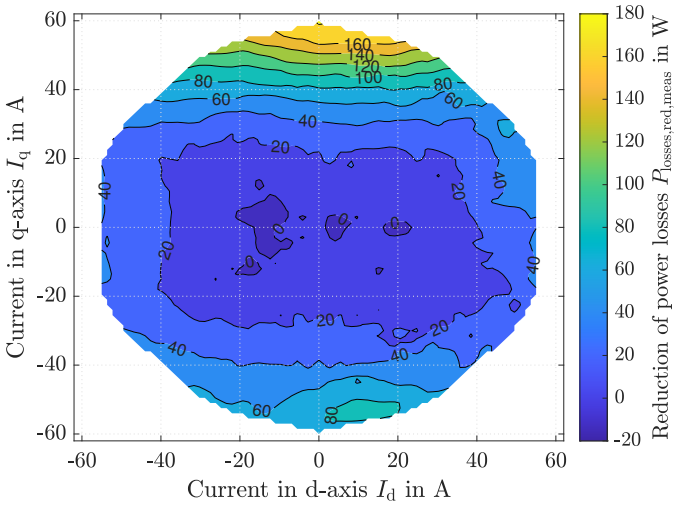


Fig. 12: Measured reference (blue) and optimized (red) voltage and current (green) of phase U with $I_d = 0\,A$ and $I_q = 30\,A$.

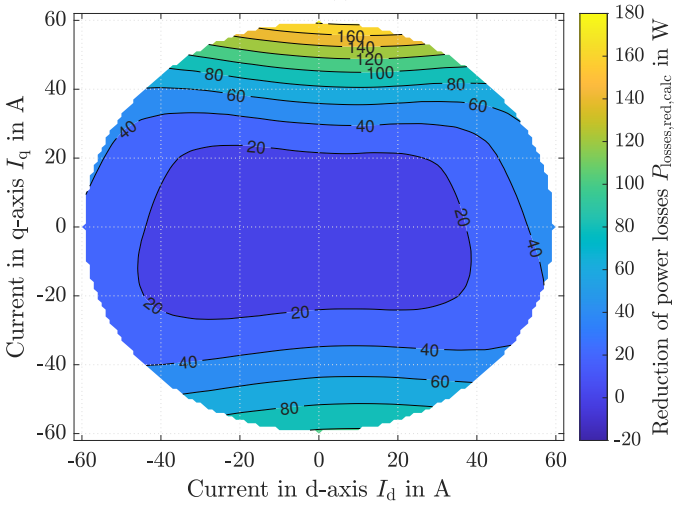
are some deviations at low current setpoints which can be caused by the accuracy of the measurement system. The reason for the asymmetric behavior with high positive and high negative currents in the q-direction is due to the effect of the voltage drop across the filter inductance L_{filter}. A positive q-current leads to a decrease in the required voltage in the d-direction, while a negative q-current increases the d-voltage setpoint. Due to this fact, less voltage is necessary to control the current, resulting in a wider range of valid values of the CM voltage u_{CM}. Figure 13 shows that the power losses of the DAB stages can be significantly reduced in nearly every OP. Figure 14 shows the relative reduction of the power losses for the calculation with a maximum relative reduction of 20 %.

V. Conclusion

This paper presents a detailed approach to minimize the sum of power losses across all DAB modules of an SST, while being real-time capable. The approach is based on a mathematical model of the power losses for a single DAB module. After combining these into a model for a phase and then for the entire SST, it is used to estimate and minimize the total power losses of all 18 DAB modules by leveraging the residual degree of freedom in the CM voltage u_{CM} of the three-phase system. Calculations demonstrate the resulting CM voltage and the reduced losses of the entire converter by up to 20 %. Experiments validate these calculated results with high accuracy. Further research could explore alternative modulation schemes for the SST, generalize the approach for unscaled high-power DABs, optimize



(a)



(b)

Fig. 13: Reduction of (a) measured power losses $P_{\text{losses,red,meas}} = P_{\text{losses,tri,meas}} - P_{\text{losses,opt,meas}}$ and (b) calculated power losses $P_{\text{losses,red,calc}} = P_{\text{losses,tri,calc}} - P_{\text{losses,opt,calc}}$ at different OP for the loss optimized method in contrast to the reference.

the distribution of power transferred by the DABs, and incorporate the required redundancy of the SST.

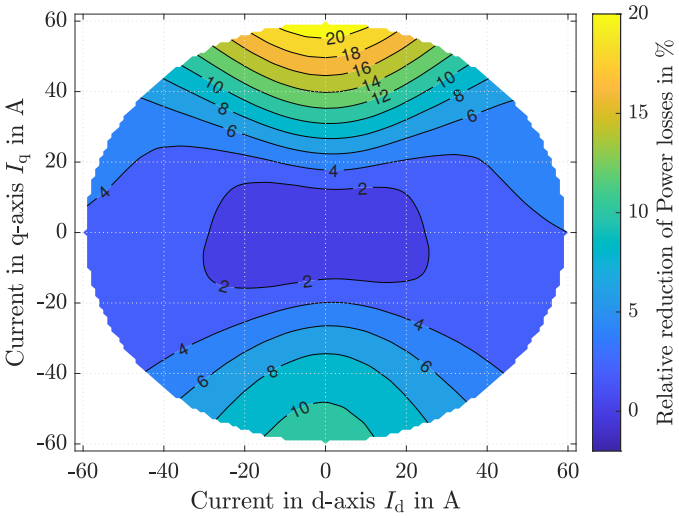


Fig. 14: Calculated relative reduction of the losses of the DAB stages.

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