Design and Investigation of Efficient Millimeter-wave Silicon-based Power Amplifiers

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Zusammenfassung

Mit dem Bestreben höhere Datenraten für die nächsten Generationen der mobilen Kommunikationsinfrastruktur, zum Beispiel für Mobilfunk der fünften und sechsten Generation, sowie für zukünftige Satellitenkommunikation zu erreichen, sind Frequenzbänder zwischen $10\,\mathrm{GHz}$ und $60\,\mathrm{GHz}$ ein Feld intensiver akademischer wie industrieller Forschung geworden. Für beide Anwendungen ist die Nutzung von Antennengruppen vorgesehen, wodurch die benötigte Signalleistung pro Antennenkanal in siliziumbasierten Technologien erreichbar wird. Trotzdem ist das Erreichen der benötigten Ausgangsleistungen mit Leistungsverstärkern in Silizium oder Siliziumgermanium herausfordernd und typischerweise werden diese in III/V Technologien wie Galliumarsenid oder Galliumnitrid realisiert. Um die limitierte Performanz von siliziumbasierten Leistungsverstärkern zu überwinden, werden in dieser Arbeit verschiedene Aspekte der Leistungsverstärkerentwicklung im Millimeterwellenfrequenzbereich untersucht.

Zuerst werden Leistungsverstärker mit einem einzelnen Verstärkerkern, welcher über diskrete LC-Netzwerke angepasst wird, betrachtet. Die Anpassnetzwerke werden auf optimale Topologie und erreichbare Netzwerkeffizienz erforscht. Das Ziel ist die Netzwerkverluste bereits vor der Implementierung genau vorhersagen zu können. In dieser Untersuchung wird der Qualitätsfaktor jeder Netzwerkkomponente in Abhängigkeit ihrer Größe und der gewählten Frequenz modelliert. Das so entwickelte Verfahren findet die maximal zu erwartende Netzwerkeffizienz für jeden Punkt im Smith Diagramm, einschließlich der optimalen Netzwerktopologie an den jeweiligen Punkten. Zwei Leistungsverstärker werden mit der gefundenen optimalen Netzwerktopologie entwickelt. Ein Leistungsverstärker, integriert in einer $130\,\mathrm{nm}$ SiGe Technologie, erreicht bei einer Arbeitsfrequenz von $28\,\mathrm{GHz}$ eine gesättigte Ausgangsleistung von $23.7\,\mathrm{dBm}$ und eine maximale leistungsbezogene Effizienz (PAE) von $40\,\%$. Ein zweiter Leistungsverstärker, integriert in einer $22\,\mathrm{nm}$ FD-SOI CMOS Technologie, erreicht bei $18\,\mathrm{GHz}$ eine maximale Ausgangsleistung von $17\,\mathrm{dBm}$ bei einer PAE

von $45\,\%$. Bei Betrieb mit einem 64-QAM moduliertem Signal erreicht der Leistungsverstärker eine durchschnittliche PAE von $12.5\,\%$. Beide Verstärker sind für ihre jeweiligen Technologien sehr kompakt und benötigen nur eine geringe Chipfläche.

Darauffolgend wird Leistungskombination zur Erhöhung der limitierten Ausgangsleistung von Silizium untersucht. Die am häufigsten eingesetzten Methoden, Transformatoren und Wilkinson-Kombinatoren, werden verglichen. Während Transformatoren für ihre hohe Effizienz und geringen Platzbedarf bekannt sind, ist ihre Nutzbarkeit zur Erzeugung hoher Leistungen bei Millimeterwellen durch geometrische Anforderungen begrenzt. Ein pseudo-differenzieller Leistungsverstärker, bestehend aus einem Transformator mit einem Windungsverhältnis von 2 zu 1 und zwei Verstärkerkernen wird in $130\,\mathrm{nm}$ SiGe BiCMOS entwickelt, um explorativ die Leistungserzeugung mit Transformatoren zu untersuchen. Durch Komplikationen während der Vermessung erreicht der Leistungsverstärker nur eine Ausgangsleistung von $23.7\,\mathrm{dBm}$ bei einer PAE von $26\,\%$. Im Anschluss wird gezeigt, dass Wilkinson-Kombinatoren ohne Isolationswiderstand 16-zu-1 Kombinierung mit Quellimpedanzen im Bereich von $10\,\Omega$ ermöglichen. Bei optimalem Design zeigen diese Kombinatoren eine hohe Effizienz. Im Vergleich zu Transformatoren steigt jedoch der Bedarf an Fläche.

Der Hauptteil dieser Arbeit untersucht den Entwurf der Verstärkerkerne und der dazugehörigen Grenzen bei großer Parallelisierung von Transistoren. Im Rahmen dieser Arbeit wird die Größe der Verstärkerkerne durch die Parallelisierung mehrerer Einheitszellen variiert. Durch die Modellierung der bei dieser Parallelisierung entstehenden parasitären Elemente wird gezeigt, dass für niedrige Impedanzen, zum Beispiel am Eingang oder bei der optimalen Lastimpedanz am Ausgang, die internen parasitären Elemente zu einer Verschlechterung der Performanz führen. Hauptsächlich tragen die notwendigen Leitungsstücke zwischen den Einheitszellen zu dieser Verschlechterung bei. Sowohl ohmsche Verluste in den Leitungssegmenten als auch Variationen in der Belastung der individuellen Einheitszellen verursachen die Reduktion in der Performanz. Eine neue Entwurfsmethode, resonierte Verstärkerkerne, wird vorgestellt, um den Einfluss der parasitären Elemente zu reduzieren. Am Ein- und Ausgang werden parallel geschaltete Induktivitäten so entworfen, dass sie sich mit den parasitären Kapazitäten der aktiven Komponenten in Resonanz befinden und so die lokalen Impedanzen innerhalb des Verstärkerkerns erhöhen. Der Einfluss der Leitungsstücke wird hierdurch minimiert. Unter Nutzung dieser Methode wer-

den Leistungsverstärkerprototypen mit hoher Ausgangsleistung entworfen und demonstrieren neue Rekorde in der Ausgangsleistung. Die finalen Prototypen erreichen bei $28\,\mathrm{GHz}$ jeweils eine gesättigte Ausgangsleistung von $31.7\,\mathrm{dBm}$ und $36.7\,\mathrm{dBm}$. Dies entspricht einer Verbesserung gegenüber vorherigen Veröffentlichungen um 6 bis $10\,\mathrm{dB}$. Die zugehörige PAE beträgt jeweils $36.8\,\%$ und $28\,\%$.

Zum Abschluss wird eine allgemeine Entwurfsmethode für hohe Effizienzen unter modulierter Anregung betrachtet. Um die Verstärkerlinearität ab Anfang des Entwurfsprozess zu berücksichtigen wird Zweitonanregung zur Bestimmung des Arbeitspunktes, Biasnetzwerks und der optimalen Lastimpedanz verwendet. Die PAE bei einem IMD3 von $-25\,\mathrm{dBc}$ wird als Optimierungsmetrik verwendet. Durch Anpassung der Anforderung an IMD3 kann die gewünschte Linearität verändert werden und es wird gezeigt, dass dies die optimale Lastimpedanz verschiebt. Unter Einsatz der eingeführten Methodik wird ein Q-Band Leistungsverstärker in $130\,\mathrm{nm}$ SiGe BiCMOS entwickelt. Bei $40\,\mathrm{GHz}$ wird eine durchschnittliche PAE von $13.2\,\%$ für ein 64-QAM moduliertes Signal demonstriert. Die durchschnittliche Ausgangsleistung beträgt $19\,\mathrm{dBm}$.

Abstract

In pursuit of high data rates for next generation mobile communication infrastructure, e.g. fifth generation mobile communication (5G) and sixth generation mobile communication (6G), and next generation satellite communication, the frequency bands between $10\,\mathrm{GHz}$ and $60\,\mathrm{GHz}$ have become an intensive field of research for both academia and industry. For both applications antenna array configurations are envisioned and thus the required signal power per antenna channel becomes attainable in silicon-based technologies. Still, the required output power levels may be challenging to achieve with complementary metal-oxide-semiconductor (CMOS) or silicon germanium (SiGe) bipolar complementary metal-oxide-semiconductor (BiCMOS) power amplifiers (PAs). Thus integration is typically carried out in compound semiconductor technologies (III-V), such as gallium arsenide (GaAs) and gallium nitride (GaN). To overcome the limited performance of silicon PAs, this work investigates various aspects of PA design at millimeter-wave (mmWave) frequencies.

Initially, single core PAs matched by lumped LC-networks are explored. The matching networks are studied for optimal network topologies and for achievable network efficiency. The goal is to enable accurate prediction of network efficiency before implementation. In this study, each network component's quality factor is modelled depending on component value and frequency of operation. The study yields the maximum expected network efficiency for $|\Gamma| < 0.9$ in a Smith chart normalized to $50\,\Omega$ accurately, including the best network topology for each point. Two PAs are then designed according to the best network topology. A first PA, integrated in $130\,\mathrm{nm}$ SiGe BiCMOS, achieves a medium saturated output power of $23.7\,\mathrm{dBm}$ and a peak power-added efficiency (PAE) of $40\,\%$ at $28\,\mathrm{GHz}$. A second PA integrated in $22\,\mathrm{nm}$ FD-SOI CMOS achieves a saturated output power of $17\,\mathrm{dBm}$ with a PAE of $45\,\%$ and an average modulated PAE of $12.5\,\%$ for a 64-quadrature amplitude modulation (QAM) signal at $18\,\mathrm{GHz}$. Both PAs are among the most area efficient designs in their respective technologies, thus being especially interesting for large antenna arrays.

In the following the focus is shifted towards increasing the limited output power of silicon using power combiners. The most used methods, transformers and Wilkinson combiners, are compared. While transformers are very efficient and compact power combiners, at mmWave frequencies their use to deliver high output power in silicon is limited by geometric constraints. A pseudo-differential PA using a transformer with a turn ratio of 2-to-1 is presented in $130\,\mathrm{nm}$ SiGe BiCMOS to explore power combining with transformers, but due to complications during the measurement the PA only achieves $23.7\,\mathrm{dBm}$ of output power at a PAE of $26\,\%$. Next, Wilkinson combining, without isolation resistor, is shown to enable 16-to-1 combination without significantly limiting the source impedance range. When optimally designed, the combiners show high efficiency, however the area consumption is increased compared to transformers.

The main part of this work investigates power amplifier core design and the limits of large device parallelization. Throughout this work the size of a device inside a PA core is varied by parallelizing multiple unit cells. By modelling the parasitics created by this parallelization, it is shown that for low impedances inside the core, for example input and load-pull impedance, the internal parasitics inside the core reduce the PA core performance. This reduction is mainly caused by the necessary line segments between the unit cells. Both ohmic loss of the line segments and variation in the loading of individual unit cells cause performance degradation. A novel design method, the resonated amplifier core, is introduced to reduce the impact of parasitics. Shunt inductors at input and output of the core, designed to be in resonance with the parasitic capacitors, are used to increase the local impedances and thus reduce the effect of the line segments. Multiple optimization steps are presented to refine the design method to improve performance. Using these methods high power SiGe BiCMOS PA prototypes are developed and demonstrate record breaking output power. The final designs achieve saturated output power levels of $31.7\,\mathrm{dBm}$ and $36.7\,\mathrm{dBm}$ at $28\,\mathrm{GHz}$, improving upon state of the art by 6 to $10\,\mathrm{dB}$. The corresponding PAE is $36.8\,\%$ and $28\,\%$, respectively.

Lastly, a general design method aiming for high modulated efficiency is explored. To consider a PA's linearity from the start of the design, two-tone excitation is used to find the operating point, bias network and load-pull impedance. PAE for a third order intermodulation distortion (IMD3) of $-25\,\mathrm{dBc}$ is used as the metric for optimization. By shifting the requirement for IMD3 the desired linearity can be adjusted, and the optimal load-pull impedance is shown to vary

depending on the desired value of IMD3. Using the introduced method a Q-band PA prototype in $130\,\mathrm{nm}$ SiGe BiCMOS is developed. It achieves $13.2\,\%$ average PAE for a 64-QAM signal. The average output power is $19\,\mathrm{dBm}$.

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Alexander Haag

Contents

Acronyms and symbols

Acronyms

5G	fifth generation mobile communication
6G	sixth generation mobile communication
AC	alternate current
ACPR	adjacent channel power ratio
ADS	Advanced Design System
Al	aluminum
APSK	amplitude and phase-shift keying
AWG	arbitrary waveform generator
BEOL	back end of line
BER	bit error rate
BiCMOS	bipolar complementary metal-oxide-semiconductor
CB	common-base
CE	common-emitter
CG	common-gate
CS	common-source
Cu	copper

CMOS	complementary metal-oxide-semiconductor
DAT	distributed active transformer
DC	direct current
DPA	Doherty power amplifier
DUT	device under test
EC	equivalent circuit
EIRP	effective isotropic radiated power
EM	electromagnetic
ESD	electrostatic discharge
EVM	error vector magnitude
FD-SOI	fully depleted silicon on insulator
FEOL	front end of line
FET	field effect transistor
FSPL	free-space path loss
GaAs	gallium arsenide
GaN	gallium nitride
GF	GlobalFoundries
GND	ground
HB	harmonic balance
HBT	heterojunction bipolar transistor
HEMT	high-electron-mobility-transistor
HPA	high power amplifier

IC	integrated circuit
IHE	Institute of Radio Frequency Engineering and Electronics
IHP	Leibniz Institute for High Performance Microelectronics
IL	insertion loss
IM3	third order intermodulation product
IMD3	third order intermodulation distortion
IMN	input matching network
KIT	Karlsruhe Institute of Technology
LEO	low earth orbit
LMBA	Load Modulated Balanced Amplifier
MIM	metal-insulator-metal
mmWave	millimeter-wave
MoM	metal-oxide-metal
MPA	medium power amplifier
NF	noise figure
OFDM	orthogonal frequency-division multiplexing
OMN	output matching network
PA	power amplifier
PAE	power-added efficiency
PAPR	peak-to-average power ratio
PCB	printed circuit board
PD	power density

Q	quality factor
QAM	quadrature amplitude modulation
RADAR	radio detection and ranging
RF	radio frequency
RFIC	radio frequency integrated circuit
RMS	root mean square
SatCom	satellite communication
SEE	single event effects
SRF	self-resonant frequency
Si	silicon
SiGe	silicon germanium
SNR	signal-to-noise ratio
TID	total ionizing dose
TL	transmission line
TX	transmitter
UC	unit cell
UCS	unit cell segment

Frequently used symbols

BW	Bandwidth
BV_{CEO}	open-base breakdown voltage
BV_{CBO}	open-emitter breakdown voltage

f	Frequency
ω	Angular frequency
L_{E}	Emitter length
P	Power
P_{out}	Output power
P_{sat}	Saturated output power
λ	Wavelength
φ	Phase shift
T	Temperature
V_{knee}	Knee voltage
Z_{in}	Input impedance
Z_{L}	Load impedance
Z_{LP}	Load-pull impedance
Z_{out}	Output impedance
Z_{S}	Source impedance
Z_0	Characteristic impedance

Constants

$\pi = 3.141\,59$	PI
$k_{\mathrm{B}} = 1.38 \times 10^{-23}\,\mathrm{J/K}$	Boltzmann's constant
$c = 299\,792\,458\,\mathrm{m/s}$	speed of light in vacuum

1 Introduction

In recent years, a strong push towards higher frequencies for communication and radio detection and ranging (RADAR) applications could be seen in academia, as well as industry. The introduction of 5G at frequencies up to 6 GHz and on-going research endeavors for the 5G FR2 bands around 28 GHz [3GP24], automotive radar at 76 to 81 GHz [HTS+12] as well as on-going research towards 6G [IYK+21] and low earth orbit (LEO) satellite constellations [ACC+23] highlight the need for continued innovation in radio frequency integrated circuit (RFIC) design. Significant advances in silicon-based technologies now enable the integration of entire high frequency systems on a single silicon (Si) chip, including digital and mixed-signal components. This is especially interesting due to a reduction in cost and packaging complexity. However, the technological advances improving the achievable transistor speeds usually come at the cost of reduced nominal supply voltages for the active devices. One important high frequency component, which is especially affected by a reduction in supply voltage, is the power amplifier (PA). PAs are a necessity in any radio frequency (RF) and mmWave system, as they provide the required signal power in either RADAR detection or communication applications. Additionally, PAs typically dissipate the most power in a transmitter, or possibly the entire transceiver, and thus their efficiency dominates the overall efficiency of the system. Fig. 1.1 illustrates a basic block diagram of an integrated transmitter chain, including a mixer, phase shifter and the PA, as well as a qualitative representation of signal strength.

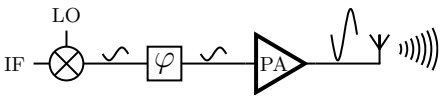


Figure 1.1: Basic transmitter chain including a mixer, phase shiter (PS), PA and antenna.

Two application scenarios envisioned at K_a-band frequencies are mobile communication and LEO satellite communication (SatCom). In Fig. 1.2 a SatCom scenario and a simplified beamforming transmitter block diagram are depicted. In the past, the stringent requirements on the performance of PAs mandated the usage of III/V technologies such as GaN or GaAs when targeting mmWave frequencies. This previously prevented the integration of a full system in a single chip. However, compared to classical transceiver architectures with just a single PA, the introduction of phased array architectures in numerous applications reduces the required output power per PA and enables the integration of entire systems in CMOS or SiGe BiCMOS technologies.

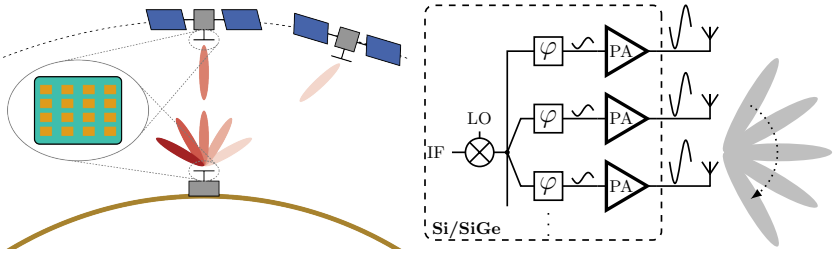


Figure 1.2: Example applications for CMOS and SiGe BiCMOS PAs: a) LEO SatCom and b) beamforming transmitters.

In Fig. 1.3 the required output power per PA versus the number of antenna channels is depicted for different total effective isotropic radiated power (EIRP) values. The transmitter architecture is assumed as previously shown in Fig. 1.2b. For the calculation a unit element antenna gain, G_unit, of $4\,\mathrm{dBi}$ and a power margin, M, of $4\,\mathrm{dB}$ for large scan angles are assumed. The PA output power, $P_\mathrm{PA,dBm}$, is calculated using

$$P_\mathrm{PA,dBm} = \mathrm{EIRP}_\mathrm{dBW} + 30 + M_\mathrm{dB} - G_\mathrm{unit,dBi} - 20 \cdot \log\left(n\right) \qquad (1.1)$$

with n being the number of channels in the array.

Given enough elements within an array the required output power per PA can be reduced. For example, to achieve $40\,\mathrm{dBW}$ in a 1024-element array, an individual PA must output around $10\,\mathrm{dBm}$, which is feasible in silicon. Additionally, an important parameter is direct current (DC) power consumption. In Fig. 1.4a the

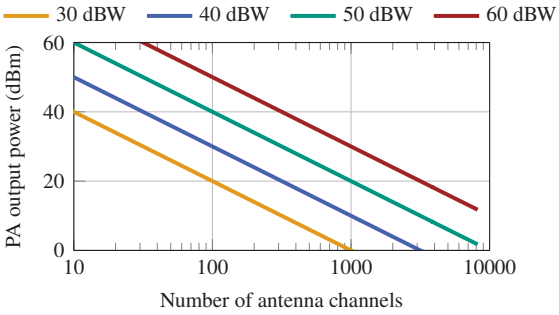


Figure 1.3: Required output power per PA versus number of antenna elements to achieve a target EIRP.

cumulative DC power consumption of all PAs within a transmitter is shown over the number of channels in the transmitter. The power consumption is calculated with

$$P_{\mathrm{DC,PA}} = \frac{P_{\mathrm{PA,W}}}{\eta} \cdot n. \tag{1.2}$$

Independent of the output power per PA a constant efficiency, η, of $25\,\%$ is used. By increasing the size of the array and reducing the output power per PA the cumulative DC power consumption of all PAs is reduced. However, this calculation assumes that the PAs dominate the overall power consumption. When the arrays become larger and the output power per PA is reduced this assumption is no longer valid and the power consumption of the other components, e.g., the phase shifters, becomes relevant. Fig. 1.4b shows the transmitter power consumption over the number of channels when a power consumption of $40\,\mathrm{mW}$ is added per channel, to model the power consumption of other components. Depending on the target EIRP values different optimum transmitter sizes are obtained for which the DC power consumption is minimized. For the given example values the optimum array size for an EIRP of $40\,\mathrm{dBW}$ is around 1024 elements, corresponding to a PA output power of approximately $10\,\mathrm{dBm}$. Similarly, for a target EIRP of $30\,\mathrm{dBW}$ the PA output power for the optimum array size of 300 is $10\,\mathrm{dBm}$.

In Fig. 1.5, the optimum output power per PA to minimize power consumption is shown versus EIRP of the transmitter. Using a maximum number of channels, n_{max}, of 4096 as the base case, the optimum PA output power remains around $10\,\mathrm{dBm}$ until an EIRP of $52\,\mathrm{dBW}$. For higher EIRP values, the array would have

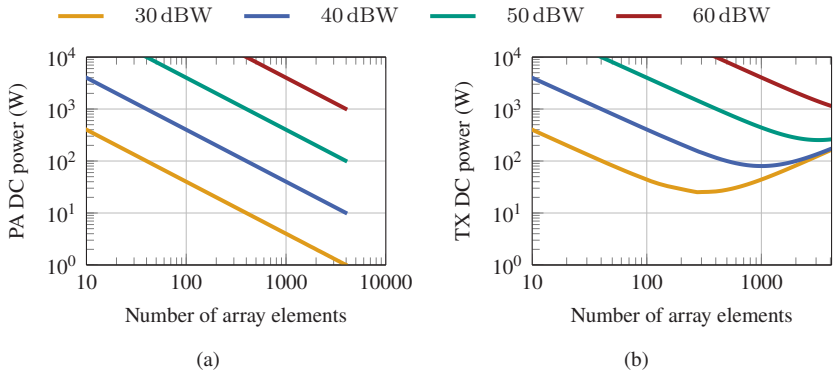


Figure 1.4: Transmitter DC power consumption for different EIRP values: a) only PA power consumption and b) system power consumption.

to be larger than 4096 elements and thus the output power per PA increases. Additionally, the same results are plotted when the efficiency of the PAs is increased to 40 %. Except for an increase in the optimum output power per PA at lower EIRP values, the trend remains the same. Lastly, the optimum PA output power for a maximum array size of 1024 is shown. For this case, the rise in output power per PA starts at an EIRP of 40 dBW. Following this analysis a larger number of channels in the array is expected to be more efficient, however, so far other factors such as physical size of the array and feasibility have been neglected. In contrast, typical phased arrays reported in [ACC+23] only feature element numbers up to 1024 and thus PA output power may range between 10 to 30 dBm for the analysed EIRP range of 30 to 60 dBW.

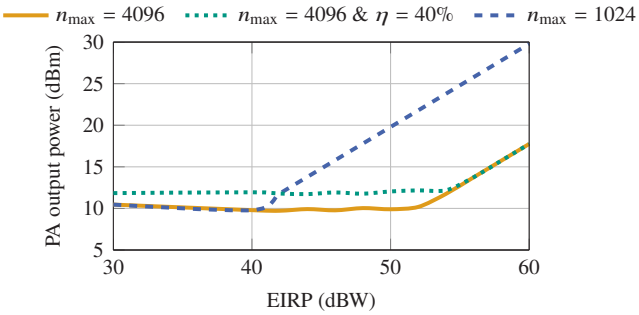


Figure 1.5: Optimum PA output power versus transmitter EIRP to minimize DC power consumption.

An example application at K_a-band are LEO satellites, which in comparison to geostationary communication satellites, are only visible for several minutes per flyover. Both the satellite and user terminal have to align their antenna beams for successful communication. This can either be done mechanically or electronically using the previously discussed phased arrays, with the latter being the preferred option [ACC+23]. Similarly, for future mobile communication multiple simultaneous beams and beam steering are envisioned. With the prospect of using antenna arrays in future communication and radar systems, PA design in CMOS or SiGe BiCMOS technologies remains a key challenge of integrated circuit (IC) design.

However, even with reduced requirements, the development of PAs at these frequencies is challenging in silicon-based technologies. Power requirements may range between $10\,\mathrm{dBm}$ to $30\,\mathrm{dBm}$ per channel, and especially the upper end is beyond what state of the art can produce with a peak efficiency above $20\,\%$ [WNP16, ELM14]. This work investigates fundamental design methods to increase the delivered power of CMOS or SiGe BiCMOS PAs at mmWave frequencies in pursuit of eliminating the expensive GaN or GaAs devices.

1.1 Power Amplifiers for Satellite Communication

As an example, potential requirements imposed on PAs for LEO SatCom at K_a-band frequencies are analyzed in the following. Fig. 1.6 visualizes the targeted frequency bands for two known LEO SatCom satellite constellations, Starlink and Telesat [ACC+23, VD19], and potential future space applications [VD19, LHHJ24]. Additionally, the frequency bands for 5G FR2 from 24.5 to $29.5\,\mathrm{GHz}$ [3GP24] and 6G FR3 are indicated. The frequency band around $28\,\mathrm{GHz}$ is actively pursued for both SatCom and mobile communication and is thus selected as one of the primary bands of interest for this work.

As previously indicated, antenna arrays are envisioned for these operations. By introducing antenna arrays, especially for LEO SatCom, the ability to electronically steer the beam during satellite flyover is a significant advantage. A first estimate of the required output power per PA can be calculated from the maximum EIRP, which is specified to be $39\,\mathrm{dBW}$ for Telesat with a maximum

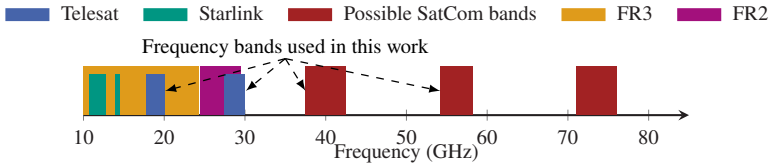


Figure 1.6: Frequency bands for LEO SatCom, 5G FR2 and 6G FR3.

antenna gain of 38 dB. This results in a total transmitted power of 31 dBm for the satellite. Similar numbers are expected for ground stations. When this transmitted power is divided into, for example, 256 antenna elements, each antenna channel has to be provided with around 7 dBm. However, this assumes only a single antenna beam and no attenuation due to a high beam angle. Assuming that multiple simultaneous beams and high beam angles should be serviced with this EIRP per beam, the transmit power per antenna grows by several decibels to around 15-20 dBm. For communication purposes this is not the saturated output power, but rather the required power at back-off. Thus, the saturated power requirement per PA under these conditions may be in the range of 25-30 dBm. As an example, throughout this work different QAM constellations, such as 64- and 256-QAM, are used to verify average PA performance for a communication scenario. For SatCom amplitude and phase-shift keying (APSK) constellations are also used [ETS24, ACC+23]. While QAM exhibits a higher peak-to-average power ratio (PAPR) compared to APSK for similar constellations, QAM is more frequently used in mobile communication, literature and thus more suitable when comparing performance.

Depending on the specific application, the EIRP requirements might be as high as 78 dBW [VD19]. Even for a 4096 (64x64) element antenna array, with an assumed antenna element gain of 9 dBi a total transmitted power of 63 dBm is required. Not accounting for additional losses, this results in a linear power requirement of 26.9 dBm per antenna channel.

While on the satellite payloads GaN-based high power amplifiers (HPAs) are preferable due to their higher efficiency [GPCC23] and power capability, CMOS and SiGe BiCMOS are a promising option for ground stations, user terminals and as driver amplifiers, if the required power levels can be met with a suitable efficiency.

1.2 State-of-the-art CMOS and SiGe BiCMOS Power Amplifiers

In Fig. 1.7a the saturated output power versus frequency of a collection of state-of-the-art CMOS and SiGe BiCMOS PAs [WEA$^+$] is presented. The figure only includes integrated PAs without off-chip combiners. For a frequency range around 28 GHz, indicated in the figure, only one publication reaches a power level beyond 30 dBm. Most of the PAs achieve a saturated output power in the range of 20 to 28 dBm. However, when the associated PAE is presented versus the saturated output power for the PAs within the indicated frequency range, the PAE significantly declines for the larger PAs. Around 30 dBm the peak PAE is at or below 17 %.

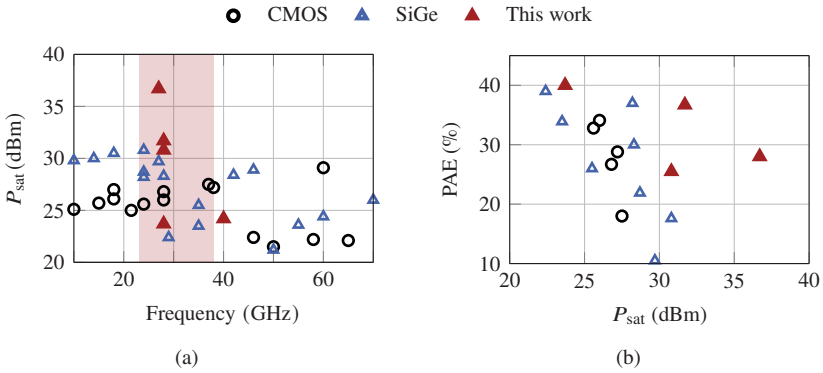


Figure 1.7: State-of-the-art silicon PAs [WEA$^+$]: a) saturated output power w.r.t. frequency from 10-70 GHz and b) PAE w.r.t. saturated output power for the indicated frequency range.

Furthermore, both SiGe BiCMOS PAs achieving 29 and 30.8 dBm utilize impractically high supply voltages beyond 5 V to achieve this performance. For faster heterojunction bipolar transistor (HBT) technologies, this is impossible. The high voltages in [ELM14, WNP16] are possible due to the slower HBTs (integrated in 0.25 and 0.35 µm CMOS nodes) used in these publications.

In [ELM14] a cascode configuration consisting of a faster low voltage HBT as the common-emitter (CE) device and a slower high voltage HBT as the common-base (CB) device is used to increase gain, breakdown voltage and the

optimum load impedance. A total of 8 PA cores are then combined through a power combiner consisting of a combination of transmission lines (TLs) and lumped components. For a $50\,\Omega$ load a combiner insertion loss of $2.4\,\mathrm{dB}$ is reported. During characterization, a saturated output power of $29.7\,\mathrm{dBm}$ for a supply voltage of $6.55\,\mathrm{V}$ is presented. By load-pulling the reported PA and presenting a load impedance of $(21.2 - 18\mathrm{j})\,\Omega$ to the PA instead of $50\,\Omega$, the saturated output power is improved to $31\,\mathrm{dBm}$ for a supply voltage of $6.9\,\mathrm{V}$. The PAE ranges from 10.2-$13\,\%$ in these cases.

In [WNP16] a high power signal source is presented, consisting of a voltage-controlled oscillator and a two-stage PA. The last stage consists of four differential PA cores. Each core is comprised of a differential cascode and a matching network, which presents the optimal impedance to the core given a $50\,\Omega$ load. The pre-matched cores are then combined through lumped $50\,\Omega$ Wilkinson combiners and interfaced differentially at the output. At $24\,\mathrm{GHz}$, the PA delivers a saturated output power of $30.8\,\mathrm{dBm}$ with a corresponding peak PAE of $17.6\,\%$ for a supply voltage of $5.8\,\mathrm{V}$.

While these example PAs in SiGe BiCMOS use Wilkinson power combining, CMOS PAs typically utilize transformer-based combining. As an example, in [HLLW18] a PA in $90\,\mathrm{nm}$ CMOS with a saturated output power of $26\,\mathrm{dBm}$ is presented. This is among the highest power levels reported in CMOS at $28\,\mathrm{GHz}$. The PAE is $34\,\%$ for a supply voltage of $2.4\,\mathrm{V}$. The PA consists of two differential PA cores, which are comprised of a cascode architecture and neutralization capacitors at the common-source (CS) device, as well as an additional neutralization network across the drain and source of the common-gate (CG) device. The cores are then combined through a transformer-based network.

The presented state of the art highlights the necessity of improvements to the design methods of silicon-based PAs at higher power levels. While PAE in the CMOS example is higher compared to the SiGe examples, the saturated output power falls short of $30\,\mathrm{dBm}$. The SiGe examples achieve up to $30\,\mathrm{dBm}$, but at lower efficiency. All presented examples utilize a cascode structure to improve output voltage swing, but the choice of the combining network architecture and details of the PA core design differ, and no efficient solution is available.

1.3 Power Amplifier Terminology

Within the context of this thesis, the structure of a PA is described as shown in Fig. 1.8. Starting at the left of Fig. 1.8, the smallest building block termed a unit cell (UC) is shown. It consists of active devices, e.g., in common-emitter or cascode configuration, with a fixed device size. Additionally, components such as resistors and capacitors could be integrated with the active devices. A PA core contains several unit cells directly connected in parallel. UCs are repeated to scale the total device size within the PA core and the core is then used as a single functional block within the design. The unit cell approach is chosen to enable convenient scaling of the PA core size. Depending on the architecture of the PA, it may consist of a single PA core directly matched to the desired system impedance through an output matching network (OMN) and input matching network (IMN) or multiple PA cores, which are interfaced through a power splitting and power combining structure. The power splitter and combiner differ from direct parallelization by including impedance transformation, e.g., transformers or transmission lines.

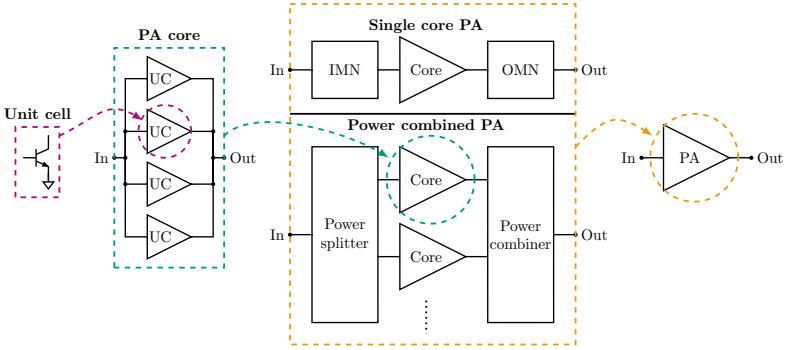


Figure 1.8: Power amplifier structure.

1.4 CMOS and SiGe BiCMOS Technologies

In this work four different technologies are used for PA design. Three of those technologies are $130\,\mathrm{nm}$ SiGe BiCMOS technologies from the Leibniz Institute for High Performance Microelectronics (IHP), namely SG13G2, SG13G2Cu and SG13G3Cu. Both G2 technologies share the same front end of line (FEOL), including the HBT devices. The HBTs offer f_T and f_max in the range of $350\,\mathrm{GHz}$ and $450\,\mathrm{GHz}$, respectively. The G3 technology provides improved HBT performance in its FEOL with f_T and f_max in the range of $470\,\mathrm{GHz}$ and $650\,\mathrm{GHz}$. The used back end of line (BEOL) is the same in the G2Cu and G3Cu technologies but differs from the SG13G2 technology. The fourth technology is GlobalFoundries (GF)' $22\,\mathrm{nm}$ CMOS fully depleted silicon on insulator (FD-SOI) technology, providing field effect transistors (FETs) with f_T and f_max in the range of $350\,\mathrm{GHz}$ and $370\,\mathrm{GHz}$. All technologies provide sufficient transistor speed for the frequency bands between $20\,\mathrm{GHz}$ to $80\,\mathrm{GHz}$ targeted within this work. A summary is provided in table 1.1.

Table 1.1: Summary and comparison of CMOS and SiGe BiCMOS technologies used in this work.

Tech.	SG13G2 SiGe BiCMOS	SG13G2Cu SiGe BiCMOS	SG13G3Cu SiGe BiCMOS	22 nm FD-SOI CMOS
f_max (GHz)	450	450	650	370
f_T (GHz)	350	350	470	350
$BV_\mathrm{CEO}/V_\mathrm{GS,max}$ (V)	1.6	1.6	≈1.5	0.8
Num. of metal layers	7	8	8	11

For the integration of passive structures and to contact the active devices the available metal layers in the BEOL are used. The composition of the layers influences the achievable performance. Fig. 1.9 illustrates the usable metal layers in the BEOL of the respective technologies. The illustrations are intentionally not to scale for propriety reasons, however the relative scale between the stacks is preserved. SG13G2 offers a total of 7 aluminum (Al) layers, of which the top two layers are thicker. To provide a ground connection the lower metal layers, M1 to M3, are stacked together, shielding the lossy Si substrate. TopMetal1 and TopMetal2 are then used for signal routing. SG13G2Cu provides 6 copper (Cu) layers and two Al layers. The lower Cu layers, M1-M3, are again

used as ground. Signal routing is possible in the thick Cu layers and in the top metal layer, ThickAl. This BEOL provides two advantages in comparison to the Al BEOL of the SG13G2 process. First, by providing three thick layers handling of large currents is simplified and secondly, the overall stack height is larger reducing losses and coupling to the lossy Si substrate. Lastly, the BEOL used in the 22 nm FD-SOI process is presented in Fig. 1.9c. It provides 6 thin metal layers, M1-M6, which are used to contact the transistors, but are too lossy for RF routing. Instead, M1-M7 are used as ground. By utilizing the first thicker metal the ground provides sufficient conductivity. Again, three thicker metal layers are available, of which two are Cu layers. Similar to SG13G2Cu, this BEOL enables better current handling capabilities and a larger total stack height.

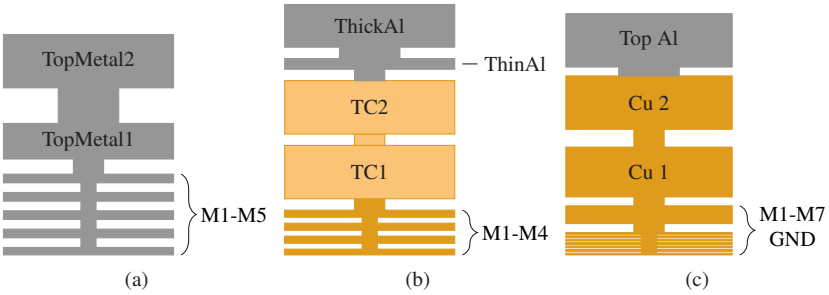


Figure 1.9: BEOL illustrations for: a) IHP's SG13G2; b) IHP's SG13G2Cu/SG13G3Cu and c) GF's 22 nm FD-SOI. Illustrations are not to scale.

1.5 Thesis Goal and Outline

The goal of this thesis is to investigate fundamental PA design challenges at mmWave frequencies. A core part is developing and refining design techniques for optimization of CMOS and SiGe BiCMOS PAs at mmWave frequencies.

The first focus topic are efficient matching and power combining networks for highly parallelized transistor configurations. The target impedances to be matched are as low as 10 Ω. Both LC-based matching for PAs with a single core and large TL-based power combining networks with up to 16 inputs are explored.

The main focus area is then set on device parallelization within the PA cores. The cause of PA core performance degradation during large device parallelization is analyzed and a method to improve performance in largely parallelized cores is introduced. This is pursued to enable efficient PAs beyond a saturated output power of $30\,\mathrm{dBm}$.

Finally, an optimization method targeted at linear PAs is presented to bridge the gap from peak performance optimization to back-off optimization in communication scenarios.

2 Power Amplifier Basics

Parts of the following chapter are based on and similar to content presented in [Cri06].

A power amplifier's main objective is to deliver a specific output power into a load. The level of output power is determined by the respective application. The signal power, P, into a load depends on the amplitude of incident current, I_{out}, and amplitude of the voltage, V_{out}, across the load, as

$$P = \frac{1}{2}\Re\left\{V_{\mathrm{out}} \cdot I_{\mathrm{out}}^{*}\right\}. \tag{2.1}$$

The voltage and current swing have to be provided by transistors operating as amplifiers. Important concepts of power amplification can be illustrated by observing the characteristics of a simplified and idealized representation of a transistor, as is shown in Fig. 2.1a. For simplicity only a bipolar device is

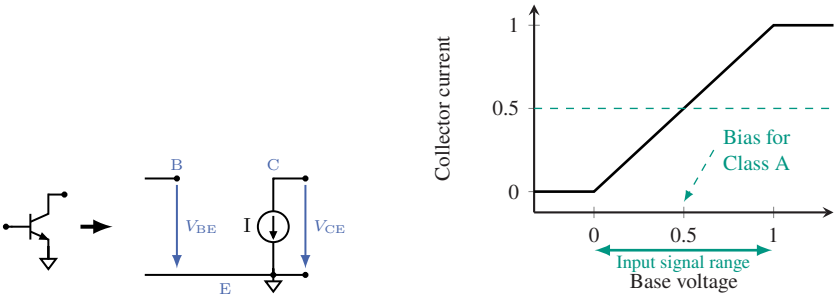


Figure 2.1: Idealized device characteristics for a transistor: a) ideal device model and b) idealized DC characteristic.

depicted, but for this analysis FET and bipolar transistors are identical. The transistor is modelled by a voltage controlled current source with a perfectly linear direct current (DC) characteristic within its operating limits, shown in Fig. 2.1b with normalized parameters. It is assumed that the transistor operation is permissible up to a maximum voltage, V_{max}, across collector and emitter and a maximum collector current, I_{max}. Both parameters are technology dependent. For simplification, no minimum voltage at the output, such as the knee voltage, V_{knee}, is required and ideal loading conditions are assumed. The resulting idealized output DC IV curve is depicted in Fig. 2.2.

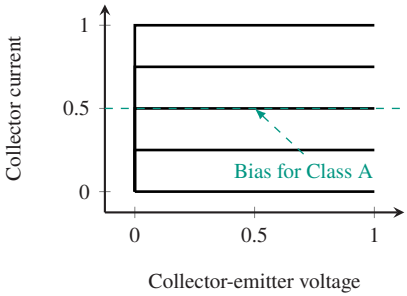


Figure 2.2: Idealized output DC IV curve.

Under these conditions the theoretical concept of class A operation can be achieved by biasing the transistor at the operating point of $V_{\mathrm{CE,max}}/2$ and $I_{\mathrm{C,max}}/2$. If the input signal drives the transistor to the limits, but not beyond a normalized base voltage of 0 or 1, the input signal is linearly amplified, illustrated in Fig. 2.3 for a sinusoidal excitation.

In this case, the output voltage and current swing have an amplitude of V_{DC} and I_{DC}, respectively. Thus, the output power, P_{out} is calculated to be

$$P_{\mathrm{out}} = \frac{1}{2} V_{\mathrm{DC}} \cdot I_{\mathrm{DC}} \tag{2.2}$$

and the dissipated DC power, P_{DC} is

$$P_{\mathrm{DC}} = V_{\mathrm{DC}} \cdot I_{\mathrm{DC}}. \tag{2.3}$$

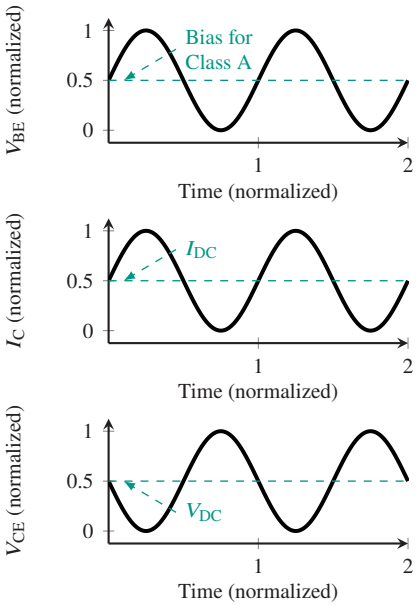


Figure 2.3: Idealized class A operation.

By dividing the RF output power by the dissipated DC power, the PA's efficiency is calculated, and for the idealized case of the class A amplifier a theoretical efficiency, $\eta = P_{\mathrm{out}}/P_{\mathrm{DC}}$ of $50\,\%$ is possible. This aspect of PA design is important. In a real amplifier, it is typically referred to as drain or collector efficiency, $\eta_{\mathrm{D,C}}$ and defined as

$$\eta_{\mathrm{C}} = \frac{P_{\mathrm{RF,out}}}{P_{\mathrm{DC}}}. \tag{2.4}$$

A more meaningful approach to define efficiency for realistic circuits with limited gain is to subtract the required RF input power, $P_{\mathrm{RF,in}}$, from the delivered output power yielding the power-added efficiency (PAE)

$$\mathrm{PAE} = \frac{P_{\mathrm{RF,out}} - P_{\mathrm{RF,in}}}{P_{\mathrm{DC}}}. \tag{2.5}$$

A theoretical efficiency higher than $50\,\%$ can be achieved by reducing the base bias voltage, which reduces the DC current consumption. As a consequence, parts of the output waveform are truncated. The three conventional modes beyond class A are class AB, B, and C. A typical way to differentiate between these classes is to use the conduction angle, α, for which the transistor is conducting current. Conduction angle and theoretical efficiency limits are summarized in table 2.1 and idealized current waveforms are shown in Fig. 2.4. While in theory a higher efficiency is achieved, a lower bias point generates significant harmonic content due to the truncation of the output sine wave, and for the theoretical analysis an ideal short is assumed as the harmonic termination. Additionally, the theoretical signal power beyond class B deteriorates, resulting in higher efficiency at the cost of lower output signal strength and the required driving power is significantly increased (up to $6\,\mathrm{dB}$ for class B). When this is taken into account PAE may not improve accordingly in practical cases.

Table 2.1: Summary of theoretical performance for basic classes of operation.

Class	A	AB	B	C
Conduction angle α	2π	π - 2π	π	0 - π
Theoretical efficiency η (%)	50	50 - 78.5	78.5	78.5 - 100

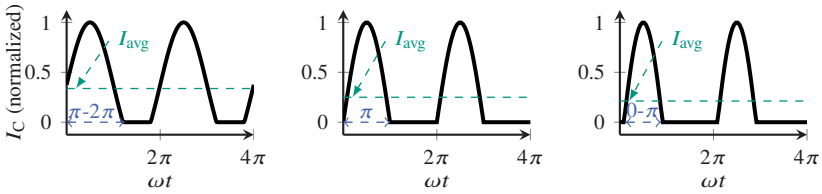


Figure 2.4: Ideal current waveforms for theoretical classes of operation: a) class AB; b) class B and c) class C.

At mmWave frequencies, generating sufficiently large output power remains one of the major challenges for PA design in CMOS and SiGe BiCMOS technologies. This is mainly attributed to the low open-base breakdown voltage, BV_{CEO}, limiting the possible voltage swing across a basic transistor setup,

as presented before. The maximum output power that can be delivered by the idealized transistor is

$$P_{\max} = \frac{1}{2} \frac{V_{\mathrm{CE,max}}}{2} \cdot \frac{I_{\mathrm{C,max}}}{2}. \tag{2.6}$$

The corresponding load resistor, R_{opt}, is calculated using the load-line method [Cri06]. The load impedance is selected such that the maximum voltage swing is reached at maximum current swing. In the case of the previously presented ideal transistor, this is

$$R_{\mathrm{opt}} = \frac{V_{\mathrm{CE,max}}}{I_{\mathrm{C,max}}}. \tag{2.7}$$

Since the theoretical limit for the amplitude of the output voltage swing, V_{peak}, is equivalent to the supply voltage or half the maximum collector emitter voltage, this limits what a transistor can deliver into a load resistor, as

$$P = \frac{1}{2} \frac{V_{\mathrm{peak}}^2}{R}. \tag{2.8}$$

For a conventional load resistance of $50\,\Omega$ and a supply voltage of $1.5\,\mathrm{V}$ this amounts to approximately $13\,\mathrm{dBm}$. To further extend the output power the optimal load resistance must be lowered. At the same time, the active device size needs to be increased to provide sufficient current swing. When a saturated output power of $30\,\mathrm{dBm}$ is targeted the optimal load resistance is calculated to be $1.1\,\Omega$, by rearranging equation 2.8 to

$$R = \frac{1}{2} \frac{V_{\mathrm{peak}}^2}{P}. \tag{2.9}$$

At mmWave, a load resistance this low is susceptible to parasitics and incurs high losses inside the matching network. This will reduce the amplifier's efficiency.

2.1 Transistors, Topologies and Challenges for Millimeter-Wave Silicon Power Amplifiers

A more realistic model of an HBT operating at mmWave frequencies is presented in Fig. 2.5. Parasitic capacitors at input and output reduce the impedances of the transistors, even for relatively small transistor sizes. Low impedances increase the influence of parasitics and result in higher matching network loss. A feedback path is introduced into the circuit by the collector-base capacitor, C_{BC}. During operation with high voltage gain, which is desirable for PAs, this capacitor's effect on the input is enhanced by the Miller effect. Parasitic resistors, introduced by the device contacts, directly affect transistor performance and prevent perfect compensation of the internal device capacitors by resonating inductors. Transistor performance is thus reduced with increasing frequency. Lastly, the transistor's output current as a function of V_{BE} is generally not linear, but either exponential for HBTs or quadratic for FETs [Sze81].

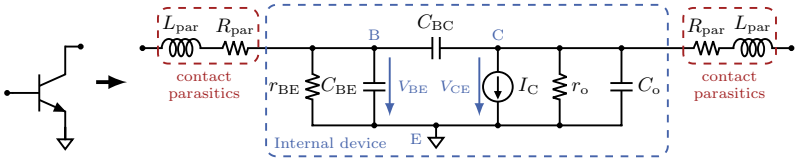


Figure 2.5: Simplified high-frequency transistor model.

The enhanced Miller effect of transistors in a basic CE configuration is one of the reasons, which makes more advanced amplifier topologies preferable. The two most prevalent topologies are neutralized differential pairs and the cascode, or a combination of both, e.g., in [LW23, WW20b, WWW20]. Additionally, transistor stacking, often used [DHG+13] with FETs, allows for higher voltage swing. The first two options are displayed in Fig. 2.6.

The neutralized differential pair contains neutralization capacitances to compensate the feedback from the output back to the input. However, it is not pursued further throughout this work, as the implementation of the neutralization capacitors for large device peripheries is challenging and restricts the layout geometry. The cascode adds a second device in CB configuration, which provides a low load impedance to the CE stage. The CE's voltage gain is thus decreased, ideally to 1, and the feedback due to the collector-base ca-

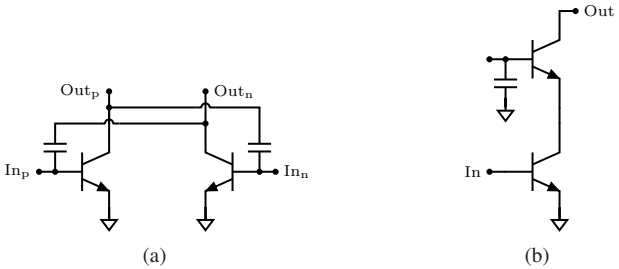


Figure 2.6: Advanced transistor arrangements for power amplification: a) neutralized differential pair and b) cascode.

pacitance reduced. The cascode provides additional advantages over a simple CE configuration, such as higher input impedance, higher output impedance combined with higher gain, increased optimal load impedance and increased voltage swing. While a CE is limited by BV_{CEO}, the CB device is limited by the open-emitter breakdown voltage, BV_{CBO} [ORW+15, CSC+11]. A $130\,\mathrm{nm}$ SiGe technology used throughout this work features a BV_{CEO} of $1.6\,\mathrm{V}$ and a BV_{CBO} of $4.8\,\mathrm{V}$. Following [ORW+15], the CB device can be operated with a collector-base voltage, V_{CB}, of $2.4\,\mathrm{V}$ ($BV_{\mathrm{CBO}}/2$) and during compressed operation RF swing across collector and emitter is allowed slightly beyond BV_{CBO}. To allow for operation close to the optimal value of BV_{CBO} the upper base must have a low ohmic termination. When the transistor is biased beyond BV_{CEO} current reversal into the base would otherwise increase the voltage inside the device's base. This could lead to localized current increase inside the device, leading to a further increase of base voltage. This could lead to the destruction of the device. The analysis in [ORW+15] did not account for mutual heating of the CE and CB device. Hence, appropriate measures, such as resistive emitter degeneration, ballasting or bias circuits, are required to stabilize the current set by the CE device. Using an idealized cascode arrangement with an assumed voltage swing amplitude of $3.5\,\mathrm{V}$ and an optimal load resistor of $50\,\Omega$ an output power of $20.8\,\mathrm{dBm}$ is possible. Still, to achieve $30\,\mathrm{dBm}$ of output power, a low load resistance of $6.1\,\Omega$ is required.

In a realistic high-frequency scenario, transistors are not purely resistive, and a reactive component has to be compensated. Additionally, the voltage swing amplitude is going to be smaller than the supply voltage. Finally, large device parallelization comes at the cost of increased parasitics. Ultimately, the PA's performance is further reduced.

Stability

Besides delivering power, stability and the associated analysis is one of the major challenges of PA design. Due to the aforementioned parasitics, inherent to the transistor itself, but also due to the added geometries during layout, feedback paths inside an amplifier design can lead to instability. To briefly summarize amplifier instability, Fig. 2.7 illustrates a simplified diagram of an amplifier split into a forward gain block ($A(j\omega)$) and a feedback gain block ($F(j\omega)$). Following the Barkhausen stability criterion, the amplifier can oscillate for $|A(j\omega)F(j\omega)| \geq 1$ and $\angle A(j\omega) + \angle F(j\omega) = 2n\pi$ [Beh11].

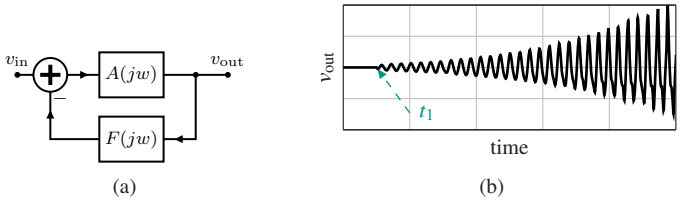


Figure 2.7: RF amplifier stability: a) generalized block diagram and b) unstable transient response to a short broadband pulse at t_1.

At low frequencies, the transistors' gain is high and attenuation from a real circuit's output to its input may be smaller. Additionally, it is challenging to avoid the phase condition for oscillation for every frequency between DC to $f_{\max}$. Without preventive measures, an oscillation can occur. This may compress the amplifier and cause unwanted output signals, performance degradation and could lead to failure of the devices. Fig. 2.7b shows the output voltage of an unstable amplifier versus time, after a short pulse was excited at the input at t_1. Due to the unstable behavior the amplifier is unusable. To predict unstable operation, amplifiers require careful stability analysis both in small- and large-signal operation [TVU24b]. Suitable methods to prevent the unstable behavior, for example adding resistors, can then be evaluated

Since determining the complete transfer function of a real RF amplifier is impractical, the Barkhausen criterion is not used. Throughout this work, the following methods are used to analyze stability. First, small-signal stability analysis using Rollett's K-factor [Rol62] is performed during the whole design phase. It is used as a first evaluation of the PA core and sub-block stability. However, in more complicated designs K-factor analysis delivers limited insight, as

it is only limited to small-signal operation and treats the PA as a single two-port block. To extend K-factor analysis a bias sweep is performed for the PAs presented in this thesis. By analyzing the PA's K-factor for different operating conditions, as they would occur during a large-signal period, a first estimate on large-signal stability can be established. Still, by treating the PA as a two-port blackbox unstable behavior can be missed. Thus, transient simulations are used to verify stability for the finished designs. To do so, a broadband pulse is excited at each terminal, RF and DC, and the response is observed.

To ensure stability, most PAs in this work are assembled on printed circuit boards (PCBs) for DC supply, including additional soldered capacitors at the DC terminals, which is a general method for stabilization [Cri06]. To suppress low-frequency oscillations, all designs utilize a parallel RC-element at the RF input of their cores to ballast the transistors and attenuate low-frequency signals.

Linearity versus Efficiency

In modern communication, complex single carrier modulation schemes such as 64- and 256-QAM are used in conjunction with multi carrier methods such as orthogonal frequency-division multiplexing (OFDM) [WAF21]. While using these modulation schemes guarantees efficient usage of the available spectrum, their high PAPR puts extensive linearity requirements on the PAs. Due to the non-linear behavior of PAs in compression a power back-off of several decibels, depending on the respective PAPR, is required and results in a lower average performance. Fig. 2.8 illustrates a PA's typical large-signal performance over input power, as well as the effect of power back-off on the performance. In this example, the PA's PAE at back-off is less than half its peak value.

Table 2.2 presents a summary of key parameters for different modulation schemes for a root-raised-cosine-filter with a roll-off factor, α, of 0.35. QAM requirements are according to 5G NR [VMR17, WAF21], APSK based on SatCom DVB-S2 [TVU24b].

To analyze the signal quality after amplification by a PA, root mean square (RMS) error vector magnitude (EVM) is used. It is defined as the RMS value

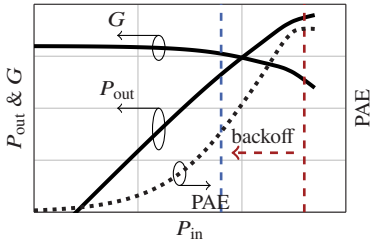


Figure 2.8: PA large-signal performance with power back-off illustration.

Table 2.2: Summary of modulation scheme parameters [VMR17, WAF21, TVU24b].

Const.	PAPR (dB)	$\mathrm{EVM_{RMS}}$ (%)	$\mathrm{EVM_{RMS}}$ (dB)
16-QAM	6.6	12.5	-18
64-QAM	7.7	8	-22
256-QAM	8.2	3.5	-29
16-APSK	$\approx$7	$\approx$15	-16.5

of the error vector, $A_{\mathrm{error,RMS}}$, over the RMS value of the constellation point magnitudes, $A_{\mathrm{ideal,RMS}}$, [VMR17]

$$\begin{aligned}\mathrm{EVM_{RMS}} &= \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left|S_{\mathrm{ideal},i}-S_{\mathrm{meas},i}\right|^2}}{\sqrt{\frac{1}{M}\sum_{i-1}^{M}\left|S_{\mathrm{ideal},i}\right|^2}} \\ &= \frac{A_{\mathrm{error,RMS}}}{A_{\mathrm{ideal,RMS}}}.\end{aligned} \tag{2.10}$$

Fig. 2.9 shows an example constellation diagram for 16-QAM, indicating the ideal ($S_{\mathrm{ideal},i}$) and measured ($S_{\mathrm{meas},i}$) vectors. The errors are for example caused by AM-AM, e.g., gain compression, and AM-PM characteristics of the PAs, especially affecting symbols with large amplitude.

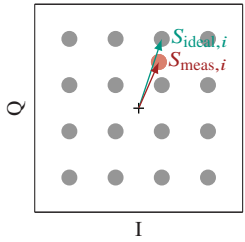


Figure 2.9: Normalized constellation diagram for a 16-QAM signal (similar to [VMR17]).

Thermal Management

Thermal management of PAs, especially for higher power levels, is critical to ensure high RF performance. First, the chip area in which DC power is dissipated is small and secondly at higher frequencies the efficiency of PAs is generally lower and in relative terms more power is dissipated. This can cause high temperatures in the chip and might lead to thermal runaway and failure of the chip. Furthermore, in some applications, such as SatCom, the amount of heat transfer is limited, as no heat transfer by convection or conduction to the environment of the satellite is possible. One aspect to simplify thermal management is to achieve high efficiency during large-signal operation. This reduces the amount of dissipated power per delivered RF power. Still, to prevent performance deterioration heat must be transferred from the active devices to a heatsink. [Bah09] shows a $12\,\mathrm{W}$ HPA losing $0.4\,\mathrm{dB}$ output power for a $1\,\mathrm{ms}$ pulse compared to a $10\,\mu\mathrm{s}$ pulse, highlighting the severity of the problem. In this work Si-based technologies are used. The silicon substrate has a relatively high thermal conductivity, k_{Si}, of $145\,\mathrm{W\,m^{-1}\,K^{-1}}$ [Bah09], enabling good heat conduction away from the active devices. However, this mandates a die attachment with sufficient heat conduction to ambient temperature at the chip bottom. Otherwise, the overall chip temperature may rise significantly. A thermal resistance, R_{th} is used to model the transition from chip to heatsink. In this work, for any off-chip interface (e.g., heatsink or die attach) equal heat transfer distribution and even surfaces, without any voids, are assumed. The thermal resistance of a structure can then be simplified to

$$R_{\mathrm{th}} = \frac{h}{A \cdot k}, \tag{2.11}$$

where h is the height, A the interface area (e.g. the chip area) and k the thermal conductivity of the respective material. Fig. 2.10 illustrates a basic thermal package model used throughout this work. The on-chip thermal resistance can be extracted using electrothermal co-simulation, for example using Keysight's Advanced Design System (ADS). This also includes thermal coupling between individual devices. In later chapters, two example SiGe BiCMOS PAs are presented highlighting the importance of thermal simulation, management and its influence on PA performance.

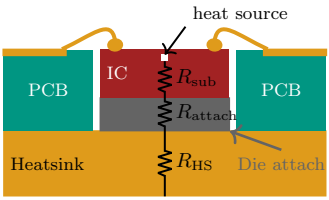


Figure 2.10: Basic thermal model used throughout this work.

3 Optimization of LC-based Output Matching Network Design

A critical aspect of PA design is the output matching network (OMN). The OMN has to transform the load impedance, commonly referred to as Z_{L} or Z_{load}, to the load-pull impedance, Z_{LP} or $Z_{\text{load-pull}}$, of the PA core. This is illustrated in Fig. 3.1. The OMN's efficiency, η_{omn}, relating the power delivered by the PA core to the OMN, P_{core}, to the power delivered to the load, P_{out}, directly influences the achievable performance of the PA in terms of output power and PAE. The bandwidth associated with the PA is also limited in part by the bandwidth of the OMN. Additionally, DC feeding and blocking have to be facilitated inside the network. Different approaches for matching networks exist, for example resistive matching, reactive LC-based matching and TL-based matching networks. While resistive matching offers a simple and generally broadband solution, it is impractical in PA design, when a high efficiency and output power are desired. For TL-based matching, the physical length of the TLs scales inversely with frequency, thus a TL-based matching network consumes a significant amount of chip area below a frequency of about 50 to $80\,\mathrm{GHz}$. A combination of both resistive and TL-based matching is used in distributed amplifiers to achieve broadband amplification. However, even when no extra DC power is dissipated on the resistors, literature examples achieve peak PAE values of only $20\,\%$ for an output power of $20\,\mathrm{dBm}$ at K_{a}-band [LFCE18]. Lastly, transformers are a popular solution achieving high network efficiency,

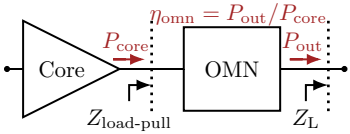


Figure 3.1: PA output matching overview. ©IEEE

especially in differential-to-differential cases. Still, transformers require specific physical geometries and in case of a high transformation ratio between Z_{L} and Z_{LP} a higher turn ratio than 1:1, which may reduce efficiency.

In contrast, LC-based matching networks feature very high integration density even at lower frequencies between K_{u}- and W-band as well as high efficiency. In this chapter, the efficiency driven design of LC-matching networks is investigated for implementation in SiGe BiCMOS BEOLs at mmWave frequencies. Two prototype PAs using optimized network topologies are then presented.

3.1 Efficiency Optimization of LC-Matching Networks

Parts of the following content are published in [8].

LC-based matching networks utilize lumped components, capacitors and inductors, to facilitate the transformation between two impedances. During the design phase of LC-based matching networks the imperfections of network components are usually neglected. At lower frequencies, this assumption may result in good performance, however the chosen network topology may not be the most efficient solution. This becomes more important as frequency increases and the impedances to be matched decrease. A plethora of analytical and numerical LC matching network optimization techniques including network losses have been previously published, for example in [CS18, HXW21, HP06, AKRH02]. These methods typically treat the optimization from a general point of view by simplifying the component imperfections to constant quality factors and by allowing for an unlimited number of components and component values. Thus, the practical insight for the designer is limited.

The goal of the following analysis is to accurately predict matching network loss before design implementation and to find network topologies optimizing the network's efficiency. An analytical solution to this problem appears impractical, as the number of possible network topologies is too large. Instead, an exhaustive search is pursued. Additionally, for this study the number of possible network components is limited. While an arbitrary number of components is possible and state of the art suggests performance improvements, implementation of a network with many components consumes significant chip area and unavoi-

dable parasitics during implementation may reduce final network efficiency. Consequently, a simpler solution may be preferred. The network configurations investigated are L-, cascaded L-, Pi- and T-networks, as illustrated in Fig. 3.2.

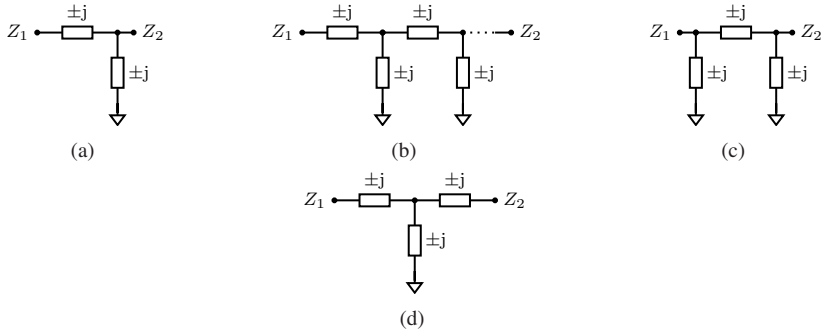


Figure 3.2: LC-based matching network topologies: a) L-network; b) cascaded L-networks; c) Pi-network and d) T-network.

To choose the optimal topology depending on the required load-pull impedance, all possible network topologies are compared for the target Z_{LP} and then the most efficient topology is selected. To move beyond state of the art, the components inside the networks are more accurately modelled by including size dependent quality factors and a quality factor reduction for DC feeding inductors. To calculate the necessary network component values for a load and load-pull impedance combination $(Z_{\mathrm{L}}, Z_{\mathrm{LP}})$, the following guidelines are used. The load impedance is assumed to be $50\,\Omega$ and the starting point for the transformation. For L-networks the required component values can be directly calculated from the impedance pair. However, depending on the load-pull impedance different network arrangements can be used. This is illustrated in Fig. 3.3a. Three different example L-network transformation paths are shown in a Smith chart to reach the same Z_{LP}.

When multi-stage L-networks are investigated, the calculation of the network components is simplified to individual L-network stages, by choosing intermediate impedances between the network stages. The choice of the intermediate impedance influences the network efficiency and component values. The intermediate impedances are chosen to have equal transformation ratio, r, for the real part per stage and linearly adjust the imaginary part between Z_{L} and Z_{LP}

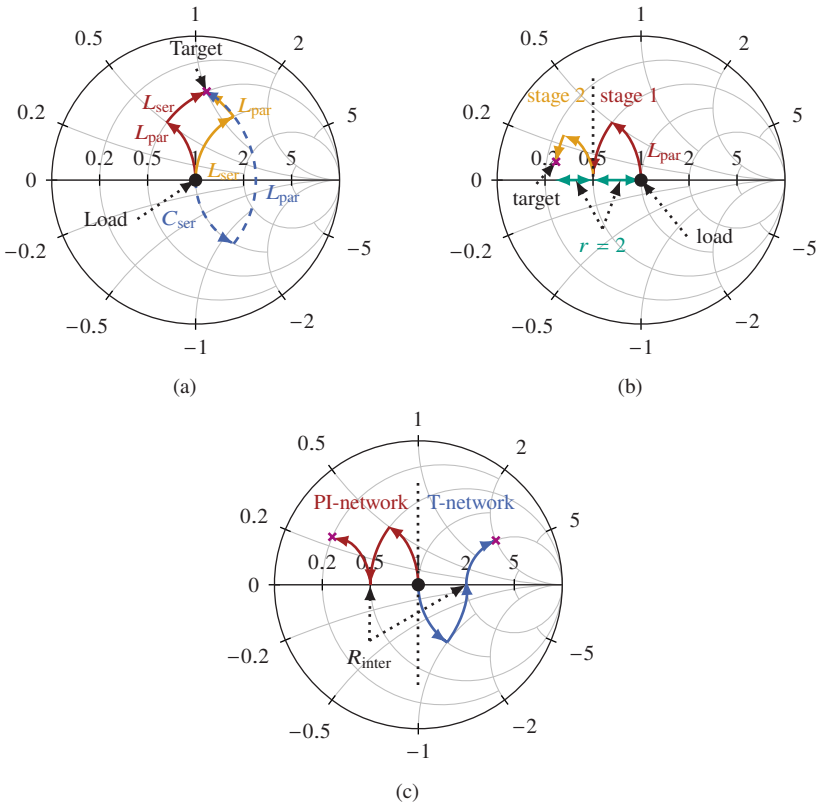


Figure 3.3: LC-based matching network Smith chart transformation paths: a) L-network; b) cascaded L-networks and c) PI- & T-network.

per stage. This is illustrated in Fig. 3.3b. In the example shown, the normalized real part is transformed from 1 to 0.5 in the first stage, and from 0.5 to 0.25 in the second stage. The ratio, r, is 2 for both stages. The normalized imaginary part is linearly adjusted, by first transforming from 0 to 0.05 in the first stage and then from 0.05 to 0.1 in the second stage.

For PI- and T-networks, the first two components connected to the load form an L-network transforming the load to a real intermediate impedance, R_{inter}. The last component is used to compensate for the imaginary part of the targeted

load-pull impedance. This is shown in Fig. 3.3c for a PI- and T-network. As a consequence, PI- and T-networks can only reach impedances within the $G = 1$ and $R = 1$ circles, respectively. Using these guidelines to construct the transformations all component values within the networks can be calculated.

When a matching network is used at a PA output, a shunt inductance within the matching network is essential for efficient and convenient DC supply. A DC feeding shunt inductor requires a large parallel capacitor to ground at the DC supply node to ensure sufficient high-frequency termination. At mmWave frequencies these capacitors influence the overall quality factor of the used inductor. As an example, this is shown in Fig. 3.4. A varying inductance with a quality factor of $Q_L = 12$ is combined with a lossy and finite parallel capacitor at 28 GHz. The used capacitor has a value of 5 pF and a quality factor of $Q_C = 15$. The negative effect on the quality factor is especially noticeable for small inductance values, which are required when the impedances become small, e.g., at a PA output. In the following analysis this effect is included for the first shunt inductance in the matching network.

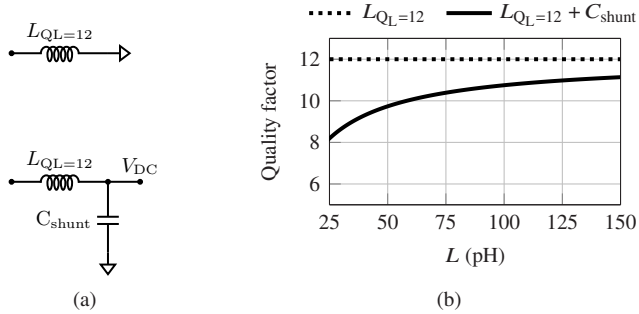


Figure 3.4: Quality factor of DC feeding inductors at 28 GHz: a) schematic and b) quality factor versus inductance. ©IEEE

To determine the quality factor depending on component value and if the component value is below the self-resonant frequency (SRF) a curve fitting approach is used. As the basis for the curve fitting 9 example inductor and 7 example capacitor layouts are evaluated using electromagnetic (EM) simulation with their values ranging from 30 to 1500 pH and 28 to 1200 fF at 28 GHz, respectively. Based on these results, the following basic functions are used to model inductors

$$L(f) = a\left(b + \frac{1}{SRF - f}\right), \tag{3.1}$$

$$Q_{\mathrm{L}}(f) = a - b(f - c)^2, \tag{3.2}$$

for which a, b, c and SRF are interpolated between the example layouts. For capacitors

$$C(f) = \left(a\mathrm{e}^{bf\cdot\frac{1}{\mathrm{GHz}}} + c\right)\mathrm{fF}, \tag{3.3}$$

$$Q_{\mathrm{C}}(f) = \left(a_Q\mathrm{e}^{b_Q f\cdot\frac{1}{\mathrm{GHz}}} + c_Q\right), \tag{3.4}$$

is used to model capacitance and quality factor. Again, a, b, c are interpolated between the results and differ from the constants used for the inductors. Fig. 3.5 compares the EM simulated and fitted results for an example inductor, showing good agreement.

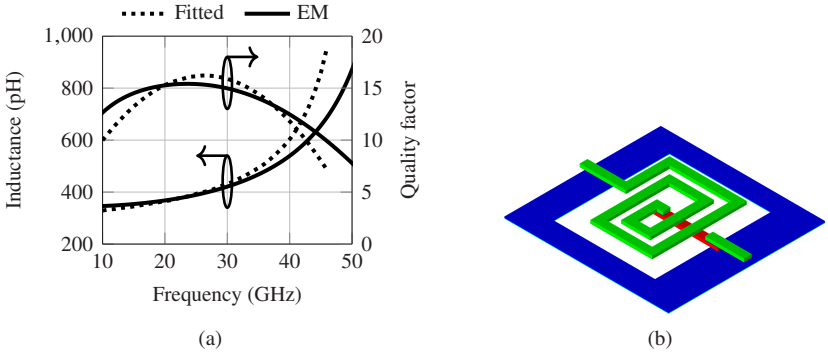


Figure 3.5: Inductor modelling: a) Comparison of EM simulated and fitted results and b) corresponding 3D EM model. ©IEEE

Based on the fitted results, quality factors accurately correspond to the component values. To illustrate this, Fig. 3.6 presents three maps of component size over frequency color-coded by the expected quality factor at each point

for series capacitors, shunt capacitors and inductors (either in shunt or series). The maps highlight that inductors tend to decrease in quality factor for very large or very small values. Capacitor quality factor decreases primarily with size, meaning decoupling capacitors will show a low quality factor. These maps must be recreated for varying frequencies of interest and technologies. By first calculating the required network component values and then using the presented component maps, the network performance can be accurately predicted w.r.t. network efficiency and bandwidth.

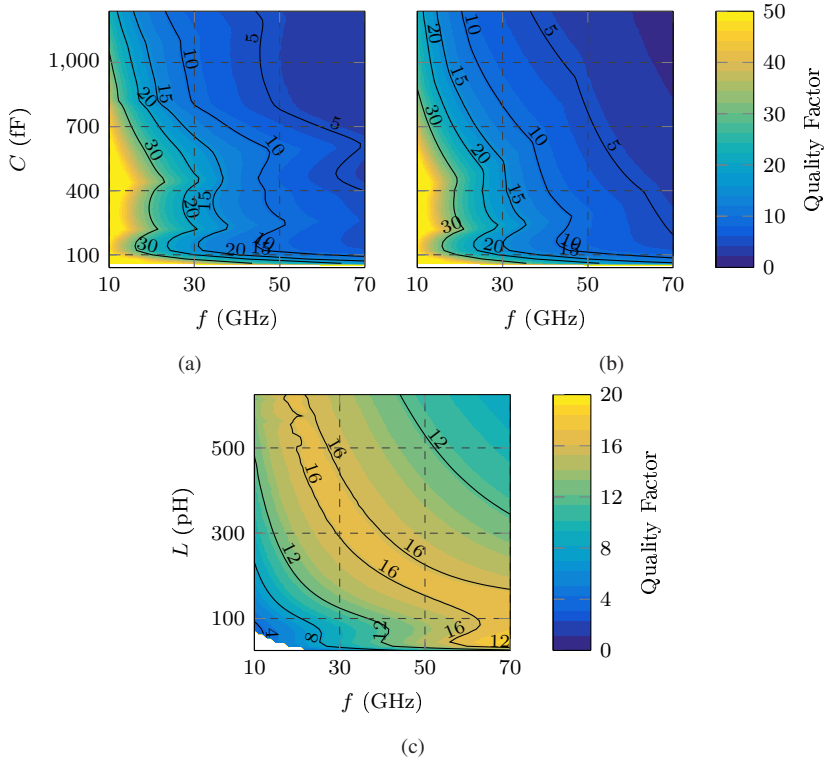


Figure 3.6: Capacitance and inductance versus frequency color-coded by expected quality factor for IHP's SG13G2Cu BEOL: a) shunt capacitors; b) series capacitors and c) inductors (series or shunt).

To co-optimize output power and efficiency, PA cores with different total device size are compared. To start, the load-pull data for each core is generated by load-pull simulations. The simulations are performed on the PA cores after EM simulation of the core layout. Fig. 3.7 shows the load-pull contours for maximum PAE. The simulated structure is a cascode PA core at 28 GHz with a total emitter length, L_{E}, of 72 µm, or 80 fingers. Additionally, load-pull simulations are performed for PA cores with 40 ($L_{\mathrm{E}} = 36\,\mu\mathrm{m}$) and 140 ($L_{\mathrm{E}} = 126\,\mu\mathrm{m}$) fingers.

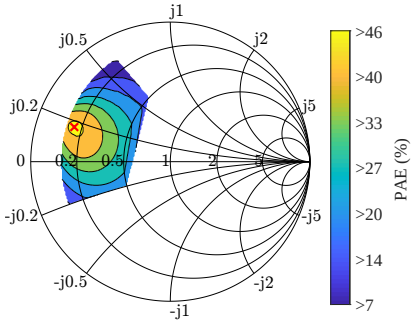


Figure 3.7: Example load-pull contours for a cascode PA core with 80 finger per device at 28 GHz. ©IEEE

In Fig. 3.8a the maximum matching network efficiency for a load impedance of $Z_L = 50\,\Omega$ transformed to any impedance on the Smith chart is shown using L-, cascaded L- and Pi/T-network topologies. To generate the presented data, each point on the Smith chart is matched using all possible network topologies and the network efficiency for each topology is calculated. The most efficient solution determines the efficiency limit shown on the map. Fig. 3.8b depicts a Smith chart color-coded by the network topology which achieves the highest network efficiency at a specific point in the Smith chart. L-networks are subdivided into groups depending on the first component connected to the load (+j inductor first, -j capacitor first) and the number of cascaded networks. Additionally, the load-pull impedances of the previously mentioned PA cores (▲ $L_{\mathrm{E}} = 126\,\mu\mathrm{m}$, ● $L_{\mathrm{E}} = 72\,\mu\mathrm{m}$ and ■ $L_{\mathrm{E}} = 36\,\mu\mathrm{m}$), are indicated in Fig. 3.6. When trying to increase output power the PA core size must be increased. This leads to a lower load-pull impedance and thus the network efficiency drops from more than 80 % down to approximately 60 % for the example cores. Using the values from the network efficiency map a drop in PAE in the range of 10 % can

be predicted for the largest core before performing the network implementation and EM optimization. The core with an emitter length of 72 µm, loses 2 % PAE compared to the smallest core and is thus chosen for the design presented in the following section. This emitter length achieves a favorable trade-off between loss of PAE while increasing the output power. Based on this analysis an initial network loss of 1.1 dB is expected for a PA core with a total emitter length of 72 µm.

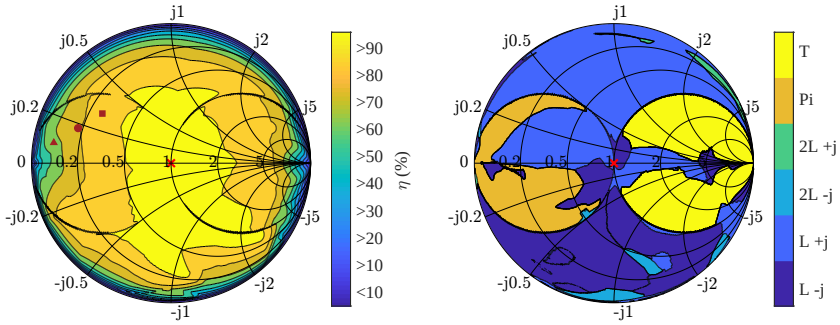


Figure 3.8: Network maps for $Z_L = 50\,\Omega$ & f = 28 GHz: a) maximum estimated network efficiency; b) most efficient topology.

In contrast to [CS18, HP06], networks with more than 3 components resulted in lower network efficiency throughout most of the Smith chart ($|\Gamma| < 0.9$). Only towards the edges of the Smith chart and for special cases more components showed higher efficiency compared to a basic L-, Pi- or T-network. This effect can be explained by the more accurate modelling of the quality factors for very small transformations as they would occur in multi-stage networks. This could in part be mitigated by optimization of individual components to improve quality factors. For PA cores with a load-pull impedance within the inductive part of the G = 1 circle the Pi-network in L-C-L configuration was the most efficient solution, including a convenient DC feed. The results presented also show that in most cases the shortest transformation path through the Smith chart is the most efficient solution. For example, to transform to the upper half of the Smith chart the optimal topologies generally start with an inductor. This avoids transforming through the lower half of the Smith chart. Additionally, Fig. 3.8a also shows higher efficiency in the lower half of the Smith chart, due to the

large quality factor advantage of capacitors over inductors at 28 GHz in this technology.

3.1.1 Efficient 23.7 dBm Ka-Band PA in 130nm SiGe

Parts of the following content are published in [8].

This section presents the design of a compact K_a-band PA in IHP's 130 nm SiGe BiCMOS technology SG13G2Cu achieving an output power of 23.7 dBm and a PAE of 40 % in class AB operation. It uses the method and results presented in the previous section for OMN optimization.

The PA's schematic is presented in Fig. 3.9. The PA is a single core design without power combining, consisting of 8 cascode UCs connected in parallel, resulting in a total emitter length of 72 µm per device. Each UC contains a bypass metal-insulator-metal (MIM) capacitor at the CB device and a parallel RC-element at the input for low-frequency stabilization. The topology for the OMN is chosen for its high efficiency. Since this technology's transistors provide high gain at 28 GHz additional loss is introduced into the input matching

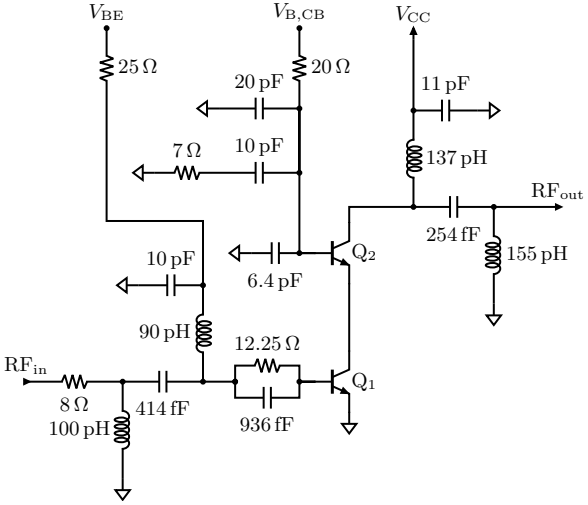


Figure 3.9: K_a-band PA schematic with optimized OMN topology. Total emitter length $L_{E,tot,Q1} = L_{E,tot,Q2} = 72$ µm.

network for stabilization. Small resistors of 25 and 20 Ω are integrated on-chip for the bias voltage supply lines at V_{BE} and $V_{\mathrm{B,CB}}$.

For the design, the PA core is EM simulated, and then load-pull simulations are performed. The resulting load-pull contours for PAE at 28 GHz are presented in Fig. 3.10a. For maximum PAE the optimum load-pull impedance is $(8+8.5\mathrm{j})\,\Omega$. By using the data of the previous section, the PAE load-pull contours can be displayed taking the OMN losses into account. The data is produced by multiplying the OMN's efficiency and the PAE load-pull data at each impedance point. This assumes sufficiently large power gain, otherwise the PAE is further degraded. The resulting contours are displayed in Fig. 3.10b. The optimal load-pull impedance without the OMN's effect is marked (×) and differs from the optimal load-pull impedance when the OMN losses are taken into account (×). The optimal impedance is shifted to $(10 + 8.5\mathrm{j})\,\Omega$. The difference in performance to the default load-pull impedance is 2 % of PAE.

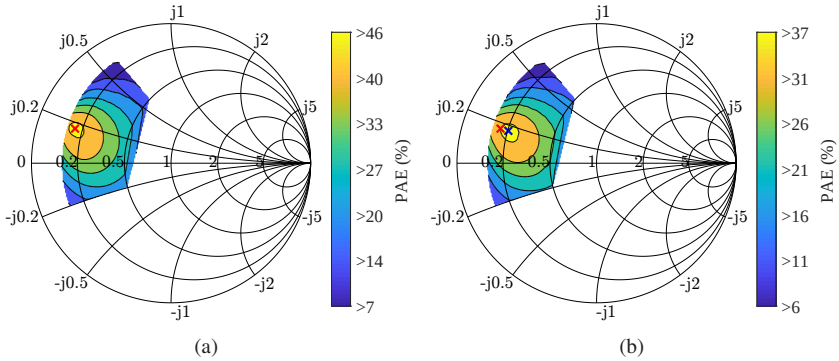


Figure 3.10: PAE load-pull contours at 28 GHz: a) ideally loaded PA core and b) PA core with OMN losses taken into account for each impedance. ©IEEE

After using the optimization of the previous section to select the topology and optimum Z_{LP}, the OMN is optimized by repeated EM simulation to increase the inductor quality factor, and the network loss is simulated to be 1 dB while transforming a 50 Ω load to $(10+8.5\mathrm{j})\,\Omega$. A microphotograph of the PA is shown in Fig. 3.11. Including pads, the PA only occupies a chip area of $0.25\,\mathrm{mm}^2$.

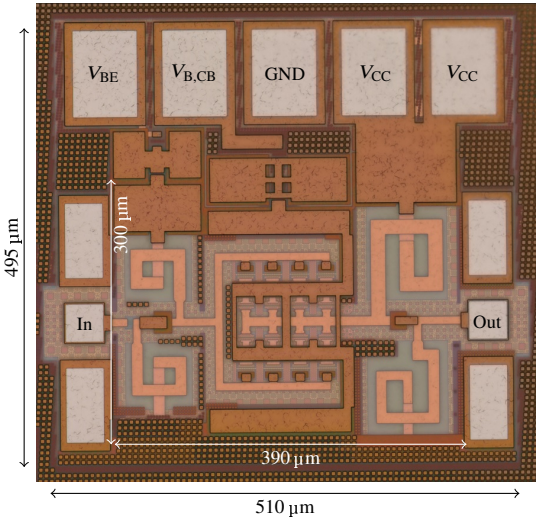


Figure 3.11: Chip microphotograph. Area: $0.25\,\mathrm{mm}^2$. RF core area: $0.12\,\mathrm{mm}^2$. ©IEEE

Characterization

The PA is characterized in class AB operation by small- and large-signal measurements, with $V_{\mathrm{BE}} = 0.89\,\mathrm{V}$, $V_{\mathrm{B,CB}} = 1.9\,\mathrm{V}$ and $V_{\mathrm{CC}} = 3.5\,\mathrm{V}$. For the small-signal measurement, calibrated on-wafer measurements are performed. The simulated and measured S-parameters versus frequency are presented in Fig. 3.12. The simulated and measured data are in good agreement. A small-signal gain of $20\,\mathrm{dB}$ is measured at $28\,\mathrm{GHz}$. The PA's input is matched better than $-10\,\mathrm{dB}$ from 25.5 to $31.3\,\mathrm{GHz}$.

For the large-signal measurement, a signal generator and power meter are used. Simulated and measured large-signal parameters are compared versus input power in Fig. 3.13a and versus frequency in Fig. 3.13b. At $28\,\mathrm{GHz}$, the PA delivers a saturated output power of $23.7\,\mathrm{dBm}$ at a maximum PAE of $40\,\%$. The achieved RF power density (PD) is $1.95\,\mathrm{W/mm}^2$. From 26 to $30\,\mathrm{GHz}$ the maximum PAE remains between 37 to $40\,\%$ and the saturated output power is larger than $23\,\mathrm{dBm}$.

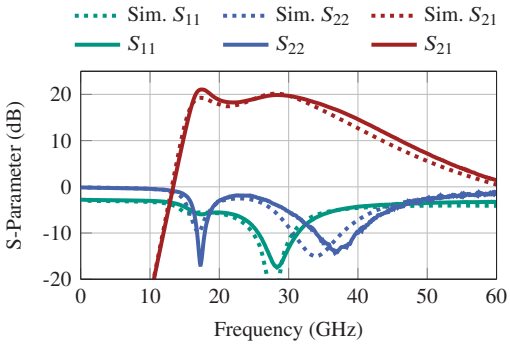


Figure 3.12: Simulated and measured S-parameter versus frequency.

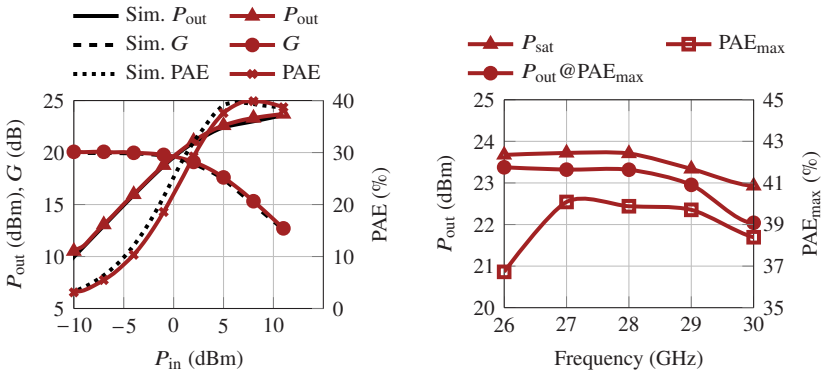


Figure 3.13: Simulated and measured single tone large-signal parameters: a) versus input power at 28 GHz and b) versus frequency.

3.1.2 Efficient Ku-Band PA in 22nm FD-SOI

The following content has been partly published in [10].

A similar design is investigated in GF's 22 nm FD-SOI CMOS technology, which offers excellent performance for high-frequency circuits, digital and mixed-signal components alike. However, the limited supply voltages of only 0.8 V per device pose a significant challenge for high-frequency power amplification. The achievable voltage swing is small and thus a large amount of device parallelization is needed to increase the delivered power. To overcome this problem, either power combining or transistor stacking, for example presented in [DHG+13], can be used. For this investigation, a compact single core design with an efficient LC-based matching network is envisioned, thus only transistor stacking is investigated. Transistor stacking, depicted in Fig. 3.14, increases the overall voltage swing of a PA by adding the voltage swing of multiple transistors. The first transistor is operated as a CS device. The following upper transistors appear as CG devices. However, to ensure reliable operation the gate cannot be alternate current (AC) grounded for the upper transistors. Instead, a voltage swing must be allowed on the gate to avoid exceeding gate-source or gate-drain voltage limits during a signal cycle. Compared to device parallelization, transistor stacking increases the output power without reduction of the output impedance.

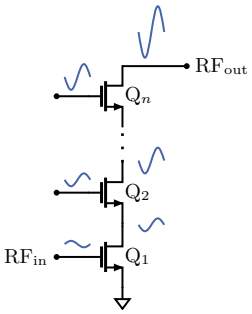


Figure 3.14: Basic transistor stacking. Similar to [DHG+13].

For the prototype, PA core performance is compared between a CS, cascode and three-stacked core design. All designs are evaluated for the same total transistor gate width per device and therefore at approximately the same drain current, I_D, per core. The three core schematics are presented in Fig. 3.15. Each core

consists of 4 identical unit cells connected in parallel. Each unit cell features an RC-element at the input for low-frequency stabilization. The upper transistor gates are biased through large resistors and decoupled by shunt capacitors. For the three-stacked device the capacitance for the upper devices is reduced to allow voltage swing on the gate.

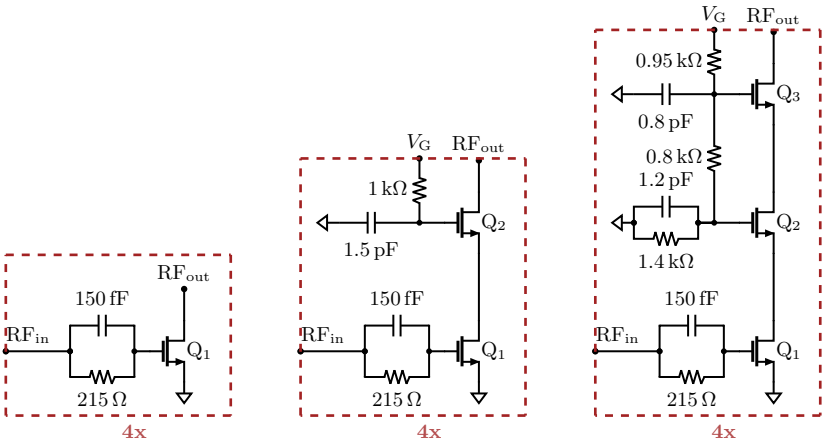


Figure 3.15: Core schematics: a) common-source ($V_{DD} = 0.8\,V$); b) cascode ($V_{DD} = 1.6\,V$) and c) three-stack ($V_{DD} = 2.4\,V$). $Q_{1,total} = Q_{2,total} = Q_{3,total} = 4$ x $67.2\,\mu m$. ©IEEE

The performance is compared for EM simulated core layouts under ideal loading conditions and with a lossy matching network to $50\,\Omega$. The ideal load impedances are determined by load-pull simulations for optimal PAE. The results including the matching network loss are also denoted with the index 'OMN'. The simulation results for the core comparison at $18\,GHz$ are shown in Fig. 3.16.

The common-source core achieves a saturated output power of $13\,dBm$, including matching network losses. This is $4\,dB$ lower than the cascode core with almost $17\,dBm$. Additionally, the common-source core's PAE is halved when matching networks are included. This significant drop in PAE is caused by the low load-pull impedance and consequently high matching network loss. Secondly, the low gain in compression (G<5 dB) reduces the PAE, as the input power is comparable to the output power. The three-stack core, including network losses, achieves $19.9\,dBm$ of saturated output power. However, even

though the output network loss is about $0.7\,\mathrm{dB}$ for the three-stack core and $1\,\mathrm{dB}$ for the cascode core, the PAE peaks for the cascode core and then declines for higher stacking. This confirms the results previously shown in [DHG+13]. A simulated peak PAE of $45\,\%$ is achieved for the cascode core including matching networks. The cascode core is thus selected for the design.

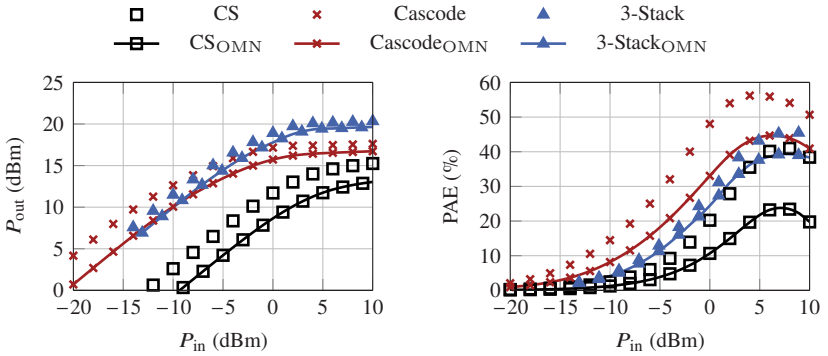


Figure 3.16: Large-signal performance comparison of a CS core, a cascode core and a 3-stacked core under ideal loading conditions and with lossy matching networks (indicated by 'OMN') at $18\,\mathrm{GHz}$: a) output power and b) PAE versus input power. ©IEEE

Due to the necessary parallelization the input and load-pull impedance for the cascode design are at $Z_{\mathrm{in}} = (10 - 5\mathrm{j})\,\Omega$ and $Z_{\mathrm{L,opt}} = (10 + 10\mathrm{j})\,\Omega$, respectively. Since the core provides high gain, the input matching network is not optimized for efficiency. Instead, the added loss is accepted in favor of more stable behavior of the PA. The OMN is a Pi-network, and its inductors are iteratively optimized using EM simulation to improve network efficiency and consequently PA performance. A schematic of the final PA design is presented in Fig. 3.17.

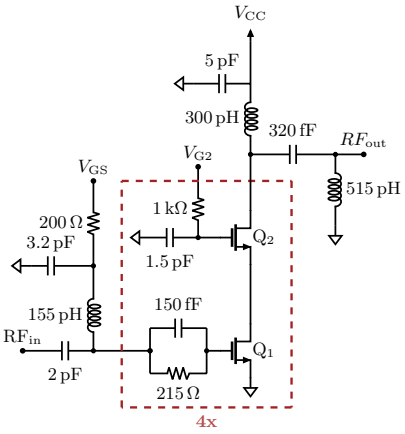
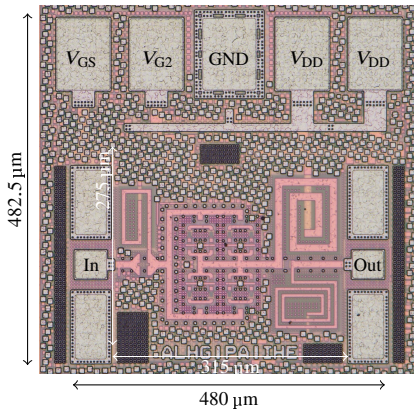


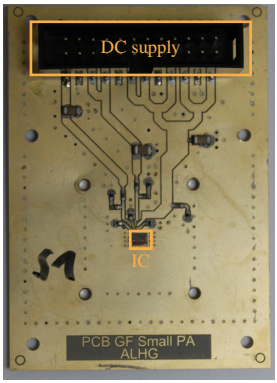
Figure 3.17: K_u-band PA schematic with optimized output matching network. Total gate width $w_{G,tot,Q1} = w_{G,tot,Q2} = 72\,\mu m$. ©IEEE

Characterization

A chip microphotograph is presented in Fig. 3.18a. The overall chip, including electrostatic discharge (ESD) protection and pads only occupies an area of $0.23\,mm^2$, of which only $0.09\,mm^2$ are occupied by the high-frequency circuit.



(a)



(b)

Figure 3.18: Prototype: a) Chip microphotograph (area: $0.23\,mm^2$, RF core area: $0.09\,mm^2$) ©IEEE and b) PCB assembly.

For the characterization, DC is supplied through a PCB, which is shown in Fig. 3.18b and the PA is biased close to class A, with V_{GS} = 0.5 V, V_{G2} = 1.3 V and V_{DD} = 1.6 V. The small-signal measurement is performed using calibrated on-wafer measurements. A comparison of simulated and measured data is presented in Fig. 3.19. The small-signal measurement shows good agreement with simulation. Peak small-signal gain is measured to be 20 dB and a relative 3 dB bandwidth of 35 % is achieved from 15.4 to 21.9 GHz.

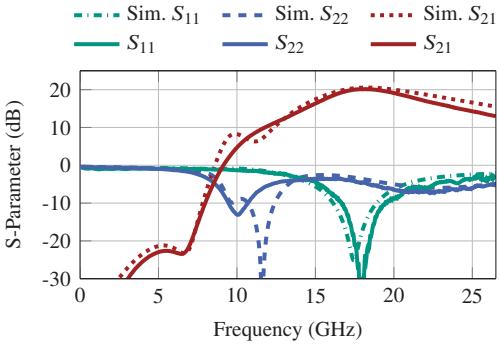
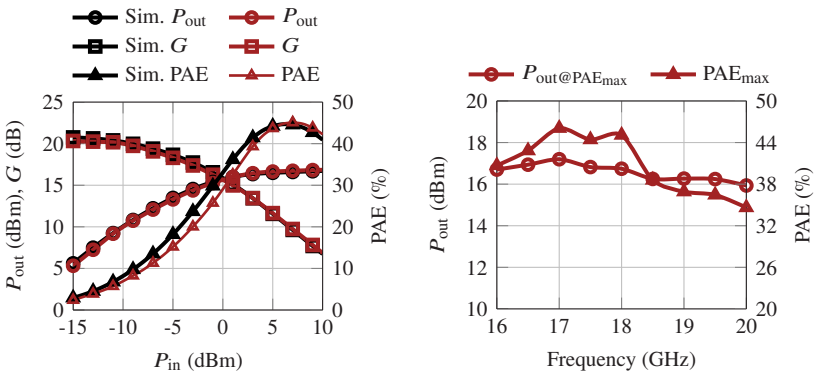


Figure 3.19: Simulated and measured S-parameters versus frequency.

Large-signal characterization is performed using a signal generator as the source and a power meter connected to the output. Cable losses are calibrated out and probe loss is accounted for with the respective data sheet values. The measurement setup is illustrated in appendix A.1. The corresponding large-signal measurement results are shown in Fig. 3.20a and 3.20b. A P_{sat} of 17 dBm at a PAE of 45 % is measured. At this point, the amplifier is 8 dB compressed. At the 1 dB compression point the PA outputs 12 dBm at a PAE of 11 %. The highest PAE is achieved between 17 to 18 GHz.

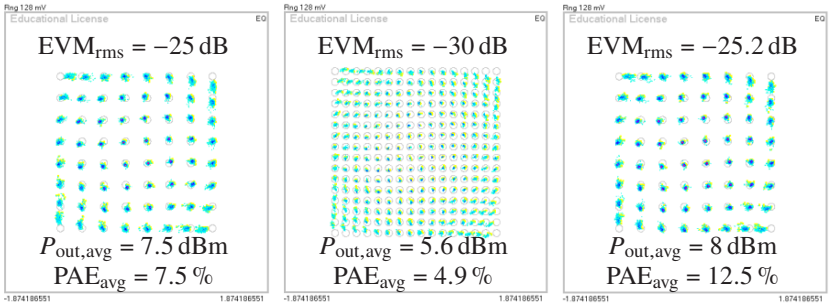
Modulated characterization is performed for 64-QAM and 256-QAM with a data rate of 1.2 Gbit/s and 0.8 Gbit/s, respectively. For the 64-QAM signal, an average output power, $P_{\mathrm{out,avg}}$, of 7.5 dBm at an average PAE, $\mathrm{PAE_{avg}}$, of 7.5 % is measured for an EVM of −25 dB. For 256-QAM at an EVM of −30 dB, a $P_{\mathrm{out,avg}}$ of 5.6 dBm is achieved at an average PAE of 4.9 %. The constellation diagrams of the modulated measurements are presented in Fig. 3.21. An improvement in performance is possible by testing different biasing conditions for the PA. When using $\mathrm{V_{G2}} = 1.15\,\mathrm{V}$ & $\mathrm{V_{GS}} = 0.35\,\mathrm{V}$ the



(a) (b)

Figure 3.20: Single tone large-signal measurement: a) large-signal parameters versus input power at 18 GHz ©IEEE and b) large-signal parameters versus frequency.

modulated performance for 1.2 Gbit/s 64-QAM is enhanced. The lower bias voltages reduce the current consumption, while maintaining similar output power for the same EVM. This improves the average PAE to 12.5 %.



(a) (b) (c)

Figure 3.21: Constellation diagrams of modulated measurements: a) 200 MSym/s 64-QAM; b) 100 MSym/s 256-QAM and c) 200 MSym/s 64-QAM with reduced biasing. ©IEEE

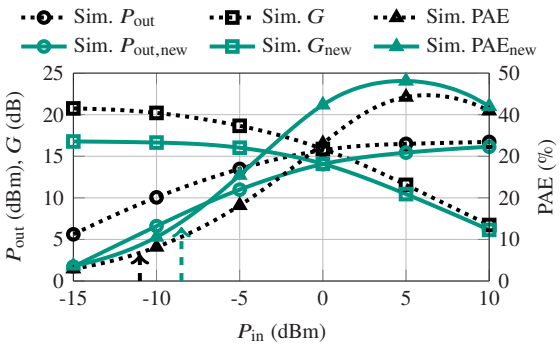


Figure 3.22: Simulated large-signal parameters at 18 GHz for different bias points versus input power.

To investigate this effect Fig. 3.22 shows the simulated large-signal parameters versus input power for both points of operation. Additionally, the average input power for which the linearity requirement ($\mathrm{EVM_{rms}} \leq -25\,\mathrm{dB}$) is reached, is indicated by an arrow. Generally, the bias point using a lower V_{GS} achieves a higher PAE at the cost of lower gain and output power. However, for this bias point the PA starts to compress for an input power approximately $5\,\mathrm{dB}$ larger compared to the initial bias point. Similarly, the average input power, which can be tolerated for a modulated signal is around $3\,\mathrm{dB}$ larger for the lower V_{GS}. When the large-signal performance is read at the respective input power levels, the new bias point is expected to provide similar power at higher PAE. Chapter 6 expands on this topic by providing a method to predict and optimize modulated performance.

3.2 Conclusion

A method to predict matching network loss before design implementation and to select an optimum network topology is presented. For the analyzed technology SG13G2Cu and an operational frequency of $28\,\mathrm{GHz}$ the majority of the Smith chart ($|\Gamma| \leq 0.9$, $Z_\mathrm{L} = 50\,\Omega$) is most efficiently matched by a matching network consisting of 2 or 3 components. Pi-networks in L-C-L configuration are among the best network options, including a convenient DC feed, for impedances within the G = 1 circle of the Smith chart.

Two PA prototypes are presented. The first prototype, integrated in a $130\,\mathrm{nm}$ SiGe BiCMOS technology for K_a-band frequencies, achieves an output power of $23.7\,\mathrm{dBm}$ at a peak PAE of $40\,\%$. The second prototype, realized in GF's $22\,\mathrm{nm}$ FD-SOI CMOS technology at $18\,\mathrm{GHz}$, shows a peak PAE of $45\,\%$ and a high modulated efficiency for a 64-QAM signal of $12.5\,\%$. Both prototypes use LC-based matching networks achieving high network and high area efficiency. Table 3.1 presents a comparison with state-of-the-art PAs. For the SiGe-based PA the highest power density (PD) per chip area is achieved. The maximum PAE is among the highest and is only improved in designs with lower output power. Overall, the PA provides state-of-the-art performance.

The PA presented in $22\,\mathrm{nm}$ FD-SOI CMOS is, to the best of the author's knowledge, the most compact design published. However, while its power density is high, it is surpassed by [ZTK$^+$20]. This can be attributed to the higher amount of stacking used in [ZTK$^+$20]. The achieved peak PAE of $45\,\%$ as well as the modulated PAE of $12.5\,\%$ compare well with state of the art, even when the advantage of the lower design frequency is taken into account.

Table 3.1: Performance comparison with state of the art.

Ref.	f_C (GHz)	P_{sat} (dBm)	PAE_{max} (%)	V_{CC} (V)	RF area (mm^2)	RF PD (W/mm^2)
Sec. 3.1.1$^+$	28	23.7	40	3.5	0.12	1.95
[WZLW21a]$^+$	35	22.8	27	3.3	0.48	0.395
[TBH$^+$21a]$^+$	29	22.4	39.8	3.2	0.16	1.07
[ZZF$^+$19]$^+$	34	22.9	21	3.3	0.4	0.487
[LHJ24]$^+$	28	22.6	40.3	3.6	0.115	1.58
[TVU24a]$^+$	18.8	22.8	37.7	1.5	0.55	0.348
Sec. 3.1.2$^\$$	18	17	45	1.6	0.09	0.64
[ZTK$^+$20]$^\$$	28	22.5	28.5	2.4	0.2	0.89
[AHST$^+$22]$^\$$	28	21	31.5	1.6	0.61†	
[XTL$^+$19]$^\$$	29.5	16.8	19.8	2.4	0.24	0.2
[MSLL22a]$^\$$	24	14.9	26.1	1.6*	0.31†	
[RST$^+$22]$^\$$	26	19.6	15.8	2.7	0.484	0.188
[DKC22]‡	26	20.5	39	2	0.9	0.12

$^+$ 130 nm SiGe BiCMOS $^\$$ 22 nm FD-SOI CMOS ‡ 28 nm FD-SOI CMOS
* Estimated from figures † Full chip

4 Efficient On-Chip Power Combining

In chapter 3, a design method predicting matching network loss and enabling compact and efficient single core PA designs is presented. However, the output power, which can be delivered by a single PA core is limited. To enhance the overall output power delivered from a single IC, multiple PA cores can be combined using power combiners. A generalized combiner block diagram is depicted in Fig. 4.1, for which n inputs are combined into a single output. Compared to increasing the PA core size, a power combiner includes impedance transformation. For silicon-based technologies the most used power combiners are transformer-based or Wilkinson power combiners, for example in [Wil60, CKA+22, WZZ+22, CHL16, DH15, WW20a, TCR13, ELM14, WNP16].

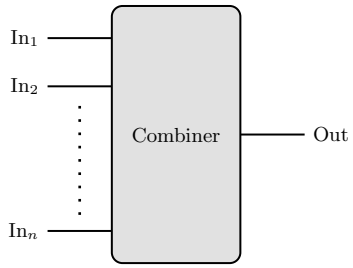


Figure 4.1: Generalized combiner drawing.

In published literature on K_a-band SiGe BiCMOS PAs with output power in the range of $30\,\mathrm{dBm}$, mostly Wilkinson combiners or in-phase current combiners are used. An in-phase combiner is similar to a Wilkinson combiner without isolation resistor. However, the achieved PAE in literature is generally low, e.g., 10-20 % [ELM14, WNP16]. Using off-chip combining structures, as in [RQG+22], a higher PAE of 26 % is achieved by reducing combiner insertion loss (IL). However, this negates the advantage of silicon's higher in-

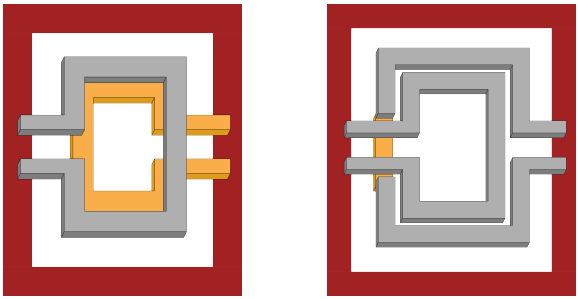
tegration density, as the off-chip combiner is larger than the silicon die itself. In comparison a plethora of publications on transformer-based PAs, for example [KLL+24, WW20a], exist that achieve high values of PAE in the range of 25-40 %. For these PAs however, the output power appears to be limited to around 28 dBm, with most achieving around 20 dBm, due to limited scalability. The best performing literature examples also avoid the differential to single-ended conversion at the output, requiring a differential interface.

To give an overview of available combining structures and to find efficient combining solutions, the following section investigates a prototype medium power amplifier (MPA) based on a study on efficient 2-to-1 fully differential transformers. This is followed by an investigation on in-phase power combiners for comparison and to increase the number of combined cores.

4.1 Transformer-based combining

The PA presented in this section and its transformers are implemented in IHP's 130 nm SiGe BiCMOS technology SG13G2. It features a 7-layer Al BEOL.

A transformer consists of at least two coupled coils. The coupling is achieved either by vertical overlap using different metal layers, as depicted in Fig. 4.2a, or by routing the coils on the same metal layer and in close horizontal proximity, as is shown in Fig. 4.2b. While horizontal implementations



(a) (b)

Figure 4.2: Typical transformer structures: a) vertical and b) horizontal

are shown [WSH+24], published literature in the targeted frequency range and in similar technologies typically uses vertical transformer implementation [WZLW21b, TBH+21b, LHJ24]. For this work, vertical implementation is chosen for transformer design. A distinct advantage of transformers is their differential nature and their ability to serve multiple purposes like matching, power combining, and DC feeding simultaneously. Additionally, a single-ended to differential conversion can be integrated into the structure.

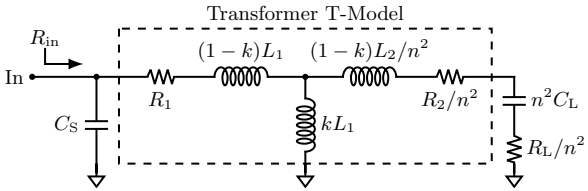


Figure 4.3: Transformer equivalent T-Model with capacitive load and tuning capacitor [AKRH02].

The behavior of a transformer can be approximated by the T-model, illustrated in Fig. 4.3 and previously presented in [AKRH02]. L_1 and L_2 are the primary and secondary inductance, k is the coupling factor, and n is the coil ratio. In [AKRH02], it is shown that the optimum efficiency of a transformer is independent of the transformation ratio and only depends on the quality factor of the primary and secondary inductors, as well as the coupling factor. The resulting equation is

$$\eta = \frac{1}{1 + 2\sqrt{\left(1 + \frac{1}{Q_1 Q_2 k^2}\right)\frac{1}{Q_1 Q_2 k^2}} + \frac{2}{Q_1 Q_2 k^2}}. \tag{4.1}$$

Compared to LC-based matching networks, for which the insertion loss scales with the transformation ratio, transformers promise superior performance. However, this assumes an optimal choice of the turn ratio, n, and sufficiently high quality factors for the inductors. To calculate the necessary turn ratio n,

$$n \approx \sqrt{\frac{1}{1+A^2} \cdot \frac{E\left(Q_1/k^2 + Q_2\right)}{Q_1}} \tag{4.2}$$

is presented in [AKRH02], with $E = r \cdot \eta$ and

$$A = \frac{1}{\sqrt{\frac{1}{Q_2^2} + \frac{Q_1}{Q_2} \cdot k^2}}. \tag{4.3}$$

This equation assumes an additional capacitor connected in parallel to R_L. Using the presented equations, Fig. 4.4 shows transformer efficiency, η, and optimal turn ratio, n over transformation ratio, r. For comparison, an efficiency trend for LC-based matching networks, taken from the results of chapter 3.1, is also included. The turn ratio is rounded down to integers. Transformation ratios in the range of 2-10 are a realistic assumption when high output power at mmWave frequencies is desired. The optimal turn ratio increases above 1:1 for a transformation ratio, $r = R_\mathrm{L}/R_\mathrm{in}$, of around 4. As transformation ratio increases, an advantage over LC-based matching networks is expected. However, during implementation of the transformers, layout effects have a critical influence on performance and as frequency increases transformers with higher turn ratios become harder to realize. In literature on Si-based PAs at mmWave frequencies, higher turn ratios than 1:1 are not commonly published. Multiple turns require a more complex layout and, in case of vertical implementation, each additional turn has to be routed closer to the lossy silicon substrate. This

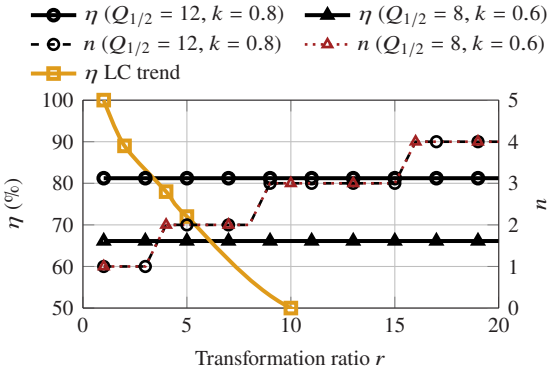


Figure 4.4: Theoretical transformer efficiency, η, and turn ratio n over transformation ratio, r.

significantly reduces the self-resonant frequency and efficiency of the transformer, as the parasitics to the lossy substrate grow.

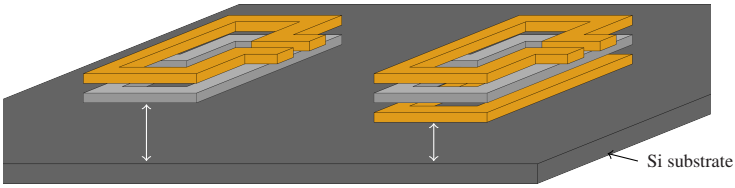


Figure 4.5: 1:1 and 2:1 transformer over Si substrate.

A simplified side view of a 1:1 and 2:1 transformer are shown in Fig. 4.5 for illustration. When a high output power is desired, low impedances have to be matched by the transformers. Consequently, higher turn ratios, e.g., 2:1 or a reduction of the load impedance by a parallel capacitor are needed to achieve a match better than $-10\,\mathrm{dB}$ and an efficiency as high as possible. To investigate the achievable performance of 2:1 transformers in the chosen technology, two prototype transformers are designed. Both transformers are designed differentially and transform $100\,\Omega$ to $(15 + 15\mathrm{j})\,\Omega$. For the measurement additional transmission lines (TLs) must be integrated between the transformers and the contact pads. The targeted impedances are therefore adjusted to $(15 - 10\mathrm{j})\,\Omega$ and $(92 - 90\mathrm{j})\,\Omega$ due to the influence of the TLs. The transformers' microphotographs are presented in Fig. 4.6a and 4.6b. Both transformers feature a 2:1 turn ratio. Version 1 is designed by scaling aligned coils of equal line width. Version 2 is improved by reducing the overall coil size of the transformer while optimizing the width of the coils. Additionally, a small offset between the primary and secondary coils is introduced for version 2 to enable better coupling. This improves the quality of the match and the insertion loss over frequency. Both transformers integrate the single turn coil on the second top metal layer, 'TopMetal1', between the two turns of the other coil, integrated in the top metal, 'TopMetal2', and a combination of three thin metal layers, 'Metal3-5'. The corresponding simulated and measured results in Fig. 4.6c and 4.6d show high bandwidth and a low loss of $1\,\mathrm{dB}$ including the transmission lines for version 2. A major advantage of the presented transformers are their very compact nature, while simultaneously matching two inputs.

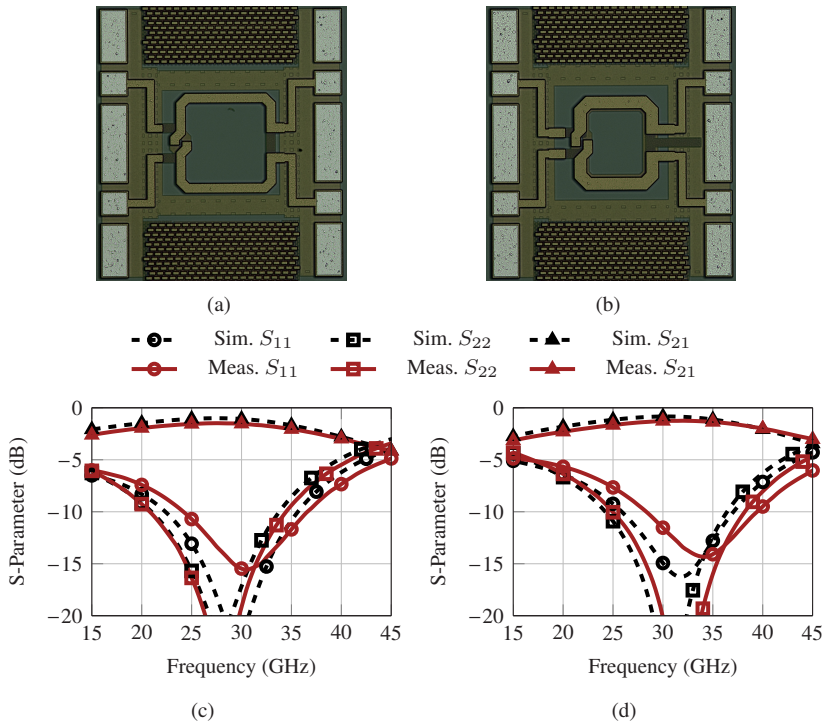


Figure 4.6: 2:1 transformers: a) chip microphotograph version 1; b) chip microphotgraph version 2; c) S-Parameters versus frequency (version 1) and d) S-Parameters versus frequency (version 2).

4.1.1 Scalability of Transformer Combining

Expanding the transformer structure to more than two inputs is possible and has been previously presented, for example in [WW20a, NJW19, WLW19]. The two main methods, illustrated in Fig. 4.7 and 4.8, are parallel current combining and series voltage combining. In Fig. 4.7a a basic version of parallel current combining of transformers is shown. It combines four inputs and is often used in published literature [TVU24a, WZLW21b]. To further expand the number of inputs a structure like Fig. 4.7b is possible, for which 8 inputs can be combined, however for a $50\,\Omega$ load, the transformers each have to provide a $200\,\Omega$ output impedance. This decreases transformer efficiency when low impedances must

be presented to the PA cores at the transformer inputs. Additionally, physical size of the PA core layout is important to enable a compact layout of the combiner. Otherwise, extra losses in the necessary connections towards the pad can reduce efficiency. From a geometrical perspective this is the maximum number of inputs, unless a pad at the chip center is allowed for which the structure could be mirrored at the top. In other cases, a TL-based combiner is needed to expand the number of combined inputs. The loss for these structures depends on the load-pull impedance required by the PA cores, but is expected to be equal to or higher than $0.8\,\mathrm{dB}$, which is achieved for a single transformer.

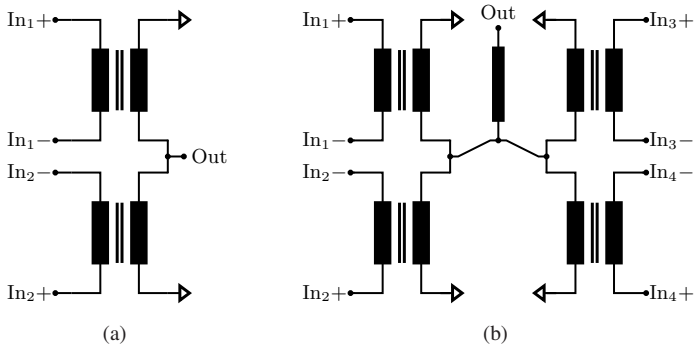


Figure 4.7: Parallel transformer combining: a) basic 4:1 and b) expanded 8:1.

In Fig. 4.8a basic series voltage combining of transformer outputs [AKRH02] is presented. By combining the voltages instead of the currents the transformation ratio in the transformers is lowered, as they now occur in series at the output. However, geometric optimization is crucial, otherwise the efficiency of the structure decreases. To expand the structure to 8 inputs, an arrangement as depicted in Fig. 4.8b is possible. This is also referred to as the distributed active transformer (DAT) [AKRH02]. For a single ended output one output terminal must be shorted to ground, disrupting the symmetry of the structure and requiring extensive layout optimization of the transformers, making the design complex. Without an added TL-based combiner or a pad at the chip center geometric constraints prevent more inputs to be combined in the structure and PA core size has to comply with the layouted combiner.

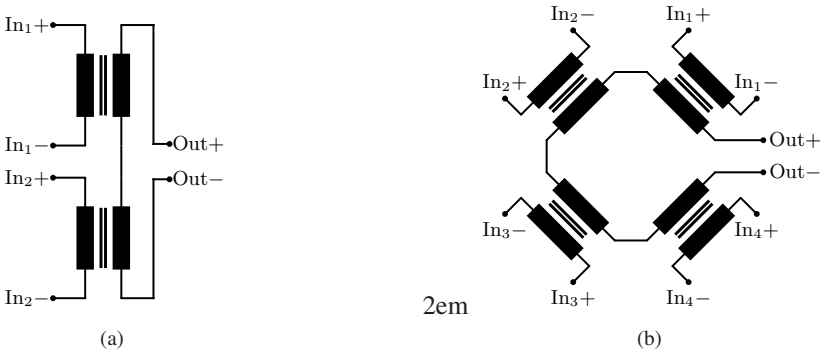


Figure 4.8: Series transformer combining: a) basic 4:2 and b) expanded 8:2.

4.1.2 23.7 dBm Pseudo Differential Ka-Band PA in 130nm SiGe

Parts of the following content have been published in [6].

Using the investigated basic 2:1 transformer a MPA is designed at 28 GHz. The PA is a pseudo differential design consisting of two PA cores. The same transformer that is optimized for the output is reused at the input. At the input, small adjustments are made by capacitors to account for the difference between the PA core's input and load-pull impedance. The corresponding schematic is presented in Fig. 4.9.

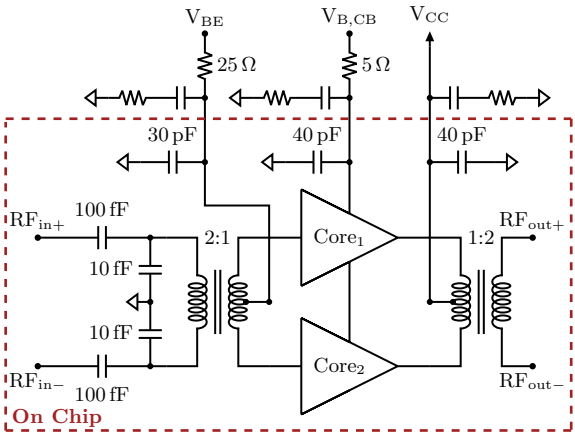


Figure 4.9: Schematic of pseudo differential K_a-band PA. ©IEEE

The used PA cores consist of parallelized UCs, each comprised of a 10 finger cascode transistor arrangement and an RC-element at the input for low-frequency stabilization. The UC schematic is shown in Fig. 4.10a. The cores are designed by gradually increasing the number of parallel unit cells until a load-pull impedance around 7.5 Ω is reached for the entire core. A total of 8 unit cells (80 fingers) can be parallelized before the impedance drops below this value. Since the PA cores are driven differentially, this results in a differential load-pull impedance in the range of 15 Ω. This is an advantage in differential designs, as the combined cores do not appear in parallel, but in series. Instead of matching the load-pull impedance on each side to 100 Ω and then connecting the branches in parallel, it is sufficient to match each branch to 50 Ω. A 3D rendered layout of the PA core, its load-pull contours and the large-signal performance at 28 GHz are depicted in Fig. 4.10. To achieve maximum output power the PA is biased at V_{BE} = 0.92 V, $V_{B,CB}$ = 2.3 V and V_{CC} = 4.5 V. The simulated output power, $P_{out,opt}$ is 25.2 dBm per core with a PAE_{opt} of 35 % at the simulated load-pull impedance of $(7 + 4j)\,\Omega$.

Using the prototyped transformers from Fig. 4.6 as the basis, the layout is optimized to present an impedance close to the load-pull impedance of the core. After EM simulation of the final layout, the impedance presented by the transformer is $(8 + 12j)\,\Omega$. Using the suboptimal impedance the core's PAE is

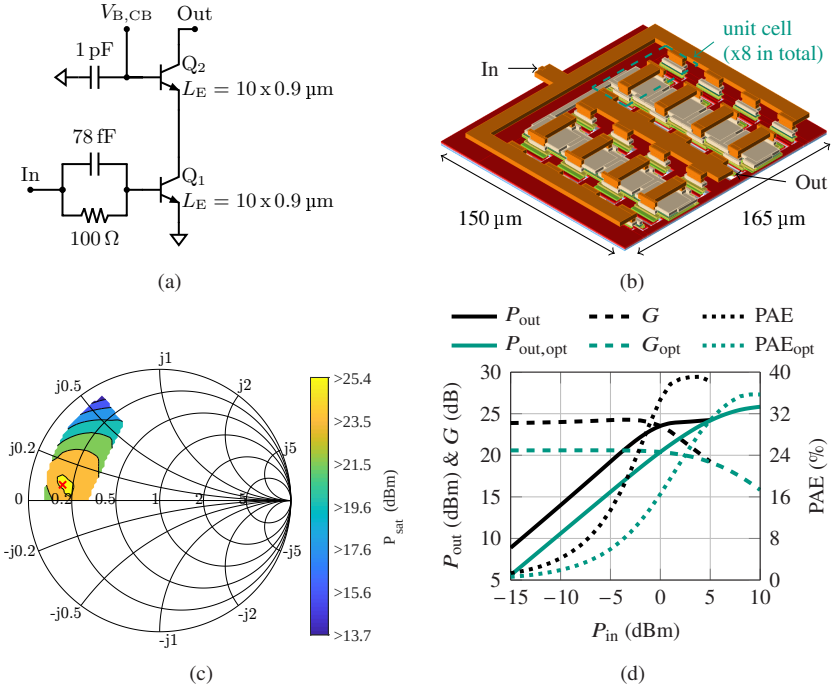


Figure 4.10: K_a-band PA core: a) unit cell schematic; b) 3D rendered core layout; c) load-pull contours for P_{sat} and d) large-signal simulation results at 28 GHz versus input power.

enhanced by 3 % at the cost of 1 dB output power. This compromise improves the network loss of the transformer compared to the optimal load-pull impedance. The core's output power is reduced to 24.2 dBm. The simulation results are shown in Fig. 4.10d. To achieve a 2:1 coil ratio, the transformer's secondary coil, connected to the output pads, is routed on the top metal, 'TopMetal2', and the second winding is routed on three thin metal layers, 'Metal3-5', stacked together. Between the two secondary windings the primary coil, connected to the PA cores, is routed on the 'TopMetal1' layer. A center tap in the primary coil is used for DC supply. A 3D rendered layout of the used transformer is shown in Fig. 4.11, as well as standalone simulation results. The transformer achieves a broadband match better than −10 dB, from 20 GHz to 48 GHz for a load impedance of 100 Ω. The simulated loss is only 0.8 dB at 28 GHz.

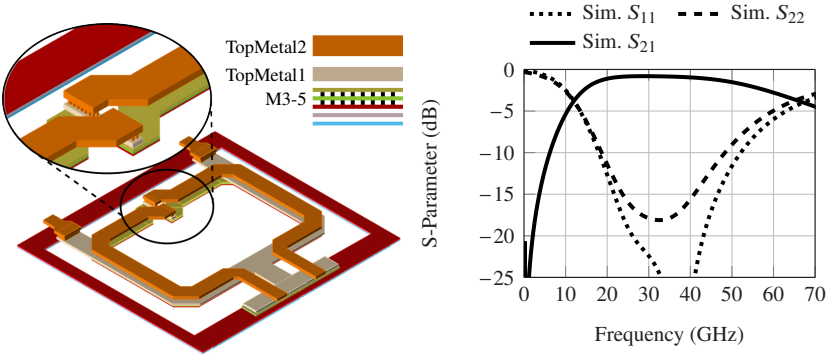


Figure 4.11: 2:1 transformer: a) 3D rendered layout and b) EM simulated S-parameters versus frequency. ©IEEE

After EM simulation of the entire PA layout, the PA is simulated to output $26.1\,\mathrm{dBm}$ at a PAE of $32\,\%$. The occupied chip area is only $0.65\,\mathrm{mm}^2$. A chip microphotograph of the PA is shown in Fig. 4.12.

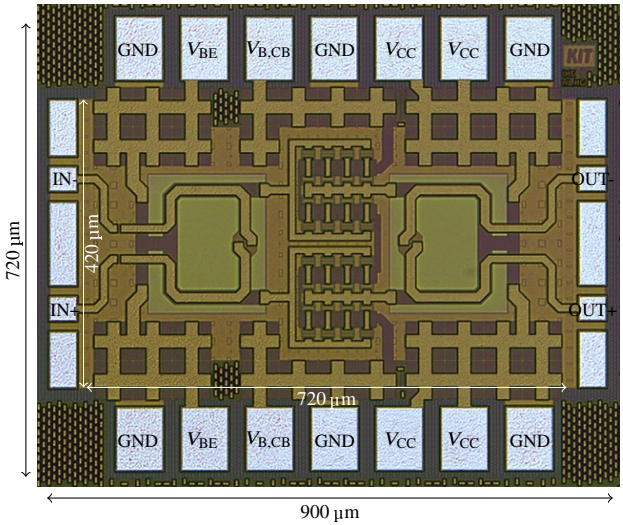


Figure 4.12: Chip microphotograph of pseudo differential K_a-band PA. Occupied chip area: $0.65\,\mathrm{mm}^2$. RF core area: $0.3\,\mathrm{mm}^2$. ©IEEE

Characterization

During characterization of the PA destructive thermal instability is discovered. To investigate the thermal stability of the PA, Keysight's ADS electrothermal simulator is used. Compared to previous simulations of this PA, in which only self-heating of the transistors is included, the electrothermal simulator includes thermal coupling between the individual transistor fingers. This is critical as the individual fingers are in close proximity to each other on this chip. Additionally, the design dissipates almost 1 W of power, elevating the temperature in the IC. Initially, the chip's bottom thermal connection to ambient ($25\,^{\circ}\mathrm{C}$) is assumed to be ideal. In this case, only the chip's bulk silicon is generating a thermal resistance between the transistors and ambient temperature. Since silicon's thermal conductivity, k_{Si}, is in the range of $145\,\mathrm{W/(m\,K)}$ and the thickness of the chip is roughly $200\,\mu\mathrm{m}$, the thermal resistance of the chip itself is in the range of $4.5\,\mathrm{K/W}$. For this case, the peak junction temperature on the chip is simulated to be $150\,^{\circ}\mathrm{C}$, which is already higher than the process specification of $125\,^{\circ}\mathrm{C}$. When the simulated peak junction temperature is observed versus input power, it decreases for increasing input power. This corresponds to an increase in PAE, as more DC power is converted to RF instead of being dissipated. The simulation results are shown in Fig. 4.13a and 4.13b.

However, during characterization a glue (Polytech TC 430 [Pol23b]) is used to attach the chip to a carrier metal. This glue layer is estimated to be $15\,\mu\mathrm{m}$ thick with a thermal conductivity, k_{TC430}, of $0.7\,\mathrm{W/(m\,K)}$. This results in an estimated thermal resistance, R_{th}, to ambient in the range of $30\,\mathrm{K/W}$. When this is included in the electrothermal simulation for the chip, the on-chip temperatures exceed $300\,^{\circ}\mathrm{C}$ and convergence could only be achieved by reducing the thermal resistance to $10\,\mathrm{K/W}$. The on-chip temperature distribution is presented in Fig. 4.13c. To reduce thermal and electrical stress of the device, the supply voltage is reduced to V_{CC} = 3.7 V and the current density is lowered by applying $0.9\,\mathrm{V}$ as V_{BE}. When the PA is simulated under these conditions it operates thermally stable for a thermal resistance of $10\,\mathrm{K/W}$ but exceeds $300\,^{\circ}\mathrm{C}$ on-chip temperatures for $30\,\mathrm{K/W}$, illustrated in Fig. 4.13d. To stabilize the temperature a resistor of $25\,\Omega$ is added in series to the V_{BE} supply line. This limits the increase in collector current when the on-chip temperature increases. Including the additional resistor the on-chip thermals are successfully stabilized to the maximum allowed value of $125\,^{\circ}\mathrm{C}$. The final on-chip temperature distribution is shown in Fig. 4.13e.

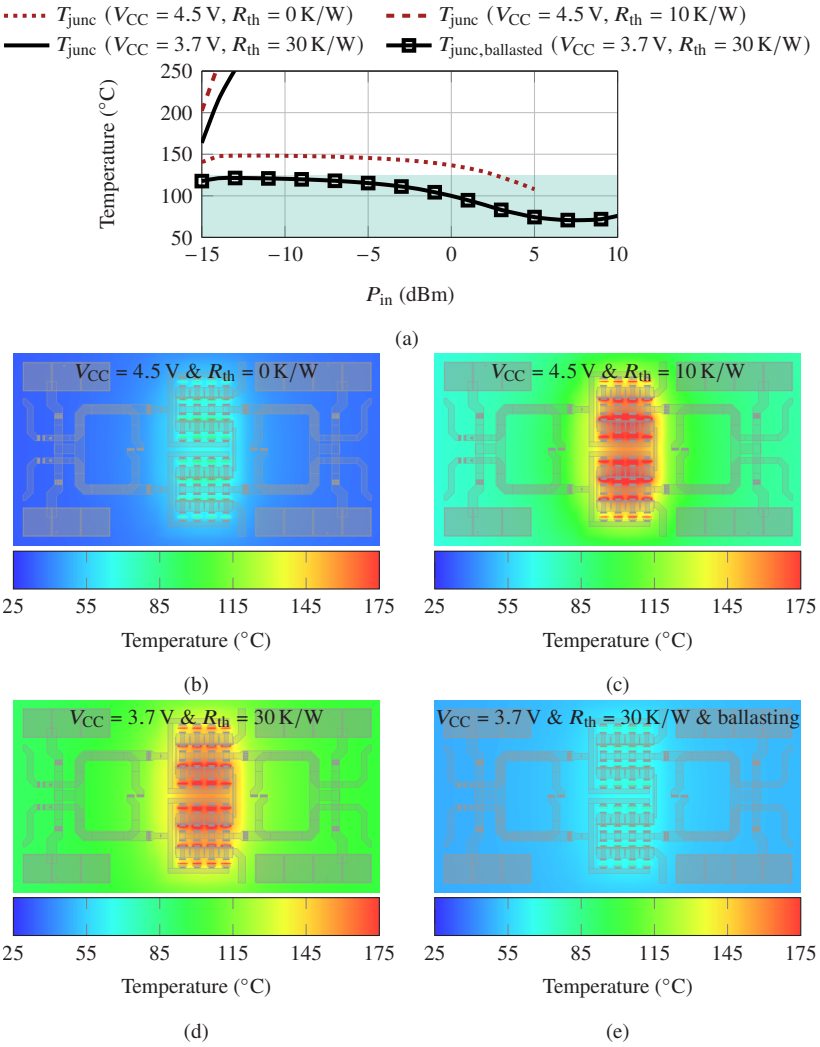
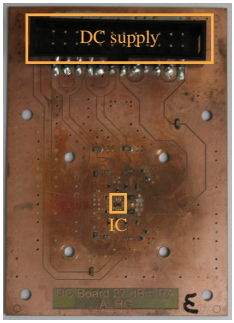
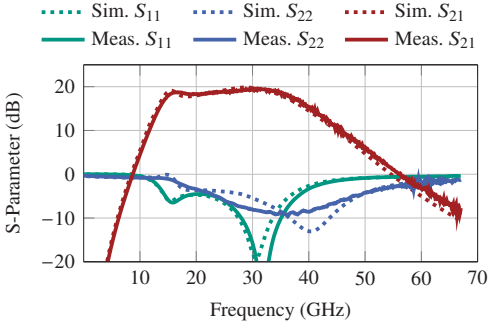


Figure 4.13: Electrothermal simulation results: a) peak junction temperature versus input power and b)-e) on-chip temperature distributions for different simulation conditions.

The reduction in supply voltage degrades the simulated performance for the saturated output power to 23.7 dBm and peak PAE to 28 %. To account for a common mode instability external capacitors and resistors are added on a DC supply PCB. The PCB is shown in Fig. 4.14a. Using the thermally stable operating point, the measurements are performed using Keysight's 4 Port PNA X in a differential setup. The small-signal measurements were carried out using a 4-port calibration. The results are shown in Fig. 4.14b and agree well with simulation. Nearly 20 dB of small-signal gain are measured, and the 3 dB bandwidth is 24 GHz.



(a)



(b)

Figure 4.14: PA characterization: a) PCB assembly and b) simulated and measured S-parameters versus frequency.

For the large-signal measurement, a differential input signal is produced by the PNA X and a power calibration is performed at the input cable. Probe loss is accounted for by data sheet values. At the output, cable loss of the measurement setup is calibrated out. The output power is then measured by the PNA through S-parameter measurements with known input power levels. The single tone large-signal measurement results at 28 GHz versus input power are presented in Fig. 4.15. At low input power an offset to the simulated values of approximately 2 dB is measured. This difference does not occur during S-parameter measurements. This phenomenon could be explained by an offset in the input power calibration at the probe tip, by overestimation of the input power. In compression, this difference is reduced, which agrees well with overestimated input power. A saturated output power of 23.7 dBm at a peak PAE of 26 % is measured. Due to the reduction in supply voltage and a change in class of

operation from class A into class AB, the output power is significantly smaller than initially designed.

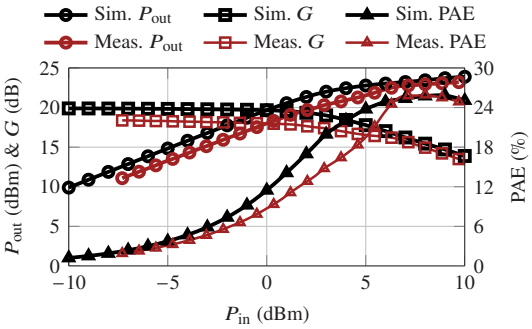


Figure 4.15: Simulated and measured large-signal parameters versus input power at 28 GHz. ©IEEE

4.2 In-phase Power Combining

Parts of the following section contain content previously published in [11].

To expand the number of combined inputs and to compare the performance to transformers, this section investigates the combining loss incurred by in-phase power combining. The configurations used as building blocks are depicted in Fig. 4.16. Compared to the classical Wilkinson combiner the isolation resistor is omitted. The isolation resistor is traditionally used to avoid changes in loading or crosstalk between the combined sources when the sources are not equal. While this is expected for combiners used between different chips, inside a single chip sufficient symmetry between the combined PA cores is expected and no extra isolation measures are needed. The remaining components are transmission lines with an electrical length of $90°$ used to match between two resistors R_S and R_L. R_S models the output of a PA core. A larger PA core typically presents

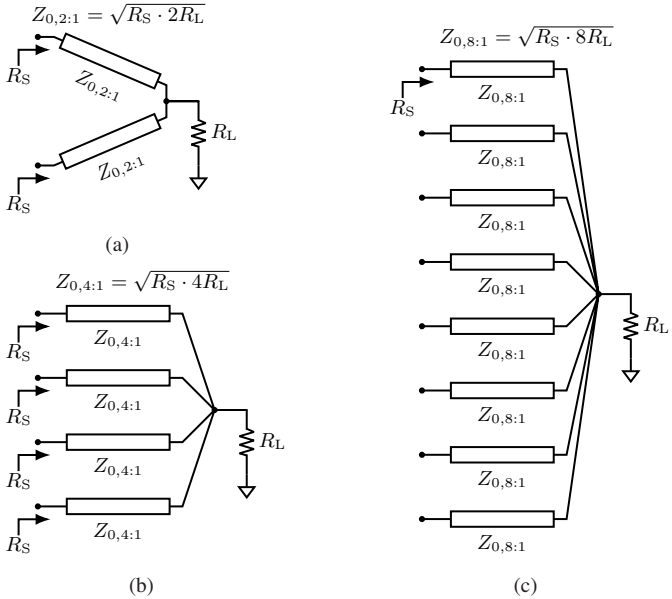


Figure 4.16: Basic single-stage combiners: a) 2-to-1; b) 4-to-1 and c) 8-to-1.

a smaller value of R_S. R_L models the load. Complex impedances could be reached by varying the electrical length of the transmission line but are not part of this analysis. Fig. 4.16a shows a single-stage 2-to-1 combiner, Fig. 4.16b a single-stage 4-to-1 combiner and Fig. 4.16c a single-stage 8-to-1 combiner. For the three cases, a formula to calculate the necessary characteristic impedance, Z_0, of the transmission lines is included in the figure.

To investigate the loss, similar to [DH17a], a transmission line with an electrical length, βl of 90° is characterized in EM simulation at 28 GHz. For the investigation, the BEOL of IHP's SG13G2Cu technology is used. The characteristic impedance for different combining scenarios is calculated using the equations from Fig. 4.16 and can be realized by changing the width of the TL. The respective TL EM models are then used to predict the losses. A simplified cross section of the BEOL and the TL setup for EM simulation is illustrated in Fig. 4.17.

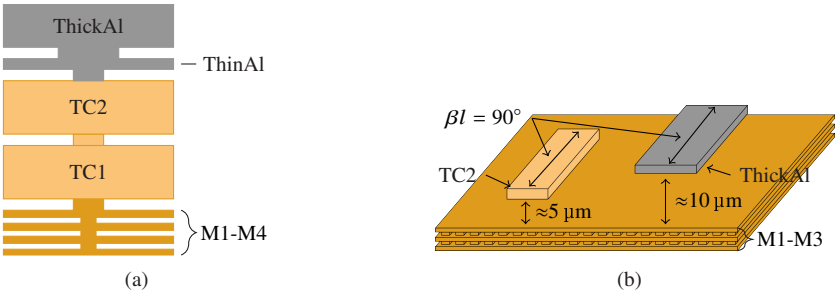


Figure 4.17: Simulation setup: a) SG13G2Cu BEOL and b) used layers for EM simulation of TLs.

Initially, the 'TC2' layer is used for integration of the TL combiner and M1-M3 are used as ground. The expected combining loss for different combinations of R_S and R_L is shown in Fig. 4.18. Fig. 4.18a presents the results for a single-stage 2-to-1 combiner, Fig. 4.18b for a single-stage 4-to-1 combiner and Fig. 4.18c for a single-stage 8-to-1 combiner. The figures are color-coded corresponding to the simulated insertion loss. The results are produced by linear interpolation between EM simulated data points. Due to physical limitations not all values of Z_0 can be realized and thus not all source resistance values can be combined into every load resistance value. This is shown by blank spaces, which become larger for a higher number of inputs. As an example, a 2-to-1 combiner can combine almost any source resistance (in the range of 5-50 Ω) into a 50 Ω load,

while an 8-to-1 combiner requires a source resistance in the range of 5-14 Ω. For all configurations, the combining loss increases towards high ratios of load to source resistance, $\frac{R_L}{R_S}$. Unintuitively, a 4-to-1 combiner's loss is increased by only 0.1 dB compared to a 2-to-1 combiner for source resistance values larger than about 20 Ω.

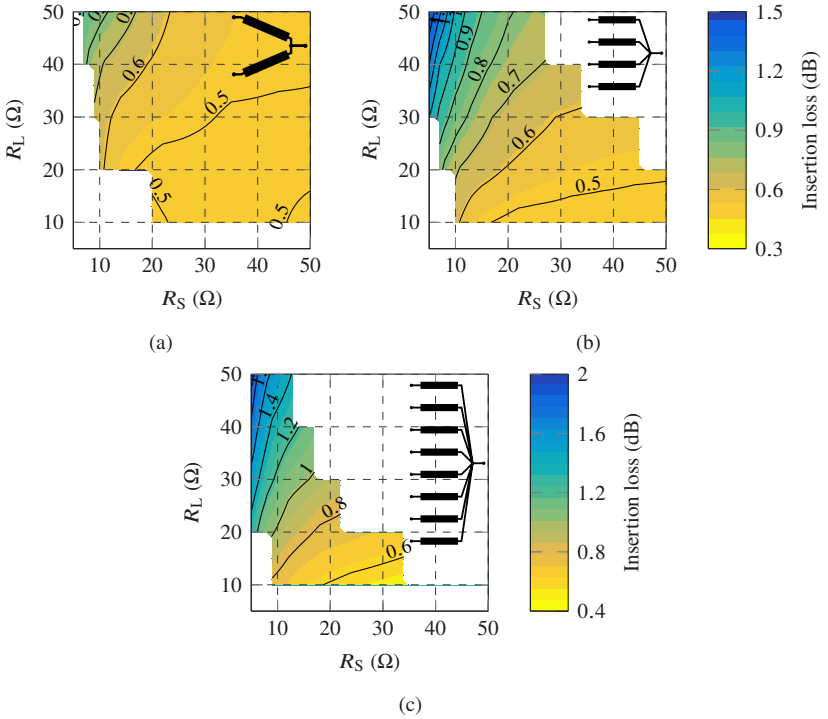


Figure 4.18: Insertion loss of power combiners for variable load and source resistances at 28 GHz: a) single-stage 2-to-1; b) single-stage 4-to-1 and c) single-stage 8-to-1 combiner.

When two stages of combiners are analyzed, as shown in Fig. 4.19a, the choice of the intermediate resistance, R_I, between the stages influences the overall combining loss. To predict the optimal intermediate resistance, the data in Fig. 4.18 is used. For a two-stage combiner, the target load resistance is fixed, generally to 50 Ω. Independent of the intermediate resistance, combining stage II must combine into the chosen load resistance. Thus, for the last stage the plot in

Fig. 4.18 is reduced to a row corresponding to the combining loss for all possible intermediate resistances that can be combined into $50\,\Omega$. By transposing this row to a column and adding it to the loss of the previous combining stage in such a way that the source resistance of the last stage is the load resistance of the first stage, the loss of both stages can be calculated for all possible combinations of R_S and R_I. The resulting map gives the combining loss in terms of source and intermediate resistance for a fixed load resistance. As an example, in Fig. 4.19b the combining loss for a two-stage combiner, consisting of 2-to-1 combiners, is presented. To illustrate the intermediate resistance's influence on the total combining loss, the combining loss of $20\,\Omega$ sources is examined. The power combination is most efficient into a $50\,\Omega$ load through a $30\,\Omega$ intermediate resistance. This is close to the geometric mean of load and source resistance ($\sqrt{R_\mathrm{S} \cdot R_\mathrm{L}}$). In the worst case, the intermediate resistance is chosen to be $10\,\Omega$ and the resulting combining loss is $0.25\,\mathrm{dB}$ higher. However, compared to the previously presented single-stage 4-to-1 combiner in Fig. 4.18b, the two-stage combiner exhibits 0.2-$0.5\,\mathrm{dB}$ higher loss. This is indicated by the results in [DH17a], where the $R_\mathrm{S} = R_\mathrm{L} = R_\mathrm{I} = 50\,\Omega$ case is presented. In this work this is being extended to variable R_S and R_I values.

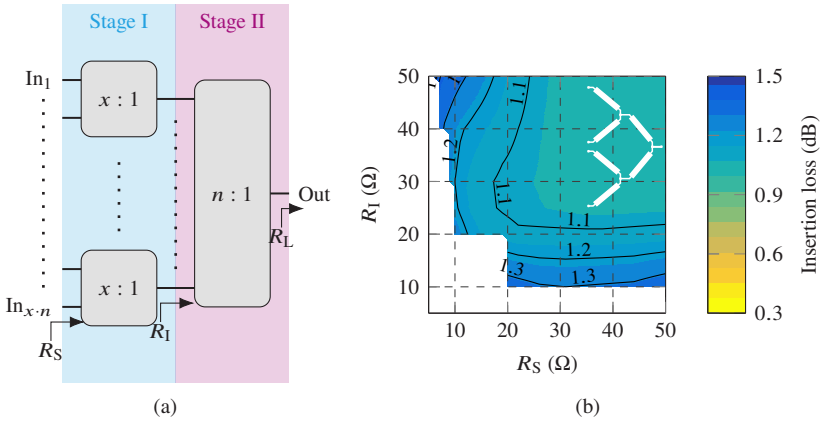


Figure 4.19: Two-stage combining: a) basic block diagram of a two-stage combiner and b) insertion loss for a two-stage combiner consisting of 2-to-1 combiners with a $50\,\Omega$ load.

Next, 8-to-1 power combination is investigated. Single-stage 8-to-1 combination, presented in Fig. 4.18c is compared with a two-stage combiner consisting

of a stage of 4-to-1 and a stage of 2-to-1 combiners. Since it is more efficient to use a single-stage 4-to-1 combiner instead of two stages of 2-to-1 combiners, given the required Z_0 for a single-stage 4-to-1 is feasible, investigating a three stage combiner consisting of 2-to-1 combiners is not pursued. The resulting combining loss for a two-stage 8-to-1 combiner consisting of a 4-to-1 combiner stage and a 2-to-1 combiner stage, ending in a $50\,\Omega$ load, is presented in Fig. 4.20. When compared to the two-stage 4-to-1 combiner in Fig. 4.19b, the 8-to-1 combiner exhibits similar losses (within $0.2\,\mathrm{dB}$) for most $R_\mathrm{S}, R_\mathrm{I}$ combinations, while combining twice as many sources, highlighting the advantage of using single-stage 4-to-1 combiners. Again, the optimal intermediate impedance is in the range of the geometric mean of source and load resistance. Compared to the single-stage 8-to-1 combiner, the two-stage 8-to-1 combiner achieves a lower combining loss by up to $0.3\,\mathrm{dB}$. This is different from the 4-to-1 case for which the single stage combination is more efficient.

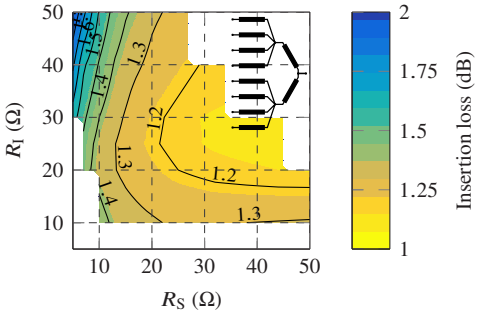


Figure 4.20: Insertion loss of a two-stage 8-to-1 power combiner into a $50\,\Omega$ load at $28\,\mathrm{GHz}$.

Lastly, optimal 16-to-1 combining is investigated. Since the results for the previous combining cases prove the superior efficiency of single-stage 4-to-1 combining, the most efficient way to combine 16 inputs appears to be two stages of 4-to-1 combiners. The resulting combining loss is presented in Fig. 4.21a achieving a total combining loss of 1.4-$1.6\,\mathrm{dB}$. However, in this case practical layout effects, such as physical distances close to the length of a $90°$ long TL may make a 4-to-1 combiner for the second stage impractical. To enable simplified implementation the outputs of two combiners in the first stage are shorted together. This halves the intermediate impedance, but stage II is reduced to a 2-to-1 combiner. The resulting combining loss is given in Fig. 4.21b showing

negligible difference to Fig. 4.21a. This topology is thus a promising choice for the on-chip combination of 16 inputs.

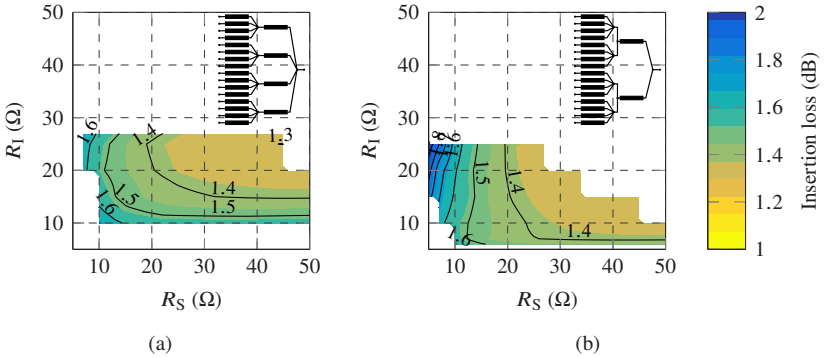


Figure 4.21: Insertion loss of two-stage 16-to-1 combining into a 50 Ω load at 28 GHz: a) two stages of 4-to-1 combiners and b) two 4-to-1 combiners shorted with 2-to-1 combiner.

Finally, the combining loss to achieve a fixed amount of power is compared. As an example, two sources with a source resistance of $R_S = 20\,\Omega$ are assumed to deliver the same amount of power as four sources with a source resistance of $R_S = 40\,\Omega$. The combining loss for the two 20 Ω sources can be seen from Fig. 4.18a, and in case of a 50 Ω load is 0.58 dB. The combining loss of four 40 Ω sources into a 50 Ω load can be read from Fig. 4.19b and is 1.03 dB for an optimal intermediate resistance. This indicates a smaller number of combining stages is preferable and thus fewer larger sources are preferable over many smaller sources for efficient power combining. If power is to be maximized, the limited number of combinable inputs also requires to maximize core output power and consequently core size.

4.2.1 Layer comparison

The presented data in section 4.2 utilizes the thick copper layers of the SG13G2Cu BEOL for implementation of the combiner's TLs. While the thick copper layers provide nearly double the conductivity compared to the 'ThickAl' layer and a larger layer thickness, the increased distance to the ground (GND) plane of the top Al layer improves the combining loss significantly. The resul-

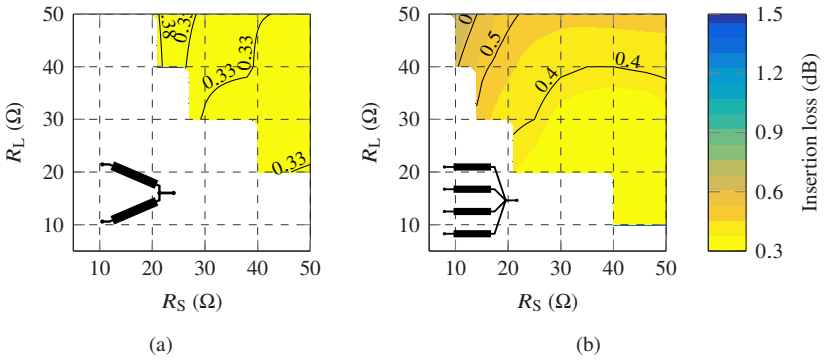


Figure 4.22: Insertion loss of power combiners for load resistance versus source resistance at 28 GHz using the 'ThickAl' layer: a) single-stage 2-to-1 combiner; b) single-stage 4-to-1 combiner.

ting combining loss is presented in Fig. 4.22a for a single-stage 2-to-1 combiner and in Fig. 4.22b for a single-stage 4-to-1 combiner in the Al layer. The improvement is in the range of 0.2-0.4 dB. However, the range of possible source and load resistance combinations is more limited in the Al layer, especially for the single-stage 2-to-1 combiner. A second disadvantage is the increased width of the TL at the same characteristic impedance, needing more chip area for the same combination compared to the Cu layer. Still, if feasible and a high efficiency is desired, including the top Al layer in the combiner design is beneficial.

In multi-stage designs the reduced coverage of the low source resistance values can be overcome by using a combiner implemented in the Cu layer as the first stage connected to the sources. This stage can be designed to show a suitable intermediate resistance to the next stage for implementation in the low loss Al layer. As an example, the combining loss of a two-stage combiner facilitating a 16-to-1 combination by using a 4-to-1 combiner in the Cu layer as stage I and a 2-to-1 combiner in the Al layer as stage II is shown in Fig. 4.23. For each input of the second stage two outputs of the first stage are shorted together. This architecture allows for the combination of 16 inputs, with source resistance values as low as 10 Ω to be combined into a 50 Ω load with a total combining loss of only 1.3 dB.

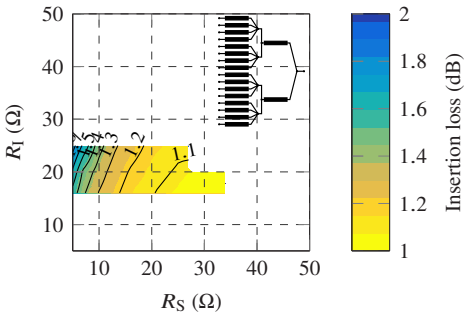


Figure 4.23: Insertion loss of a two-stage 16-to-1 power combiner into a 50 Ω load at 28 GHz, consisting of a 4-to-1 stage in the Cu layer and a 2-to-1 stage in the Al layer.

Additional data plots illustrating the performance comparisons of different combiner arrangements are included in the appendix A.2.

4.3 Conclusion

This chapter presents power combining structures and their limitations. While recent state-of-the-art publications at K_a-band, for example [WW20a, KLL$^+$24], tend to use transformer-based combining structures for PAs, the achieved and targeted output powers are at or below 28 dBm. However, the higher end of these power levels, as in [WW20a, NJW19], are typically only reached by using pads at the chip center and a differential interface, to avoid the lossy differential to single-ended conversion. To the best of the author's knowledge, for higher levels of output power only Wilkinson-like combining structures were used in previous publications. This chapter's results align well with this trend. While transformers are a useful, compact and efficient matching method, their limited geometry is unsuitable to achieve large output power levels. For high transformation ratios, adjusted coil ratios might be needed, e.g., 2:1, complicating the design significantly and increasing insertion loss. Thus, to avoid high transformation ratios, a higher number of smaller cores is required to achieve high power levels. However, the number of cores that can be combined is also limited by the layout geometry, explaining why transformer-based PAs are a popular solution for low and medium power levels below 28 dBm. For

higher power levels, TL-based combiners can combine a higher number, up to 16, of inputs, efficiently. Additionally, the transformation ratio is only limited by the available characteristic impedance, Z_0, and the number of inputs is only limited by the physical distance between the two furthest inputs approaching half a wavelength. By choosing an optimal intermediate impedance for multi-stage TL combiners, it is possible to combine 16 individual $10\,\Omega$ inputs into a $50\,\Omega$ load with an insertion loss of only $1.3\,\mathrm{dB}$.

5 Resonated Amplifier Cores

Parts of the following chapter contain content previously published in [4].

At the center of a PA is the PA core in which the amplification is facilitated through active devices in parallelized unit cells (UCs). Two typical arrangements of transistors for PA design could be identified in scientific publications for silicon-based technologies. In the past and for III/V technologies, most commonly the CE or CS configurations are used. To improve on this, extensive research has been carried out on the cascode topology and transistor stacking, especially for FET-based designs. At mmWave frequencies useful stacking is usually limited to around three to four devices. Additionally, neutralized differential pairs can be introduced. Overall, extensive research is conducted on methods to improve unit cell topologies. In this chapter, instead of further optimizing the device topology itself, large parallelization of devices inside the PA core is investigated.

To generate the simulation results presented in the following, IHP's $130\,\mathrm{nm}$ SiGe BiCMOS technology SG13G2Cu is used.

5.1 Large Device Parallelization in PA Cores

Independent of the chosen transistor arrangement, when designing a large PA core, it may not be possible to scale a single device indefinitly. This may be due to restrictions in the technology, increasing parasitics inside and around the device or thermal considerations. A possible solution is to design the PA core by repeating parallelized UCs, each containing devices with a fixed size, as is pursued throughout this thesis.

The UC arrangement used throughout this chapter is depicted in Fig. 5.1. Due to the physical size of each UC, a short parasitic line segment is needed to connect the UCs together at their inputs and outputs. The presented arrangement can

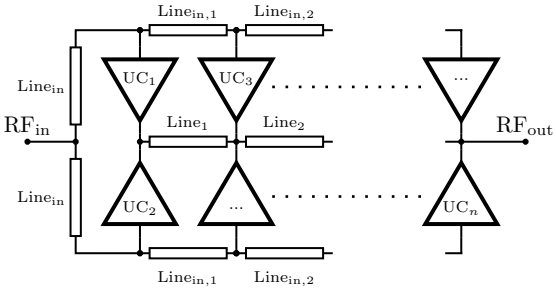


Figure 5.1: Parallel UC arrangement with phase compensation. ©IEEE

compensate the phase shift introduced by the line segments as each signal path through the core has the same length. Other arrangements for parallelization are possible, and a second example is presented in appendix A.4.

The PA cores analyzed in the following consist of cascode UCs, each with 10 finger transistors or an emitter length of $9\,\mu\text{m}$ per transistor. This is the maximum size of a single device in the chosen technology. The corresponding schematic and a 3D rendered layout are illustrated in Fig. 5.2. A parallel RC-element is introduced at the input of the UC for low-frequency stabilization. The supply voltage is chosen to be $3.5\,\text{V}$ and the UCs are biased in class AB operation. Throughout the following chapter this unit cell design is used.

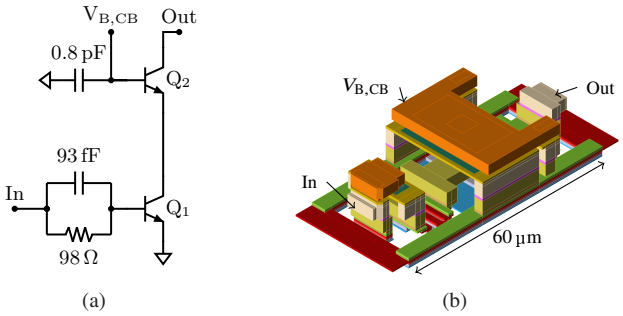


Figure 5.2: Cascode UC with $L_{\text{E,Q1}} = L_{\text{E,Q2}} = 9\,\mu\text{m}$: a) schematic and b) 3D rendered layout. ©IEEE

At 28 GHz an analysis on EM simulated PA core layouts of different total sizes is performed. Three PA core example layouts, consisting of 6, 10 and 16 parallel UCs, are presented in Fig. 5.3. The EM simulated cores are then compared to ideally parallelized PA cores in schematic without any internal parasitics.

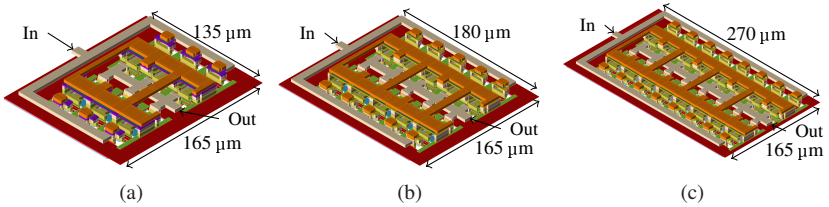


Figure 5.3: PA core layout examples: a) 6x UCs (L_{E} = 54 µm); b) 10x UCs (L_{E} = 90 µm) and c) 16x UCs (L_{E} = 144 µm).

In Fig. 5.4 resulting P_{sat} and peak PAE over the total number of UCs within a PA core are presented. For the following analysis, the number of parallelized UCs within a PA core is used as a measure of PA core size. The PA cores are ideally loaded according to their optimum load-pull impedance to maximize P_{sat}. Both the EM simulated PA cores and the PA cores in schematic show increasing output power as total PA core size increases. However, an EM simulated core consisting of 16 UCs ($L_{\mathrm{E}} = 144\,\mu\mathrm{m}$) only achieves a 1.85 dB improvement in output power compared to a core consisting of 8 UCs ($L_{\mathrm{E}} = 72\,\mu\mathrm{m}$). From

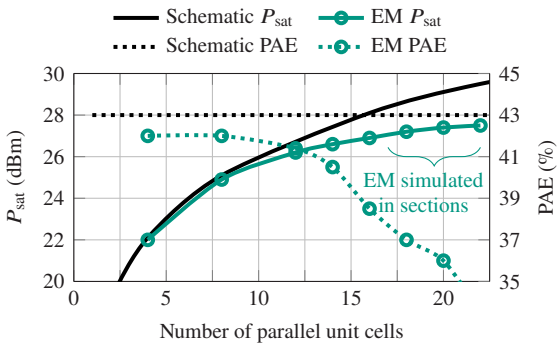


Figure 5.4: P_{sat} and $\mathrm{PAE}_{\mathrm{max}}$ versus number of parallel UCs per PA core, at 28 GHz, assuming ideal loading conditions. ©IEEE

schematic a 3 dB improvement is expected. Similarly for large EM simulated cores, even when ideally loaded, a drop in peak PAE of around 4-8 % is observed. To enable convergence of EM simulation for large cores with more than 16 UCs, the PA core is divided into multiple sections during EM simulation. By dividing a large core into multiple sections, the performance is overestimated by approximately 0.3-0.5 dB.

5.1.1 PA Core Interconnect Analysis

To investigate the drop in output power, the internal parasitics of the PA cores are analyzed. The UC outputs are modelled as a current source with a parallel resistor, r_o, and capacitor, C_o. To derive the component values, EM simulation results of a single UC are used and the large-signal output impedance is modelled by the complex conjugate of the optimum load-pull impedance for P_sat. Then, the values are calculated at a given frequency point. For a single UC, the load-pull impedance is determined to be $(62 + 48\mathrm{j})\,\Omega$, which yields $r_\mathrm{o} = 100\,\Omega$ and $C_\mathrm{o} = 44.5\,\mathrm{fF}$ at 28 GHz. The metal interconnects between the UCs are modelled as small inductors with low quality factors. These can be calculated at each position from the S-parameters of an EM simulated line segment. This yields the equivalent circuit (EC) for the PA core interconnects given in Fig. 5.5.

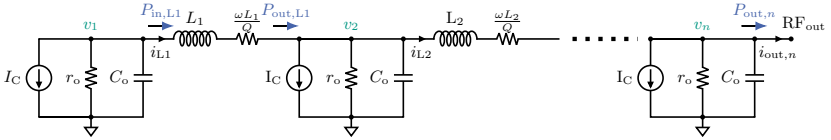


Figure 5.5: Core output interconnect equivalent circuit (EC). ©IEEE

The given model is a linear equivalent circuit during operation at the saturated output power level. Using the principle of linear superposition, all currents and voltages throughout the network can be calculated for a given load impedance connected to the $\mathrm{RF_{out}}$ node. From this an efficiency for the entire core, η_core, an efficiency for each of the interconnects, η_{L_x}, and a total efficiency for all interconnects in a core, $\eta_{\mathrm{ohm},n}$, can be calculated. The used formulas are

$$\eta_{\text{core},n} = \frac{P_{\text{out},n}}{n \cdot P_{\text{out},1}} = \frac{0.5 \cdot \text{Re}\left\{v_n \cdot i^*_{\text{out},n}\right\}}{n \cdot 0.5 \cdot \text{Re}\left\{v_1 \cdot i^*_{\text{out},1}\right\}}, \tag{5.1}$$

$$\eta_{L_x} = \frac{P_{\text{out,L}x}}{P_{\text{in,L}x}} = \frac{0.5 \cdot \text{Re}\left\{v_{x+1} \cdot i^*_{Lx}\right\}}{0.5 \cdot \text{Re}\left\{v_x \cdot i^*_{Lx}\right\}}, \tag{5.2}$$

and

$$\eta_{\text{ohm},n} = \frac{\left(\sum_{k=1}^{n-1} \prod_{i=k}^{n-1} \eta_{L_i}\right) + 1}{n}. \tag{5.3}$$

$\eta_{\text{core},n}$ relates the output power of a PA core with n unit cells ($P_{\text{out},n}$) to n times the output power of a PA core consisting of a single unit cell ($P_{\text{out},1}$). It includes any performance deterioration of a core with interconnect parasitics. $\eta_{\text{ohm},n}$ gives the total ohmic losses in the interconnects of a PA core. η_{L_x} gives the ohmic efficiency of the x-th inductor inside a PA core. For the equivalent circuit, the connected load impedance is chosen to be the complex conjugate of the impedance seen from the output, RF_{out}.

Using the equivalent circuit (EC) the results for $P_{\text{sat,EC}}$ shown in Fig. 5.6a and for $\eta_{\text{core,EC}}$ and $\eta_{\text{ohm,EC}}$ shown in Fig. 5.6b are produced. The results show that the performance of large cores deteriorates due to their internal parasitics. For

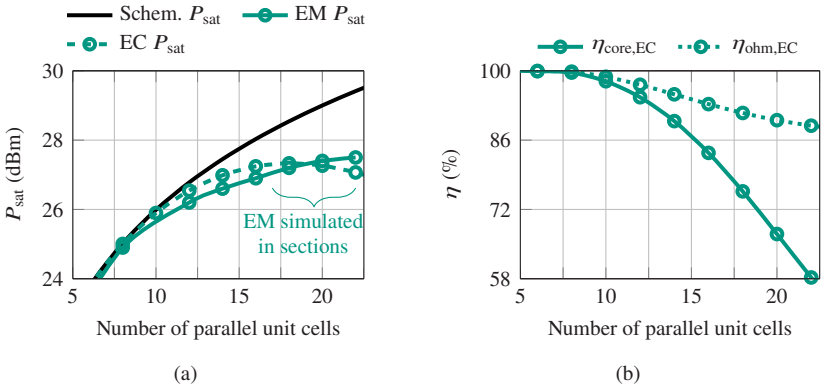


Figure 5.6: Linear analysis results for PA core output equivalent circuit: a) P_{sat}; b) internal core efficiency. ©IEEE

cores with more than 12 UCs, the overall efficiency of the core, $\eta_{\text{core,EC}}$, is significantly smaller than the efficiency expected from the ohmic losses in the inductors, $\eta_{\text{ohm,EC}}$. This is due to load variations presented to the individual current sources, which are caused by the small interconnects when the local impedances become low. By presenting non-optimal loading to the current sources, the amount of power a current source delivers to the load is reduced beyond the ohmic losses of the inductors.

5.2 Resonated Amplifier Cores

The previously described effects are most pronounced when the impedances at the input and output are below 5 to 7 Ω. To mitigate the ohmic losses and loading effects by the interconnect parasitics, this thesis proposes the concept of "Resonated Amplifier Cores". The concept is shown in Fig. 5.7. Multiple shunt inductors are directly connected to the input ($L_{\mathrm{in},x}$) and output ($L_{\mathrm{out},x}$) of the PA core UCs. These inductors are used to periodically resonate out the parasitic capacitance of the UCs to maximize the local node impedance at the input and output ($Z_{\mathrm{N},1}$, $Z_{\mathrm{N},2}$, ... and $Z_{\mathrm{in},1}$, $Z_{\mathrm{in},2}$, ...). This decreases the ohmic losses and load variations experienced inside the PA core due to the short line segments. Additionally, the matching network losses will be reduced, as the impedances to be matched at the input and output contacts are higher compared to a direct parallel UC arrangement of the same size. Furthermore, a single shunt inductor at the output of a large PA core does not help to alleviate the impact of the parasitic interconnects, because the local impedances inside the core are unaffected and thus the ohmic losses and loading effects inside the core are not reduced. Multiple DC supply paths are inherently included in the structure and current density requirements of the metals are easier to meet. For comparison, the previously presented approach in section 5.1, in which the full supply current must go through the output contact, may require impractically

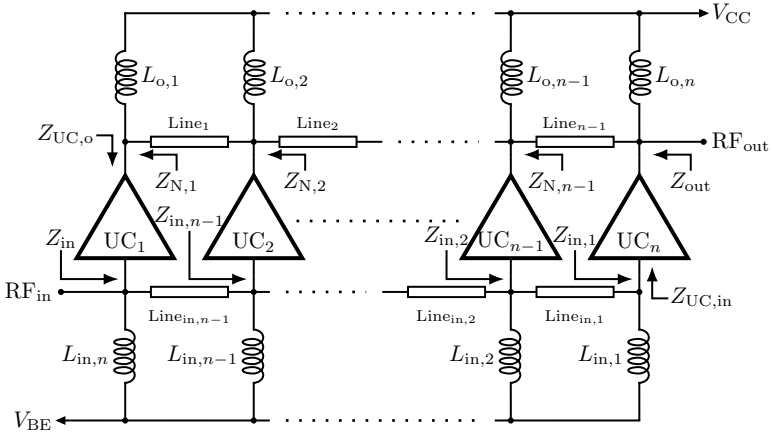


Figure 5.7: Resonated amplifier core concept schematic. ©IEEE

wide metal connections for a large PA core. Visually, resonated amplifier cores are similar to a distributed amplifier, but compared to a distributed amplifier no artificial transmission line is created by the parasitic line segments and the design is narrow band.

5.2.1 Resonated Core Interconnect Analysis

To compare the resonated cores to the previous direct device parallelization a similar equivalent circuit analysis is performed. For the analysis, the EC in Fig. 5.5 is expanded by shunt inductors at each UC output, as is illustrated in Fig. 5.8. The shunt inductors are assumed to have a quality factor of 12. The results after linear superposition are presented in Fig. 5.9. Results for the resonated core are denoted by the additional index 'res'. The resonated core is showing significant performance improvements for PA cores with more than 12 UCs ($L_\mathrm{E} > 108\,\mu\mathrm{m}$) as more power can be delivered to the load. This is due to an improvement in the overall core efficiency, by reduced ohmic losses in the interconnects and reduced variations in the impedances presented to the UCs. However, as the resonated core includes shunt inductors, the real part of the optimum load-pull impedance is larger than for direct device parallelization. Therefore, when a lossy matching network transforms a $50\,\Omega$ load to the optimum load-pull impedance, the matching network losses are expected to be smaller for the resonated core. For example, the impedance used to load the equivalent circuit of a PA core consisting of 12 UCs is calculated to be $Z_\mathrm{L,opt,EC}(12\text{x UC}) = (5.4 + 2.1\mathrm{j})\,\Omega$, whereas for the resonated core, it is calculated to be $Z_\mathrm{L,opt,res,EC}(12\text{x UC}) = 9.6\,\Omega$, corresponding to a $65\,\%$ increase in magnitude of the load-pull impedance.

Lastly, results from layouted and EM simulated resonated cores with optimized inductor values are compared to direct device parallelization from section 5.1.

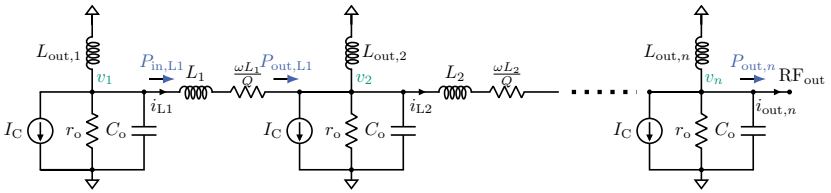


Figure 5.8: Resonated amplifier core output interconnect equivalent circuit. ©IEEE

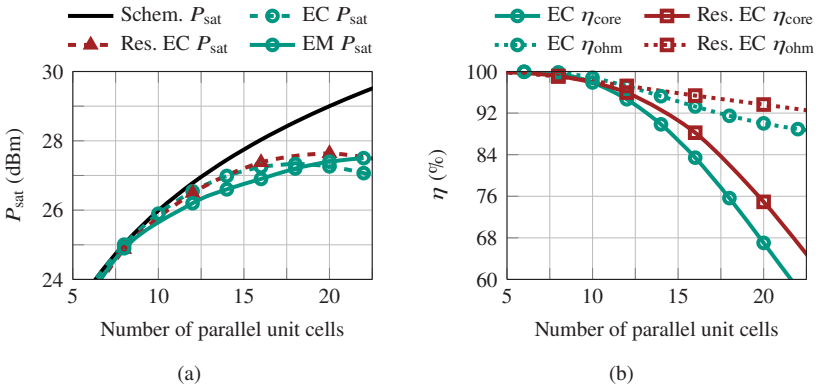


Figure 5.9: Linear analysis results for PA core output equivalent circuits: a) P_{sat} and b) internal core efficiency. ©IEEE

The comparison includes a lossy matching network to $50\,\Omega$, and the results are presented in Fig. 5.10. For the matching network, a Pi-network in L-C-L configuration is chosen to enable convenient DC supply to the classical cores. The quality factor for inductors and capacitors in the network is assumed to be $Q_L = 12$ and $Q_C = 20$, respectively. To keep the comparison fair, the same network topology is used for the resonated cores. The resulting PAE of the resonated PA cores is higher compared to the PA cores using only direct device parallelization. Towards larger cores the difference in PAE is simulated to be as large as $6\,\%$ for the same core size, while delivering nearly $1\,\mathrm{dB}$ more power to the load. This difference is expected to grow for even larger cores.

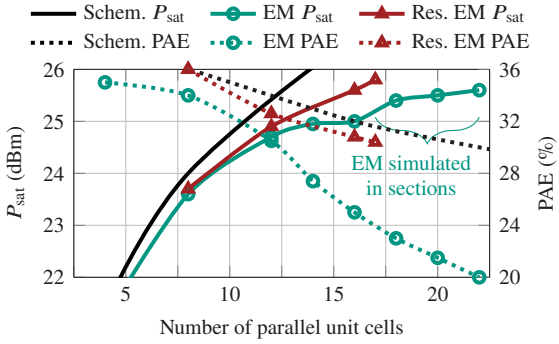


Figure 5.10: P_{sat} and $\mathrm{PAE}_{\mathrm{max}}$ versus number of parallel UCs per PA core at $28\,\mathrm{GHz}$, assuming a $50\,\Omega$ load with a lossy matching network. ©IEEE

5.3 30.8 dBm K_a-Band Power Amplifier in 130nm SiGe

Parts of the content in the following section have been previously published in [4].

In this section a K_a-band power amplifier achieving a saturated output power of $30.8\,\mathrm{dBm}$ is presented. It is implemented in IHP's SG13G2Cu SiGe BiCMOS technology. The PA consists of four resonated amplifier cores. A pair of two cores is driven differentially through transformers, and a transmission line combiner is used to combine the pairs. The resonated cores adopt the same UCs as presented in Fig. 5.2. A simplified block diagram of the overall PA is shown in Fig. 5.11.

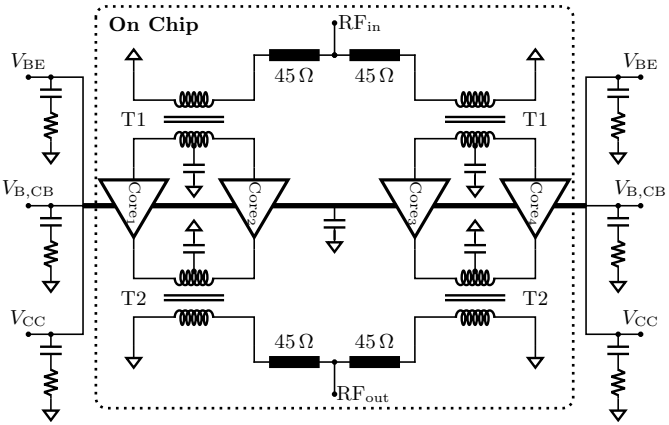


Figure 5.11: Block diagram of the $30.8\,\mathrm{dBm}$ K_a-band PA.

5.3.1 Resonated Amplifier Core Design

The resonated cores are designed using a uniform inductor size throughout the core. The inductors at the input and output of the UCs are calculated by analyzing the cascode UC for its input and load-pull impedance. The output impedance a of UC is modelled by the complex conjugate of its load-pull impedance ($Z_{\mathrm{UC,out}} =$

$Z^*_{\mathrm{UC,loadpull}}$). It is assumed that the UCs provide sufficient isolation, such that input and output can be treated separately from each other. Using the well known concept of resonance the transistor's capacitance at input and output can be resonated out at one frequency by shunt inductors of value

$$L_{\mathrm{o},x} = \frac{1}{\omega^2\, C_{\mathrm{out}}} = \frac{1}{\omega\, \mathrm{Im}\,\{Y_{\mathrm{out}}\}} \tag{5.4}$$

and

$$L_{\mathrm{in},x} = \frac{1}{\omega^2\, C_{\mathrm{in}}} = \frac{1}{\omega\, \mathrm{Im}\,\{Y_{\mathrm{in}}\}}. \tag{5.5}$$

For the calculation the influence of the parasitic interconnects between the resonated UCs is neglected. The individual resonated UCs are designed to have a real load-pull and input impedance. Fig. 5.12 presents the required resonating inductance at the input and output of a unit cell segment (UCS) at 28 GHz. The UCs are grouped in segments to reduce the required inductance for resonance. Instead of a single UC, a segment of three UCs is used per inductor. This enables area efficient implementation of the resonating inductors, as the physical width of the segment fits to the area needed for integration of the required shunt inductance. This is done to avoid an inductor layout with high aspect ratio or low quality factor.

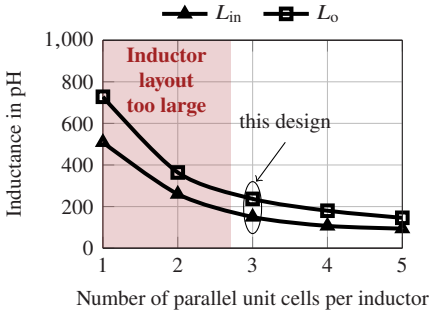
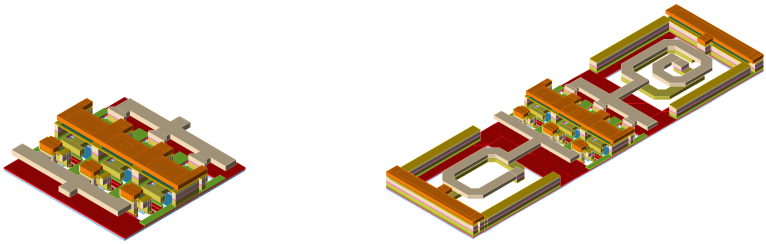


Figure 5.12: Resonating inductance at 28 GHz versus number of parallel UCs in the UC segment. ©IEEE

In Fig. 5.13a the UCS, consisting of 3 unit cells, is shown before applying the resonating inductors and in Fig. 5.13b after the resonating inductors are

connected to the unit cell segment. To design the output resonating inductor the unit cell segment's load-pull impedance for P_{sat} is observed in Fig. 5.14a. An indication of how the load-pull impedance is transformed by a shunt inductor in case of resonance is also included. At $28\,\mathrm{GHz}$, for the load-pull impedance for maximum delivered power of $(21 + 20\mathrm{j})\,\Omega$ an ideal shunt inductance of $239\,\mathrm{pH}$ is required for resonance. The load-pull contours for maximum PAE are shown in Fig. 5.14b and an optimal PAE is achieved at $(20.5 + 25\mathrm{j})\,\Omega$. At $28\,\mathrm{GHz}$, this yields a required shunt inductance of $237\,\mathrm{pH}$. This is similar to the value for optimal output power, however the projected impedance for optimal PAE is higher and is therefore further pursued.



(a) (b)

Figure 5.13: 3D rendered cascode UCS design: a) before resonating and b) resonated. ©IEEE

After applying the shunt inductor and EM simulation, the load-pull contours for optimal P_{sat} and optimal PAE are presented in Fig. 5.14c and 5.14d, respectively. A slight deviation towards lower impedances is visible. This is due to the limited quality factor of the chosen inductor. At the input, the input impedance of $(8 - 23\mathrm{j})\,\Omega$ is resonated out by a $146\,\mathrm{pH}$ inductor to achieve a theoretical input impedance of $74\,\Omega$. After EM simulation the input impedance is simulated to be $(79 - 3\mathrm{j})\,\Omega$. The deviation is expected to be caused by the finite isolation between input and output and other parasitic effects not captured without EM simulation.

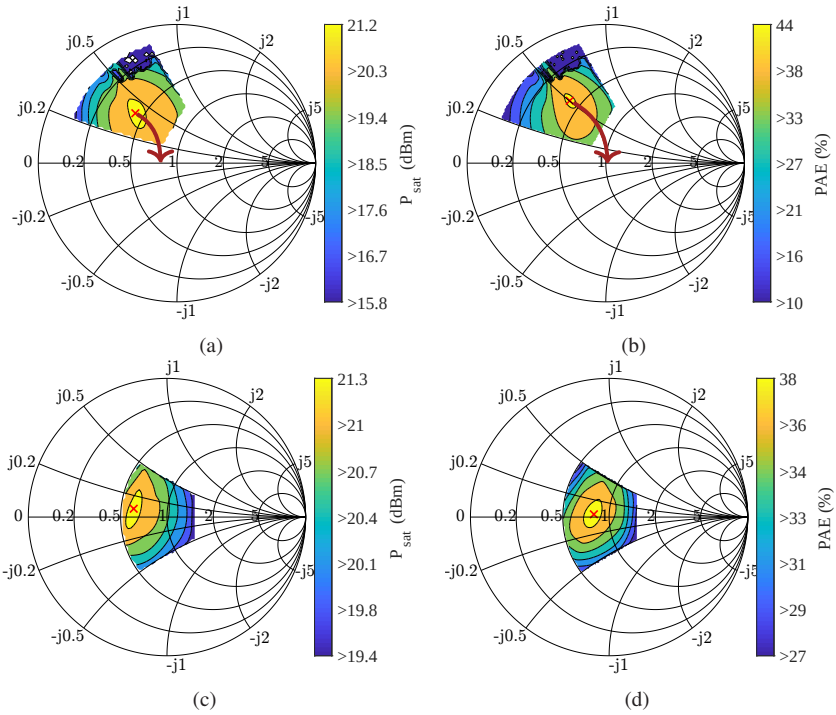


Figure 5.14: Resonated cascode UC segment design: Load-pull contours for a) P_{out} before resonance; b) PAE before resonance; c) resonated P_{out} and d) resonated PAE.

The designed resonated UCS is repeated four times. The resulting resonated core schematic is presented in Fig. 5.15a and a 3D rendered model of the entire core is shown in Fig. 5.15b. The large-signal simulation results after EM simulation of the entire core layout are presented in Fig. 5.15c. The resonated PA core outputs $26.4\,\mathrm{dBm}$ at a maximum PAE of $35\,\%$ in class AB operation. The supply voltage is set to be $3.9\,\mathrm{V}$ from which the core draws $300\,\mathrm{mA}$ in saturation. The input impedance, Z_{in}, and the load-pull impedance, Z_{LP}, are simulated to be $(15 + 10\mathrm{j})\,\Omega$ and $(12 - 2.5\mathrm{j})\,\Omega$, respectively. Since the interconnect parasitics within the core are neglected during calculation of the resonating inductors, the overall load-pull impedance after EM simulation of the entire PA core is expected to have a negative imaginary part.

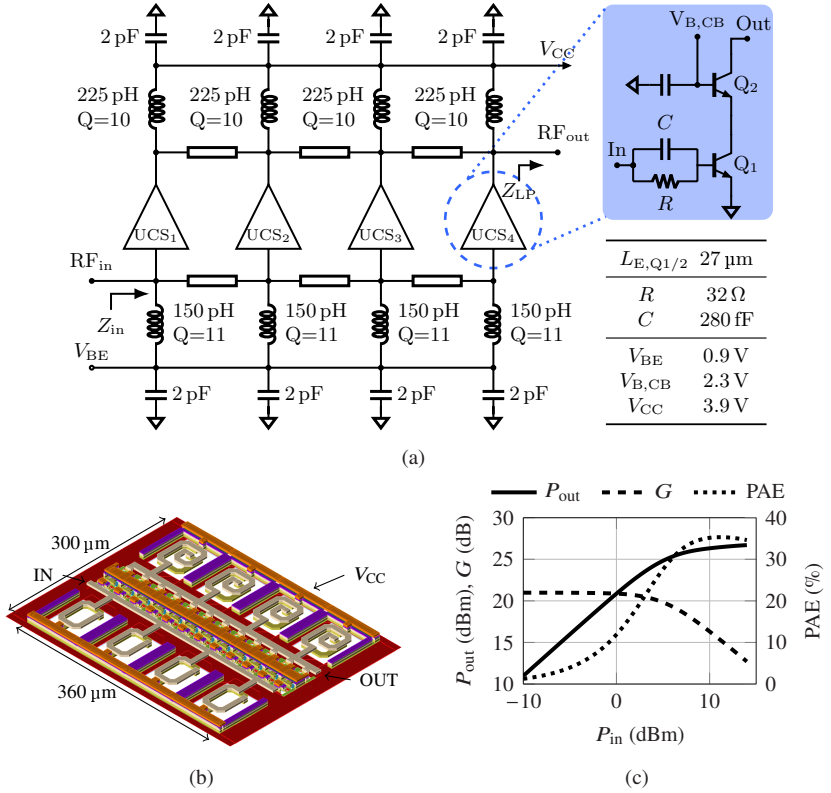


Figure 5.15: Resonated amplifier core: a) schematic, b) 3D rendered EM model ©IEEE and c) large-signal simulation results at 28 GHz.

To confirm optimal choice of resonating inductance (for uniform inductor size throughout the core), first the input inductors are kept at their initial value and the output inductors are replaced by variable inductors in simulation. The inductors have a quality factor of 12 and no variation between the individual output inductors is investigated. For each iteration, load-pull simulations are performed to find the optimal load impedance and the corresponding saturated output power and PAE. The results are presented in Fig. 5.16. When the output inductance is swept ('vs L_{out}'), the value chosen by the introduced design technique shows the highest saturated output power and efficiency for the tested

values. The same procedure is repeated at the input. This time the output inductors are kept at their original value, and the input inductors are swept in simulation. While for values smaller than $150\,\mathrm{pH}$ the performance declines, due to the additional reduction in local impedance, a larger input inductance only marginally affects the performance. At some point, significantly larger inductance values would deteriorate performance due to lower quality factors when implemented in a real BEOL.

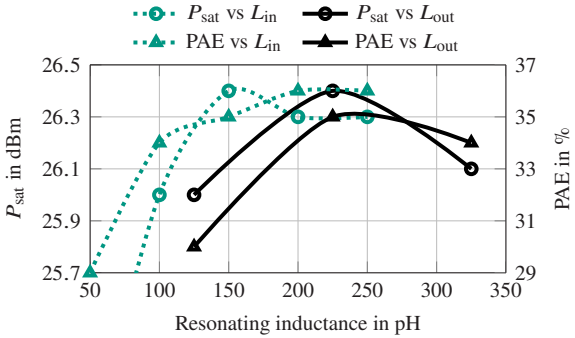
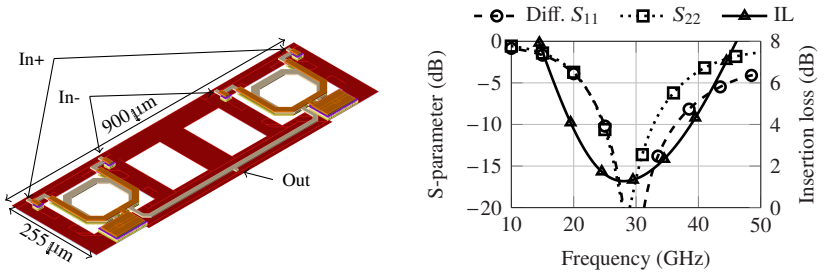


Figure 5.16: Resonated PA core performance versus L_{out} and L_{in}. ©IEEE

5.3.2 Power Combiner Design

The output combiner is a transformer- and TL-based combiner. The TLs transform the load resistance of $50\,\Omega$ to an impedance of $(54 - 42\mathrm{j})\,\Omega$ presented to each of the transformers. The output transformers then transform this to a differential impedance of $(24 - 5\mathrm{j})\,\Omega$, or $(12 - 2.5\mathrm{j})\,\Omega$ per core. While this combiner is very compact, the usage of transformers in this case is suboptimal. Transformers are typically designed to compensate the capacitive nature of a transistor, however, this compensation is already performed by the inductors within the core. Hence, small parallel capacitors had to be integrated into the transformers to achieve an impedance match better than $-10\,\mathrm{dB}$ in the final circuit. A 3D rendered model of the combiner, and its EM simulation results are provided in Fig. 5.17. When excited with ideal differential sources of equal amplitude, an insertion loss of $1.3\,\mathrm{dB}$ is expected at $28\,\mathrm{GHz}$. However, during operation of the PA, an additional penalty of approximately $0.3\,\mathrm{dB}$ is expected.

This is caused by the amplitude and phase imbalance incurred by the input transformer during single-ended to differential conversion of the input signal.



(a) (b)

Figure 5.17: Power combiner: a) 3D rendered layout and b) simulation results versus frequency.

A microphotograph of the PA is presented in Fig. 5.18. It occupies a total chip area of $1.6\,\mathrm{mm}^2$.

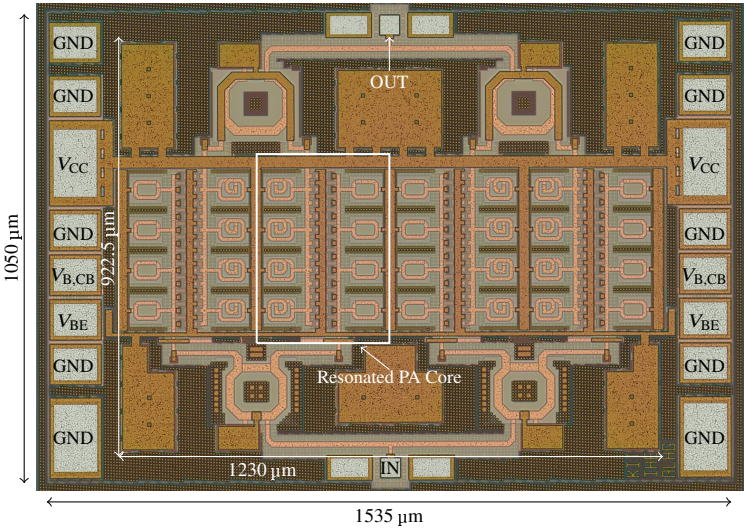


Figure 5.18: Chip microphotograph. Area: $1.6\,\mathrm{mm}^2$. RF core area: $1.13\,\mathrm{mm}^2$. ©IEEE

5.3.3 On-chip Thermal Analysis

The thermal management requires additional attention for the characterization of this PA. Previously presented amplifier designs in chapters 3 and 4 are measured using a commercially available die attach glue, Polytec's TC 430 [Pol23b], with a thermal conductivity of $k = 0.7\,\mathrm{W/(m\,K)}$. To attach the die, the liquid glue is dispensed onto the chip carrier, e.g., a PCB or metal plate, the chip is positioned on top of the dispensed glue and then the glue is cured by applying heat. Since the glue has a relatively low thermal conductivity, a thin glue layer is desired, however, minimum glue layer thickness is limited by the filler particles used inside the respective glue. For Polytec's TC 430 the filler particle size is smaller than $20\,\mu\mathrm{m}$. The described setup is illustrated in Fig. 5.19a. Assuming that heat transfer is equally distributed through the whole die attach layer and no imperfections occur, the interface can be simplified to an equivalent thermal resistance. For the presented chip size of $1.6\,\mathrm{mm}^2$ the resulting thermal resistance to ambient versus die attach layer thickness, h, is presented in Fig. 5.19c for Polytec's TC 430, Polytec's EC 101 and indium. Polytec's TC 430 shows the highest thermal resistance over layer thickness. For the designed PA, it is expected to present a thermal resistance of approximately $13\,\mathrm{K/W}$ at a layer thickness of $15\,\mu\mathrm{m}$. Polytec's EC 101 is an electrically conductive glue and thus shows a higher thermal conductivity of $k = 1.3\,\mathrm{W/(m\,K)}$ [Pol23a]. However, the metal fillers inside the glue are larger (at most $30\,\mu\mathrm{m}$) compared to TC 430 and thus a larger layer thickness is required. Subsequently a minimum thermal resistance of $12\,\mathrm{K/W}$ is estimated for EC 101 and no significant improvement is possible. Metals, such as indium, inherently provide high thermal conductivity. For indium, the thermal conductivity is in the range of $k \approx 80\,\mathrm{W/(m\,K)}$ and the expected thermal resistance of the attach layer is below $1\,\mathrm{K/W}$. For all materials, the expected value is marked by an arrow in the figure. Since indium's melting point is comparably low, $T_{\mathrm{liquid}} \approx 157\,^{\circ}\mathrm{C}$, it can be used similarly to the glues. A patch of indium foil is positioned below the chip. Then, the chip is positioned on top of the metal patch and pressed onto the indium patch while heat is applied. The indium setup is illustrated in Fig. 5.19b and is similar to the glue setup.

Using the calculated values for the thermal resistances electrothermal simulations are performed on the PA using Keysight's ADS. For both materials $2\,\mathrm{K/W}$ are added to the total thermal resistance, R_{th}, to account for the connected heatsink and imperfections during the measurement. In both cases an ambient

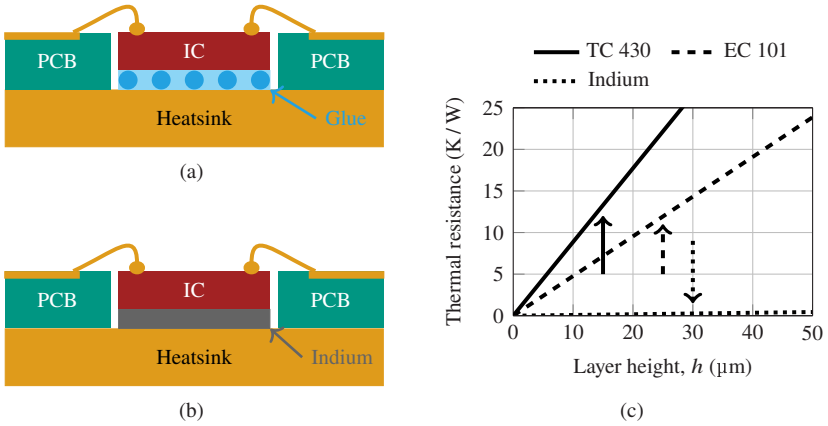


Figure 5.19: Thermal management analysis: a) IC attached by glue; b) IC attached by indium; c) thermal resistance versus layer height, h, for $1.6\,\mathrm{mm}^2$ IC area.

temperature of $25\,^\circ\mathrm{C}$ at the heatsink is assumed. In Fig. 5.20a and 5.20b the simulated on-chip temperature distributions are presented in quiescent operation for a class AB bias point. For the glue as the die attach material a peak junction temperature of $278\,^\circ\mathrm{C}$ is simulated. For indium as the die attach material a peak junction temperature of $148\,^\circ\mathrm{C}$ is expected.

For the glue, the temperature between the PA cores only drops to around $160\,^\circ\mathrm{C}$, while for indium the temperature between the PA cores is close to ambient, thus for indium the PA cores are almost thermally decoupled from each other. In comparison, a high thermal resistance results in thermal coupling between the PA cores and a $130\,^\circ\mathrm{C}$ higher temperature. This effect is not visible when only self-heating of individual transistors is observed. In large-signal simulation, including thermal simulations, increasing the input power level leads to non-convergence of the harmonic balance (HB) solver for the glue layer, shown in Fig. 5.20c for output power at 28 GHz. In Fig. 5.20d junction temperatures, T_{junc}, beyond $400\,^\circ\mathrm{C}$ show that the PA would be destroyed due to thermal runaway during the measurement if no extra measures are taken. Using indium as the interface this effect is not visible. In contrast, junction temperatures decrease with higher input drive, as less DC power is dissipated and instead converted to RF power. For the characterization, the PA is thus bonded onto a metal heat sink using an indium layer.

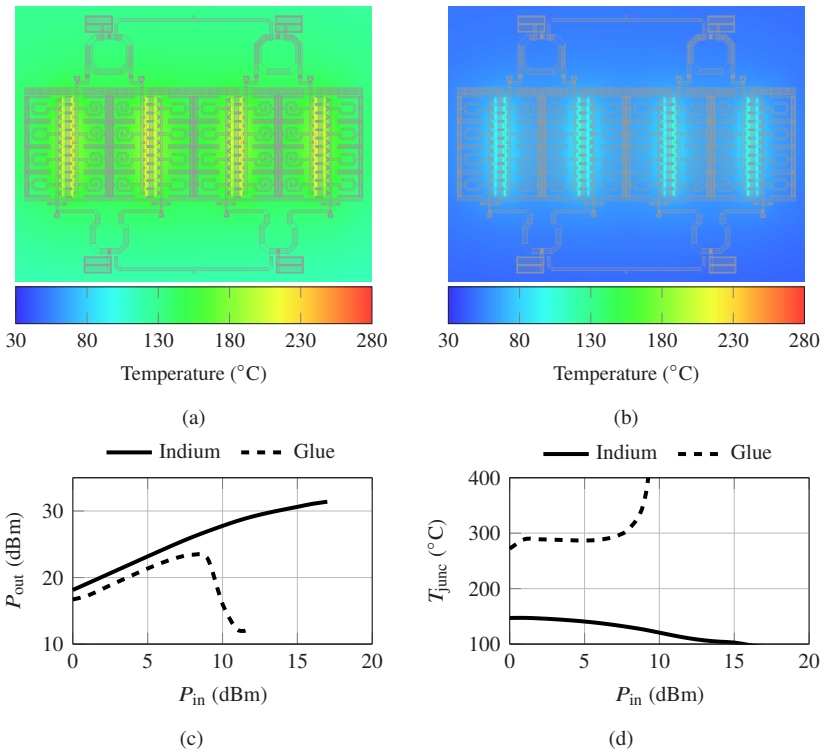
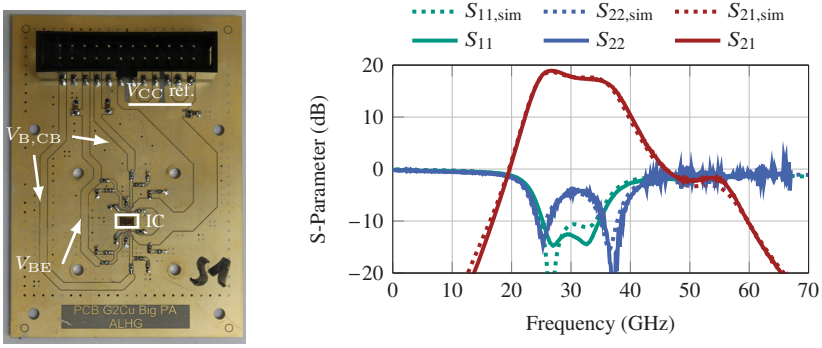


Figure 5.20: Electrothermal simulation of the K_a-band PA: a) on-chip thermal simulation (TC 430, $R_{th} = 15\,\mathrm{K/W}$); b) on-chip thermal simulation (indium, $R_{th} = 3\,\mathrm{K/W}$); c) output power versus input power at 28 GHz and d) junction temperature versus input power at 28 GHz.

5.3.4 Characterization

For the measurement the RF pads are directly probed and DC is supplied through wire bonds connected to a PCB. The PCB is shown in Fig. 5.21a. As the current consumption of this PA is high, a reference path for the supply voltage, V_{CC}, is included in the PCB. The reference plane for the supply voltage is thus moved closer to the IC. The PA is operated with $V_{CC} = 3.9\,\mathrm{V}$, $V_{B,CB} = 2.3\,\mathrm{V}$ and $V_{BE} = 0.9\,\mathrm{V}$. The small-signal simulation and measurement results are presented in Fig. 5.21b. They show excellent agreement. A small-signal gain of 18 dB is measured at 28 GHz. The input return loss is better than $-10\,\mathrm{dB}$

from 25 to 35 GHz. Towards frequencies higher than 40 GHz, the calibration is imperfect for port 2 due to high attenuation in the output path. This results in ripples in the measured data.



(a) (b)

Figure 5.21: PA characterization: a) PCB assembly and b) measured and simulated S-parameters versus frequency.

The large-signal measurements are carried out using a signal generator connected to an external driver amplifier. The input power levels are calibrated to the end of the cable connected to the input probe. Probe mismatch and loss is accounted for by performing a two-tier calibration. First, a calibration is performed that shifts the reference plane to the end of the cable, which is connected to the probe's coaxial adapter. Then a second calibration on a known calibration substrate is performed to acquire the S-Parameters of the probe. Output power is measured by a power meter. The output cable and attenuator loss are calibrated out. The setup is illustrated in the appendix in Fig. A.1b. The single-tone measurement results at 28 GHz are shown in Fig. 5.22a. The measurement shows very good agreement with simulation. A saturated output power of 30.8 dBm is measured. Large-signal measurement results for saturated output power and maximum PAE versus frequency are presented in Fig. 5.22b. From 26 to 32 GHz the PA can deliver more than 30 dBm of power with a PAE of 23.5 % or more. In the same frequency range, the output power at 1 dB compression is measured to be in the range of 25.5 to 28 dBm.

Modulated measurements are performed for a 200 MBd, 400 MBd 64-QAM and a 100 MBd 256-QAM signal. The corresponding constellation diagrams

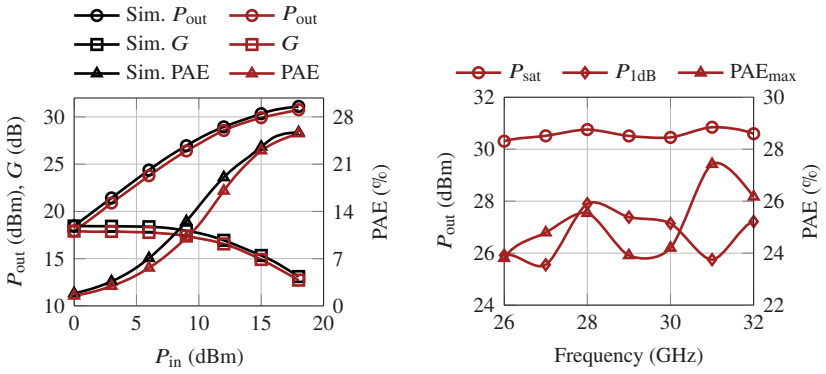


Figure 5.22: Large-signal measurement: a) measured and simulated P_{out}, gain and PAE versus P_{in} at 28 GHz and b) P_{sat} and PAE_{max} versus frequency.

are presented in Fig. 5.23. The roll-off factor, α, is set to 0.35. For the 200 MBd 64-QAM signal an average output power, $P_{out,avg}$, of 22.8 dBm with an average PAE, PAE_{avg}, of 7.1 % is measured.

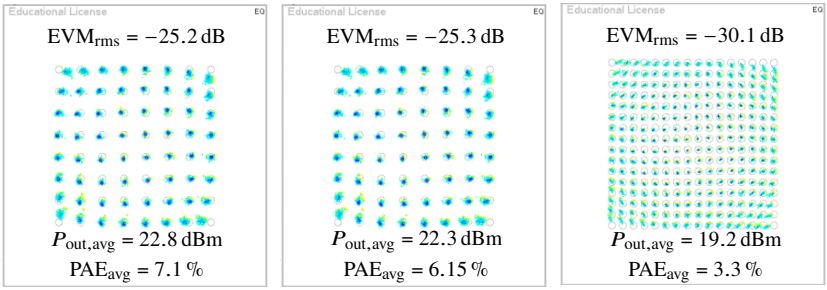


Figure 5.23: Constellation diagrams of modulated measurements: a) 200 MSym/s 64-QAM. b) 400 MSym/s 64-QAM and c) 100 MSym/s 256-QAM. ©IEEE

5.4 24 dBm Q-Band Power Amplifier in 22nm FDSOI

Parts of the content in the following section have been previously published in [9].

A high power PA is designed in GlobalFoundries' $22\,\mathrm{nm}$ FD-SOI technology further expanding upon the resonated amplifiers core method. It delivers a saturated output power of $24\,\mathrm{dBm}$ at $38\,\mathrm{GHz}$. The PA block diagram is presented in Fig. 5.24. It consists of four identical resonated cores. At the input and output of the PA cores a single-stage 4-to-1 in-phase power splitter and combiner are used. At the output, a combining loss of $0.95\,\mathrm{dB}$ is expected from EM simulation.

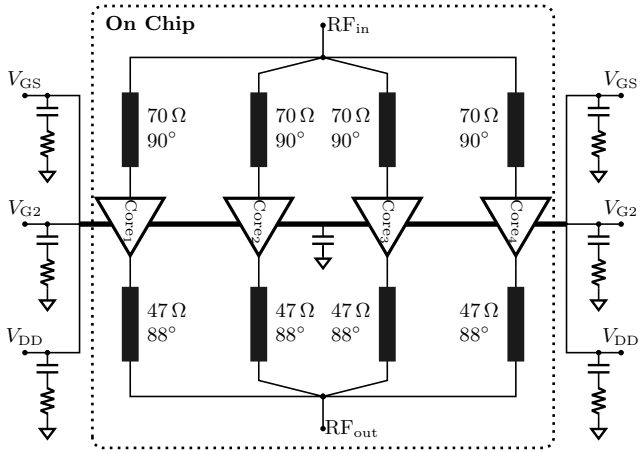


Figure 5.24: Q-Band PA schematic.

5.4.1 Resonated Amplifier Core Design

This design's resonated core adopts an advanced design method with non-uniform inductor size throughout the resonated core. For this design method, the influence of the parasitic interconnects between the resonated unit cell seg-

ments is included during the calculation of the resonating inductors. Similar to the core analysis at the start of this chapter, the parasitic interconnects are modelled as small inductors with low quality factor, $L_{\mathrm{p},x}$. The method's idea remains to achieve real load-pull and input impedances. As the parasitic inductors contribute to the compensation of the capacitance, each successive inductor within the core has to compensate for less capacitance. This introduces a gradient for the shunt inductor values. The shunt inductors become larger towards the input and output contact point ($L_{\mathrm{o},1} < ... < L_{\mathrm{o},n}$, $L_{\mathrm{in},1} < ... < L_{\mathrm{in},n}$). However, by adjusting the inductors within the PA core, the node impedances at the input and output of the UCs are accurately compensated and maximized. Since each previous node influences the next node, the quality factor of the shunt inductors must be included during the calculation. The calculation is only shown for the output side but can be applied to the input in the same way. For x = 1 the shunt inductor can be calculated as in the uniform case, with

$$L_{\mathrm{o},1} = \frac{1}{\omega \,\mathrm{Im}\left\{Y_{\mathrm{UC,out}}\right\}}. \tag{5.6}$$

To include the effect a shunt inductor has on the following shunt inductors, its admittance (including quality factor), $Y_{L,\mathrm{out},1}$, is then added to the node admittance

$$\frac{1}{Z_{\mathrm{N},1}} = Y_{\mathrm{N},1} = Y_{\mathrm{UC,out}} + Y_{L,\mathrm{out},1}. \tag{5.7}$$

For x>1 the calculation changes as the parasitic impedance of $L_{\mathrm{p},x}$ is added. The node admittance at position x before resonance, $Y_{\mathrm{N},x,\mathrm{noL}}$, is then calculated with

$$Y_{\mathrm{N},x,\mathrm{noL}} = \frac{1}{\dfrac{1}{Y_{\mathrm{N},x-1}} + Z_{L_{\mathrm{p},x-1}}} + Y_{\mathrm{UC,out}}. \tag{5.8}$$

The required shunt inductance to resonate this admittance is calculated and the inductor admittance is then added to the node admittance at position x. The resonated node impedance becomes

$$\frac{1}{Z_{\mathrm{N},x}} = Y_{\mathrm{N},x} = Y_{\mathrm{N},x,noL} + Y_{L,\mathrm{out},x}. \tag{5.9}$$

This is an iterative solution starting at UCS_1 for the output and at the n-th UC segment for the input. Because of this procedure inductor size increases. Fig. 5.25 shows the required inductance versus UC segment position in the PA core at $40\,\mathrm{GHz}$. Especially at the output, inductors become large and thus hard to integrate in limited space. The associated quality factor also declines. The core is thus limited to four UC segments.

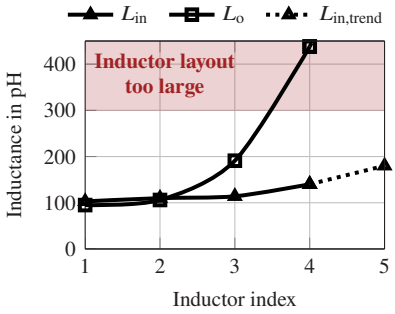
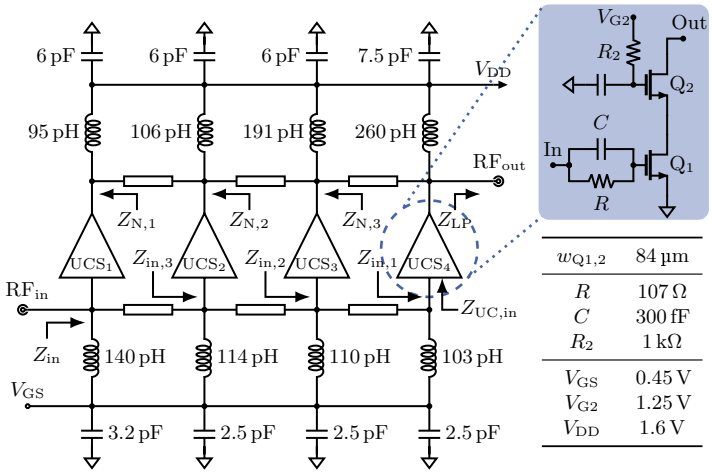


Figure 5.25: Resonating inductance versus inductor position in the PA core in $22\,\mathrm{nm}$ FD-SOI ($40\,\mathrm{GHz}$).

The schematic of the resonated core is shown in Fig. 5.26. Series metal-oxide-metal (MoM) capacitors are placed towards the $\mathrm{RF_{in}}$ and $\mathrm{RF_{out}}$ contacts of the core. This is only done for DC-blocking. The UCs contain a cascode configuration with a parallel RC-element at the input, decoupling capacitors at the upper gate and a large resistor for the upper gate bias supply. The gate width for each UC is $84\,\mu\mathrm{m}$. In this design, a UC segment consists of a single UC and the segment size is constant throughout the core. Thus, in this section UC and UCS are interchangeable.

This resonated core is simulated to deliver $19.6\,\mathrm{dBm}$ to a load impedance of $(11.5 - 6.5\mathrm{j})\,\Omega$ with a peak PAE of $28.4\,\%$. The load-pull impedance has a negative imaginary part as the last inductor in the core design is smaller than what is required for perfect resonance. A higher inductance was impractical due to spatial limitations and decreasing inductor quality factor. The input impedance, including the DC blocking capacitor, is simulated to be $(25 + 9\mathrm{j})\,\Omega$. After adding the DC blocking capacitor at the output, the output power is reduced to $19.3\,\mathrm{dBm}$ at a peak PAE of $27\,\%$ for a load-pull impedance of $(11.5 + 3.5\mathrm{j})\,\Omega$.



$w_{Q1,2}$	84 µm
R	107 Ω
C	300 fF
R_2	1 kΩ
V_{GS}	0.45 V
V_{G2}	1.25 V
V_{DD}	1.6 V

Figure 5.26: Q-band resonated amplifier core schematic.

To compare the designed resonated core to traditional cores, table 5.1 summarizes key parameters of different PA core designs with varying number of parallel UCs in this technology. A single UC (1x UC), three parallel UCs (3x UC) and four parallel UCs (4x UC) are compared to the resonated core. A single UC (1x UC), without shunt inductors, is simulated to have a load-pull and input impedance of $(10+13.8\text{j})\,\Omega$ and $(7.7-22.4\text{j})\,\Omega$, respectively. Theoretically, if

Table 5.1: Large-signal PA core performance at 40 GHz ©IEEE

Core size	1x UC	3x UC	4x UC	**4x UC resonated**
Total gate width	84 µm	252 µm	336 µm	336 µm
$Z_{L,opt,sim}$	$(10+13.8\text{j})\,\Omega$	$(6.2-6.3\text{j})\,\Omega$	$(4.3-9.1\text{j})\,\Omega$	$(11.5-6.5\text{j})\,\Omega$
$Z_{in,sim}$	$(7.7-22.4\text{j})\,\Omega$	$(5.28+2\text{j})\,\Omega$	$(6.5+7\text{j})\,\Omega$	$(25-9\text{j})\,\Omega$
P_{sat}	15.4 dBm	17.2 dBm	16.5 dBm	19.6 dBm
PAE	40.8 %	18.4 %	7.3 %	28.4 %

the same number of UCs are parallelized as in the presented resonated core, but without shunt inductors, the load-pull and input impedance for four unit cells would be in the range of $(2.5+3.45\mathrm{j})\,\Omega$ and $(1.93-5.6\mathrm{j})\,\Omega$, respectively. However, the theoretical values assume ideal parallelization in schematic. After EM simulation of the entire core layout consisting of four UCs, the PA core is simulated to have a load-pull impedance of $(4.3-9.1\mathrm{j})\,\Omega$ and an input impedance of $(6.5+7\mathrm{j})\,\Omega$. The difference between theoretical and EM simulated impedance values is caused by the short parasitic line segments between the unit cells. In relative terms the magnitude of the load-pull impedance is changed by around $100\,\%$, indicating performance is degraded by the line segments. Thus, the PA core with four unit cells only outputs $16.5\,\mathrm{dBm}$ with a PAE of $7.3\,\%$ into its load-pull impedance. This does not include further performance deterioration due to matching network loss. The same effect, albeit not as strong, is noticeable for a PA core consisting of three unit cells. For optimum load impedance, $Z_{\mathrm{L,opt,sim}}$, and input impedance, Z_{in}, the resonated core provides a larger real part compared to all other cores. Compared to the single UC the peak PAE is reduced, however the output power is $4.2\,\mathrm{dB}$ higher.

A chip microphotograph is provided in Fig. 5.27. The overall chip measures $1025\,\mu\mathrm{m}$ by $1600\,\mu\mathrm{m}$ ($1.64\,\mathrm{mm}^2$).

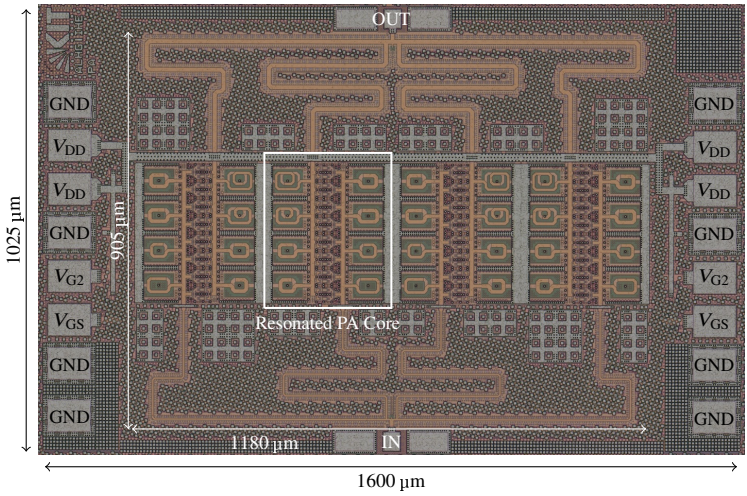
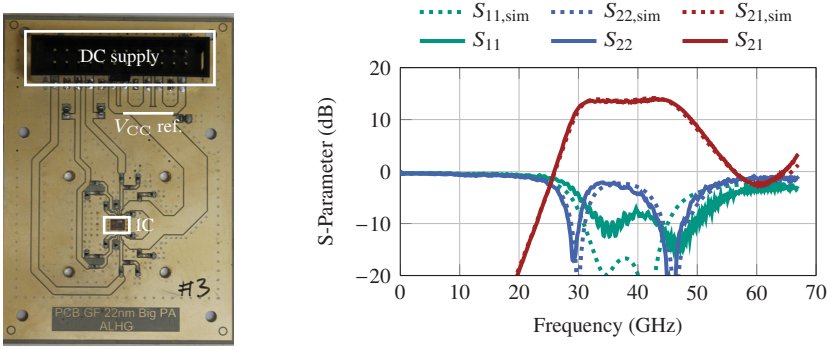


Figure 5.27: Chip microphotograph. Area: $1.64\,\mathrm{mm}^2$. RF core area: $1.07\,\mathrm{mm}^2$. ©IEEE

5.4.2 Characterization

The PA is bonded onto a PCB for DC supply and then directly probed on the RF pads. The PCB assembly is depicted in Fig. 5.28a. The biasing conditions are $V_{\mathrm{G}} = 0.45\,\mathrm{V}$, $V_{\mathrm{G2}} = 1.25\,\mathrm{V}$ and $V_{\mathrm{DD}} = 1.6\,\mathrm{V}$. The PA is biased in class AB operation and draws roughly $550\,\mathrm{mA}$ of supply current in quiescent operation. The small-signal measurement results are shown in Fig. 5.28b and agree well with simulation. A peak small-signal gain of $13.9\,\mathrm{dB}$ is measured. The input match is slightly detuned compared to simulation. A small-signal $3\,\mathrm{dB}$ bandwidth of $19\,\mathrm{GHz}$ ($49\,\%$ relative) is achieved.



(a) (b)

Figure 5.28: PA characterization: a) PCB assembly and b) measured and simulated S-parameters versus frequency.

The single-tone large-signal measurements are carried out using a signal generator as the source and a power meter as the load. The results are presented in Fig. 5.29a over input power at $38\,\mathrm{GHz}$ and in Fig. 5.29b over frequency. At $38\,\mathrm{GHz}$ a saturated output power of $23.9\,\mathrm{dBm}$ and a peak PAE of $20.8\,\%$ is achieved. The saturated output power between 34 to $42\,\mathrm{GHz}$ is larger than $23\,\mathrm{dBm}$ and the corresponding PAE is above $17\,\%$.

Modulated measurements are performed for $200\,\mathrm{MBd}$ and $400\,\mathrm{MBd}$ 64-QAM and $200\,\mathrm{MBd}$ 256-QAM signals. The results are summarized in table 5.2 and constellation diagrams are presented in Fig. 5.30. An average PAE, $\mathrm{PAE}_{\mathrm{avg}}$, of $6.2\,\%$ and average output power, $P_{\mathrm{out,avg}}$, of $14.6\,\mathrm{dBm}$ are measured for a

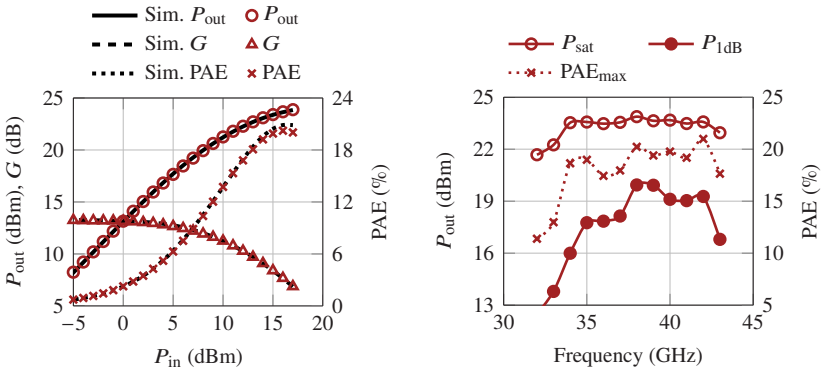
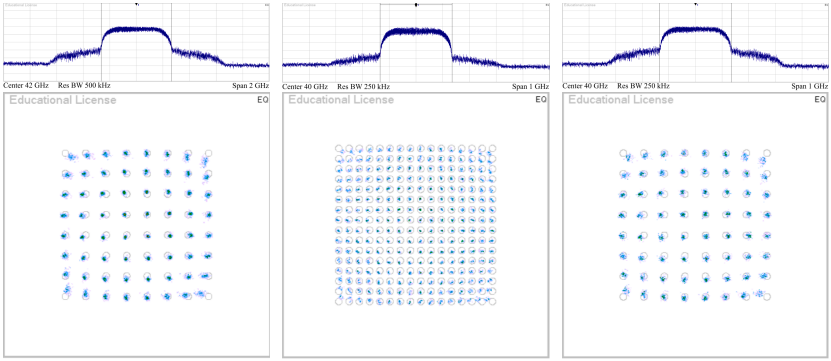


Figure 5.29: Large-signal measurement: a) measured and simulated P_{out}, gain and PAE versus P_{in} at 28 GHz and b) P_{sat} and PAE_{max} versus frequency.

400 MBd 64-QAM signal. For 200 MBd at 40 GHz and with increased bias voltages, $V_G = 0.5$ V, $V_{G2} = 1.3$ V, the average output power could be increased to 16.5 dBm at 5.8 % average PAE. For a 256-QAM 200 MBd signal an average output power of 13.3 dBm with an average PAE of 3.5 % is measured.

Table 5.2: Summary of modulated measurement results.

Modulation	64-QAM	256-QAM	64-QAM
BW (MHz)	400	200	200
Data rate (Gbit/s)	2.4	1.6	1.2
EVM_{RMS} (dB)	−25.2	−25.1	−30.2
$P_{out,avg}$ (dBm)	14.6	13.3	16.5
PAE_{avg} (%)	6.2	3.5	5.8



(a) (b) (c)

Figure 5.30: Modulated measurement results: a) 400 MBd 64-QAM; b) 200 MBd 256-QAM and c) 200 MBd 64-QAM with increased bias voltages.

The PA is compared to other state-of-the-art PAs in table 5.3. Generally, an improvement in output power in the range of 3-4 dB is observed. However, as this is the first iteration in this technology, the prototype shows a reduced PAE compared to selected state of the art and the area consumption is higher. Improvements are possible by a further optimization of the PA core and combiner design. Removing the DC block from the output is expected to add another 0.3 dB of output power.

Table 5.3: Performance comparison with state of the art for the 22 nm FD-SOI PA.

Ref.	**This work**		[ZNL+21]	[MSLL22b]	[PPC+19a]
Tech.	22 nm FD-SOI		22 nm FD-SOI	22 nm FD-SOI	28 nm CMOS
Arch.	Cascode Resonated, 4:1 Wilkinson		2 Stack, Transformer	2 Stack, Transformer	Diff. Cascode, Transformer
f_C (GHz)	38		39	37	38.5
P_{sat} (dBm)	24.4*	23.9	20.4	13.6	16.8
PAE_{max} (%)	18.8*	20.8	25.6	18.5	32.9
OP_{1dB} (dBm)	19.3*	20.2	17.8	9.5	14.9
G_{lin} (dB)	13.7*	13.8	15	15.4	25.8
V_{DD} (V)	1.6	1.6	1.6	1.8	1.8
RFPD ($\frac{mW}{mm^2}$)	257*	234	730 (estimated)	180 (estimated)	600 (estimated)
Area (mm^2)	1.07		0.15 (estimated)	0.31 (full chip)	0.07
Mod.	64-QAM		64-QAM	256-QAM	64-QAM
Data rate	1.2 Gbit/s	2.4 Gbit/s	2.4 Gbit/s	3.2 Gbit/s	8.4 Gbit/s
EVM_{RMS} (dB)	−25.2*	−25.2	−25	-	−25.3
$P_{out,avg}$ (dBm)	16.5*	14.6	13.5	6.2	10.3
PAE_{avg} (%)	5.8*	6.2	10.6	5.3	16.9

* changed bias conditions ($V_{G2} = 1.3\,V$ & $V_{GS} = 0.5\,V$)

5.5 32 dBm K_a-Band Power Amplifier in 130nm SiGe

Parts of the following section contain content previously published in [11].

Following the improvements to the resonated amplifier cores method in the last section, another version of a K_a-band PA in IHP's SG13G2Cu SiGe BiCMOS technology is designed. It achieves a saturated output power of $31.7\,\mathrm{dBm}$ at $28\,\mathrm{GHz}$. The design is similar to the previous section and a second iteration of the PA in section 5.3. The design is improved by further advancing the resonated amplifier core design method. This allows for performance improvements of the core. The overall PA is comprised of four resonated PA cores which are combined in-phase through an efficient 4-to-1 combiner. A schematic of the PA is illustrated in Fig. 5.31.

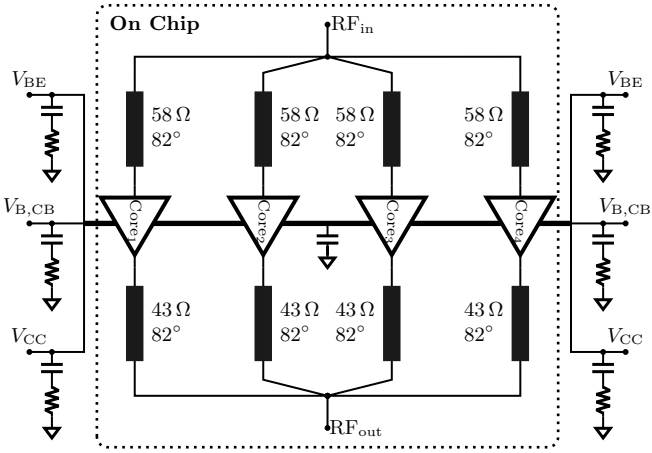


Figure 5.31: $32\,\mathrm{dBm}$ K_a-band PA schematic.

5.5.1 Resonated Amplifier Core Design

In the previous section on the 22 nm FD-SOI PA design a non-uniform inductor design is introduced. However, the needed inductor size grows to values which are challenging to realize at mmWave. Additionally, large inductor values are susceptible to lower quality factors and to make the resonated PA core compact in physical size a lower inductor size is preferred. To reduce the impact of increasing inductor size, the UC segment size throughout the PA core can be optimized as well. In this design, each UCS contains four unit cells, while the last UCS is increased in size, from four ($L_\mathrm{E} = 36\,\mu\mathrm{m}$) to five ($L_\mathrm{E} = 45\,\mu\mathrm{m}$) UCs. In Fig. 5.32 the required input and output inductance of the UC segments in the core are presented with fixed UC segment size ('fixed') and for an adjusted UC segment size at index 4. A reduction of inductor size by 40 % is achieved at the output, allowing for higher quality factors and thus better performance.

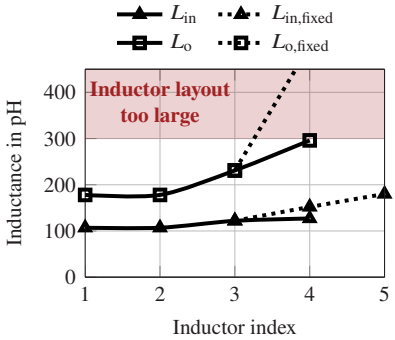


Figure 5.32: Non-uniform resonated core design with varied unit cell segment size for index 4 in 130 nm SiGe BiCMOS (28 GHz).

The updated resonated amplifier core's schematic is presented in Fig. 5.33. The core is comprised of four UC segments. Each UC within the segments contains a cascode topology, with an RC-element at the input for stabilization and bypass capacitors at the common-base device of the cascode. The device size per UC is $L_\mathrm{E} = 9\,\mu\mathrm{m}$. A bias circuit, similar to [WCC+19], is integrated in close proximity to the transistors. This ensures that UCs and bias circuits are thermally coupled.

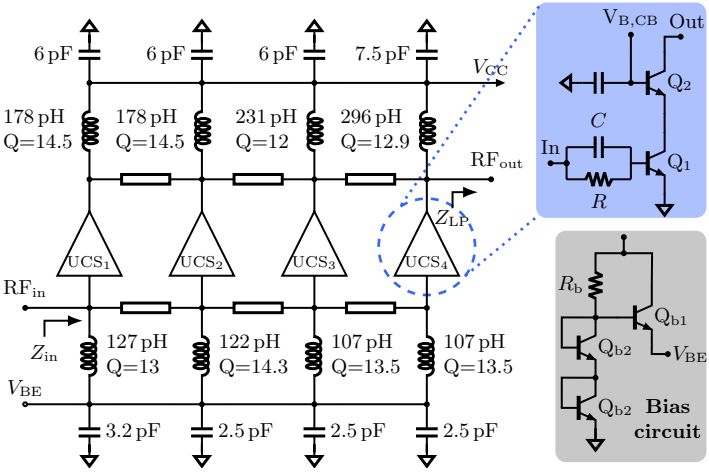


Figure 5.33: Improved resonated amplifier core schematic.

Compared to the previous design in section 5.3, this core leverages an increased UC segment size for segments 1 to 3, by raising the number of UCs from 3 to 4 in each segment. As a result, the required inductance value for resonance is reduced, especially at the output. By further increasing the transistor size at UC segment 4, high inductance values at the output are avoided. Fig. 5.34 presents load-pull data of an updated stand-alone UC segment and a 3D rendered EM model of the new UC segment before and after resonating inductors are applied. A single segment is expected to deliver approximately 21.6 dBm of saturated output power.

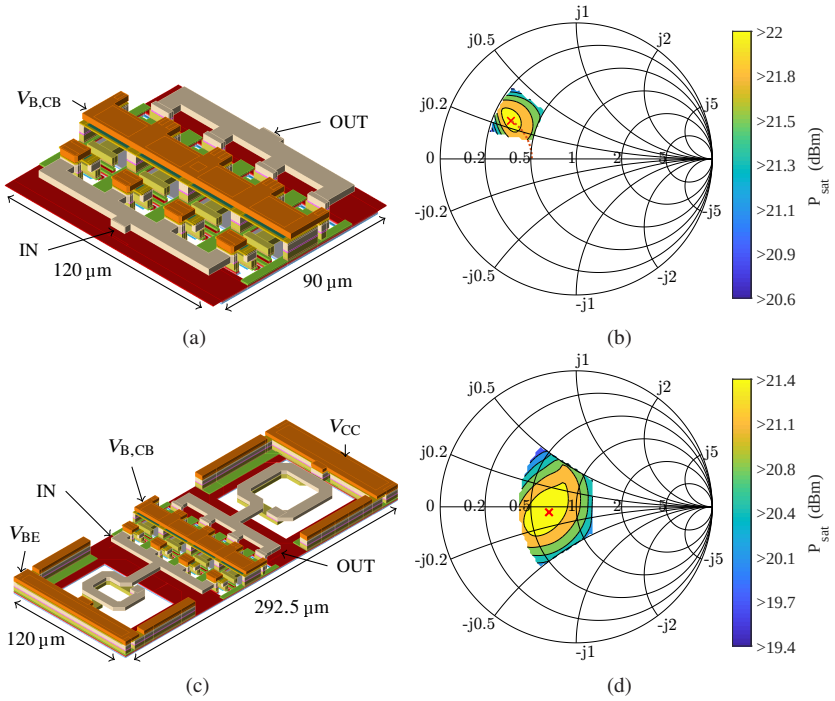


Figure 5.34: UCS design: a) 3D rendered layout UCS; b) load-pull contours for P_{sat} at 28 GHz; c) 3D rendered layout resonated UCS and d) load-pull contours for P_{sat} at 28 GHz (resonated).

The increased physical space and reduced necessary inductance yield higher inductor quality factors of up to 14.5, while including decoupling capacitors. Fig. 5.35 compares the inductor quality factors for this core version with the previous core version from section 5.3.

Due to the improved inductors the new resonated PA core achieves an overall larger core size at a comparable load-pull impedance. After EM simulation, this core outperforms the previous version in terms of output power and PAE, while the supply voltage is reduced to 3.5 V. A 3D rendered model of this core is shown in Fig. 5.36a and Fig. 5.36b summarizes large-signal performance metrics of the core comparison.

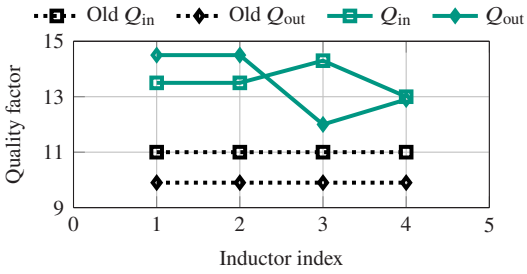
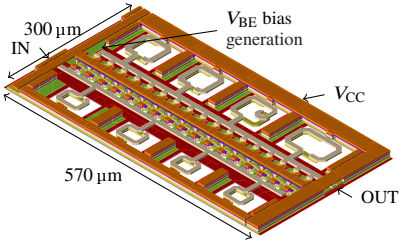


Figure 5.35: Inductor quality factor comparison between new and old core version.



(a)

Version	**New**	Old
P_{sat} (dBm)	26.6	26.4
PAE_{max} (%)	43	35
V_{CC} (V)	3.5	3.9
$Z_{L,opt}$	(9.5 – 5i) Ω	(12 – 3i) Ω
$L_{E,core}$ (µm)	153	108

(b)

Figure 5.36: Resonated amplifier core: a) 3D rendered layout and b) performance comparison with old resonated amplifier core version.

5.5.2 4:1 Power Splitter and Combiner Design

For maximum combining efficiency the input and output splitting and combining networks are implemented in the top Al layer of the technology. While Cu layers offer better conductivity, the Al layer provides a higher line width for the same characteristic impedance and thus provides better RF performance. This has been previously presented in chapter 4.2. Both the input splitter and output combiner are single-stage direct 4-to-1 networks. The 3D rendered layouts are shown in Fig. 5.37a and 5.37b, including size indications. The input splitter also includes two additional supply lines to meet current density limits of the technology during operation. The EM simulated splitter and combiner performance is presented in Fig. 5.37c and 5.37d, respectively. At the input, the minimum insertion loss is 0.8 dB in common mode operation. The bandwidth, for which the match is better than −10 dB is approximately 6.5 GHz. The output combiner

shows a minimum insertion loss of only $0.64\,\mathrm{dB}$ at $28\,\mathrm{GHz}$, while presenting the load-pull impedance of $(9.5 - 5\mathrm{j})\,\Omega$ to the four inputs transformed from a $50\,\Omega$ load. The matched bandwidth is approximately $6\,\mathrm{GHz}$.

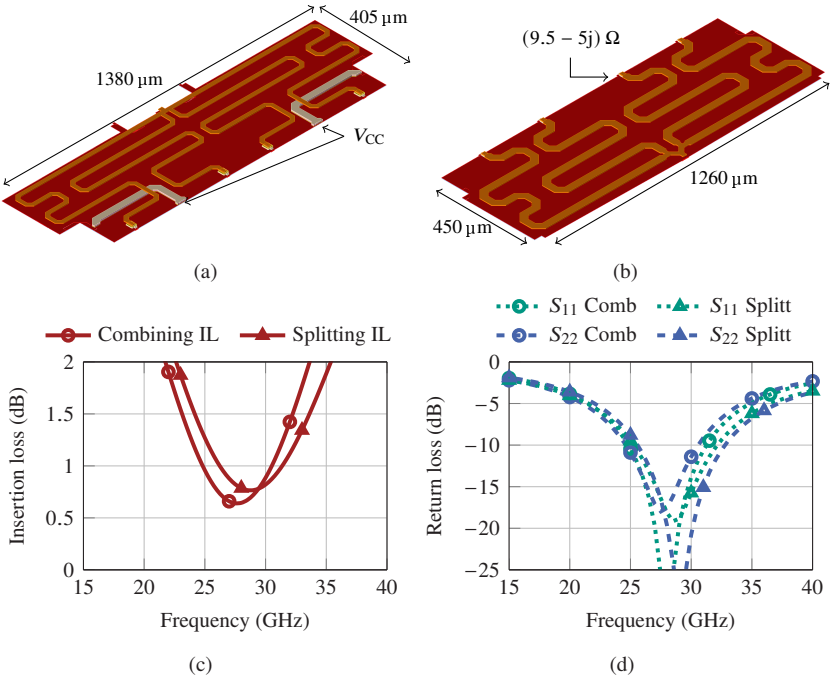


Figure 5.37: Input splitter and output combiner information: a) 3D rendered layout of 1:4 input splitter; b) 3D rendered layout of 4:1 output combiner; c) EM simulated splitter and combiner insertion loss and d) EM simulated splitter and combiner return loss versus frequency.

The phase and amplitude imbalance for the input and output network are shown in Fig. 5.38. The depicted imbalance is taken between the ports with maximum imbalance and is therefore a worst case estimate. For the output, the amplitude imbalance is below $0.2\,\mathrm{dB}$ up to a frequency of $35\,\mathrm{GHz}$, while the phase imbalance is below $1°$. For the input splitter, the imbalances are slightly higher due to the additional V_{CC} supply lines. The phase imbalance is simulated to be below $2.3°$ and the amplitude imbalance below $0.25\,\mathrm{dB}$ up to $35\,\mathrm{GHz}$.

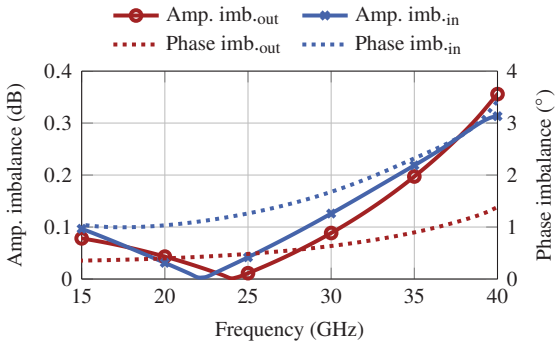


Figure 5.38: Input splitter and output combiner phase and amplitude imbalance versus frequency.

5.5.3 Characterization

A chip microphotograph of the PA is shown in Fig. 5.39. It occupies a total area of $3.25\,\mathrm{mm}^2$.

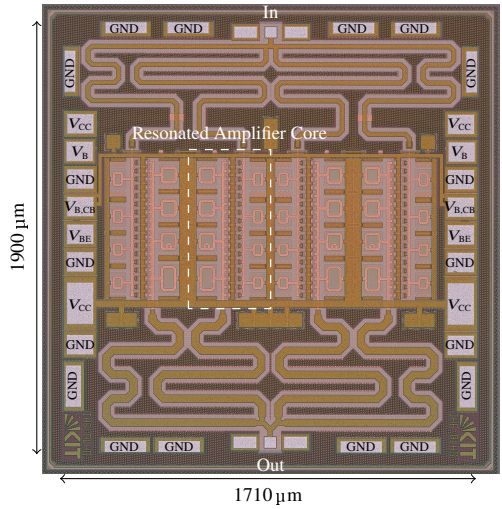
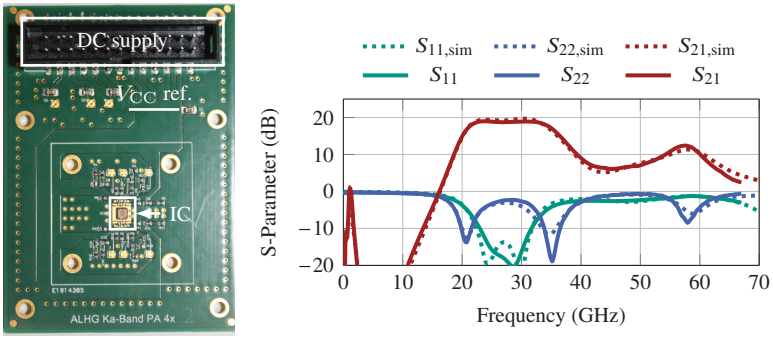


Figure 5.39: Chip microphotograph. Area: $3.25\,\mathrm{mm}^2$. RF core area: $1.99\,\mathrm{mm}^2$.

For the characterization DC is supplied through a dedicated PCB. The PA is placed inside a cutout of the PCB and bonded onto a metal heat sink using an indium patch. The PCB assembly is shown in Fig. 5.40a. The PA is biased using the bias circuit with $V_{\mathrm{BE}} \approx 0.87\,\mathrm{V}$, $V_{\mathrm{B,CB}} = 1.9\,\mathrm{V}$ and $V_{\mathrm{CC}} = 3.5\,\mathrm{V}$. The RF pads are directly probed. Simulated and measured S-parameters versus frequency are provided in Fig. 5.40b. The measurement results agree well with simulation and a maximum small-signal gain of $19\,\mathrm{dB}$ is achieved. The $3\,\mathrm{dB}$ bandwidth is measured to be $15.4\,\mathrm{GHz}$.



(a) (b)

Figure 5.40: PA characterization: a) PCB assembly and b) measured and simulated S-parameters versus frequency.

Large-signal measurements are performed with a signal generator and driver amplifier as the source and an attenuator and power meter as the load. Losses in the measurement setup are deembedded and the results are presented in Fig. 5.41a and 5.41b. At $28\,\mathrm{GHz}$, the PA delivers a saturated output power of $31.7\,\mathrm{dBm}$ with a PAE of $36.8\,\%$. The PA can deliver more than $30\,\mathrm{dBm}$ of power from 25 to $31\,\mathrm{GHz}$.

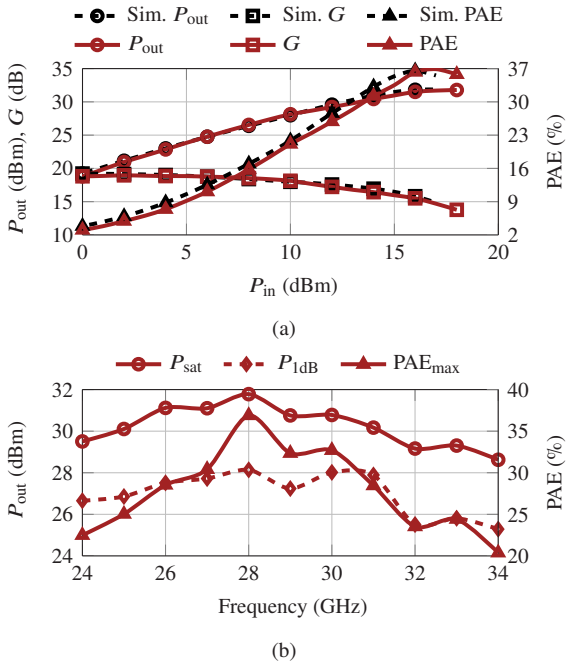
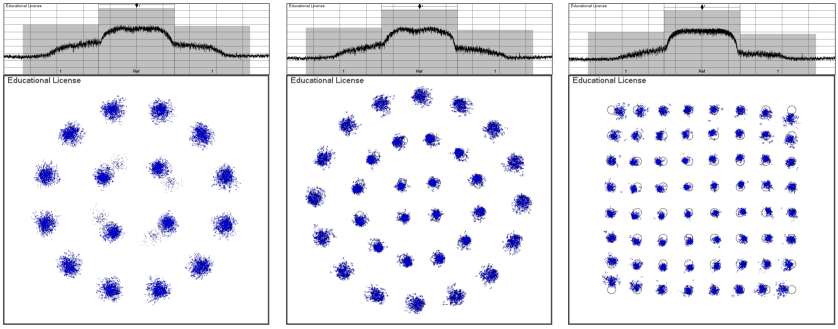


Figure 5.41: Characterization results: a) large-signal parameters versus input power at 28 GHz and b) large-signal parameters versus frequency.

The PA is tested by a 16-APSK, 32-APSK, 64-QAM and 256-QAM signal with symbol rates between 100 MBd and 400 MBd. A loss calibration of the measurement setup is performed up to the end of the measurement cables. Probe loss is calibrated out by using data sheet values. A roll-off factor, α, of 0.35 is used and equalization is enabled. The results are summarized in table 5.4 and a set of constellation diagrams are provided in Fig. 5.42. For the 64-QAM signal, the PA achieved a high modulated output power of 24.7-25.1 dBm with a PAE of 10.6-12.2 %.

Table 5.4: Summary of modulated measurement results.

Mod.	BW (MHz)	$\mathrm{EVM_{RMS}}$ (dB)	ACPR (dB)	$P_{\mathrm{out,avg}}$ (dBm)	$\mathrm{PAE_{avg}}$ (%)
16-APSK	100	−21.4	−21.9	28	19.9
16-APSK	400	−21.2	−22.7	27.8	18.7
32-APSK	100	−21.1	−23.5	27.1	14.3
32-APSK	400	−22.8	−25.3	26	18
64-QAM	100	−25.3	−29.1	25.1	12.2
64-QAM	400	−25.4	−29.9	24.7	10.6
256-QAM	100	−30.1	−32.2	22.8	7.2
256-QAM	200	−30.1	−33.1	21.2	5.2



(a) (b) (c)

Figure 5.42: Modulated measurement results: a) 400 MSym/s 16-APSK; b) 400 MSym/s 32-APSK and c) 400 MSym/s 64-QAM.

5.6 36.7 dBm K_a-Band Power Amplifier in 130nm SiGe

Parts of the following section contain content previously published in [11].

In this section a K_a-band PA in IHP's SG13G2Cu technology is presented. This design expands on the PA design of the previous section. It achieves a saturated output power of $36.7\,\mathrm{dBm}$ at $28\,\mathrm{GHz}$. The same PA core as presented in detail in section 5.5.1 Fig. 5.33 is used. A schematic of the expanded PA is shown in Fig. 5.43. It consists of 16 PA cores, which are combined in a two-stage combiner. First, 4 PA cores are combined into one output. Then two of these outputs are shorted together with a short TL, followed by a 2-to-1 combiner.

5.6.1 16:1 Power Splitter and Combiner Design

For the splitting and combining the results presented in chapter 4.2 are applied. The 1-to-16 power splitter is a two-stage splitter design. Stage I facilitates a 1-to-4 splitting ratio by utilizing a 1-to-2 splitter, with each of its outputs being connected to two second stage splitters. The stage I splitter is divided into two TL segments, one in the top Al layer, with a characteristic impedance of $50\,\Omega$ and electrical length of $40°$, followed by a TL in the thick Cu layer, with a characteristic impedance of $25\,\Omega$ and electrical length of $40°$. This increases the total physical length of the stage I splitter compared to a single TL segment of constant characteristic impedance. The physical length would otherwise be too short to contact the following stage. Stage I matches a $50\,\Omega$ source to 4 loads with an impedance of $(22+22\mathrm{j})\,\Omega$. This is the intermediate impedance between stage I and II, seen from stage I. When observed from stage II a source impedance of $(22-22\mathrm{j})\,\Omega$ is presented. Stage 2 is a 1-to-4 power splitter integrated in the top Al layer. It matches a $(22-22\mathrm{j})\,\Omega$ source to 4 $(16.7+3.9\mathrm{j})\,\Omega$ loads. The splitter includes a DC block. To achieve sufficient on-chip current carrying capability 10 supply pads are distributed along the chip edge, of which 8 are distributed along the input splitter. The metal contacts for each supply pad can carry up to $650\,\mathrm{mA}$. A total current of $6.5\,\mathrm{A}$ can be delivered to the active devices. A shielded bias distribution network is integrated below the ground plane of the splitter. A 3D rendered layout of the described input splitter is shown in Fig. 5.44a.

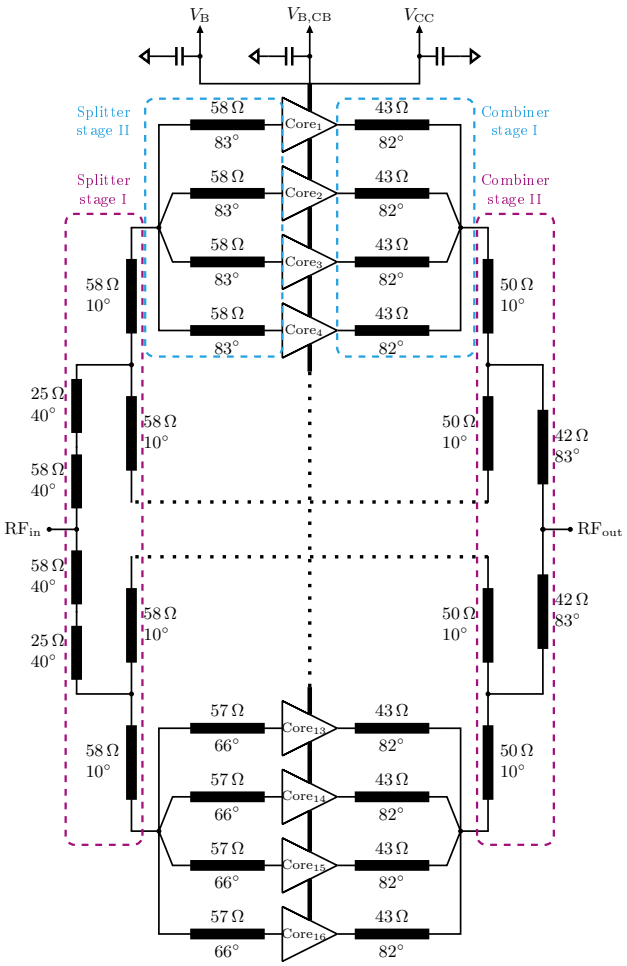


Figure 5.43: 4.7 W K_a-band PA schematic.

Combiner stage I is a 4-to-1 combiner, directly connected to the PA cores. It combines the output of four cores and transforms an intermediate load impedance of $(33 + 3\mathrm{j})\,\Omega$ to the load-pull impedance, $(9.5 - 5\mathrm{j})\,\Omega$, of the PA cores. In contrast to the previous 31.7 dBm PA, this combiner is not integrated in

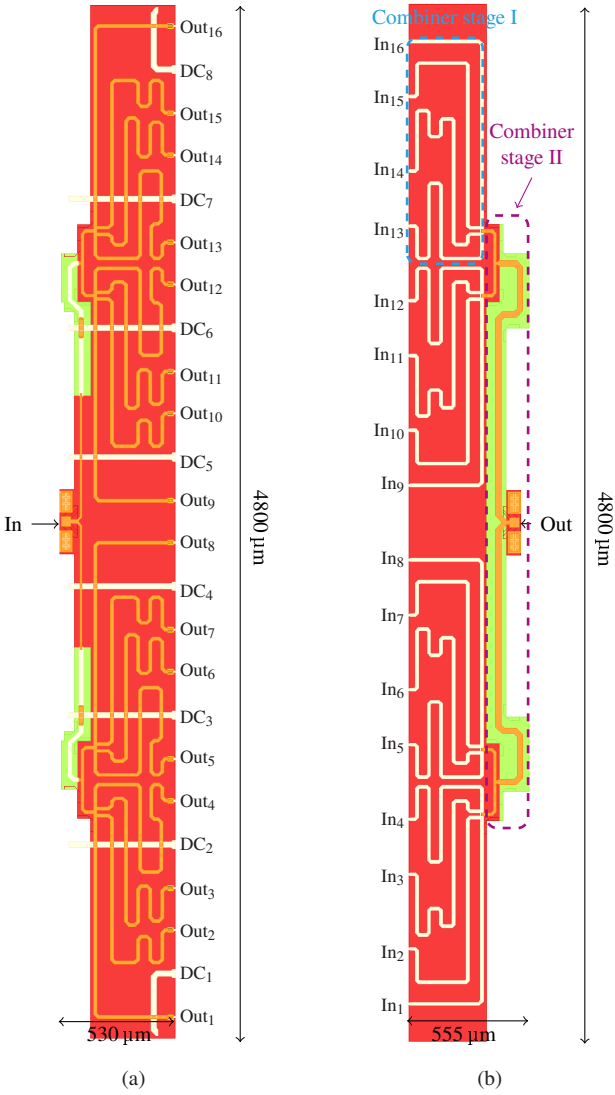


Figure 5.44: 3D rendered layouts of: a) 1:16 input splitter and b) 16:1 output combiner.

the top Al layer, but in the thick Cu layers. As the thick Cu layer requires a smaller line width for the same characteristic impedance this allows for a more compact design of stage I, thus simplifying the design of stage II. The second stage facilitates a 4-to-1 combination through a 2-to-1 structure, for which each input is connected to the output of two combiners of stage I. A dedicated 4-to-1 structure in stage II is not feasible due to layout size constraints. A 3D rendered layout of the full combiner is depicted in Fig. 5.44b.

The splitter and combiner are EM simulated in sections. Simulated S-parameters of the EM simulated input splitter and output combiner stages as individual blocks are presented in Fig. 5.45a and 5.45b for the splitter stages and in Fig. 5.45c and 5.45d for the combiner stages. The splitting stages are well matched at the center frequency and incur a splitting loss of 0.54 and $0.73\,\mathrm{dB}$, respectively. Both combiner stages are matched better than $-20\,\mathrm{dB}$ at the design frequency and the combining loss for stage I and II at $28\,\mathrm{GHz}$ is 0.75 and $0.55\,\mathrm{dB}$, respectively.

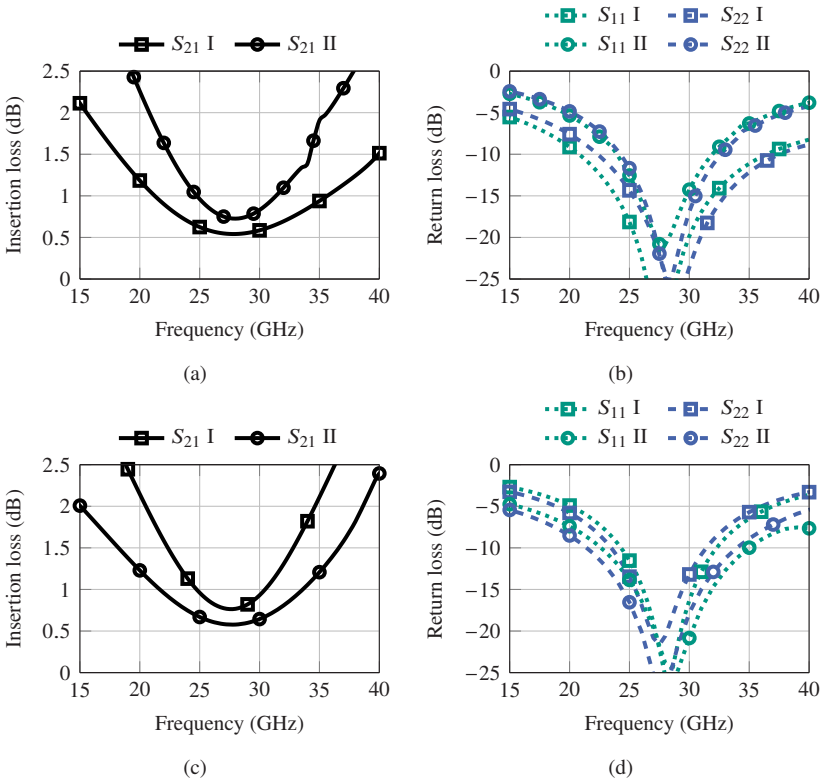


Figure 5.45: Splitter and combiner insertion and return loss versus frequency after EM simulation: a) splitter insertion loss; b) splitter return loss; c) combiner insertion loss and d) combiner return loss.

The resulting S-parameters, when the splitter and combiner stages are simulated as a whole are provided in Fig. 5.46a and 5.46b. At 28 GHz, a splitting and combining loss of 1.35 dB is expected. The 3 dB bandwidth at input and output is 33 GHz and 18.5 GHz, respectively. The maximum amplitude and phase imbalance between any port of the splitter and combiner are shown in Fig. 5.46c. The input splitter shows a significant amplitude imbalance of 0.6 dB at 28 GHz, mostly caused by the additional supply lines interacting with the

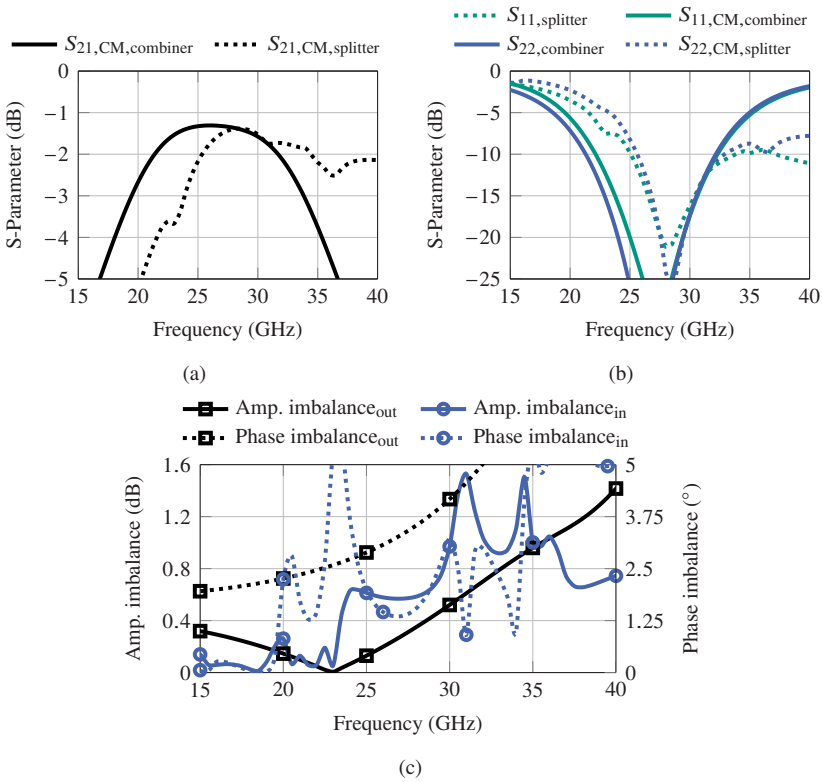


Figure 5.46: Splitter and combiner S-parameters versus frequency after EM simulation: a) common-mode S_{21}; b) return loss; c) amplitude and phase imbalance.

RF structures asymmetrically. In the frequency range of interest, the maximum phase imbalance is smaller than $5°$ for both the splitter and combiner .

Finally, Fig. 5.47 shows a chip microphotograph of the whole PA. Including pads the PA occupies an area of $8.83\,\mathrm{mm}^2$. Excluding pads the PA occupies $7.78\,\mathrm{mm}^2$.

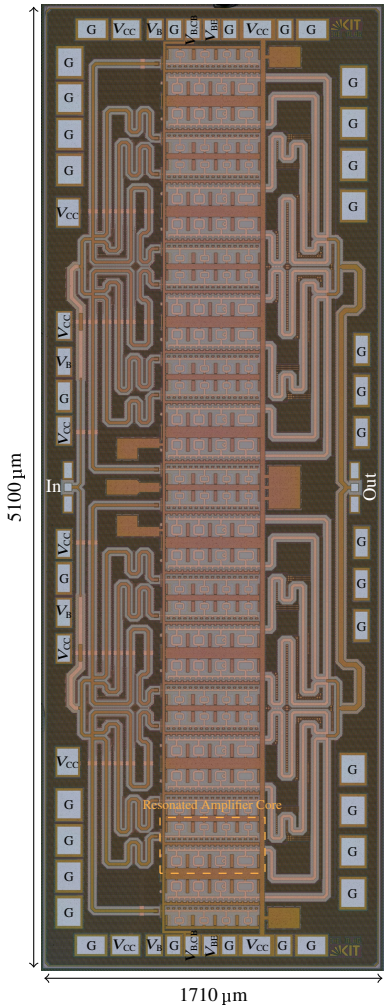


Figure 5.47: Chip microphotograph. Area: $8.83\,\mathrm{mm}^2$. RF core area: $7.78\,\mathrm{mm}^2$.

5.6.2 Characterization

For the characterization a custom DC supply PCB and a heatsink are designed and manufactured. An illustration of the entire assembly during measurement is presented in Fig. 5.48. As the PA sinks a current of up to $5\,\mathrm{A}$ from a $3.5\,\mathrm{V}$ supply, DC calibration is needed for accurate measurement results. The DC reference plane during the measurement is marked in the figure. The IC is directly bonded onto the metal heatsink for sufficient thermal connection to ambient. To attach the chip an indium layer is used.

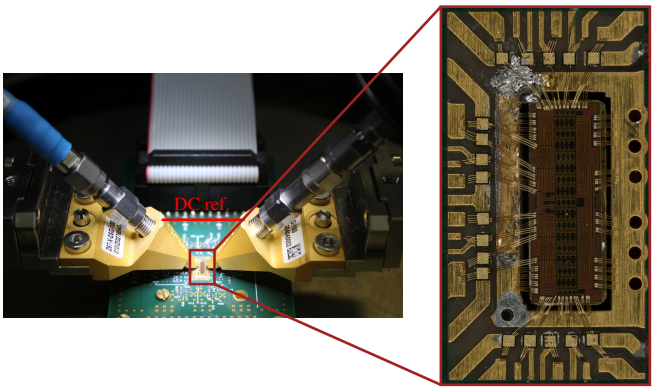


Figure 5.48: Measurement assembly.

Due to the size of the PA the small-signal measurement setup includes significant attenuation both in the input and output path. Calibration is thus only accurate up to $40\,\mathrm{GHz}$ and ripples are visible for the S_{22} data. The RF input and output are directly probed using FormFactor's |Z|-Probe, which can withstand more than $5\,\mathrm{W}$ of RF power at $28\,\mathrm{GHz}$. A coaxial DC block is directly connected to the probe contacting the output pad. The simulation and measurement results are presented in Fig. 5.49 showing decent agreement. A small-signal gain of $17.5\,\mathrm{dB}$ is measured and a $3\,\mathrm{dB}$ bandwidth from 22.5 to $34.5\,\mathrm{GHz}$, corresponding to a relative bandwidth of $42\,\%$, is achieved. The input is well matched and the relative bandwidth for which the PA is matched better than $-10\,\mathrm{dB}$ is measured to be $25\,\%$.

For the single-tone large-signal measurements, a signal generator followed by a driver amplifier is used as the signal source. A power meter following a $2.92\,\mathrm{mm}$

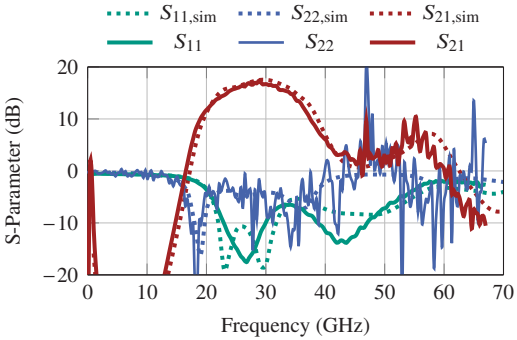


Figure 5.49: Measured and simulated S-parameters versus frequency.

coaxial attenuator is used as the load. Harmonics are filtered due to the attenuator's cutoff frequencies of 40 GHz. Single-tone large-signal simulation and measurement results at 27 GHz are presented versus input power in Fig. 5.50a. A saturated output power, P_{sat}, of 36.7 dBm is measured, while a PAE of 28 % is achieved. Single tone large-signal measurement results versus frequency are included in Fig. 5.50b. The PA can output more than 35 dBm from 25.5 to 29 GHz. Compared to the single frequency measurement at 27 GHz, however, the peak values at 27 GHz are 0.7 dB worse in this measurement. This is attributed to the limited cooling provided to the PA during the longer measurement sweep in Fig. 5.50b. The ambient temperature changes considerably, as the probe station's chuck is heated by the PA during the duration of the entire sweep.

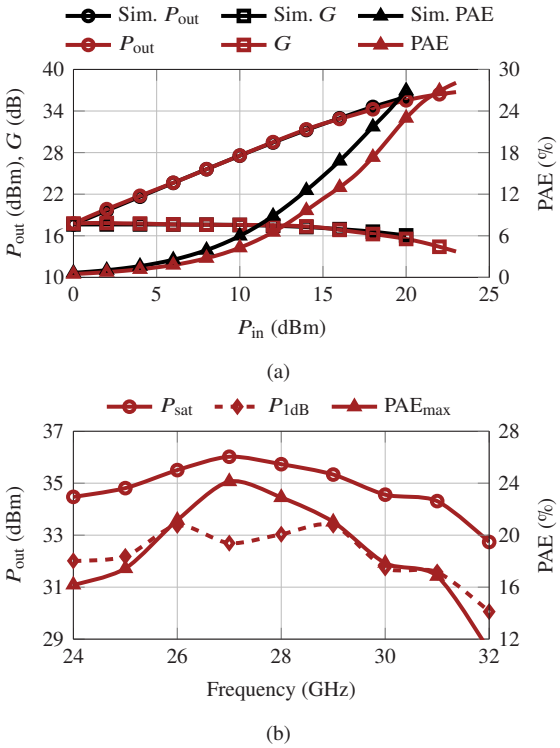
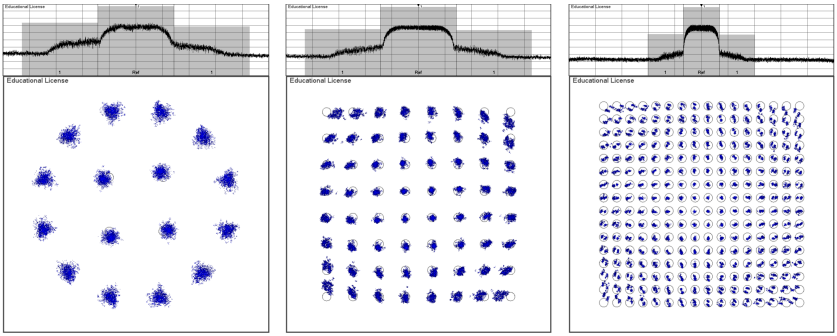


Figure 5.50: Measured and simulated single-tone large-signal parameters: a) large-signal parameters versus input power at 27 GHz and b) large-signal parameters versus frequency.

Finally, the PA is characterized with modulated signals. The base band signals are generated by an arbitrary waveform generator (AWG), which is followed by a vector signal generator for amplification and frequency mixing. The measurement setup is illustrated in the appendix in Fig. A.1c. A driver amplifier is used, to prevent operating the signal generator at high amplitude settings, which add non-linearity. The investigated signals are $400\,\mathrm{MBd}$ 16-APSK, $400\,\mathrm{MBd}$ 64-QAM and $200\,\mathrm{MBd}$ 256-QAM. A roll-off factor, α, of 0.35 is used. A summary of the measurement results is provided in table 5.5 and constellation diagrams are presented in Fig. 5.51. The PA delivers record breaking levels of average signal output power, $P_{\mathrm{out,avg}}$, in the range of 29-32.4 dBm, while maintaining an average efficiency, $\mathrm{PAE_{avg}}$, of 7.1-12.5 %.

Table 5.5: Summary of modulated measurement results.

Modulation	16-APSK	64-QAM	256-QAM
BW (MHz)	400	400	200
Data rate (Gbit/s)	1.6	2.4	1.6
$\mathrm{EVM_{RMS}}$ (dB)	-22.6	-25.1	-30.2
ACPR (dB)	-22.7	-30.7	-37.5
$P_{\mathrm{out,avg}}$ (dBm)	32.4	29.2	26.1
$\mathrm{PAE_{avg}}$ (%)	12.5	7.1	3.6



(a) (b) (c)

Figure 5.51: Measurement results for modulated signals: a) 400 MSym/s 16-APSK; b) 400 MSym/s 64-QAM and c) 200 MSym/s 256-QAM.

5.7 Conclusion

This chapter presents the investigation of internal parasitics of PA cores and their influence on the PA. The internal parasitics are degrading PA core performance once the impedances, either at source or load side, become low. Within this work, when the input or load-pull impedance dropped below 5-7 Ω, performance degradation increased beyond 1 dB at 28 GHz compared to an ideal schematic core of the same size. However, to increase achievable output power on a single IC, using PA cores with large parallelization is necessary to overcome both the limited number of PA cores that can be combined in a single chip efficiently and the low supply voltages mandated by modern Si technologies. To extend the size of cores, without high performance degradation, the resonated amplifier cores method is introduced and achieves superior PA core performance. Four prototype PAs, each with high output power in their respective technologies, are fabricated. Each successive prototype enhances the employed method, with the final two prototypes showing record breaking performances both in terms of output power and PAE. To illustrate this, table 5.7 lists key performance parameters of the presented and other published PAs. By adopting the presented core design method SiGe is reaching power levels previously only achieved by GaN-based designs. In silicon, the improvement is in the range of 6 to 10 dB.

Increasing the output power beyond 36.7 dBm without significant reduction of PAE is limited by the physical length of a third combining stage. For the resonated PA cores used in the 36.7 dBm design, the necessary TL length to combine 2x16 PA cores is in the range of half a wavelength at 28 GHz. This results in extra line loss added to the combining loss, as the combiner only requires a line length of roughly $\lambda/4$ for its transformation. This could only be overcome by placing the PA output pad at the chip center, complicating access to the RF output.

Table 5.6: Performance comparison of high power PAs with state of the art.

Ref.	f_C (GHz)	P_{sat} (dBm)	PAE_{max} (%)	G_{lin} (dB)	V_{CC} (V)	RF PD (W/mm^2)
Sec. 5.3[+]	28	30.8	25.5	18	3.9	1.06
Sec. 5.5[+]	28	31.7	37	19	3.5	0.8
Sec. 5.6[+]	27	36.7	28	17.8	3.5	0.6
[CKA+23][+]	18	30	23.5	21.4	4.2	0.89
[WW20a][+]	28	28.3	30.4	20.5	2	0.5
[RQG+22][++]	28	30.8[‡]	26.7[‡]	13.9	5.5	0.49*
[ELM14][++]	27	29.7	10.5	24.5	5.5	0.47*
[WNP16][+++]	24	30.8	17.6	16.1	5.8	0.41*
[HW19][†]	28	26	34	16.3	2.4	1.38*
[NJW19][††]	60	30.1	20.8	24.7	2.2	0.155
[NP16][Φ]	27	31.5	33	17	12	0.7
[WYL18][Φ]	28	31	27.3	21.3	4	0.32*
[PPC+19b][$]	30	40	28	16	17.5	0.6*
[CZL+22][$]	28	34	31.5	30	20	0.23*
[NJT+21][$$]	30	38.2	26.1	20	15	0.49*

[+] 0.13 µm SiGe [++] 0.25 µm SiGe [+++] 0.35 µm SiGe
[†] 90 nm CMOS [††] 45 nm CMOS SOI [Φ] 0.15 µm GaAs
[$] 0.15 µm GaN HEMT [$$] 0.1 µm GaN HEMT [‡] off-chip combined
* Estimated from figures

Table 5.7: Modulated performance comparison of high power PAs with state of the art.

Ref.	Modulation	Data rate (Gbit/s)	$\mathrm{EVM_{RMS}}$ (dB)	P_{out} (dBm)	PAE (%)
Sec. 5.3^{+}	64-QAM	1.2	−25.2	22.8	7.1
Sec. 5.5^{+}	64-QAM	2.4	−25	24.7	10.6
Sec. 5.6^{+}	64-QAM	2.4	−25.1	29.2	7.1
[CKA^{+}23]$^{+}$	-	-	-	-	-
[WW20a]$^{+}$	64-QAM	1.2	−25	20.9	18.4
[RQG^{+}22]$^{++}$	64-QAM	2.4	−25.8	23.7‡	11.3‡
[ELM14]$^{++}$	-	-	-	-	-
[WNP16]$^{+++}$	-	-	-	-	-
[HW19]†	64-QAM	2.46	−25	19.8	-
[NJW19]††	64-QAM	8	−27.1	20.9	4.3
[NP16]$^{\Phi}$	-	-	-	-	-
[WYL18]$^{\Phi}$	-	-	-	-	-
[PPC^{+}19b]$^{\$}$	-	-	-	-	-
[CZL^{+}22]$^{\$}$	LTE	5x100 MHz	-	28	10.5
[NJT^{+}21]$^{\$\$}$	-	-	-	-	-

$^{+}$ 0.13 µm SiGe $^{++}$ 0.25 µm SiGe $^{+++}$ 0.35 µm SiGe
† 90 nm CMOS †† 45 nm CMOS SOI $^{\Phi}$ 0.15 µm GaAs
$^{\$}$ 0.15 µm GaN HEMT $^{\$\$}$ 0.1 µm GaN HEMT ‡ off-chip combined
* Estimated from figures

6 Linear Power Amplifier Design Using Two-Tone Load-pull

Parts of the following chapter contain content previously published in [12].

In previous chapters design methods are presented that are applied to improve peak performance metrics such as the saturated output power or PAE. However, especially for communication, a PA is not used at its peak performance values. Instead, the PA must be operated with a certain back-off from saturation, depending on the desired modulation scheme. Modern and more complex modulation techniques, like 64-QAM OFDM, show extensive PAPR. If the PA is operated too close to saturation for this case, the bit error rate increases significantly as the modulation symbols with high amplitude are distorted. However, at back-off PAs exhibit reduced efficiency and output power. Simulatively predicting the required back-off and resulting performance in terms of average output power and PAE for a modulated signal is challenging and to the best of the author's knowledge no straight forward design method exists for optimization. In published literature, extensive research is performed on circuit topologies such as the Doherty power amplifier (DPA) and linearization techniques, but the design methods, e.g., which impedances to match and how to determine them, remain the same.

Table 6.1: Q-band MPA specifications for future space applications.

f (GHz)	P_{out} (dBm)	PAE (%)	Gain (dB)	$S_{11}\&S_{22}$ (dB)	IMD3 (dBc)	Temp. (°C)	Supply (V)
37-43	≈20	≈20	20	< -15	<−25	−25-85	3.3

As an example, in table 6.1 basic specifications for a MPA for future space applications at Q-band as part of a transmitter (TX) chain are presented. The specifications are provided as part of a research project. The MPA can either be

used for a single channel in an antenna array or as a driver for a GaN or vacuum tube HPA. The presented specifications for the MPA are not requirements at saturation, but performance required while meeting a linearity criterion. For this project, the linearity is specified by IMD3. IMD3 describes the difference in amplitude of the fundamental tones to the third order intermodulation products (IM3s) under two-tone excitation and is illustrated in Fig. 6.1. For two tones with frequencies f_1 and f_2, a PA produces intermodulation products at different frequencies, due to its non-linearity. Second order intermodulation products at the frequencies $f_2 - f_1$, $2f_1$, $f_1 + f_2$ and $2f_2$ are far from the fundamental tones and can thus be filtered. However, third order intermodulation products at the frequencies $2f_1 - f_2$ and $2f_2 - f_1$ are very close to the fundamental tones and cannot be filtered and thus have a significant impact on the signal quality. Other intermodulation products at higher frequencies or of higher order are not shown.

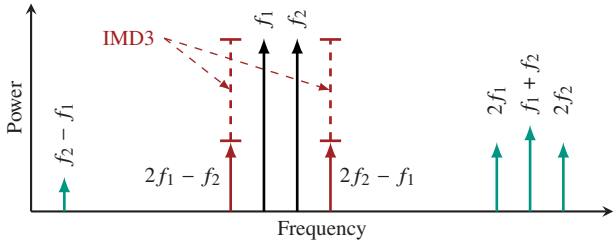


Figure 6.1: Simplified PA output spectrum during two-tone excitation of f_1 and f_2.

Additionally, a small-signal return loss requirement for the output is specified, which is typically not fulfilled for a large-signal match. This necessitates extra attention for the design. This chapter presents a design approach to optimize a PA for a given IMD3 requirement and a Q-band MPA design utilizing this method.

6.1 Two-Tone Load-pull

In classical PA design either load-line or load-pull is used to find the impedance to be presented to the PA's output. The optimization target could be highest saturated output power, highest peak PAE or highest output power at a certain gain compression, typically $1\,\mathrm{dB}$. Each requirement may result in a different optimal impedance. To illustrate this, Fig. 6.2 shows the load-pull contours of a 10 finger cascode PA core for peak PAE and P_{sat} at $40\,\mathrm{GHz}$. For P_{sat} an optimal load-pull impedance of $Z_{\mathrm{LP,sat}} = (69 + 45\mathrm{j})\,\Omega$ is found. For highest PAE the optimal load-pull impedance is $(87 + 105\mathrm{j})\,\Omega$. In both cases the gain compression of the PA was limited to at most $4\,\mathrm{dB}$ during load-pull. A trade-off between both impedances can be used to achieve a desired performance in compression.

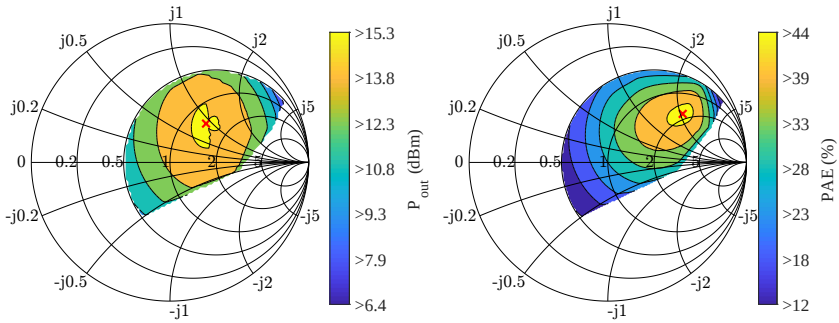


Figure 6.2: Load-pull contours at $40\,\mathrm{GHz}$ for a) P_{sat} and b) PAE. ©IEEE

This method, however, allows for no insight into performance at back-off or for certain linearity requirements at back-off. To accommodate for this, this work proposes to use load-pull with two-tone stimulus at the input. Two-tone load-pull can be used to find the impedance yielding the highest output power or PAE for a certain linearity requirement, e.g., at a fixed IMD3. As an example, for the same PA core, as in Fig. 6.2, the two-tone load-pull contours for P_{out} and PAE at IMD3 = $-25\,\mathrm{dBc}$ are shown in Fig. 6.3a and 6.3b. The stimulus is centered around $40\,\mathrm{GHz}$ with a frequency spacing, Δf, of $100\,\mathrm{MHz}$ between the two tones. The optimal impedances are $(55 + 31\mathrm{j})\,\Omega$ and $(71 + 51\mathrm{j})\,\Omega$ for optimal two-tone P_{out} and PAE, respectively. These impedances are closer

to the single-tone load-pull impedance for maximum saturated output power than to the impedance for peak PAE. A maximum two-tone PAE of $24.3\,\%$ is observed. If the single-tone load-pull impedance for peak PAE is used a two-tone PAE of $20\,\%$ is achieved. In relative terms this corresponds to a $20\,\%$ improvement in PAE by two-tone load-pull.

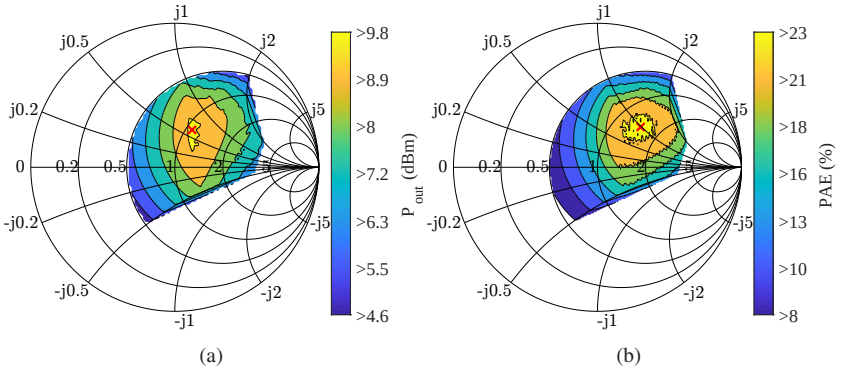


Figure 6.3: Two-tone load-pull contours for IMD3 = $-25\,\mathrm{dBc}$ and $f_1 = 39.95\,\mathrm{GHz}$ and $f_2 = 40.05\,\mathrm{GHz}$: a) optimal two-tone P_{out} and b) optimal two-tone PAE. ©IEEE

A comparison of single-tone and two-tone performance versus input power is presented in Fig. 6.4. The index '1TLP' describes simulation results for the single-tone load-pull impedance for peak PAE and '2TLP' describes results for the two-tone load-pull impedance for PAE. In Fig. 6.4a single-tone large-signal simulation results are presented. Most noticeable are the differences in gain, G, and peak PAE. In Fig. 6.4b IMD3 versus two-tone input power (describing the summed power of both input tones) is depicted, including an indication for which input power the IMD3 limit of $-25\,\mathrm{dBc}$ is reached. This happens at a $6\,\mathrm{dB}$ higher input power level for the two-tone load-pull impedance. When the two-tone large-signal performance versus input power, shown in Fig. 6.4c, is read for this input power the two-tone load-pull impedance achieves a better performance.

Following this insight, the single-tone load-pull impedance for saturated output power appears to be the more linear option. However, this changes as the linearity criterion is changed. To illustrate this the optimal two-tone load-pull impedances for varying IMD3 requirements are presented in Fig. 6.5. Arrows in

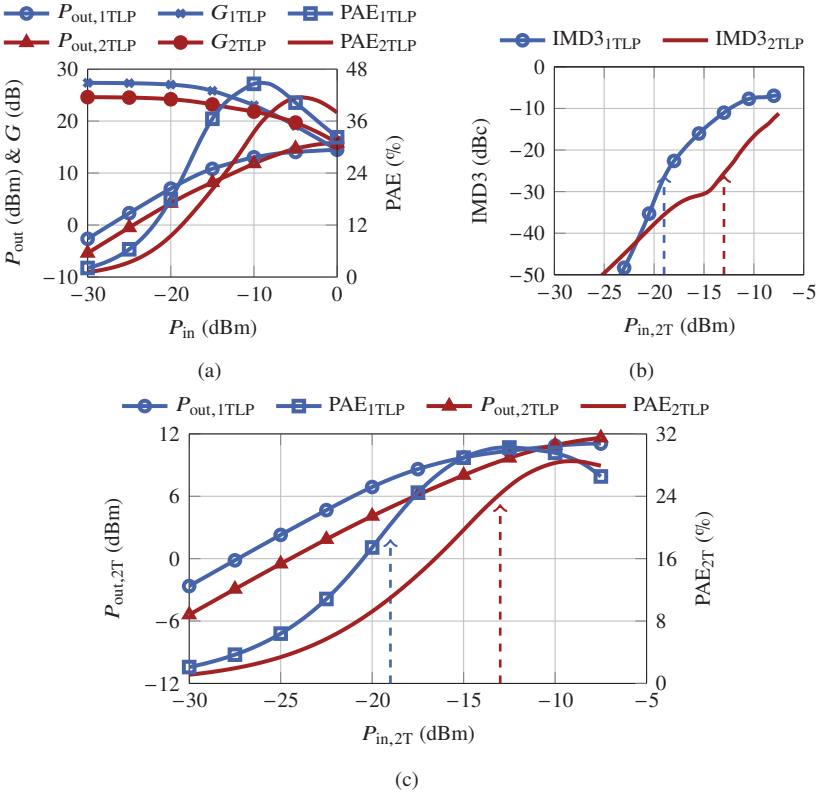


Figure 6.4: Large-signal simulation results versus input power for different loading conditions: a) single-tone P_{out} and PAE at 40 GHz, b) two-tone IMD3 and c) two-tone P_{out} and PAE.

the magnified plot indicate the direction of decreasing IMD3 (stricter linearity requirement). For IMD3 at $-20\,\text{dBc}$ the two-tone load-pull impedances tend towards their single-tone counterpart. This could be explained by the PA being able to operate closer to saturation for a low linearity requirement. For IMD3 between $-22.5\,\text{dBc}$ and $-30\,\text{dBc}$ the two-tone load-pull impedance for PAE tends towards the single-tone load-pull impedance for P_{sat}. This could indicate that at this impedance linearity deteriorates slower and therefore achieves the best results. For IMD3 below $-30\,\text{dBc}$ the optimal two-tone impedances move

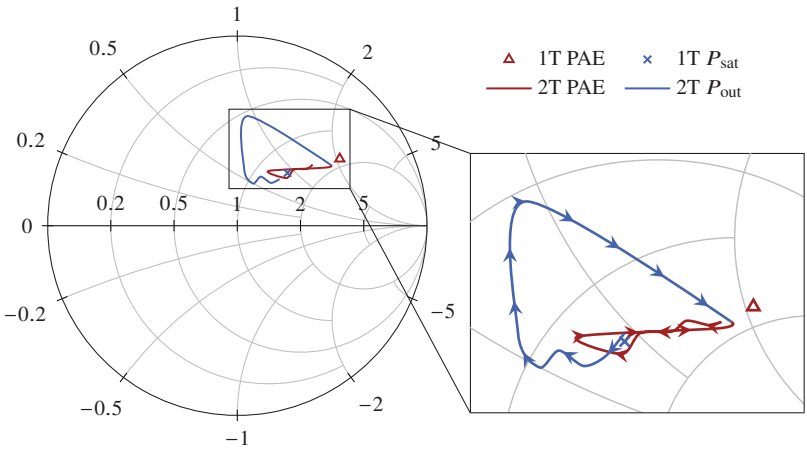


Figure 6.5: Optimal load-pull impedances for single-tone stimulus and two-tone stimulus for different IMD3 ($-17.5\,\mathrm{dBc} \geq \mathrm{IMD3} \geq -35\,\mathrm{dBc}$) limits. ©IEEE

towards the single-tone load-pull impedance for PAE, for which a high gain and thus the highest performance in deep back-off is achieved. This effect is also visible in Fig. 6.6a showing two-tone PAE versus IMD3 for optimal two-tone load-pull impedances (for each IMD3 point a load-pull simulation is performed) and for the single-tone load-pull impedance. For IMD3 between $-15\,\mathrm{dBc}$ and $-32.5\,\mathrm{dBc}$ an improvement is possible by two-tone load-pull, but towards the lower and upper end the single-tone impedance delivers similar performance.

Additionally, by performing two-tone load-pull for different biasing options, optimal bias conditions can be selected. In Fig. 6.6b the two-tone PAE and output power at an IMD3 of $-25\,\mathrm{dBc}$ under ideal voltage (vb) or current (ib) bias are presented. For the current bias, V_{BE} values correspond to small-signal operation. In this case, compared to voltage biasing, a current biased core could achieve $0.8\,\mathrm{dB}$ more power, for the same PAE of $24.7\,\%$.

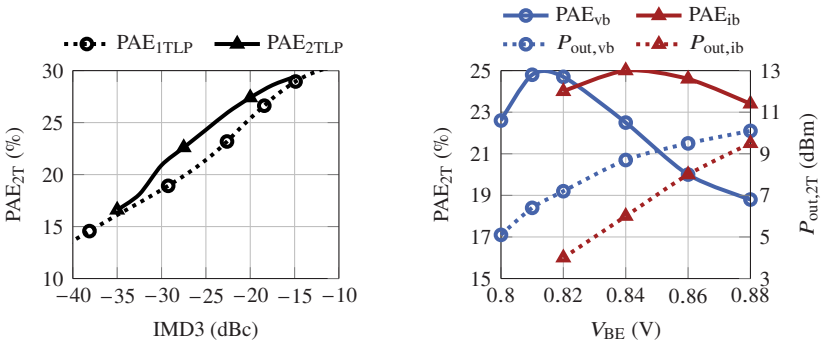


Figure 6.6: Two-tone optimization: a) PAE versus IMD3 for different loading conditions and b) PAE and P_{out} for different bias conditions.

6.2 Linear Q-Band Power Amplifier in 130nm SiGe

The MPA presented in the following is designed in IHP's SG13G3Cu technology. The MPA is designed at a center frequency of $40\,\mathrm{GHz}$ and for a linear output power of $20\,\mathrm{dBm}$.

The schematic of the developed MPA is presented in Fig. 6.7. A balanced amplifier topology is adopted to ensure decent small-signal return loss at the output. $3\,\mathrm{dB}$ hybrid couplers are placed at the input and output to achieve balanced operation, and their isolated ports are terminated with $50\,\Omega$. At each branch of the couplers two PA cores are combined and driven differentially through transformers. The transformers are chosen for their compact size and to facilitate the impedance matching and DC supply simultaneously. In total, the MPA consists of four identical PA cores. Each PA core employs a cascode configuration with a parallel RC element at the input for low-frequency stabilization and decoupling capacitors at the upper base device. Additionally, a bias circuit enabling improved temperature stability is integrated inside each PA core.

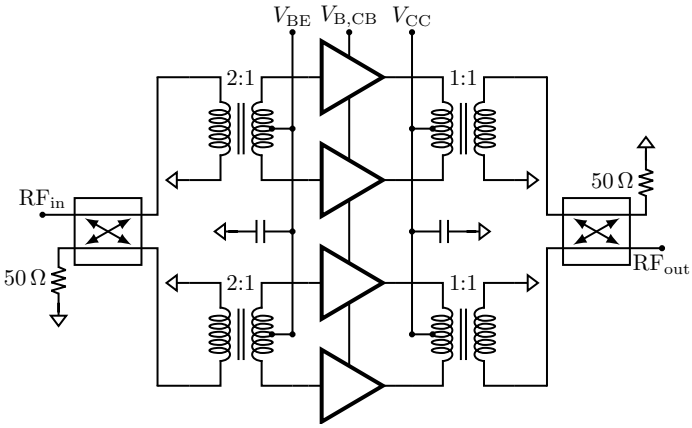


Figure 6.7: Q-band MPA schematic. Total emitter length $L_{\text{E,tot,Q1}} = L_{\text{E,tot,Q2}} = 144\,\mu\text{m}$. ©IEEE

6.2.1 Analysis and Design

To enable balanced operation a hybrid coupler is designed. For the design, a coupled line and branch line coupler, both of which are typically used, e.g. [CCG+23], are compared in Fig. 6.8. The couplers are designed for operation at Q-band frequencies and then EM simulated to compare their performance. The corresponding 3D rendered EM models are shown in Fig. 6.8a and 6.8b. The couplers especially differ in the chip area required for implementation. The coupled line coupler consumes only $0.1\,\text{mm}^2$ compared to $0.28\,\text{mm}^2$ for the branch line coupler. The simulation results are presented in Fig. 6.8c and Fig.6.8d for insertion and return loss.

Both couplers achieve high performance at Q-band, however, the coupled line (CL) coupler shows a $0.3\,\text{dB}$ lower insertion loss compared to the branch line (BL) coupler. When just a single band is targeted, both couplers show sufficient bandwidth, but if an extension to multi-band coverage is desired only the coupled line coupler achieves sufficient bandwidth and is thus chosen for the design. Since the branch line coupler offers an overall worse performance at this frequency range, a rat-race coupler was not investigated as no performance improvement over the coupled line coupler is expected. This is due to the increased total line length of the rat-race coupler compared to the branch line

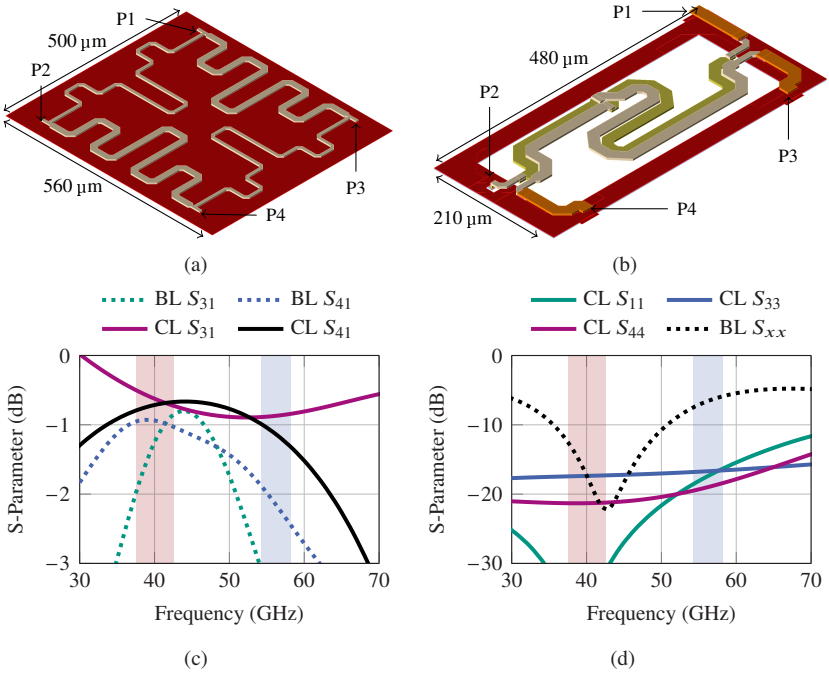


Figure 6.8: 3 dB hybrid couplers: a) 3D rendered layout branch line (BL) coupler and b) 3D rendered layout coupled line (CL) coupler. c) EM simulated insertion loss versus frequency and d) EM simulated return loss versus frequency ($1 \leq x \leq 4$).

coupler and thus, further increased area consumption and possibly increased loss. Lastly, the amplitude and phase imbalance for both couplers are presented in Fig. 6.9. The coupled line coupler shows reduced phase and amplitude imbalance over a larger bandwidth compared to the branch line coupler. For the targeted frequency band around 40 GHz the amplitude imbalance is below 0.4 dB and the phase imbalance is within 0.5°.

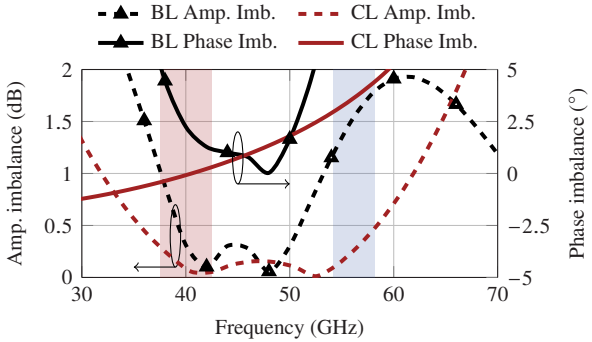
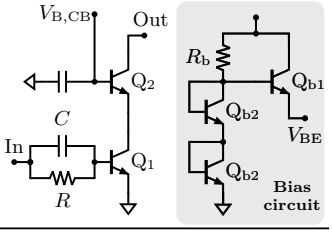


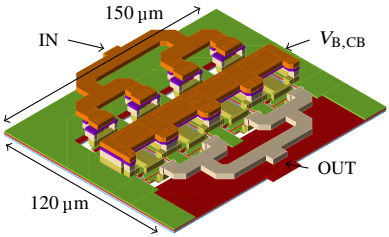
Figure 6.9: Input and output coupler amplitude and phase imbalance versus frequency.

The PA cores are designed for a linear output power of 20 dBm. The total emitter length needed for this power level is estimated by using results from Fig. 6.3b as a reference. In Fig. 6.3b an emitter length of 9 µm is used and an output power of 9.3 dBm is achieved. From this, it is estimated that a minimum total emitter length of 110 µm is required to surpass 20 dBm. Additional buffer is assumed for network loss and thus the final total emitter length of the PA is set to be 144 µm per transistor. To avoid low impedances the transistor size is divided into four equally sized PA cores, each with an emitter length of 36 µm per transistor. The schematic of the core, its bias circuit and the corresponding 3D rendered layout are shown in Fig. 6.10a and 6.10b. Including bias circuit and EM simulated parasitics, two-tone load-pull is performed on the resulting PA core and a peak PAE of 27 % at −25 dBc IMD3 is found. The two-tone



$L_{E,Q1,2}$	R	C	R_b	V_{CC}
36 µm	30 Ω	380 fF	0.8 kΩ	3.3 V

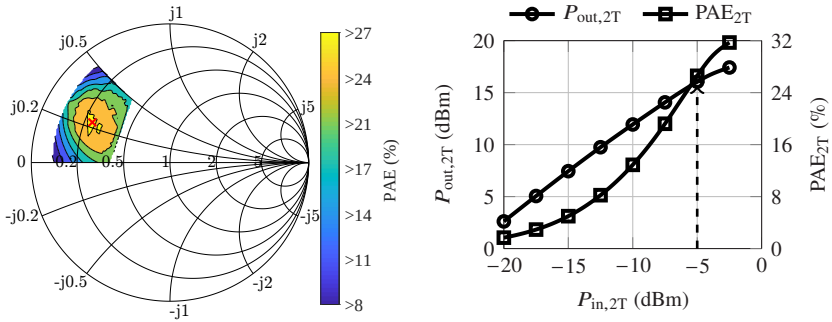
(a)



(b)

Figure 6.10: MPA core design: a) schematic and b) 3D rendered layout.

load-pull contours for two-tone PAE are presented in Fig. 6.11a. An optimal two-tone load impedance of $(9 + 12.5\mathrm{j})\,\Omega$ is determined. The input impedance of the core is simulated to be $(4.1 - 13\mathrm{j})\,\Omega$. The two-tone output power and PAE versus two-tone input power under ideal loading conditions is depicted in Fig. 6.11b.



(a) (b)

Figure 6.11: MPA core design: a) two-tone load-pull contours for PAE and b) large-signal parameters versus input power.

As the coupled line couplers are designed for a $50\,\Omega$ environment, transformers are used to match two differentially driven PA cores to $50\,\Omega$. The 3D rendered layouts of the input and output transformers are shown in Fig. 6.12a and Fig. 6.12b, respectively. At the input, the simulated input impedance, $Z_{\mathrm{in,core}}$, of $(4.1 - 13\mathrm{j})\,\Omega$ is too low for a basic transformer structure and a 2:1 transformer is used to provide a decent match. The input transformer is then optimized for low amplitude imbalance at $40\,\mathrm{GHz}$ to achieve equal compression in the driven cores. At the output, a 1:1 transformer is used and optimized for low insertion loss. For both transformers S-parameters versus frequency after EM simulation are presented in Fig. 6.12c and Fig. 6.12d. Amplitude and phase imbalance versus frequency are shown in Fig. 6.13.

The input transformer achieves a nearly perfect amplitude balance at $40\,\mathrm{GHz}$ but deviates for higher frequencies. Additionally, to achieve low amplitude imbalance the transformer's center frequency is shifted towards lower frequencies. The output transformer achieves an insertion loss of $1.2\,\mathrm{dB}$ and is matched to the load-pull impedance better than $-20\,\mathrm{dB}$. It is centered around $40\,\mathrm{GHz}$ and shows an amplitude imbalance of only $0.3\,\mathrm{dB}$. The phase imbalance of both

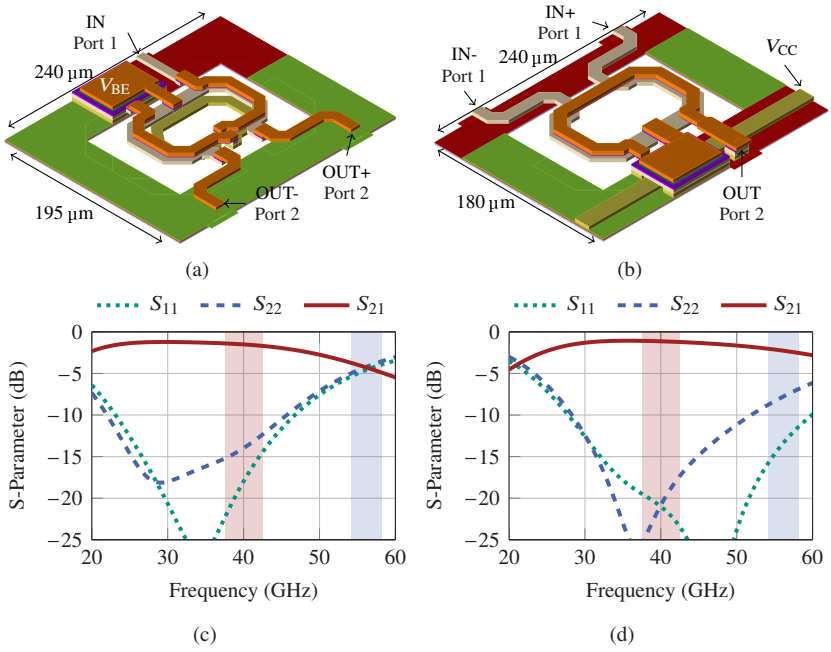


Figure 6.12: 3D rendered layouts: a) input transformer and b) output transformer. Simulation results for S-parameters versus frequency: c) input transformer and d) output transformer.

transformers is in the range of $5°$ for the targeted band around $40\,\mathrm{GHz}$. The total expected loss at the MPA output, including the coupler, is $1.8\text{-}2\,\mathrm{dB}$.

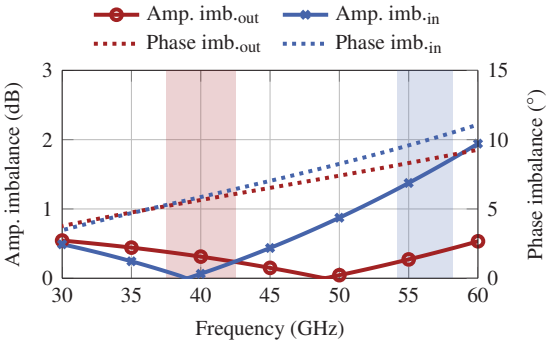


Figure 6.13: Input and output transformer amplitude imbalance and phase error versus frequency.

Lastly, a bias circuit for the CE transistor is designed to achieve stable performance over temperature. Simplified bias conditions such as voltage and current biasing do not offer stable performance versus temperature. To illustrate this, a simulative comparison of P_{out} and PAE at IMD3 = $-25\,\mathrm{dBc}$ for all three bias options (developed bias circuit, voltage and current bias) versus temperature is presented in Fig. 6.14.

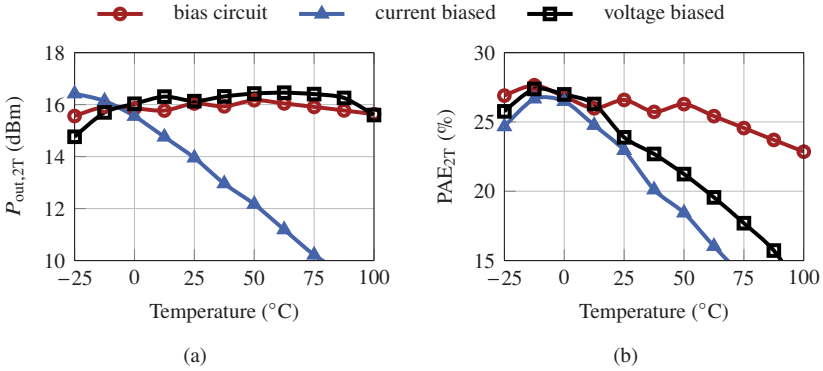


Figure 6.14: Simulated MPA core performance at IMD3 = $-25\,\mathrm{dBc}$ versus temperature for a dedicated bias circuit, voltage and current bias: a) P_{out} and b) PAE.

Additionally, the collector current, I_{C}, for the same operating conditions is shown in Fig. 6.15. A voltage bias enables stable output power over most of the temperature range; however this comes at the cost of increased collector current for higher temperatures, resulting in a decline of PAE and increased dissipated power. This can possibly lead to thermal runaway effects. In contrast, a current bias reduces the collector current at higher temperatures at the cost of significantly reduced output power and thus limited PAE. The designed bias circuit achieves a more stable operation compared to the other cases by a slow increase of collector current over temperature enabling a stable output power and a smaller decrease in PAE.

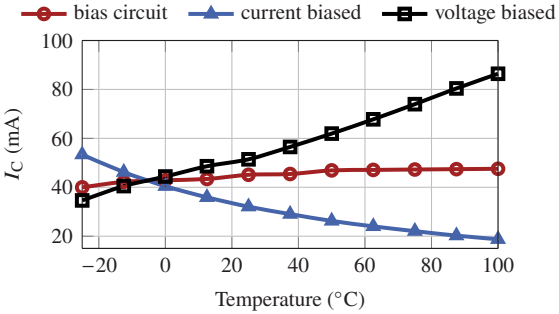


Figure 6.15: Simulated MPA core collector current, I_C, at IMD3 = −25 dBc versus temperature for a dedicated bias circuit, voltage and current bias.

A chip microphotograph of the complete MPA is presented in Fig. 6.16. It occupies a total area of $0.9\,\mathrm{mm}^2$.

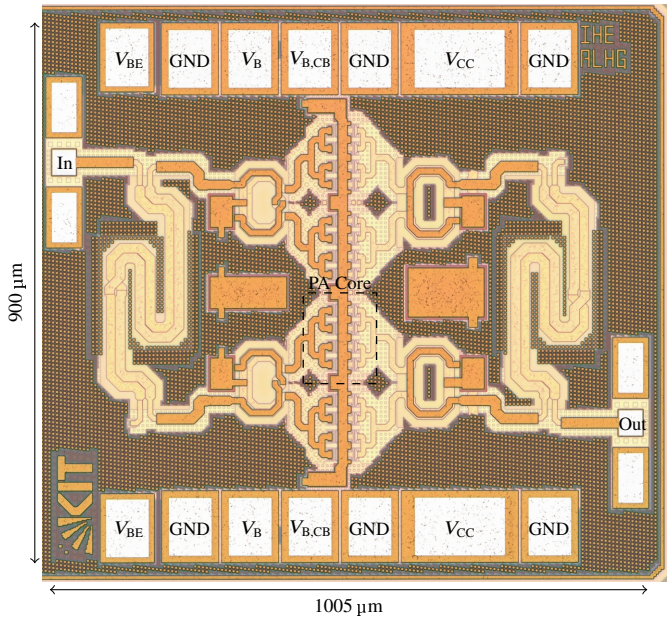


Figure 6.16: Chip microphotograph. Area: $0.9\,\mathrm{mm}^2$. RF core area: $0.53\,\mathrm{mm}^2$. ©IEEE

6.2.2 Characterization

The MPA is characterized by probing the RF pads directly and providing DC through a PCB with additional bypass capacitors. The PCB is depicted in Fig. 6.17a. The simulated and measured S-parameters for five measurement samples, as well as the simulated noise figure (NF) of the MPA are shown in Fig. 6.17b. A small-signal gain of 21 dB is achieved around 40 GHz and the MPA is matched to 50 Ω better than −10 dB at the input and output from 17 GHz up to 67 GHz. The 3 dB bandwidth is measured to be 16 GHz. For the targeted frequency band around 40 GHz the variation in small-signal gain is less than 0.6 dB. The noise figure is simulated to be around 5 dB.

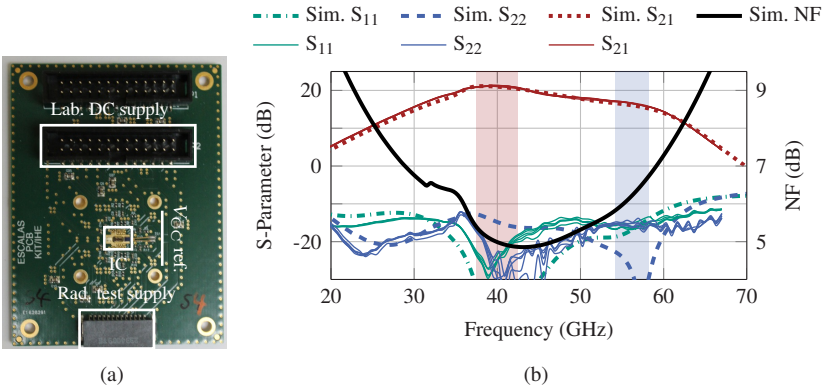


Figure 6.17: PA characterization: a) PCB assembly and b) simulated and measured S-parameter, simulated NF versus frequency.

Single-tone large-signal measurements are carried out with a signal generator as the source and a power meter as the load. At 39 GHz peak performance is achieved. The measured large-signal parameters versus input power are presented in Fig. 6.18a for output power and power gain and in Fig. 6.18b for PAE. A peak saturated output power of 24.2 dBm at a peak PAE of 33 % is achieved. At 6 dB power back-off the PAE is measured to be 12 %.

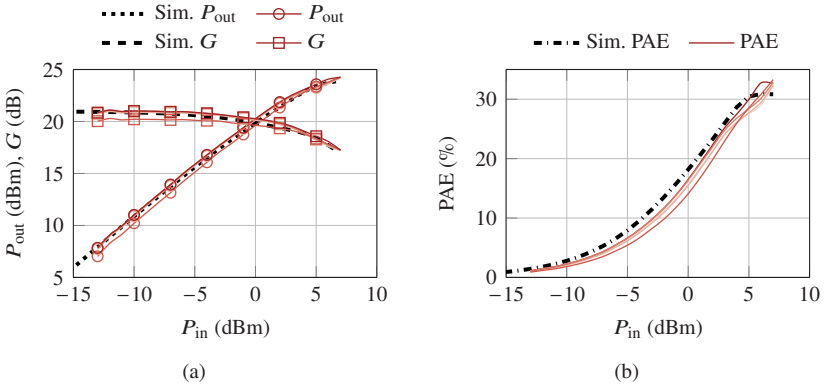


Figure 6.18: Simulated and measured (five samples) large-signal parameters at 39 GHz versus input power: a) P_{out} and G and b) PAE.

PAE and output power versus frequency are shown in Fig. 6.19. While peak values are achieved at 39 GHz, highest performance at 1 dB compression is achieved at 40 GHz and 42 GHz, thus the following measurements are presented at a center frequency of 40 GHz.

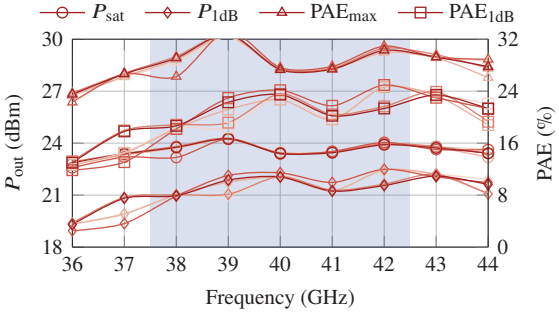


Figure 6.19: Measured large-signal parameters (five samples) versus frequency.

The measurement setup used in the following is depicted in the appendix in Fig. A.1c. To verify accurate prediction of performance by two-tone load-pull, first a two-tone measurement and then measurements with modulated signals are performed. Two-tone excitation is performed with a tone spacing, Δf, of 100 MHz and equal power distribution in both tones. The displayed two-tone

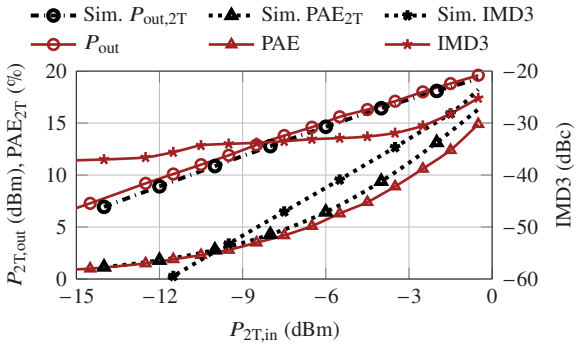


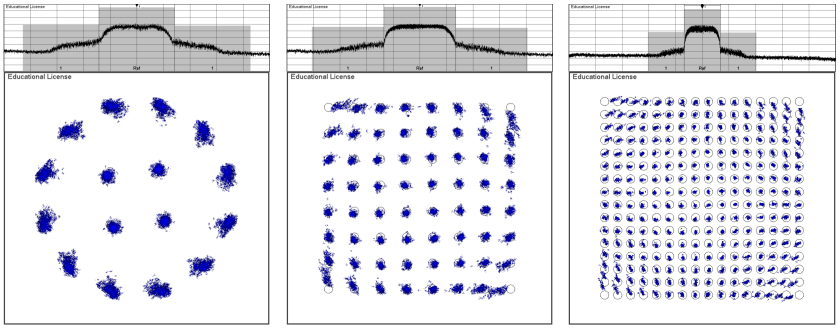
Figure 6.20: Simulated and measured large-signal parameter versus input power for two-tone excitation with f_c = 40 GHz and $\Delta f = 100$ MHz.

input power, $P_{\text{2T,in}}$, is the sum of both tones. Similarly, the two-tone output power, $P_{\text{2T,out}}$, is the sum of both amplified tones (only the desired tones). IMD3 always displays the worst tone to IM3 suppression. Simulated and measured two-tone output power and PAE, as well as IMD3 versus two-tone input power are presented in Fig. 6.20. PAE and output power agree well with simulation. For simulated and measured IMD3 a discrepancy for lower input power is observed and can be explained by the limited signal quality provided by the measurement setup. Towards higher input power, when the non-linearity of the PA dominates, the measured IMD3 closely resembles the simulated values. For IMD3 = -25.2 dBc, a PAE of 15 % and output power of 19.6 dBm are achieved.

Modulated measurements are performed for a 16-APSK and 64-QAM signal with a symbol rate of 400 MBd and a 256-QAM signal with a symbol rate of 200 MBd. The measurement results are summarized in table 6.2 and constellation diagrams are presented in Fig. 6.21. Both high average output power and average PAE are achieved for different modulations. For 64-QAM the PAE is measured to be 13.2 % at an EVM_{rms} of -25.3 dB.

Table 6.2: Summary of modulated measurement results.

Modulation	16-APSK	64-QAM	256-QAM
BW (MHz)	400	400	200
Data rate (Gbit/s)	1.6	2.4	1.6
$\mathrm{EVM_{RMS}}$ (dB)	−22.5	−25.3	−30.6
ACPR (dB)	−23.4	−29.3	−34
$P_{\mathrm{out,avg}}$ (dBm)	21.32	19	17.3
$\mathrm{PAE_{avg}}$ (%)	20.9	13.2	9.2



(a) (b) (c)

Figure 6.21: Measurement results for modulated signals at 40 GHz: a) 400 MSym/s 16-APSK; b) 400 MSym/s 64-QAM and c) 200 MSym/s 256-QAM.

In cooperation with a project partner, seven samples are further evaluated for their reliability in radiation tests. First, the samples are subjected to a 110 h burn-in at an elevated ambient temperature, T_{ambient}, of 85 °C. During this time, the PAs are turned on to catch aging effects and device failures before radiation testing. Fig. 6.22 shows the DC supply current consumption versus burn-in time and the ambient temperature profile. To simplify the test setup, the DC supplies of three PAs are connected to the same DC source simultaneously. Thus, each measurement is the summed current consumption of three PAs. The PAs are biased at the same operating point through their biasing circuits as for the previous high-frequency characterization. The average

current consumption per PA at 20 °C before burn-in is 121 mA. During burn-in the current consumption per PA is increased to 160 mA and after the burn-in is complete, it is 127 mA at an ambient temperature of 20 °C. Compared to before the burn-in, a relative increase of almost 5 % is observed. This is well within the range of 9 % anticipated by the manufacturer for this test. Additionally, no devices failed during the burn-in procedure.

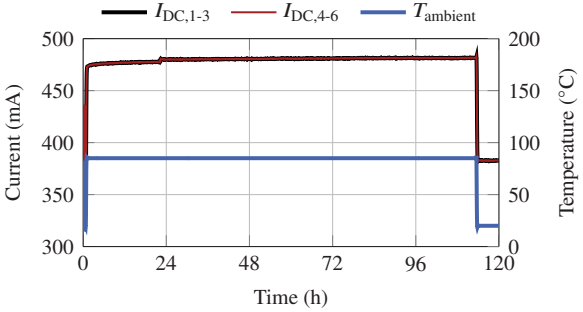


Figure 6.22: DC current consumption and ambient temperature versus time for a 110 h burn-in.

After burn-in total ionizing dose (TID) and single event effects (SEE) tests are performed on the PAs. During the SEE test, the samples are turned on and subjected to an ion beam with an ion flux of 30 000 Ion/s. When the ions hit the PAs, the ions can cause a change in voltage at their impact location inside the chip. This could lead to unstable conditions. The goal of this test is to verify that no device failures occur due to the ions. Fig. 6.23 shows the DC current consumption, temperature profile and beam flux versus test time for two samples. The profile of the current consumption follows the ambient temperature profile and no failures due to the ion beam are observed.

For the TID test, the PAs are subjected to a total dose of 100 krad of ionizing radiation. After the TID test, two samples are re-characterized in large-signal measurements. Fig. 6.24 shows the single-tone large-signal measurement results of the two samples before (P_{out} S1, P_{out} S3) and after (P_{out} S1 rad., P_{out} S3 burn-in) radiation testing. Sample 3 (S3) took part in the burn-in, but not the radiation related tests and is used as a reference. Sample 1 (S1) received the burn-in, SEE and TID tests. The measurement setup after radiation testing is different from the initial characterization as no driver amplifier is used. As a

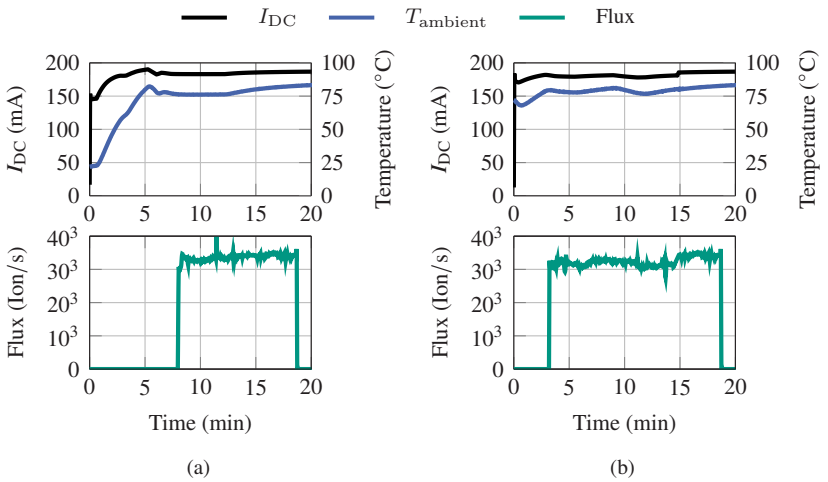


Figure 6.23: SEE test results for two samples: a) sample 1 and b) sample 2.

consequence, the PAs cannot be driven into saturation. Still, good agreement is achieved and performance only deteriorated by approximately $0.5\,\mathrm{dB}$ compared to before testing. No difference between sample 1 and 3 can be seen after radiation testing, showing all performance deterioration is due to the aging by burn-in.

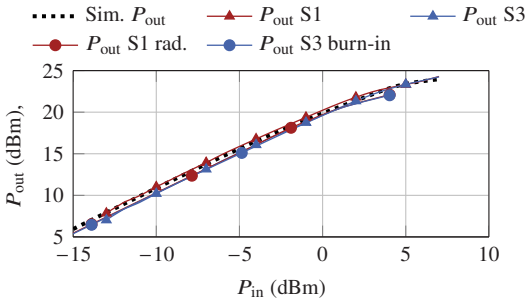


Figure 6.24: Single-tone large-signal measurement results after burn-in and radiation testing.

6.3 Conclusion

In this study, a new design method for performance optimization with linearity requirements is presented and a Q-band MPA targeting 37.5-$42.5\,\mathrm{GHz}$ for future space applications is designed. The presented optimization technique can be applied to any other type of PA design and proves useful in selecting a load impedance for the PA depending on a specific linearity requirement. A shift in optimal loading depending on the imposed linearity is shown in simulations. Burn-in and radiation testing are successfully performed on multiple samples of the designed PA without any device failures. Aging effects are within expected ranges and after being subjected to all tests, the performance difference is measured to be $0.5\,\mathrm{dB}$. This shows this design is a suitable candidate for space applications. For the designed MPA, a comparison with state of the art is provided in table 6.3. This work features state-of-the-art modulated output power and PAE. Compared to other PAs around this frequency range the highest modulated output power is achieved. Only [LHHJ24] achieves higher modulated PAE. This can be explained by three factors; First, the PA designed in this work could be significantly improved by replacing the input and output transformers for a low-loss 2-to-1 combiner. This is expected to improve PAE and P_{out} by $3\,\%$ and $0.4\,\mathrm{dB}$ respectively but comes at the cost of increased area consumption. If the requirement for the small-signal output match is relaxed, the balanced architecture could be replaced by an in-phase 4-to-1 combiner associated with a total combining loss of only $1.1\,\mathrm{dB}$ for the entire PA. This is expected to improve the performance to $25\,\mathrm{dBm}$ saturated output power and peak PAE to approximately $38\,\%$. Similarly, the average performance for modulated signals would improve by $0.8\,\mathrm{dB}$, resulting in an expected average PAE of $16\,\%$. Second, the modulated output power achieved by this PA is $1\,\mathrm{dB}$ larger and thus a lower PAE is expected. Lastly, EVM requirements for the same modulation complexity are generally harder to meet with QAM, as a higher PAPR is produced.

Table 6.3: Performance comparison with state of the art

Ref.	f_C (GHz)	P_{sat} (dBm)	PAE_{max} (%)	V_{CC} (V)	Modul.	$P_{out,avg}$ (dBm)	PAE_{avg} (%)
This work^{+}	40	24.2	33	3.3	64QAM 400 MHz	19	13.2
[LHHJ24]$^{+}$	43	24	35.3	3.3	64APSK 250 MHz	18.1	21
[HWW19]$^{+}$	39	17	21.4	1.5	64QAM 500 MHz	9.3	17.2†††
[CCG^{+}23]$^{\$}$	40	25.1	27.9	2	64QAM 200 MHz	16.5	13.1
[DDT^{+}20]†	39	26	26.6	2.2	64QAM 600 MHz	19.5	8.3
[LCCF18]††	47	22.7	40	4	-	-	-

$^{+}$ 130 nm SiGe BiCMOS $^{\$}$ 45 nm CMOS † 28 nm CMOS
†† 0.1 µm GaAs ††† collector efficiency

7 Conclusion and Outlook

The presented work investigates CMOS and SiGe BiCMOS power amplifier design at mmWave frequencies. The presented methods and prototype PAs aim for high efficiency and high output power for future communication, RADAR and SatCom applications. First, using an LC-matching network optimization technique, very compact and highly efficient PAs with low to medium output power are presented. Then, chapters 4 and 5 focus on design methods to increase the limited output power of Si-based PAs at mmWave frequencies. In chapter 6 optimization of PA performance while meeting linearity specifications is investigated.

In chapter 3 an LC-matching network optimization technique is introduced. It focuses on accurate prediction of the final network performance before implementation by including network component losses depending on the component value and frequency of operation. By applying this method to the SG13G2Cu technology at $28\,\mathrm{GHz}$, the PI network in L-C-L configuration is selected as the most efficient network solution for impedances within the G = 1 circle of the Smith chart. In previously published literature, a higher number of components in the network improved network performance for increasing transformation ratio, however, by including the component imperfections in more detail, networks with more than three components do not show a significant advantage for typical matching scenarios in the Smith chart ($Z_0 = 50\,\Omega$, $|\Gamma| < 0.9$). Two prototype PAs are designed using the insight gained by this method. The first PA is implemented in IHP's $130\,\mathrm{nm}$ BiCMOS technology SG13G2Cu and the second PA is integrated in GlobalFoundries' $22\,\mathrm{nm}$ FD-SOI technology. Both PAs show very high efficiency and are among the best in terms of RF core power density in published literature. These results highlight that LC-matching networks are suitable candidates for both high efficiency and especially area efficient designs. This is an important aspect in tightly spaced antenna array configurations. The method presented can be extended to other operational frequencies.

The following chapter explores different on-chip power combining techniques. Transformer-based combining and Wilkinson combiners are investigated for their insertion loss and scalability. Special focus is set on maximizing the achievable output power. Research conducted within this chapter suggests that the number of inputs which can be combined on-chip with reasonable combiner efficiency using these structures is limited to 16 at K_a-band. A higher number of inputs either yields impractical RF pads at the chip center, or very lossy input and output networks, as the physical distances become longer than $\lambda/4$ within the combiner. The limited number of PA cores requires a large amount of parallelization inside each core to increase the achievable output power. This, in turn, reduces the impedances to be matched, requiring solutions that can provide high combining efficiency for large transformation ratios. A transformer-based prototype is explored, showing promising results in simulation. It consists of two cores and a single transformer. To expand the transformer-based PA the limited scalability and highly complicated design of transformer-based combining structures is a critical issue. Additionally, the loss of this single transformer is similar to the loss of a 4:1 TL-based Wilkinson combiner. Thus, TL-based combiners and their scalability are investigated and appear to be more efficient in the chosen technology. By choosing optimal intermediate impedances for multi-stage combiners, the combining loss for 16 individual $10\,\Omega$ sources into a $50\,\Omega$ load can be kept as low as $1.2\,\mathrm{dB}$.

Due to the limited number of PA cores that can be power combined chapter 5 explores the challenges and limits of large device parallelization in PA cores. First, the limits in PA core design are fundamentally investigated by an analysis of the core parasitics during implementation. The size or output power of a single PA core is limited by these parasitics. The parasitics mainly impact the core's performance when the impedances to be matched become low, e.g., in the range of 5-10 Ω. At some point a larger PA core cannot deliver more power into its optimal load, than a smaller core. Additionally, large PA cores require matching networks with high network losses, reducing the achievable PAE. To improve the performance of large cores a novel design method named 'Resonated Amplifier Cores' is introduced. A resonated amplifier core utilizes multiple shunt inductors at the input and output of the core to resonate out the parasitic capacitances of the core. The local impedances inside the core are thus increased and the parasitics' impact on the core performance is reduced. Additionally, the impedances to be matched are larger. Optimization techniques for the new design method are presented. Four prototype PAs are developed, each

refining the design method further. The first PA is realized in IHP's 130 nm BiCMOS technology SG13G2Cu and to the best of the author's knowledge, is the first silicon-based PA achieving more than 30.5 dBm of output power with a PAE of about 25 % at K_a-band frequencies without requiring an off-chip combiner. The PA is designed using constant inductor values within its PA cores. In a second PA the method is tested in GlobalFoundries' 22 nm FD-SOI at Q-band frequencies. For this PA, an output power of 24 dBm is achieved at 40 GHz. This PA used a non-uniform calculation method for the shunt inductors, for which parasitics are more accurately compensated. However, the improved compensation requires increasing inductor size throughout the core, reaching impractical values with low quality factors. Lastly, two PAs are integrated in IHP's SG13G2Cu technology including further improvements to the non-uniform inductor design. Throughout the core the number of unit cells per inductor and the inductor size are varied for an optimal compensation of the parasitics combined with a high inductor quality factor. Optimized TL combiners from chapter 4 significantly reduce the losses in the passives compared to the first prototype. Both PAs show record breaking performance with the first PA achieving 31.7 dBm of output power at 28 GHz with a record breaking PAE of 36.7 % and the second PA achieving a close to GaN-level output power of 36.7 dBm (4.7 W) at a PAE of 28 %. This level of output power advances the state of the art of SiGe BiCMOS PAs by around 6 to 10 dB. A comparison is presented in Fig. 7.1

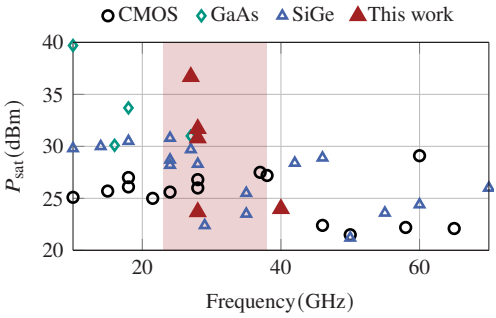


Figure 7.1: Comparison with state of the art showing saturated output power versus frequency for publications in SiGe BiCMOS, CMOS and GaAs technologies. Used references are listed in appendix A.5.

An advantage over state of the art is achieved. Additionally, Fig. 7.2 explores the achieved PAE versus saturated output power for the highlighted frequency range. It shows that the designs are among the most efficient for their respective signal power.

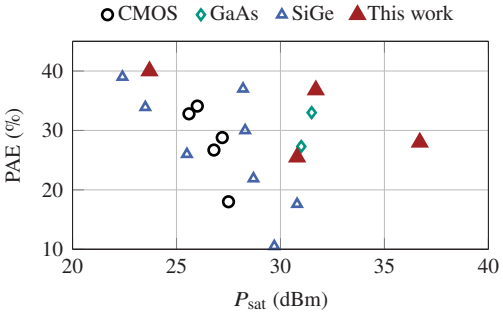


Figure 7.2: Comparison with state of the art showing peak PAE versus saturated output power for publications in SiGe, CMOS and GaAs technologies. The references used are the same as in Fig. 7.1.

In the final chapter a PA design method for performance optimization at a given linearity criterion and a corresponding MPA prototype for future space applications at Q-band frequencies are presented. The design method extends the typical load-pull simulation performed at single-tone excitation to two-tone excitation. This is done to find the optimal load-pull impedance for a certain IMD3 requirement instead of optimal P_{sat} or peak PAE. The acquired two-tone load-pull impedance varies depending on the IMD3 requirement. The optimum impedance for the specification provided in this chapter is close to the optimal load-pull impedance for single-tone P_{sat}. The MPA is then designed for a linear output power of approximately $20\,\mathrm{dBm}$. While a high PAE of $13.2\,\%$ for a 64-QAM signal is achieved, the matching network could be improved to reach even higher efficiency. A main contributor to the elevated loss is the balanced operation. While this achieves a sufficiently low output return loss, the coupler adds roughly $0.6\,\mathrm{dB}$ of additional loss. When the coupler loss is neglected, the achieved average PAE for a 64-QAM signal could be beyond $16\,\%$.

The design methods and prototypes presented in this dissertation rival or surpass state-of-the-art performance. Different challenges for mmWave PA design

are explored. The presented design methods are extensions of basic design principles and can be broadly applied to other technologies and numerous problems.

Outlook

To move beyond the presented work, the optimization of the resonated amplifier cores, used throughout chapter 5, could be expanded to differential circuits. This may lead to multiple advantages due to a potential increase in inductor quality factor. While not discussed in this work, usage of virtual ground allows for inductor quality factors beyond 20 in the presented technologies. This reduces the loss attributed to the inductors and further maximizes the local impedances. Secondly, the width of the line segment connecting the unit cells could be adjusted to reduce its inductive effect, however as impedance drops this may run into geometric limits. A last layout improvement may be tapping the RF input and output at the center of the unit cells instead of opposing sides, but then other challenges arise, such as routing the input and output between the resonating inductors and high width of the cores.

Another potential optimization method is to allow for individual biasing of the unit cell segments inside the resonated amplifier core and adjust biasing depending on the imposed requirements, e.g., high peak efficiency or high back-off efficiency. A significant challenge may be the control of the rising number of bias paths.

A third promising option is the combination of the design methods presented for high peak performance, such as in chapter 3 and 5, with the technique presented in chapter 6 on back-off performance. Multiple methods could be used in conjunction. Additionally, for the PA cores developed in chapter 5, a combination with topologies used for back-off improvements such as Doherty or Load Modulated Balanced Amplifier (LMBA) may leverage the advantages of more techniques.

Lastly, resonated amplifier cores may be successfully implemented to allow for frequency switching. By introducing switches into the resonating inductors, it may be possible to achieve high output power for multiple bands. However, layout optimization grows in complexity and area consumption would significantly increase.

A Appendix

This appendix presents additional data, illustrations of measurement setups and DC supply boards for the high power designs. Additionally, a basic on-chip temperature sensor developed and investigated during this work and a chip to coaxial connector transition are shown.

A.1 Measurement Setups

This section presents the measurement setups used throughout this work for small-signal (Fig. A.1a), single-tone large-signal (Fig. A.1b) and multi-tone large-signal as well as modulated (Fig. A.1c) characterization. DC is provided by a source measurement unit and for most designs routed through a dedicated DC supply PCB.

For small-signal characterization Keysight's PNA X is used up to $67\,\mathrm{GHz}$. Using standardized calibration substrates, the measurement's reference plane is shifted to the probe-tips. The output path is attenuated for protection of the measurement equipment. For the high power designs, high attenuation causes ripples in the S_{22} measurements.

Large-signal single-tone characterization is performed using a signal generator as the signal source. Depending on the required input power level an additional driver amplifier is included in the setup. The load is comprised of an attenuator and a power meter. Calibration is performed to the end of the coaxial cables. Probes are either removed by two-tier calibration, yielding the S-parameter data of the probes, or using the data-sheet values of the probes. Harmonic content is significantly attenuated in all measurements as the attenuators used during measurements have a cut-off frequency of $40\,\mathrm{GHz}$. Stability is ensured in a second step by verifying the output spectrum of the PA.

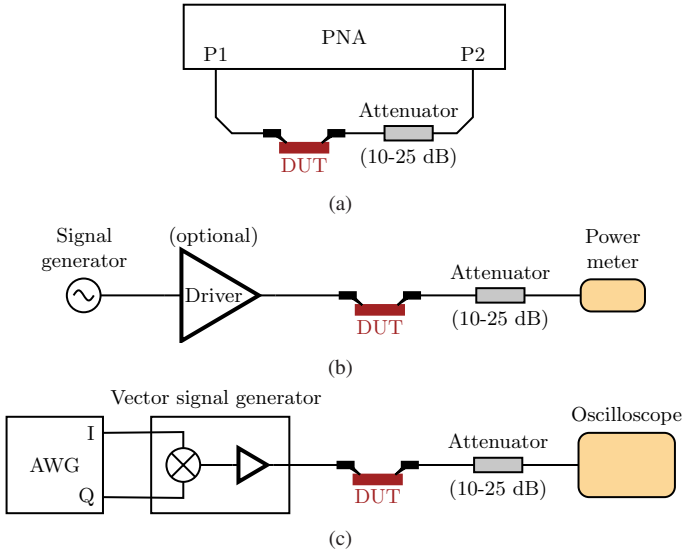


Figure A.1: Measurement setups: a) small signal measurement setup; b) single tone large signal measurement setup and c) measurement setup for modulated signals.

Multi-tone and modulated measurements are performed using an AWG as the baseband source for complex modulated signals (e.g., 64-QAM). The I- and Q-signals are fed to a vector signal generator, which in turn mixes the signals up to a specified carrier frequency and specified amplitude. A digital oscilloscope is used to demodulate the data after amplification by the device under test (DUT). Power calibration is performed in the same manner as for single-tone characterization. For the largest designs in chapter 5 an additional driver amplifier is connected to the vector signal generator.

A.2 In-phase Power Combiner Comparison

This section provides additional data visualization for the results presented in chapter 4.2. Figure A.2 presents the difference in combining loss for different combiner configurations towards a $50\,\Omega$ load at $28\,\mathrm{GHz}$. A positive number corresponds to a lower loss for the single stage configuration. A negative number

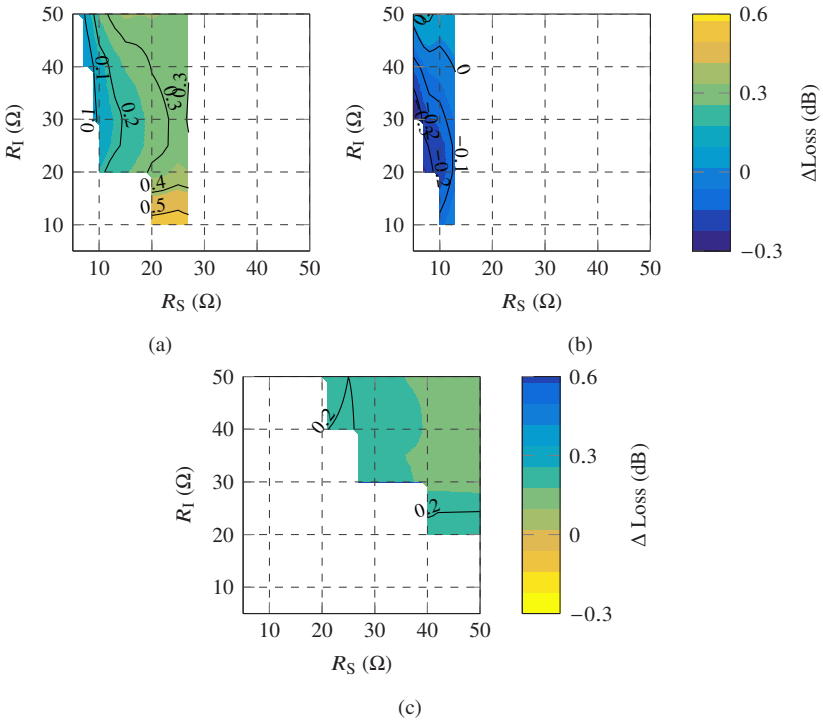


Figure A.2: Combining loss difference of: a) two stage 4-to-1 and one stage 4-to-1 combiner in the Cu layer; b) two stage 8-to-1 and one stage 8-to-1 combiner in the Cu layer and c) two stage 4-to-1 and one stage 4-to-1 combiner in the Al layer.

corresponds to a higher loss for the single stage configuration. Both in the Cu and Al layer single stage 4:1 combining results in a 0.2 to 0.3 dB advantage over two stages of 2:1 combining, as presented in Figs. A.2a and A.2c. This changes for higher combining ratios. Illustrated in Fig. A.2b for an 8:1 combiner in the Cu layer, the single stage combiner incurs a 0.3 dB higher loss compared to a two-stage design.

Fig. A.3 depicts the insertion loss of a two-stage 16:1 combiner integrated in the Al layer consisting of two stages of 4:1 combiners. While this combiner shows the lowest loss, less than 1.1 dB for all possible impedance combinations, it is

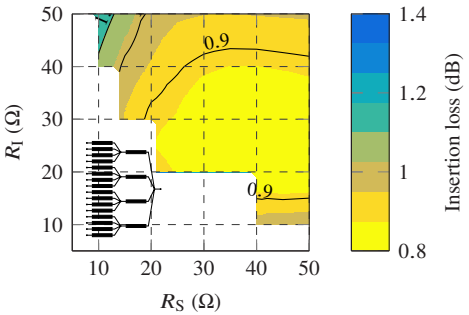


Figure A.3: Insertion loss of a two stage 16:1 power combiner into a 50 Ω load at 28 GHz, consisting of two stages of 4:1 combiners in the Al layer.

impractical during integration. The required line widths in the Al layer result in large area consumption, especially for the first stage which is repeated four times. Due to the area consumption integration of the second stage becomes challenging, as the distance between the outputs of the first stage could be in the range of half a wavelength.

A.3 Printed Circuit Boards for Measurements

For most of the measurements presented in this work, PCBs for DC supply and heat sinking are designed. The PCBs include a decoupling network to ensure low frequency stability of the PAs. Fig. A.4 presents the decoupling network used for all DC voltages. The first inductance connected to the chip models the required wire bond and is in the range of 0.5-2 nH depending on the wire bond's length and how many wires are parallelized. All further inductances model track length on the PCB and finally the cable to the DC power supply. Resistors after the bypass capacitors are used to present additional loss.

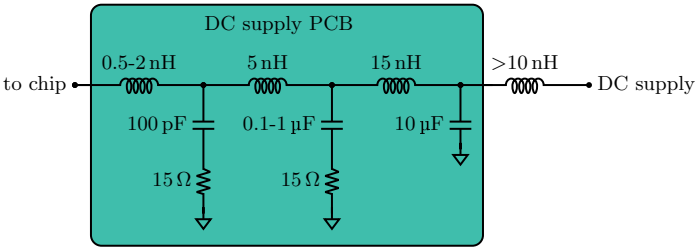


Figure A.4: Decoupling network for DC supply voltages on the PCBs.

A.4 Additional Material on Core Design

This section contains additional material for chapter 5.

In literature unit cells are typically arranged as shown in Fig. A.5. The UCs are directly connected in parallel, however, in this arrangement the line segments do not compensate for the phase shift of each UC. The signal path for the inner most unit cells, 1 & 2 in this case, and the outer most UCs is different in length. Therefore, the amplified signal does not add up perfectly at the output of the core and the arrangement presented in chapter 5 is preferred for larger cores. Additionally, as more UCs are parallelized the PA core becomes physically wide and placing multiple PA cores next to each other will create long routing distances.

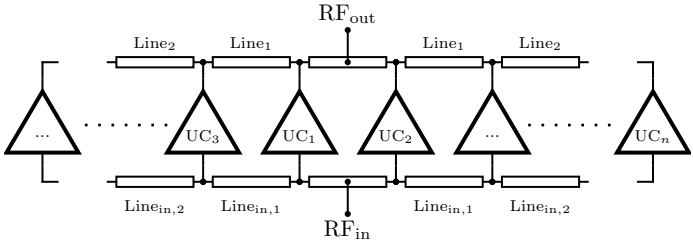


Figure A.5: Parallel unit cell arrangements by direct device parallelization. ©IEEE

A.5 References for State of the Art Comparison

The references used in Fig. A.6 are summarized in this section.

SiGe references: [WZZ+22, CHL16, CKA+22, LHW18, WW20a, WNP16, WNP16,ELM14,WW20a,TBH+21b,DH17b,XWW24,TCR13,DH15,LKS22, CS17,GC21,LR16,RQG+22].

CMOS references: [TP21,RJA18,CHA+13,HCM14,JLP+23,HLLW18,HLLW18, MMM+23,ZLC24,ZYC+24,HCM16,HML+23,SK19,NJW19,HJD+24,EAR19].

GaAs references: [XWT+22,WYL18,NP16,AYM+21,PKC+11].

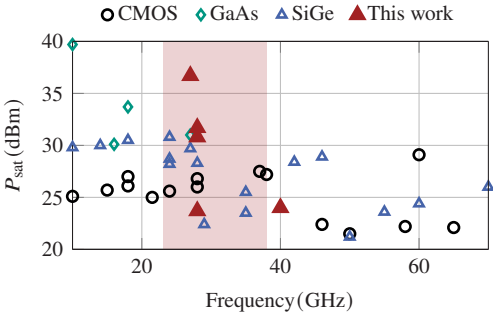


Figure A.6: State of the art comparison showing saturated output power versus frequency for publications in SiGe BiCMOS, CMOS and GaAs technologies.

A.6 Temperature Sensor

During the simulation of PAs the thermal coupling between individual transistors is typically neglected. However, as output power and consequently power consumption increases, the on-chip temperatures rise and a significant thermal coupling between the transistors can occur. Tools like Keysight's ADS allow for electrothermal co-simulation to include thermal coupling effects, but simulation time grows, especially for large circuits. To verify simulation results and to track on-chip temperatures during operation, a compact on-chip temperature

sensor prototype is developed. The footprint's size is optimized to allow for placement of multiple sensors within a PA core. This allows for detection of local temperature differences. Two versions of a basic temperature sensor are shown in Fig. A.7. By shorting either an HBT's base and collector or collector and emitter an HBT can be operated as a diode. The voltage across the HBT in diode configuration when injecting a constant reference current, I_{Ref}, is temperature dependent.

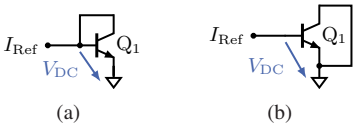


Figure A.7: Basic temperature sensing by HBTs in diode configuration: a) shorted Collector-Base and b) shorted Collector-Emitter.

For a single finger transistor, in both cases, a similar temperature sensitivity, ΔV_{temp}, of approximately $1\,\mathrm{mV/°C}$ for a constant reference current of $10\,\mu\mathrm{A}$ is achieved. The resulting DC voltage versus temperature is presented in Fig. A.8. In the case of a larger reference current only the shorted collector-base version is a suitable solution, however due to self-heating of the transistor smaller reference currents are preferred.

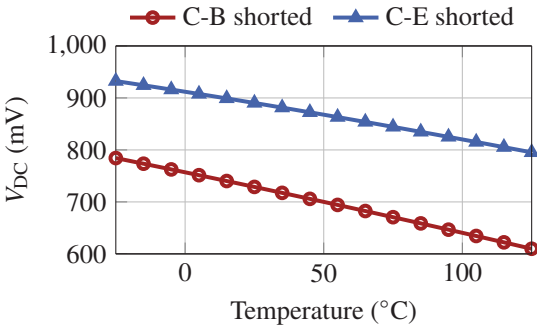


Figure A.8: Simulated DC voltage during current injection ($10\,\mu\mathrm{A}$) versus temperature.

A 3D rendered layout of the shorted collector-emitter version in IHP's SG13G2Cu technology is presented in Fig. A.9 occupying only 10 by $10\,\mu\mathrm{m}$. The layout

can be directly interfaced below a ground plane on the lower metal layers to avoid interference with RF performance.

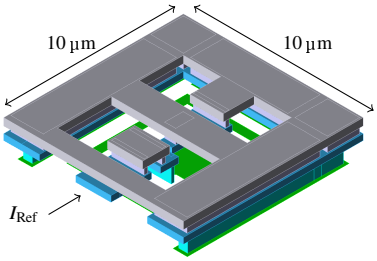
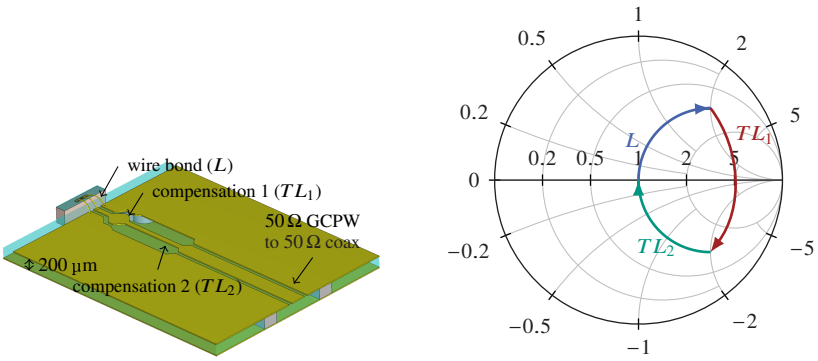


Figure A.9: 3D rendered layout of an example temperature sensor.

A digital control circuit and a stable reference current source, to enable the usage of multiple temperature sensors within a chip, are not developed in this work.

A.7 28 GHz Chip to Coaxial Transition

During a project investigating the suitability of SiGe BiCMOS PAs for space applications, such as SatCom, a package transition from the chip pad to a coaxial connector is designed. The PA presented in chapter 3.1.1 is used as a prototype. The transition is intended for PA characterization before and after radiation exposure of the chip. The transition assumes $50\,\Omega$ interfaces both at the chip pad and at the coaxial connector. It is designed to compensate for the wire bonds required to contact the RF pads. A 3D rendered model of the structure is presented in Fig. A.10a. The compensation utilizes a wide TL section, TL_1, followed by another inductive section, TL_2 for compensation. A simplified Smith chart illustration of the resulting transformation is presented in Fig. A.10b.



(a) (b)

Figure A.10: Chip to coaxial transition: a) 3D model and b) simplified transformation.

The designed transition is EM simulated, and the insertion loss is expected to be 0.4 dB at 28 GHz. The simulation conditions are: Wire bonds are made of gold and have a diameter of 17 µm. The PCB is manufactured using Rogers' 4003C ($\epsilon_R = 3$, $\tan\delta = 0.01$) with a substrate thickness of 200 µm and metal thickness of 17 µm. The simulation results for the transition are presented in Fig. A.11.

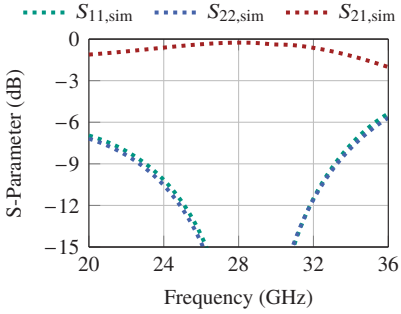


Figure A.11: Simulated S-parameters after EM simulation versus frequency.

Initial S-parameter measurements are shown in Fig. A.12. For comparison, the bare die measurements and simulation results are included. At 28 GHz,

measurement results indicate good RF performance of the transition, however mechanical instability caused wire bond failures upon tightening and untightening the coaxial connectors and no further characterization was possible.

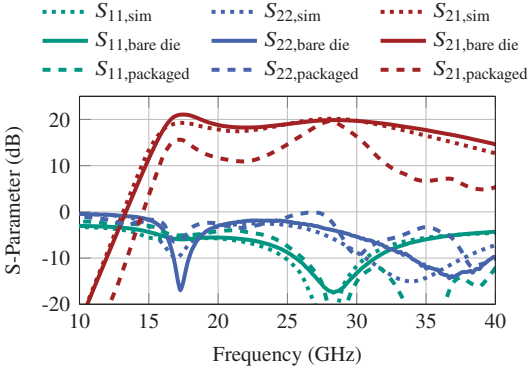


Figure A.12: Simulated and measured S-parameters versus frequency.

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