State-of-Grid-Based Control of Hybrid AC/DC Microgrids

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M.Sc. Ömer Ekin
geb. in Iskenderun, Türkei

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Hauptreferent:	Prof. Dr. Veit Hagenmeyer
Korreferent:	Prof. Dr.-Ing. Giovanni De Carne

Abstract

The increasing integration of renewable energy sources and the electrification of mobility, heating, and industry increase the complexity of power system operation and control. Microgrids have emerged as a promising concept to address this complexity by enabling the coordinated integration of distributed energy resources within well-defined subsystems. While conventional microgrids are typically based on Alternating Current (AC) architectures, the inherent Direct Current (DC) nature of emerging technologies, such as Photovoltaic (PV) systems, Battery Energy Storage Systems (BESSs), and Electric Vehicles (EVs), makes DC microgrids an efficient and flexible alternative, offering higher efficiency and reduced system complexity. However, the control of DC microgrids interconnected with AC systems, or hybrid AC/DC microgrids, remains an open research challenge, particularly when aiming for decentralized and communication-free operation.

This dissertation presents a novel State-of-Grid (SoG)-based control framework for hybrid AC/DC microgrids, enabling decentralized, communication-free State-of-Charge (SoC) balancing, coordinated power sharing, and grid-supportive behavior under realistic operating conditions. The proposed approach projects the energy states of distributed storage units into observable local grid quantities, specifically, voltage and frequency, and utilizes these signals to coordinate power sharing and SoC balancing among BESSs, without requiring explicit communication.

Building on this foundation, the SoG concept is extended to incorporate ancillary services. A SoG-based Virtual Synchronous Machine (VSM) is introduced to provide inertia and frequency support in the AC domain, with the SoC state

dynamically modulating the power reference. In parallel, the concept of Grid-Supportive Loads (GSLs) is developed to enhance voltage stability on the DC side. These ZIP-modeled loads autonomously adjust their power consumption in response to local voltage deviations and employ an energy-aware restoration strategy to preserve system balance.

The stability of the proposed control strategies is analyzed using Lyapunov methods and Singular Perturbation Theory. Experimental validation is conducted in the Smart2DC microgrid laboratory, established as part of this dissertation. Four representative scenarios are examined: islanded DC operation, cross-domain SoC balancing, virtual inertia provision, and the interaction of SoG-controlled storage units with GSLs.

The results demonstrate that the proposed framework achieves reliable SoC equalization, stable voltage and frequency regulation, and robust operation even under heterogeneous storage capacities, line asymmetries, and dynamic load profiles, all without relying on communication infrastructure. The methods developed in this dissertation establish a practical foundation for autonomous, resilient microgrids and demonstrate their viability under realistic operating conditions.

Kurzfassung

Die zunehmende Integration erneuerbarer Energien sowie die Elektrifizierung von Mobilität, Wärme und Industrie erhöhen die Komplexität des Betriebs und der Regelung elektrischer Energiesysteme. Microgrids haben sich als vielversprechendes Konzept etabliert, um dieser Komplexität zu begegnen, indem sie die koordinierte Einbindung verteilter Energieressourcen in klar abgegrenzten Teilsystemen ermöglichen. Während herkömmliche Microgrids typischerweise auf Wechselstrom (AC) Architekturen basieren, macht die inhärente Gleichstrom (DC) Natur wesentlicher Technologien wie Photovoltaikanlagen, Batteriespeicher und Elektrofahrzeuge DC-Microgrids zu einer effizienten und flexiblen Alternative mit höheren Wirkungsgraden und reduziertem Systemaufwand. Die Regelung von DC-Microgrids, die mit AC-Systemen gekoppelt sind, also hybriden AC/DC-Microgrids, stellt jedoch nach wie vor eine offene Forschungsfrage dar, insbesondere wenn eine dezentrale und kommunikationsfreie Betriebsweise angestrebt wird. Diese Dissertation stellt ein neuartiges State-of-Grid (SoG)-basiertes Regelungskonzept für hybride AC/DC-Microgrids vor, das dezentrale, kommunikationsfreie State-of-Charge (SoC)-Balancierung, koordinierte Lastaufteilung und netzstützendes Verhalten unter realistischen Betriebsbedingungen ermöglicht. Der Ansatz projiziert die Energiezustände der verteilten Speichereinheiten in lokal messbare Netzgrößen, konkret in Spannung und Frequenz, und nutzt diese Signale, um die Leistungsaufteilung und SoC-Balancierung der Batterien ohne explizite Kommunikation zu koordinieren.

Das SoG-Konzept wird erweitert, indem das SoG-Signal über den Interlink-Wandler in die Frequenz des AC-Netzes eingebettet wird. Dadurch wird eine SoC-Balancierung über beide Domänen hinweg ermöglicht und gleichzeitig virtuelle Trägheit in das AC-Subsystem integriert. Zusätzlich wird das Konzept

der Grid-Supportive Loads (GSLs) eingeführt, die lokale Spannungssignale nutzen, um den DC-Bus bei transienten Störungen zu stabilisieren.

Die Stabilität der vorgeschlagenen Regelungsstrategien wird mithilfe von Lyapunov-Methoden und der Theorie singulärer Störungen analytisch untersucht. Ihre Robustheit wird experimentell in einem eigens für diese Arbeit etablierten DC-Microgrid-Labor validiert. Die Validierung umfasst vier repräsentative Szenarien: Inselbetrieb des DC-Netzes, domänenübergreifende SoC-Balancierung, Bereitstellung virtueller Trägheit und koordinierte Interaktion von SoG-gesteuerten Speichern und GSLs.

Die Ergebnisse zeigen, dass das SoG-basierte Konzept eine schnelle und zuverlässige SoC-Angleichung, stabile Spannungs- und Frequenzregelung sowie eine Resilienz gegenüber heterogenen Speicherkapazitäten, asymmetrischen Leitungsimpedanzen und dynamischen Last- und Erzeugungsprofilen ermöglicht, und das ohne Kommunikationsinfrastruktur.

Abschließend werden mögliche zukünftige Forschungsrichtungen aufgezeigt, darunter die Integration einer tertiären Regelungsebene, adaptive Parameteranpassung und die Erweiterung des Konzepts auf vermaschte und niederimpedante AC-Netze.

Preface

I would like to express my sincere gratitude to my doctoral supervisor and mentor, Prof. Veit Hagenmeyer, for his continuous support, scientific guidance, and for providing the outstanding working conditions that made this research both possible and inspiring. His visionary perspective and emphasis on rigorous scientific reasoning have profoundly shaped my way of thinking.

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Special thanks go to Prof. Gilney Damm, whose constructive feedback, thematic guidance, and insightful discussions were highly valuable. His advice and explanations greatly deepened my understanding of the theoretical foundations.

I would like to thank all my colleagues at the Institute for Automation and Applied Informatics (IAI), in particular the team at the Energy Lab, for the productive working environment and the collaborative atmosphere. Special thanks go to Friedrich, Luigi, Richard, Johannes, and Simon for their continuous support, insightful discussions, and shared enthusiasm for research, which created an inspiring environment that made this work possible.

I am grateful to my family for their love and support throughout this journey. Most of all, I owe my deepest thanks to my wife, Canan, for her continuous support and for providing stability and perspective throughout this demanding time. Her presence has been my greatest source of strength and ambition.

Contents

Acronyms and symbols

Acronyms

AC	Alternating Current
L-ADRC	Linear-Active Disturbance Rejection Control
NL-ADRC	Nonlinear-Active Disturbance Rejection Control
AGC	Automatic Generation Control
BESS	Battery Energy Storage System
BPF	Band-Pass Filter
DC	Direct Current
CCM	Continuous Conduction Mode
DBS	DC-Bus Signaling
DSP	Digital Signal Processor
ENTSO-E	European Network of Transmission System Operators for Electricity
ES	Electric Spring
EV	Electric Vehicle
ESU	Energy Storage Unit
FPT	First-Passage Time
FPGA	Field-Programmable Gate Array
GFL	Grid-Following

GFM	Grid-Forming
GSL	Grid-Supportive Load
HIL	Hardware-in-the-Loop
HPF	High-Pass Filter
HW	Hardware
IC	Interlink Converter
IEA	International Energy Agency
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
ISO	International Organization for Standardization
KIT	Karlsruhe Institute of Technology
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPC	Model Predictive Control
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
P&O	Perturb and Observe
PCC	Point of Common Coupling
PHIL	Power Hardware-in-the-Loop
PI	Proportional-Integral
PID	Proportional-Integral-Differential
PIL	Processor-in-the-Loop
PLL	Phase-Locked Loop
PV	Photovoltaic
PWM	Pulse-Width Modulation
RCP	Rapid Control Prototyping

RES	Renewable Energy Source
RoCoF	Rate of Change of Frequency
RMS	Root-Mean-Square
S&H	Sample-and-Hold
SESCL	Smart Energy System Control Laboratory
SiC	Silicon Carbide
SoC	State-of-Charge
SoG	State-of-Grid
SoH	State-of-Health
V2G	Vehicle-to-Grid
VSM	Virtual Synchronous Machine
ZIP	Impedance / Current / Power

Notation

$()^*$	Set-point/reference value
$()_e$	Equilibrium point
$\dot{()}$	Time derivative
$\hat{()}$	Estimated/observed value
$\tilde{()}$	Deviation (small-signal quantity)
$\bar{()}$	Dimensionless (normalized) quantity

Latin symbols and variables

C	Capacity

E	Energy
f	Frequency
I	Current
L	Inductance
M	Virtual inertia constant
n	Number (e.g., battery modules)
P	Active power
Q	Reactive power
$Q_{\mathrm{B},i}$	Charge capacity of battery i (in Coulombs or Ampere-hours)
R	Resistance
t	Time
V	Voltage
Z	Impedance

Greek symbols and variables

α, β	Clarke axes
Δ	Difference / step size
λ	Eigenvalue
ϕ	Phase shift
ψ	Restoration weight (activates/deactivates GSL function)
σ	SoG control mapping gain
θ	Phase angle

ω	Angular frequency

Operators and math symbols

∂_x	Partial derivative with respect to x, i.e., $\partial_x f := \frac{\partial f}{\partial x}$
$\dot{x}$	Time derivative of x
$\min(a, b)$	Minimum of a and b
$\max(a, b)$	Maximum of a and b
$\mathrm{sat}_{[a,b]}(x)$	Saturation of x to the interval $[a, b]$, defined as $\max\big(a,\ \min(x, b)\big)$
$\sup A$	Supremum (least upper bound) of the set A, i.e., the smallest number $\geq$ all elements of A
$x \propto y$	x is proportional to y
$f \sim g$	$f(x)$ is asymptotically equivalent to $g(x)$ as $x \to \infty$, i.e., $f(x)/g(x) \to 1$ as $x \to \infty$
$A \subset B$	A is a proper subset of B ($A \subseteq B$ and $A \neq B$)
$a := b$	a is defined as b

General subscript conventions

agg	aggregated
adapt	adaptive
ctrl	control
min	minimal
max	maximal

meas	measured
nom	nominal

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1 Introduction

1.1 Background and Motivation

In response to the growing impacts of climate change and the finite nature of fossil fuel reserves, the large-scale integration of Renewable Energy Sources (RESs) has become a strategic priority across academia, industry, and policy-making institutions [1, 2]. Fossil resources, such as coal, oil, and gas, store solar energy accumulated over geological timescales, but are available only in limited quantities and cannot be replenished within human time horizons [2]. Ongoing reliance on fossil fuels not only reinforces resource scarcity but also poses a significant risk to the long-term security of energy supply for future generations.

While renewables already met $54.4\,\%$ of Germany's electricity demand in 2024, their share of total primary energy[1] amounted to only $22.4\,\%$ [3]. Meeting global climate goals, most notably the Paris Agreement's objective of climate neutrality by 2050 [4, 5], therefore requires a decisive expansion of renewable generation but also a systemic transformation of energy usage across all sectors. This includes the electrification of mobility, heating, and industrial processes, collectively captured by the vision of an all-electric society [6]. Realizing this transformation necessitates not only greater renewable capacity to meet increasing electric demand, such as from electric vehicles and heat pumps, but also

[1] Primary energy includes all energy content before conversion, such as crude oil, sunlight, or wind, and covers electricity, heat, and fuels [3].

innovative concepts to address structural challenges, including the decentralization and diversification of actors (e.g., prosumers and distributed generators) [7].

A promising response to these structural and operational challenges is the deployment of microgrids. First introduced in [8] and defined by CIGRÉ as "*electricity distribution systems containing loads and distributed energy resources (such as generators, storage devices or controllable loads) that can be operated in a controlled, coordinated way either while connected to the main power network or while islanded*" [9], microgrids facilitate coordinated operation of distributed resources.

By the late 19th century, Alternating Current (AC) established itself as the dominant standard for electrical power transmission, primarily due to the relative ease with which its voltage levels could be transformed using transformers [10, 11]. Over the following decades, AC grids have achieved a high level of technological maturity. Their widespread deployment is supported by a globally established infrastructure, inherent compatibility with conventional grid topologies and loads, and robust protection mechanisms, such as residual current circuit breakers and grid protection relays, that ensure reliable and cost-efficient operation [12]. These factors form the foundation for the scalability and continued dominance of AC-based microgrids and distribution systems.

Recent advances in power electronic converters and energy storage technologies have sparked a renewed interest in Direct Current (DC). Modern semiconductor devices and sophisticated control strategies have largely overcome DC's limitations related to voltage transformation and switching [13, 14]. At the same time, an increasing prevalence of decentralized components, such as Photovoltaics (PVs), Battery Energy Storage Systems (BESSs), Electric Vehicles (EVs), and modern electronic loads, operate inherently in DC. Recent advances in power electronic interfaces and the increasing use of DC-native technologies have renewed the interest in DC microgrids as an efficient system architecture [13, 14, 15, 16, 17, 18].

The following list summarizes advantages of DC microgrids as typically reported in the literature [13, 19, 20, 21].

Advantages of DC Microgrids

- **Reduced energy losses and costs**
  By directly connecting sources, storage systems, and loads, DC microgrids eliminate unnecessary power conversion stages. The structural differences in energy conversion paths between AC and DC microgrids are illustrated in Figure 1.1. This improves overall efficiency while reducing both converter investment and long-term maintenance costs.

- **More efficient conductor utilization**
  Unlike AC, DC current flows uniformly across the full conductor cross-section, avoiding the skin effect[2]. In addition, corona losses[3] are reduced due to the constant electric field. Furthermore, as no reactive power flows are required in DC systems, conductor capacity can be fully utilized for active power transmission. Together, these effects can approach up to $150\,\%$ higher ampacity with less material, improving both energetic and economic efficiency.

- **Lower electromagnetic interference**
  Minimizing the number of AC/DC conversions reduces electromagnetic emissions, thereby simplifying interference suppression and enhancing electromagnetic compatibility.

- **Improved integration of electric mobility**
  Supplying EV charging stations directly from DC microgrids simplifies the charging infrastructure by reducing the number of required conversion stages. Beyond efficiency gains, this enables more compact and lightweight charger designs, eases bidirectional energy exchange for

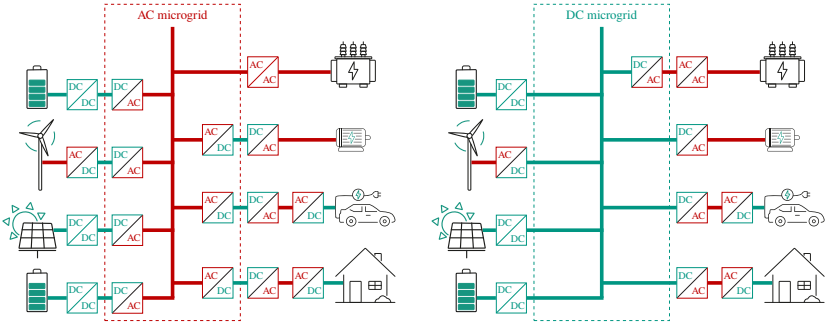
[2] The skin effect refers to the tendency of alternating current to concentrate near the surface of a conductor, effectively reducing the usable cross-sectional area and increasing resistance at higher frequencies [21].

[3] Corona losses arise from the ionization of air around a conductor subjected to a rapidly varying electric field, as in AC systems. In DC systems, the steady electric field leads to significantly lower ionization and energy loss [20].

Vehicle-to-Grid (V2G) applications, and facilitates the large-scale deployment of fast-charging stations. These features make DC microgrids particularly well-suited for supporting widespread e-mobility integration.

- **Simplified energy recuperation**
  Regenerative braking and other forms of energy recovery can be more easily managed in DC systems, since the direct energy flow avoids synchronization issues and allows straightforward reinjection into local storage.

- **Reduced control complexity**
  The absence of frequency dynamics, reactive power flow, and pronounced harmonic distortion in DC systems simplifies control requirements and reduces overall system complexity.



(a) AC microgrid scheme **(b)** DC microgrid scheme

Figure 1.1: Comparison between AC and DC microgrids, illustrating reduced conversion stages in DC systems and their potential benefits for scalable integration of distributed resources.

Challenges and Limitations

Despite their compelling advantages, DC microgrids also present notable challenges that must be addressed before widespread adoption becomes feasible. Key challenges include:

- **Higher requirements for power electronics and control**
  Unlike AC systems, DC microgrids lack natural current zero-crossings, which complicates protection design and fault current interruption. The coordination of power electronic converters requires precise control schemes and often higher controller bandwidths. This can increase the cost and complexity of converter hardware, including larger DC-link capacitors and more sophisticated protection mechanisms [19].

- **Absence of standardized regulations and protection schemes**
  While AC systems benefit from decades of standardization and well-established safety protocols, DC systems still lack harmonized grid codes and universal protection concepts. This regulatory uncertainty can slow down deployment and complicate integration with existing infrastructure [22].

- **Limited compatibility with legacy infrastructure**
  Most existing infrastructure is designed for AC operation. Retrofitting or hybridizing legacy systems for partial or full DC operation can introduce substantial engineering and economic challenges [13].

Beyond these structural and regulatory aspects, DC microgrids must meet core operational requirements: stable regulation of the DC-bus voltage, balanced power sharing among distributed resources, State-of-Charge (SoC) balancing in BESSs, and seamless coupling with AC grids. DC microgrids do not only operate in isolation and can be interconnected with AC grids, forming hybrid AC/DC microgrids. This hybrid structure enables coordinated operation of distributed resources across domains but also introduces specific control challenges that go beyond the individual AC or DC systems. Consequently, control strategies that enable coordinated and cross-domain operation are gaining increasing importance [23]. Throughout this dissertation, the term "DC microgrid" refers to DC-based subsystems that can be physically or functionally connected to AC infrastructure, unless stated otherwise.

At the same time, the ongoing displacement of large-scale synchronous generators, whose rotational inertia contributes significantly to system stability, leads to increased frequency volatility in AC transmission systems [24]. To mitigate the resulting loss of inertia, modern power systems increasingly rely on inverter-based generation and storage units that are capable of providing frequency support functions [25].

With the increasing integration of DC microgrids into AC power systems, their potential to contribute to overall system stability becomes more significant. Addressing this potential requires control approaches that enable stable, efficient, and coordinated operation across AC and DC domains.

Centralized control architectures are based on wide-area communication networks, making them costly to implement and more vulnerable to cyberattacks [26]. As an alternative, decentralized and communication-free strategies avoid these communication-related drawbacks, thereby lowering implementation complexity and enhancing overall reliability [27].

While numerous decentralized and communication-free control strategies have been reported in the literature, they typically address specific control objectives in isolation, such as DC bus voltage regulation, power sharing, SoC balancing, or AC-side frequency support. Approaches that explicitly coordinate these objectives within a unified control framework and simultaneously consider interactions between AC and DC subsystems are less frequently addressed in existing decentralized control concepts, as discussed in Section 2.4.

The present dissertation develops and validates an integrated, communication-free control concept for hybrid AC/DC microgrids. The concept coordinates SoC balancing, voltage regulation, and power sharing across AC and DC subsystems based solely on local measurements. It provides a unified formulation that implements these functions within a single framework and substantiates them through structured stability analysis and experimental validation.

1.2 Research Objectives

To address the previously identified challenges and the associated research gap, this dissertation pursues the following objectives:

1. **Advanced decentralized control methods for DC microgrids:** Design and implementation of decentralized, communication-free control strategies for DC microgrids that ensure accurate voltage regulation, efficient power sharing, and system-wide SoC balancing across both AC- and DC-connected storage systems.

2. **Cooperative interaction strategies between DC and AC microgrids:** Development of novel strategies that enable coordinated energy exchange between DC and AC subsystems. This includes the provision of grid-supportive services, such as frequency support and virtual inertia from DC-connected resources.

3. **Grid-Supportive Loads (GSLs) for enhanced network stability:** Design of decentralized demand-side control mechanisms through which loads contribute to voltage stability and improved dynamic performance in DC microgrids.

4. **Stability analysis of DC microgrids:** Conducting a comprehensive stability analysis that addresses both small-signal disturbances and nonlinear dynamic behavior, with the objective of establishing a theoretical foundation for stable operation under realistic conditions.

5. **Laboratory demonstration for experimental validation:** Design and implementation of a laboratory-scale DC microgrid for realistic validation of the proposed control concepts under practical operating conditions.

1.3 Summary of Scientific Contributions

Based on the objectives outlined above, this dissertation makes the following scientific contributions to the field of decentralized control and stability of hybrid AC/DC microgrids:

1. **Introduction of the State-of-Grid (SoG) concept for decentralized SoC balancing and AC/DC coupling:** This dissertation introduces the SoG concept as a communication-free control framework for autonomous power flow regulation and SoC balancing in DC microgrids. Inspired by the physical principle of communicating vessels, the SoG approach leverages local voltage or frequency deviations to represent the global energy state of the system. This enables self-organizing coordination of distributed BESSs without central control or explicit communication. Furthermore, the method facilitates seamless coupling between DC and AC grids by using small frequency deviations in the AC domain to implicitly signal energy surpluses or deficits. The underlying concepts and experimental validations have been published in [J1] and [J7].

2. **Development and implementation of SoG-based frequency support and virtual inertia:** Building on the SoG concept, a method is developed for frequency-dependent power provision in which the SoC of the DC microgrid directly influences the inertia and frequency support behavior of a Virtual Synchronous Machine (VSM) model. The SoG value is computed in real-time and used to adapt the power reference dynamically. This enables enhanced frequency support during high SoC conditions, while preventing excessive battery discharge under low SoC conditions. The corresponding results have been published in [J2].

3. **Decentralized control of GSL:** A novel control method for so-called GSL is proposed, in which constant Impedance / Current / Power (ZIP)-type loads actively support voltage stability based on local voltage measurements. The control is fully decentralized and operates without any communication infrastructure. By implementing adaptive voltage

references and an energy-aware restoration strategy, the method improves system stability. The corresponding results have been published in [J3], [C3], [C5], and [C7].

4. **Stability analysis of the proposed control strategies:** Comprehensive stability proofs are provided for all proposed control methods, employing both linear and nonlinear analysis techniques. Depending on the system structure, Lyapunov-based methods and Singular Perturbation Theory are applied. The results confirm local and partially semiglobal stability under realistic operating conditions and form the theoretical foundation for robust practical implementation. The corresponding results have been published in [J1].

5. **Experimental validation and structured evaluation methodology in the Smart2DC laboratory:** As part of the present work, the Smart2DC laboratory is established as a real-world DC microgrid test environment. Beyond the testbed itself, a structured and reproducible testing methodology is introduced, including quantitative performance metrics and a consistent scenario design aligned with practical microgrid requirements (Section 5.2). The setup comprises physical power electronic converters, distributed battery systems, and controllable loads, enabling the implementation and validation of all proposed control strategies under realistic power flow conditions. Key functions, such as SoG-based coordination, VSM-based frequency support, and the control of GSLs, are tested in scenarios including load transients, battery plug-and-play events, and PV variability. The results demonstrate the practical feasibility, robustness, and scalability of the proposed methods. The detailed description of the laboratory setup is published in [C8]. All experimental datasets and MATLAB® scripts required to reproduce the figures in Chapter 5 are published in [D1].

Together, these contributions provide a unified and experimentally validated control method for decentralized, communication-free control of hybrid AC/DC microgrids. The developed methods enable power sharing, decentralized SoC

balancing across hybrid AC/DC microgrids, frequency support, and demand-side grid services, while operating entirely without explicit data exchange. By combining theoretical analysis with real-world implementation, this work advances the state-of-the-art in resilient microgrid control.

1.4 Structure of the Dissertation

This dissertation is structured into six chapters. Figure 1.2 provides a thematic overview of the structure and highlights the scientific publications associated with selected sections. The core chapters distinguish between system-level strategies, including SoC balancing and SoG-based coordination, and component-level approaches, such as ancillary services enabled by VSM implementations and GSL control. The vertical flow reflects the logical progression from foundational modeling and theoretical development, through control design and stability analysis, to experimental validation. While the figure does not represent the full chapter hierarchy, it serves as a conceptual map linking the core contributions and their interrelations. Symbols placed next to each content block indicate the type of scientific publication that contributed to the respective section: J for journal articles, C for conference papers, and D for data publications.

Chapter 1 provides the motivation for investigating DC microgrids. It outlines the research problem, defines the specific research objectives, and concludes with a summary of the key scientific contributions of this work.

Chapter 2 provides an overview of the technical background and current state of research relevant to this work. The chapter then introduces essential system components, including BESSs, RESs, and the most commonly used converter topologies, followed by a discussion of system-level aspects such as grid integration and operational coordination. Finally, the chapter critically evaluates existing control approaches with respect to voltage regulation, power sharing,

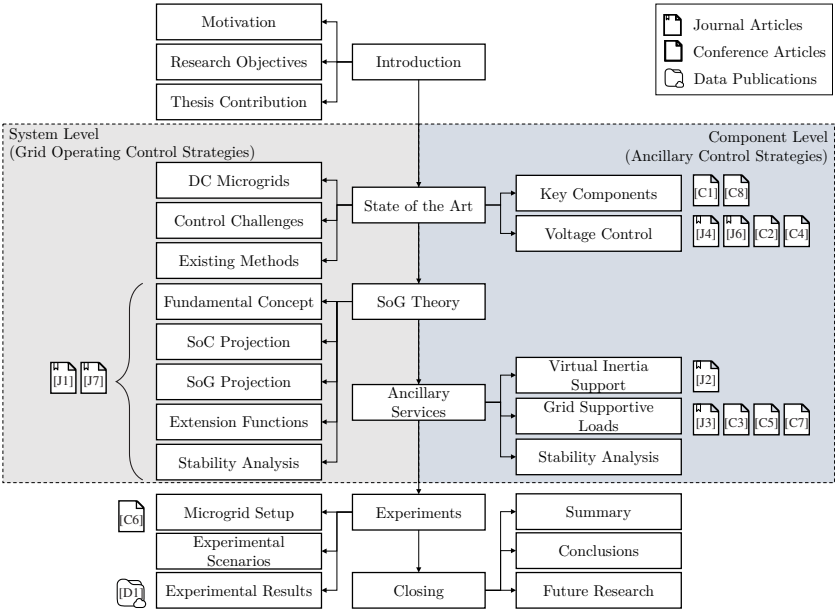


Figure 1.2: Thematic structure of the dissertation and associated scientific publications. The diagram illustrates the logical flow of the work and the core research domains, comprising system-level control strategies (gray), component-level control methods (blue), and experimental validation. It serves as a simplified overview and does not reflect the full chapter hierarchy. The symbols indicate the type of scientific publication (journal, conference, or data) associated with each section.

SoC balancing, and AC–DC interaction, thereby identifying key limitations and open research questions addressed in this dissertation.

Chapter 3 presents the development of a SoG-based control method for autonomous SoC balancing and system-wide energy coordination in and between DC and AC microgrids. The chapter begins by introducing the underlying physical principles and formally derives decentralized SoC and SoG mappings based solely on local voltage or frequency measurements. It then analyzes the control effect within representative system configurations and evaluates the method's stability and scalability. The chapter concludes with practical considerations

regarding tuning parameters, dynamic behavior, and possible extensions of the approach.

Chapter 4 builds on the SoG control method and introduces two advanced strategies to enhance grid support capabilities: a SoG-based VSM for adaptive frequency support in AC microgrids and a decentralized control scheme for GSL that actively contributes to DC voltage stability. The chapter presents the control design of both methods, analyzes their local stability, and discusses their interplay with the overarching SoG concept.

Chapter 5 presents the experimental validation of the proposed control strategies using the Smart2DC laboratory established as part of this dissertation. The chapter outlines the testbed architecture and experimental methodology. It then discusses selected validation scenarios, such as islanded operation, AC/DC coupling, virtual inertia, and demand-side support, to verify the functionality of the decentralized control approaches under realistic conditions. The experimental results are complemented by an evaluation of system performance, focusing on feasibility, stability, and identified limitations.

Finally, Chapter 6 summarizes the contributions of this dissertation, offering critical reflections on the developed control methods in terms of practical implementation and system-level impact. The chapter discusses the methods' relevance to the future low-inertia power systems, identifies current limitations, and highlights promising avenues for further research into the decentralized, communication-free operation of hybrid AC/DC microgrids.

Appendix A provides supplementary material that complements the main chapters. It includes detailed derivations, control diagrams, implementation-related information relevant for reproducibility and technical transparency.

2 Fundamentals and State of the Art

This chapter provides an overview of the theoretical background and selected state-of-the-art concepts relevant to hybrid AC/DC microgrid control, with a particular focus on the background most relevant to the contributions of this dissertation. Section 2.1 introduces the microgrid architecture employed in this dissertation, along with a taxonomic classification of the control approach. This classification defines the conceptual framework within which all subsequent control strategies operate. Section 2.2 then describes the key components of the system. Building on this foundation, Section 2.3 analyzes the principal control challenges specific to DC microgrids, including bus voltage regulation, load sharing, SoC balancing, stability considerations, and the coupling to an AC grid. A critical review of existing approaches is presented in Section 2.4, where current approaches are evaluated in terms of methodology, communication requirements, and structural limitations, thereby identifying remaining research gaps. Finally, Section 2.5 synthesizes the preceding analysis and states the research questions together with the contributions of this dissertation.

2.1 Architectural Concepts and Control Classification in DC Microgrids

The implemented DC microgrid in this dissertation adopts a non-isolated single-bus topology, which is one of the most common configurations for low-voltage systems due to its simplicity and compatibility with commercially available

converter modules [28, 29]. In this structure, all major components, including BESSs, controllable loads, and PVs, as well as the AC grid interface are connected to a common DC-bus via appropriate power electronic converters (e.g., DC/DC, DC/AC), as illustrated in the conceptual architecture shown in Figure 1.1(b). The detailed electrical implementation of this topology is provided in Figure 2.1. A more detailed discussion of the components presented in Figure 2.1 is provided in Section 2.2.

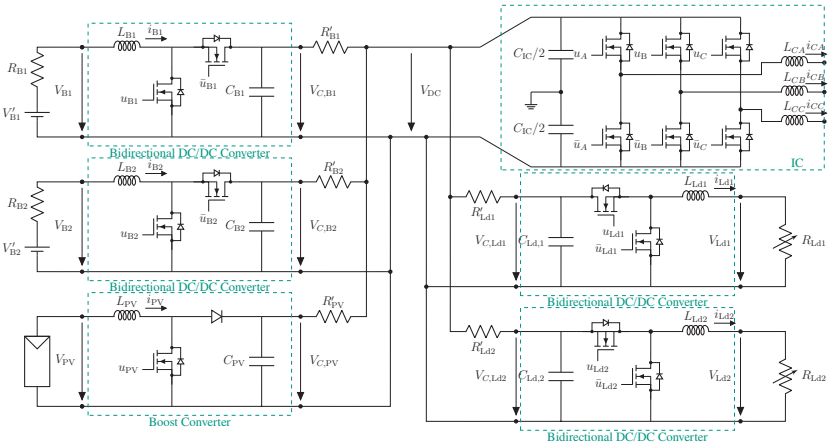
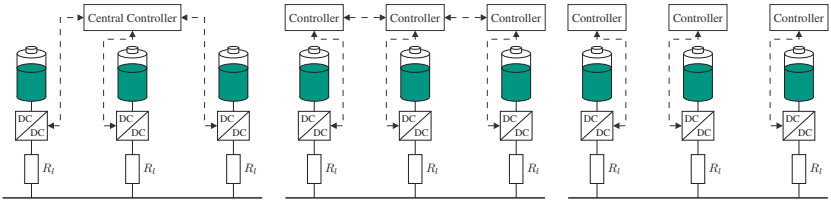


Figure 2.1: Electrical circuit of the experimental DC microgrid setup. The system comprises two BESS units, two controllable loads, a PV generator, and a grid-connected Interlink Converter (IC). All converters are connected to a common DC-bus, forming a non-isolated, bus-based topology used for experimental validation. Adapted from [J1].

Alternative DC microgrid topologies, such as ring, zonal, or multibus configurations, offer higher operational flexibility and fault tolerance by enabling reconfiguration or sectional isolation [28]. These benefits come at the cost of higher complexity in protection coordination and increased hardware requirements. For example, zonal architectures [28] allow for localized fault clearing but require additional switching and control logic. In contrast, the shared-bus

topology adopted in this dissertation represents a compromise favoring implementation simplicity and applicability in compact, low-voltage laboratory environments.

Beyond the physical structure, DC microgrids are often classified by their control architecture as *centralized*, *distributed*, or *decentralized* [30]. These paradigms differ fundamentally with respect to communication requirements, coordination capabilities, and scalability. Figure 2.2 illustrates the associated information flows.



(a) Centralized Control **(b)** Distributed Control **(c)** Decentralized Control

Figure 2.2: Comparison of control architectures in microgrids. (a) Centralized: a single supervisory controller manages all units using global information. (b) Distributed: individual units operate autonomously, coordinated via limited peer-to-peer communication. (c) Decentralized: units act solely based on local measurements, without explicit communication.

In addition to this classification, microgrid control can be interpreted from a hierarchical point of view. Although this structure is originally developed in the context of AC microgrids, it is equally applicable to DC systems. The absence of frequency dynamics in DC grids, however, alters the formulation of certain control tasks. The hierarchy is commonly divided into three levels [31]:

- **Primary control** (local): Ensures voltage and current regulation at the converter level, often implemented via droop control or local Proportional-Integral (PI) loops.
- **Secondary control** (coordinated): Compensates deviations introduced by primary control, such as voltage restoration or current balancing. It typically requires communication and can act across multiple units.

- **Tertiary control** (global): Optimizes power flows and economic dispatch at the system level, including interactions with adjacent grids or upstream utility.

AC-specific aspects of the hierarchical structure and their implications for AC/DC coupling are discussed in Section 2.3.5.

At the converter level, voltage regulation is realized through a cascaded structure with an inner current loop and an outer voltage loop that tracks the reference voltage provided by the SoG controller (see Chapter 3). The general design considerations for voltage control in DC microgrids are discussed in Section 2.4.1, whereas the detailed implementation and tuning of the applied PI control loops are documented in Appendix A.1.

While the physical and control architecture is intentionally simplified to enable a focused validation of the proposed decentralized control methods, the overall setup remains representative of practical low-voltage DC microgrids typically encountered in residential or industrial environments.

2.2 Key Components of the Microgrid

DC microgrids can comprise a wide variety of components, depending on their specific application and design objectives. In this section, the focus is placed on those components that are relevant to the proposed concepts and experimental validation conducted in the scope of this dissertation.

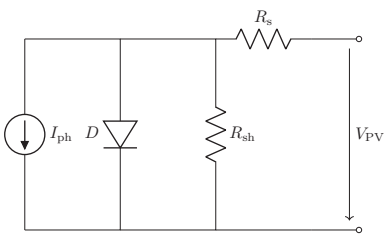
2.2.1 Photovoltaic Systems as Renewable Energy Sources

PV systems are employed in the present dissertation as representative RES, reflecting their growing relevance in low-voltage DC distribution grids. Their high modularity, steadily declining costs, and DC output make them particularly

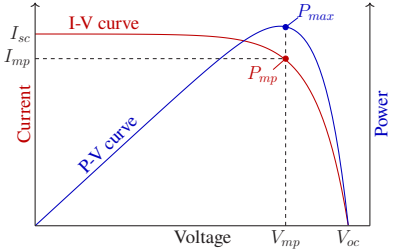
well suited for integration into DC microgrid architectures [32, 33]. The output of a PV module depends on irradiance, temperature, and angle of incidence, making it intrinsically variable and non-dispatchable.

A widely used model to describe the electrical behavior of a PV module is the single-diode equivalent circuit [34], shown in Figure 2.3(a). Due to its nonlinear characteristics, the module exhibits a distinct Maximum Power Point (MPP), which varies with environmental conditions and is illustrated in Figure 2.3(b). To operate near this point, Maximum Power Point Tracking (MPPT) algorithms are employed, typically by adjusting the reference voltage or duty cycle of a DC/DC converter [35, 36, 37].

In this dissertation, a modified Perturb and Observe (P&O) algorithm is employed as the MPPT controller for the PV interface. Details of the algorithm and its implementation are provided in Appendix A.2.



(a) Single-diode equivalent circuit model of a PV module. The photo-generated current I_{ph} flows through the nonlinear p-n junction (diode D) and is affected by parasitic series (R_s) and shunt (R_{sh}) resistances. The model captures the nonlinearity of the I-V behavior under varying environmental conditions.



(b) Current-voltage (I-V) and power-voltage (P-V) characteristics of a PV module. The curves exhibit a distinct maximum power point P_{mp}, defined by the optimal operating voltage V_{mp} and current I_{mp}, which vary with irradiance and temperature.

Figure 2.3: Modeling and characteristic behavior of PV modules. Subfigure (a) shows the single-diode equivalent circuit, while (b) illustrates the corresponding I-V and P-V curves under standard operating conditions.

2.2.2 Battery Energy Storage Systems

BESSs play a vital role in enabling the integration of RESs and enhancing the stability of power systems [38, 39]. Among the various available technologies, BESSs are particularly widespread due to their high efficiency, fast response times, and relatively low cost [40]. Lithium-ion batteries, in particular, have gained increasing importance owing to their rapidly declining capital costs [41]. According to a report by the International Energy Agency (IEA) [42], battery prices fell by approximately $90\,\%$ between 2010 and 2023, significantly improving the economic viability of BESS for grid-scale applications.

In power systems, BESSs fulfill a wide range of functions, including the provision of ancillary services, peak shaving, and support for voltage and frequency regulation. Most notably, they help mitigate the mismatch between generation and consumption by storing surplus energy during periods of high PV generation and releasing it during times of increased demand [43, 44].

In addition to stationary systems, EV batteries offer significant potential for short-term grid support. Through bidirectional charging, also known as V2G, these mobile units can feed energy back into the grid, enhancing flexibility and enabling new forms of ancillary service provision [45].

Recent projections indicate that globally EV batteries will begin to play a substantial role in grid balancing from around 2030 onward [46]. By 2050, the technically available storage capacity of these mobile resources is expected to reach between $32\,\mathrm{TW\,h}$ and $62\,\mathrm{TW\,h}$, surpassing the projected global storage demand of $3.4\,\mathrm{TW\,h}$ to $19.2\,\mathrm{TW\,h}$ [46]. A V2G participation rate between $12\,\%$ and $43\,\%$ would be sufficient to meet this demand. However, realizing this potential at scale will require the implementation of supportive regulatory frameworks and market incentives to promote widespread participation and integration into power system operations [46].

A critical factor in the economic viability of BESSs, whether stationary or vehicle-based, is their long-term cycle life. The key metric used to quantify battery degradation is the State-of-Health (SoH), which reflects the remaining

capacity and performance relative to the original specification [47, 48]. SoH degradation is influenced by multiple operating conditions, including temperature, the number of charge/discharge cycles, the charge rate (C-rate), and the operating range of the SoC [49, 50]. The SoC represents the fraction of usable energy relative to the total capacity and is typically expressed as a percentage. Excessively high or low SoC levels or, equivalently, deep discharges accelerate battery aging and reduce the SoH. Experimental studies have shown that constraining the SoC to a moderate operating window, typically $20\,\%$ to $80\,\%$ for stationary systems and $30\,\%$ to $80\,\%$ for EVs, significantly improves battery lifetime by limiting capacity fade [50]. The control challenges associated with SoC regulation, particularly in multi-battery systems within interconnected microgrids, are discussed in detail in Section 2.3.3 and Section 2.4.3.

In this dissertation, the SoC of each battery is estimated by Coulomb Counting, a widely used method that integrates the charge and discharge currents over time [47, 48]. With the discharge current defined as positive, the estimate reads [51]

$$\mathrm{SoC}_i(t) = \mathrm{SoC}_{0,i} - \frac{1}{Q_{\mathrm{B}i}} \int_{t_0}^{t} i_{\mathrm{B}i}(\tau)\,\mathrm{d}\tau, \qquad t \geq t_0, \tag{2.1}$$

where $\mathrm{SoC}_{0,i}$ denotes the initial SoC, $Q_{\mathrm{B}i}$ is the nominal capacity of battery i, and $i_{\mathrm{B}i}(t)$ is the battery current at time t. This estimate provides the basis for the control and coordination strategies in Section 2.4.3 and Chapter 3.

2.2.3 Electrical Loads and ZIP Representation

Electrical loads are a fundamental component of any microgrid and play a decisive role in shaping system dynamics, power flow, and control requirements. In DC microgrids, a wide range of consumer devices, from household electronics to EV chargers, are typically interfaced through power electronic converters. These interfaces lead to diverse and often voltage-dependent load characteristics, particularly under dynamic conditions.

For control design and system-level simulations, loads are often approximated by constant resistance models due to their simplicity and analytical tractability. In this approach, the instantaneous power demand of each load is assumed to be proportional to the square of its terminal voltage, as expressed by

$$P_{\mathrm{Ld}i} = \frac{V_{\mathrm{Ld}i}^2}{R_{\mathrm{Ld}i}}, \tag{2.2}$$

where $V_{\mathrm{Ld}i}$ denotes the voltage at the terminal of load i, and $R_{\mathrm{Ld}i}$ is its equivalent resistance. While adequate for baseline studies, this formulation neglects more complex voltage sensitivity observed in real-world loads [52].

To capture the voltage dependence of aggregated loads, the ZIP model represents the steady-state active power as an additive combination of a constant-power (P) term, a constant-current (I) term, and constant-impedance (Z) term [52], with

$$P_{\mathrm{Ld}i} = P_{\mathrm{Ld}i}^{\mathrm{nom}} \left(w_{\mathrm{P}} + w_{\mathrm{I}} \frac{V_{\mathrm{Ld}i}}{V_{\mathrm{Ld}i}^{\mathrm{nom}}} + w_{\mathrm{Z}} \left(\frac{V_{\mathrm{Ld}i}}{V_{\mathrm{Ld}i}^{\mathrm{nom}}} \right)^2 \right), \tag{2.3}$$

where $P_{\mathrm{Ld}i}^{\mathrm{nom}}$ denotes the nominal active power of load i at the nominal voltage $V_{\mathrm{Ld}i}^{\mathrm{nom}}$. The coefficients $w_{\mathrm{P}}, w_{\mathrm{I}}, w_{\mathrm{Z}} \in \mathbb{R}$ are weighting factors associated with constant-power (P), constant-current (I), and constant-impedance (Z) behavior, respectively. Imposing $w_{\mathrm{P}} + w_{\mathrm{I}} + w_{\mathrm{Z}} = 1$ normalizes the model such that $P_{\mathrm{Ld}i}(V_{\mathrm{Ld}i}^{\mathrm{nom}}) = P_{\mathrm{Ld}i}^{\mathrm{nom}}$. The ZIP model offers a compact empirical description of how active power varies with voltage in a neighborhood of $V_{\mathrm{Ld}i}^{\mathrm{nom}}$. Outside this range or under fast dynamics, device-specific models may be required.

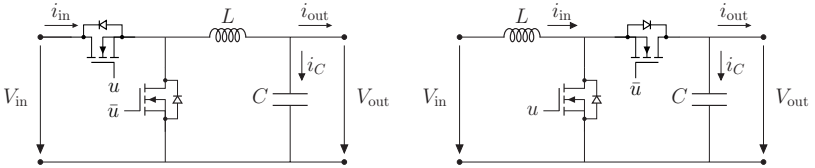
Although the general system model in this dissertation primarily assumes resistive loads as per Equation (2.2), the ZIP formulation is adopted in the context of actively controlled GSLs. These voltage-responsive consumers are designed to dynamically adapt their power consumption based on local measurements and are modeled accordingly in Chapter 4.

2.2.4 Power Electronic Converters as Grid Interface

Power electronic converters form the interface between sources, storage units, loads, and the common bus in microgrids. They enable controlled bidirectional power exchange and couple the AC and DC domains, thereby supporting flexible and modular architectures [53, 54].

This dissertation focuses on two representative units: (i) a non-isolated bidirectional DC/DC half-bridge operated in buck and boost modes and (ii) a three-phase two-level voltage-source converter serving as the IC between the AC and DC grids. The half-bridge is widely adopted due to its structural simplicity, inherent bidirectionality, and suitability for both operating modes [55, 56]; broader overviews of converter families are available in [57, 58].

For tractable analysis, idealized averaged models in Continuous Conduction Mode (CCM) are employed, neglecting switching delays, switching losses, and parasitic elements such as line inductance and capacitance [55, 59]. Averaging over one switching period yields continuous-time state-space models parameterized by the duty cycle $d \in [0, 1]$, which are used for control design and stability analysis [53].



(a) Bidirectional DC–DC converter (buck mode) **(b)** Bidirectional DC–DC converter (boost mode)

Figure 2.4: Circuit topologies of the bidirectional DC–DC converters used in this dissertation. Subfigure (a) illustrates the buck mode, while (b) shows the boost mode. Both modes share the same hardware and are activated depending on the power flow direction.

2.2.4.1 Buck Converter

The DC/DC converter in buck operation reduces the input voltage to a lower output level and is commonly used to supply low-voltage loads in DC microgrids [54, 53]. Under ideal components and CCM, switching-period averaging yields

$$\frac{di_L}{dt} = \frac{1}{L}\left(V_{\text{in}}d - V_{\text{out}}\right), \tag{2.4}$$

$$\frac{dV_{\text{out}}}{dt} = \frac{1}{C}\left(i_L - i_{\text{out}}\right), \tag{2.5}$$

where $d \in [0, 1]$ is the duty cycle, V_{in} and i_{L} denote input voltage and inductor current, V_{out} the output voltage, and i_{out} the load current.

In steady-state and under ideal assumptions, the buck relations are [53]

$$\frac{V_{\text{out}}}{V_{\text{in}}} = d, \qquad I_{\text{out}} = \frac{I_{\text{in}}}{d}. \tag{2.6}$$

In practice, nonidealities and uncertainties (such as parasitics, switching and conduction losses, dead time, and component tolerances) can reduce the accuracy of the averaged model, particularly at low voltage levels. Despite such nonidealities, the buck converter remains a core building block in DC microgrids due to its simplicity and efficiency. In this dissertation it steps the DC-bus down to lower-voltage nodes, with a controller that provides voltage tracking and dynamic current shaping; the design is detailed in Appendix A.1.

2.2.4.2 Boost Converter

The DC/DC converter operating in boost mode, also known as a step-up mode, increases the output voltage above the input level [53]. This functionality is particularly important for energy sources such as BESSs or PV modules, whose terminal voltages often remain below the desired DC-bus voltage.

The averaged state-space model under ideal CCM operation is given by [53]:

$$\frac{di_L}{dt} = \frac{1}{L}\left(V_{\text{in}} - V_{\text{out}}(1-d)\right), \tag{2.7}$$

$$\frac{dV_{\text{out}}}{dt} = \frac{1}{C}\left(i_L(1-d) - i_{\text{out}}\right), \tag{2.8}$$

where i_L denotes the inductor current, and $d \in [0,1]$ the duty cycle, V_{in} the input voltage, V_{out} the output voltage, and i_{out} denotes the output current.

The corresponding steady-state conversion ratios are [53]:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{1-d}, \qquad I_{\text{out}} = I_{\text{in}}(1-d). \tag{2.9}$$

While the theoretical gain becomes unbounded as $d \to 1$, practical implementations are constrained by non-ideal effects. In particular boost inductor resistance impose an upper bound on the conversion ratio. Operating near this limit leads to elevated current stress, increased conduction losses, and thermal challenges [54, 56]. As a result, practical voltage gains range between one and five. In this dissertation, the voltage levels are selected such that the required boost ratio remains below two. These models are well established in the literature [53, 56] and serve as a foundational framework for developing control strategies that enhance the converter's dynamic behavior. The cascaded control architecture implemented in this dissertation is described in detail in Appendix A.1.

2.2.4.3 Three-Phase Two-Level Interlink Converter

To enable controlled energy exchange between the DC microgrid and the AC utility grid, a conventional three-phase two-level converter is employed as the IC. This topology is widely adopted in hybrid AC/DC systems due to its maturity and inherent bidirectional power capability [53, 60].

The converter consists of three half-bridge legs connected to a split DC-link, as illustrated in Figure 2.5. Two series-connected capacitors establish a midpoint potential, which is grounded to reduce common-mode voltage and improve electromagnetic compatibility [61, 62]. Each phase leg includes two actively controlled switches, enabling Pulse-Width Modulation (PWM) for precise control of the converter output voltages.

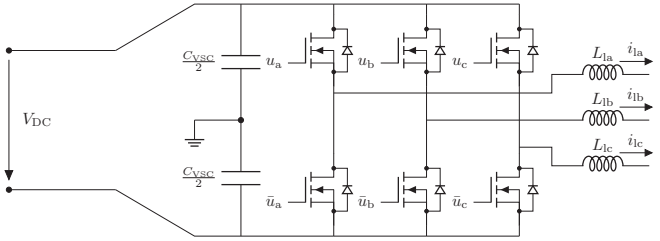


Figure 2.5: Three-phase two-level interlink converter topology. The converter consists of six Silicon Carbide (SiC)-based switching legs with antiparallel diodes, connected to a split DC-link capacitor C_{VSC}. Each phase is interfaced with the AC grid via an output inductor L_i. This topology is used for active power exchange and AC grid support in hybrid microgrid systems.

This converter serves as the central interface for coupling the AC and DC domains throughout this dissertation. Its control design is discussed in Section 2.4.4. The underlying modeling approach based on dq transformation is detailed in Appendix A.3, while the complete control structure is presented in Appendix A.5.

2.3 Control Challenges in DC Microgrids

Building on the motivation presented in Section 1.1, this chapter identifies the fundamental control challenges arising from decentralized, communication-free DC microgrid operation. These challenges form the basis for the systematic review in Section 2.4, where existing solutions are assessed against these requirements.

2.3.1 Voltage Control

Although voltage control is not the main focus of this dissertation, it forms a critical prerequisite for the higher-level SoG scheme introduced in Chapter 3. A stable DC-bus voltage is essential to ensure power-quality compliance and functions as the global error signal for active power imbalances in DC microgrids. Unlike conventional AC grids[1], where the mechanical inertia of synchronous machines mitigates the immediate impact of active power imbalances, DC systems lack inherent kinetic energy. Their transient energy buffer is confined to the capacitances connected to the common DC-link. Due to practical constraints on the physical size and cost of the capacitor bank, its energy storage capacity is inherently limited. As a result, even small mismatches between generation and demand can lead to rapid voltage excursions [63].

To ensure dynamic voltage stability, decentralized power-electronic converters must therefore be equipped with high-bandwidth controllers capable of restoring the bus voltage within milliseconds. Without such fast and well-tuned voltage control, the system can experience pronounced oscillations, disproportionate converter loading, and potentially destabilizing interactions, especially in systems with multiple parallel units operating without coordinated impedance shaping [64].

The proposed supervisory control layer relies on the assumption that each converter tracks its local voltage reference V^* at least an order of magnitude faster than the SoG algorithm updates those references. Violating this timescale separation would invalidate the theoretical assumptions underpinning the stability and optimality of the proposed approach [60].

Complementary to the main contributions of this dissertation, additional research was conducted on advanced voltage control strategies, resulting in four peer-reviewed publications ([C2], [C4], [J4], [J6]). These works demonstrate

[1] This statement refers to conventional AC power systems with substantial synchronous inertia. The particular case of low-inertia AC microgrids is addressed in Section 2.3.5.

the feasibility of decentralized, communication-free control concepts for voltage regulation in DC microgrids.

An overview of representative control strategies is provided in Section 2.4.1, with references to the aforementioned publications for further details. The specific controller used in the experimental validation presented in Chapter 5 is described in Appendix A.1.

In summary, reliable voltage control is indispensable for the proposed higher-level schemes. It ensures stable system operation under dynamic conditions and provides the basis for supervisory coordination in communication-free microgrid architectures.

2.3.2 Power Sharing

Coordinated power sharing among distributed energy resources is fundamental to the reliable operation of DC microgrids. In its classical sense, power sharing refers to the instantaneous distribution of load demand among parallel units, typically realized through droop control based on the common bus voltage. Under ideal conditions, this mechanism ensures proportional current contributions. In practice, however, line resistances and parameter mismatches distort the voltage profile and lead to imbalances in the shared currents [65].

Beyond the instantaneous perspective, it is also relevant how the average power contribution evolves over extended horizons. Especially in the case of BESSs, an unequal cumulative power allocation results in diverging SoC trajectories. This motivates the concept of SoC balancing, which can be understood as the long-term extension of power sharing. Instead of focusing on momentary currents alone, SoC balancing adjusts the average power allocation over time to ensure fairness and to preserve the availability of all BESS units.

Recent research has therefore proposed control strategies that retain the decentralized and communication-free nature of droop control while integrating

local SoC information. Such energy-aware approaches enhance storage utilization, support autonomous operation during islanding, and mitigate long-term degradation [66].

The subsequent section further examines the need for advanced SoC balancing control mechanisms.

2.3.3 State-of-Charge Balancing

Maintaining balanced SoC levels across all BESS units is critical for ensuring operational flexibility, maximizing usable capacity, and reducing degradation. Imbalances can arise from a variety of sources, including unequal initial conditions, asymmetric loading, component tolerances, and uncoordinated control actions [67].

An unbalanced SoC distribution can lead to significant reductions in effective storage capacity and dynamic response capabilities of the microgrid. When some BESSs reach their upper SoC limits, they can no longer absorb excess power, particularly during periods of surplus renewable generation, resulting in curtailment and inefficient resource utilization. Conversely, when certain units approach deep discharge, they can no longer contribute to supply loads. Even if other BESSs retain sufficient energy, the total deliverable power of the system is limited by the individual power ratings and current constraints of the remaining units. As a result, the system can become unable to meet demand, not due to a lack of energy per se, but due to the uneven SoC distribution and associated converter limitations [68].

This situation is exemplified in Figure 2.6, which illustrates a decentralized urban DC microgrid with spatially distributed BESSs exhibiting heterogeneous SoC levels. Although sufficient energy is available in the system, unbalanced utilization can result in operational constraints and limit system responsiveness.

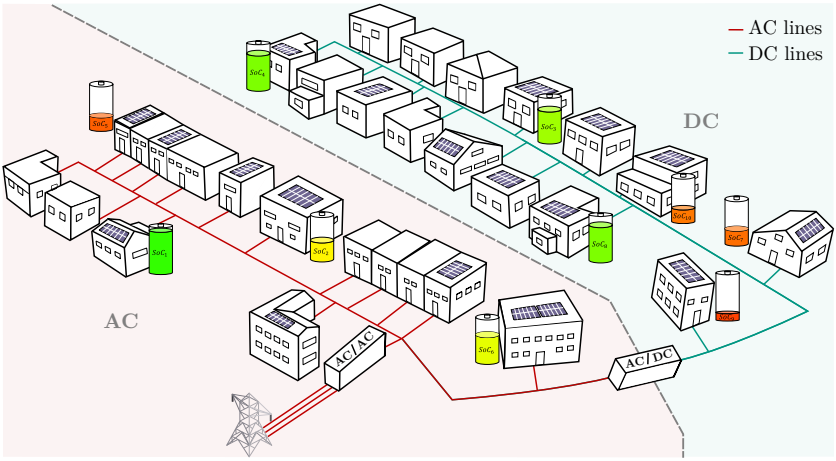


Figure 2.6: Conceptual representation of an urban hybrid AC/DC microgrid with spatially distributed storage systems. The diagram illustrates a heterogeneous BESS landscape with varying SoCs, connected via AC (red) and DC (green) distribution lines.

Beyond these immediate performance issues, SoC imbalance also accelerates long-term degradation of the BESSs. Units that remain at high SoC levels for extended periods, or are exposed to disproportionate charge-discharge cycling, experience elevated thermal and electrochemical stress [69]. This contributes to asymmetric aging, reduced energy throughput, and premature capacity loss. As an illustrative case, early-day charging during periods of high solar irradiance can cause BESSs to remain close to full SoC for extended durations, accelerating aging mechanisms. Predictive control strategies that shift charging toward late afternoon hours, based on solar forecasts and load profiles, have been shown to mitigate such degradation mechanisms and extend battery lifetime [69].

From a control perspective, addressing SoC imbalance in decentralized microgrids is particularly challenging. Classical droop-based power sharing mechanisms allocate current based on local voltage deviations but are inherently blind to the energy state of individual units. Consequently, units with low SoC can continue to discharge, while those with higher reserves remain underutilized. To overcome this, SoC-aware power modulation strategies have been

proposed [66]. These approaches dynamically adjust the power contribution of each unit based on its internal energy level, thereby promoting equitable utilization and guiding the system toward a balanced SoC distribution, without requiring centralized coordination or real-time communication. A comprehensive overview and classification of such SoC balancing methods is provided in Section 2.4.3.

2.3.4 Stability Analysis

To ensure dependable operation of the proposed control strategies, a mathematical stability analysis is essential. In line with the IEEE PES Task Force on Microgrid Stability Definitions, Analysis, and Modeling [70], stability in microgrids is defined as the system's ability to return to a stationary or quasi-stationary operating point after a disturbance (e.g., sudden load change, short circuit, or generator outage), while ensuring that all relevant variables, such as voltage, current, and frequency, remain within acceptable limits and without triggering unintended load shedding or generator disconnections.

In the context of DC microgrids, the concept of stability extends beyond classical interpretations found in large-scale AC systems, as it must address the distinct characteristics of converter-based operation and limited inertia. Stability analysis becomes particularly challenging in decentralized systems, where local controllers interact without centralized coordination [71].

To capture the diverse nature of such disturbances and system responses, the literature distinguishes between several dimensions of stability [60, 70, 72]:

- **Supply and Power Balance Stability** refers to the ability of the system to maintain a feasible power flow equilibrium and meet demand despite changes in generation or topology. It encompasses coordinated power sharing, load matching, and controlled shedding where needed.
- **Control System Stability** refers to the ability of local control loops to ensure stable, convergent system behavior under parameter variations, disturbances,

or inter-unit interactions. Inadequate or overly aggressive controller tuning can lead to instability, particularly in tightly coupled microgrids.

- **Small- vs. Large-Signal Stability** distinguishes between local and nonlinear system behavior. Small-signal analysis is concerned with the local response around a nominal operating point and is typically addressed via linearization and eigenvalue analysis. While efficient, this method only guarantees stability in a neighborhood of the equilibrium. Large-signal stability, in contrast, considers nonlinear system dynamics under more severe disturbances and is often assessed using Lyapunov's direct method [72].
- **Short- vs. Long-Term Stability** differentiates between fast and slow dynamics. Short-term stability concerns events over milliseconds to seconds, typically governed by converter controls and rapid load fluctuations. Long-term stability involves slower phenomena such as thermal effects, battery degradation, and energy storage dynamics, which unfold over minutes to hours and must be addressed in system-level planning and energy management.

A graphical overview of this classification, adapted from [70], is provided in Figure 2.7.

In this dissertation, the stability of the proposed control strategies is rigorously assessed using well-established analytical methods. Section 3.5 employs Lyapunov-based techniques and Singular Perturbation Theory to evaluate the global system behavior under bounded disturbances. In addition, small-signal stability is investigated in Section 4.2 through linearization and eigenvalue analysis around representative operating points.

2.3.5 Integration and Interaction with AC Grids

The integration of DC microgrids into existing AC power systems presents not only a complex technical challenge, but also a significant opportunity for enhancing grid flexibility, resilience, and sustainability. This section outlines the

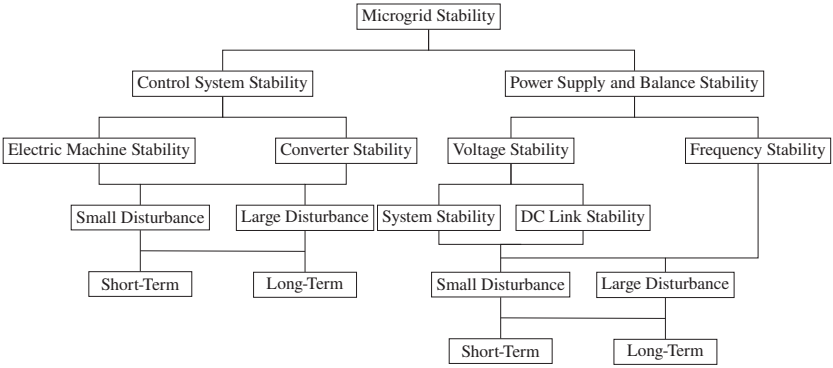


Figure 2.7: Overview of microgrid stability categories as proposed in [70]. The classification distinguishes between control system stability and power supply and balance stability, further subdivided into electric machine, converter, voltage, frequency, and DC-link stability. Each category can be analyzed under small- and large-signal disturbances and in short- or long-term time frames.

fundamental principles and key integration challenges associated with AC/DC coupling, thereby laying the foundation for the IC control strategy discussed in Section 2.4.4.

In conventional AC power systems, the inertia of synchronous generators provides an instantaneous reserve of kinetic energy that inherently buffers short-term active power imbalances. A sudden increase in demand, for example, is initially supplied by this kinetic store, causing the rotor speed and thus the grid frequency to decline [73, 74]. The dynamic frequency response of a synchronous generator can be described by the swing equation, which relates the net accelerating power to the rate of change of rotor speed [75]:

$$J\,\omega_g\,\frac{d\omega_g}{dt} = P_{\mathrm{E}} - P_{\mathrm{L}}, \tag{2.10}$$

where P_{E} denotes the generated electrical power, P_{L} the instantaneous load demand, J the moment of inertia, and ω_g the rotor angular velocity, which is directly proportional to the grid frequency. This equation can be obtained by differentiating the kinetic energy stored in the rotating masses, $E_k = \frac{1}{2}J\omega_g^2$, by differentiating with respect to time.

To account for frequency-sensitive demand and other damping effects, a linear term can be included, yielding the damped swing equation:

$$J\,\omega_g \frac{d\omega_g}{dt} = P_{\mathrm{E}} - P_{\mathrm{L}} - D_f\big(\omega_g - \omega^*\big), \tag{2.11}$$

with effective damping coefficient $D_f > 0$ and nominal angular frequency ω^*.

Frequency control in power systems is structured across multiple temporally layered stages, each designed to counteract imbalances between generation and demand over different time scales. These stages range from the immediate physical response of synchronous inertia to slower, economically optimized redispatch measures. The overall structure of this frequency response is schematically illustrated in Figure 2.8, as defined by the European Network of Transmission System Operators for Electricity (ENTSO-E) [76]. The main stages are:

- **Inertial Response:** The instantaneous power exchange between synchronous machines and the grid that occurs immediately after an active power imbalance. It originates from the kinetic energy stored in the rotating masses of synchronous generators, which is governed by the swing equation (see Equation (2.11)).
- **Primary Frequency Control:** Within approximately up to $30\,\mathrm{s}$, generators begin to actively adjust their output in proportion to the frequency deviation. This autonomous response helps stabilize the frequency without centralized coordination.
- **Secondary Frequency Control:** This stage, also known as Automatic Generation Control (AGC), restores the nominal frequency and power balance through centralized adjustments. It typically operates on a time scale of $30\,\mathrm{s}$ to $15\,\mathrm{min}$.
- **Tertiary Frequency Control:** Acting beyond 15 minutes, tertiary control replaces secondary reserves and optimizes power dispatch based on economic and operational considerations.

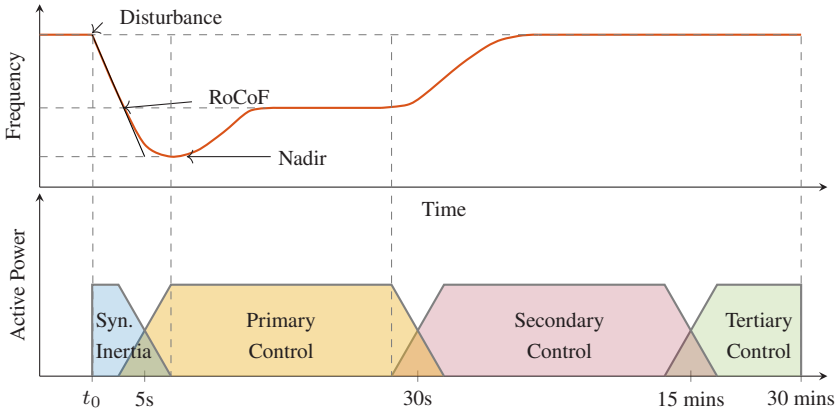


Figure 2.8: Schematic representation of frequency response stages in power systems following a disturbance, based on the ENTSO-E classification [76]. The illustration highlights the sequential activation of system inertia, primary control, secondary control, and tertiary control to restore frequency and active power balance.

A reduction in system inertia leads to higher values of the Rate of Change of Frequency (RoCoF)[2], thereby narrowing the time window available for primary and secondary control actions [77]. These challenges are further exacerbated by the displacement of conventional synchronous generators with inverter-based resources such as wind turbines and PVs, which contribute little or no rotational inertia [78, 79]. The widespread blackout in the United Kingdom on 9 August 2019 is an example of the vulnerabilities introduced by low-inertia operation [80, 81].

To counteract this challenge, a variety of control concepts, commonly grouped under the term of virtual or synthetic inertia, has been developed. They emulate the instantaneous energy exchange of synchronous machines through coordinated control of power electronic converters and their associated energy sources.

[2] RoCoF is defined as the time derivative of grid frequency and serves as an indicator of how quickly the frequency deviates from its nominal value following a disturbance. High RoCoF values imply lower system inertia and faster frequency dynamics, which can pose stability and protection challenges.

The fundamental principles and practical implementations of such converter-based inertia emulation are discussed in Section 2.4.4. Key contributions and representative implementations of these IC functions are documented in the literature [82, 83, 84, 85, 86].

2.3.6 Grid-Supportive Loads

The increasing integration of variable RESs, such as PV and wind power, has led to a growing demand for flexibility in modern power systems. Conventional flexibility solutions, primarily based on energy storage technologies, face inherent limitations in terms of economic viability, scalability, and sustainability, particularly within low-inertia and distribution-level grids. In response, recent research efforts have increasingly focused on the integration of GSL as a complementary flexibility resource [87].

Unlike conventional passive loads, GSLs are equipped with embedded control algorithms that dynamically adjust their power consumption in response to real-time measurements of local and system-wide states. Through coordinated setpoint modulation, GSLs actively support grid stability, reduce the reliance on centralized energy storage, and improve the system's ability to mitigate disturbances. This functionality is particularly valuable in low-inertia DC grids, where voltage deviations can propagate rapidly and simultaneously affect multiple converters. In such environments, the distributed and fast-reacting nature of GSL control offers a robust and scalable approach that enhances system resilience.

A compelling demonstration of the potential of GSLs is presented in [87]. Within a large-scale 2000-bus test system, the integration of only $20\,\%$ grid-supportive demand enabled an additional frequency support capacity of up to $2000\,\mathrm{MW}/0.1\,\mathrm{Hz}$, without requiring any frequency regulation contributions from wind or solar generators. As a result, the frequency nadir deviation is reduced by almost $60\,\%$ compared to a reference scenario without GSL integration. These findings highlight that such loads can not only respond effectively

to both voltage sags and frequency excursions in a balanced manner but also provide substantial ancillary services to the grid.

2.4 Overview of Existing Control Approaches

Building on the challenges outlined in Section 2.3, this chapter surveys the control strategies proposed to address them. In accordance with the research objectives stated in Section 1.2, the discussion is deliberately confined to decentralized and communication-free approaches.

2.4.1 Voltage Control Methods

As outlined in Section 2.3.1, local voltage control forms the high-bandwidth inner control layer in the hierarchical structure considered in this dissertation. Its primary task is to ensure that each converter maintains its output voltage V aligned with the reference V^* provided by the higher-level SoG controller described in Chapter 3.

A comprehensive review of voltage control techniques for DC microgrids is beyond the scope of this dissertation, as such methods are extensively covered in existing literature (e.g., [88, 89, 90]). The following discussion therefore focuses on representative approaches developed and validated within the scope of this research, which serve as enabling mechanisms for the higher-level control concepts proposed in this dissertation.

Several advanced voltage control strategies have been developed and experimentally validated in the context of this research. These approaches, documented in [C2] [C4], [J4] and [J6] include:

- A nonlinear distributed control method for multi-terminal DC microgrids, experimentally validated using a Power Hardware-in-the-Loop (PHIL)

platform and shown to outperform conventional PI-based approaches in dynamic scenarios [C2].

- An extended nonlinear control framework for AC-coupled DC microgrids integrating grid support functionality, which also includes advanced DC-bus voltage regulation under multiple converter interactions [C4].
- A Linear-Active Disturbance Rejection Control (L-ADRC) strategy for buck and boost converters, designed to operate under matched and mismatched disturbances and validated through DC microgrid Hardware (HW) testing [J4].
- A Nonlinear-Active Disturbance Rejection Control (NL-ADRC) combining sliding mode observation and Lyapunov-based feedback, capable of achieving robust voltage control in converters with non-minimum phase characteristics [J6].

These advanced control strategies confirm the feasibility of decentralized and communication-free voltage regulation with high dynamic performance. However, for the experimental validation of the higher-level control concepts presented in Chapter 3, the objective was not to benchmark voltage control algorithms but to verify the system-level functionality under realistic laboratory conditions. For this purpose, a classical cascaded voltage-current control with feedforward compensation and clamping anti-windup is selected, owing to its proven robustness, ease of implementation, and widespread adoption in industry. This choice ensures that the observed system behavior can be directly attributed to the proposed higher-level control mechanisms rather than to specific characteristics of advanced local controllers. The detailed design and tuning procedures are provided in Appendix A.1.

2.4.2 Droop Control as a Basis for Power Sharing

Power-sharing schemes in DC microgrids can broadly be classified into voltage-based droop methods, current-based strategies, and hybrid approaches that combine multiple control principles or integrate local state estimation. Among these, voltage-based droop control remains the most widely adopted primary layer due to its simplicity, plug-and-play capability, and independence from communication [91]. In its conventional form, it emulates a resistive voltage source according to

$$V_i = V_i^* - R_{\mathrm{d},i}\, I_i, \tag{2.12}$$

where V_i is the output voltage of BESS unit i, V_i^* the nominal DC-bus voltage, I_i the output current, and $R_{\mathrm{d},i}$ the virtual droop resistance. A smaller droop coefficient $R_{\mathrm{d},i}$ results in a higher output voltage for a given current, thereby increasing the unit's share in supplying the load, whereas a larger coefficient reduces its participation.

While attractive for its robustness and scalability, conventional droop control is sensitive to line impedances, converter parameter variations, and other non-idealities [92, 93]. More critically for microgrids comprising multiple BESSs, it does not consider the SoC of individual units. As a result, low SoC units can be forced to deliver the same current as fully charged units, causing uneven capacity utilization, accelerated degradation, and potentially premature system shutdown despite significant remaining energy elsewhere. These shortcomings motivate the development of SoC-aware droop methods, which adjust the power contribution of each unit according to its energy status. The following section reviews representative SoC balancing approaches.

2.4.3 SoC Balancing Control

Recent research has proposed a wide range of methods for balancing the SoC among BESSs in DC microgrids. The primary objective of these strategies is to ensure uniform utilization of the available storage capacity, thereby improving

operational efficiency and extending system lifetime. The comprehensive review by Fagundes *et al.* [66] classifies existing approaches into three main categories: centralized, distributed, and decentralized control methodologies. As outlined in Section 2.1, this dissertation focuses on decentralized strategies.

In [94], the droop coefficient is locally adjusted as a function of the SoC, with the aim of assigning higher power contributions to storage units with higher SoC levels, while relieving those with lower SoC. This approach promotes gradual equalization of SoC values over time. However, line resistances and heterogeneous BESS capacities are not considered.

The approach proposed in [95] extends the SoC-based droop control concept introduced in [94] by implementing a dual-quadrant strategy for distributed energy storage systems in DC microgrids. Unlike [94], which considers only discharging behavior, the extended method differentiates between charging and discharging modes. During charging, the droop coefficient is chosen to be proportional to the n-th power of the SoC, whereas during discharging it is set inversely proportional to the SoC. Here, the parameter n serves as a convergence factor.

In [96], a fuzzy logic-based droop control scheme is introduced to achieve SoC balancing among distributed BESSs in a DC microgrid. The method adaptively adjusts the virtual resistances of each unit without requiring centralized communication. However, differences in line resistance and storage capacity are not addressed.

In [97], a decentralized generation-storage coordination strategy is proposed for islanded DC microgrids with high PV penetration. The storage control relies on an SoC-dependent droop mechanism that not only facilitates power sharing but also adaptively adjusts the DC-bus voltage to prevent overcharging and deep discharging of the BESSs. In addition, a power-adaptive control scheme is introduced for the PV generators, which limits their power injection based on the DC-bus voltage when the storage units approach high SoC levels. This approach enables coordinated operation between generation and storage without requiring centralized control.

In [98], the conventional SoC-based droop control is extended by incorporating the relative capacity of individual battery units. The droop coefficient is set proportional to a power function of the SoC, and an additional capacity weighting factor is introduced. This ensures that storage units with higher capacity contribute more power, while enabling a more effective SoC balancing among BESSs with heterogeneous capacities.

In [99], a fully filter-based decentralized SoC balancing strategy is presented. The approach combines a High-Pass Filter (HPF)-based SoC balancing mechanism with a Band-Pass Filter (BPF)-based droop control scheme. The HPF-based component optimizes power sharing based on the SoC and capacity of each unit, while the BPF compensates for voltage deviations to ensure stable current distribution. Line resistances are explicitly taken into account to mitigate their impact on voltage regulation and SoC balancing. The proposed method is validated through Processor-in-the-Loop (PIL) simulations and demonstrates improved voltage stability and faster SoC convergence compared to conventional droop-based approaches.

In [100], a hardware-validated SoC-aware droop control method is proposed, in which the droop characteristic is vertically shifted as a function of the local SoC while maintaining a fixed slope. This mechanism reduces the power contribution of units with higher SoC and increases it for units with lower SoC, thereby promoting charge equalization without requiring communication. The method assumes equal line resistances and identical battery capacities, and does not consider heterogeneous grid conditions, grid-supportive load functionalities, or operation in hybrid AC/DC systems.

A communication-less hybrid AC/DC equalization concept is presented in [101]. One Energy Storage Unit (ESU) is designated as a sender unit whose SoC acts as reference for the others. The sender reports its SoC to all units by superimposing a small AC current on the DC-bus, which the remaining ESUs sense and then shift their droop curves relative to the sender's SoC. This power-line signaling avoids a digital data link but still relies on an explicit auxiliary signaling mechanism and a special sender role. The method targets hybrid AC/DC operation

but does not provide a unified metric that intrinsically links DC-bus voltage deviations and AC-frequency deviations for cross-domain SoC balancing, nor does it explicitly address heterogeneous line resistances or capacity spreads.

In [102], an SoC-aware droop scheme treats the BESS units as master regulators of the DC-bus. The reference voltage is held constant within a nominal SoC band and adjusted only at low or high SoC, which bounds DC-bus excursions. The droop slope is scheduled by the local SoC to equalize heterogeneous BESSs. Interaction with PV and the utility grid is coordinated via DC-bus signaling, where predefined voltage thresholds trigger rule-based mode changes such as grid injection or absorption. Consequently, coordination relies on discrete DC-Bus Signaling (DBS) threshold events on the DC side, with system behavior inferred from bus-voltage excursions rather than from a continuous cross-domain coupling variable.

Patent [103] likewise modulates output current by vertically shifting the droop characteristic according to SoC at fixed slope in order to promote self-balanced charge distribution without communication. As a result, units with higher SoC increase their power contribution, whereas those with lower SoC decrease theirs, promoting self-balanced charge distribution without requiring communication.

In contrast to the approaches discussed above, this dissertation develops a SoG-based framework that coordinates BESSs, the IC, and GSLs using only local measurements. Without communication, the method achieves (i) SoC-aware power sharing within the DC domain, (ii) cross-domain SoC balancing across AC and DC subsystems via the IC, and (iii) concurrent frequency support with virtual inertia on the AC side. The design explicitly accounts for heterogeneous storage capacities and non-ideal line resistances, and embeds voltage-sensitive response curves for GSLs as part of the primary layer. Beyond small-signal analysis, stability is established using Lyapunov and input-to-state stability arguments as well as Singular Perturbation Theory. The concept is validated under representative scenarios in the Smart2DC laboratory (see Chapter 3 and Chapter 5).

A comparative summary of relevant approaches is provided in Table 2.1, which contrasts key characteristics such as tolerance to variable line resistances (ΔR_L), operation with heterogeneous battery capacities, capability for GSL, synergistic AC coupling (S-AC), and cross-domain SoC balancing between DC and AC subsystems. The table also reports the employed validation method, which ranges from simulation to Hardware-in-the-Loop (HIL) and full hardware experiments.

Table 2.1: State of the Art Comparison

Reference	ΔR_L	unequal BESS	GSL	S-AC	DC-AC SoC Bal.	Validation
[94, 100]	×	×	×	×	×	HW
[96]	×	×	×	×	×	HIL
[95]	×	×	×	×	×	Sim
[97]	✓	✓	×	×	×	HIL
[98]	×	✓	×	×	×	Sim
[99]	✓	✓	×	×	×	PIL
[101]	×	×	×	✓	✓	Sim
[102]	×	✓	×	✓	×	HIL
[104]	×	✓	×	×	×	HIL
[105]	✓	×	×	✓	×	HW
This Thesis	✓	✓	✓	✓	✓	HW

Abbreviation: ΔR_L: Variable line resistances; unequal BESS: Heterogeneous battery capacities; GSL: Grid-Supportive Load capabilities; S-AC: Synergistic AC coupling; DC-AC SoC Bal.: State of Charge (SoC) balancing across DC and AC domains; ✓: Presence of feature; ×: Absence of feature.

The SoC-aware strategies reviewed above enable communication-free, decentralized coordination of BESSs in DC microgrids and improve charge balance, operational efficiency, and lifetime. Their effectiveness is, however, inherently

limited to the DC domain. In practice, many microgrids interface with AC infrastructure as part of hybrid AC/DC systems, where seamless energy exchange and coordinated cross-domain SoC balancing become essential. The following chapter therefore examines AC coupling techniques that enable robust and synergistic integration of DC microgrids into broader power-system architectures.

2.4.4 AC Coupling Control Techniques

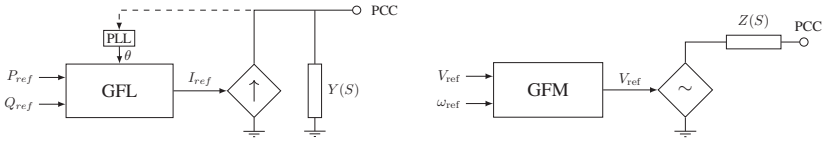
As discussed in Section 2.3.5, the transition from synchronous generators to power-electronic-interfaced resources reduces the inherent rotational inertia of conventional AC systems. The resulting change in system dynamics poses challenges for frequency and voltage stability [106, 107, 75]. To mitigate these effects, virtual or synthetic inertia concepts emulate inertial response through the control of power electronic converters and their energy sources, thereby providing a stabilizing effect comparable to that of rotating masses [108].

A prominent implementation is the VSM. By embedding virtual inertia, damping, and voltage control, VSMs mimic the dynamic behavior of synchronous generators and enable inverter-based resources to contribute to frequency and voltage stability in AC grids [109, 110, 111, 112]. The present subsection introduces the principles and modeling of VSM systems as a basis for the SoG-based VSM strategy in Section 4.1. Comprehensive reviews of virtual-inertia control methods are available in [109, 113, 114, 111, 115, 112].

2.4.4.1 Grid-Following and Grid-Forming Control

To overcome limitations of Grid-Following (GFL) operation, Grid-Forming (GFM) control has emerged as a promising alternative [116, 117]. In GFM mode, converters establish voltage and frequency internally, which enables much faster responses to grid disturbances than GFL operation. The fundamental difference between GFL and GFM control paradigms is illustrated in Figure 2.9. While GFL inverters regulate output current in response to the

estimated grid frequency at the Point of Common Coupling (PCC), typically synchronized via a Phase-Locked Loop (PLL), GFM inverters actively generate a terminal voltage with defined amplitude and frequency, thereby taking a grid-forming role. In the following, the control strategies relevant to this study are introduced, namely droop control (in GFL) and the VSM (in GFM).



(a) Grid-following control (schematic). **(b)** Grid-forming control (schematic).

Figure 2.9: Conceptual comparison of GFL and GFM control paradigms. (a) GFL: synchronization via PLL with outer active/reactive power or DC-link controllers that provide current references to an inner current loop (current-source behavior). (b) GFM: generation of internal voltage, frequency, and angle references (droop, virtual oscillator, or VSM) with voltage control, virtual impedance, and current limiting (voltage-source behavior). Adapted from [117].

2.4.4.2 Droop-Based Control Approaches

Conventional frequency control for converter-interfaced generation typically operates in GFL mode. A static droop law maps active power to frequency (P-f droop) and reactive power to voltage (Q-V droop), thereby emulating the governor and excitation responses of synchronous machines and providing primary frequency regulation [118, 119, 120, 121].

These frequency and voltage droops are commonly derived under the assumption of predominantly inductive line impedance[3], which approximately decouples active and reactive power. For a voltage-source inverter connected to the

[3] This assumption is reasonable for medium- and high-voltage grids or long cables [122]. In low-voltage grids with small X/R ratios, virtual impedance or modified droop laws are used to achieve robust sharing [123, Ch. 7, Ch. 19].

grid through an inductive reactance $X_L \gg R_L$ and for small angle deviations, the steady-state power exchange can be approximated as [124]

$$P \approx \frac{V_f V_{\text{grid}}}{X_L}\,\delta, \tag{2.13}$$

$$Q \approx \frac{V_f}{X_L}\left(V_f - V_{\text{grid}}\right), \tag{2.14}$$

where P and Q denote three-phase active and reactive power at the PCC, V_f and V_{grid} denote per-phase Root-Mean-Square (RMS) phasor voltages (positive sequence), X_L is the per-phase series reactance, and δ is the phase-angle difference (the "power angle") between the converter and grid voltage phasors.

These relations motivate the conventional droop laws [60]:

$$\omega = \omega^* - m_P\,(P - P^*), \tag{2.15}$$

$$V_f = V^* - m_Q\,(Q - Q^*), \tag{2.16}$$

with nominal setpoints ω^* and V^* and references P^* and Q^*. The droop slopes are defined as

$$m_P = -\frac{\Delta\omega}{\Delta P}, \qquad m_Q = -\frac{\Delta V}{\Delta Q}, \tag{2.17}$$

such that the maximum expected deviations in P and Q map to allowable deviations in frequency and voltage, respectively[4].

Although droop control is essential for decentralized sharing and frequency tracking, it does not provide an inertial response [125, 126]. In GFL converters the response remains reactive to the grid: it relies on PLL-based angle estimation and lacks a direct coupling between internal power balance and frequency, which limits performance during fast disturbances [127, 128, 129]. Although power electronic interfaces allow rapid actuation, immediate frequency support is

[4] Some references use the inverse slopes $n_P = \Delta P/\Delta\omega$ and $n_Q = \Delta Q/\Delta V$. This dissertation adopts $m_P = \Delta\omega/\Delta P$ and $m_Q = \Delta V/\Delta Q$ for consistency with Equations (2.15)–(2.16).

achieved with GFM control, which establishes voltage and frequency internally and can incorporate explicit frequency or swing dynamics [126, 116, 117].

2.4.4.3 Virtual Synchronous Machine (VSM)

Building on the physical principles outlined in Section 2.3.5, VSM control embeds a dynamical model analogous to the swing equation of a synchronous machine in order to establish GFM behavior and provide rapid autonomous frequency support [113, 130, 131, 132]. A power-based form of the swing dynamics is

$$P_{\mathrm{m}} - P_{\mathrm{e}} = 2H\,\dot{\omega} + D_p\,(\omega - \omega^*), \tag{2.18}$$

where H is the inertia constant, D_p is a damping coefficient, ω is the internal electrical angular frequency, and P_{m} and P_{e} denote input and output powers in per-unit. A commonly used normalized VSM implementation is

$$\dot{\tilde{\omega}} = \frac{1}{2H}\Big(P_{\mathrm{ref}} - P - D_p\,(\omega_{\mathrm{vsm}} - \omega_{\mathrm{g}})\Big), \tag{2.19}$$

with $\tilde{\omega} = \omega_{\mathrm{vsm}} - \omega^*$, reference power P_{ref}, measured output power P, internal angular frequency ω_{vsm}, and grid angular frequency ω_{g}. Equation (2.19) shows that virtual inertia H and frequency-dependent damping D_p are explicit design parameters. Practical realizations typically complement the frequency dynamics with a voltage-control loop and virtual impedance to regulate terminal voltage magnitude and shape the output impedance for stability and power sharing.

Comparative studies report improved transient performance and grid-support capabilities of VSM control relative to static droop control [127]. Motivated by these findings, Section 4.1 presents the formulation and analysis of a SoG-based VSM for communication-free AC/DC coupling.

2.4.5 Grid-Supportive Load Control

The potential of GSLs to provide ancillary services has been outlined in Section 2.3.6. This section discusses the implementation and control of GSLs and their role in complementing converter-based DC microgrids.

Field trials in the 2000s established that end-use devices can autonomously respond to frequency excursions and support stability without centralized dispatch [133]. Subsequent work moved beyond emergency underfrequency shedding toward continuous, sub-minute services and device-side controllers embedded in modern power-electronic loads (e.g., variable-speed drives, EV chargers) [87, 134, 135]. Compared with aggregator-style demand response on minute-hour horizons, GSLs aim at decentralized actions based solely on local measurements, thereby reducing latency and communication dependencies [87].

In DC microgrids, the signal for load-side support is the bus voltage. DC-native GSLs modulate their effective V-I characteristic to adapt power intake as a function of voltage deviations. Two complementary directions have emerged:
(i) Local electronic load control that realizes a variable internal impedance (or equivalent droop) with embedded screening logic and Proportional-Integral-Differential (PID) regulation, enabling rapid curtailment or absorption with minimal overhead. This improves bus-voltage regulation and helps preserve supply to critical loads [136].
(ii) Predictive scheduling of voltage-responsive loads within a Model Predictive Control (MPC) framework that co-optimizes voltage-based demand response and storage dispatch under uncertainty. Compared with stochastic MPC, approaches assisted by a deep Q network have reported lower operating cost, fewer battery cycles, and improved restoration of the DC-bus target by anticipating when to actuate voltage-based demand response versus storage injection [137].

The Electric Spring (ES) concept, originally proposed for AC systems, has been adapted to DC as series or shunt compensators co-located with noncritical loads. Multiple DC-ES units can be coordinated using a two-layer architecture, with primary droop for effort sharing and a secondary consensus layer to regulate

the average bus-voltage reference while balancing internal energy states [138]. Building on this idea, distributed virtual inertia on the load side can be realized by modulating a virtual capacitance within ES converters. A model-predictive controller adapts the virtual capacitance to increase it during disturbances for slower bus-voltage variation and to decrease it for faster recovery, while a consensus loop equalizes noncritical-load voltage deviations across devices. HIL tests and small-signal eigenvalue analysis substantiate the dynamic and stability benefits [139].

Despite these advancements, several open issues remain. These include rigorous stability and fairness guarantees without communication for heterogeneous, potentially non-passive ZIP-type loads, SoC-aware demand-side responses that do not rely on global signals, and reproducible validation in residential- and building-scale DC microgrids under converter nonlinearities and measurement noise. Furthermore, restoration strategies are required that explicitly consider the limited energy budgets of loads capable of providing only short-term support. These gaps motivate the controller in Section 4.2, which uses only local voltage feedback with a ZIP-based load representation, aligns demand modulation with SoC-aware support, and integrates an energy-based restoration mechanism.

2.5 Research Gaps and Contributions of this Dissertation

Building upon the preceding review and its identified limitations, this section first outlines the open challenges in hybrid AC/DC microgrid control. It then summarizes the contributions of this dissertation that address these challenges.

Open Challenges in Hybrid AC/DC Microgrid Control

Despite the substantial progress outlined in the preceding sections, several critical challenges remain that must be addressed to enable robust and scalable

control of decentralized DC microgrids that are interfaced to an AC grid or an AC microgrid.

- **Decentralized SoC balancing across hybrid DC–AC microgrids:** As indicated in Table 2.1, most methods either target isolated DC domains or focus on AC-side control. Communication-free methods capable of harmonizing BESSs utilization across interconnected DC and AC microgrids, remain largely unsolved.
- **Concurrent SoC balancing and frequency support:** While numerous studies have addressed decentralized SoC balancing within DC microgrids, the simultaneous provision of ancillary services, such as virtual inertia support and primary frequency control, to an interconnected AC grid remains insufficiently addressed. Achieving both objectives concurrently requires advanced control strategies that enable IC to support frequency and voltage regulation without compromising SoC balancing performance.
- **Integration of GSL in Decentralized DC Control:** Although recent studies have demonstrated the potential of GSL to enhance frequency and voltage stability, their systematic integration into decentralized energy management schemes for DC microgrids remains an open problem. In particular, there is a lack of robust coordination mechanisms that allow GSLs, BESSs, and generation units to operate in a harmonized manner without relying on centralized communication or control.
- **Consideration of nonlinear stability beyond small-signal:** Many of the existing control strategies focus on linearized (small-signal) stability. However, scalable and application-oriented methods are required to evaluate microgrid stability under nonlinear dynamics, ideally offering global guarantees or explicitly defined regions of attraction.
- **Experimental validation:** The literature frequently lacks system-level validations under realistic operating conditions with transparent reporting. There is a need for reproducible experiments with predefined metrics,

representative scenarios, and documented controller parameters, procedures, and datasets.

Addressing these challenges calls for novel, robust, and scalable control schemes that operate without centralized coordination or communication.

Research Contributions and Innovations

To address the gaps identified in Section 2.3 and Section 2.4, this dissertation develops an SoG-based control framework for decentralized hybrid AC/DC microgrids. At its core, the proposed approach encodes each unit's SoC into bounded setpoint offsets, thereby yielding a locally measurable coordination that enables communication-free SoC balancing and proportional power sharing in isolated DC microgrids as well as across AC/DC coupling via the IC (Chapter 3). Building on this principle, the IC control is extended toward GFM behavior to provide virtual inertia and frequency response on the AC side while preserving SoG-driven energy coordination (Chapter 4). Furthermore, GSLs are integrated into DC microgrids through decentralized voltage-dependent response characteristics, strengthening bus-voltage regulation and disturbance rejection without explicit communication (Chapter 4). The resulting closed-loop behavior is substantiated by nonlinear stability analysis, including Lyapunov-based arguments and Singular Perturbation Theory, complemented by reproducible system-level validation on the Smart2DC laboratory platform (Chapter 5). A consolidated overview of the dissertation's contributions is provided in Section 1.3.

2.6 Summary and Concluding Remarks

This chapter provides an overview of architectural concepts, component models, and control classifications for hybrid AC/DC microgrids under decentralized,

communication-free operation. It introduced the adopted non-isolated single-bus architecture and the control taxonomy that frames the subsequent developments (Section 2.1). The key components and models were summarized, including PV with MPPT, BESSs with coulomb-counting SoC estimation, half-bridge DC/DC converters and a three-phase two-level IC, as well as resistive and ZIP load representations (Section 2.2).

The analysis of control challenges in Section 2.3 highlights four key aspects. First, high-bandwidth local voltage regulation is essential to maintain DC-bus stability under fast transients (Section 2.3.1). Second, power sharing and SoC balancing are intrinsically interdependent, and conventional droop control is sensitive to resistive distribution lines and parameter mismatches (Section 2.3.2, Section 2.3.3). Third, stability must be evaluated in both supply-balancing and control-system dimensions, requiring not only small-signal analysis but also nonlinear methods to address system dynamics beyond linearization (Section 2.3.4). Fourth, effective AC/DC interaction requires coordinated IC control and the systematic integration of GSLs for decentralized voltage support (Section 2.3.5, Section 2.3.6).

The review of existing approaches (Section 2.4) identified persistent gaps: limited SoC awareness in the primary layer, cross-domain SoC balancing via the IC, early adoption of GSL in DC microgrids, reliance on idealized impedances, and a shortage of reproducible system-level experiments (Table 2.1). These findings motivate the SoG framework in Chapter 3 and its extensions to GFM behavior and GSL integration in Chapter 4, with rigorous stability analysis and experimental validation presented in Chapter 5.

3 The State-of-Grid Control Concept

This chapter presents the central contribution of this dissertation: the SoG control concept. The method enables communication-free SoC balancing and proportional power sharing in hybrid AC/DC microgrids.

The core idea is to encode each unit's SoC as a small bounded offset of its converter output voltage setpoint. These slowly varying offsets drive autonomous SoC equalization and proportional sharing based solely on local measurements, without explicit communication. The method is extended to AC grids by encoding SoC information in small frequency setpoint offsets, thereby enabling coordinated operation and SoC balancing across the AC and DC domains. An overview of the structural elements of the SoG control architecture is shown in Figure 3.1. The approach comprises two complementary components: (i) a

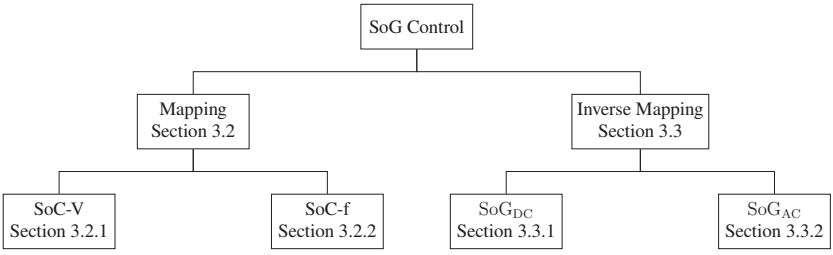


Figure 3.1: Schematic representation of the SoG control concept. The framework is structured into mapping (Section 3.2), which projects the SoC to measurable quantities such as voltage (V) or frequency (f), and inverse mapping (Section 3.3), which enables decentralized inference of the global system state.

mapping that projects internal energy states (SoCs) onto system-wide observable variables (voltages and frequency), and (ii) an inverse mapping, that allows each unit to estimate the global state of the grid from local voltage or frequency measurements.

Figure 3.2 illustrates how the concept applies in a hybrid microgrid. On the DC side (left), each converter-integrated BESS operates according to a local SoC-V mapping, described in Section 3.2.1. On the AC side (right), inverters apply a SoC-f mapping, introduced in Section 3.2.2. The interface converter connects both domains and regulates the cross-domain power flow based on the SoG metric, which is defined in Section 3.3.

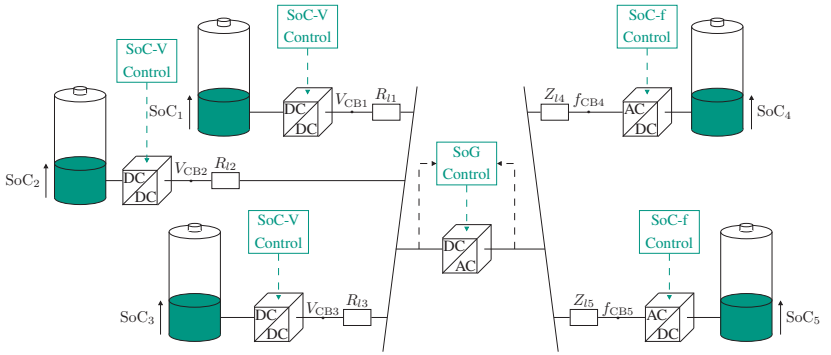


Figure 3.2: Illustrative overview of the proposed SoG-based control concept for hybrid AC/DC microgrids. Converter-integrated BESS on the DC side (left) encode their SoC as small voltage deviations via the local SoC-V mapping (Section 3.2.1), while inverters on the AC side (right) project their SoC into the frequency deviations (Section 3.2.2). The central IC links both domains and uses the inverse SoG mappings to compute the system-wide energy imbalance (Section 3.3) and control the cross-domain power flow accordingly (Section 3.4). This architecture enables implicit coordination of energy states and self-organized power sharing without communication.

Before proceeding, the operating assumptions and design conditions used throughout the development are stated.

Assumptions for Control Design and Analysis

To enable a systematic development and analysis of the proposed control strategy, the following assumptions are made. They reflect a typical microgrid configuration and are justified based on practical design principles and established methodologies.

Assumption 3.1 (Time-scale separation). *The system is assumed to exhibit a hierarchical time-scale separation, with current control operating faster than voltage control, and voltage control faster than energy or SoC dynamics. This can be enforced by controller tuning and is used for singular perturbation arguments (see Appendix A.6).*

Assumption 3.2 (Predominantly inductive AC grid). *The AC grid is assumed to exhibit a high X/R ratio, which enables simplified active power sharing via frequency deviations and the SoG frequency mapping (see Section 3.2.2). Such an inductive characteristic can be obtained by (i) series filter inductors at the converter output, (ii) emulating virtual inductance through inverter control algorithms, or (iii) proper selection of line parameters (cross section, material, and length).*

Assumption 3.3 (Proper system sizing). *The DC microgrid is assumed to be adequately sized with respect to converter ratings, energy storage capacity, and line impedance. No single unit is assumed to dominate the bus dynamics. This assumption ensures that the common bus voltage provides a valid system-wide indicator of the global energy state. The sizing follows established design criteria, such as those discussed in* [140].

The remainder of this chapter is organized as follows. Section 3.1 sets out the core concept, defines the notation, and outlines the principal design parameters. Section 3.2 then formalizes the mapping of internal energy states to observable variables. Section 3.2.1 derives the SoC-to-voltage map for the DC side; Section 3.2.2 extends the mapping to the AC side by mapping SoC to small frequency setpoint offsets. Section 3.3 develops the inverse SoG mapping for

global grid-state estimation and provides precise definitions of $\mathrm{SoG}_{\mathrm{DC}}$ and $\mathrm{SoG}_{\mathrm{AC}}$. Building on these results, Section 3.4 presents a decentralized AC/DC coupling method that controls interlink power exchange from locally inferred SoG signals. Finally, Section 3.5 provides the stability analysis. The chapter closes with a summary and concluding remarks in Section 3.6.

3.1 Core Concept and Definitions

The proposed SoG-based control approach is inspired by the physical analogy of interconnected hydraulic vessels[1]. In physics, such systems illustrate how fluid levels in communicating vessels naturally equalize based solely on hydrostatic pressure differences, without requiring centralized coordination [141].

The classical mobility analogy [142] relates equivalent variables across physical domains. In the hydraulic-electrical view adopted in this dissertation, the *across* variable is the hydrostatic pressure p and the *through* variable is the volumetric flow rate Q; these map to the electrical voltage v and current i, respectively [143]. Table 3.1 summarizes the mapping used in the present dissertation.

Table 3.1: Key analogies between electrical and hydraulic systems expressed in generalized variables.

Generalized Variable	Electrical System	Hydraulic System
Effort	Voltage (V)	Hydrostatic Pressure (p)
Flow	Current (I)	Flow Rate (Q)
Resistance	Electrical Resistance (R)	Hydraulic Resistance (R_{h})
New (introduced)	State-of-Charge (SoC)	Fluid Level (h)

[1] The analogy used in this dissertation follows the classical mobility analogy under idealizations: incompressible single-phase fluid in rigid, leak-free containers; laminar flow and small-signal operation; negligible capillarity, cavitation, thermal effects, and fluid inertia in the steady-state argument. Identical cross sections are not required for level equalization.

In both domains, the relation between effort, flow, and resistance follows the same formal relationship. For the hydraulic system in Figure 3.3(a), the pressures at the bases of two vessels are

$$p_1 = \rho g h_1, \quad p_2 = \rho g h_2, \tag{3.1}$$

such that the driving pressure difference

$$\Delta p = p_1 - p_2 = \rho g (h_1 - h_2) \tag{3.2}$$

induces the volumetric flow

$$Q = \frac{\Delta p}{R_h}. \tag{3.3}$$

In the corresponding electrical system shown in Figure 3.3(b), the converter output voltages take the role of the pressures,

$$V_{\mathrm{C,B1}} \Leftrightarrow p_1, \quad V_{\mathrm{C,B2}} \Leftrightarrow p_2, \tag{3.4}$$

and the potential difference

$$\Delta V = V_{\mathrm{C,B1}} - V_{\mathrm{C,B2}} \tag{3.5}$$

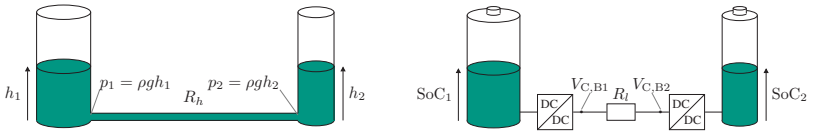
yields the analogous relation

$$Q = \frac{\Delta p}{R_{\mathrm{h}}} \quad \Longleftrightarrow \quad I = \frac{\Delta V}{R}. \tag{3.6}$$

This side-by-side mapping preserves the effort-flow analogy ($p \leftrightarrow V,\ Q \leftrightarrow I$) and power consistency ($p\,Q \leftrightarrow V\,I$), while motivating the interpretation

$$\Delta p_i \propto \Delta h_i \quad \Longleftrightarrow \quad \Delta V_{\mathrm{C,B}i} \propto \Delta \mathrm{SoC}_i. \tag{3.7}$$

Hence, this analogy motivates the SoC-based reference voltage formulation adopted in this dissertation, in which the converter voltage reference is modulated according to the instantaneous SoC to achieve SoC balancing.



(a) Communicating vessels. **(b)** Battery interaction on a DC-bus.

Figure 3.3: Analogy between (a) communicating vessels and (b) their electrical counterpart, representing the conceptual foundation of the SoG approach. In both systems, equilibrium emerges naturally through decentralized interactions without centralized coordination. Adapted from [J7].

Conceptually, each battery is treated as a vessel and its SoC as the fluid level. The resulting 'pressure' variation in the analogy is realized in the electrical domain by a slight, bounded deviation of the converter's terminal voltage from its nominal value. When several BESSs are connected to a common DC-bus, these local deviations interact through the grid and collectively reflect a shared SoG signal that indicates the global stored energy condition of the system. In hydraulics, water flows from higher to lower levels until equilibrium is reached. In the electrical domain, the developed controller adjusts each unit's terminal voltage as a function of its SoC, thereby creating slight, controlled voltage differences that drive energy transfer from higher SoC units to lower-SoC units until balance is achieved. Once SoCs have equalized, they remain aligned even as generation or load changes occur, as all units respond proportionally to deviations in the shared bus voltage. No communication infrastructure or centralized data processing is required; local voltage measurements suffice to achieve self-organized, system-wide energy balancing.

A central feature of the SoG concept is that local voltage deviations aggregate into a shared DC-bus signal. A positive offset within admissible bounds indicates a predominantly high system SoC, whereas a negative offset indicates an energy deficit. This self-organizing behavior enables continuous adaptation to the collective energy state without external commands.

Originally conceived for DC microgrids, the SoG concept extends naturally to hybrid AC/DC systems. On the AC side, the same information can be conveyed by small frequency setpoint variations. A higher SoC corresponds to a slightly

higher reference frequency, prompting the unit to supply more active power to the grid. Conversely, a lower SoC results in a slightly reduced frequency reference, leading the unit to decrease its output or even absorb power when required. At the IC, this mapping defines the direction of energy exchange between the DC and AC subsystems. A reference frequency slightly above nominal indicates surplus energy on the AC side and results in power export to the DC side. A reference frequency slightly below nominal setpoint indicates an energy deficit and results in import from DC to AC. In this way, small bounded frequency offsets realize decentralized coordination and support synchronized SoC balancing across distributed BESSs without explicit communication.

Based on the physical analogy and conceptual foundations above, the next section introduces mapping functions that translate the internal SoC of distributed BESSs into observable quantities, namely voltage on the DC side and frequency on the AC side. These local quantities act as implicit coordination signals from which a global indicator of the grid condition, the SoG, can be inferred in a fully decentralized manner.

3.2 Mapping of Internal Energy States

Based on Section 3.1, this section defines the mapping laws that encode each unit's SoC as small, bounded offsets of its voltage (DC) and frequency (AC) references. The mappings are local, static mappings that are monotone in SoC and limited to permissible operating ranges.

3.2.1 SoC-to-Voltage Mapping (DC-Side)

On the DC side, the reference voltage of converter i is modulated as

$$V^*_{\mathrm{C,B}i} \;=\; V^*_{\mathrm{DC}} \left(1 + \sigma \, \frac{\mathrm{SoC}_i - \mathrm{SoC}^*_i}{\mathrm{SoC}_{\Delta,i}}\right), \qquad \text{for } i \in \{1, \ldots, n\}, \tag{3.8}$$

where n is the number of BESSs connected to the DC-bus, V_{DC}^{*} denotes the constant baseline bus-voltage reference, $\mathrm{SoC}_i \in [0,1]$ is the instantaneous SoC, $\mathrm{SoC}_i^{*} \in [0,1]$ is the desired operating point (e.g., $\mathrm{SoC}_i^{*} = 0.5$ for $50\,\%$), and $\mathrm{SoC}_{\Delta,i}$ is the normalization factor of the mapping, specified in (3.10). The dimensionless gain $\sigma \in (0,1)$ is a global mapping gain that sets the sensitivity of the SoC to voltage mapping and bounds the maximum permissible voltage deviation (e.g., $\sigma = 0.05$ for $\pm 5\,\%$) (see Figure 3.5). Using $\mathrm{SoC}_{\Delta,i}$ from (3.10), the mapping remains within the admissible envelope,

$$V_{\mathrm{C,B}i}^{*} \in \left[V_{\mathrm{DC}}^{*}(1-\sigma),\, V_{\mathrm{DC}}^{*}(1+\sigma)\right], \tag{3.9}$$

and varies monotonically with SoC_i. In particular, the mapping is affine and therefore globally Lipschitz continuous on $[0,1]$ with the Lipschitz constant $L_i = (V_{\mathrm{DC}}^{*}\sigma)/\mathrm{SoC}_{\Delta,i}$.

3.2.1.1 Normalization Factor $\mathrm{SoC}_{\Delta,i}$

The factor $\mathrm{SoC}_{\Delta,i}$ rescales the instantaneous deviation from the reference SoC_i^{*} relative to the admissible operating interval $[\mathrm{SoC}_i^{\min}, \mathrm{SoC}_i^{\max}]$ such that the normalized deviation lies in $[-1,1]$. This yields symmetric weighting of positive and negative deviations even if SoC_i^{*} is not centered in the admissible range. The normalization factor $\mathrm{SoC}_{\Delta,i}$ is defined as

$$\mathrm{SoC}_{\Delta,i} = \begin{cases} \mathrm{SoC}_i^{\max} - \mathrm{SoC}_i^{*}, & \text{if } \mathrm{SoC}_i - \mathrm{SoC}_i^{*} > 0, \\ \mathrm{SoC}_i^{*} - \mathrm{SoC}_i^{\min}, & \text{otherwise.} \end{cases} \tag{3.10}$$

This definition ensures that, for all $\mathrm{SoC}_i \in [\mathrm{SoC}_i^{\min}, \mathrm{SoC}_i^{\max}]$, the normalized deviation satisfies

$$\frac{\mathrm{SoC}_i - \mathrm{SoC}_i^{*}}{\mathrm{SoC}_{\Delta,i}} \in [-1,1]. \tag{3.11}$$

Note that $\mathrm{SoC}_{\Delta,i}$ is constant for a given sign of the deviation and switches its value only at $\mathrm{SoC}_i = \mathrm{SoC}_i^{*}$. The resulting mapping in (3.8) is therefore

continuous and strictly monotone, while its derivative may be discontinuous at SoC_i^*.

Figure 3.4 illustrates the effect for two converter-integrated BESSs with distinct references SoC_1^* and SoC_2^*. In the symmetric case (left), $\mathrm{SoC}_1^* = 0.5$ corresponds to the midpoint. In the asymmetric case (right) with $\mathrm{SoC}_2^* > 0.5$, the headroom above the reference is reduced. Without normalization, a positive deviation above SoC_2^* would induce a larger control action than an equally sized negative deviation.

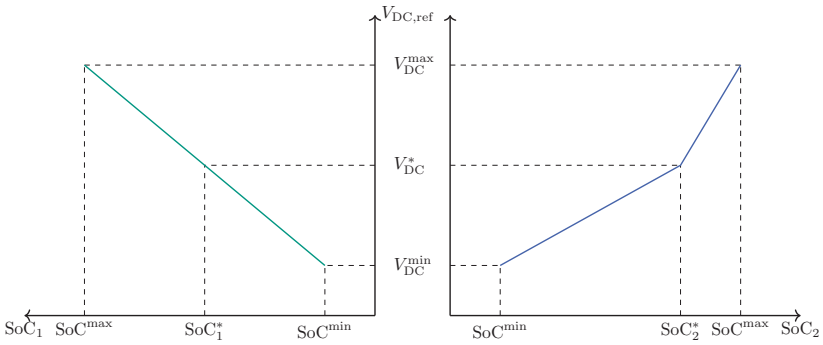


Figure 3.4: Illustration of the necessity of the normalization factor $\mathrm{SoC}_{\Delta,i}$ for two BESSs with different reference values. Left: symmetric case with $\mathrm{SoC}_1^* = 0.5$. Right: asymmetric case with $\mathrm{SoC}_2^* > 0.5$. Without normalization, the slope for $\mathrm{SoC}_2 > \mathrm{SoC}_2^*$ would be significantly steeper, leading to excessive voltage deviations $V_{\mathrm{C,B2}}^*$, while the slope for $\mathrm{SoC}_2 < \mathrm{SoC}_2^*$ would remain too shallow. The normalization compensates for this and ensures uniform control sensitivity. Adapted from [J7].

The factor $\mathrm{SoC}_{\Delta,i}$ compensates this asymmetry and restores uniform control sensitivity.

3.2.1.2 Selecting the Mapping Gain σ

The mapping gain σ bounds the relative offset of the reference voltage. It must be selected to respect the admissible voltage envelope, to preserve time-scale separation with the inner voltage loop, and to ensure observability relative to the

measurement noise floor. Figure 3.5 illustrates how the chosen σ maps the SoC trajectory into the voltage reference $V^*_{\mathrm{C,B}i}$: larger σ increases both the steady offset and the ramp slope.

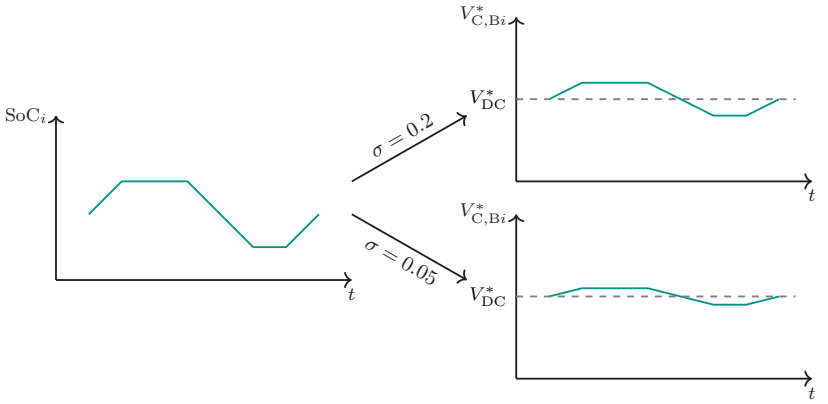


Figure 3.5: Effect of the mapping gain σ on the mapping of the battery SoC_i into the output voltage $V^*_{\mathrm{C,B}i}$. The left side shows a representative time profile of the battery SoC. The right side illustrates how different values of σ influence the voltage mapping (top: $\sigma = 0.2$, bottom: $\sigma = 0.05$). Larger values of σ result in stronger voltage deviations. Adapted from [J7].

First, the voltage envelope imposes hard bounds. With admissible bus limits $V_{\min}$ and $V_{\max}$ and nominal voltage V^*_{DC}, the constraint

$$\sigma \;\le\; \min\left\{ \frac{V_{\max}}{V^*_{\mathrm{DC}}} - 1,\; 1 - \frac{V_{\min}}{V^*_{\mathrm{DC}}} \right\} \tag{3.12}$$

guarantees $V^*_{\mathrm{C,B}i} \in [V_{\min},\, V_{\max}]$ even at the extremes of the mapping.

Second, time-scale separation requires the SoC-driven reference to vary slowly compared with the closed-loop voltage dynamics. Let $\bar{s}_i := \sup_t |\dot{\mathrm{SoC}}_i(t)|$ be a bound on the SoC rate and let ω_v denote the closed-loop bandwidth of the inner

voltage control. From the mapping law, the derivative of the projected voltage is bounded as

$$\left|\dot{V}^{*}_{\mathrm{C,B}i}\right| \;\leq\; \frac{\sigma V^{*}_{\mathrm{DC}}}{\mathrm{SoC}_{\Delta,i}}\,\bar{s}_i. \tag{3.13}$$

To keep the mapping quasi-static for the inner loop and to enforce Assumption 3.1, requires

$$\frac{\sigma V^{*}_{\mathrm{DC}}}{\mathrm{SoC}_{\Delta,i}}\,\bar{s}_i \;\leq\; \gamma\,\omega_v\,V^{*}_{\mathrm{DC}}, \tag{3.14}$$

which is equivalent to

$$\sigma \leq \gamma\,\frac{\omega_v\,\mathrm{SoC}_{\Delta,i}}{\bar{s}_i}. \tag{3.15}$$

Thereby, $\gamma > 0$ denotes the admissible relative ramp-tracking error of the inner voltage loop. Under this condition, the reference varies more slowly than the inner-loop dynamics, and the ramp-tracking error is bounded by $\gamma\,V^{*}_{\mathrm{DC}}$. A practical choice is $\gamma \in [0.05,\,0.1]$, corresponding to at most 5-10% relative tracking error during worst-case SoC-induced ramps and matching the common design heuristic of at least one decade time-scale separation.

Finally, observability requires that the smallest effective offset exceeds the measurement noise floor. If V_{n} denotes this noise floor, the condition

$$\sigma\,V^{*}_{\mathrm{DC}} \;\geq\; k_v\,V_{\mathrm{n}}, \qquad k_v \in [5,\,10], \tag{3.16}$$

must be satisfied, where k_v represents a safety margin factor. This constraint ensures that the minimal offset remains discernible despite measurement noise, typically ensuring the offset is several times larger than the effective measurement noise level.

In practice, σ must satisfy all three requirements simultaneously, leading to the joint constraint

$$\frac{k_v V_{\mathrm{n}}}{V^{*}_{\mathrm{DC}}} \;\leq\; \sigma \;\leq\; \min\!\left\{\frac{V_{\max}}{V^{*}_{\mathrm{DC}}}-1,\;1-\frac{V_{\min}}{V^{*}_{\mathrm{DC}}},\;\gamma\,\frac{\omega_v\,\mathrm{SoC}_{\Delta,i}}{\bar{s}_i}\right\}. \tag{3.17}$$

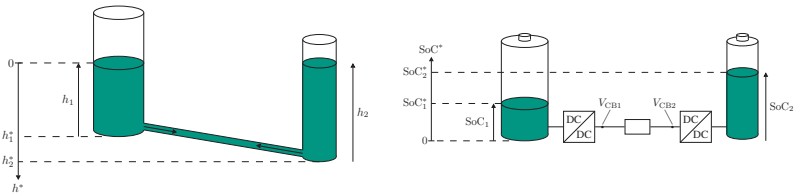
3.2.1.3 Desired Operating Point SoC_i^*

The parameter SoC_i^* in Equation (3.8) defines the bias of the normalized deviation $(\mathrm{SoC}_i - \mathrm{SoC}_i^*)$ and thereby determines the equilibrium point around which the reference voltage $V_{\mathrm{C,B}i}^*$ is modulated.

Intuitively, SoC_i^* sets the vessels height in the hydraulic analogy (see Figure 3.6): increasing SoC_i^* reduces $V_{\mathrm{C,B}i}^*$ for a given SoC_i, thereby decreasing the unit's tendency to discharge. Conversely, a lower SoC_i^* increases $V_{\mathrm{C,B}i}^*$ and prompts stronger power injection. Thus, relative differences in SoC_i^* among BESS units shape the steady-state power sharing without requiring communication, while the local mapping law itself remains unchanged.

To ensure meaningful modulation and avoid excessive sensitivity due to the normalization (see Equation (3.10)), the desired operating point should remain well within the permissible bounds $\mathrm{SoC}_i^* \in (\mathrm{SoC}_i^{\min}, \mathrm{SoC}_i^{\max})$.

In practice, the setpoints SoC_i^* also serve as tuning parameters in higher-level control layers, enabling the implementation of energy policies such as reserve maintenance, prioritization, or cycling constraints. These supervisory updates must be significantly slower than the local voltage control loop. Piecewise-constant scheduling on the order of minutes has proven sufficient.



(a) Communicating vessels. **(b)** Battery interaction on a DC-bus.

Figure 3.6: Hydraulic analogy and DC implementation. Modifying the desired SoC operating point SoC_i^* shifts the projected voltage $V_{\mathrm{C,B}i}^*$, altering the local charging or discharging tendency, while the mapping law itself remains unchanged.

3.2.1.4 Control Structure of the SoC to Voltage Mapping

Figure 3.7 shows the realization of the SoC-to-voltage mapping for a converter-integrated BESS. The estimated SoC is translated into a voltage reference that encodes the unit's relative energy state and enables implicit coordination via the shared DC-bus.

The SoC estimator (see Section 2.2.2) provides the value $\mathrm{SoC}_{\mathrm{B1}}$, which is used to compute the voltage reference $V^*_{\mathrm{C,B1}}$ according to the mapping rules in (3.8) and (3.10). In this way, the internal energy status is projected onto a locally measurable electrical quantity, enabling implicit coordination through the shared DC-bus.

Accurate tracking of the voltage reference is achieved by a cascaded controller structure. The outer voltage loop determines the battery current reference i^*_{B1},

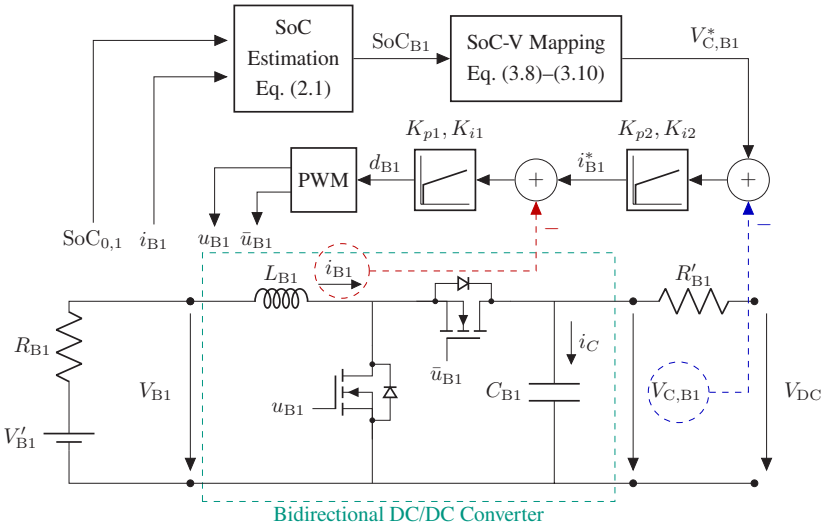


Figure 3.7: Detailed decentralized control scheme for a converter-integrated battery in a DC microgrid. The SoC-V droop mapping (Equations (3.8)–(3.10)) generates a voltage reference based on the estimated SoC (Equation (2.1)). This reference is tracked by cascaded PI voltage and current controllers, which drive the bidirectional DC/DC converter. Adapted from [J1].

which is tracked by the inner current loop. The resulting control signal is translated into PWM gating signals for the bidirectional converter. This control hierarchy ensures that the terminal voltage $V_{\mathrm{C,B1}}$ closely follows $V^*_{\mathrm{C,B1}}$, thereby allowing the unit to modulate the common bus voltage according to its SoC.

Two implementations of the cascaded voltage and current control are investigated:

- An outer-loop proportional voltage control with an inner-loop PI current controller;
- An outer-loop PI voltage control with an inner-loop PI current controller (hereafter referred to as the PI-based SoG controller).

Comparative performance is assessed experimentally in Section 5.3. Design and implementation details for the voltage and current loops are provided in Appendix A.1.

3.2.2 SoC-to-Frequency Mapping (AC-Side)

As outlined in Section 3.1, the SoG concept encodes the local SoC as a small, bounded offset of the frequency reference on the AC side. Under the classical active power-frequency characteristics in distribution grids[2], a slightly elevated frequency setpoint biases a GFM unit toward exporting active power, whereas a reduced setpoint favors import. Leveraging this property, the frequency reference of the jth battery-side inverter is defined as

$$f^*_{\mathrm{B}j} = f^*_{\mathrm{AC}} \left(1 + \sigma \frac{\mathrm{SoC}_j - \mathrm{SoC}^*_j}{\mathrm{SoC}_{\Delta,j}}\right), \qquad \text{for } j \in \{1, \ldots, m\}, \tag{3.18}$$

where m is the number of BESS inverters on the AC side, f^*_{AC} is the constant baseline frequency reference, and $\sigma \in (0, 1)$ is the dimensionless mapping gain

[2] This formulation assumes a predominantly inductive AC grid impedance (see Assumption 3.2).

introduced in Section 3.2.1. The normalization factor $\mathrm{SoC}_{\Delta,j} > 0$ is defined identically to (3.10), ensuring symmetric treatment of positive and negative SoC deviations even if SoC_j^* is not centered in the admissible range.

The mapping in (3.18) is affine in SoC_j, centered at SoC_j^*, strictly monotone, and bounded by design. It is the formal counterpart of (3.8) with the replacements $V_{\mathrm{DC}}^* \to f_{\mathrm{AC}}^*$ and $V_{\mathrm{C,B}i}^* \to f_{B_j}^*$. Using a common σ across domains preserves a consistent SoG encoding. If domain specific tuning is required, a dedicated σ_f can be introduced on the AC side and selected according to the AC analogue of the DC feasibility bound (3.17), namely

$$\frac{k_f\, f_{\mathrm{n}}}{f_{\mathrm{AC}}^*} \;\le\; \sigma_f \;\le\; \min\left\{ \frac{f_{\max}}{f_{\mathrm{AC}}^*} - 1,\; 1 - \frac{f_{\min}}{f_{\mathrm{AC}}^*},\; \gamma\, \frac{\omega_f\, \mathrm{SoC}_{\Delta,j}}{\bar{s}_j} \right\}, \tag{3.19}$$

which is obtained by applying the same design arguments as those used to derive (3.17), namely observability with respect to the frequency measurement noise floor, compliance with the admissible frequency envelope, and preservation of time-scale separation in the inner frequency loop, formulated for frequency domain quantities.

3.3 Inverse SoG Mapping

While the mappings defined in Equations (3.8) and (3.18) are applied by BESSs to project their internal SoC into observable grid quantities, namely voltage and frequency, the inverse mapping enables all other components to reconstruct a representative system condition, referred to as the SoG, from these quantities. Each unit observes the DC-bus voltage V_{DC} or grid frequency f_{AC} and applies the inverse mapping to estimate a representative indicator of the aggregated energy balance. This estimation can then be used to regulate power transfer between interconnected microgrids, such as between DC and AC microgrids (see Section 3.4), to provide adaptive frequency support (see Section 4.1), or to coordinate flexible loads (see Section 4.2). The mechanism requires no explicit

communication and forms a cornerstone of the proposed decentralized control concept for hybrid AC/DC microgrids.

3.3.1 Definition of $\mathrm{SoG}_{\mathrm{DC}}$

Inverting the DC side mapping law (3.8) yields the DC side SoG,

$$\mathrm{SoG}_{\mathrm{DC},k} = \mathrm{SoG}^{*}_{\mathrm{DC},k} + \frac{\mathrm{SoG}_{\Delta,k}}{\sigma}\left(\frac{V_k}{V^{*}_{\mathrm{DC}}} - 1\right), \qquad \forall k \in \mathcal{K}, \tag{3.20}$$

where $\mathcal{K}$ denotes the index set of components that evaluate the inverse mapping at their local DC terminals (e.g., ICs between microgrids, GSLs, VSMs). For each $k \in \mathcal{K}$, V_k is the locally measured DC-node voltage at the component terminals. The term $\mathrm{SoG}^{*}_{\mathrm{DC},k}$ is a defined nominal reference, whereas the factor $\mathrm{SoG}_{\Delta,k}$ serves as a normalization factor, defined analogously to (3.10) as

$$\mathrm{SoG}_{\Delta,k} = \begin{cases} \mathrm{SoG}^{\max}_{k} - \mathrm{SoG}^{*}_{k}, & \text{if } \mathrm{SoG}_{\mathrm{DC},k} \geq \mathrm{SoG}^{*}_{k}, \\ \mathrm{SoG}^{*}_{k} - \mathrm{SoG}^{\min}_{k}, & \text{otherwise,} \end{cases} \tag{3.21}$$

ensuring symmetric sensitivity to positive and negative SoC deviations. The parameter $\sigma \neq 0$ is the DC-side mapping gain used in (3.8). A higher value of $\mathrm{SoG}_{\mathrm{DC},k}$ indicates a surplus of available storage in the system, whereas a lower value indicates a deficit.

Equation (3.20) yields a meaningful estimate if the locally measured voltage V_k is a reliable proxy for the common bus state. This requires (i) selecting the mapping gain σ in accordance with the envelope and time scale conditions in (3.12) and (3.14), and (ii) ensuring that topological asymmetries are either small or explicitly compensated. Unequal line resistances bias the shared bus voltage and can distort the consensus signal. The impact of heterogeneous cable impedances on SoG-based coordination is analyzed in [J1] and corroborated experimentally.

3.3.2 Definition of $\mathrm{SoG}_{\mathrm{AC}}$

In analogy to the DC-side inverse mapping in (3.20) and obtained by algebraic inversion of the forward frequency mapping (3.18), the AC-side SoG at converter node l is defined as

$$\mathrm{SoG}_{\mathrm{AC},l} = \mathrm{SoG}^{*}_{\mathrm{AC},l} + \frac{\mathrm{SoG}_{\Delta,l}}{\sigma}\left(\frac{f_l}{f^{*}_{\mathrm{AC}}} - 1\right), \qquad \forall l \in \mathcal{L}, \tag{3.22}$$

where $\mathcal{L}$ denotes the index set of components that evaluate the inverse AC-side mapping at their local AC terminals. For each $l \in \mathcal{L}$, f_l is the locally estimated grid frequency (after PLL/filtering) at the component terminals. Moreover, f^{*}_{AC} is the nominal frequency and $\mathrm{SoG}_{\Delta,l}$ is the AC-side normalization factor, defined analogously to (3.21). A slightly positive bias in f_l indicates a tendency toward active power export, and a negative bias indicates import, consistent with the classical P-f characteristics in grids with predominantly inductive impedance (see Assumption 3.2).

Equation (3.22) provides a reliable estimate if (i) σ satisfies (3.19) and (ii) the local frequency is estimated with adequate accuracy. Harmonics and switching transients must be attenuated by a robust PLL or suitable filtering so that the smallest induced offset remains above the measurement noise floor.

3.4 SoG-Based AC-DC Coupling

The active power transfer between DC and AC subsystems is governed by the difference in their respective SoG quantities, $\mathrm{SoG}_{\mathrm{DC},k}$ and $\mathrm{SoG}_{\mathrm{AC},l}$, which are reconstructed from local SoC measurements using the inverse mappings introduced in Section 3.3 (cf. Equations (3.20) and (3.22)). These normalized values serve as locally computable indicators of the subsystem energy states.

A higher SoG value in one domain signifies a relative surplus, whereas a lower value in the other domain indicates a deficit. This motivates defining a coupling

law such that the active power transfer commanded to the IC is proportional to the SoG mismatch. With the sign convention that a positive reference $P^*_{kl} > 0$ denotes power flow from DC to AC, the mismatch is defined as

$$\Delta\mathrm{SoG}_{kl} := \mathrm{SoG}_{\mathrm{DC},k} - \mathrm{SoG}_{\mathrm{AC},l}. \tag{3.23}$$

This quantity serves as the driving signal for the active power exchange. To scale the response in accordance with the converter rating, the proportional control law is introduced as

$$P_{kl} = K_P \Delta\mathrm{SoG}_{kl}. \tag{3.24}$$

To achieve zero steady-state error in the cross-domain SoG alignment, the proportional law in (3.24) can be extended to a PI structure:

$$\tilde{P}_{kl}(t) = K_P \Delta\mathrm{SoG}_{kl}(t) + K_I \int_0^t \Delta\mathrm{SoG}_{kl}(\tau)\, d\tau, \tag{3.25}$$

where $K_I > 0$ is the integral gain.

To mitigate chattering[3] near equilibrium and ensure compliance with the converter rating, a deadband and saturation are applied,

$$P^*_{kl} = \mathrm{sat}_{[-P_{\mathrm{IC}}^{\max},\, P_{\mathrm{IC}}^{\max}]}\Big(\mathcal{D}_{P_{\mathrm{IC}}^{\min}}(P_{kl}) \Big), \tag{3.26}$$

with

$$\mathcal{D}_\Delta(x) = \begin{cases} 0, & |x| < \Delta, \\ x, & \text{otherwise}, \end{cases} \qquad \mathrm{sat}_{[a,b]}(x) = \min\{\, \max\{x, a\},\, b\}. \tag{3.27}$$

Thereby, $P_{\mathrm{IC}}^{\max}$ denotes the rated converter power, and $P_{\mathrm{IC}}^{\min} > 0$ defines a small deadband that filters out minor fluctuations caused by measurement noise or

[3] Chattering refers to high-frequency switching around a decision boundary, which increases losses and device wear and can degrade closed-loop performance [144].

ripple. By construction, $P^*_{kl} > 0$ denotes power export from DC to AC, whereas $P^*_{kl} < 0$ indicates import.

The resulting control scheme is illustrated in Figure 3.8. It visualizes the decentralized processing of local SoC measurements, the SoG mismatch computation, and the generation of the active power reference P^*_{kl}, which is tracked by a IC controller such as a VSM.

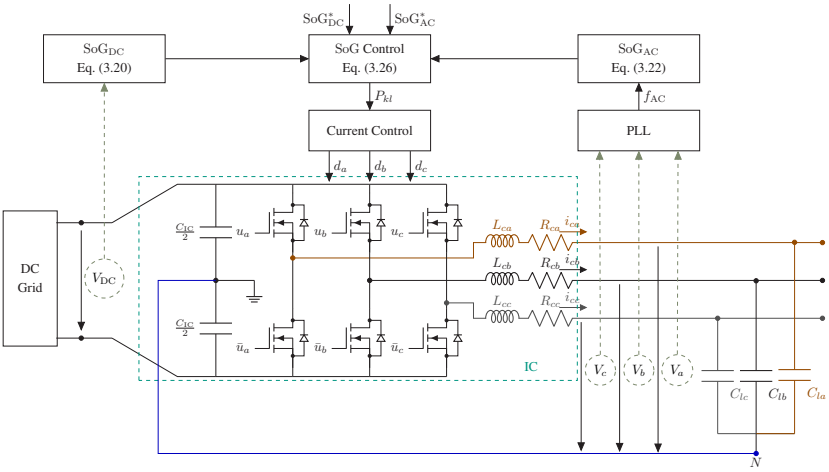


Figure 3.8: Control structure of the SoG-based DC/AC IC. The SoG values from the DC and AC domains ($\mathrm{SoG}_{\mathrm{DC},k}$, $\mathrm{SoG}_{\mathrm{AC},l}$) are obtained through inverse mappings (see (3.20), (3.22)). Their mismatch $\Delta\mathrm{SoG}_{kl}$ generates the active power reference P^*_{kl} according to (3.26). By convention, $P^*_{kl} > 0$ indicates power flow from DC to AC. The reference is tracked by a GFM loop (e.g., a VSM) that issues the modulation commands d_a, d_b, d_c.

To better understand the behavior of the proposed control law, the resulting mapping from $\mathrm{SoG}_{\mathrm{DC},k}$ and $\mathrm{SoG}_{\mathrm{AC},l}$ to the power reference P^*_{kl} is visualized in Figure 3.9.

This three-dimensional surface illustrates how the active power reference emerges from local SoC values via the projection and inverse-mapping scheme. The SoC values are first projected to voltage and frequency references based on Equations (3.8) and (3.18) (red and blue curves in Figure 3.9). These references

are then mapped back to the normalized SoG quantities using (3.20) and (3.22), and their difference determines the power reference via (3.26).

The surface highlights key operating regions: a high DC-side SoG and low AC-side SoG yield positive P^*_{kl} values (yellow), corresponding to power export. The opposite configuration results in negative values (blue), representing power import.

Dashed lines in the figure trace an example where $\mathrm{SoC}_{\mathrm{DC},k} = 0.3$ and $\mathrm{SoC}_{\mathrm{AC},l} = 0.6$. This path follows the projection to local references, reconstruction of SoG values, and final combination to yield the normalized power reference. The resulting point on the three-dimensional surface exemplifies how the converter behavior is fully determined from local information.

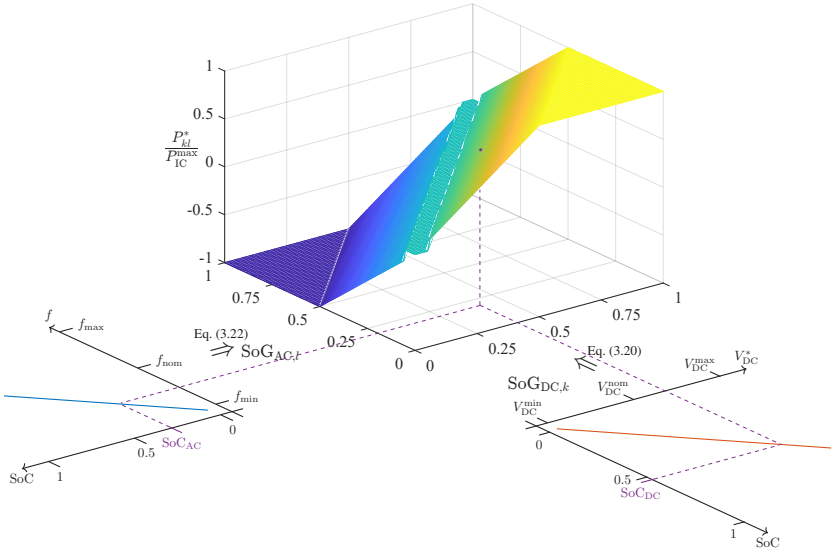


Figure 3.9: SoG-based coupling function: three-dimensional mapping from $\mathrm{SoG}_{\mathrm{DC}}$ and $\mathrm{SoG}_{\mathrm{AC}}$ to the normalized power reference $P^*_{kl}/P^{\max}_{\mathrm{IC}}$. A high $\mathrm{SoG}_{\mathrm{DC}}$ combined with a low $\mathrm{SoG}_{\mathrm{AC}}$ results in DC/AC export (yellow surface region), whereas a low $\mathrm{SoG}_{\mathrm{DC}}$ with a high $\mathrm{SoG}_{\mathrm{AC}}$ leads to AC/DC import (blue surface region).

3.5 Stability Analysis of the SoG-Based Control Scheme

This section establishes the local exponential stability of the closed-loop SoG-based control system using Singular Perturbation Theory. The analysis follows Theorem A.8.1 in Appendix A.8, which is aligned with the structure of Theorem 11.4 in [72].

The closed-loop dynamics are first reformulated as an equilibrium-shifted nonlinear state-space model that incorporates the local control laws. By scaling the proportional and integral gains of the embedded PI voltage controller with a small parameter $\varepsilon > 0$, the system is cast into a standard singularly perturbed form with explicitly separated time scales.

Following the procedure in Theorem A.8.1, the proof proceeds by decomposing the dynamics into a reduced-order (slow) subsystem and a boundary-layer (fast) subsystem. Regularity of the slow manifold is verified, and local exponential stability of the reduced subsystem is demonstrated using Lyapunov theory. To obtain dimensionally consistent design conditions, a per-unit normalization with respect to the equilibrium DC-link voltage is introduced later in this section. Uniform exponential stability of the fast subsystem about the slow manifold is established by a separate Lyapunov estimate. Altogether, the five technical conditions required by the Singular Perturbation Theorem are verified.

In addition, structural properties of the physical system imply forward invariance of a compact, physically admissible domain. In particular, saturating integrators enforce bounded SoC trajectories, and the DC-link voltage remains strictly positive, which guarantees that all closed-loop signals are well-defined[4]. As a consequence, the equilibrium is semiglobal.

[4] In this context, the term “well-defined” indicates that all closed-loop quantities and associated mappings are single-valued and finite over the domain of interest, such that no singularities or ambiguities arise [145].

3.5.1 System Modeling and State-Space Representation

To analyze the dynamic behavior of the DC microgrid, a reduced-order equivalent circuit model is employed, as depicted in Figure 3.10. The model retains the components and couplings that are essential for control and stability analysis.

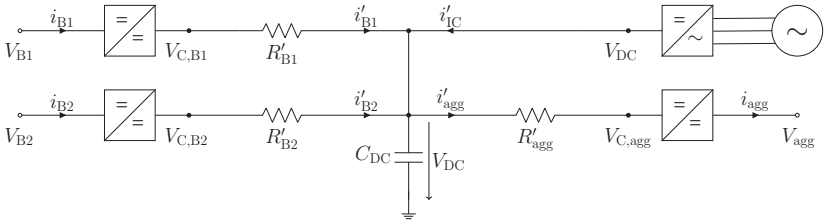


Figure 3.10: Reduced equivalent circuit of the considered DC microgrid, comprising two BESS units and a bidirectional IC. The combined influence of PV generation and local demand is modeled by an aggregated current source i'_{agg}. Adapted from [J1].

Each BESS unit $i \in \{1, 2\}$ is interfaced to the common DC-link capacitor C_{DC} through its own bidirectional DC–DC converter. The converters regulate the branch output voltages $V_{\mathrm{C,B}i}$ relative to the DC-link voltage V_{DC}. The DC microgrid is interconnected with the AC side via a bidirectional IC that controls the power exchange.

On the DC side, the PV generation and local demand is represented by an aggregated current source i'_{agg}, defined as

$$i'_{\mathrm{agg}} = i_{\mathrm{Ld}} - i_{\mathrm{PV}}, \tag{3.28}$$

where i_{PV} denotes the aggregated current generated by the PV subsystems and i_{Ld} the current drawn by local loads. This abstraction captures the net current injection into the DC-bus and reflects the dynamic behavior of prosumers. A positive i'_{agg} corresponds to load-dominant conditions, while a negative value indicates net power injection from the PV subsystems.

Applying Kirchhoff's laws and incorporating the Coulomb Counting approach (see Section 2.2.2) for modeling the SoC and the DC-bus voltage dynamics, the following nonlinear differential equation system is obtained:

$$\frac{d}{dt}\mathrm{SoC}_i = -\frac{1}{Q_{\mathrm{B}i}}\left(\frac{V_{\mathrm{C,B}i} - V_{\mathrm{DC}}}{R'_{\mathrm{B}i}}\right)\frac{V_{\mathrm{C,B}i}}{V_{\mathrm{B}i}}, \quad i \in \{1,2\}, \tag{3.29a}$$

$$\frac{d}{dt}V_{\mathrm{DC}} = \frac{1}{C_{\mathrm{DC}}}\left(\frac{V_{\mathrm{C,B1}} - V_{\mathrm{DC}}}{R'_{\mathrm{B1}}} + \frac{V_{\mathrm{C,B2}} - V_{\mathrm{DC}}}{R'_{\mathrm{B2}}} - i'_{\mathrm{agg}} + i'_{\mathrm{IC}}\right), \tag{3.29b}$$

where $Q_{\mathrm{B}i}$ denotes the nominal capacity of battery i, $V_{\mathrm{B}i}$ its open-circuit voltage, $V_{\mathrm{C,B}i}$ the capacitor voltage in the equivalent circuit, and $R'_{\mathrm{B}i}$ the corresponding resistance parameter. Furthermore, C_{DC} is the DC-link capacitance, and i'_{IC} the IC current injected into the DC-bus.

Assuming a stiff AC grid[5] at the PCC and operation at nominal frequency, that is $f_l \equiv f^*_{\mathrm{AC}}$, the AC-side inverse mapping in (3.22) yields $\mathrm{SoG}_{\mathrm{AC},l} = \mathrm{SoG}^*_{\mathrm{AC},l}$. Together with the DC-side inverse mapping (3.20) and the setpoint alignment $\mathrm{SoG}^*_{\mathrm{DC},i} = \mathrm{SoG}^*_{\mathrm{AC},l}$, the SoG mismatch is reduced to

$$\Delta\mathrm{SoG}_{kl} = \frac{\mathrm{SoG}_{\Delta,k}}{\sigma}\left(\frac{V_{\mathrm{DC}}}{V^*_{\mathrm{DC}}} - 1\right). \tag{3.30}$$

Neglecting deadband and saturation effects, the SoG-based PI power reference (3.25) is given by

$$P_{kl}(t) = k_p\left(V_{\mathrm{DC}}(t) - V^*_{\mathrm{DC}}\right) + k_i\int_{t_0}^{t}\left(V_{\mathrm{DC}}(\tau) - V^*_{\mathrm{DC}}\right)d\tau, \tag{3.31}$$

with

$$k_p = K_P\,\frac{\mathrm{SoG}_{\Delta,k}}{\sigma V^*_{\mathrm{DC}}}, \qquad k_i = K_I\,\frac{\mathrm{SoG}_{\Delta,k}}{\sigma V^*_{\mathrm{DC}}}. \tag{3.32}$$

[5] A stiff AC grid implies that voltage and frequency remain essentially constant, which represents a strong grid with negligible internal impedance [146].

Hence, the control law is reduced to the standard form of a PI controller acting on the DC-link voltage deviation e_v. The corresponding IC current is

$$i'_{\mathrm{IC}}(t) = -\frac{P_{kl}(t)}{V_{\mathrm{DC}}(t)}. \tag{3.33}$$

Equations (3.29a) and (3.29b) constitute the nonlinear physical model that forms the basis for the subsequent control-oriented reformulation.

Before introducing the control-theoretic notation and variable mappings, the following standing assumptions are made to ensure physical validity and to streamline the stability analysis.

3.5.1.1 Standing Assumptions

The following assumptions are introduced to ensure model validity and to establish the mathematical consistency required for the stability analysis.

Assumption 3.4 (Strictly positive DC-bus voltage). *For all $t \geq 0$, the following condition holds:*

$$V_{\mathrm{DC}}(t) > 0. \tag{3.34}$$

This assumption ensures that the DC-link voltage remains strictly positive at all times. It preserves the physical validity of the model and guarantees that the control input $u_3 = P_{kl}/V_{\mathrm{DC}}$ is well-defined.

In practice, Assumption 3.4 is inherently satisfied due to the structural properties of the converters and the unidirectional current conduction enforced by the freewheeling diodes (see Figure 2.1). When all active switches are turned off, the diodes maintain a current path toward the DC-bus, ensuring that the DC-bus voltage cannot fall below the minimum voltage of the connected sources. Neglecting the small forward voltage drop of the diodes (typically about $0.7\,\mathrm{V}$),

the DC-link voltage is bounded from below by the smallest source voltage at any time:

$$V_{\mathrm{DC}}(t) \geq \min\big(V_{\mathrm{B1}}(t),\, V_{\mathrm{B2}}(t),\, V_{\mathrm{PV}}(t),\, V_{\mathrm{AC}}(t)\big) > 0, \quad \forall t \geq 0. \tag{3.35}$$

This inherent property of the system guarantees that $V_{\mathrm{DC}}(t) > 0$ under all realistic operating conditions, provided that at least one of the sources (e.g. BESSs, PV, or AC grid) remains energized. The trivial case where all sources and the AC grid are simultaneously disconnected or de-energized is excluded, since stability analysis in such a scenario would be meaningless and falls outside the practical operating domain of the system.

Assumption 3.5 (Bounded SoC). *Each battery SoC remains within a physically meaningful range:*

$$\mathrm{SoC}_i(t) \in [\underline{\mathrm{SoC}}_i,\, \overline{\mathrm{SoC}}_i] \subseteq [0, 1]. \tag{3.36}$$

This assumption prevents overcharging or deep discharge of the storage units.

To enforce this boundedness, a saturating integrator is embedded into the SoC dynamics, following the method proposed in [147]. Concretely, the dynamics of SoC_i are modified to:

$$\frac{d}{dt}\mathrm{SoC}_i = \mathscr{S}(\mathrm{SoC}_i, i_{\mathrm{B}i}), \quad \text{for } i \in \{1, 2\}, \tag{3.37}$$

where p denotes the nominal input signal, and $\mathscr{S}(x, p)$ is defined as

$$\mathscr{S}(\mathrm{SoC}_i, i_{\mathrm{B}i}) = \begin{cases} \max\{0, i_{\mathrm{B}i}\}, & \mathrm{SoC}_i \leq \underline{\mathrm{SoC}}_i, \\ i_{\mathrm{B}i}, & \mathrm{SoC}_i \in (\underline{\mathrm{SoC}}_i, \overline{\mathrm{SoC}}_i), \\ \min\{0, i_{\mathrm{B}i}\}, & \mathrm{SoC}_i \geq \overline{\mathrm{SoC}}_i. \end{cases} \tag{3.38}$$

At the lower boundary ($\mathrm{SoC}_i \leq \underline{\mathrm{SoC}}_i$), the saturating integrator uses $\max\{0, i_{B,i}\}$, which zeroes negative inputs and thus prevents further decrease below $\underline{\mathrm{SoC}}_i$. At

the upper boundary ($\mathrm{SoC}_i \geq \overline{\mathrm{SoC}}_i$) it uses $\min\{0, i_{\mathrm{B}i}\}$, which zeroes positive inputs and thus prevents exceeding $\overline{\mathrm{SoC}}_i$. Inside the interval, the integrator evolves according to $\frac{d}{dt}\mathrm{SoC}_i = i_{\mathrm{B}i}$.

This modification ensures that the SoC trajectories remain confined to the physically meaningful domain $[\underline{\mathrm{SoC}}, \overline{\mathrm{SoC}}]$ at all times while preserving the stability properties of the singularly perturbed closed-loop system, as shown in [147].

Although the SoC dynamics are implemented with a saturating integrator to enforce boundedness, the saturation limits do not correspond to valid equilibrium points. As shown in (3.46) and (3.41), the steady-state condition $u_i = x_3^e$ implies $\mathrm{SoC}_i = \mathrm{SoC}_i^*$, which lies strictly within the admissible range.

At the boundaries, the integrator halts further excursions but cannot maintain a steady-state. The stability analysis therefore focuses on the unsaturated dynamics, which govern the relevant local behavior.

In the next step, the control laws are embedded and the dynamics are transformed into an equilibrium-shifted state-space representation with explicitly separated time scales, which enables the singular perturbation analysis.

3.5.1.2 Transformation into a Control-Oriented Structure

To facilitate analysis and controller embedding, the physical model is reformulated in control-oriented notation. The state vector is defined as $x := [x_1,\, x_2,\, x_3,\, x_4]^\top$, where x_1 and x_2 denote the normalized SoC of the two BESS units (dimensionless), x_3 is the DC-link voltage, and $x_4 \equiv \xi$ is the PI integrator state of the DC-link voltage error. The control inputs are $u := [u_1,\, u_2,\, u_3]^\top$, where u_1 and u_2 are the controlled output voltages of the two bidirectional DC–DC converters ($V_{\mathrm{C,B1}}$ and $V_{\mathrm{C,B2}}$), and $u_3 \equiv P_{kl}$ is the active power setpoint of the IC. Consistent with (3.40b), the sign convention is such that $u_3 > 0$ extracts power from the DC-bus (DC→AC), which enters as the negative current

term $-u_3/x_3$ in (3.40b). The disturbance is defined as $z_1 := i'_{\mathrm{agg}}$. The admissible domain defined by Assumption 3.4 and Assumption 3.5 implies $x_3 > 0$ (cf. Equation (3.34)) and bounded SoC states $x_i \in [\underline{x}_i,\, \overline{x}_i] \subset (0, 1)$ (cf. (3.36)) for $i \in \{1, 2\}$, ensuring the well-posedness of all control and system equations within the physical operating range.

An overview of the mapping between physical quantities and control-theoretic variables is given in Table 3.2.

Table 3.2: Mapping of physical quantities to control-theoretic variables.

Variable Type	Physical Notation	Control-Theoretic Notation	Operating Range
State Variables	$\mathrm{SoC}_{1,2}$	$x_{1,2}$	$[0, 1]$
	V_{DC}	x_3	$\mathbb{R}^+ \setminus \{0\}$
	ξ	x_4	$\mathbb{R}$
Control Inputs	$V_{\mathrm{C,B1}}, V_{\mathrm{C,B2}}$	$u_{1,2}$	$x_3^*[1-\sigma,\, 1+\sigma]$
	P_{kl}	u_3	$[-P_{\mathrm{IC}}^{\max},\, P_{\mathrm{IC}}^{\max}]$
Disturbance	i'_{agg}	z_1	$[-i_{\mathrm{PV}}^{\max},\, i_{\mathrm{Ld}}^{\max}]$

With the shorthand notation

$$\alpha_i := \frac{1}{Q_{\mathrm{B}i} R'_{\mathrm{B}i} V_{\mathrm{B}i}}, \qquad i \in \{1, 2\}, \tag{3.39}$$

the closed-loop dynamics take the compact form

$$\dot{x}_i = -\alpha_i \big(u_i^2 - u_i x_3\big), \qquad i \in \{1, 2\}, \tag{3.40a}$$

$$\dot{x}_3 = \frac{1}{C_{\mathrm{DC}}} \left(\frac{u_1 - x_3}{R'_{\mathrm{B1}}} + \frac{u_2 - x_3}{R'_{\mathrm{B2}}} - \frac{u_3}{x_3} - z_1 \right), \tag{3.40b}$$

$$\dot{x}_4 = x_3 - x_3^*. \tag{3.40c}$$

The term u_3/x_3 is the IC current contribution and is well-defined on the admissible domain $x_3 > 0$ (cf. Assumption 3.4).

The SoG-based voltage references for the battery-side converters are implemented as (cf. Equation 3.8):

$$u_i = x_3^e \left(1 + \sigma \frac{x_i - x_i^*}{\mathrm{SoC}_{\Delta,i}}\right), \qquad i \in \{1, 2\}, \tag{3.41}$$

where $x_3^{\mathrm{e}} = x_3^*$ is the equilibrium DC-link voltage, whose derivation is given later in this section, $\sigma \in (0, 1)$ a global mapping gain, and $\mathrm{SoC}_{\Delta,i} \in (0, 1]$ a normalization factor. Choosing the constant scale x_3^{e} (rather than the instantaneous x_3) avoids multiplicative couplings in (3.40) and simplifies the subsequent stability analysis.

The IC controls the DC-link voltage using a local PI controller, given by

$$u_3 = k_p(x_3 - x_3^*) + k_i x_4, \tag{3.42}$$

which corresponds to the SoG-based power control law given in (3.31).

Equations (3.40)–(3.42) describe the embedded closed-loop dynamics in a compact form that facilitates controller embedding and subsequent analysis. In the next step, the equilibrium point is explicitly characterized and the system is reformulated in deviation coordinates around this equilibrium.

3.5.1.3 Equilibrium Point

To determine the equilibrium operating point of the system, the time derivatives in the nonlinear state-space model are set to zero. This yields a set of algebraic equations that describe the steady-state behavior of the system. The control laws used for this analysis correspond to Equations (3.41) and (3.42), where the control inputs are explicitly expressed as functions of the system states.

The steady-state condition of the integrator state in Equation (3.40c) yields

$$\dot{x}_4 = x_3^e - x_3^* = 0 \quad \Rightarrow \quad x_3^e = x_3^*, \tag{3.43}$$

which implies that the steady-state output of the PI controller defined in Equation (3.42) is simplified to

$$u_3^e = (k_p(x_3^e - x_3^*) + k_i x_4^e) = k_i x_4^e \quad \Rightarrow \quad x_4^e = \frac{u_3^e}{k_i}. \tag{3.44}$$

For the battery states x_1 and x_2, the steady-state of the nonlinear dynamics yields

$$\dot{x}_i = -\alpha_i \, u_i \, (u_i - x_3^e) = 0 \quad \Rightarrow \quad u_i \in \{0,\, x_3^e\}, \qquad i \in \{1, 2\}. \tag{3.45}$$

The candidate $u_i = 0$ is inadmissible because the input is restricted to the operating range $u_i \in V_{DC}^*[\,1-\sigma,\, 1+\sigma\,] \subset \mathbb{R}_{>0}$ (see Tab. 3.2), hence $u_i \neq 0$ and necessarily

$$u_i = x_3^e, \qquad i \in \{1, 2\}. \tag{3.46}$$

Substituting this into the SoC control law (3.41) yields the steady-state condition:

$$u_i = x_3^e \left(1 + \sigma \frac{x_i^e - x_i^*}{\mathrm{SoC}_{\Delta,i}}\right) = x_3^e, \tag{3.47}$$

$$\Rightarrow \quad \frac{x_i^e - x_i^*}{\mathrm{SoC}_{\Delta,i}} = 0 \quad \Rightarrow \quad x_i^e = x_i^*, \qquad i \in \{1, 2\}. \tag{3.48}$$

For the voltage dynamics, the steady-state condition of Equation (3.40b) reads:

$$\dot{x}_3 = \frac{1}{C_{\mathrm{DC}}} \left(\frac{u_1 - x_3}{R'_{\mathrm{B1}}} + \frac{u_2 - x_3}{R'_{\mathrm{B2}}} - \frac{u_3}{x_3} - z_1 \right) = 0. \tag{3.49}$$

With (3.43) and (3.47), this simplifies to:

$$\frac{1}{C_{\mathrm{DC}}}\left(-\frac{u_3^e}{x_3^e}-z_1\right)=0 \quad \Rightarrow \quad u_3^e=-z_1 x_3^e. \tag{3.50}$$

Substituting this into Equation (3.44) yields the equilibrium value of the integral state:

$$x_4^e=-\frac{z_1 x_3^e}{k_i}. \tag{3.51}$$

Based on the previous derivation, the equilibrium point of the closed-loop system is given by:

$$\begin{aligned} &x_1^e=x_1^*, \quad x_2^e=x_2^*, \quad x_3^e=x_3^*, \\ &x_4^e=-\frac{z_1 x_3^e}{k_i}, \quad u_1^e=u_2^e=x_3^e, \quad u_3^e=-z_1 x_3^e. \end{aligned} \tag{3.52}$$

This equilibrium is fully defined by the reference values of the SoC variables (x_1^*, x_2^*) and the voltage setpoint x_3^*. The integral state x_4^e compensates for the constant disturbance z_1 through the PI control action, thereby ensuring that the DC-link voltage remains regulated at the desired level. The converters outputs u_1 and u_2 match the steady-state voltage, while u_3 represents the power required from the IC to balance the aggregated DC-side load.

3.5.1.4 Coordinate Transformation and Reformulation in Error Coordinates

In preparation for the singular perturbation analysis, the nonlinear closed-loop system is reformulated around the previously derived equilibrium point (3.52).

The system is reformulated by introducing the error coordinates

$$\tilde{x}_i(t) := x_i(t) - x_i^e, \tag{3.53}$$

where $\tilde{x} = (\tilde{x}_1,\, \tilde{x}_2,\, \tilde{x}_3,\, \tilde{x}_4)^\top$ denotes the vector of state errors from equilibrium.

Substituting the error variables into the control laws (3.41) and (3.42) yields:

$$u_i = x_3^{\mathrm{e}} + \beta_i\, \tilde{x}_i, \qquad \beta_i := \frac{\sigma\, x_3^{\mathrm{e}}}{\mathrm{SoC}_{\Delta,i}}, \qquad i \in \{1, 2\}, \tag{3.54a}$$

$$u_3 = u_3^{\mathrm{e}} + k_p\, \tilde{x}_3 + k_i\, \tilde{x}_4, \qquad u_3^{\mathrm{e}} = -z_1\, x_3^{\mathrm{e}}. \tag{3.54b}$$

Substituting (3.54a)–(3.54b) into (3.40) and subtracting the equilibrium relations in (3.52)

$$\dot{\tilde{x}}_1 = -\alpha_1 \left[\left(x_3^e + \beta_1 \tilde{x}_1\right)^2 - \left(x_3^e + \beta_1 \tilde{x}_1\right) \left(\tilde{x}_3 + x_3^e\right) \right], \tag{3.55a}$$

$$\dot{\tilde{x}}_2 = -\alpha_2 \left[\left(x_3^e + \beta_2 \tilde{x}_2\right)^2 - \left(x_3^e + \beta_2 \tilde{x}_2\right) \left(\tilde{x}_3 + x_3^e\right) \right], \tag{3.55b}$$

$$\dot{\tilde{x}}_3 = \frac{1}{C_{\mathrm{DC}}} \left[\frac{\beta_1 \tilde{x}_1 - \tilde{x}_3}{R'_{B1}} + \frac{\beta_2 \tilde{x}_2 - \tilde{x}_3}{R'_{B2}} - \frac{k_p \tilde{x}_3 + k_i \tilde{x}_4}{x_3^e + \tilde{x}_3} - z_1\, \frac{\tilde{x}_3}{x_3^e + \tilde{x}_3} \right], \tag{3.55c}$$

$$\dot{\tilde{x}}_4 = \tilde{x}_3. \tag{3.55d}$$

This transformed system in error coordinates serves as the basis for the subsequent singular perturbation-based stability analysis. It enables a structured decomposition into slow and fast subsystems and facilitates the application of the Lyapunov-based proof techniques discussed in Section 3.5.2.

3.5.2 Stability Analysis Using Singular Perturbation Theory

This section analyzes the stability of the shifted nonlinear system using Singular Perturbation Theory. The method follows the structure of Theorem 11.4 in [72],

which provides sufficient conditions for the exponential stability of singularly perturbed systems.

3.5.2.1 Time-Scale Separation and System Transformation

To express the system in singularly perturbed form, the proportional and integral gains of the embedded PI controller are scaled with the small parameter $\varepsilon > 0$ [148, 149]. The gain parameters are defined as

$$k_p = \frac{\bar{k}_p}{\varepsilon}, \qquad k_i = \frac{\bar{k}_i}{\varepsilon}, \qquad \bar{k}_p > 0,\ \bar{k}_i > 0, \tag{3.56}$$

where $\bar{k}_p$ and $\bar{k}_i$ are arbitrary positive design constants. This scaling requires the controller gains to increase on the order of $1/\varepsilon$, without implying identical magnitudes. Since the subsequent derivations and stability conditions hold for arbitrary $\bar{k}_p, \bar{k}_i > 0$, the analysis is restricted to the representative case $\bar{k}_p = \bar{k}_i = 1$, which simplifies the notation without loss of generality.

Substituting these expressions into the dynamics of $\dot{\tilde{x}}_3$ yields

$$\varepsilon\dot{\tilde{x}}_3 = \frac{1}{C_{\mathrm{DC}}}\left[\varepsilon\left(\frac{\beta_1\tilde{x}_1 - \tilde{x}_3}{R'_{\mathrm{B1}}} + \frac{\beta_2\tilde{x}_2 - \tilde{x}_3}{R'_{\mathrm{B2}}} - z_1\,\frac{\tilde{x}_3}{x_3^e + \tilde{x}_3}\right) - \frac{\tilde{x}_3 + \tilde{x}_4}{\tilde{x}_3 + x_3^e}\right]. \tag{3.57}$$

Introducing the substitution $x_{\mathrm{f}} := \tilde{x}_3$, the fast subsystem can be expressed as

$$\begin{aligned}\varepsilon\dot{x}_{\mathrm{f}} &= g(x_{\mathrm{f}}, \tilde{x}) \\ &= \frac{1}{C_{\mathrm{DC}}}\left[\varepsilon\left(\frac{\beta_1\tilde{x}_1 - x_{\mathrm{f}}}{R'_{\mathrm{B1}}} + \frac{\beta_2\tilde{x}_2 - x_{\mathrm{f}}}{R'_{\mathrm{B2}}} - z_1\,\frac{x_{\mathrm{f}}}{x_3^e + x_{\mathrm{f}}}\right) - \frac{x_{\mathrm{f}} + \tilde{x}_4}{x_{\mathrm{f}} + x_3^e}\right].\end{aligned} \tag{3.58}$$

3.5.2.2 Reduced (Slow) Subsystem

In the singular perturbation limit $\varepsilon \to 0$, the fast dynamics are assumed to settle instantaneously, leading to the algebraic constraint

$$0 = g(x_{\mathrm{f}}, \tilde{x}) = -\frac{1}{C_{\mathrm{DC}}} \left[\frac{x_{\mathrm{f}} + \tilde{x}_4}{x_{\mathrm{f}} + x_3^e} \right], \tag{3.59}$$

which implicitly defines the so-called slow manifold. For the considered system, this condition yields

$$x_{\mathrm{f}} = h(\tilde{x}) = -\tilde{x}_4. \tag{3.60}$$

The manifold is well-defined and smooth locally for $|\tilde{x}_4| < x_3^{\mathrm{e}}$, which keeps the denominator $x_{\mathrm{f}} + x_3^{\mathrm{e}}$ bounded away from zero. Moreover,

$$\frac{\partial g}{\partial x_{\mathrm{f}}}\Big|_{x_{\mathrm{f}} = -\tilde{x}_4} = -\frac{1}{C_{\mathrm{DC}}\,(x_3^{\mathrm{e}} - \tilde{x}_4)} \;\neq\; 0, \tag{3.61}$$

so the Implicit Function Theorem[6] ensures that $h(\tilde{x})$ is unique and continuously differentiable in a neighborhood of the origin. This ensures that the slow manifold is well-defined and smooth, thereby satisfying the regularity condition ($\mathcal{C}2$) required by the Singular Perturbation Theorem.

Substituting the slow manifold into the remaining subsystem equations yields the reduced-order system:

$$\dot{\tilde{x}}_1 = -\alpha_1 \left(x_3^e + \beta_1 \tilde{x}_1\right) \left(\beta_1 \tilde{x}_1 + \tilde{x}_4\right), \tag{3.62a}$$

$$\dot{\tilde{x}}_2 = -\alpha_2 \left(x_3^e + \beta_2 \tilde{x}_2\right) \left(\beta_2 \tilde{x}_2 + \tilde{x}_4\right), \tag{3.62b}$$

$$\dot{\tilde{x}}_4 = -\tilde{x}_4. \tag{3.62c}$$

[6] The Implicit Function Theorem ensures the existence and differentiability of $h(\tilde{x})$ locally, provided $\partial g / \partial x_f \neq 0$ (see, e.g., [150, p.223ff]).

This reduced system characterizes the slow dynamics on the invariant manifold and provides the basis for the subsequent stability analysis. System (3.62) admits algebraic fixed points at $\tilde{x}_4 = 0$ and $\tilde{x}_i \in \{0, -x_3^e/\beta_i\}$ for $i \in \{1, 2\}$. These points represent candidate equilibria of the reduced system; however, only those within the admissible operating region defined by Assumption 3.4 and Assumption 3.5 are feasible.

The case $\tilde{x}_i = -x_3^e/\beta_i$ with $\beta_i = \sigma x_3^e/\mathrm{SoC}_{\Delta,i} > 0$ leads to

$$-\frac{x_3^e}{\beta_i} = -\frac{\mathrm{SoC}_{\Delta,i}}{\sigma}. \tag{3.63}$$

Since $\sigma \in (0, 1)$, it follows that $|\tilde{x}_i| > \mathrm{SoC}_{\Delta,i}$, which violates the SoC domain constraints. Hence, these equilibria lie outside the admissible region and are excluded from the analysis.

Second, note that the condition $x_3^e + \beta_i \tilde{x}_i = 0$ leads to vanishing input $u_i = 0$, which contradicts the input admissibility condition $u_i \in x_3^e[1 - \sigma,\ 1 + \sigma] \subset \mathbb{R}_{>0}$. Thus, these points are likewise infeasible.

As a result, the only equilibrium point of system (3.62) within the admissible operating region is the origin, i.e., $\tilde{x}_1 = \tilde{x}_2 = \tilde{x}_4 = 0$. The subsequent stability analysis will therefore focus exclusively on this operating point.

3.5.2.3 Stability of the Reduced (Slow) Subsystem

The stability of the reduced system is examined using the quadratic Lyapunov function candidate

$$V(\tilde{x}_1, \tilde{x}_2, \tilde{x}_4) = \frac{1}{2}\tilde{x}_1^2 + \frac{1}{2}\tilde{x}_2^2 + \frac{\vartheta}{2}\tilde{x}_4^2, \tag{3.64}$$

where $\vartheta > 0$ is a positive weighting parameter. The analysis is carried out in the domain

$$\mathcal{D} := \left\{ (\tilde{x}_1, \tilde{x}_2, \tilde{x}_4) \in \mathbb{R}^3 \,\middle|\, |\tilde{x}_1| < 1,\ |\tilde{x}_2| < 1 \right\}. \tag{3.65}$$

The time derivative of V along the trajectories of the reduced system yields

$$\begin{aligned}\dot{V} = &-\alpha_1 \left[x_3^{\mathrm{e}}\beta_1\tilde{x}_1^2 + x_3^{\mathrm{e}}\tilde{x}_1\tilde{x}_4 + \beta_1^2\tilde{x}_1^3 + \beta_1\tilde{x}_1^2\tilde{x}_4\right] \\ &-\alpha_2 \left[x_3^{\mathrm{e}}\beta_2\tilde{x}_2^2 + x_3^{\mathrm{e}}\tilde{x}_2\tilde{x}_4 + \beta_2^2\tilde{x}_2^3 + \beta_2\tilde{x}_2^2\tilde{x}_4\right] - \vartheta\tilde{x}_4^2. \end{aligned} \tag{3.66}$$

On the domain $\mathcal{D}$ (where $|\tilde{x}_i| < 1$ for $i \in \{1, 2\}$), the SoC-error monomials are dominated by their quadratic terms. In particular, for $i \in \{1, 2\}$,

$$|\tilde{x}_i|^3 \leq |\tilde{x}_i|^2, \qquad |\tilde{x}_i|^4 \leq |\tilde{x}_i|^2, \tag{3.67}$$

which follows from the elementary inequality $|r|^m \leq |r|^n$ for $|r| \leq 1$ and $m \geq n$.

To obtain a dimensionless representation of the design conditions and to make the dependence on the mapping gain explicit, the analysis introduces the following per-unit variables:

$$\bar{x}_4 := \frac{\tilde{x}_4}{x_3^{\mathrm{e}}}, \qquad \bar{\beta}_i := \frac{\beta_i}{x_3^{\mathrm{e}}} = \frac{\sigma}{\mathrm{SoC}_{\Delta,i}}, \qquad i \in \{1, 2\}, \tag{3.68}$$

Substituting $\beta_i = x_3^{\mathrm{e}}\bar{\beta}_i$ and $\tilde{x}_4 = x_3^{\mathrm{e}}\bar{x}_4$ into the reduced system (3.62) yields

$$\dot{\tilde{x}}_i = -\alpha_i \left(x_3^{\mathrm{e}}\right)^2 \left(1 + \bar{\beta}_i\tilde{x}_i\right)\left(\bar{\beta}_i\tilde{x}_i + \bar{x}_4\right), \qquad i \in \{1, 2\}, \tag{3.69}$$

$$\dot{\bar{x}}_4 = -\bar{x}_4, \tag{3.70}$$

The Lyapunov function employed for the reduced system is

$$V(\tilde{x}_1, \tilde{x}_2, \bar{x}_4) = \tfrac{1}{2}\tilde{x}_1^2 + \tfrac{1}{2}\tilde{x}_2^2 + \tfrac{\vartheta}{2}\bar{x}_4^2, \tag{3.71}$$

for which $\dot{\bar{x}}_4 = -\bar{x}_4$ on the slow manifold.

The mixed terms involving $\tilde{x}_i\bar{x}_4$ and $\tilde{x}_i^2\bar{x}_4$ are bounded using Young's inequality

$$|\tilde{x}_i\bar{x}_4| \leq \frac{1}{2\delta_i}\,\tilde{x}_i^2 + \frac{\delta_i}{2}\,\bar{x}_4^2, \tag{3.72}$$

$$|\tilde{x}_i^2\bar{x}_4| \leq \frac{1}{2\delta_i'}\,\tilde{x}_i^4 + \frac{\delta_i'}{2}\,\bar{x}_4^2. \tag{3.73}$$

On $\mathcal{D}$, the inequality $|\tilde{x}_i| < 1$ for $i = 1, 2$ implies $|\tilde{x}_i|^3 \leq \tilde{x}_i^2$ and $|\tilde{x}_i|^4 \leq \tilde{x}_i^2$. Substituting these bounds into $\dot{V}$ yields

$$\begin{aligned}\dot{V} \leq\ & -\ \alpha_1(x_3^{\mathrm{e}})^2\left(\bar{\beta}_1 - \frac{1}{2\delta_1} - \frac{\bar{\beta}_1}{2\delta_1'} - \bar{\beta}_1^2\right)\tilde{x}_1^2 \\ & -\ \alpha_2(x_3^{\mathrm{e}})^2\left(\bar{\beta}_2 - \frac{1}{2\delta_2} - \frac{\bar{\beta}_2}{2\delta_2'} - \bar{\beta}_2^2\right)\tilde{x}_2^2 \\ & -\ \left[\vartheta - \alpha_1(x_3^{\mathrm{e}})^2\left(\frac{\delta_1}{2} + \frac{\bar{\beta}_1\delta_1'}{2}\right) - \alpha_2(x_3^{\mathrm{e}})^2\left(\frac{\delta_2}{2} + \frac{\bar{\beta}_2\delta_2'}{2}\right)\right]\bar{x}_4^2. \end{aligned} \tag{3.74}$$

The balancing parameters are selected as

$$\delta_i = \frac{2}{\bar{\beta}_i}, \qquad \delta_i' = \frac{1}{\bar{\beta}_i}. \tag{3.75}$$

Conditions for all coefficient brackets in (3.74) to be strictly positive reduce to

$$\bar{\beta}_i - \frac{1}{2\delta_i} - \frac{\bar{\beta}_i}{2\delta_i'} - \bar{\beta}_i^2 = \frac{3}{4}\,\bar{\beta}_i\,(1 - 2\bar{\beta}_i), \tag{3.76}$$

which are strictly positive whenever

$$0 < \bar{\beta}_i < \tfrac{1}{2} \quad\Longleftrightarrow\quad 0 < \sigma < \tfrac{1}{2}\,\mathrm{SoC}_{\Delta,i}. \tag{3.77}$$

With the same choice of δ_i, δ_i', the $\bar{x}_4^2$ coefficient is positive if

$$\vartheta > \ (x_3^{\mathrm{e}})^2\left[\alpha_1\left(\frac{1}{\bar{\beta}_1} + \frac{1}{2}\right) + \alpha_2\left(\frac{1}{\bar{\beta}_2} + \frac{1}{2}\right)\right] + \varepsilon, \quad \varepsilon > 0. \tag{3.78}$$

Based on (3.77)–(3.78), the derivative $\dot{V}$ is strictly negative on $\mathcal{D}$, which implies asymptotic stability of the reduced system within the operation region $\mathcal{D}$. Moreover, the Lyapunov candidate V is a positive definite quadratic function and, under the same coefficient conditions, its time derivative admits the bound

$$\dot{V} \leq -\varrho V, \quad \text{for some } \varrho > 0 \text{ and all } (\tilde{x}_1, \tilde{x}_2, \bar{x}_4) \in \mathcal{D}. \tag{3.79}$$

This inequality confirms exponential stability of the equilibrium within the admissible domain $\mathcal{D}$. In the symmetric case $\mathrm{SoC}_i^* = 0.5$, the admissible half-range becomes $\mathrm{SoC}_{\Delta,i} = 0.5$. Substitution into (3.77) yields

$$\sigma < 0.25, \tag{3.80}$$

which corresponds to a maximum permissible voltage deviation of $25\,\%$.

Remark (Semiglobal stability within the admissible domain). *While the stability analysis is formally restricted to the admissible domain $\mathcal{D}$, the use of a saturating integrator ensures that all trajectories remain confined within $\mathcal{D}$ for all $t \geq 0$, as explained in Assumption 3.5. Hence, the equilibrium is semiglobally exponential stable within the physically meaningful operating range.*

3.5.2.4 Stability of the Boundary-Layer (Fast) Subsystem

In the context of Singular Perturbation Theory, the fast subsystem describes the boundary-layer dynamics that evolve on the fast time scale $\tau = t/\varepsilon$. Its stability around the slow manifold is a crucial condition for the overall stability of the singularly perturbed system.

Introducing the stretched time variable $\tau = t/\varepsilon$, the fast subsystem dynamics take the form

$$\frac{dx_\mathrm{f}}{d\tau} = -\frac{1}{C_\mathrm{DC}} \frac{x_\mathrm{f} + \tilde{x}_4}{x_\mathrm{f} + x_3^\mathrm{e}}, \tag{3.81}$$

where $x_\mathrm{f} := \tilde{x}_3$ denotes the fast state, and $\tilde{x}_4$ is treated as a constant parameter on the fast time scale.

Assumption 3.6 (Bounded deviation from the equilibrium). *There exists a small positive constant $\delta > 0$ such that the fast state satisfies $|x_{\mathrm{f}}| \leq \delta \ll x_3^e$. This ensures that $x_{\mathrm{f}} + x_3^e > 0$ at all times, preserving the physical validity of the system and guaranteeing that the denominator in* (3.81) *remains positive.*

To analyze the stability of the equilibrium point $x_{\mathrm{f}} = -\tilde{x}_4$, the following Lyapunov candidate function is considered:

$$V(x_{\mathrm{f}}) = \frac{1}{2}\big(x_{\mathrm{f}} + \tilde{x}_4\big)^2. \tag{3.82}$$

This function is positive definite with respect to the deviation from the slow manifold, and it vanishes if and only if $x_{\mathrm{f}} = -\tilde{x}_4$.

Taking the derivative of $V(x_{\mathrm{f}})$ along the trajectories of (3.81) yields:

$$\frac{dV}{d\tau} = \big(x_{\mathrm{f}} + \tilde{x}_4\big)\frac{dx_{\mathrm{f}}}{d\tau} = -\frac{1}{C_{\mathrm{DC}}\big(x_{\mathrm{f}} + x_3^e\big)}V(x_{\mathrm{f}}).$$

By Assumption 3.6 and Assumption 3.4, the term $x_{\mathrm{f}} + x_3^e$ is uniformly bounded by $x_3^e - \delta > 0$. Therefore, the reciprocal is bounded by:

$$\frac{1}{x_{\mathrm{f}} + x_3^e} \geq \frac{1}{x_3^e + \delta}. \tag{3.83}$$

Consequently, the derivative of the Lyapunov function is upper bounded as

$$\frac{dV}{d\tau} \leq -\lambda V(x_{\mathrm{f}}), \quad \text{with} \quad \lambda := \frac{1}{C_{\mathrm{DC}}(x_3^e + \delta)} > 0. \tag{3.84}$$

This inequality implies that $V(x_{\mathrm{f}})$ decays exponentially at rate λ, ensuring that the fast state x_{f} converges locally exponentially to the slow manifold $x_{\mathrm{f}} = -\tilde{x}_4$.

Remark (Local nature of the stability result). *The exponential stability of the fast subsystem is established locally within the compact set defined by Assumption 3.6. This restriction reflects the requirement that the deviation $|x_{\mathrm{f}}|$*

remains sufficiently small to preserve positivity of $x_{\mathrm{f}} + x_3^e$ and ensures physical feasibility.

The exponential stability of the boundary-layer (fast) subsystem about the slow manifold is ensured within the admissible domain. In conjunction with the stability of the reduced (slow) subsystem and the regularity of the slow manifold, this forms the basis for applying the Singular Perturbation Theorem. A verification of all five conditions ($\mathcal{C}1$))–(($\mathcal{C}5$) is provided in the following.

3.5.2.5 Verification of the Conditions in Theorem A.8.1

The Singular Perturbation Theorem applied in this analysis requires the verification of five technical conditions (($\mathcal{C}1$)–($\mathcal{C}5$)), defined in Appendix A.8. Verification of the five technical conditions is provided in the following.

Regarding Condition ($\mathcal{C}1$) (Equilibrium at the Origin). In the error coordinates, the equilibrium point is shifted to the origin: $\tilde{x} = 0$, $x_{\mathrm{f}} = 0$. By construction of the state-space representation, $f(t, 0, 0, \varepsilon) = 0$ and $g(t, 0, 0, \varepsilon) = 0$ hold for all $t \geq 0$ and $\varepsilon > 0$. Thus, ($\mathcal{C}1$) is satisfied. □

Regarding Condition ($\mathcal{C}2$) (Existence of the Slow Manifold). At $\varepsilon = 0$, the fast dynamics satisfy

$$0 = g(t, \tilde{x}, x_{\mathrm{f}}, 0) = -\frac{1}{C_{\mathrm{DC}}} \frac{x_{\mathrm{f}} + \tilde{x}_4}{x_{\mathrm{f}} + x_3^e}. \tag{3.85}$$

Under Assumption 3.4, the denominator remains positive. The unique solution is $x_{\mathrm{f}} = h(t, \tilde{x}) = -\tilde{x}_4$, which is smooth and satisfies $h(t, 0) = 0$. ($\mathcal{C}2$) is therefore fulfilled. □

Regarding Condition ($\mathcal{C}3$) (Smoothness and Boundedness of Data). Within the compact domain

$$B_\rho := \{\, \tilde{x} \in \mathbb{R}^4 \mid |\tilde{x}_1|, |\tilde{x}_2| \leq 1,\ |\tilde{x}_3| \ll x_3^e \,\}, \tag{3.86}$$

all polynomial and rational terms in f, g, h as well as their partial derivatives remain smooth and uniformly bounded, due to Assumption 3.4 and Assumption 3.5. Hence, ($\mathcal{C}3$) holds. □

Regarding Condition ($\mathcal{C}4$) (Exponential Stability of Reduced System). Using the Lyapunov function defined in (3.64), and under the parameter constraints derived in (3.77) and (3.78), the time derivative satisfies

$$\dot{V} \leq -\lambda_1 \|\tilde{x}\|^2 \tag{3.87}$$

for a certain $\lambda_1 > 0$, thus proving exponential stability of the reduced system. Therefore, ($\mathcal{C}4$) is satisfied. □

Regarding Condition ($\mathcal{C}5$) (Exponential Stability of Boundary-Layer System). Stability of the boundary-layer system was shown using the Lyapunov function (3.82). Its derivative, as given in (3.84), satisfies

$$\dot{V} = -\frac{1}{C_{\mathrm{DC}}(x_{\mathrm{f}} + x_3^e)}(x_{\mathrm{f}} + \tilde{x}_4)^2 < 0 \tag{3.88}$$

within the compact set $|x_{\mathrm{f}}| \leq \delta_V \ll x_3^e$. Hence, the boundary-layer system is uniformly exponentially stable, and ($\mathcal{C}5$) is satisfied. □

Since all five conditions ($\mathcal{C}1$)–($\mathcal{C}5$) of Theorem A.8.1 are verified, the overall singularly perturbed system is locally exponentially stable around the equilibrium point.

Remark (Semiglobal practical exponential stability within the admissible domain). *The Lyapunov analysis establishes local exponential stability around*

the equilibrium. Due to forward invariance induced by the saturating integrator (Assumption 3.5) and the positivity of the DC-link (Assumption 3.4), all trajectories starting in the compact admissible set $\mathcal{D}$ remain in $\mathcal{D}$. Hence the equilibrium is semiglobally, and practically exponentially stable within $\mathcal{D}$. In particular, it is globally attractive on $\mathcal{D}$ for the chosen parameterization.

3.6 Summary and Concluding Remarks

This chapter presents the SoG concept as a decentralized control method for DC and hybrid AC/DC microgrids. Motivated by the analogy of communicating vessels, the method establishes a bidirectional mapping between the internal energy state, represented by the local SoC and externally observable variables such as voltage and frequency. The key idea is to encode each unit's SoC into small, bounded offsets of its converter setpoints, thereby enabling autonomous SoC balancing and proportional power sharing based solely on local measurements.

To realize this principle, a forward mapping translates local SoC values into voltage or frequency reference deviations (see Equations (3.8) and (3.18)), while an inverse mapping reconstructs a global indicator from local measurements, yielding $\mathrm{SoG}_{\mathrm{DC}}$ and $\mathrm{SoG}_{\mathrm{AC}}$ as defined in (3.20) and (3.22).

Together, these mappings establish an implicit signaling mechanism that embeds internal coordination variables and enables fully decentralized decision-making, SoC balancing, and proportional power sharing based solely on local measurements (see Section 3.2 and Section 3.3). The control scheme enables cross-domain operation by formulating compatible mappings on the DC and AC sides. A decentralized power law governs the interlink power exchange in proportion to the local SoG mismatch, subject to deadband and saturation constraints, thereby ensuring bidirectional coupling between the two domains (see Equation (3.26)).

The mapping gains are designed to ensure observability, robustness, and compatibility with the required time-scale separation. Feasible regions are defined

via analytical constraints for both DC and AC domains (see (3.17) and (3.19)). A normalization factor $\mathrm{SoC}_{\Delta,i}$ accounts for asymmetric operating ranges and ensures consistent control sensitivity among units. On the AC side, the mapping relies on the assumption of a predominantly inductive grid, as formalized in Assumption 3.2.

The closed-loop dynamics are embedded into a nonlinear state-space model (see Equations (3.40), (3.41) and (3.42)) and cast into a singularly perturbed form through gain scaling. The resulting decomposition into slow and fast subsystems (see Section 3.5.2.1) allows a structured stability analysis based on Lyapunov theory. The analysis derives explicit conditions for local exponential stability of the reduced (slow) subsystem (see Section 3.5.2.3) and for uniform exponential stability of the boundary-layer (fast) dynamics (see Section 3.5.2.4). With the Assumptions 3.1–3.3, and with boundedness and positivity ensured by Assumptions 3.5 and 3.4, the overall system exhibits semiglobal practical exponential stability within the physically admissible domain.

Overall, the SoG concept provides a consistent, scalable, and analytically validated control method for decentralized SoC balancing, power sharing among BESSs, and coordinated AC/DC power exchange, without relying on any communication infrastructure. The subsequent chapter extends this concept to VSM capabilities and GSL coordination (see Section 4.1 and Section 4.2). Chapter 5 presents a detailed experimental validation of the proposed methods under representative test scenarios.

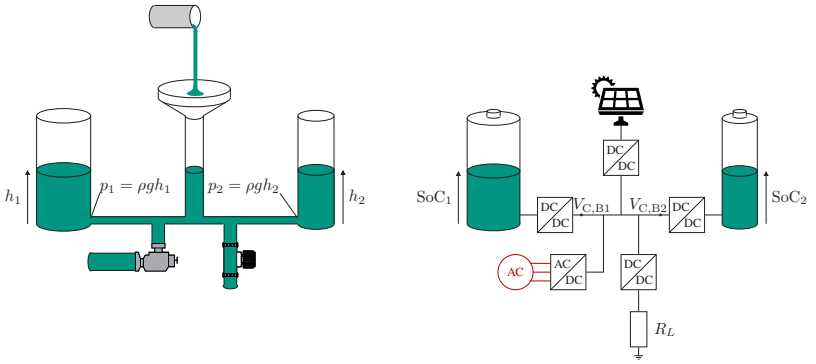
4 Extended Control Strategies

Building upon the SoG-based control framework introduced in Chapter 3, the present chapter extends the approach to incorporate additional grid-supportive functionalities. Two complementary strategies are developed.

1. An SoG-based VSM for inertia emulation and frequency support in AC microgrids.
2. A Communication-free concept for GSLs in DC microgrids, where loads dynamically adapt their consumption in response to local grid conditions.

Both extensions preserve the decentralized and communication-free nature of the SoG framework while broadening its range of ancillary services. Drawing on the physical analogy of communicating vessels, as illustrated in Figure 4.1, the concept is generalized beyond energy storage to capture the interaction between AC grids and adaptive loads. The resulting mechanisms are seamlessly integrated into the existing SoG architecture, forming a consistent and scalable control strategy for converter-dominated microgrids.

Similar to how hydrostatic pressure differences drive volumetric flow between communicating vessels, the instantaneous power consumption of GSLs can be modulated according to local SoG values. A low SoG, reflected in reduced voltage or frequency, indicates an energy deficit and triggers load reduction. Conversely, a high SoG signals surplus energy and allows additional consumption. This self-organizing behavior enables flexible loads to enhance grid stability without explicit communication or centralized coordination.



(a) Communicating vessels with coupled levels. **(b)** Equivalent electrical system with BESS and loads.

Figure 4.1: Extended analogy between (a) communicating vessels and (b) a shared DC-bus with batteries, flexible loads, and AC coupling. In both representations, equilibrium emerges from decentralized interactions without centralized coordination, illustrating the conceptual foundation of the extended SoG approach. Adapted from [J7].

The remainder of this chapter is organized as follows. Section 4.1 presents the SoG-based VSM, including the control structure, synchronization mechanism, and its role in inertia provision. Section 4.2 introduces the concept of GSLs, develops the control law, and analyzes its impact on system dynamics. A consolidated stability analysis of the extended framework is provided at the end of the chapter.

4.1 SoG-Based Virtual Synchronous Machine

As outlined in Section 3.4, the SoG concept provides a fully decentralized method for coordinating power exchange between DC and AC subsystems. In its baseline form, this coupling is realized through a proportional control law (see Equation (3.26)), which controls the active power of the IC in response to differences between the local SoG values on the DC and AC sides.

Future AC grids with high penetration of converter-based resources are expected to rely increasingly on virtual inertia and fast frequency support in order to

ensure stable operation in low-inertia conditions, as highlighted in Section 2.3.5. To address this requirement, the SoG framework is extended in this section by embedding a VSM method into the IC. This integration enables the converter to provide dynamic frequency support and inertia emulation, while retaining the communication-free characteristics of the SoG control principle.

4.1.1 Control Structure of SoG-Based VSM

Figure 4.2 illustrates the control architecture of the proposed SoG-based VSM used to operate the IC. A VSM, governed by the swing equation (2.19) introduced in Section 2.4.4, generates the virtual angle θ_{vsm}, which defines the synchronous reference frame (dq-frame) for the cascaded control system. The outer voltage loop controls the converter's terminal voltage, through providing the current references i_d^* and i_q^* to the inner current control loop.

The frame conversion is performed using a standard dq/abc transformation, and the resulting modulation signals are processed by a carrier-based PWM scheme to generate the converter's switching signals.

Dashed connections in Figure 4.2 denote measured signals, including the DC-link voltage V_{DC}, the converter terminal voltage V_{VSM}, the inductor current I_{VSM}, and the grid voltage V_g. These quantities are continuously monitored and fed into the corresponding control blocks. The instantaneous active and reactive powers are computed based on Equation (A.33) and serve as inputs to the VSM control law. Details of the voltage and current control implementation are provided in Appendix A.5.

Unlike conventional VSM schemes, where the active power reference P_{IC}^* is typically constant or externally defined, the proposed approach introduces a dynamic modulation based on the internal state of the hybrid microgrid. Specifically, the power reference is shaped by the difference between the AC-side and DC-side SoG quantities, enabling the IC to self-regulate its power exchange in response to the system's internal energy distribution.

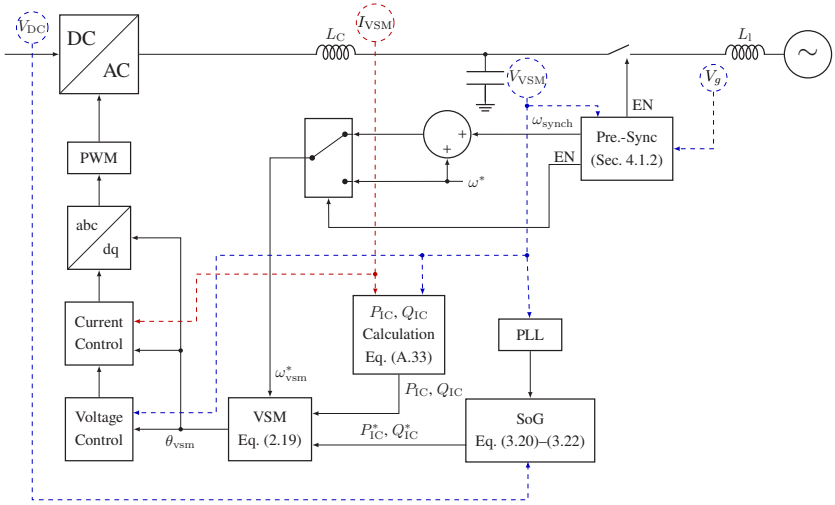


Figure 4.2: Schematic diagram of the SoG-based VSM control structure. The SoG block provides active and reactive power references $(P^*_{\mathrm{IC}}, Q^*_{\mathrm{IC}})$ according to Equations (3.20)–(3.22). A VSM (Equation (2.19)) generates the internal angle θ_{vsm}, which is used by the voltage and current controllers to regulate the IC. Pre-synchronization (Section 4.1.2) and a PLL ensure stable grid connection. Dashed lines indicate measured signals.

The modulation law is defined as

$$P^*_{\mathrm{IC}} = P^{\mathrm{nom}}_{\mathrm{IC}} - k_h\big(\mathrm{SoG}_{\mathrm{AC}} - \mathrm{SoG}_{\mathrm{DC}}\big), \tag{4.1}$$

where $P^{\mathrm{nom}}_{\mathrm{IC}}$ denotes the nominal power exchange and $k_h > 0$ is a proportional gain that determines the strength of the SoG-based coupling. A high DC-side energy state results in an increase of $P^*\mathrm{IC}$, thereby promoting power injection, whereas a low DC energy state decreases P^*_{IC}. The reactive power reference is fixed at $Q^*_{\mathrm{IC}} = 0$, as the SoG modulation explicitly addresses the coupling between active power and the energy state, while reactive power regulation is delegated to grid-side mechanisms.

Before power exchange is initiated, a pre-synchronization routine ensures phase alignment between the virtual angle θ_{VSM} and the grid angle θ_{PLL}, as described

in Section 4.1.2. Once synchronization has been established, the controller transitions to grid-connected operation and the modulation path shown in Figure 4.2 becomes active.

The SoG block implements the communication-free coordination of AC and DC sides as defined in Equations (3.20)–(3.22). The resulting signal continuously modulates the active power setpoint via (4.1), providing an energy-aware inertial response on the system level. This effectively integrates the DC-side energy state into the converter's real-time power control behavior.

To prevent chattering near the operating point and to ensure compliance with the converter's power limits, a deadband and saturation are applied to the power reference according to the hysteresis scheme defined in (3.27).

4.1.2 Phase-Based Pre-Synchronization Using Time-Stamped Reference Crossings

To connect the DC microgrid to the AC grid, accurate phase alignment between the virtual phase angle θ_{VSM} generated by the VSM and the measured grid phase angle θ_{PLL} is essential. This alignment is established through a pre-synchronization mechanism that measures the instantaneous phase mismatch based on time-stamped crossings relative to a selectable reference angle $\theta_{\mathrm{T}} \in [0, 2\pi)$, typically chosen as $\theta_{\mathrm{T}} = \pi$.

The phase angles θ_{PLL} and θ_{VSM} are each compared to the reference θ_{T} to detect positive crossings. At each detected crossing, a Sample-and-Hold (S&H) block captures the current value of a locally integrated time base, yielding timestamps t_1 for the grid and t_2 for the VSM. The signed time difference

$$\Delta t = t_2 - t_1 \tag{4.2}$$

represents the relative phase offset. A positive $\Delta t > 0$ indicates that the VSM phase leads the grid, requiring deceleration, while $\Delta t < 0$ implies that the grid leads, requiring the VSM to accelerate.

This time error is held constant by a third S&H block, triggered by the grid crossing event, and subsequently scaled by a synchronization gain $K_{\mathrm{sync}} > 0$ to compute the frequency correction:

$$\omega_{\mathrm{sync}} = K_{\mathrm{sync}} \Delta t. \tag{4.3}$$

The resulting value ω_{sync} is added to the nominal VSM frequency command, yielding:

$$\omega^*_{\mathrm{vsm}} = \omega^* + \omega_{\mathrm{sync}}, \tag{4.4}$$

which accelerates or decelerates the virtual machine accordingly. This adjustment continues until the absolute time error $|\Delta t|$, corresponding to the phase mismatch, falls below a predefined threshold. At this point, the synchronization is considered successful, and the IC transitions into grid-synchronized operation by closing the circuit breaker.

Figure 4.3 illustrates the timing behavior for two representative cases. In scenario (a), the grid phase leads the VSM, resulting in $t_1 < t_2$ and thus $\Delta t > 0$, commanding deceleration. In scenario (b), the grid lags behind, yielding $\Delta t <$

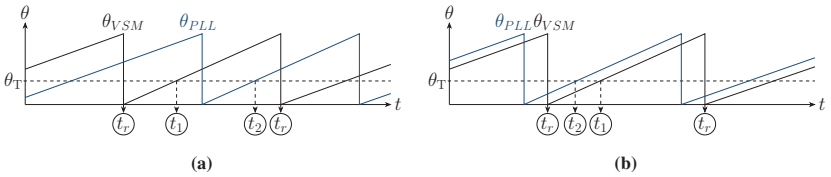


Figure 4.3: Phase relationship during pre-synchronization. (a) When the grid phase leads, the VSM decelerates. (b) When the grid phase lags, the VSM accelerates. The time stamps t_1 and t_2 are obtained at the respective θ_{T} crossings using S&H blocks. Adapted from [J3].

0, and the VSM is accelerated accordingly. In both cases, ω_{sync} facilitates smooth convergence of the phases, enabling soft synchronization without transients.

The detailed control architecture is shown in Figure 4.4. It consists of two comparators followed by an S&H unit, which holds the time instants at the defined θ_{T}-crossings of θ_{PLL} and θ_{VSM}. The integrated time signal provides a continuous and monotonic time reference, ensuring consistent timestamping for both phase angles.

The difference Δt is computed in real-time and stored using a third S&H block. This stored value is then scaled by K_{sync} to yield the synchronization frequency correction ω_{sync}, which is superimposed onto the VSM frequency setpoint. The integration path in the lower branch ensures that the virtual phase evolves continuously over time, enabling gradual convergence without abrupt changes. Once the synchronization condition is met, the breaker closes, and grid-connected operation commences.

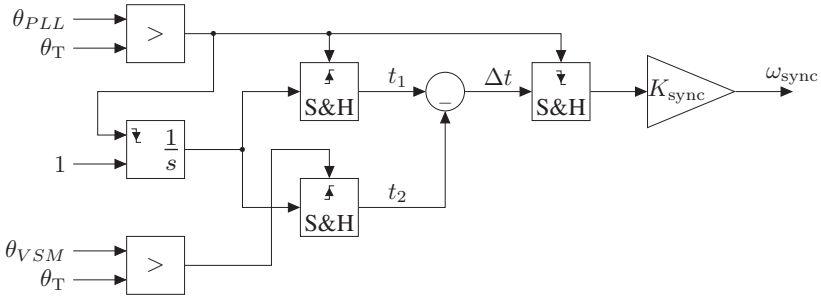


Figure 4.4: Block diagram of the pre-synchronization control based on S&H time stamping. Two S&H blocks capture the local time base at the θ_{T} crossings of θ_{PLL} and θ_{VSM}. Their difference $\Delta t = t_2 - t_1$ is held constant and scaled by K_{sync} to generate the frequency correction ω_{sync}. Adapted from [J3].

4.2 Grid-Supportive Load Concept

As outlined in Section 2.3.6, the increasing penetration of power-electronic-interfaced generation and the growing need for system flexibility have heightened the importance of GSLs. This section introduces a communication-free GSL concept for DC microgrids. The controller relies solely on the locally measured bus voltage and adapts each load by scaling the load-side voltage reference V^{*}_{Ldi} within a narrow band around $V^{\mathrm{nom}}_{\mathrm{Ldi}}$) to preserve service quality. A ZIP representation provides the mapping from voltage to power and its inverse yields a terminal voltage for a prescribed power. An energy-based restoration state ψ schedules a controlled return to nominal operation once a per-load energy budget is reached. The remainder of the section presents the control law (Section 4.2.1), the restoration mechanism (Section 4.2.2), and the closed-loop stability analysis (Section 4.2.3).

4.2.1 GSL Control Method

Figure 4.5 illustrates the control structure of the proposed GSL concept. The instantaneous bus voltage $V_{\mathrm{C,Ld1}}$ is measured locally and processed by the GSL control block to compute a dimensionless scaling factor ξ_{Ldi}. This factor dynamically modulates the reference voltage V^{*}_{Ldi}, which defines the desired power operating point of the i^{th} load. The reference voltage V^{*}_{Ldi} is tracked via a cascaded PI control structure, consisting of an outer voltage controller and an inner current controller. The resulting modulation signal is then applied to the bidirectional DC/DC converter using PWM. The entire control loop is implemented based solely on local measurements, without requiring any communication or centralized coordination. Detailed implementation aspects of the PI control structure are provided in Appendix A.1.

To ensure a smooth transition between grid-supportive operation and the nominal operating point of the load, an energy-based restoration mechanism is

integrated. As detailed in Section 4.2.2, this mechanism introduces a restoration weight $\psi \in [0, 1]$, which continuously evaluates whether the load can still provide support. As long as support is possible, ψ maintains the adapted operating point. Once support is no longer possible, ψ gradually returns the load to its nominal condition, thereby avoiding abrupt changes in power consumption.

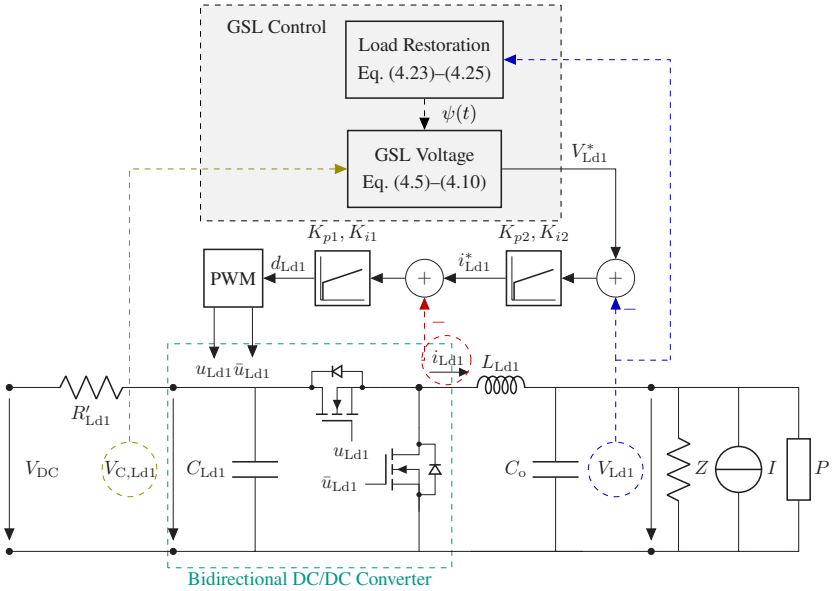


Figure 4.5: Block diagram of the proposed GSL controller for the i^{th} ZIP load. All signals are obtained from local measurements. The restoration weight ψ is generated by the energy-based restoration block in Section 4.2.2. Adapted from [J3].

The control strategy enables dynamic load adaptation by deliberately modulating the reference voltage V^*_{Ldi}, thereby adjusting the instantaneous power consumption of the load in a grid-supportive manner. Crucially, this modulation is constrained within a narrow voltage band, typically within $\pm 5\%$ of the nominal load voltage, to ensure that the functional behavior and user experience of the load remain unaffected.

Mathematically, the adaptive reference voltage for the i^{th} GSL is given by:

$$V^{*}_{\mathrm{Ldi}} = V^{\mathrm{nom}}_{\mathrm{Ldi}} \xi_{\mathrm{Ldi}}, \tag{4.5}$$

where $V^{\mathrm{nom}}_{\mathrm{Ldi}}$ denotes the nominal operating voltage of the load and ξ_{Ldi} is a dimensionless scaling factor derived from the locally measured DC-bus voltage. The factor ξ_{Ldi} is chosen such that V^{*}_{Ldi} remains within the predefined permissible voltage range of the device while enabling it to contribute to stabilizing the bus voltage.

The basic form is introduced in [C1] as

$$\xi_{\mathrm{Ldi}} = \begin{cases} 1 + \zeta_i, & \text{if } \xi_i \geq 1 + \zeta_i, \\ 1 - \zeta_i, & \text{if } \xi_i \leq 1 - \zeta_i, \\ \xi_i, & \text{otherwise}, \end{cases} \tag{4.6}$$

where ξ_i denotes the unsaturated scaling factor computed from the measured bus voltage, $\zeta_i \in (0, 1)$ specifies the saturation limits around the nominal value, i.e., the allowable deviation range of $\xi_i(t)$, and ξ_{Ldi} denotes the resulting scaling factor used to compute the modulated load voltage. Equivalently, the saturated output can be expressed in compact form using the saturation operator defined in (3.27):

$$\xi_{\mathrm{Ldi}} = \mathrm{sat}_{[1-\zeta_i,\, 1+\zeta_i]}(\xi_i) = \max\big(\min(\xi_i,\, 1 + \zeta_i),\, 1 - \zeta_i\big). \tag{4.7}$$

The preliminary, unsaturated scaling factor ξ_i is computed as

$$\xi_i = 1 + k_{\mathrm{GSL}} \psi \left(\frac{V_{\mathrm{DC}}}{V^{*}_{\mathrm{DC}}} - 1 \right), \tag{4.8}$$

where k_{GSL} is a gain factor that determines the sensitivity of the GSL response and ψ is an optional restoration variable (see Section 4.2.2). This formulation ensures that the GSL reduces its consumption when the DC-bus voltage drops

and increases it slightly when the voltage rises, thus contributing to stabilizing the grid voltage while remaining within device limits.

To avoid excessive or unnecessary control actions, a hysteresis logic is incorporated into the computation of ξ_{Ldi}. This mechanism ensures that the GSL control only reacts to significant deviations while it prevents frequent switching within a predefined tolerance band. Specifically, the response is defined as

$$\xi_{\mathrm{Ldi}}(t) = \begin{cases} 1, & \text{if } \mathcal{H}_i(t) = 1, \\ \mathrm{sat}_{[1-\zeta_i,\, 1+\zeta_i]}\big(\xi_i(t)\big), & \text{if } \mathcal{H}_i(t) = 0, \end{cases} \tag{4.9}$$

where the hysteresis state $\mathcal{H}_i(t)$ is updated according to the following rule:

$$\mathcal{H}_i(t^+) = \begin{cases} 0, & \mathcal{H}_i(t^-) = 1 \text{ and } \xi_i(t) \notin [1-\Lambda_i,\, 1+\Lambda_i], \\ 1, & \mathcal{H}_i(t^-) = 0 \text{ and } \xi_i(t) = 1, \\ \mathcal{H}_i(t^-), & \text{otherwise.} \end{cases} \tag{4.10}$$

where the superscripts t^- and t^+ indicate the values immediately before and after the update at time t, respectively. The parameter Λ_i specifies the hysteresis tolerance band that prevents frequent switching within small fluctuations.

Figure 4.6 compares the purely saturation-based control approach, corresponding to Equation (4.5) without hysteresis, shown in Figure 4.6(a), with the extended hysteresis-based control, described by Equation (4.9) combined with the hysteresis update law (4.10), shown in Figure 4.6(b). The hysteresis-based approach effectively reduces control oscillations around the nominal point and improves robustness against noise and minor voltage fluctuations.

To realistically represent the load behavior of GSL, the well-established ZIP model is employed, which captures constant-impedance (Z), constant-current (I), and constant-power (P) components of the load. This model reflects the voltage-dependent nature of practical loads more accurately than a purely constant-power assumption.

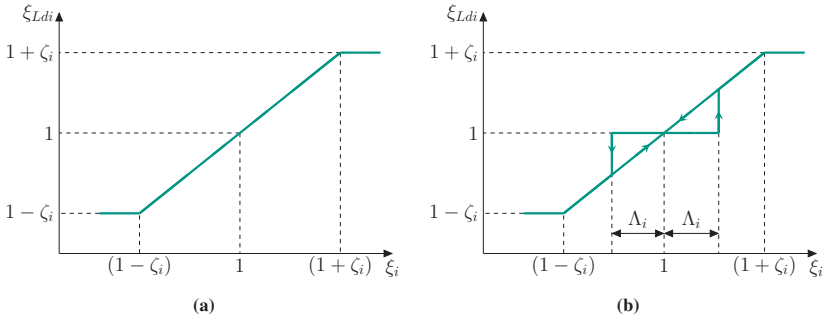


Figure 4.6: Comparison of GSL control strategies: (a) purely saturation-based control, where the response directly follows the saturated voltage deviation; (b) hysteresis-based control, where the hysteresis logic prevents frequent switching within the defined tolerance band Λ_i. Both plots show ξ_{Ldi} as a function of the normalized bus voltage deviation ξ_i. Adapted from [C5].

The instantaneous power consumption of the i-th GSL is therefore given by

$$P_{\mathrm{Ldi}} = P_{\mathrm{Ldi}}^{\mathrm{nom}}\Big(\underbrace{w_{\mathrm{P}}}_{\substack{\text{const.}\\ \text{Power}}} + \underbrace{w_{\mathrm{I}}\frac{V_{\mathrm{Ldi}}}{V_{\mathrm{Ldi}}^{\mathrm{nom}}}}_{\substack{\text{const.}\\ \text{Current}}} + \underbrace{w_{\mathrm{Z}}\Big(\frac{V_{\mathrm{Ldi}}}{V_{\mathrm{Ldi}}^{\mathrm{nom}}}\Big)^2}_{\substack{\text{const.}\\ \text{Impedance}}}\Big), \tag{4.11}$$

where $P_{\mathrm{Ldi}}^{\mathrm{nom}}$ is the nominal power at the nominal voltage $V_{\mathrm{Ldi}}^{\mathrm{nom}}$, and $w_{\mathrm{P}}, w_{\mathrm{I}}, w_{\mathrm{Z}}$ are the weighting factors of the constant-power, current, and impedance components, respectively.

The individual contributions of the ZIP components at a given operating point can also be expressed in terms of their absolute power contributions:

$$P_{\mathrm{P}} := P_{\mathrm{Ldi}}^{\mathrm{nom}} w_{\mathrm{P}}, \quad P_{\mathrm{I}} := P_{\mathrm{Ldi}}^{\mathrm{nom}} w_{\mathrm{I}}, \quad P_{\mathrm{Z}} := P_{\mathrm{Ldi}}^{\mathrm{nom}} w_{\mathrm{Z}}, \tag{4.12}$$

where P_{P}, P_{I}, and P_{Z} represent the constant-power, current-proportional, and impedance-proportional parts of the total load power, respectively.

This formulation allows the GSL to respond realistically to voltage variations while maintaining a controllable degree of flexibility for grid support. By adjusting the weights $w_{\mathrm{P}}, w_{\mathrm{I}}$, and w_{Z}, the behavior of different types of loads (e.g., resistive heaters, electronic devices, motors) can be accurately represented within the proposed control method.

The power-voltage characteristic of the ZIP load defines an implicit quadratic relation between the normalized power $P_{\mathrm{Ldi}}/P_{\mathrm{Ldi}}^{\mathrm{nom}}$ and the normalized voltage $V_{\mathrm{Ldi}}/V_{\mathrm{Ldi}}^{\mathrm{nom}}$. To explicitly determine the voltage required for a prescribed power P_{Ldi}, the mapping is defined as

$$\Phi : \mathcal{D}_{\Phi} \to [V_{\mathrm{Ldi}}^{\min}, V_{\mathrm{Ldi}}^{\max}], \quad P_{\mathrm{Ldi}} \mapsto V_{\mathrm{Ldi}}, \tag{4.13}$$

where $\mathcal{D}_{\Phi}$ denotes the set of admissible power values for which the discriminant of the quadratic equation remains non-negative. By finding the roots of (4.11), the mapping can be expressed explicitly as

$$V_{\mathrm{Ldi}} = \Phi\big(P_{\mathrm{Ldi}}\big) = V_{\mathrm{Ldi}}^{\mathrm{nom}} \frac{-w_{\mathrm{I}} + \sqrt{w_{\mathrm{I}}^2 - 4w_{\mathrm{Z}}\big(w_{\mathrm{P}} - \frac{P_{\mathrm{Ldi}}}{P_{\mathrm{Ldi}}^{\mathrm{nom}}}\big)}}{2w_{\mathrm{Z}}}, \tag{4.14}$$

with

$$\mathcal{D}_{\Phi} = \left\{ P_{\mathrm{Ldi}} \geq 0 \;\middle|\; w_{\mathrm{I}}^2 - 4w_{\mathrm{Z}} \left(w_{\mathrm{P}} - \frac{P_{\mathrm{Ldi}}}{P_{\mathrm{Ldi}}^{\mathrm{nom}}} \right) \geq 0 \right\}, \tag{4.15}$$

where the physically meaningful (non-negative) solution of the quadratic equation is selected to ensure physical admissibility. This closed-form expression provides a direct method to compute the terminal voltage corresponding to a desired power while respecting the electrical constraints imposed by the ZIP parameters. The parameters satisfy $w_{\mathrm{P}} + w_{\mathrm{I}} + w_{\mathrm{Z}} = 1$ with $w_{\mathrm{Z}} \neq 0$, ensuring a well-defined mapping in (4.14).

In the limiting case $w_Z = 0$, the quadratic term vanishes and (4.11) reduces to a linear equation in V_{Ldi}, which can be explicitly solved as

$$V_{\mathrm{Ldi}} = V_{\mathrm{Ldi}}^{\mathrm{nom}} \frac{1}{w_{\mathrm{I}}} \left(\frac{P_{\mathrm{Ldi}}}{P_{\mathrm{Ldi}}^{\mathrm{nom}}} - w_{\mathrm{P}} \right), \quad \text{for } w_{\mathrm{I}} > 0. \tag{4.16}$$

This linear expression remains valid under the condition $w_{\mathrm{I}} > 0$, which ensures the invertibility of the affine mapping. In the special case $w_{\mathrm{Z}} = 0$ and $w_{\mathrm{I}} = 0$, the power becomes entirely independent of voltage, i.e., purely constant-power. In this case, no meaningful voltage modulation can be derived from the power reference.

To unify the expressions for all admissible weightings $(w_{\mathrm{P}}, w_{\mathrm{I}}, w_{\mathrm{Z}})$, the voltage mapping can be summarized as

$$V_{\mathrm{Ldi}} = \begin{cases} V_{\mathrm{Ldi}}^{\mathrm{nom}} \dfrac{-w_{\mathrm{I}} + \sqrt{w_{\mathrm{I}}^2 - 4w_{\mathrm{Z}}\left(w_{\mathrm{P}} - \frac{P_{\mathrm{Ldi}}}{P_{\mathrm{Ldi}}^{\mathrm{nom}}}\right)}}{2w_{\mathrm{Z}}}, & w_{\mathrm{Z}} \neq 0, \\ V_{\mathrm{Ldi}}^{\mathrm{nom}} \dfrac{1}{w_{\mathrm{I}}} \left(\dfrac{P_{\mathrm{Ldi}}}{P_{\mathrm{Ldi}}^{\mathrm{nom}}} - w_{\mathrm{P}} \right), & w_{\mathrm{Z}} = 0,\ w_{\mathrm{I}} > 0. \end{cases} \tag{4.17}$$

This piecewise formulation guarantees that the voltage setpoint remains well-defined for all relevant ZIP parameterizations within the feasible domain. The condition $w_{\mathrm{Z}} = 0$ may be relevant for load types without a resistive component, such as current- or power-controlled converters.

To further generalize the response of the GSL to variations in the DC-bus voltage, the absolute power contributions P_{I} and P_{Z} are assumed to have a certain degree of flexibility and can vary within specified bounds

$$P_{\mathrm{I}} \in [P_{\mathrm{I}}^{\min}, P_{\mathrm{I}}^{\max}], \quad P_{\mathrm{Z}} \in [P_{\mathrm{Z}}^{\min}, P_{\mathrm{Z}}^{\max}], \quad V_{\mathrm{DC}} \in [V_{\mathrm{DC}}^{\min}, V_{\mathrm{DC}}^{\max}]. \tag{4.18}$$

The constant-power component P_{P} is insensitive to voltage variations and therefore does not appear in the voltage-dependent modulation equations.

The corresponding droop coefficients m_{I} and m_{Z} describing the linear sensitivity of P_{I} and P_{Z} to voltage deviations can then be defined as

$$m_{\mathrm{I}} = \frac{P_{\mathrm{I}}^{\max} - P_{\mathrm{I}}^{\min}}{V_{\mathrm{DC}}^{\max} - V_{\mathrm{DC}}^{\min}}, \qquad m_{\mathrm{Z}} = \frac{P_{\mathrm{Z}}^{\max} - P_{\mathrm{Z}}^{\min}}{V_{\mathrm{DC}}^{\max} - V_{\mathrm{DC}}^{\min}}. \tag{4.19}$$

The actively modulated power of the GSL is

$$P_{\mathrm{Ldi}}^{*} = P_{\mathrm{Ldi}}^{\mathrm{nom}} + \Delta P_{\mathrm{Ldi}}, \tag{4.20}$$

with

$$\Delta P_{\mathrm{Ldi}} = m_{\mathrm{I}}\big(V_{\mathrm{DC}} - V_{\mathrm{DC}}^{*}\big) + m_{\mathrm{Z}}\big(V_{\mathrm{DC}} - V_{\mathrm{DC}}^{*}\big)^{2}. \tag{4.21}$$

Substituting the modulated power terms back into Equation (4.14) yields a fully parameterized expression for $V_{\mathrm{Ld}i}/V_{\mathrm{Ldi}}^{\mathrm{nom}}$ that accounts for the dynamic adjustment of w_{I} and w_{Z} in response to V_{DC}:

$$\frac{V_{\mathrm{Ldi}}}{V_{\mathrm{Ldi}}^{\mathrm{nom}}} = \frac{-w_{\mathrm{I}}}{2w_{\mathrm{Z}}} + \frac{1}{2w_{\mathrm{Z}}}\Bigg(w_{\mathrm{I}}^{2} - 4w_{\mathrm{Z}}\Bigg(P_{\mathrm{Ldi}}^{\mathrm{nom}} + m_{\mathrm{I}}(V_{\mathrm{DC}} - V_{\mathrm{DC}}^{*}) + m_{\mathrm{Z}}(V_{\mathrm{DC}} - V_{\mathrm{DC}}^{*})^{2}\Bigg)\Bigg)^{\frac{1}{2}}. \tag{4.22}$$

This generalized formulation enables the control to dynamically regulate the power contribution of the GSL as a function of the instantaneous DC-bus voltage, while accounting for the nonlinear ZIP characteristics.

While the proposed control enables temporary load modulation to support the grid, not all loads can remain curtailed without compromising their primary function. After contributing a specified energy budget, selected units must be restored to their nominal power to maintain service continuity. The following subsection introduces an energy-based restoration strategy that schedules and shapes this transition toward nominal operation.

4.2.2 Load Restoration Strategy

Restoring critical loads after grid-supportive actions is essential to maintain service continuity. The proposed restoration strategy is energy-based, enabling a smooth transition back to nominal operation while avoiding abrupt changes that could destabilize the microgrid.

4.2.2.1 Restoration Condition

The restoration process is triggered when the cumulative energy deviation of the i-th GSL exceeds a predefined threshold $E_{\mathrm{GSL}}^{\max}$, ensuring that the load resumes its nominal operation only when necessary and without imposing undue stress on the system. The restoration trigger is defined by the condition

$$\underbrace{\int_{t-T_p}^{t} \left(P_{\mathrm{GSL}}(\tau) - P_{\mathrm{Ldi}}^{\mathrm{nom}}\right) \mathrm{d}\tau}_{A_1} + \underbrace{\frac{T_{\mathrm{res}}}{2}\left(P_{\mathrm{GSL}}(t) - P_{\mathrm{Ldi}}^{\mathrm{nom}}\right)}_{A_2} > E_{\mathrm{GSL}}^{\max}, \tag{4.23}$$

where T_p denotes the time window over which the power deviation is integrated, and T_{res} defines the restoration period. $P_{\mathrm{GSL}}(t)$ is the instantaneous power of the i-th GSL, and $P_{\mathrm{Ldi}}^{\mathrm{nom}}$ its nominal power rating. The term $E_{\mathrm{GSL}}^{\max}$ represents the maximum allowable energy deviation before restoration is initiated.

In (4.23) the area A_1 represents the historical energy deficit accumulated within the observation window of length T_p, while A_2 quantifies the additional energy required to ensure a smooth transition back to the nominal state. As illustrated in Figure 4.7, deviations occurring prior to $t - T_p$ are deliberately disregarded. This restriction prevents the accumulation of numerous minor deviations over extended periods, which would otherwise trigger an unnecessary restoration process. To regulate the transition back to nominal power levels, a restoration variable $\psi(t) \in [0, 1]$ is introduced, which scales the GSL action in (4.8). During grid support $\psi = 1$. The restoration process is triggered once the total energy deviation, captured in (4.23) by the sum $A_1 + A_2$, exceeds a predefined

threshold. Once this restoration condition (4.23) is met, ψ is driven gradually from 0 to 1 over a configurable restoration period T_{res}, ensuring a smooth and continuous ramp-up of the load (see Figure 4.7). This modulation prevents sudden power surges and allows prioritization among multiple loads based on system conditions, available energy, or criticality.

When the nominal power $P_{\mathrm{Ldi}}^{\mathrm{nom}}$ is not explicitly known, e.g., not measured, the relative voltage adjustment factor $\xi_{\mathrm{Ld}i}$ can be used as an alternative in combination with (4.11), assuming that voltage and current dynamics are much faster than the ξ dynamics (time-scale separation). In normalized form, the restoration condition is expressed as

$$\int_{t-T_p}^{t} \big(\xi_{\mathrm{Ld}i}(\tau) - 1\big)\mathrm{d}\tau + \frac{T_{\mathrm{res}}}{2}\big(\xi_{\mathrm{Ld}i}(t) - 1\big) > \Xi_{\mathrm{GSL}}^{\max}, \tag{4.24}$$

where $\Xi_{\mathrm{GSL}}^{\max}$ is the maximum permissible normalized energy deviation, which can be chosen based on the characteristics of the i-th load.

This inequality defines the point at which restoration of the i-th GSL begins.

4.2.2.2 Restoration Process

Once the restoration condition is met, the restoration process is carried out in a controlled and gradual manner to avoid introducing sharp transients. Specifically, the restoration variable $\psi(t)$ is ramped down linearly from 1 to 0 over the restoration time T_{res}, reducing the grid-supportive action of the load while restoring its nominal operation.

After completion of the ramp-down, the load remains at its nominal power for a hold period T_{hold}. Finally, $\psi(t)$ is ramped back to 1 to re-enable full GSL functionality.

The evolution of $\psi(t)$ during these phases is illustrated in Figure 4.7 and described as follows:

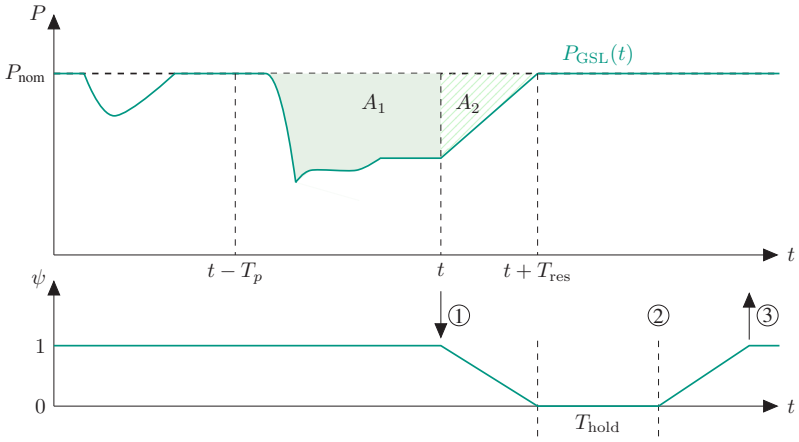


Figure 4.7: Conceptual illustration of the restoration method for critical loads in a DC microgrid. The restoration variable $\psi(t)$ is gradually modulated to enable smooth prioritization and reactivation of the load. The shaded areas indicate energy measures: A_1 represents the historical energy deficit accumulated within the observation window T_p, while A_2 quantifies the additional energy required for a smooth transition back to the nominal state. Deviations prior to $t - T_p$ are not considered in the integral. The circled markers indicate three stages of the procedure: ① Restoration initiation; ② Restoration hold; ③ Re-enabling of GSL functionality.

① **Restoration initiation:** When (4.23) holds, restoration is initiated and drives $\psi : 1 \to 0$, thereby reducing the support term in (4.8). Consequently, (4.5) with (4.11) returns the operating point toward $V_{\mathrm{Ldi}}^{\mathrm{nom}}$ with

$$\psi(t) = 1 - \frac{t - t_{\mathrm{start}}}{T_{\mathrm{res}}}, \quad t \in [t_{\mathrm{start}}, t_{\mathrm{start}} + T_{\mathrm{res}}], \tag{4.25}$$

where t_{start} marks the onset of the restoration process.

② **Restoration hold:** The load operates at its nominal power level with $\psi = 0$ for a defined interval T_{hold} to ensure service continuity.

③ **Re-enabling GSL functionality:** Finally, the restoration variable $\psi(t)$ is ramped back up from 0 to 1, fully restoring the grid-supportive capability of the load.

4.2.3 Impact of GSL on System Stability

The impact of GSL on system stability is assessed through an eigenvalue analysis of the linearized system Jacobian. In this analysis, the restoration variable ψ is set to $\psi = 1$, which represents full activation of the GSL mechanism. This assumption corresponds to the worst-case contribution of GSL to the system dynamics, as it eliminates additional restoration-related damping effects, and thus provides a conservative stability estimate. By substituting Equations (4.5) and (4.8) into the ZIP load model Equation (4.11), the normalized active power consumption of a single load i can be written as

$$\begin{aligned}\frac{P_{\mathrm{Ld}i}}{P_{\mathrm{Ldi}}^{\mathrm{nom}}} = w_{\mathrm{P}} + w_{\mathrm{I}} \left(1 + k_{\mathrm{GSL}}\psi \left(\frac{V_{\mathrm{DC}}}{V_{\mathrm{DC}}^*} - 1\right)\right) \\ + w_{\mathrm{Z}} \left(1 + k_{\mathrm{GSL}}\psi \left(\frac{V_{\mathrm{DC}}}{V_{\mathrm{DC}}^*} - 1\right)\right)^2 .\end{aligned} \tag{4.26}$$

Applying the control-theoretic coordinate mapping in Table 3.2, this can be expressed as

$$\frac{P_{\mathrm{Ld}i}}{P_{\mathrm{Ldi}}^{\mathrm{nom}}} = w_{\mathrm{P}} + w_{\mathrm{I}} \left(1 + k_{\mathrm{GSL}}\psi \frac{\tilde{x}_3}{x_3^*}\right) + w_{\mathrm{Z}} \left(1 + k_{\mathrm{GSL}}\psi \frac{\tilde{x}_3}{x_3^*}\right)^2 . \tag{4.27}$$

For $z_i = i_{\mathrm{Ld}i}$ the deviation of the aggregated load current can be formulated as

$$\begin{aligned}z_i = \frac{P_{\mathrm{Ldi}}^{\mathrm{nom}}}{x_3^* + \tilde{x}_3} \Bigg[w_{\mathrm{P}} + w_{\mathrm{I}} \Big(1 + k_{\mathrm{GSL}}\psi \frac{\tilde{x}_3}{x_3^*}\Big) \\ + w_{\mathrm{Z}} \Big(1 + k_{\mathrm{GSL}}\psi \frac{\tilde{x}_3}{x_3^*}\Big)^2 \Bigg],\end{aligned} \tag{4.28}$$

where $x_3 := x_3^* + \tilde{x}_3 > 0$, stated in Assumption 3.4, is assumed to hold.

Substituting this expression into the system Equations (3.55) affects only the dynamic of

$$\dot{\tilde{x}}_3 = \frac{1}{C_{\mathrm{DC}}}\Bigg[\frac{\beta_1\tilde{x}_1 - \tilde{x}_3}{R_1} + \frac{\beta_2\tilde{x}_2 - \tilde{x}_3}{R_2} - \frac{k_p\tilde{x}_3 + k_i\tilde{x}_4}{\tilde{x}_3 + x_3^e} - \frac{P_{\mathrm{Ldi}}^{\mathrm{nom}}}{x_3^* + \tilde{x}_3}\Bigg(w_{\mathrm{P}} + w_{\mathrm{I}}\Big(1 + k_{\mathrm{GSL}}\psi\frac{\tilde{x}_3}{x_3^*}\Big) + w_{\mathrm{Z}}\Big(1 + k_{\mathrm{GSL}}\psi\frac{\tilde{x}_3}{x_3^*}\Big)^2\Bigg)\Bigg]. \tag{4.29}$$

The closed-loop system is compactly defined as

$$\dot{\tilde{x}} = f(\tilde{x}), \tag{4.30}$$

where $f : \mathbb{R}^4 \to \mathbb{R}^4$ denotes the right-hand side of the nonlinear system, the effect of GSL control is explicitly captured in the modified $\dot{\tilde{x}}_3$ dynamics.

To assess the impact of the GSL control strategy on the system's local stability properties, the nonlinear model described by Equation (3.55) is linearized around the equilibrium point. The resulting Jacobian matrix is given by

$$\mathcal{J} = \left.\frac{\partial f(\tilde{x})}{\partial\tilde{x}}\right|_{\tilde{x}=0}. \tag{4.31}$$

The restoration factor ψ is fixed at $\psi = 1$ throughout the analysis, corresponding to a fully active GSL response and yielding a conservative estimate of the stability margin.

This yields the linearized system

$$\dot{\tilde{x}} \approx \mathcal{J}\tilde{x} = \begin{bmatrix} -\alpha_1\beta_1 x_3^e & 0 & \alpha_1 x_3^e & 0 \\ 0 & -\alpha_2\beta_2 x_3^e & \alpha_2 x_3^e & 0 \\ \frac{\beta_1}{C_{\mathrm{DC}}R_1} & \frac{\beta_2}{C_{\mathrm{DC}}R_2} & \mathcal{J}_{33} & -\frac{k_i}{C_{\mathrm{DC}}x_3^e} \\ 0 & 0 & 1 & 0 \end{bmatrix} \tilde{x}, \tag{4.32}$$

with the partial derivative

$$\mathcal{J}_{33} = \left.\frac{\partial \dot{\tilde{x}}_3}{\partial \tilde{x}_3}\right|_{\tilde{x}_3=0} = \frac{1}{C_{\mathrm{DC}}}\left(-\frac{1}{R_1} - \frac{1}{R_2} - \frac{k_p}{x_3^e} - \frac{P_{\mathrm{Ldi}}^{\mathrm{nom}}}{(x_3^*)^2}\left[k_{\mathrm{GSL}}\psi\big(w_{\mathrm{I}} + 2w_{\mathrm{Z}}\big) - 1\right]\right). \tag{4.33}$$

The term involving k_{GSL}, as defined in (4.8), appears exclusively in the coefficient of the expression $\big(w_{\mathrm{I}} + 2w_{\mathrm{Z}}\big)$, which represents the sum of the current-proportional and the impedance depended load power. In contrast, the constant-power component w_{P} remains independent of k_{GSL}. This observation clearly indicates that the GSL functionality is implemented solely through the I and Z components, whereas the P component does not contribute to the grid-supportive response.

In the following, the influence of the GSL, parametrized by k_{GSL}, on the eigenvalues of the Jacobian matrix $\mathcal{J}$, and thus on the system's stability, is systematically investigated. To this end, four representative ZIP load scenarios are defined, each characterized by a distinct composition of w_{P}, w_{I}, and w_{Z}, while ensuring the normalization condition $w_{\mathrm{P}}+w_{\mathrm{I}}+w_{\mathrm{Z}} = 1$, to preserve power balance. This guarantees that the total load level remains constant across all scenarios, isolating the effect of k_{GSL} from changes in overall load magnitude.

In all scenarios, k_{GSL} is varied over the interval $k_{\mathrm{GSL}} \in [0, 5]$ in increments of $\Delta k_{\mathrm{GSL}} = 0.01$, allowing a detailed assessment of its effect on stability.

4.2.4 Investigated ZIP Scenarios

Figure 4.8 shows the root locus plots of the linearized system for the four defined ZIP load scenarios (cf. Section 2.2.3):

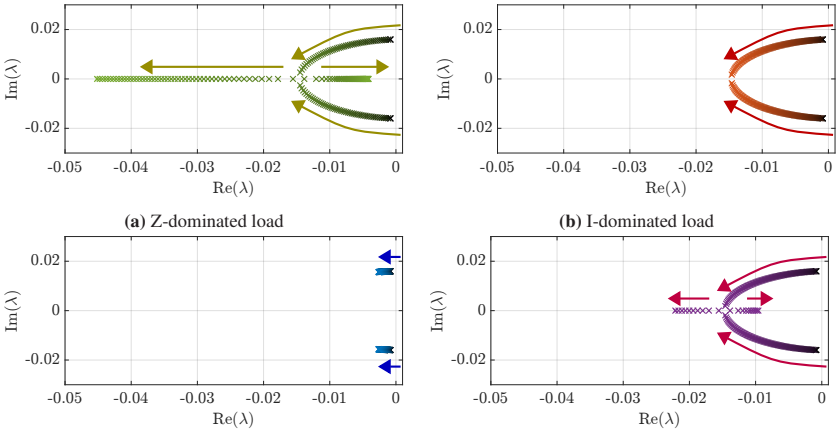
(i) Z-dominated, with $(w_{\mathrm{P}}, w_{\mathrm{I}}, w_{\mathrm{Z}}) = (0.1, 0.0, 0.9)$,

(ii) I-dominated, with $(w_{\mathrm{P}}, w_{\mathrm{I}}, w_{\mathrm{Z}}) = (0.1, 0.9, 0.0)$,

(iii) P-dominated, with weightings $(w_{\mathrm{P}}, w_{\mathrm{I}}, w_{\mathrm{Z}}) = (0.9, 0.1, 0.0)$, and

(iv) a mixed case, with balanced weights $(w_{\mathrm{P}}, w_{\mathrm{I}}, w_{\mathrm{Z}}) = (0.3, 0.4, 0.3)$.

The root locus plots illustrate the evolution of system eigenvalues in the complex plane as the GSL gain k_{GSL} increases. This classical technique provides insight into the system's stability and damping characteristics.



(a) Z-dominated load **(b)** I-dominated load

(c) P-dominated load **(d)** Mixed ZIP load

Figure 4.8: Root locus plots for varying GSL gain ($k_{\mathrm{GSL}} \in [0, 5]$) across four representative ZIP load scenarios. Arrows indicate the trajectory of the eigenvalues as k_{GSL} increases. The results highlight that stability improvements depend on the dominant load type and the GSL gain, with pronounced damping enhancement in Z- and I-dominated cases.

In the Z-dominated scenario (Figure 4.8(a)), the dominant complex-conjugate poles initially move leftward along the real axis as k_{GSL} increases, reflecting enhanced damping and improved system stability. However, beyond a certain gain level, the poles begin to move back toward the imaginary axis, indicating a reduction in damping. This non-monotonic behavior suggests an optimal range for k_{GSL}.

For the I-dominated load case (Figure 4.8(b)), a similar trend is observed. Initially, the poles shift toward more negative real parts and the imaginary component decreases, indicating less oscillatory and more aperiodic behavior. However, for high values of k_{GSL}, the damping benefit saturates or even slightly degrades.

In contrast, the P-dominated scenario (Figure 4.8(c)) shows minimal movement of the eigenvalues over the investigated gain range, confirming that the GSL has negligible influence on system dynamics when the load is dominated by constant-power behavior.

The mixed case (Figure 4.8(d)) combines characteristics of the other scenarios. The poles exhibit moderate movement toward more negative real parts and slightly reduced imaginary parts as k_{GSL} increases, indicating a balanced but less pronounced stabilizing effect.

Overall, the analysis reveals that the stabilizing effect of the GSL controller is highly dependent on the ZIP load composition and that excessive gain can be counterproductive. In particular, Z- and I-dominated scenarios benefit from moderate GSL gains, whereas the P-dominated case remains largely unaffected.

4.3 Summary and Concluding Remarks

This chapter extends the SoG control framework introduced in Chapter 3 by incorporating additional grid-supportive functionalities, enabling a comprehensive, decentralized control strategy for both AC and DC microgrids. Two

complementary approaches are developed and analyzed: an SoG-based VSM for AC systems and a communication-free GSL concept for DC grids.

The SoG-based VSM integrates inertia emulation and frequency support into the SoG framework, leveraging local SoG measurements to dynamically adjust the active power reference of the interface converter. This allows for both stable DC–AC coupling and provision of virtual inertia, entirely without communication infrastructure. A dedicated pre-synchronization mechanism ensures smooth and robust grid connection by aligning the virtual and grid phases. In the present implementation, the reactive power reference is set to $Q^* = 0$, since the SoG-based modulation targets the active-power and frequency-energy coupling, while reactive-power control can be incorporated in future extensions if required.

For DC microgrids, the proposed GSL concept utilizes flexible loads as active control elements. By modulating their power consumption in response to the local SoG level, GSLs contribute to voltage stabilization without impairing their primary functionality. The strategy combines saturation and hysteresis mechanisms to achieve robust and realistic responses, while an energy-based restoration method guarantees a smooth return to nominal operation once sufficient energy balance is restored. The control is further enriched by adopting a voltage-dependent ZIP load model, which accurately captures practical load behaviors and provides a rigorous foundation for the power-voltage relationship.

A stability analysis based on linearization around the equilibrium point and eigenvalue evaluation demonstrates the stabilizing potential of GSLs, particularly in Z- and I-dominated load scenarios. The analysis shows that increasing the GSL gain k_{GSL} can significantly improve damping and shift eigenvalues further into the stable region. However, this effect is non-monotonic: beyond a certain gain threshold, additional increases may reduce the damping benefit or even deteriorate system stability. In contrast, the constant-power component remains largely unaffected by the GSL mechanism.

Throughout the analysis, the restoration factor is fixed at $\psi = 1$, yielding a conservative stability estimate. The impact of partial restoration ($\psi < 1$) and time-varying restoration schedules remains a topic for future work.

Overall, this chapter demonstrates how the SoG concept can be generalized beyond energy storage to incorporate AC–DC interactions, inertia emulation, and demand-side flexibility. The resulting decentralized framework provides a wide range of ancillary services, including frequency support, voltage stabilization, and load restoration, relying solely on local measurements and without requiring explicit communication or centralized coordination. These features make the proposed approach particularly suited for modern, converter-dominated microgrids with high shares of renewable energy and flexible loads.

5 Experimental Setup and Validation

This chapter provides an experimental validation of the control strategies developed in Chapter 3 and Chapter 4. To quantify their performance under laboratory conditions that reflect practical operating constraints of low-voltage DC and hybrid AC/DC microgrids, the Smart2DC Microgrid laboratory is conceived, designed, and established as part of this dissertation at the Smart Energy System Control Laboratory (SESCL) [151] of the Karlsruhe Institute of Technology (KIT).

This chapter presents the experimental setup and the main validation results, addressing:

- the design and implementation of the Smart2DC microgrid laboratory, including the hardware components and real-time control infrastructure,
- the development of a structured and reproducible testing methodology for microgrid control validation,
- the definition of performance metrics and evaluation criteria aligned with practical microgrid requirements, and
- the experimental demonstration and discussion of the SoG-based control strategy, as well as the complementary VSM and GSL functionalities, under realistic operating scenarios.

The remainder of this chapter is organized as follows: Section 5.1 describes the Smart2DC laboratory HW and the real-time control and measurement infrastructure. Section 5.2 sets out the test methodology and four representative scenarios. The experimental results are presented in Section 5.3. Finally, Section 5.4 provides a comprehensive discussion of the findings.

5.1 Laboratory Design and System Architecture

The experimental validation of the proposed SoG-based control strategies is conducted in the Smart2DC laboratory at the SESCL of KIT [151]. Its modular design allows the realization of different microgrid configurations and operating scenarios in a controlled environment.

A schematic overview of the Smart2DC laboratory is shown in Figure 5.1. The laboratory consists of two main subsystems: a modular, high-dynamic rapid-prototyping cabinet and the DC house, which serves as a flexible and realistic test environment. While the DC house is part of the overall laboratory infrastructure, all experiments presented in this dissertation are conducted exclusively on the rapid-prototyping cabinet, which is therefore described in detail below.

The rapid-prototyping cabinet integrates programmable power supplies, racks of SiC-Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)-based half-bridges, and passive components such as capacitors, inductors, and resistors, as well as additional modular elements. These components can be flexibly configured into various electrical circuits, enabling the emulation of different microgrid configurations and operating conditions. Dedicated DC and AC interfaces connect the cabinet to the busbar-matrix of the SESCL, which ensures seamless connectivity to the other laboratory components. The specific HW models and ratings are summarized in Appendix A.7.

Figure 5.2 provides an illustrative representation of the electrical setup, highlighting how the available HW components are interconnected to realize the

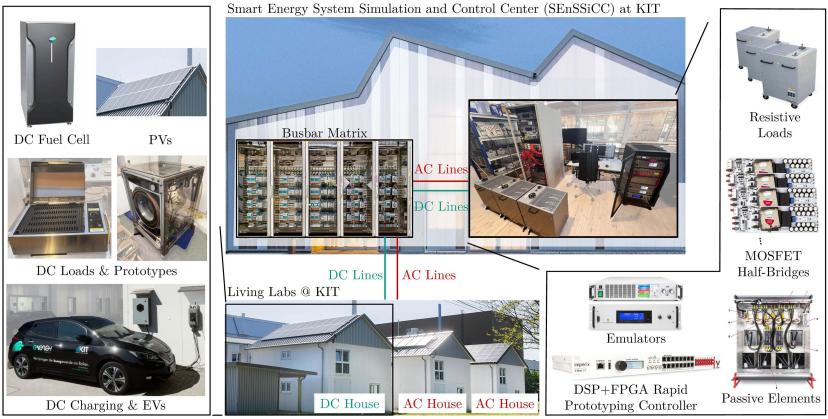


Figure 5.1: Schematic overview of the Smart2DC microgrid laboratory at KIT. The facility includes a modular rapid-prototyping cabinet, DC and AC houses for residential-scale validation, and a connection to a configurable busbar-matrix enabling flexible interconnection of sources, loads, and converters. Representative elements such as fuel cells, PV panels, EV chargers, and emulators for loads and storage are integrated to support experimental studies on hybrid AC/DC microgrids. Adapted from [C6].

microgrid topology. This diagram complements the schematic topology shown in Figure 5.3 by indicating the physical arrangement and modular composition of the system.

The measurement and control infrastructure is based on an imperix B-Box Rapid Control Prototyping (RCP) real-time platform with a hybrid Digital Signal Processor (DSP) operating at an internal clock frequency of $250\,\mathrm{kHz}$[1]. Voltage and current measurements are performed using imperix DIN800V and DIN50A sensors, which deliver differential analog signals directly to the 16-bit inputs of the B-Box RCP. The control algorithms are developed in MATLAB® R2024b and Simulink® and automatically converted to real-time code using the imperix ACG SDK. During experiments, the B-Box communicated with a host computer via Ethernet to adjust parameters and record real-time data.

[1] RCP refers to a methodology for fast implementation and testing of control algorithms on real-time HW. DSP and Field-Programmable Gate Array (FPGA) are specialized HW components that enable deterministic and highly parallel signal processing with minimal latency.

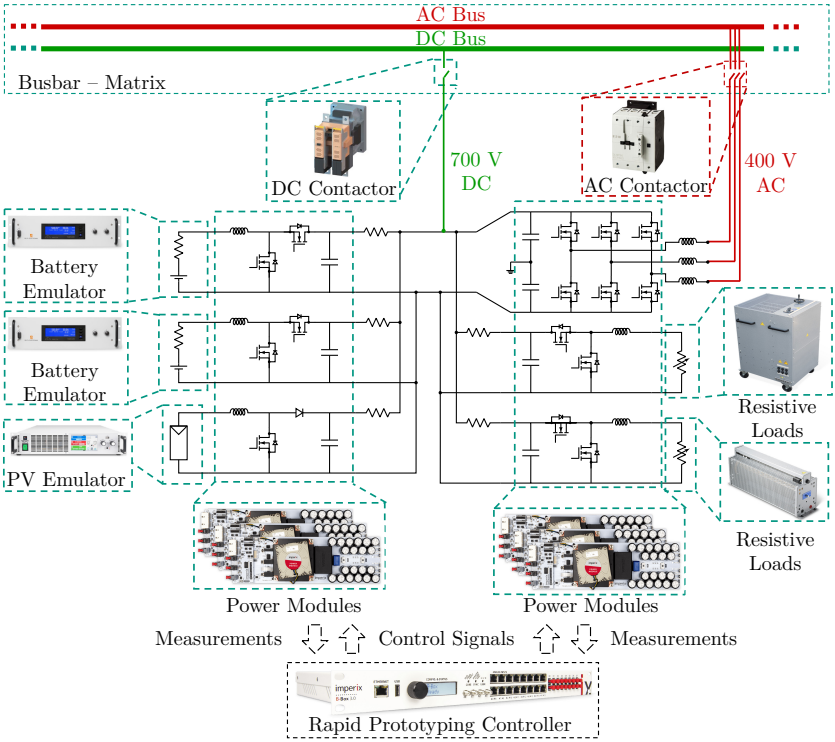


Figure 5.2: Illustrative electrical setup of the DC microgrid, showing the interconnection of HW components that realize the topology introduced in Figure 2.1. The figure highlights the integration of battery and PV emulators, power modules, controllable resistive loads, and the rapid-prototyping controller, all connected via the configurable busbar-matrix to the common 700 V DC bus (green lines) and 400 V AC grid (red lines).

External influences such as solar irradiation, ambient temperature, or battery aging are eliminated by emulating the PV generator and BESS with programmable DC power supplies. This enables controlled initialization of the system with well-defined initial states.

Figure 5.3 illustrates the topology of the experimental DC/AC microgrid setup used for the validation of the proposed control strategies. The system comprises two BESSs on the DC-side ($\mathrm{SoC}_{\mathrm{B1}}$, $\mathrm{SoC}_{\mathrm{B2}}$), a PV emulator with a DC/DC

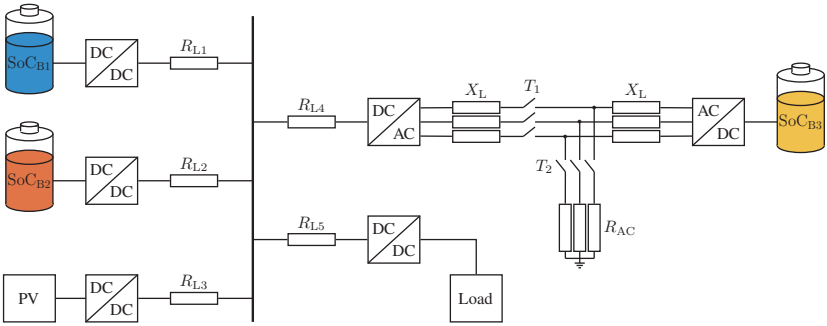


Figure 5.3: Schematic topology of the DC/AC microgrid used to validate the proposed SoG-based control strategies. Switch T_1 defines the operating mode (closed: AC-connected; open: islanded DC). Switch T_2 introduces a step load on the AC bus to study frequency transients. The line impedance X_L represents the transmission path, and R_{AC} models the AC-side load or impedance. Adapted from [J7].

converter, a controllable load, a DC–AC IC, and a BESS on the AC side ($\mathrm{SoC_{B3}}$).

The DC and AC subsystems are interconnected via a three-phase IC, which is coupled to a modeled transmission line and an AC-side impedance (R_{AC}). Switch T_1 selects the operating topology: with T_1 closed the system operates in the AC-connected configuration via the modeled line; with T_1 open the setup runs in islanded DC mode without an AC segment. A second switch T_2 connects a step load to the AC bus to inject a reproducible disturbance that provokes a frequency drop. All BESSs and loads interface with the central DC-bus through individually controllable power converters.

The control parameters applied in the experiments are selected to ensure stable and responsive operation of the system under all tested scenarios. Table 5.1 summarizes the parameters used for each of the implemented control concepts, including gains, deadbands, hysteresis offsets, time constants, virtual inertia and damping coefficients. Unless explicitly stated otherwise, the listed values apply in the respective investigations.

This setup and its configuration provided the flexibility and dynamic performance required to validate the proposed control strategies under realistic and controllable conditions.

Table 5.1: System and Control Parameters of the Hybrid AC/DC Microgrid Hardware Setup.

Symbol	Description	Value	Unit
	System References		
V_{DC}^{*}	Nominal DC-bus voltage	700	V
ω^{*}	Nominal AC angular frequency	$2\pi 50$	rad/s
SoC_{i}^{*}	SoC reference value ($i \in \{1,2,3\}$)	0.5	–
V_{AC}^{*}	Nominal AC L2N/L2L voltage	230/400	V
	Component Ratings		
$P_{\mathrm{IC}}^{\max}$	Nominal IC power rating	10	kW
$P_{\mathrm{B},i}^{\mathrm{nom}}$	Nominal battery power	5	kW
$P_{\mathrm{PV}}^{\max}$	Peak power rating of PV	3	kW
$Q_{\mathrm{B},i}$	Battery charge capacity	1	Ah
$V_{\mathrm{B},i}$	Nominal battery voltage	380	V
	Converter Parameters		
L_{χ}	Converter inductance ($\chi \in \{\mathrm{B}i, \mathrm{PV}, \mathrm{Ld}i, \mathrm{IC}\}$)	2.5	mH
C_{χ}	Converter capacitance ($\chi \in \{\mathrm{B}i, \mathrm{PV}, \mathrm{Ld}i, \mathrm{IC}\}$)	0.5	mF
	Timing Parameters		
f_s	Switching frequency	20	kHz
	Control Parameters		
σ	SoG control mapping gain	0.05	–
ψ	restoration weighting factor	0.5	–
H	Virtual inertia constant	1.0	s
D_p	Damping coefficient	10	–
$K_{P,v}$	Proportional gain of V controller (Buck/Boost)	0.10 / 0.92	–
$K_{I,v}$	Integral gain of V controller (Buck/Boost)	5.00 / 4.50	s^{-1}
$K_{P,i}$	Proportional gain of I controller (Buck/Boost)	0.01 / 2.50	–
$K_{I,i}$	Integral gain of I controller (Buck/Boost)	0.10 / 625	s^{-1}

5.2 Test Methodology and Scenarios

To evaluate the performance of the proposed SoG-based control framework introduced in Chapter 3 and Chapter 4, this chapter defines suitable quantitative metrics that reflect the central contributions of the dissertation. These include SoG-based SoC balancing with proportional power sharing, frequency-supportive DC–AC coupling via the SoG-based VSM, and demand-side support through the GSL concept. The selected metrics characterize both the dynamic response and the steady-state behavior of the overall system.

Currently, no specific International Electrotechnical Commission (IEC), Institute of Electrical and Electronics Engineers (IEEE) or International Organization for Standardization (ISO) standard defines standardized performance criteria or test procedures explicitly aimed at the comprehensive evaluation of such integrated control strategies in hybrid AC/DC microgrids. Existing international standards, such as IEC 61427-1/2 [152] and IEC 62933-1-1 [153], primarily address the characterization of energy storage systems in terms of capacity, efficiency, lifetime, and safety, while standards for battery management systems, such as IEC 62619 [154], focus on functional safety and protective mechanisms. Furthermore, established guidelines for grid-supportive functionalities, such as those defined in IEEE 1547 [155] and IEC 62116 [156], concentrate on AC grids and components, emphasizing interoperability, anti-islanding, and ancillary services, but omit a systematic evaluation of dynamic control performance and grid-supportive contributions in DC and hybrid AC/DC systems.

In the absence of explicit standardized criteria for these functionalities, this dissertation defines a set of technically motivated, transparent, and reproducible evaluation metrics tailored to the specific objectives of the proposed control concepts. These metrics are designed to quantify:

- the effectiveness and dynamic response of SoG-based power balancing,
- the ability of the SoG-based VSM to support frequency and inertia in the AC grid, and

- the contribution of GSL to voltage stability.

This structured evaluation framework ensures a comprehensive assessment aligned with the specific objectives of the proposed SoG-based control methods. It enables reproducible and meaningful comparisons both within this study and as a foundation for future research.

The following sections define a set of evaluation metrics and describe a systematic test methodology, including representative scenarios, to validate the proposed functionalities under realistic operating conditions.

5.2.1 Evaluation Metrics and Methodology

This section introduces the quantitative metrics and structured methodology used to assess the dynamic and steady-state performance of the SoG-based control concepts under realistic conditions. As highlighted by the comparison in Table 2.1, existing studies have so far addressed only specific aspects of the broader problem investigated here. A direct quantitative comparison is therefore not meaningful, as the objectives, system assumptions, and test conditions of previous approaches differ significantly. Instead of a performance comparison, this work provides a functional demonstration that illustrates the capabilities of the proposed control concept in realistic scenarios and highlights its integrative strength compared to fragmented individual approaches.

To evaluate the performance of the developed SoC balancing control, a set of quantitative metrics is defined. Depending on the specific experimental scenario, a subset of these metrics is applied to assess relevant aspects of stability, dynamic response, quasi-steady-state accuracy, and power-sharing quality. These metrics have been selected to reflect key operational requirements of real-world microgrids, including fast convergence of energy balancing, robust power sharing under parameter asymmetries, and maintenance of voltage quality under dynamic load and generation conditions.

The evaluation criteria are defined as follows:

- **Convergence of SoC Difference:**
  For an N-battery system, the maximum SoC imbalance at time t is defined as

$$\Delta_{\mathrm{SoC}}(t) = \max_{1\le i\le N} \mathrm{SoC}_i(t) - \min_{1\le i\le N} \mathrm{SoC}_i(t)\,. \tag{5.1}$$

  The asymptotic SoC difference

$$\Delta_{\mathrm{SoC},\infty} := \lim_{t\to\infty} \sup \big|\Delta_{\mathrm{SoC}}(t)\big|, \tag{5.2}$$

  is required to satisfy

$$\Delta_{\mathrm{SoC},\infty} < \big|\Delta_{\mathrm{SoC}}(0)\big|. \tag{5.3}$$

  This condition ensures that the balancing control effectively reduces the initial SoC mismatch over time.

- **First-Passage Time (FPT):**
  The SoC equalization represents an initial convergence process. For this phase, the relevant dynamic metric is the First-Passage Time (FPT), defined as

$$t_\varepsilon := \inf\big\{t \ge 0 \,\big|\, \big|\Delta_{\mathrm{SoC}}(t)\big| < \varepsilon\big\}, \tag{5.4}$$

  i.e., the earliest time at which the SoC difference enters the specified tolerance band ε. Unlike the conventional FPT time, t_ε does not require the system to remain within the tolerance thereafter. This distinction is essential, since after the initial equalization, dynamic PV and load steps are deliberately introduced to test the robustness of the convergence under realistic disturbances. Thus, the FPT captures the rapidity of the initial equalization, while the robustness of maintaining this state under subsequent dynamics is evaluated separately. Typical choices for the tolerance ε are $1\,\%$ or $5\,\%$ of the nominal SoC.

- **Residual SoC Difference:**
  The residual SoC difference after the completion of the SoC balancing process is defined as the supremum of the SoC difference for all $t \geq t_\varepsilon$:

$$\Delta_{\mathrm{SoC}}^{\mathrm{res}} := \sup_{t \geq t_\varepsilon} \left| \Delta_{\mathrm{SoC}}(t) \right|. \tag{5.5}$$

  This metric quantifies the maximum deviation of the SoC difference from the nominal equilibrium within the quasi-steady-state phase. It ensures that, despite ongoing dynamics in other system variables, the SoC difference remains consistently within the specified tolerance band ε for all $t \geq t_\varepsilon$.

- **Residual Relative Power Mismatch:**
  For an N-battery system, the instantaneous power imbalance at time t is defined as

$$\Delta_P(t) = \max_{1 \leq i \leq N} P_{\mathrm{B}i}(t) - \min_{1 \leq i \leq N} P_{\mathrm{B}i}(t). \tag{5.6}$$

  The residual relative power mismatch after the completion of the SoC balancing process is defined as the supremum of the normalized power difference for all $t \geq t_\varepsilon$:

$$\Delta_P^{\mathrm{res}} := \frac{\sup_{t \geq t_\varepsilon} \left| \Delta_P(t) \right|}{\sum_{j=1}^{N} P_{\mathrm{B}j}^{\mathrm{nom}}}, \tag{5.7}$$

  where $P_{\mathrm{B}j}^{\mathrm{nom}}$ denotes the rated nominal power of the j-th battery. This metric characterizes the maximum relative power mismatch within the quasi-steady-state phase, ensuring that power sharing remains within acceptable limits despite ongoing dynamics in other system variables.

- **Voltage Sag Mitigation:**
  The improvement in the voltage response following a load step is quantified as the relative reduction of the maximum voltage deviation compared to an unmitigated reference case. This metric is particularly relevant in

scenarios involving highly dynamic GSL, where voltage stabilization is critical.

The maximum voltage deviation in the reference scenario (without GSL) is defined as

$$\Delta V_{\mathrm{ref}} := \max_{t \geq t_0} \left| V_{\mathrm{DC}}(t) - V_{\mathrm{DC}}^{\mathrm{nom}} \right|_{\text{(without GSL)}}, \tag{5.8}$$

and the maximum deviation under the proposed control (with GSL) as

$$\Delta V_{\mathrm{GSL}} := \max_{t \geq t_0} \left| V_{\mathrm{DC}}(t) - V_{\mathrm{DC}}^{\mathrm{nom}} \right|_{\text{(with GSL)}}. \tag{5.9}$$

The relative improvement in percent is then given by

$$\eta_V := \left(1 - \frac{\Delta V_{\mathrm{GSL}}}{\Delta V_{\mathrm{ref}}} \right) \cdot 100\%. \tag{5.10}$$

A higher value of η_V indicates superior mitigation of the voltage sag achieved by the proposed control. It should be noted that these voltage dynamics occur on a significantly faster timescale than the SoC balancing process and are therefore evaluated independently of it.

Collectively, the evaluation metrics capture the speed of the initial SoC equalization, expressed by the FPT, the steadiness of the quasi-steady-state phase, represented by $\Delta_{\mathrm{SoC}}^{\mathrm{res}}$ for SoC balancing and $\Delta_{P}^{\mathrm{res}}$ for power sharing, and the dynamic of the bus-voltage response, described by η_V. Unless stated otherwise, a common tolerance ε is used for all scenarios. The experiment start time is denoted by t_0, and the FPT t_ε is measured relative to this reference. Residual quantities are evaluated for $t \geq t_\varepsilon$. These conventions provide a consistent evaluation framework and allow direct comparison between different scenarios and controller settings.

5.2.2 Test Scenarios and Varied Parameters

To evaluate the control performance under different operating conditions, the following input parameters are systematically varied during the experiments:

- **Initial SoC of the BESSs:** asymmetric initial charge levels,
- **PV power injection:** no injection, PV power equal to the load, PV surplus,
- **Load profile:** constant load, positive load step, negative load step,
- **Interlink configuration:** decoupled, coupled to a stiff AC grid, coupled to a weak AC grid formed by a BESS, including frequency variations to emulate grid dynamics,

These parameters are chosen to replicate typical grid situations, such as PV injection, load steps, and asymmetric storage utilization. The subsequent test scenarios distinguish between different system configurations and activated control functions. Table 5.2 summarizes the four systematically defined test scenarios that are used to validate the proposed control concept.

The individual scenarios are described in detail below.

Scenario I: DC islanded mode
This baseline scenario serves as the reference for validating the SoG control, as introduced in Chapter 3, without external influences. To assess the robustness of the proposed approach under different system conditions, three configurations are investigated: a reference configuration with symmetric storage capacities and line resistances, a variant with asymmetric storage capacities to emulate heterogeneous BESSs, and a variant with asymmetric line resistances to reflect unequal cable impedances or installation conditions. In all cases, two BESSs with different initial SoCs exchange energy exclusively within an islanded DC microgrid. The evaluation focuses on the convergence of SoC balancing, voltage stability, the control performance during load and PV steps, and the proportional distribution of power between the two BESSs. This scenario directly addresses

Table 5.2: Systematic overview of the four test scenarios for validating the proposed control concept.

Scenario (Section)	Operating mode	Objective	Active functions
I (5.3.1)	DC islanded mode	SoC balancing in DC microgrids	SoG control
II (5.3.2)	DC/AC coupling	SoC balancing across DC/AC microgrids	SoG + IC
III (5.3.3)	DC/AC coupling with VSM	Provision of SoG-based virtual inertia	SoG + VSM
IV (5.3.4)	Full-system operation	Transient behavior with active GSL	SoG + VSM + GSL

the heterogeneity and asymmetry challenges identified in Section 2.3.3 and validates the corresponding contribution proposed in Section 2.5.

Scenario II: DC/AC coupling balancing

In this scenario, a third BESS is connected to the system via a bidirectional IC. The objective is to demonstrate cross-domain SoC balancing between DC- and AC-connected BESSs, as proposed in Section 3.4, and to analyze the resulting load sharing across both domains. The coupling is achieved indirectly through small frequency reference modulations in the AC grid, which steer the energy flow based on the SoG difference. The evaluation focuses on the synchronization of storage states, the selectivity of energy transfer, and the distribution of power contributions between the connected units. This scenario responds to the AC/DC coupling challenge highlighted in Section 2.3.5 and validates the proposed cross-domain balancing mechanism introduced in Section 3.4.

Scenario III: DC/AC coupling with VSM

This scenario extends the interlink coupling by introducing a VSM, following the concept presented in Section 4.1, which responds to frequency deviations and

emulates inertial behavior. The objective is to evaluate the frequency-supportive properties of the system, particularly in terms of frequency stability, response time, and inertial behavior during transients. It specifically targets the lack of inherent inertia and frequency support noted in Section 2.3.5 and demonstrates the novel SoG-based VSM concept from Section 4.1.

Scenario IV: Full-system operation with GSL
The final scenario adds GSL, based on the concept described in Section 4.2, which responds to local grid signals in addition to the storage control. The objective is to investigate the coordinated interaction of all subsystems and to validate load control based on local measurements. The evaluation focuses on active load support during transients, the interaction between storage and interlink components, and the distribution of power contributions between BESSs and GSL. This scenario addresses the need for fast local voltage support under high load dynamics (see Section 2.3.6) and validates the GSL concept introduced in Section 4.2.

The evaluation methodology defined in this chapter, along with the four test scenarios, forms the methodological foundation for the experimental investigation of the proposed control concept. Together, they systematically cover the control challenges identified in Section 2.3, overcome the limitations of existing approaches discussed in Section 2.4, and substantiate the contributions defined in Section 2.5.

5.3 Experimental Results and Evaluation

This section presents and analyzes the experimental results obtained for the test scenarios defined in Section 5.2. These experiments serve to validate the developed control strategy under realistic and dynamic operating conditions, demonstrating its functionality, robustness, and scalability. To increase the temporal resolution of transient events during the laboratory experiments, the storage

capacities are deliberately scaled down. This measure significantly reduces the test duration without distorting the qualitative system dynamics.

Each scenario targets a specific functional aspect of the proposed approach and is evaluated based on representative measurements of the SoC, power flows, DC-bus voltage, and, where applicable, AC frequency. Where relevant, key performance indicators such as response times and maximum deviations are additionally summarized.

The experimental results are organized according to the four scenarios introduced above and are analyzed with respect to the evaluation criteria defined in Section 5.2.1. This systematic presentation highlights both the dynamic behavior and the grid-supportive properties of the proposed control strategy under the tested conditions.

5.3.1 Scenario I: SoG-Based Control in DC Islanded Microgrid

In this scenario, the SoG-based control strategy is validated in an islanded DC microgrid, focusing on its ability to balance the SoC of two BESSs without external influences or communication. To evaluate the robustness of the control under different system conditions, three configurations are tested:

(i) a reference case with symmetric storage capacities and line resistances with SoG control,

(ii) a case with asymmetric storage capacities with SoG control,

(iii) a case with asymmetric storage capacities and PI-based SoG control,

(iv) a case with asymmetric line resistances with SoG control, and

(v) a case with asymmetric line resistances and PI-based SoG control.

These variants emulate realistic conditions such as heterogeneous BESSs and unequal cabling, which commonly occur in practice.

In the course of the experiment, seven predefined operating intervals are executed to represent different steady-state and transient conditions. These deliberate step changes in PV generation and load power test the controller's ability to maintain SoC balancing and voltage stability under dynamic operating conditions. The corresponding power setpoints for PV generation and loads are summarized in Table 5.3, and the time evolution of the PV and load profiles is shown in Figure 5.4(d).

Table 5.3: Power setpoints in Scenario I experiment

	①	②	③	④	⑤	⑥	⑦
P_{PV} [kW]	0.0	3.3	0.0	1.5	1.5	1.5	3.3
P_{Ld1} [kW]	1.0	1.0	1.0	1.0	3.0	1.0	1.0
P_{Ld2} [kW]	0.5	0.5	0.5	0.5	1.0	0.5	0.5

(i) Reference Configuration with Symmetric Parameters

In the symmetric reference configuration, the two BESSs are configured with identical capacities and equal line resistances. The SoG-based control reduces the initial SoC difference of approximately $20\,\%$ monotonically, as illustrated in Figure 5.4(b). Both SoCs converge toward a common value without overshoot. During the seven operating intervals, transient SoC and power responses remain within the specified bounds, demonstrating the robustness of the control strategy against generation and load variations.

The FPT time t_ε, as defined in Section 5.2.1, at which the SoC difference enters a $1\,\%$ tolerance band, is measured to be $110.72\,\mathrm{s}$, corresponding to the first crossing of the $1\,\%$ threshold marked in Figure 5.5(a). In the subsequent quasi-stationary phase $t \geq t_\varepsilon$, the residual SoC difference $\Delta_{\mathrm{SoC}}^{\mathrm{res}}$ decreases further, reaching a minimum of $0.1\,\%$ after $222.66\,\mathrm{s}$ and remaining confined within a

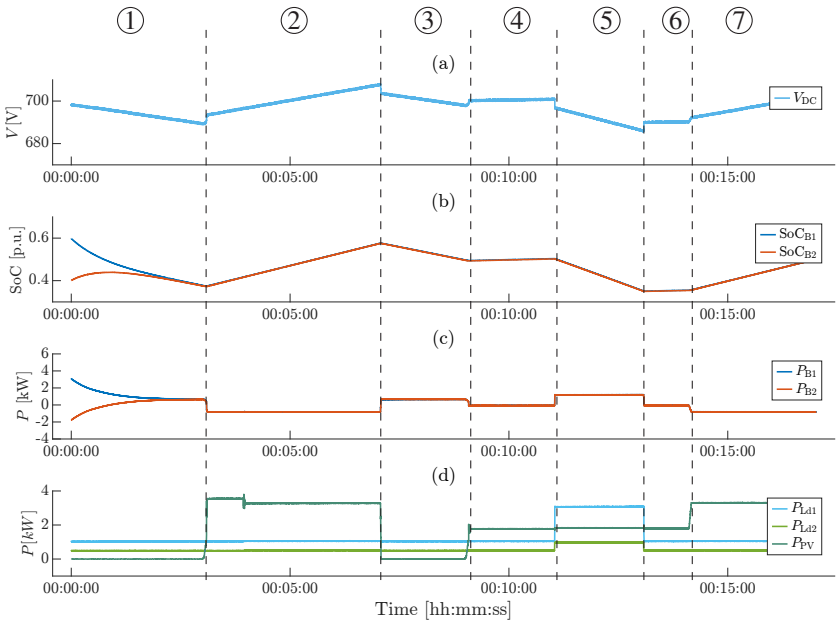


Figure 5.4: Time evolution of (a) DC-bus voltage, (b) SoC, (c) Battery powers, and (d) PV and load powers for the symmetric reference case with $Q_1 = Q_2 = 1.0\,\text{Ah}$ and equal line resistances. The SoG control drives the BESSs to nearly equal SoC while keeping V_{DC} near 700 V. Dashed vertical markers ① to ⑦ correspond to the scenario steps in Table 5.3. Adapted from [J1].

narrow band of $0.18\,\%$. As shown in Figure 5.5(b), the residual relative power mismatch Δ_P^{res} remains moderate after t_ε, with a maximum of approximately $2.46\,\%$, which reflects the favorable conditions of the symmetric configuration for achieving balanced power sharing. Throughout the experiment, the DC-bus voltage remains well regulated at 700 V, with observed variations between 685.9 V and 708.2 V, corresponding to deviations of $-2\,\%$ and $1.2\,\%$ around the nominal value of 700 V during load and PV steps (Figure 5.4(a)). The battery power flows P_{B1} and P_{B2} adjust dynamically (Figure 5.4(c)) in response to the seven predefined operating intervals, while maintaining the SoC balancing process.

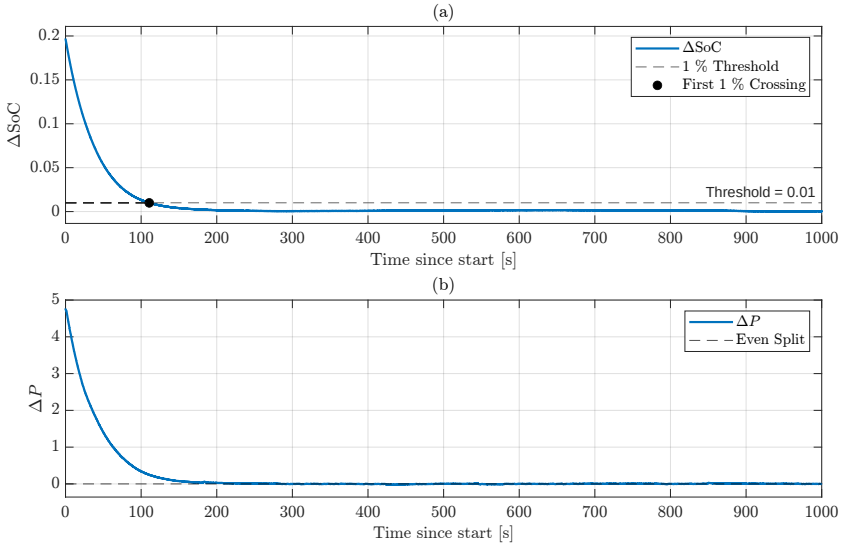


Figure 5.5: Analysis corresponding to Figure 5.4. (a) Absolute SoC difference $\Delta\mathrm{SoC}$ with a $1\,\%$ threshold (dashed) and the FPT t_ε marked by the dot. (b) Relative power mismatch with respect to an even split (dashed) over time.

These results confirm that the SoG-based control reliably achieves fast and robust SoC balancing in the symmetric configuration, maintains the SoC difference within a narrow tolerance band in the quasi-stationary phase, ensures reasonably balanced power sharing between the units, and stabilizes the DC-bus voltage under dynamic operating conditions.

(ii) Configuration with Asymmetric Storage Capacities

In the second configuration, the two BESSs are operated with asymmetric capacities, specifically $Q_1 = 1.0\,\mathrm{Ah}$ and $Q_2 = 0.5\,\mathrm{Ah}$, while line resistances remain identical. As shown in Figure 5.6(b), the SoG-based control effectively reduces the initial SoC difference and ensures synchronized SoC trajectories across the different operating points, including both surplus generation (e.g., ②) and high-demand periods (e.g., ③). Despite the asymmetry in energy

capacity, the DC-bus voltage V_{DC} remains well regulated between $687.5\,\mathrm{V}$ and $711.1\,\mathrm{V}$, corresponding to a maximum deviation of $-1.8\,\%$ and $1.6\,\%$ around the nominal value of $700\,\mathrm{V}$.

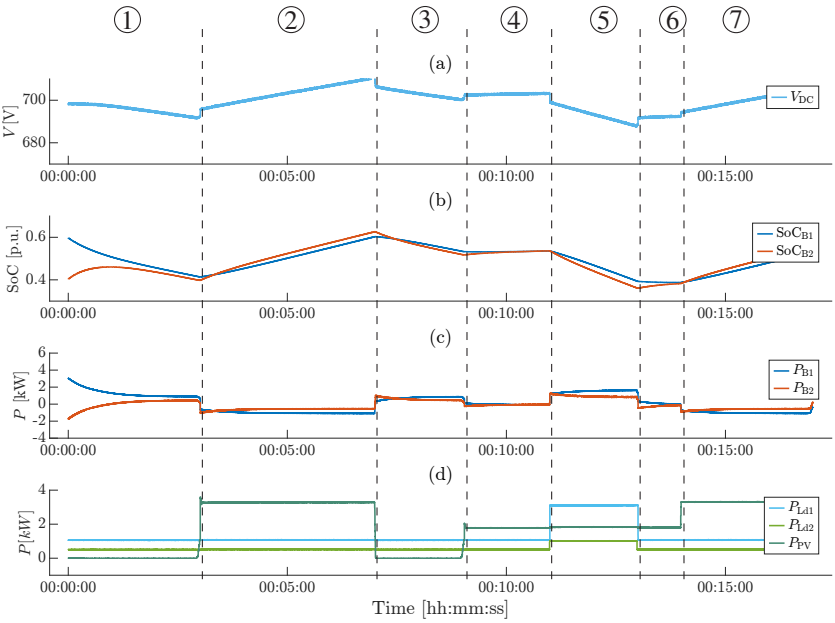


Figure 5.6: Time evolution of (a) DC-bus voltage, (b) SoC, (c) Battery powers, and (d) PV and load powers for the asymmetric capacity case with $Q_1 = 1.0\,\mathrm{A\,h}$ and $Q_2 = 0.5\,\mathrm{A\,h}$ and identical line resistances. The SoG control reduces the initial SoC difference and yields synchronized SoC trajectories across operating points, both under surplus generation (e.g. ②) and increased demand (e.g. ③), while keeping V_{DC} near $700\,\mathrm{V}$. Owing to the capacity asymmetry, a steady-state SoC offset remains that is consistent with the unequal stored energy. Dashed vertical markers ① to ⑦ correspond to the scenario steps in Table 5.3. Adapted from [J1].

The SoC difference enters the $1\,\%$ tolerance band at FPT $t_\varepsilon = 186.71\,\mathrm{s}$, as defined in Section 5.2.1 and indicated in Figure 5.7(a). In the subsequent quasi-stationary phase $t \geq t_\varepsilon$, a residual SoC offset $\Delta_{\mathrm{SoC}}^{\mathrm{res}}$ of up to $3.25\,\%$ persists. This offset is physically consistent with the asymmetric storage capacities and

reflects an expected steady-state behavior, where the larger battery stores and delivers approximately twice the energy of the smaller one.

At first glance, the power sharing appears unbalanced due to the visible mismatch ΔP between the battery power trajectories. However, a capacity-weighted analysis, illustrated by the gray dashed line in Figure 5.7(b), reveals that the apparent mismatch is primarily a result of the capacity asymmetry. When scaled to their respective storage ratings, both BESSs contribute proportionally to their capacity. Battery 2, being half the size of Battery 1, consistently provides approximately half the power. This confirms that the SoG control ensures coordinated and proportional power sharing even under capacity asymmetry.

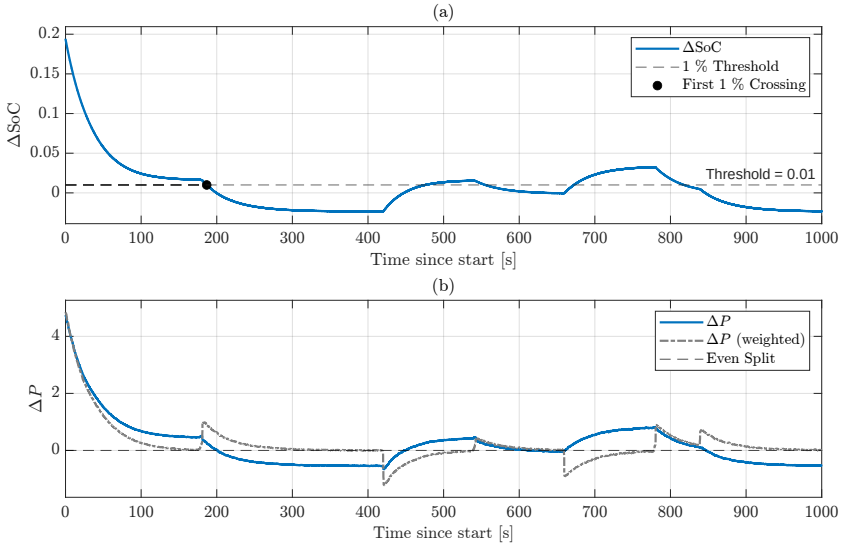


Figure 5.7: Analysis corresponding to Figure 5.6. (a) Absolute SoC difference $\Delta\mathrm{SoC}$ with a $1\,\%$ reference (dashed) and the FPT t_ε if applicable. (b) Relative power mismatch with respect to an even split. Due to capacity asymmetry, $\Delta\mathrm{SoC}$ settles to a small steady-state offset that is consistent with the unequal stored energy, while the power sharing remains coordinated across operating points.

Nevertheless, the unweighted residual relative power mismatch Δ_P^{res} reaches instantaneous deviations of up to $8.05\,\%$, which is significantly higher than in

the symmetric case. This again reflects the impact of the underlying capacity difference, rather than a deficiency in the control concept. Throughout the experiment, the DC-bus voltage remains stable within $1.79\,\%$ of its nominal value, with transient deviations during load and PV steps (Figure 5.6(a)) being rapidly corrected by the controller. The battery power flows P_{B1} and P_{B2} dynamically adjust to the seven predefined operating intervals (Figure 5.6(c)), while maintaining the SoC balancing process despite the inherent asymmetry of the BESSs.

These results demonstrate that the SoG-based control also achieves robust SoC convergence and maintains the DC-bus voltage within acceptable limits in the presence of asymmetric storage capacities. However, the residual SoC difference and power mismatch remain significantly higher compared to the symmetric case, which is attributable to the unequal energy storage capabilities of the two units.

(iii) Configuration with Asymmetric Storage Capacities and PI-based SoG Control

To mitigate the stationary mismatch observed in the SoG-based control under asymmetric storage capacities, an additional experiment is conducted applying the PI-based SoG voltage mapping, as described in Section 3.2.1, to the same configuration. The two BESSs retain the asymmetry $Q_1 = 1.0\,\mathrm{Ah}$ and $Q_2 = 0.5\,\mathrm{Ah}$, while the control incorporates an integral component to eliminate steady-state errors. The time evolution of the SoC, battery power flows, DC-bus voltage, and power exchanges is shown in Figure 5.8. The integral action successfully removes the steady-state SoC offset, resulting in convergence of both SoCs. Minor oscillations arise around changes in the operating point due to the integral term acting predominantly on the larger BESS. These oscillations remain bounded, and the DC-bus voltage V_{DC} stays close to its nominal value of $700\,\mathrm{V}$, with variations between $691.3\,\mathrm{V}$ and $708.3\,\mathrm{V}$, corresponding to symmetric deviations of about $\pm 1.2\,\%$. Compared to the previous experiment

without integral action, the lower voltage deviation is significantly reduced, highlighting the improved regulation achieved by the PI-based extension.

Compared to the SoG control case, the FPT time t_ε at which the SoC difference first falls below the $1\,\%$ tolerance band is significantly reduced to $22.92\,\mathrm{s}$, as shown in Figure 5.9(a). However, due to the faster response and the accumulating integral action of the controller, an overshoot is observed after t_ε, resulting in a temporary SoC deviation of up to $9.8\,\%$. This overshoot gradually diminishes, and by $186.71\,\mathrm{s}$ the residual SoC difference decreases to $1.63\,\%$, substantially lower than in the SoG-based control case at the same time.

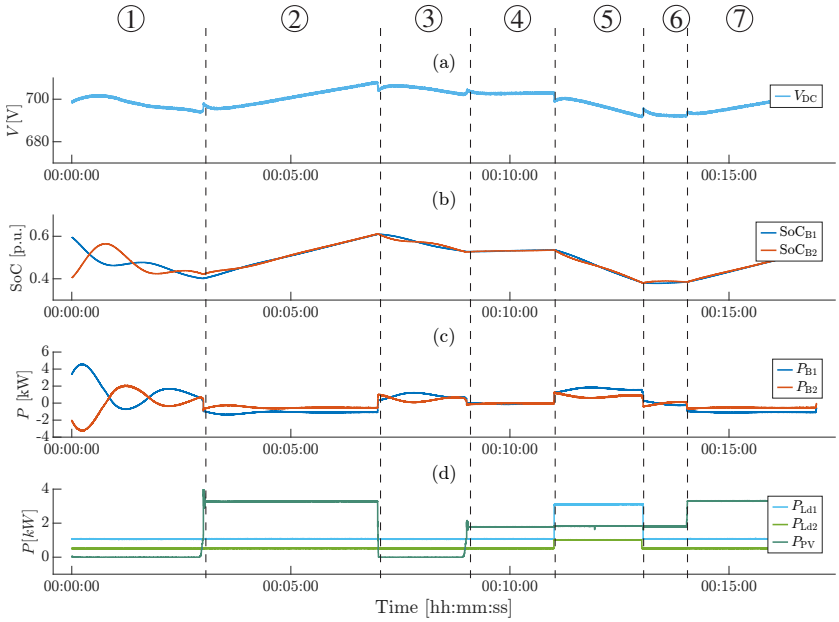


Figure 5.8: Time evolution of (a) DC-bus voltage, (b) SoC, (c) Battery powers, and (d) PV and load powers for the asymmetric capacity case with $Q_1 = 1.0\,\mathrm{A\,h}$ and $Q_2 = 0.5\,\mathrm{A\,h}$ with PI-based SoG control. The integral action removes the steady-state SoC offset and achieves complete equalization. Small oscillations occur around the operating-point changes due to the integral action acting on the dominant BESS; they remain bounded, and V_{DC} stays near 700 V. Dashed vertical markers ① to ⑦ correspond to the scenario steps in Table 5.3. Adapted from [J1].

The residual relative power mismatch Δ_P^{res} remains at similar peak levels compared to the SoG-based control, reaching maximum instantaneous deviations of approximately $22.76\,\%$, as illustrated in Figure 5.9(b). As with the SoG-based control, these extreme deviations occur primarily during load and PV transitions and diminish over time, highlighting the ability of the control to redistribute power dynamically.

These results demonstrate that while the integral component effectively reduces the steady-state SoC mismatch and improves the balancing accuracy in the quasi-stationary phase, it introduces pronounced transient overshoots and oscillations during dynamic operating intervals, reflecting the typical trade-off between steady-state accuracy and transient performance in PI-controlled systems.

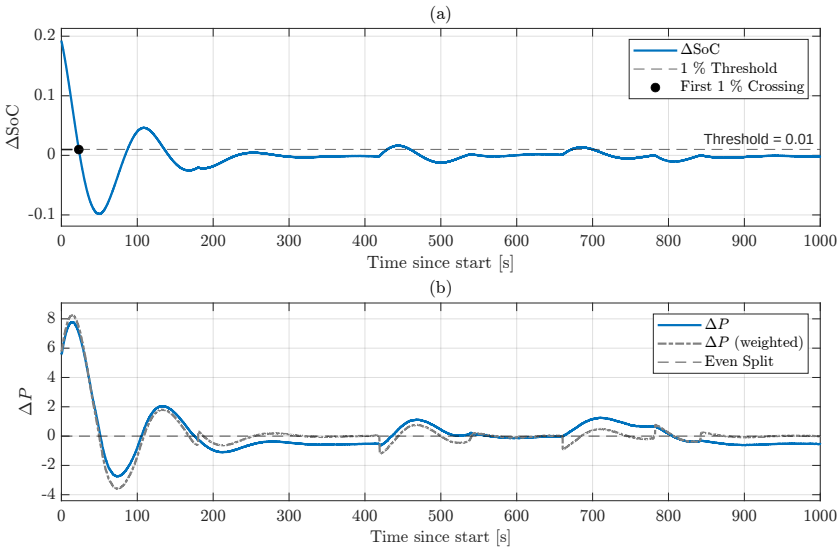


Figure 5.9: Analysis corresponding to Figure 5.8. (a) Absolute SoC difference ΔSoC with a $1\,\%$ threshold (dashed) and the FPT t_ε marked by the dot. (b) Relative power mismatch (blue) and weighted power mismatch (grey), both with respect to an even split over time. The integral action drives ΔSoC below $1\,\%$ within t_ε and both metrics converge close to zero; transient oscillations remain bounded.

(iv) Configuration with Asymmetric Line Resistances

In this experiment, the robustness of the SoG-based control is evaluated under asymmetric line impedances by increasing the resistance on the side of Battery 1 to $R_{\mathrm{B1}} = 2.5\,\Omega$. This scenario reflects practical situations with unequal cabling or contact resistances, which distort the locally perceived SoG measurement and thus affect the balancing dynamics. Figure 5.10 shows the time evolution of voltages, SoC, battery powers, and power flows under this condition. The FPT time t_ε is determined to be $55.56\,\mathrm{s}$, as indicated in Figure 5.11(a). In the quasi-stationary phase $t \geq t_\varepsilon$, the residual SoC difference remains slightly

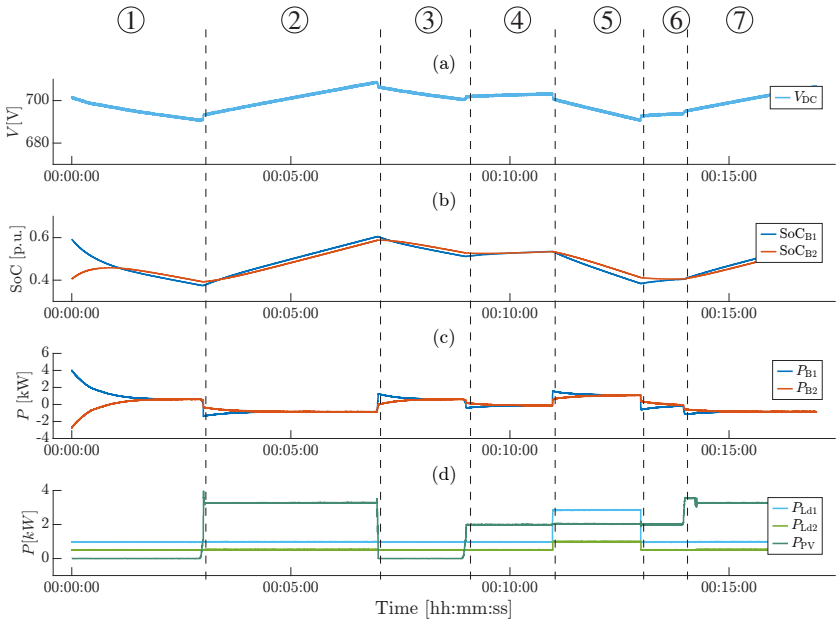


Figure 5.10: Time evolution of (a) DC-bus voltage, (b) SoC, (c) Battery powers, and (d) PV and load powers with increased line resistance on storage 1 ($R_{\mathrm{B1}} = 2.5\,\Omega$). The additional drop across R_{B1} perturbs the local SoG signal and biases the SoC-to-V mapping, which slows the balancing dynamics and leads to a persistent steady-state SoC offset, while the trajectories remain coordinated across operating points. Dashed vertical markers ① to ⑦ correspond to the scenario steps in Table 5.3. Adapted from [J1].

above the threshold, with a maximum of $1.75\,\%$, suggesting that the control partially compensates the imbalance despite the distorted signal. The residual relative power mismatch Δ_P^{res} exhibits peak values of approximately $11.83\,\%$, as depicted in Figure 5.11(b). However, these extreme relative deviations occur only during periods of very low total power, as evident from the absolute power traces in Figure 5.10(c), where small absolute differences translate into disproportionately large relative percentages. Over time, the controller mitigates these mismatches dynamically, confirming its effectiveness even under challenging conditions.

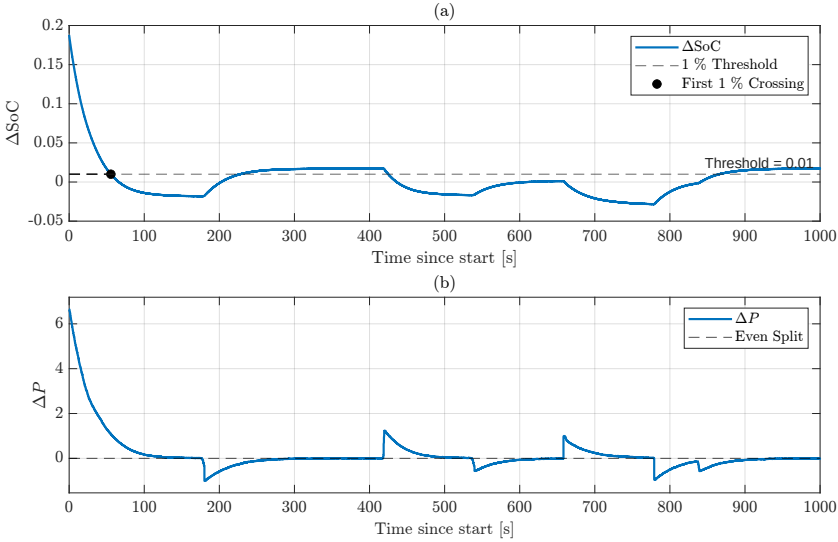


Figure 5.11: Analysis corresponding to Figure 5.10. (a) Absolute SoC difference $\Delta\mathrm{SoC}$ with a $1\,\%$ threshold (dashed) and the FPT t_ε indicated by the dot if the threshold is reached. The additional drop across R_{B1} biases the local SoG signal and yields a persistent steady-state SoC offset. (b) Relative power mismatch with respect to an even split over time; sharing remains coordinated across operating points.

Throughout the experiment, the DC-bus voltage remains close to its nominal value of $700\,\mathrm{V}$, with variations between $690.3\,\mathrm{V}$ and $708.6\,\mathrm{V}$, corresponding to deviations of $-1.4\,\%$ and $1.2\,\%$ despite the distorted conditions, underscoring

the resilience of the system. The power flows P_{B1} and P_{B2} exhibit asymmetric behavior corresponding to the increased resistance of unit 1, yet both contribute to the balancing process.

These results demonstrate that the SoG-based control maintains acceptable SoC balancing and voltage stability even in the presence of significant line asymmetry. Nevertheless, both the steady-state and transient metrics indicate a slight degradation compared to the symmetric reference case, which is attributable to the distorted local voltage feedback.

(v) Configuration with Asymmetric Line Resistances and PI-based Control

To further improve the balancing performance under asymmetric line impedances, the PI-based SoG mapping, as introduced in Section 3.2.1, is applied to the configuration with $R_{\mathrm{B1}} = 2.5\,\Omega$. The integral control component is intended to compensate the distortion of the local SoG signal caused by the increased voltage drop, thereby enhancing the balancing accuracy in the quasi-stationary phase.

Figure 5.12 depicts the time evolution of voltages, SoC, battery powers, and power flows under this condition. The FPT time t_ε, i.e., the point at which the SoC difference falls below $1\,\%$ and remains within this bound, is reduced to $28.05\,\mathrm{s}$, compared to $55.56\,\mathrm{s}$ without PI control, demonstrating the improved convergence rate.

However, in the quasi-stationary phase $t \geq t_\varepsilon$, the maximum SoC deviation initially remains elevated at approximately $3.37\,\%$ due to overshoot and oscillations introduced by the integral action. These oscillations gradually decay, and after approximately $250\,\mathrm{s}$, the deviation settles below $1.2\,\%$, as shown in Figure 5.13(a).

The residual relative power mismatch Δ_P^{res} reaches peak values of about $3.5\,\%$, which occur primarily during periods of very low total power output, where even

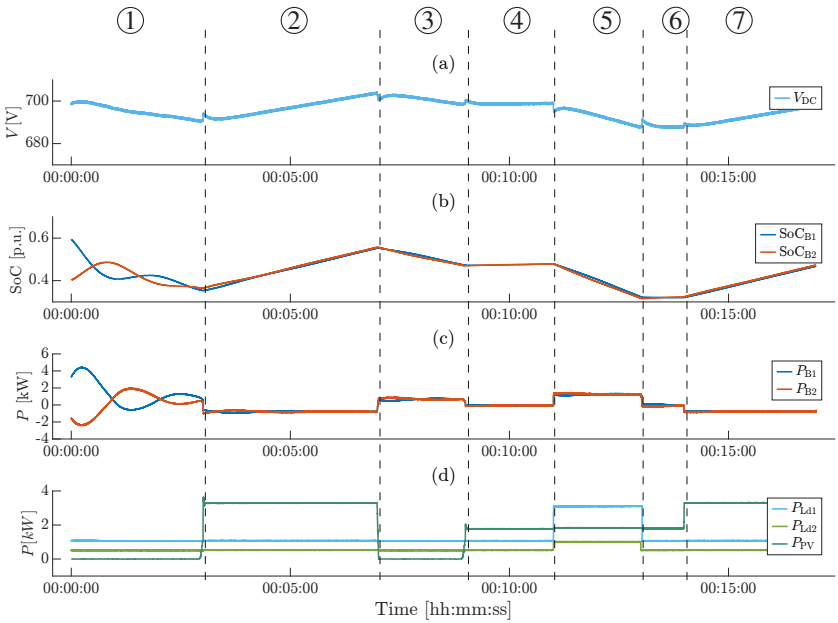


Figure 5.12: Time evolution of (a) DC-bus voltage, (b) SoC, (c) Battery powers, and (d) PV and load powers with increased line resistance on storage 1 ($R_{B1} = 2.5\,\Omega$) under PI SoG control. The integral action compensates the bias introduced by the additional drop across R_{B1}, removes the steady-state SoC difference, and achieves complete equalization, while V_{DC} remains near 700 V. Transient overshoot and mild oscillations appear around operating-point changes, consistent with the asymmetric capacity case. Dashed vertical markers ① to ⑦ correspond to the scenario steps in Table 5.3. Adapted from [J1].

minor absolute differences appear disproportionately large when normalized. This behavior is consistent with the observations in the SoG-based control variant and is evident in the absolute power profiles in Figure 5.12(c).

Throughout the experiment, the DC-bus voltage remains within a deviation of $1.82\,\%$ from nominal, confirming stable voltage regulation despite the asymmetric conditions and the more aggressive control action.

These results confirm that the PI-based SoG control improves the steady-state balancing accuracy and reduces the FPT time compared to the SoG-based

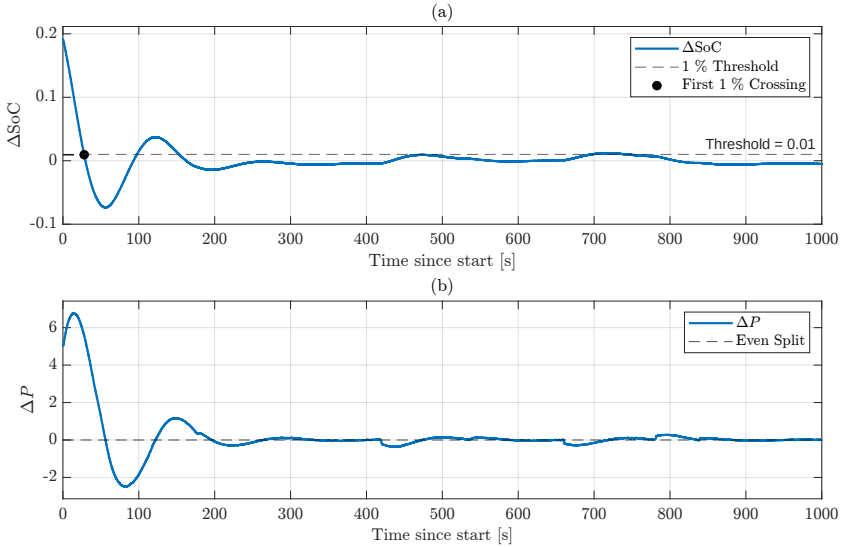


Figure 5.13: Analysis corresponding to Figure 5.12. (a) Absolute SoC difference $\Delta\mathrm{SoC}$ with a $1\,\%$ threshold (dashed) and the FPT t_ε marked. (b) Relative power mismatch with respect to an even split over time. The integral action compensates the bias introduced by the increased line resistance on storage 1 and drives $\Delta\mathrm{SoC}$ below $1\,\%$ within t_ε; the mismatch settles near zero with bounded oscillations around operating-point changes.

control, even under asymmetric line resistances. Nevertheless, the enhanced performance comes at the cost of transient overshoots and oscillations, reflecting the typical trade-off between fast convergence, steady-state accuracy, and transient stability in PI-controlled systems.

5.3.2 Scenario II: SoG-Based Control with additional AC-connected Battery

This scenario extends the configuration shown in Figure 5.3 by including an additional battery on the AC side, which is coupled to the AC system via a grid-forming IC. The IC establishes the secondary voltage and frequency reference

for the local AC network and enables the SoC-frequency mapping derived in Section 3.2.2 through deliberate frequency deviations.

At the beginning of the experiment, the three BESSs are initialized with different states of charge ($\mathrm{SoC}_{\mathrm{B1}} = 60\%$, $\mathrm{SoC}_{\mathrm{B2}} = 40\%$, $\mathrm{SoC}_{\mathrm{B3}} = 50\%$). During the test, four predefined operating intervals are executed to represent distinct steady-state and transient conditions. The corresponding PV and load setpoints are summarized in Table 5.4, and the temporal evolution of the operating points is indicated in Figure 5.14.

Table 5.4: Power setpoints in Scenario II experiment

	①	②	③	④
P_{PV} [kW]	1.25	3.3	3.3	3.3
$P_{\mathrm{DC,Ld}}$ [kW]	1.5	1.5	1.5	1.5
$P_{\mathrm{AC,Ld}}$ [kW]	0.75	1.5	2.5	1.5

Figure 5.15 presents the quantitative evaluation of the SoC difference and the residual relative power mismatch under these conditions. The FPT time t_ε, defined as the time at which the maximum SoC difference permanently falls below $1\,\%$, is determined to be approximately $535.59\,\mathrm{s}$. In the quasi-stationary phase ($t \geq t_\varepsilon$), the residual SoC difference remains slightly above the nominal threshold, with a maximum of $1.7\,\%$, suggesting that the inter-domain balancing is subject to minor steady-state inaccuracies compared to the purely AC scenarios.

The maximum relative power mismatch Δ_P^{res} reaches peak values of approximately $12.9\,\%$ during transients but remains within $1.14\,\%$ in the quasi-stationary phase. As in previous scenarios, the transient peaks coincide with periods of low absolute power levels, where small absolute deviations translate into large relative percentages.

Throughout the experiment, the DC-bus voltage remains between $683.8\,\mathrm{V}$ and $709.6\,\mathrm{V}$, corresponding to deviations of $-2.3\,\%$ and $+1.4\,\%$ during the applied

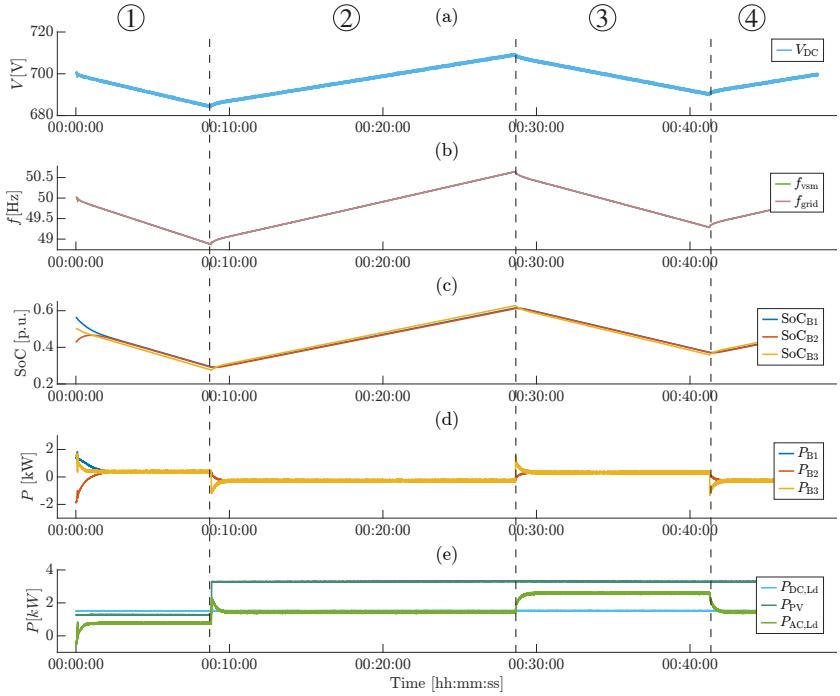


Figure 5.14: SoG coordinated operation with an additional AC connected battery (via a GFM IC). Time evolution of (a) DC-bus voltage V_{DC}, (b) VSM frequency f_{vsm} and grid frequency f_{grid}, (c) states of charge of the three BESSs, (d) Battery powers P_{B1}–P_{B3}, and (e) PV, DC, and AC load powers. The SoG control yields coordinated SoC trajectories across the DC and AC domains and enables proportional energy sharing, while V_{DC} remains near 700 V. The VSM tracks f_{grid} during operating point changes. Dashed vertical markers ① to ④ correspond to the steps in Table 5.4. Adapted from [J7].

disturbances. Similarly, the AC bus frequency remains centered around its nominal value of 50 Hz, with variations between 48.9 Hz and 50.6 Hz, corresponding to deviations of $-2.2\,\%$ and $+1.3\,\%$. Overall, the results highlight that both SoG variables, DC-bus voltage and AC frequency, exhibit bounded and comparable deviations from their nominal setpoints, underscoring the consistent performance of the proposed SoG-based control framework across domains. These results demonstrate that the proposed SoG-based control successfully extends to

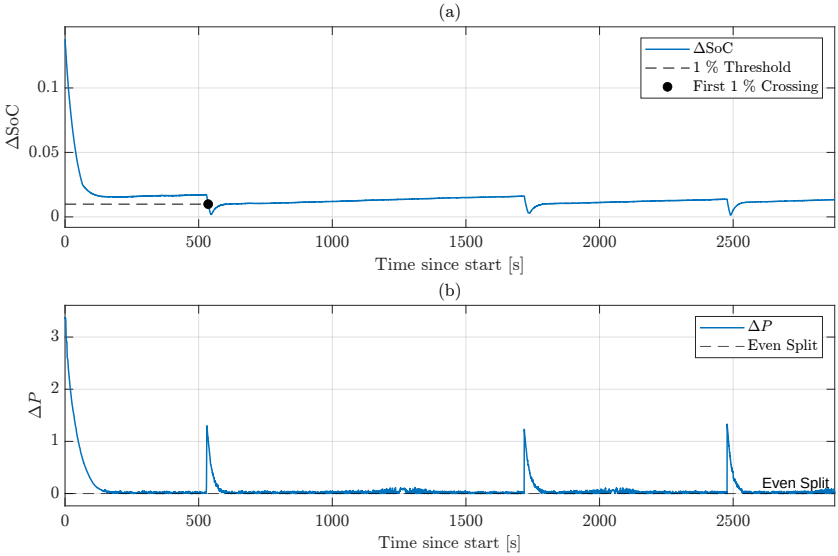


Figure 5.15: Analysis corresponding to Figure 5.14. (a) SoC spread across the three BESSs, as defined in (5.1), with a 1 % threshold (dashed) and the FPT t_ε marked. (b) Residual relative power mismatch with respect to the sharing target (even split) across the DC and AC domains.

hybrid AC/DC systems, achieving coordinated balancing among three BESSs. While the dynamic and steady-state performance slightly degrades compared to the symmetric DC-only reference case, the system maintains acceptable accuracy and stability under the more complex inter-domain operating conditions.

To further examine the origin of the residual discrepancies, Figure 5.16 depicts the pairwise differences in state of charge (Δ_{SoC}) and instantaneous battery power (ΔP) among the three BESSs. The plot reveals that the largest transient peaks and the dominant part of the steady-state residual error originate from the differences Δ_{1-3} and Δ_{2-3}, i.e., from the deviations between the DC side and AC side BESSs. This observation is consistent with the additional conversion stages and the cumulative effect of line resistances and converter impedances that are present along the AC coupling path. In contrast, the purely DC-side difference Δ_{1-2} remains comparatively small and converges faster, highlighting

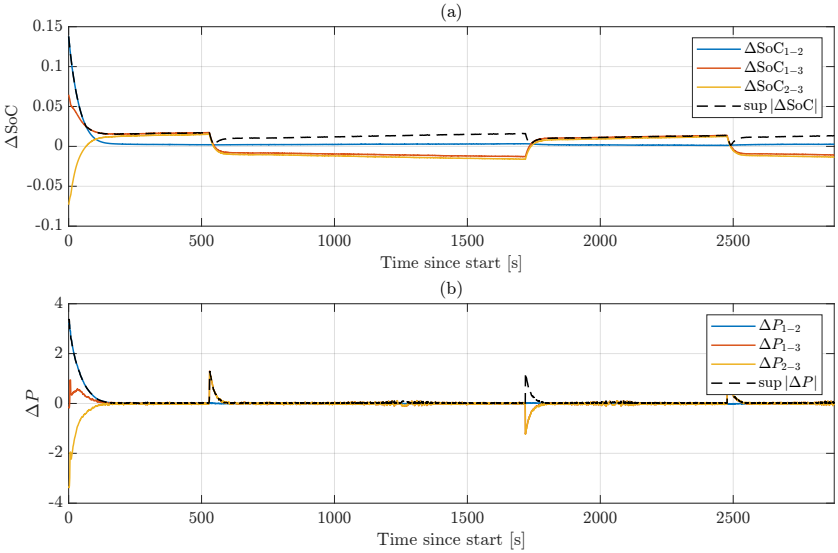


Figure 5.16: Pairwise differences for Scenario II, corresponding to Figure 5.14. (a) Pairwise SoC differences Δ_{1-2}, Δ_{1-3}, Δ_{2-3}; the envelope shows the supremum norm $\|\Delta\|_\infty = \sup_t |\Delta(t)|$, together with a 1 % reference (dashed). (b) Pairwise instantaneous battery power differences ΔP. The largest peaks and the dominant contribution to the steady-state residual stem from Δ_{1-3} and Δ_{2-3} (DC vs. AC side), whereas the purely DC-side difference Δ_{1-2} remains smaller and settles faster.

that the inter-domain coupling is the main source of the observed residual error. These findings confirm that the SoG-based control maintains coordinated operation also in the presence of non-negligible AC/DC interface dynamics, although at the expense of slightly increased balancing effort compared to the DC-only configuration.

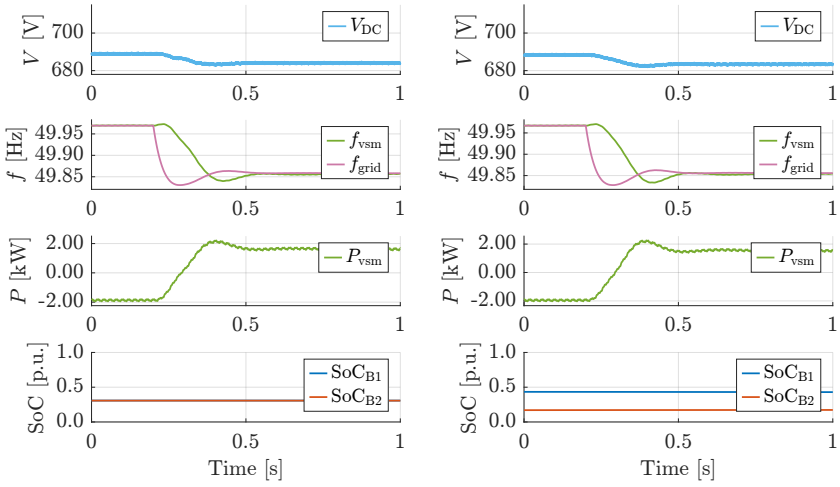
5.3.3 Scenario III: SoG-Based VSM with Frequency Support

This scenario extends the SoG-based control by integrating a VSM control, as described in Section 4.1, on the AC side to demonstrate inertial behavior

during dynamic events. While frequency support through VSMs has already been widely investigated in the literature, including standardized test procedures such as those in [110, 132], the novelty here lies in showing that the IC provides frequency support proportional to the mean SoC of the DC-side BESSs.

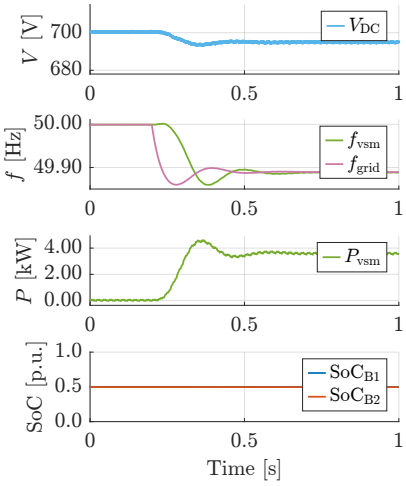
To this end, the experimental setup shown in Figure 5.3 is augmented by an AC-connected battery, interfaced through a grid-forming IC. The IC supplies the AC side with both the voltage and frequency reference and enables the mapping of the collective SoC state of the AC microgrid onto the AC frequency, following the approach derived in Section 3.2.2. A sudden AC load increase from 1.2 kW to 2.5 kW triggers the system response.

Six experiments are conducted to assess the system behavior at three different average SoC levels: low, medium, and high. For each SoC level, a pair of

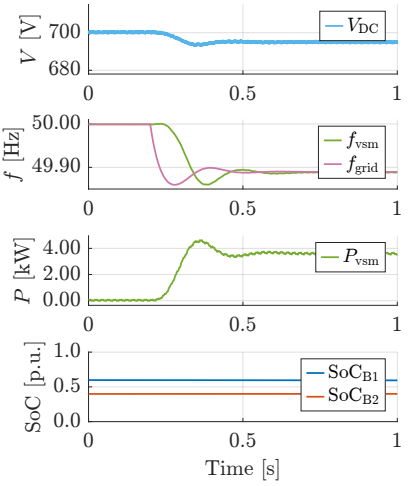


(a) $SoC_1 = SoC_2 = 0.3$ **(b)** $SoC_1 = 0.43, SoC_2 = 0.17$

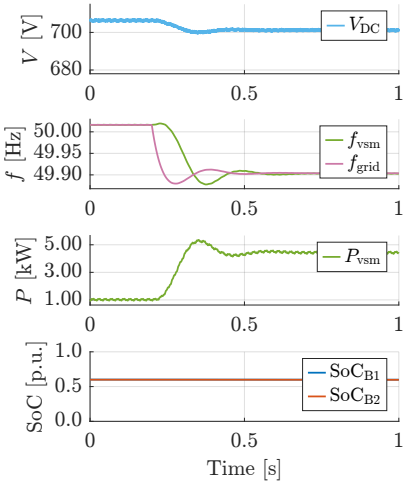
Figure 5.17: Experimental responses to an artificially induced frequency drop at different states of charge. Each panel shows how the AC microgrid, via the SoG-based VSM, adjusts its power contribution according to the available energy. Subfigures correspond to different SoC settings: (a) $SoC_1 = SoC_2 = 0.3$, (b) $SoC_1 = 0.43, SoC_2 = 0.17$, (c) $SoC_1 = SoC_2 = 0.5$, (d) $SoC_1 = 0.6, SoC_2 = 0.4$, (e) $SoC_1 = SoC_2 = 0.6$, (f) $SoC_1 = 0.72, SoC_2 = 0.465$. Adapted from [J2].



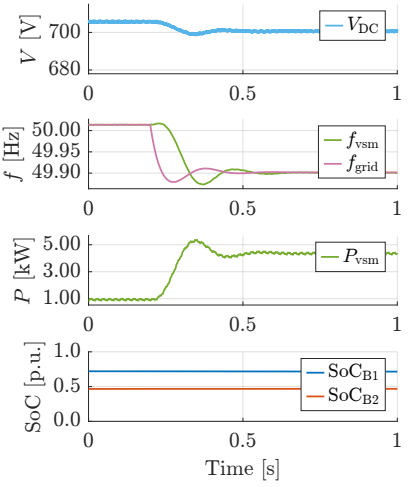
(c) $\mathrm{SoC}_1 = \mathrm{SoC}_2 = 0.5$



(d) $\mathrm{SoC}_1 = 0.6, \mathrm{SoC}_2 = 0.4$



(e) $\mathrm{SoC}_1 = \mathrm{SoC}_2 = 0.6$



(f) $\mathrm{SoC}_1 = 0.72, \mathrm{SoC}_2 = 0.465$

Figure 5.17: Frequency-drop responses at additional SoC settings (continued).

experiments is performed: one with symmetrically distributed SoCs between the two DC-side BESSs and one with asymmetrically distributed SoCs but similar mean values. For example, tests (a) and (b) both correspond to a mean SoC of 0.3, with configurations of ($\mathrm{SoC}_1 = \mathrm{SoC}_2 = 0.3$) and ($\mathrm{SoC}_1 = 0.43, \mathrm{SoC}_2 = 0.17$), respectively. Similar pairings are carried out for medium (c, d) and high (e, f) SoC levels.

The results in Figure 5.17 confirm two key findings. First, within each pair of experiments, the response of the IC is primarily governed by the mean SoC, and not by its distribution among the BESSs. This demonstrates that the SoG-based VSM correctly reflects the aggregate energy content of the DC-side BESSs. Second, comparing across different mean SoC levels reveals that a higher mean SoC enables stronger frequency support. For instance, in the low SoC case (a), the frequency nadir reaches $49.8608\,\mathrm{Hz}$, corresponding to a deviation of $0.1392\,\mathrm{Hz}$. In contrast, under identical load conditions but with a higher mean SoC of 0.6 (e), the nadir improves to $49.8667\,\mathrm{Hz}$, i.e., a deviation of only $0.1333\,\mathrm{Hz}$. This corresponds to a relative improvement of approximately $4.24\,\%$.

These findings demonstrate that the SoG-based control enables the IC to inherently account for the mean energy state of the connected BESSs. As a result, the frequency support is both proportional and adaptive, providing a higher level of stabilization when more energy is available, while maintaining robust performance in all tested configurations without requiring communication.

5.3.4 Scenario IV: SoG-Based Control with GSL in DC Microgrid

This experiment investigates the contribution of the GSL concept to stabilize the DC-bus voltage. To isolate the GSL effect from AC-side dynamics, the microgrid operates in islanded mode and dynamic support by the IC is disabled. GSLs

are particularly relevant under constrained supply conditions, accordingly, AC-side support is suppressed to highlight the GSL contribution independent of IC dynamics.

Two experiments are conducted in this scenario. In both cases, a resistive load ($\Delta P_{\mathrm{Ld}} = 4\,\mathrm{kW}$) is connected directly to the DC-bus at $t = 0.1\,\mathrm{s}$ to induce a voltage sag. In the first experiment (Figure 5.18), the post-step total demand remains below the aggregate power capability of the batteries. In the second experiment (Figure 5.19), the post-step demand exceeds the instantaneous power available under the current limits of the BESSs and PV interfacing converters.

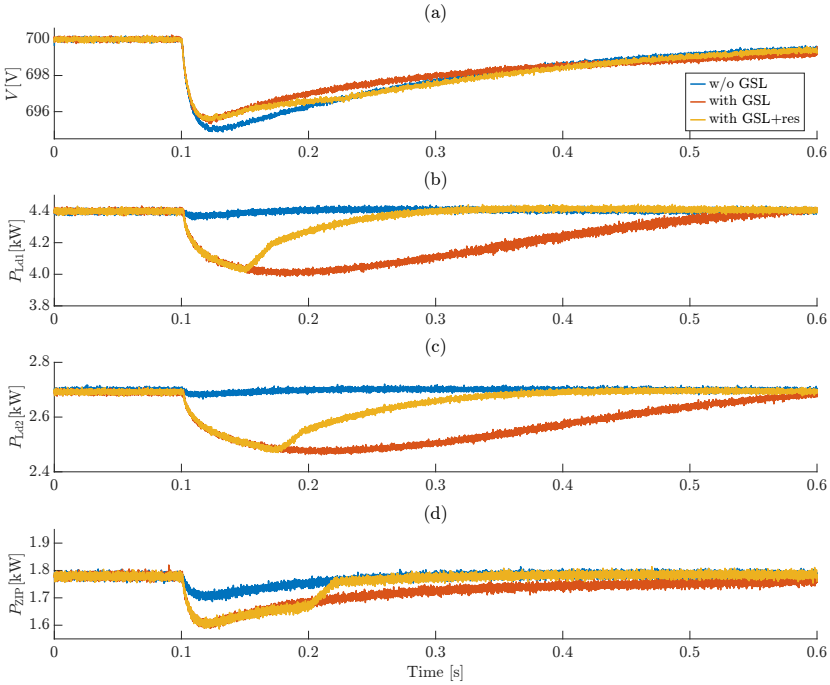


Figure 5.18: Voltage and power responses to a load step in the DC microgrid for three cases: baseline without GSL, with GSL, and with GSL plus restoration activation (see legend). The GSL attenuates the bus-voltage excursion by $13.11\,\%$ while requiring only $10\,\%$ variation in its power consumption; with restoration enabled, the load smoothly returns to nominal after support. Adapted from [J3].

This worst-case condition is chosen to accentuate the stabilizing contribution of the GSL. Thereby three configurations are compared: (i) without GSL, (ii) with GSL responding proportionally to the detected voltage drop, and (iii) with GSL including the restoration function introduced in Section 4.2.2. Figure 5.18 illustrates the stabilizing effect of the GSL under normal conditions. The setup comprises three loads, P_{Ld1}, P_{Ld2}, and P_{ZIP}. P_{Ld1} and P_{Ld2} are converter interfaced resistive loads with nominal powers of $4.4\,\mathrm{kW}$ and $2.7\,\mathrm{kW}$, respectively. P_{ZIP} is implemented as a ZIP load with equal weights $w_{\mathrm{Z}} = w_{\mathrm{I}} = w_{\mathrm{P}} = 0.33$ and a nominal power of $1.8\,\mathrm{kW}$. In the first case (Figure 5.18), without GSL the

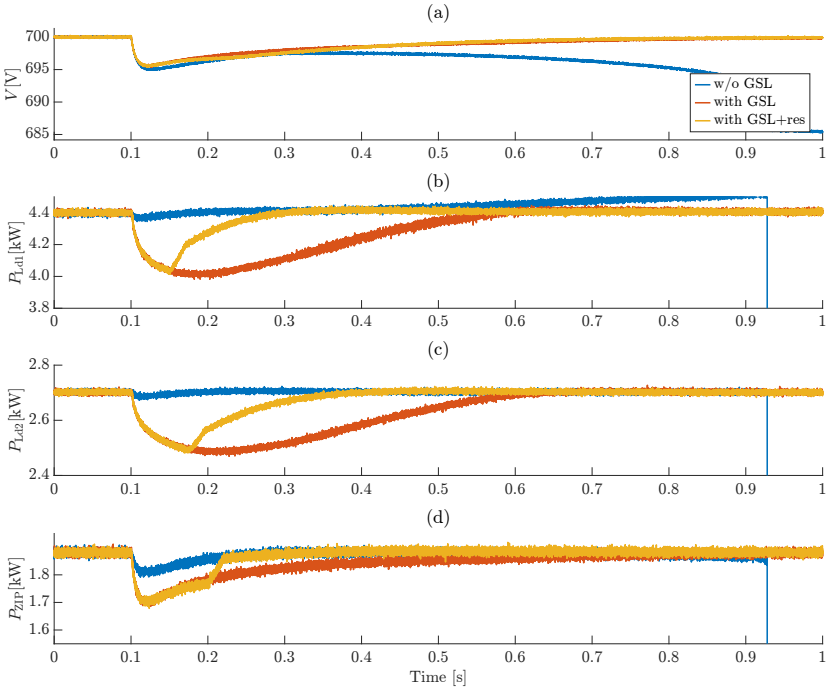


Figure 5.19: Worst-case overload in which total demand exceeds the aggregate available power from PV and storage. Responses are shown for three cases: baseline without GSL, with GSL, and with GSL plus restoration activation (see legend). Without GSL, the DC-bus voltage becomes unstable. Activating the GSL curtails consumption and preserves stability; with restoration enabled, the load returns smoothly toward nominal once the overload clears. Adapted from [J3].

DC-bus voltage drops by $5.102\,\mathrm{V}$ to $694.89\,\mathrm{V}$. With active GSL, the minimum improves to $695.56\,\mathrm{V}$, which corresponds to a $13.11\,\%$ reduction of the peak voltage deviation, achieved with only a $10\,\%$ temporary variation in the GSL power. The GSL with restoration control achieves a similar improvement in the reduction of the voltage drop. The restoration thresholds were intentionally chosen to trigger during the transient event, in order to reveal their influence on the recovery process. As seen in Figure 5.18, P_{Ld1} initiates restoration at approximately $1.5\,\mathrm{s}$, P_{Ld2} at about $1.75\,\mathrm{s}$, and P_{ZIP} at around $2.0\,\mathrm{s}$. Overall, restoration introduces a delayed action on the voltage recovery because the load power is driven back to its nominal value while the bus is still settling.

These observations underline the effectiveness of the GSL in mitigating voltage sags with minimal intervention, even for loads that can provide only limited support and must return to their nominal operating point.

In the second experiment (Figure 5.19), the post-step demand drives the battery converters into their current-limited region. In the baseline without GSL, the condition $P_{\mathrm{dem}} > P_{\mathrm{avail}}(t)$ is met as V_{DC} declines, the bus crosses the protection threshold V_{prot}, and the system trips at $t = 0.927\,\mathrm{s}$. With the GSL enabled, voltage-contingent curtailment reduces P_{dem} such that $P_{\mathrm{dem}} \leq P_{\mathrm{avail}}(t)$ holds throughout the event, maintaining $V_{\mathrm{DC}} > V_{\mathrm{prot}}$ and preventing shutdown. After the overload subsides, the restoration drives the GSL back to its nominal power without adverse transients.

5.4 Summary and Discussion of Results

The experimental results presented in this chapter address the research objectives and challenges outlined in Section 2.5, namely: the integration of decentralized, communication-free SoC balancing, hybrid AC/DC operation, grid-supportive behavior through VSM and GSL, and robust performance under realistic operating conditions, combined in a unified control concept. The findings demonstrate that these objectives were achieved despite the challenges

of heterogeneous storage capacities, asymmetric line impedances, and dynamic load and generation conditions. The underlying data and scripts for all experiments in this chapter are publicly available in [D1].

Across the four scenarios, several key observations can be stated:

- **SoC balancing:** In Scenario I, the SoG-based control achieves fast and robust SoC equalization even under dynamic PV and load changes. Symmetric configurations result in the smallest residual mismatches and the most balanced power sharing. Asymmetric storage capacities and line impedances introduce predictable challenges, higher steady-state SoC and power mismatches, yet the control maintains acceptable performance. The introduction of a PI component improves steady-state accuracy and reduces FPTs, but at the cost of overshoots and oscillations during transients. These findings reflect the inherent trade-off between transient and steady-state performance typical for PI-based SoG controllers.
- **AC/DC coupling and SoC-frequency mapping:** Scenario II illustrates that the SoG-based control extends to hybrid AC/DC systems and supports coordinated energy balancing across domains. The frequency deviations introduced by the IC reflect the collective SoC and facilitate cross-domain power sharing, although with slightly degraded precision compared to the DC-only case.
- **Frequency support through VSM:** In Scenario III, the integration of a SoG-based VSM demonstrates that the frequency support provided by the IC is proportional to the mean SoC of the DC-side BESSs, independent of their distribution. This confirms that the SoG mapping reliably informs the AC-side inertia-like behavior without the need for additional communication.
- **GSL:** Finally, Scenario IV highlights the potential of GSLs to mitigate voltage sags and maintain stability during extreme load events. The GSL achieves significant improvement of voltage restoration with minimal power reduction and even prevents system instability in worst-case

conditions. These results underline the value of GSLs as a fast and local support mechanism, especially in constrained or islanded microgrid conditions.

These findings collectively validate the main hypotheses of this dissertation:

1. The SoG-based framework enables effective and communication-free SoC balancing.
2. It extends naturally to hybrid AC/DC systems while maintaining acceptable performance.
3. The combination with VSM and GSL functionalities further enhances grid-supportive behavior and resilience, both in steady-state and during transients.

While the control concept performed robustly in all tested scenarios, some limitations and trade-offs deserve attention. The PI-based mapping improves steady-state SoC convergence but introduces overshoot and oscillations, which must be tuned appropriately for specific applications. The observed high relative power mismatches during periods of very low absolute power highlight the sensitivity of normalized metrics in such conditions and suggest that absolute as well as relative indicators should be considered.

Moreover, while the experiments focus on the DC microgrid and the local AC interlink, the broader interaction with large, constrained AC grids is not explicitly tested here. Future work could extend the validation to scenarios with realistic grid impedance and more complex AC-side dynamics.

In summary, the experimental results confirm that the SoG-based control concepts developed in this dissertation meet the design objectives of decentralization, scalability, and grid-supportive behavior under realistic and challenging conditions. The combination of SoG-based balancing, VSM-like inertia, and fast-reacting GSLs offers a coherent and effective toolkit for the operation of future hybrid microgrids.

6 Summary, Conclusion, and Future Work

6.1 Summary

This dissertation addresses the challenge of coordinating Battery Energy Storage Systems (BESSs) in hybrid AC/DC microgrids in a fully decentralized, communication-free manner while (i) balancing the State-of-Charge (SoC) across the distributed BESSs, (ii) enabling synergistic coupling between DC and AC microgrids, and (iii) delivering grid-supportive behavior through virtual inertia in AC grids and demand-side support through Grid-Supportive Load (GSL). Starting from a systematic analysis of the control challenges and a critical review of existing methods, research gaps are identified in the integration of SoC balancing, grid support, and scalability in a unified framework without relying on centralized communication (Chapter 2).

To address these gaps, a State-of-Grid (SoG) control framework is developed that projects internal energy states into observable grid variables, DC voltage reference on the DC side and frequency reference on the AC side, so that BESSs and interface converters can self-organize using only local measurements (Chapter 3). The stability of the proposed SoG method is analyzed within a singular-perturbation framework, employing Lyapunov functions for the reduced slow subsystem and the boundary-layer dynamics. The closed-loop system is proven locally exponentially stable around the equilibrium, and explicit design constraints for the mapping gains and Proportional-Integral (PI) parameters are

derived, clarifying the required time-scale separation and admissible envelopes for implementation (Section 3.5).

The framework is extended with a SoG-based Virtual Synchronous Machine (VSM) for frequency support and with GSLs that stabilize DC voltage transients via Impedance / Current / Power (ZIP)-type load modulation and an energy-aware restoration strategy (Chapter 4).

The proposed framework is further validated experimentally in the Smart2DC laboratory, established as part of this dissertation, and tested under realistic boundary conditions. A structured evaluation methodology is specified in Section 5.2. It introduces quantitative performance metrics and a consistent set of test scenarios to enable reproducible and comparable experimental assessment under realistic operating constraints. Four representative scenarios demonstrate the feasibility and robustness of the proposed framework, including its ability to handle asymmetric storage capacities, heterogeneous line impedances, and dynamic load and generation profiles (Chapter 5).

On the DC side, the SoG-based control achieves SoC equalization among heterogenous BESSs while maintaining the bus voltage within admissible envelopes. The method remains effective in the presence of asymmetric line impedances and unequal capacities, and it does not rely on communication links. Two variants of the underlying voltage controller are investigated. The first is a basic proportional version, which can result in steady-state deviations in the presence of asymmetric batteries or line resistances. The second is a PI-based version, which compensates these deviations but can introduce small overshoot during the initial equalization process (Section 5.3.1).

For cross-domain operation, a frequency-based mapping steers the interlink power according to an SoG mismatch between domains. This enables balancing across DC- and AC-connected storage while respecting local converter limits (Section 5.3.2). On the AC side, a SoG-based VSM provides frequency support with a magnitude that adapts to the available energy, resulting in improved nadir and recovery metrics under identical disturbances (Section 5.3.3).

Demand-side flexibility is incorporated through GSL on the DC-bus. A local load controller with saturation, hysteresis, and energy restoration reduces voltage excursions during disturbances and restores nominal service of critical loads in a controlled manner (Section 5.3.4). The combined results demonstrate that the proposed SoG concept forms a consistent and reproducible basis for decentralized coordination in hybrid microgrids.

6.2 Conclusion

The aim of this dissertation is to develop and validate a decentralized control framework for hybrid AC/DC microgrids that enables SoC balancing across distributed BESSs, coordinated AC-DC coupling, and concurrent grid-supportive behavior through virtual inertia and adaptive loads. In response to these research objectives, this dissertation provides the following contributions:

1. **Decentralized control methods for DC microgrids.** The proposed SoG-based controller achieves reliable SoC equalization and power sharing based solely on local measurements. This conclusion is substantiated by the experimental results presented in Section 5.3.1 (Scenario I).

   In the symmetric baseline (Scenario I (i)), the proposed scheme ensures effective power sharing and achieves SoC alignment. Across all variations in load and Photovoltaic (PV) injection, the DC-bus voltage V_{DC} remains centered at $700\,\mathrm{V}$ with deviations limited to $-2.0\,\%$ to $1.2\,\%$. After the First-Passage Time (FPT), both SoC trajectories evolve synchronously, and the residual deviation remains confined within $0.18\,\%$.

   In the case of asymmetric storage capacities (Scenario I (ii)) with $Q_1 = 1.0\,\mathrm{Ah}$ and $Q_2 = 0.5\,\mathrm{Ah}$, the controller maintains convergence of the SoC trajectories and weighted power sharing. A persistent steady-state deviation emerges, with Δ_{SoC} reaching up to $3.25\,\%$, which is notably higher than in the symmetric reference. Similarly, with asymmetric line

resistances (Scenario I (iv)), the SoC trajectories and power sharing remain coordinated, although a smaller, steady-state deviation persists. The residual offset in this case reaches $1.75\,\%$. The larger deviation under capacity asymmetry arises from physically consistent differences in energy ratings, whereas line asymmetry produces an apparent offset due to additional voltage drops across the resistances, which in turn bias the local SoG signal.

To mitigate the observed steady-state deviations, a small integral component is introduced into the underlying voltage controller. This modification eliminates the residual offset at the expense of transient overshoot. For asymmetric capacities (Scenario I (iii)), the FPT decreases significantly, accompanied by an initial overshoot. Throughout this scenario, the DC-bus voltage remains within approximately $\pm 1.2\,\%$ of its nominal. Likewise, for asymmetric line resistances (Scenario I (v)), the equalization time is reduced by the integral term.

In summary, the proportional SoG mapping ensures monotonic SoC convergence and effective power sharing. If residual steady-state offsets must be eliminated, the inclusion of integral action is beneficial, provided that moderate transient overshoots can be tolerated.

2. **Cooperative interaction strategies between DC and AC microgrids.** The proposed SoG-based control framework inherently enables decentralized cross-domain SoC balancing between DC and AC microgrids, by embedding the SoC of each BESS into voltage and frequency references. The experimental results presented in Section 5.3.2 and Section 5.3.3 underscore this conclusion.

   Scenario II confirms that two BESSs on the DC side and one on the AC side converge to a common SoC trajectory despite being initialized at different SoC ($\mathrm{SoC}_{B1} = 60\,\%$, $\mathrm{SoC}_{B2} = 40\,\%$, $\mathrm{SoC}_{B3} = 50\,\%$). The residual SoC deviation converges below $1\,\%$ and remains within $1.7\,\%$ in the quasi-stationary phase. Throughout the experiment, both the DC-bus voltage and AC frequency stay within tight bounds ($683.8\,\mathrm{V}$ to $709.6\,\mathrm{V}$,

48.9 Hz to 50.6 Hz), confirming robust and coordinated behavior across domains without any communication.

Furthermore, the control method is extended to provide virtual inertia support concurrent to the SoC-based coordination mechanism. The analysis and experiments in Section 5.3.3 (Scenario III) demonstrate that the inertial response of the Interlink Converter (IC) scales with the mean SoC of the DC-connected storage units and remains largely insensitive to its distribution. This confirms that the proposed SoG-based mapping allows the IC to incorporate SoC-dependent inertial behavior without communication, thereby achieving adaptive and grid-supportive coupling between DC and AC microgrids.

These findings verify that SoG-driven coupling enables fully decentralized, communication-free coordination of energy exchange and grid-supportive services across DC and AC domains. Taken together, this represents a significant advancement toward scalable, resilient hybrid microgrids where distributed storage units contribute autonomously to both energy balancing and frequency support.

3. **GSL for enhanced grid stability.** A fully decentralized controller for converter-interfaced ZIP loads is designed to provide fast voltage support based solely on local DC-bus voltage measurements. The control method shapes the output voltage of the load converter via a bounded hysteresis with saturation, allocates a finite support budget $E_{\mathrm{GSL}}^{\max}$, and triggers a deterministic energy-based restoration with the time constant T_{res}. The scheme is communication-free and compatible with the SoG-based BESS coordination and the interlink VSM (Chapter 4).

   Stability analysis in Section 4.2.3 and experimental results in Section 5.3.4 confirm the compatibility and positive impact of the proposed GSL method on system stability. In a $4\,\mathrm{kW}$ positive load step the minimum DC-bus voltage improves from $694.89\,\mathrm{V}$ to $695.56\,\mathrm{V}$. This corresponds to a $13.11\,\%$ reduction of the voltage sag with only a temporary $10\,\%$ power modulation of the GSL. Under worst-case overloads

beyond the aggregate source capability the controller preserves bus stability and maintains controllability. After mitigation the load returns smoothly to nominal within the configured restoration window T_{res}. The scheme operates fully decentralized and interoperates with the SoG storage coordination and the IC.

4. **Stability analysis and design conditions for the proposed control strategies.** The theoretical stability analysis presented in Section 3.5 confirms that the proposed SoG-based coordination scheme exhibits local exponential stability and, within the admissible operating domain constrained by saturating integrators and a strictly positive DC-bus voltage, semiglobal practical exponential stability. These results are established using Singular Perturbation Theory and Lyapunov arguments for the reduced-order and boundary-layer subsystems. For controller design, the dimensionless gain condition $0 < \sigma < 0.5\,\mathrm{SoC}_{\Delta,i}$ and the inequality in Equation (3.78) provide actionable tuning rules that translate directly into parameter selection. These tuning criteria ensure stable behavior and are compatible with practical implementation.

   In addition, the small-signal stability assessment of the proposed GSL controller, presented in Section 4.2.3, reveals improved damping for I- and Z-dominated ZIP load compositions, while P-dominated loads remain largely unaffected. Excessive tuning of the gain k_{GSL} yields diminishing returns, thereby justifying the use of moderate gains, as confirmed by the eigenvalue analysis. Taken together, these theoretical and numerical findings delineate a reliable and well-defined operating range for the proposed layered control architecture. They also explain the robust closed-loop behavior observed in the experiments presented in Chapter 5.

5. **Laboratory demonstrator and structured testing methodology for experimental validation.** To ensure the practical viability of the proposed control methods, a comprehensive experimental validation is conducted using the Smart2DC microgrid laboratory established specifically for this dissertation at the Smart Energy System Control Laboratory (SESCL) of

Karlsruhe Institute of Technology (KIT). The laboratory provides a modular and reconfigurable platform based on a non-isolated single-bus architecture comprising bidirectional Silicon Carbide (SiC)-based DC/DC converters, a three-phase AC interface, programmable ZIP loads, and PV emulation units. In addition to the laboratory infrastructure, a structured validation methodology is formulated in Section 5.2. It comprises quantitative performance metrics and a standardized set of benchmark scenarios. The scenario set systematically addresses islanded DC operation, hybrid AC/DC coupling, SoC-adaptive frequency support, and demand-side voltage support. The resulting evaluation framework enables reproducible validation procedures and comparable assessment of decentralized control approaches.

The testbed is designed to reflect realistic conditions of low-voltage hybrid AC/DC microgrids and supports real-time control via rapid-prototyping hardware. The experiments cover a range of operational scenarios, including DC islanded operation, cross-domain SoC balancing, frequency support through a VSM, and GSL-based dynamic load support, as outlined in Chapter 5.

The laboratory validation confirms that all proposed control methods operate reliably under practical constraints, such as asymmetric component ratings, limited bus capacitance, and realistic line resistances. Moreover, the results demonstrate the robustness of the approaches to dynamic disturbances and validate the theoretical predictions presented in Chapter 3 and Chapter 4.

Despite the demonstrated robustness and applicability of the proposed control methods, several underlying assumptions define the intended scope of operation. First, the experimental validation assumes practical line resistances equivalent to distribution-level cabling up to several kilometers. While the approach remains effective within this range, very long transmission distances can introduce dominant voltage drops that require additional compensation strategies. Second, the AC-side coupling assumes a predominantly inductive impedance, which

holds for many low-voltage and medium-voltage grids but can require adaptation in highly resistive or mixed impedance grids. Finally, all stability proofs rely on Continuous Conduction Mode (CCM) and ideal converter tracking, as commonly assumed in analytical control design. These assumptions provide a tractable and practically relevant modeling basis, yet future work may consider non-ideal regimes and meshed architectures to broaden the applicability.

Overall, the results confirm that the proposed SoG framework presented in this dissertation provides a scalable, communication-free control method for hybrid AC/DC microgrids. By coordinating energy balancing, frequency support, and voltage stability solely via local measurements, the developed methods contribute a significant step toward resilient, autonomous power systems. Their experimental validation under realistic conditions underscores their potential for real-world deployment in decentralized hybrid AC/DC microgrids.

6.3 Outlook

This dissertation establishes a comprehensive basis for decentralized self-organization control of hybrid AC/DC microgrids, including SoG-based VSM control on the AC side and a decentralized GSL mechanism on the load side. Building on this foundation, the most impactful future research directions are outlined in this section.

AC-Side Specific Research Directions

- **Impedance modeling and adaptation:** The current control design assumes a predominantly inductive AC grid impedance (see Assumption 3.2). Future work could extend this assumption to more general cases, including resistive or mixed impedance characteristics. This would allow improved robustness of the control strategy under varying grid conditions and enable broader applicability in diverse microgrid topologies.

- **Formal AC-side stability analysis:** While DC-side stability has been rigorously proven in this work, a formal stability proof of the AC-side dynamics remains an open topic. Such a proof would need to consider interactions between grid impedance, converter dynamics, and the hybrid AC/DC coupling, especially in the presence of grid-forming interfacing converters and dynamic frequency regulation.
- **Reactive power control:** In the current implementation, the reactive power reference is set to $Q^* = 0$, as the focus lies on active-power-based frequency stabilization. Incorporating reactive power control into the SoG-based framework offers a promising avenue for extending the method's applicability, especially in grids where voltage stability and reactive power exchange are critical.

GSL-Specific Research Directions

- **Adaptive parameter tuning:** The proposed GSL mechanism relies on fixed gains such as k_{GSL}, scaling coefficients ζ_i, and restoration thresholds. Future work may explore data-driven adaptation strategies, including reinforcement learning or online optimization, to tune these parameters in real-time. Such approaches could maximize grid support capabilities while preserving device longevity and adhering to operational constraints.
- **Hybrid AC/DC integration:** While the current implementation focuses on DC-connected ZIP loads, extending the GSL approach to hybrid AC/DC systems is a natural progression. This would require coordinated control strategies to provide simultaneous voltage support in the DC domain and frequency support in the AC domain, potentially enabling fully decentralized and GSL behavior across both domains.
- **Partial-restoration strategies:** In this dissertation, the GSL mechanism is either active or fully disabled during the restoration phase. Future research could analyze the stability and performance of intermediate restoration strategies, where the restoration factor $\theta \in (0, 1)$ allows partial

continuation of GSL action. This could improve damping and resilience without overburdening the load devices.

System-Level and Hierarchical Extensions

- **Integration of tertiary control:** The SoG-based framework currently operates at the primary control level, enabling fast and decentralized coordination. Future extensions could introduce a tertiary control layer responsible for optimizing power flow between interconnected microgrids or between microgrids and the main grid. Such an architecture could support economic dispatch, congestion management, and energy trading.
- **Adaptive SoG-based control:** Experimental results show that PI-based enhancements improve steady-state accuracy, while P-based control offers faster initial responses. This trade-off suggests that adaptive control schemes capable of switching or blending P and PI action based on operating conditions, could further improve dynamic performance.

In summary, this dissertation establishes a communication-free control framework that enables self-organizing operation of hybrid AC/DC microgrids and validates its performance experimentally. The open extensions outlined above lie beyond the present scope and constitute promising directions to further advance grid-supportive microgrid control.

List of Publications

Journal articles

[J1] **Ö. Ekin**, M. Leuthäußer, G. De Carne, and V. Hagenmeyer, "State-of-Grid Based SoC Balancing and AC Coupling Control for DC Microgrids," *IEEE Transactions on Industrial Electronics*, December 2025. doi: 10.1109/TIE.2025.3639739.

[J2] **Ö. Ekin**, F. Perez, G. Damm, and V. Hagenmeyer, "State-of-Grid Based Virtual Synchronous Machine for Hybrid AC-DC Microgrids," *TechRxiv*, October 2025. doi: 10.36227/techrxiv.176070803.35965180/v1.

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[J4] A. Korompili, **Ö. Ekin**, M. Stevic, V. Hagenmeyer, and A. Monti, "Linear Active Disturbance Rejection Control-Based Voltage Controller for Buck and Boost DC/DC Converters in DC Distribution Grids," *IEEE Access*, vol. 13, pp. 19 085–19 109, 2025. doi: 10.1109/ACCESS.2025.3533080.

[J5] J. Galenzowski, S. Waczowicz, H. K. Çakmak, E. Tajalli-Ardekani, S. Beichter, **Ö. Ekin**, R. Mikut, and V. Hagenmeyer, "Understanding novel district concepts: A structured exploration of interdisciplinary clustering in urban energy systems," *Energy Reports*, vol. 14, pp. 3673–3689, 2025. doi: 10.1016/j.egyr.2025.10.021.

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Conference contributions

[C1] **Ö. Ekin**, G. Arena, S. Waczowicz, V. Hagenmeyer, and G. De Carne, "Comparison of Four-Switch Buck-Boost and Dual Active Bridge Converter for DC Microgrid Applications," in *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Kiel, Germany, 2022, pp. 1–6. doi: 10.1109/PEDG54999.2022.9923074.

[C2] **Ö. Ekin**, F. Perez, G. Damm, and V. Hagenmeyer, "A Real-Time PHIL Implementation of a Novel Nonlinear Distributed Control Strategy for a Multi-Terminal DC Microgrid," in *2023 IEEE Belgrade PowerTech*, Belgrade, Serbia, 2023, pp. 1–6. doi: 10.1109/PowerTech55446.2023.10202843.

[C3] **Ö. Ekin**, A. Balakrishnan, L. Spatafora, and V. Hagenmeyer, "Distributed Control Strategy for Grid Supportive Loads in DC Microgrids," in *2024 9th IEEE Workshop on the Electronic Grid (eGRID)*, Santa Fe, NM, USA, 2024, pp. 1–6. doi: 10.1109/eGRID62045.2024.10842713.

[C4] **Ö. Ekin**, F. Perez, F. Wiegel, V. Hagenmeyer, and G. Damm, "Grid Supporting Nonlinear Control for AC-Coupled DC Microgrids," in *2024 IEEE*

Sixth International Conference on DC Microgrids (ICDCM), Columbia, SC, USA, 2024, pp. 1–6. doi: 10.1109/ICDCM60322.2024.10664838.

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[C6] **Ö. Ekin**, F. Wiegel, L. Spatafora, R. Jumar, M. Ghadrdan, S. Waczowicz, G. De Carne, and V. Hagenmeyer, "The Smart2DC Microgrid Laboratory at Karlsruhe Institute of Technology," in *2025 IEEE Seventh International Conference on DC Microgrids (ICDCM)*, 2025, pp. 1–6. doi: 10.1109/ICDCM63994.2025.11144732.

[C7] M. Courcelle, **Ö. Ekin**, G. De Carne, and V. Hagenmeyer, "Load Sensitivity-Based Adaptive Control Strategy for Grid-Supportive Loads in DC Microgrids," in *2025 10th IEEE Workshop on the Electronic Grid (eGRID)*, 2025, pp. 1–6. doi: 10.1109/eGRID63452.2025.11255307.

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Book chapter contributions

[B1] F. Wiegel, S. An, J. Wachter, S. Beichter, A.-C. Süß, **Ö. Ekin**, and V. Hagenmeyer, *Integrating distributed energy resources in real-world sector-coupled microgrids: challenges, strategies, and experimental insights*. IET, 2024, ch. 6, pp. 147–173. doi: 10.1049/PBPO149E_ch6.

Data publications

[D1] **Ö. Ekin**, “Experimental Data and Scripts for ’State-of-Grid Based SoC Balancing and AC Coupling Control for DC Microgrids’.” Zenodo, Sep. 2025. doi: 10.5281/zenodo.17061990.

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A Appendix

A.1 Proportional Integral (PI) Voltage Control

The high-level control strategies developed in this dissertation, most notably the mapping-based method of Section 3.2, provide a voltage reference that must be accurately tracked by a low-level DC–DC converter controller (cf. Fig. 3.7). In accordance with Assumption 3.1, the upper-level logic evolves on a slow timescale and therefore relies on a much faster inner loop to maintain the prescribed voltage. For completeness and reproducibility, this appendix documents the implementation of the low-level controller that was employed in the experimental validation presented in Chapter 5.

A.1.1 Buck Voltage Control

Figure A.1 depicts the cascaded PI architecture adopted for the synchronous buck converter. An outer voltage loop generates a reference current $i^*(t)$ for an inner current loop, which directly manipulates the inductor current by adjusting the Pulse-Width Modulation (PWM) duty ratio $d_{\mathrm{B1}}(t)$. Both loops are realized as PI controllers with conditional-integration (anti-windup) logic, ensuring robust performance under actuator saturation.

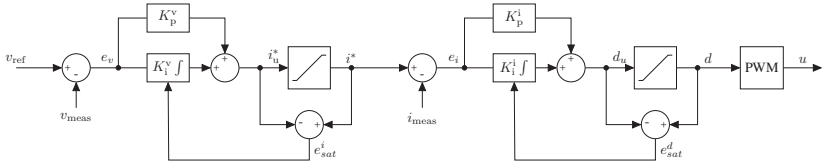

Figure A.1: Block diagram of the cascaded PI control for a buck converter with anti-windup. The outer voltage loop (K_p^v, K_i^v) compares v_{ref} and v_{meas} and generates the current reference $i^\star$ through a limiter with back-calculation (e_{sat}^i and e_{sat}^d). The inner current loop (K_p^i, K_i^i) compares $i^\star$ and i_{meas} and produces the duty command d via a second limiter with anti-windup. The PWM maps d to the gate signal u.

Control Laws

Let

$$e_v(t) = V^*(t) - V_{\mathrm{meas}}(t), \qquad e_i(t) = i^*(t) - i_{\mathrm{meas}}(t), \tag{A.1}$$

be the voltage and current tracking errors, respectively. The unsaturated PI outputs are defined as

$$i_{\mathrm{u}}^*(t) = -K_{\mathrm{P}}^{\mathrm{v}}\, e_v(t) - K_{\mathrm{I}}^{\mathrm{v}} \int_0^t e_v(\tau)\,\mathrm{d}\tau, \tag{A.2}$$

$$d_{\mathrm{u}}(t) = -K_{\mathrm{P}}^{\mathrm{i}}\, e_i(t) - K_{\mathrm{I}}^{\mathrm{i}} \int_0^t e_i(\tau)\,\mathrm{d}\tau, \tag{A.3}$$

where $K_{\mathrm{P}}^{\mathrm{v}}$ and $K_{\mathrm{I}}^{\mathrm{v}}$ are the proportional and integral gains of the outer voltage controller, and $K_{\mathrm{P}}^{\mathrm{i}}$ and $K_{\mathrm{I}}^{\mathrm{i}}$ are the proportional and integral gains of the inner current controller, respectively. All gains are treated as positive constants chosen to meet the desired bandwidth and robustness specifications.

Physical limitations are enforced via saturation operators,

$$i^*(t) = \mathrm{sat}_{[i_{\min},\, i_{\max}]}\big(i_{\mathrm{u}}^*(t)\big), \tag{A.4}$$

$$d(t) = \mathrm{sat}_{[0,\,1]}\big(d_{\mathrm{u}}(t)\big), \tag{A.5}$$

with $i_{\min}, i_{\max}$ derived from component ratings and limits. To prevent integrator wind-up during saturation, the integral states ι_{v} and $\iota_{\mathrm{i}}(t)$ with

$$\iota_{\mathrm{v}}(t) := \int_0^t e_v(\tau)\,\mathrm{d}\tau, \qquad \iota_{\mathrm{i}}(t) := \int_0^t e_i(\tau)\,\mathrm{d}\tau. \tag{A.6}$$

obey the following conditional-integration dynamics, in analogy to the anti-windup formulation presented in Equation (3.38):

$$\frac{d}{dt}\iota_{\mathrm{v}}(t) = \mathscr{S}(\iota_{\mathrm{v}}, e_v), \qquad \frac{d}{dt}\iota_{\mathrm{i}}(t) = \mathscr{S}(\iota_{\mathrm{i}}, e_i). \tag{A.7}$$

This strategy freezes the corresponding integrator whenever the associated actuator is saturated, thereby preserving stability margins and ensuring rapid restoration once the control signal re-enters the admissible range.

A.1.2 Boost-Converter Voltage Control

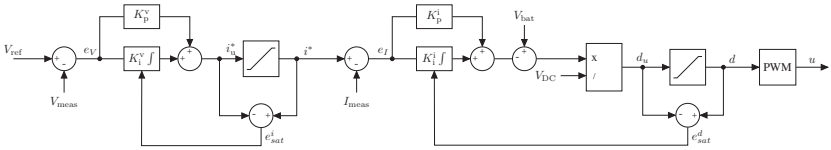

Figure A.2: Block diagram of the cascaded PI control for a boost converter with optional feedforward and antiwindup. The outer voltage loop (K_p^v, K_i^v) forms $e_v = v_{\mathrm{ref}} - v_{\mathrm{meas}}$ and generates the current reference $i^\star$ through a limiter with back-calculation (e_{sat}^i and e_{sat}^d). The inner current loop (K_p^i, K_i^i) regulates $e_i = i^\star - i_{\mathrm{meas}}$ and, together with a duty feedforward d_u based on the measured V_{bat} and V_{DC}, produces the duty command. A duty limiter with antiwindup yields d, and the PWM maps d to the switching signal u.

A brief comparison of the circuit topologies in Figure 2.4 highlights why this structural difference is essential. The buck converter shown in Figure 2.4(a), typically used for supplying local loads as discussed in Section 2.2.3, exhibits a non-conducting output path when the duty cycle d is initially set to zero. In

this case, the lower switch is off and no current flows to the load, which means the converter starts up from zero voltage in a controlled manner as d increases.

In contrast, the boost converter shown in Figure 2.4(b), which is used for interfacing BESSs and PV sources (see Section 2.2.4), exhibits a fundamentally different behavior. When $d = 0$, the lower switch is fully on, directly connecting the battery to the inductor. If the output capacitor is initially discharged, this can lead to very high inrush currents, potentially exceeding device ratings.

To prevent such undesirable transients, the duty cycle is initialized using a feedforward estimate based on the steady-state relation $d = V_{\mathrm{in}}/V_{\mathrm{out}}$. This approach improves the startup behavior by anticipating the required duty ratio and avoiding abrupt current surges. It effectively acts as an open-loop compensation stage and complements the closed-loop PI control structure described above.

Figure A.2 shows the cascaded PI voltage controller used for boost converters. The overall structure closely resembles the buck converter scheme described in Section A.1.1, comprising an outer voltage loop and an inner current loop with conditional-integration anti-windup mechanisms.

The key difference lies in the duty cycle computation. Instead of directly mapping the PI output to the duty ratio, the output of the current controller is first augmented by the measured battery voltage $V_{\mathrm{B}}(t)$, and the resulting sum is then normalized by the measured DC-bus voltage $V_{\mathrm{DC}}(t)$:

$$d_{\mathrm{u}}(t) = \frac{V_{\mathrm{B}}(t) + u_{\mathrm{PI}}(t)}{V_{\mathrm{DC}}(t)}. \tag{A.8}$$

This additional computation stage serves as an optional feedforward path that improves dynamic performance during sudden load transients by compensating for variations in the input voltage.

As before, the resulting duty cycle is subjected to saturation:

$$d(t) = \mathrm{sat}_{[0,1]}\left(d_{\mathrm{u}}(t)\right), \tag{A.9}$$

with the corresponding integrator dynamics frozen if saturation occurs.

This extended formulation completes the documentation of the cascaded PI voltage control implementations used in the experimental setups of this dissertation.

Implementation Remarks

- **Tuning methodology** – The proportional gains $K_{\mathrm{P}}^{\mathrm{v}}$ and $K_{\mathrm{P}}^{\mathrm{I}}$ were selected via frequency-domain loop-shaping, targeting a crossover-frequency ratio of roughly 10:1 between current and voltage loops. The integral gains were then chosen to eliminate steady-state error while maintaining a phase margin in excess of 50°.
- **Sampling and computation** – All control laws are executed within a 100 kHz interrupt service routine; hence the inner loop benefits from a single-cycle latency.
- **Reference limiting** – Prior to saturation, $i_{\mathrm{u}}^{*}(t)$ is clipped by design limits derived from inductor current ratings and thermal considerations, ensuring safe operation under all tested conditions.

The foregoing formulation provides a self-contained and reproducible description of the cascaded PI voltage-control scheme used throughout this work.

A.2 MPPT Perturb and Observe

In the context of this dissertation, a modified Perturb and Observe (P&O) algorithm was employed to perform Maximum Power Point Tracking (MPPT) of a PV system. The algorithm is based on an advanced method presented in the literature [35], yet it is not the focus of the research conducted here but rather serves as a tool to optimally adjust the operating point of the PV system.

Compared to the conventional P&O method, the algorithm used here implements a deliberately constrained search space strategy. Instead of traversing the entire P-V curve, the search is limited to the vicinity of the Maximum Power Point (MPP), which reduces both the response time under irradiance changes and the steady-state oscillations around the MPP.

The algorithm operates with two voltage thresholds, defined as $65\,\%$ and $95\,\%$ of the open-circuit voltage V_{oc}. If the operating point lies outside this predefined range, the duty cycle D is adjusted by a defined step size ΔD to quickly bring the operating point back into the optimal range.

The MPPT algorithm applied in this work is illustrated in the flowchart shown below. These modifications lead to improved efficiency and stable operation of the PV system, even under changing weather conditions.

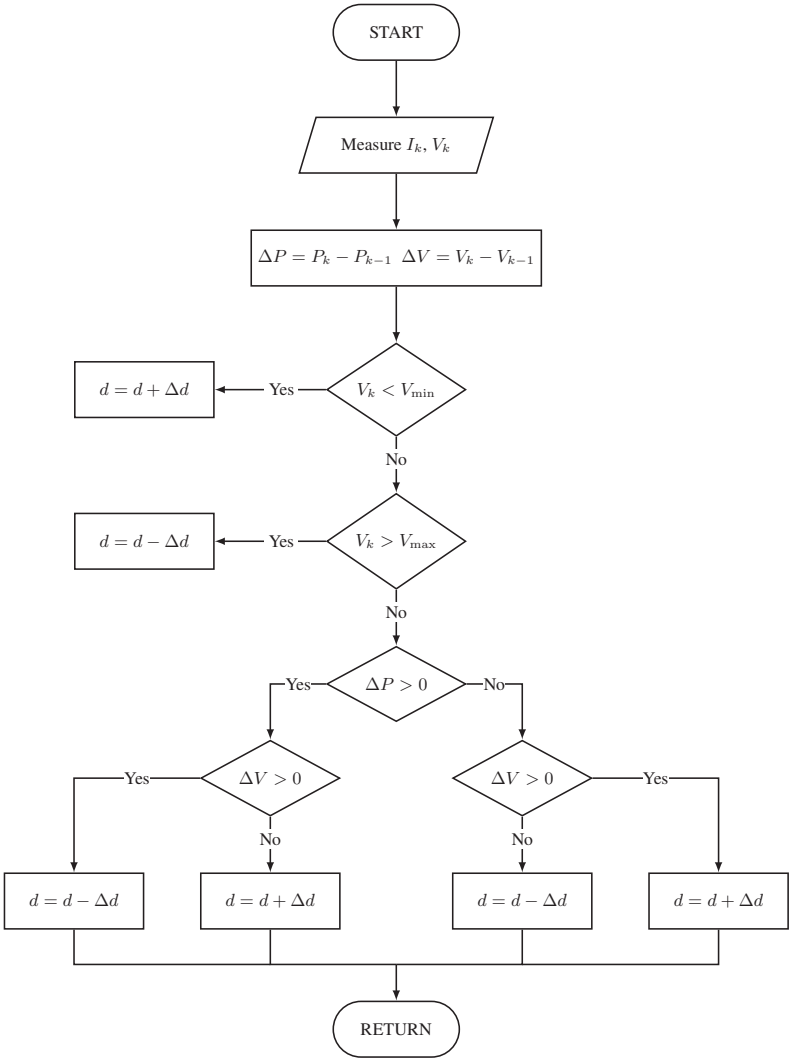

Figure A.3: Flowchart of the modified P&O MPPT used in this work. The method measures (I_k, V_k), computes $\Delta P = P_k - P_{k-1}$ and $\Delta V = V_k - V_{k-1}$, constrains the operating point to a predefined voltage window $[V_{\min}, V_{\max}]$, and updates the duty cycle d in steps of $\pm\Delta d$ according to the signs of ΔP and ΔV to maintain operation near the MPP.

A.3 Space Vector Representations and Transformation into Rotating Reference Frames

The analysis of three-phase electrical systems can be significantly simplified by transforming the quantities such as currents and voltages from phase variables (a, b, c) into a two-axis system. In particular, the so-called Clarke transformation $(abc \rightarrow \alpha\beta)$ and the subsequent Park transformation $(\alpha\beta \rightarrow dq)$ play a central role in this process. The Park transformation, often also referred to as the vector or dq transformation, allows quantities that are time-varying in the stationary reference frame to be represented as (nearly) time-invariant quantities in the rotating reference frame. This greatly facilitates the control and state analysis of power electronic systems and electrical machines [60, 157].

A.3.1 Clarke Transformation ($abc \rightarrow \alpha\beta$)

The first stage, the Clarke transformation, converts the three-phase quantities x_a, x_b, x_c into two orthogonal components x_α and x_β. A common formulation is [60]:

$$\begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} = \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix}. \tag{A.10}$$

This transformation is also referred to as the $\alpha\beta$ space vector representation. Geometrically, it corresponds to a projection of the three-phase system onto two orthogonal axes (α and β). Ideally, this yields a rotating vector that contains the same information as the original three-phase system.

Normalization and Variants

Various normalization factors for the Clarke matrix are found in the literature. A commonly used formulation that ensures power invariance is:

$$\begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix}. \tag{A.11}$$

A.3.2 Park Transformation ($\alpha\beta \rightarrow dq$)

The second stage is the Park transformation itself, which transfers the system into a rotating reference frame. The transformation is defined as [60]:

$$\begin{pmatrix} x_d \\ x_q \end{pmatrix} = \begin{pmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{pmatrix} \begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix}. \tag{A.12}$$

Here, θ is the angle of the reference frame, typically determined by a Phase-Locked Loop (PLL). In the synchronously rotating reference frame, θ corresponds to the time integral of the grid frequency $\omega = 2\pi f$.

dq Transformation

The dq transformation converts the two-axis system ($\alpha\beta$) into a synchronously rotating coordinate system (dq). The relationship between the components x_d, x_q and the original phase quantities x_a, x_b, x_c can be expressed directly as an $abc \rightarrow dq$ transformation:

$$\begin{pmatrix} x_d \\ x_q \end{pmatrix} = \frac{2}{3} \begin{pmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{pmatrix} \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix}. \quad \text{(A.13)}$$

Here, θ denotes the instantaneous phase angle of the coordinate system. This transformation accounts for the rotational components of the individual phase axes and enables the representation of the system as DC quantities in the synchronous rotating reference frame.

In the synchronous case, the d component x_d appears as a DC quantity, while the q component x_q can represent either the reactive power or the torque component, depending on the application.

Inverse Transformation

To transform back to the phase quantities (abc), the inverse Park transformation is applied first:

$$\begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix} = \begin{pmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{pmatrix} \begin{pmatrix} x_d \\ x_q \end{pmatrix}, \quad \text{(A.14)}$$

followed by the inverse Clarke transformation:

$$\begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} x_\alpha \\ x_\beta \end{pmatrix}. \quad \text{(A.15)}$$

Alternatively, the inverse $dq \rightarrow abc$ transformation can be expressed directly as

$$\begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} = \begin{pmatrix} \cos\theta & -\sin\theta \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{pmatrix} \begin{pmatrix} x_d \\ x_q \end{pmatrix}. \tag{A.16}$$

This transformation converts the components x_d and x_q in the rotating coordinate system back into the phase quantities x_a, x_b, and x_c. It is commonly used to calculate the three-phase setpoints for the control of converters from the controller output.

A.4 Derivation of the Model Equations

This section explains the derivation of equations (A.23)–(A.24). The model equations are based on the application of Kirchhoff's laws to the AC side.

Derivation on the AC Side ($\dot{I}_{ld}$ and $\dot{I}_{lq}$)

The starting point is the voltage equation for one of the three phases $x \in \{a, b, c\}$:

$$L_l \frac{d}{dt} i_{l,x} + R_l i_{l,x} = v_{\mathrm{conv},x} - v_{l,x}, \tag{A.17}$$

where:

- L_l is the inductance and R_l is the series resistance between the converter and the grid,
- $v_{\mathrm{conv},x}$ denotes the converter output voltage,
- $v_{l,x}$ represents the grid voltage.

By transforming this equation into the d–q reference frame, the differential equations for the d- and q-components of the current are obtained. Cross-coupling terms appear due to the transformation into the synchronously rotating frame:

$$L_l \frac{d}{dt} I_{ld} - \omega_g L_l I_{lq} + R_l I_{ld} = V_{\mathrm{conv},d} - V_{l,d}, \tag{A.18}$$

$$L_l \frac{d}{dt} I_{lq} + \omega_g L_l I_{ld} + R_l I_{lq} = V_{\mathrm{conv},q} - V_{l,q}. \tag{A.19}$$

The converter voltages in $d-q$ coordinates can be expressed in terms of the modulation signals u_d and u_q:

$$\begin{pmatrix} V_{\mathrm{conv},d} \\ V_{\mathrm{conv},q} \end{pmatrix} = \frac{V_{\mathrm{DC}}}{2} \begin{pmatrix} u_d \\ u_q \end{pmatrix}. \tag{A.20}$$

Substituting these expressions and rearranging yields equations (A.23)–(A.24):

$$\dot{I}_{ld} = -\frac{R_l}{L_l} I_{ld} + \omega_g I_{lq} + \frac{1}{2L_l} V_{\mathrm{DC}} u_d - \frac{V_{l,d}}{L_l}, \tag{A.21}$$

$$\dot{I}_{lq} = -\frac{R_l}{L_l} I_{lq} - \omega_g I_{ld} + \frac{1}{2L_l} V_{\mathrm{DC}} u_q - \frac{V_{l,q}}{L_l}. \tag{A.22}$$

A.5 Cascaded Voltage and Current Control of the Interlink Converter

Grid-connected converter systems are inherently time-varying, as the grid voltages oscillate sinusoidally at the fundamental frequency. This time variance complicates both modeling and controller design. To obtain a simple and decoupled control structure nevertheless, voltage and current quantities are transformed into a reference frame that rotates synchronously with the grid frequency

(often referred to as the dq reference frame, $dq0$, vector reference frame, or synchronous reference frame) [60, p. 67 ff.]. A detailed mathematical description of this transformation is provided in Appendix A.3.

The so-called Clarke and Park transformations (see Appendix A.3) ensure that sinusoidal quantities in the three-phase system (abc) appear as (nearly) stationary quantities in the dq frame. This allows the active (d-axis) and reactive power components (q-axis) to be controlled independently [60]. The derivation of the dynamic equations is based on a grid model with resistance R and inductance L, where the phase voltages v_a, v_b, v_c and currents i_a, i_b, i_c are transformed into v_d, v_q, i_d, and i_q.

In the dq reference frame, the following differential equations result (see derivation in Appendix A.4):

$$\dot{I}_{ld} = -\frac{R_l}{L_l} I_{ld} + \omega_g I_{lq} + \frac{1}{2L_l} V_{\mathrm{DC}} u_d - \frac{V_{l,d}}{L_l}, \tag{A.23}$$

$$\dot{I}_{lq} = -\frac{R_l}{L_l} I_{lq} - \omega_g I_{ld} + \frac{1}{2L_l} V_{\mathrm{DC}} u_q - \frac{V_{l,q}}{L_l}. \tag{A.24}$$

Alternatively, the well-known form of the dq-voltage equations is given by:

$$v_d = R\, i_d + L\, \frac{di_d}{dt} - \omega L\, i_q + e_d, \tag{A.25}$$

$$v_q = R\, i_q + L\, \frac{di_q}{dt} + \omega L\, i_d + e_q, \tag{A.26}$$

where:

- v_d, v_q: voltages in dq coordinates,
- i_d, i_q: currents in dq coordinates,
- e_d, e_q: induced voltages or grid voltages,
- ω: angular frequency of synchronous rotation.

The cross-coupling terms $\pm\omega L i_q$ and $\pm\omega L i_d$ in (A.25)–(A.26) dynamically couple the axes. To reduce the control effort, these terms are compensated by feedforward control:

$$v_d^* = R\, i_d + L\, \frac{di_d}{dt} - \omega L\, i_q, \tag{A.27}$$

$$v_q^* = R\, i_q + L\, \frac{di_q}{dt} + \omega L\, i_d. \tag{A.28}$$

The complete control laws of the inner current control loop are:

$$v_d^* = Ri_d + L\frac{di_d}{dt} - \omega L i_q + K_{p,i_d}(i_d^* - i_d) + K_{i,i_d}\int (i_d^* - i_d)dt, \tag{A.29}$$

$$v_q^* = Ri_q + L\frac{di_q}{dt} + \omega L i_d + K_{p,i_q}(i_q^* - i_q) + K_{i,i_q}\int (i_q^* - i_q)dt. \tag{A.30}$$

The outer voltage control loop compares the setpoint voltages v_d^* and v_q^* with the measured voltages v_d and v_q, respectively, and generates the current setpoints i_d^* and i_q^*:

$$i_d^* = K_{p,v_d}(v_d^* - v_d) + K_{i,v_d}\int (v_d^* - v_d)dt, \tag{A.31}$$

$$i_q^* = K_{p,v_q}(v_q^* - v_q) + K_{i,v_q}\int (v_q^* - v_q)dt. \tag{A.32}$$

Actuator constraints and anti-windup mechanisms are implemented to prevent integrator wind-up and maintain stability under saturation conditions [158].

A key property of the dq-based control is the ability to control active power (P) and reactive power (Q) independently. For a balanced three-phase system in synchronous rotation [60]:

$$P = \tfrac{3}{2}\,(v_d i_d + v_q i_q), \qquad Q = \tfrac{3}{2}\,(v_q i_d - v_d i_q). \tag{A.33}$$

In many grid control strategies, the d-axis is aligned such that $v_q \approx 0$. Under this condition:

- Active power (P) can be controlled by adjusting the phase angle between the grid and converter voltages, which corresponds physically to the so-called power angle, approximately proportional to the sine of the phase angle. The d-axis refers to the active power component.
- Reactive power (Q) is primarily influenced by the voltage magnitude. A difference in amplitude between the converter output and the grid voltage results in a reactive current component in the q-axis.

For this decoupling to be effective, the converter must satisfy the following conditions:

1. remain synchronized with the grid phasor (e.g., via a PLL),
2. assume or enforce a balanced three-phase system,
3. implement decoupling and feedforward strategies to mitigate cross-coupling effects.

Once these conditions are met, active power can be controlled through phase angle adjustment (via i_d) and reactive power through voltage amplitude adjustment (via i_q). This is a major advantage of dq-based control over scalar voltage and frequency control.

At high loads or during voltage sags, the setpoints cannot always be realized. Therefore, actuator constraints are imposed:

- Maximum current: $|i_d + j\, i_q| \leq i_{\max}$ to prevent semiconductor overloading,
- Maximum voltage setpoint: $|v_d^* + j\, v_q^*| \leq V_{\max}$, limited by the DC-link voltage and modulation scheme.

If these limits are reached, the integrators of the PI controllers are limited through anti-windup mechanisms (e.g., back-calculation or conditional integration) [158], which prevent integrator wind-up when the controller outputs saturate.

Control Structure Overview

1. **Outer control loop (power control):** generates the setpoints i_d^*, i_q^* based on the desired active and reactive power (e.g., DC-link voltage control for P; voltage support for Q).
2. **Inner control loop (current control):** decouples the d- and q-axes and controls i_d, i_q to their setpoints via PI controllers.
3. **Modulation:** converts the resulting v_d^*, v_q^* into abc coordinates and drives the IC.

The transformation into the dq reference frame enables largely decoupled control of active power (via the phase angle) and reactive power (via the voltage magnitude) in grid-connected applications. Crucially, the converter must be synchronized to the grid phasor via PLL and assume an approximately balanced three-phase system. On this basis, the inner current control loop achieves high dynamic performance and robust tracking of the setpoints. The outer control loops shape the desired active power (e.g., via DC-link voltage control) and reactive power (e.g., via voltage support), closely interacting with the grid measurements and setpoints.

For advanced aspects of tuning PI current controllers in grid-forming converters, including stability under weak-grid conditions, LCL filter design, and adaptive parameter adjustment, the reader is referred to the comprehensive treatment in [159].

A.6 Time-Scale Separation

In many engineering systems, different dynamic processes evolve on distinctly different time scales. This property can be systematically exploited in modeling and control design to simplify the overall system description and enable more efficient analysis.

A well-established mathematical framework for the analysis of such systems is the Singular Perturbation Theory [160, 72]. The key idea is to explicitly separate the dynamics into fast and slow components by introducing a small perturbation parameter ε. This structure allows for a hierarchical analysis and controller synthesis, where the fast and slow dynamics are treated sequentially.

The singularly perturbed model of a dynamical system can be written as [72, p. 371f]:

$$\dot{x} = f(t, x, z, \varepsilon), \tag{A.34}$$

$$\varepsilon \dot{z} = g(t, x, z, \varepsilon), \tag{A.35}$$

where f and g are continuously differentiable functions in their arguments $(t, x, z, \varepsilon) \in [0, t_1] \times D_x \times D_z \times [0, \varepsilon_0]$, with $D_x \subset \mathbb{R}^n$ and $D_z \subset \mathbb{R}^m$ being open, connected domains.

In the limiting case $\varepsilon \to 0$, the second Equation (A.35) reduces to an algebraic constraint:

$$0 = g(t, x, z, 0). \tag{A.36}$$

The model is said to be in standard form if (A.36) admits $k \geq 1$ isolated real solutions:

$$z = h_i(t, x), \quad i = 1, 2, \ldots, k. \tag{A.37}$$

This condition ensures that each equilibrium of (A.36) corresponds to a well-defined reduced system with n states. For each solution manifold (A.37), substituting into (A.34) and setting $\varepsilon = 0$ yields the so-called reduced system:

$$\dot{x} = f(t, x, h(t, x), 0). \tag{A.38}$$

This reduced or quasi-steady-state model describes the slow dynamics of the system, under the assumption that the fast states z instantaneously adjust to their equilibrium values. This assumption is justified because, for small ε, it holds that $\dot{z} = g/\varepsilon$, implying very fast dynamics of the z-subsystem whenever $g \neq 0$.

A.7 Hardware Components

This appendix provides additional information on the hardware components of the Smart2DC microgrid laboratory used in the context of this dissertation.

Table A.1: Power Electronics Components

Component	Manufacturer	Type/Model	Remarks
Power Half-Bridge	Imperix	PEB8038	SiC-MOSFET, 800 V, 38 A, 200 kHz
Rapid Control Prototyping Platform	Imperix	B-Box RCP	Dual-Core ARM + Kintex FPGA, 250 kHz control
PWM Signal Chain	Imperix	Optical Transmission	Galvanically isolated, noise-immune

Table A.2: Sensing Components

Component	Manufacturer	Type/Model	Remarks
Current Sensor (± 50 A)	Imperix	DIN-Rail ML50A	99 mV A^{-1}, 200 kHz bandwidth, galvanically isolated
Voltage Sensor (± 800 V)	Imperix	DIN-Rail ML800V	2.46 mV V^{-1}, >60 kHz bandwidth, galvanically isolated

Table A.3: Energy Sources and Loads

Component	Manufacturer	Type/Model	Remarks
PV/Battery Emulator	EA / Delta	PSI 1000 / SM15K-CP	Bidirectional, 15 kW, autoranging up to 1500 V
Programmable DC Loads	EA / in-house design	–	Adjustable load profiles, dynamic tests

Table A.4: Passive Components

Component	Manufacturer	Type/Model	Remarks
Inductor 2.36 mH / 20 A	Hahn	V23105	Line filter, passive rack
EMI Filter	Schaffner	FN3025HP-20-71	Grid-side interference suppression
Capacitors 500 µF	KEMET / Arcotronics	C274AC35100SA 0J	Line filter / damping
Resistors 1 Ω-100 Ω / 10 kW	Fritzlen	HS25 1R0J	adjustable slide resistors

A.8 Singular Perturbation Method

For completeness, Theorem 11.4 on the stability of singularly perturbed systems from [72] is stated below. This theorem provides the theoretical foundation for the stability analysis of the controlled DC microgrid system presented in Section 3.5.

Theorem A.8.1 (Stability of Singularly Perturbed Systems). *Consider the singularly perturbed system*

$$\dot{x} = f(t, x, z, \varepsilon), \tag{A.39}$$

$$\varepsilon \dot{z} = g(t, x, z, \varepsilon), \tag{A.40}$$

where $x \in \mathbb{R}^n$, $z \in \mathbb{R}^m$, $\varepsilon > 0$, and f and g are sufficiently smooth[1] functions. Assume the following conditions hold:

($\mathcal{C}1$) $f(t, 0, 0, \varepsilon) = 0,\ g(t, 0, 0, \varepsilon) = 0$ for all $t \geq 0,\ \varepsilon \in [0, \varepsilon_0]$.

($\mathcal{C}2$) The equation $g(t, x, z, 0) = 0$ has an isolated solution $z = h(t, x)$ with $h(t, 0) = 0$.

($\mathcal{C}3$) The functions $f, g, h,$ and their derivatives up to second order are bounded for $z - h(t, x) \in B_\rho$.

($\mathcal{C}4$) The reduced system

$$\dot{x} = f\big(t, x, h(t, x), 0\big) \tag{A.41}$$

is exponentially stable.

[1] "Sufficiently smooth" refers to functions possessing as many continuous derivatives as required by the analysis. For example, if the application of the theorem demands continuous second derivatives, then the functions are considered sufficiently smooth if they are at least C^2. The precise smoothness requirement is context-dependent and typically indicated as C^k, where $k \in \mathbb{N} \cup \{\infty\}$ denotes the number of continuous derivatives.

(C5) The boundary-layer system

$$\frac{dy}{d\tau} = g\big(t, x, y + h(t,x), 0\big) \tag{A.42}$$

is exponentially stable, uniformly in (t, x).

Then there exists $\varepsilon^* > 0$ *such that for all* $0 < \varepsilon < \varepsilon^*$*, the equilibrium of the full system* (A.39)–(A.40) *is locally exponentially stable.*