

Performance results of the first version of the MIZAR ASIC for the PBR mission

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The Multi-channel Intergrated Zone-sampling Analogue-memory based Readout (MIZAR) ASIC is a new type of front-end electronics which has been developed for the detection of the optical Cherenkov signals by Extensive Air Showers directly observed from sub-orbital and orbital altitudes. It sets the stage for a new generation of low-power consuming 64-channel Application-Specific Integrated Circuit (ASIC). The ASIC is implemented in a commercial 65 nm CMOS technology to readout an 8×8 matrix of Silicon Photo-Multipliers (SiPMs). The event is recorded at channel level in an array of 256 cells, each one equipped with an analogue memory, a 12-bits Wilkinson Analog-to-Digital Converter (ADC) and latches running at a sampling rate of 200 MS/s. The converted data are sent off-chip to a Field Programmable Gate Array (FPGA) which controls the digital end-of-column logic of the ASIC and implements the trigger logic. The goal is to employ it for the first time on the POEMMA Balloon with Radio (PBR) NASA mission which is devoted to measure Ultra-High Energy Cosmic Rays (UHECRs) and perform neutrino astronomy from stratospheric altitudes through the detection of atmospheric Cherenkov light. The first version of the MIZAR ASIC has been sent to production and it is now under test at INFN Torino. The results of the preliminary tests related to the characterization of the chip are presented.

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1. Introduction

Detecting Cherenkov light emitted by Extensive Air Showers (EAS) initiated by Ultra-High Energy Cosmic Rays (UHECRs) or neutrinos presents specific challenges, particularly when observations are performed from near-space platforms, such as low Earth orbit (~ 500 km) or sub-orbital altitudes (30–40 km). Simulations suggest that the Cherenkov signals generated under these conditions can persist for several tens of nanoseconds, depending on the angular separation between the shower axis and the telescope's line of sight. This implies that the Front-End Electronics (FEE) must be capable of time resolutions of around 10 ns or better to adequately capture the signal's temporal profile. In addition to high time resolution, waveform acquisition capabilities become essential to distinguish EAS-related signals from other spurious events, such as direct cosmic ray hits on the detector.

Responding to these experimental demands, INFN Torino initiated the design of a new generation of Application-Specific Integrated Circuits (ASICs). This ASIC is tailored to meet the stringent timing and triggering requirements for high-energy astroparticle detection. The development is closely aligned with recent, ongoing, and future missions focused on UHECR and neutrino detection, including stratospheric balloon experiments like EUSO-SPB2 [1] and space-based concepts such as Terzina [2], POEMMA [3] and M-EUSO [4]. A preliminary overview of the ASIC architecture can be found in [5], with more recent iterations detailed in [6]. In this context, the chip's performance is being evaluated as part of the POEMMA-Balloon-Radio (PBR) mission [7].

The PBR mission [7] is the next balloon-borne mission of the JEM-EUSO program after the EUSO-SPB2 experiment [1], which flew aboard a NASA Super Pressure Balloon launched on May 13, 2023, from Wanaka, New Zealand. EUSO-SPB2 employed a dual-instrument payload: a fluorescence telescope with a MAPMT focal plane aimed at nadir to observe fluorescence from EeV-scale EAS, and a Cherenkov telescope (CTel) equipped with a SiPM camera to detect Cherenkov light from PeV-scale EAS, including those from tau neutrino decays.

The PBR concept builds upon this heritage, however, with some significant differences. The major component of PBR are one large (1-meter diameter), tiltable telescope housing a hybrid focal surface for both fluorescence and Cherenkov measurements. The payload includes also a Radio Instrument (RI) of two antennas mounted beneath the telescope. The optical component is designed to produce two distinct focal spots on the camera for the Cherenkov measurements. More details can be found in [8]. This optical design enhances event discrimination for Cherenkov measurements by allowing the system to distinguish between single-spot direct hits from cosmic rays and dual-spot patterns from off-axis background light, effectively reducing false triggers and improving the signal-to-noise ratio.

At the heart of the Cherenkov component of the instrument is a high-speed focal plane camera, consisting of 512 Silicon Photomultiplier (SiPM) pixels (Hamamatsu S14521-6050AN-04). The camera is optimized for detecting nanosecond-scale optical pulses with a 10 ns integration time and a 512-frame analog memory for signal buffering. The readout system is centered around a dedicated front-end ASIC that performs fast waveform sampling, analog-to-digital conversion, and data derandomization. This architecture enables the precise reconstruction of temporal signal profiles and supports high-throughput event capture with minimal dead time.

The telescope's field of view spans 6.4° in zenith and 12.8° in azimuth. During flight, it

can be pointed across a range of elevation angles—from the horizontal plane to 10° below the Earth's limb—allowing for diverse observational strategies. These include detecting above-the-limb Cherenkov light from UHECR-induced EAS and potentially observing tau-lepton decays resulting from Earth-skimming UHE neutrino interactions.

2. The Front end Electronics

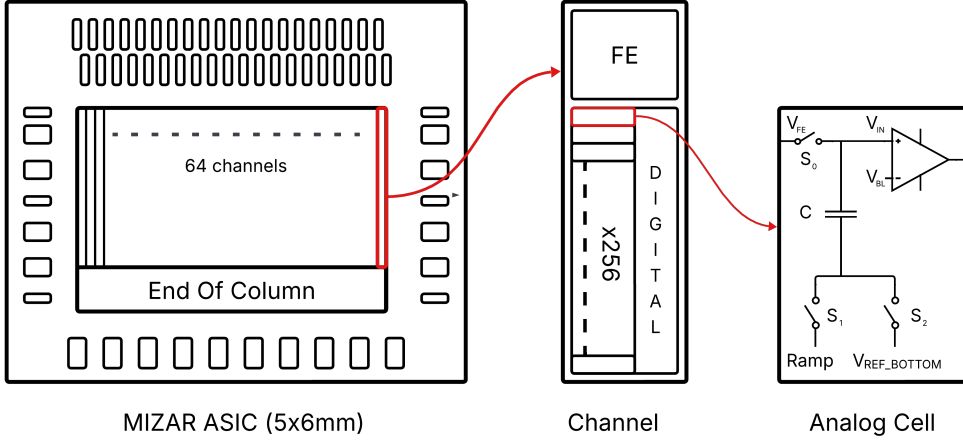


Figure 1: Block diagram of the MIZAR architecture.

The custom-designed ASIC, realized in a commercial 65-nm CMOS process and operating at a 1.2 V supply, offers a highly energy-efficient solution for applications requiring low-power, high-performance signal processing. Specifically developed to handle 8×8 arrays of SiPMs, it provides 64 parallel channels capable of waveform sampling for accurate reconstruction of incoming signals.

Figure 1 illustrates a block diagram of the MIZAR architecture. Each channel features a Front-End (FE) analog block which generates a signal distributed among an array of 256 cells, equipped with analog memories and sampling the input at the nominal frequency of 200 MHz. The memory architecture integrates a storage capacitor and a single-slope ADC per cell, a configuration that simplifies hardware complexity while allowing parallel digitization of all stored samples. This approach significantly reduces system dead time without compromising precision. To further optimize power usage, digitization is decoupled from sampling and is triggered only upon event validation through internal or external trigger signals. The ADC resolution is configurable from 8 to 12 bits, enabling lower-resolution operation for background monitoring, which decreases digitization overhead when fine detail is unnecessary. The analog memory can function as a monolithic unit or be segmented into 32- or 64-cell buffers, enabling multi-buffer acquisition. This buffering allows data from one event to be digitized while the system remains available for subsequent triggers, thus minimizing event losses due to readout latency.

The chip integrates both analog and digital circuitry on a single die using a digital-on-top layout strategy. Figure 2 shows the physical layout of a section as example of this approach. With a compact footprint of $6 \times 5 \text{ mm}^2$ and a target power consumption of 5 mW per channel, the ASIC meets the stringent requirements of future space-based and sub-orbital UHECR and neutrino observatories.

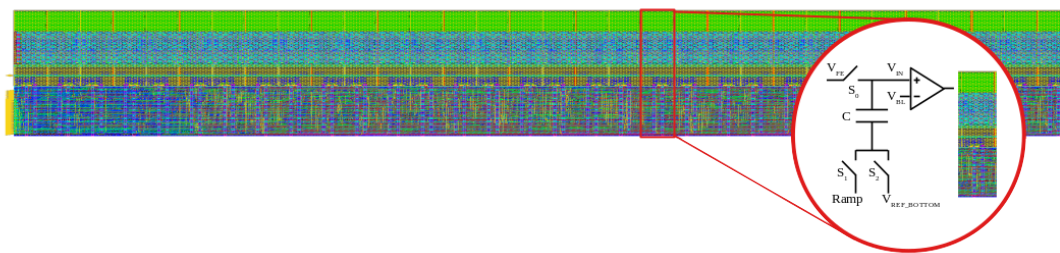


Figure 2: Layout of a section made of 32 cells. In the round area a single cell is magnified next to the analog schematic.

The trigger and readout system is designed to efficiently identify relevant events while minimizing unnecessary data throughput (see Figure 3). Each channel includes two programmable thresholds: a high threshold, used to flag events where most of the signal is localized in a single pixel, and a low threshold, which captures events distributed over neighboring pixels. When the signal exceeds the low threshold, a programmable counter initiates a validation window. If the signal also crosses the high threshold within this interval, only the high-threshold trigger is forwarded to the FPGA; otherwise, the low-threshold trigger is sent. The FPGA then evaluates the 64-bit hitmap from each ASIC, which encodes the active channels, and decides whether to accept the event for readout. The FPGA follows three decision paths:

1. *Event Acceptance:* If the high threshold is exceeded in one or two adjacent pixels, or if the low threshold is exceeded in two to four neighboring pixels, the event is flagged for readout.
2. *Event Rejection:* If the hitmap lacks sufficient spatial correlation, the event is discarded. In cases where a single edge pixel is triggered, the FPGA may check adjacent ASICs for extended event signatures before rejecting the event.
3. *No Response:* If the FPGA fails to respond within a defined time window ($\Delta t_c \sim 80$ ns), the system resets and resumes monitoring new triggers.

Upon event acceptance, digitization is centered on the time at which the signal crosses threshold (t_S). The memory architecture supports flexible segmentation from 32 to 256 cells per channel, with resolutions selectable between 8 and 12 bits. A typical setup uses 8 independent 32-cell blocks, capturing a 160 ns time window with 12-bit resolution. The sampled waveform consists of 32 points spaced by $T_{clk} = 5$ ns, covering the interval from $t_S - 80$ ns to $t_S + 80$ ns.

The digitization of an individual event requires a maximum of $20.5 \mu\text{s}$ ($2^{12} \times T_{clk}$). While one block undergoes conversion, the remaining seven are still available for incoming events. If all buffers are occupied, only the hitmap is sent, and new data cannot be recorded until space is freed. The data output per channel comprises a 48-bit header and 386 bits of digitized waveform, totaling 434 bits. For the entire ASIC, this corresponds to 27,776 bits per event. Transmission is handled by a DDR serializer operating at 400 MHz, with a full ASIC readout taking $34.7 \mu\text{s}$. Thanks to eight parallel conversion chains and assuming a single FPGA can manage five ASICs, the system remains responsive even under high trigger rates. Deadtime occurs only when all buffers are full simultaneously, a scenario mitigated by the memory segmentation and derandomization scheme.

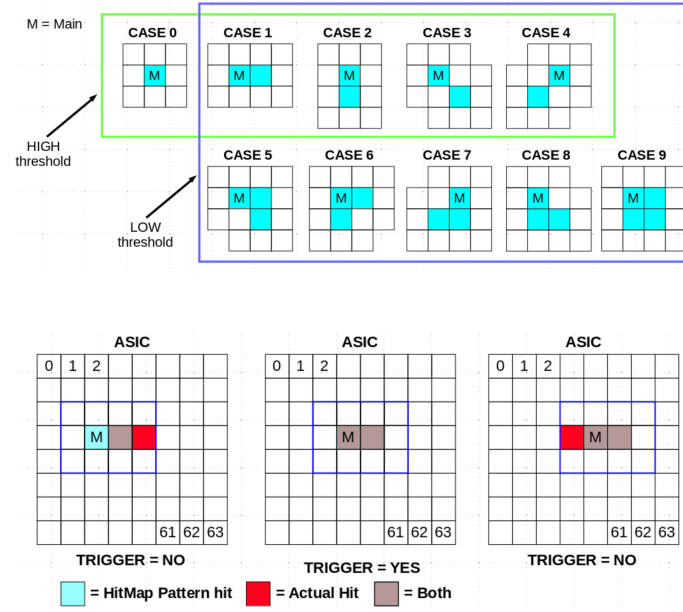


Figure 3: [Top] Hitmap validator pattern case: various patterns are searched by the FPGA to determine whether data is accepted or rejected. [Bottom] Pattern matching algorithm: each pixel is classified as main (M), and the pattern fingerprint is verified. This procedure is carried out in parallel for every pixel and each pattern case [9].

3. Results of the preliminary tests on the MIZAR ASIC

In the first quarter of the year a batch of 200 MIZAR ASICs have been delivered by the foundry and six samples have been bonded on the Front-End Boards (FEBs) received in the same period. In the following a description of the test setup and the results are provided. The test campaign considered the six available chips whose functionalities have been under investigation.

3.1 Setup description

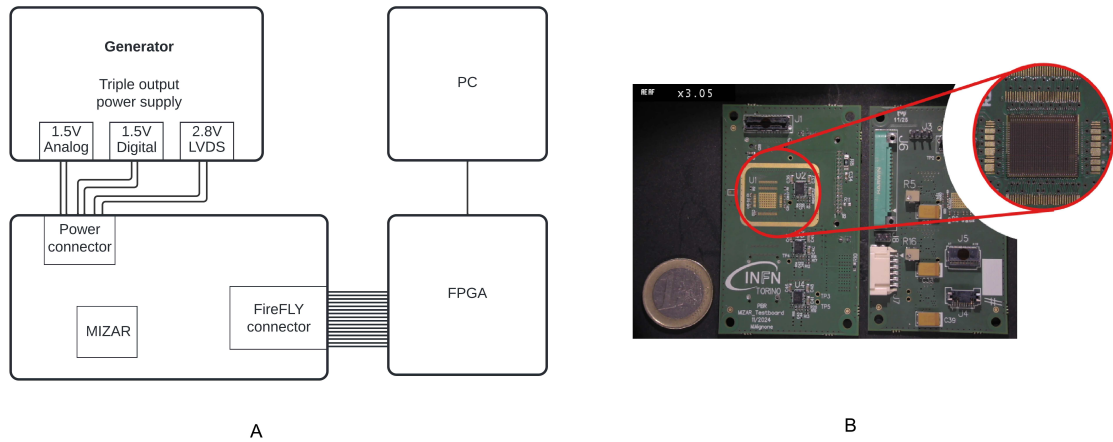


Figure 4: A. Block diagram of testing setup. B. FEB and MIZAR bonded on the board

Figure 4, A depicts a block diagram representation of the test setup used in laboratory. Each MIZAR ASIC has been bonded on a FEB which is connected to a power supply. The generator was set to 1.5 V for both analog and digital blocks and to 2.8 V for the Low-Voltage Differential Signaling (LVDS) lines. The board itself then provides the three power domains to the chips through its voltage regulators. Figure 4, B shows front and back sides of the FEB while the magnified area is a close up of the bonded ASIC. The MIZAR chip is interfaced to the FPGA with a FireFly cable to ensure the configuration and the communication. All chips are active and the power consumption values are consistent with the < 5 mW/channel requirement expected from the simulations.

3.2 SPI and ASIC configuration

Parameter	Value	Description
High VTH	15	Channel high threshold
Low VTH	15	Channel low threshold
CTR_TP_VB	250 μA	Test pulse amplitude
CTR_MIR_VB	320 nA	Current supplied by the ramp generator per unit time
CTR_LO_VTH_GBL	900 mV	High threshold baseline
CTR_HI_VTH_GBL	900 mV	Low threshold baseline
VTH_LSB	1 mV	LSB value
GCR_DC_COUPLING	on	DC coupling
TP sequence	20 ns	Test pulse duration

Table 1: Parameters used for data acquisition.

Table 1 reports the values of the main parameters used during data acquisition. The High and Low thresholds span a range determined by the VTH_GBL and VTH_LSB registers, according to the relation $VTH_GBL - n \times VTH_LSB$, with n ranging from 0 to 31. A value of $n = 31$ corresponds to the baseline set by the CTR_LO_VTH_GBL and CTR_HI_VTH_GBL registers, while $n = 0$ represents the baseline reduced by 31 LSB steps. The test pulse injected into each channel is characterized by the CTR_TP_VB register, which sets its amplitude, and by the TP sequence section, which defines its duration. The configuration also includes the CTR_MIR_VB register, which controls the slope of the ramp used in the ADC conversion by regulating the current supplied over time. The current can be programmed to vary from 40 nA to 640 nA in discrete steps of 40 nA . Throughout the tests, DC coupling was used by enabling the GCR_DC_COUPLING register.

3.3 Test pulse

The FE of each channel can be configured to process the input signal coming from the SiPM or to generate a Test Pulse (TP). Latter was enabled to study both the hitmap generation and the data serialization. The TP provided to each channel was enabled via Serial Peripheral Interface (SPI) by writing the PCR_CAL_MODE register and its amplitude and duration were programmable as well. In this test mode the FPGA was programmed to force the ASICs to provide the raw data of

the hitmap and the converted data. The whole group of available bonded chips successfully sent out the required information, proving the testability of each MIZAR ASIC.

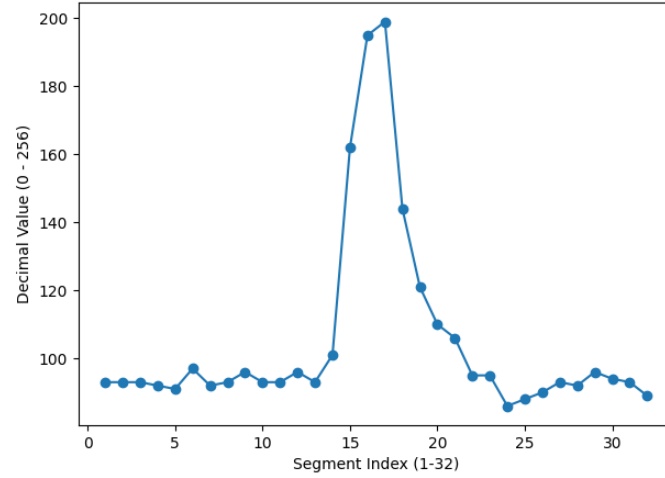


Figure 5: Test pulse acquisition on channel 5, chip 1. 8 bit configuration, 32 cells partitioning.

Figure 5 reports a typical pulse internally generated by the FE, converted by the Wilkinson ADCs and serialized by the digital logic of the end of column. The test was realized at the sampling frequency of 100 MHz using the 32-cells partition and the 8 bits resolution. These results were carried out without any baseline correction yet. In addition, a preliminary characterization of the preamplifier gain response was conducted by varying the 4 bit GCR_GAIN_CTR register settings. The measured gain behavior demonstrated consistency with the design specifications. Finally, a preliminary study on the signals has identified a possible fixed pattern noise, but this feature is currently under investigation since it requires more data acquisitions.

4. Conclusions

A new type of FEE for the detection of the optical Cherenkov signals by EAS directly observed from sub-orbital and orbital altitudes has been described. It is based on a new type of ASIC which is specifically developed for space applications with low power consumption (~ 5 mW/channel) and sufficiently radiation hard. The ASIC's 200 MHz clock frequency enables a precise waveform sampling to clearly recognize an EAS Cherenkov signal from other types of sources such as direct cosmic ray hits, noise spikes or atmospheric events. The developed trigger logic is capable of reducing the fake event rates and the data overhead in order to downlink all the events of interest. The hitmaps also allow the possibility of triggering on signals generated by a bi-focal system. This is considered to be another key way to uniquely recognize an EAS event. The first version of the MIZAR ASIC has been produced and it is currently under tests. Preliminary results indicate a performance in line with the expected basic characteristics of the chip. A more detailed evaluation will follow in the forthcoming months. The MIZAR ASIC is expected to fly on board the PBR mission.

5. Acknowledgments

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