Novel Concepts for On-chip Phase and Flicker Noise Measurements

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Kurzfassung

Im Zuge vielfältiger technischer Weiterentwicklung wächst die Bedeutung von integrierten Oszillatoren mit möglichst stabiler Phase. In neuen Anwendungsgebieten wie Quantencomputern, Radarsensoren für (autonome) Automobile oder dem 6G Mobilfunkstandard sind lokale Oszillatoren mit sehr geringem Phasenrauschen (englisch: Phase Noise) essenzielle Systembestandteile. Zugleich wird durch Verbesserungen in Produktionsverfahren, sowie durch neuartige Halbleiterfertigungstechniken die Größe von integrierten Transistoren immer weiter reduziert. Mit der Verkleinerung der Kanalfläche geht allerdings inhärent ein Anstieg des mittleren Flickerrauschens einher, sowie eine größere Varianz der Bauteile. Des Weiteren werden bei derart geringen Kanalflächen zuvor vernachlässigbare Rauscheffekte relevant, wie etwa das durch Ladungsfallen verursache Generations-Rekombinations-Rauschen (englisch: random telegraph noise).

Im Spannungsfeld zwischen erhöhtem Stromrauschen der einzelnen Komponenten und der eng begrenzten Phasenrauschen-Spezifikation fusst die erfolgreiche Schaltungsentwicklung auf einem eingehenden Verständnis der Stromrauschen-zu-Phasenrauschen-Konvertierungsmechanismen, sowie auf präzisen statistischen Simulationsmodellen.

Das intuitive Verständnis der Schaltung bezüglich Phasenrauschens wird erschwert durch die Komplexität der zugrundeliegenden mathematischen Beziehungen, aber ebenso durch proprietäre verschlüsselte Bauteil-Modelle. In dieser Arbeit wird daher die Möglichkeit untersucht, allgemeine technologieunabhängige Modelle zu verwenden, um einen tieferen Einblick in die qualitativen Zusammenhänge zu erlangen. Hier kann zum einen veranschaulicht werden, dass die Berechnung der Empfindlichkeit der Oszillationsphase als Funktion der Zeit eine Vereinfachung der Bauteil-Modelle erlaubt. Andererseits wird jedoch gezeigt, dass die Simulation der statistischen Eigenschaften der Phase (also das Phasenrauschen-Spektrum) auf akkurate Bauteil-Modelle angewiesen ist.

Weiterhin wird in der Arbeit untersucht wie Abweichungen des Rauschspektrums von der typischen $1/f$-Abhängigkeit das Phasenrauschen verschiedener Oszillatortopologien beeinflusst. Die

Messungen von Strukturen, die auf den neuesten Gate-All-Around und FinFET Technologieknoten gefertigt wurden, zeigen eine direkte lineare Abhängigkeit solcher Effekte, wobei der Gewichtungsfaktor gemäß der Floquet-Theorie berechnet werden kann. Diese Erkenntnis betont weiterhin die Relevanz statistischer Rauschmodelle mit korrekter Spannungs- und Kanalflächenabhängigkeit.

Um derartige Modelle zu entwickeln werden Messwerte für eine Vielzahl von Transistoren benötigt, wobei unterschiedliche Schwellenspannungen, Bauteilgeometrien und angelegte Spannungen charakterisiert werden müssen. Die herkömmlichen Labormessungen sind allerdings zeitintensiv und beanspruchen pro Bauteil eine relativ große Die-Fläche. Die Herangehensweise ist daher im Hinblick auf die straffen Projekt-Zeitpläne der Process-Design-Kit Entwicklung zunehmend ungeeignet. Eine integrierte Teststruktur kann hier als nützliche Ergänzung dienen, um viele Datensätze in einer kurzen Zeitspanne zu erzeugen. In dieser Arbeit wird daher eine neue Methode zur Messung von Flickerrausch-Leistungsspektren mit hoher Messgenauigkeit bei frei wählbaren Spannungen vorgestellt. Im Vergleich zu vorherigen Ansätzen ist es hier möglich, das parasitäre Rauschen weiterer Bauteile im Messsystem mithilfe von Korrelationstechniken zu unterdrücken. Die Daten der Messung der entwickelten Teststruktur zeigen eine gute Übereinstimmung mit hochpräzisen Refernezmessungen.

Selbst bei einem lokalen Oszillator, der mit perfekten Modellen entwickelt wurde, sind unerwartete Effekte im Phasenrauschen nicht ausgeschlossen, etwa aufgrund von Alterungsprozessen oder unvorhergesehenen äußeren Einflüssen. Eine Überwachung der Oszillatoren (englisch build-in self-test) kann daher auch in der Anwendung hilfreich sein, um Verschlechterungen zu erkennen und bei Bedarf Gegenmaßnahmen, wie etwas Spannungsanpassungen, vorzunehmen. In der Arbeit wird eine neue derartige Teststruktur vorgestellt, die vor allem bei Anwendung mit mehreren Oszillatoren, wie etwa Transceiver, mit ihrem minimalen zusätzlichen Flächenbedarf besticht. Die Messung der entsprechenden Schaltung liefert verlässliche Ergebnisse, wobei vor allem die größere Robustheit gegenüber Quantisierungsrauschen im Vergleich zu vorherigen Ansätzen hervorzuheben ist.

Abstract

With the advancement of technology, the need for spectrally pure signal generation is increasing. Emerging applications ranging from quantum computing to automotive radar to increased bandwidth 6G communication rely on local oscillators with tight phase noise specifications. At the same time, enhancements of production processes and novel manufacturing techniques enable an ongoing shrinkage of semiconductor device feature sizes. However, a reduction of the transistor channel area is intrinsically accompanied by a rise in both the mean value of the flicker noise and in device-to-device variations. Furthermore, at this scale previously negligible noise effects begin to play a significant role, such as random telegraph noise due to charge trapping of single charge carriers.

In this conflict field of wanting more stability from noisier devices, successful circuit design is based on a thorough understanding of the phase fluctuation upconversion mechanism and accurate statistical device models.

Intuition about phase noise is often hindered by the complexity of the underlying mathematics and of the proprietary circuit models. Therefore, in this work, the feasibility of using technology-agnostic general compact models to increase design insight is investigated. It is shown that the susceptibility of the oscillator's phase toward noise is a robust quantity, permitting model simplifications for design exploration. The statistical phase properties, on the other hand, are shown to rely on highly accurate compact models.

Furthermore, it is investigated how deviations from the typical $1/f$ flicker noise influence the phase noise of different oscillator topologies. The results measured in leading-edge Gate-All-Around and FinFET technology nodes show a direct upconversion of these effects weighted by the sensitivity of relevant bias conditions according to Floquet theory. These findings further underline the relevance of refined bias- and area-dependent noise models including their statistical deviations.

For the development of the required statistically accurate models, noise data is needed for a multitude of transistors, including variations in device flavors, geometries, and bias conditions. Conventional laboratory measurements are, however, time- and area-intensive, making them increasingly inadequate in light of tight process-design kit release timelines. Here, high-throughput integrated solutions can serve as a valuable supplement to generate high-volume data. Hence, a novel on-chip concept is presented for the high-sensitivity measurement of flicker noise spectra at freely selectable bias conditions. Measurement of the designed test chips shows a good match between the proposed technique and high-precision laboratory equipment.

Even a local oscillator designed with perfect models is not excluded from unexpected phase noise behavior, for example due to aging or unforeseen external influences. In-field monitoring techniques can be used to identify performance degradations and apply countermeasures, such as supply voltage adjustments. Therefore, in this work, the delta jitter is introduced as a novel on-chip phase noise measurement technique with minimal area-overhead for applications with multiple local oscillators. The measurement of the design delivers reliable results and shows increased quantization robustness compared to previous techniques.

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Theoretical Background

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Conclusion and Appendices

List of Abbreviations

AC	alternating current
ACB	AC-buffer
ADC	analog-to-digital converter
BEOL	back end of line
BIST	build-in self-test
BSIM-CMG	Berkley short-channel insulated gate field-effect transistor model - common gate
ctc	cycle-to-cycle
CMOS	complementary metal–oxide–semiconductor
DAC	digital-to-analog converter
DAE	differential algebraic equation
DC	direct current
DRC	design rule check
DIBL	drain induced barrier lowering
DUT	device under test
FD-SOI	fully depleted silicon on insulator
FEOL	front end of line
FFT	fast Fourier transform
FinFET	fin field-effect transistor

FN	flicker noise
FNM	flicker noise monitor
GAA	Gate-All-Around
GDS	graphic design system
GPIB	General Purpose Interface Bus
HDL	hardware description language
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
ISF	impulse sensitivity function
LO	local oscillator
LNA	low-noise amplifier
LPF	low-pass filter
LVS	layout versus schematic
MIM	metal-insulator-metal
MIMO	multiple-input multiple-output
MNA	modified nodal analysis
MOM	metal-oxide-metal
MOS	metal-oxide semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
mux	multiplexer
NMOS	n-channel metal-oxide-semiconductor
NUT	net under test
ODE	ordinary differential equation
PDK	process-design kit
PLL	phase-locked loop

PMOS	p-channel metal-oxide-semiconductor
PSD	power spectral density
PVT	process-voltage-temperature
QAM	quadrature amplitude modulation
PE	priority encoder
PN	phase noise
RO	ring oscillator
R-C	resistive-capacitive
RF	radio-frequency
RTN	random telegraph noise
SMU	source measurement unit
SPICE	simulation program with integrated circuit emphasis
SR	shift register
TDC	time-to-digital converter
TIE	time-interval-error
TU	test unit
VAMP	voltage amplifier
VCO	voltage-controlled oscillator

Chapter 1

Introduction

What is electronic noise?

The answer to this question is not as straightforward as one might think. A commonly stated "definition" goes along the lines that *noise is an unwanted random signal that is added to the desired signal* [7]. While this answer gives a general idea, two annotations need to be made: First, the *unwanted random signals* can be of diverse origins, including, but not limited to quasi-random system-internal crosstalk, interference from external industrial noise sources or even due to atmospheric and cosmic processes. However, in the context of analog circuit design (and in this thesis), the focus is tightened on circuit-internal, fundamental physical noise sources [8,9]. And second, while these fundamental physical processes are in fact *unwanted* in the large majority of circuits, (emerging) applications exist which purposefully utilize the fluctuations: Random number generators [10], energy harvesting circuits [11], amplification using stochastic resonance [12] and certain oscillator synchronization techniques [13, 14] rely on noise for correct circuit operation.

1.1 Motivation

Irrespective of whether the electronic noise is beneficial or detrimental to the system, a thorough understanding of noise processes and its circuit effects forms the basis for successful circuit design. This thesis focuses specifically on the flicker noise (FN) of metal-oxide-semiconductor field-effect transistors (MOSFETs), which can be traced back to the trapping and de-trapping of charge carriers, and its effect on the phase of oscillatory circuits. Establishing a link between the measurement of flicker noise and phase noise (PN) in advanced technology nodes and the development of integrated flicker noise and phase noise measurement macros constitute the main aspects of this work.

1.1.1 Flicker Noise

The continued downscaling of semiconductor devices entails a simultaneous increase of the inversely area-dependent flicker noise [15]. The intensity of this noise process strongly depends on the architecture, materials, and manufacturing of the device. Due to process variations in the trap density variations over orders of magnitude between single device under tests (DUTs) can be observed [16]. Leaving aside the mentioned noise-utilizing applications, flicker noise is generally the source of unwanted signal degradation. For example, flicker noise leads to a deterioration of the signal-to-noise ratio in amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs) [17] and complementary metal–oxide–semiconductor (CMOS) image sensors [18]. Another noteworthy consequence of flicker noise are undesired phase fluctuations in radio-frequency (RF) oscillators and mixers, that is phase noise (see next section).

For advanced and emerging applications, reliable statistical models are needed to build circuits according to tightening specifications (see next section). Here, careful monitoring of the fundamental intrinsic device noise sources forms a fundamental pillar. Furthermore, the recording of high-volume statistics is essential for fabrication monitoring, as well as technology selection (especially in light of the trend to disaggregated systems adding more freedom with respect to the chosen technology node [19]).

The characterization of flicker noise is currently carried out primarily in an off-chip laboratory setup, where the measurement time per device and bias condition is in the range of multiple minutes. Generating high-volume statistics for accurate (Monte Carlo) modeling of a large set of bias conditions can therefore take multiple weeks, a critical time frame in view of tight process-design kit (PDK) release deadlines. For fabrication monitoring, the semiconductor industry typically combines the low-throughput off-chip measurements with high-volume measurements of secondary noise measures (as upconverted phase noise). Here, the former approach is area- and time-intensive (typically 6 pads per DUT with required stepping), while the latter delivers noise results convoluted with direct current (DC) and alternating current (AC) device characteristics rather than the underlying noise spectrum.

Therefore, a high-throughput on-chip flicker noise measurement solution can serve as a valuable complement to the currently employed characterization methods.

1.1.2 Phase Noise

In local oscillators (LOs) electronic noise leads to the fluctuation of the signal's phase. Depending on the application of the oscillator, specific consequences of phase noise might be observed [20]. In digital modulation systems, as quadrature amplitude modulation (QAM), information is encoded in the signal's phase, such that too much noise will lead to symbol errors in the transmitted data (see Fig. 1.1(a)). In communication systems (see Fig. 1.1(b)) transmitter phase noise spreads the energy of the LO in frequency domain, leading to signal leakage into adjacent channels. On the receiving end, an interfering signal, even outside of the observed frequency band, can map to the intermediate frequency in the downconversion process. In Doppler radar systems the frequency-shifted reflection of the target might not be detectable because it is masked by the phase noise of unwanted signal echoes. Lastly, in digital systems phase noise appears as variations of the clock period, which might lead to timing violations and therefore ultimately to bit errors, especially for high-speed data transmission.

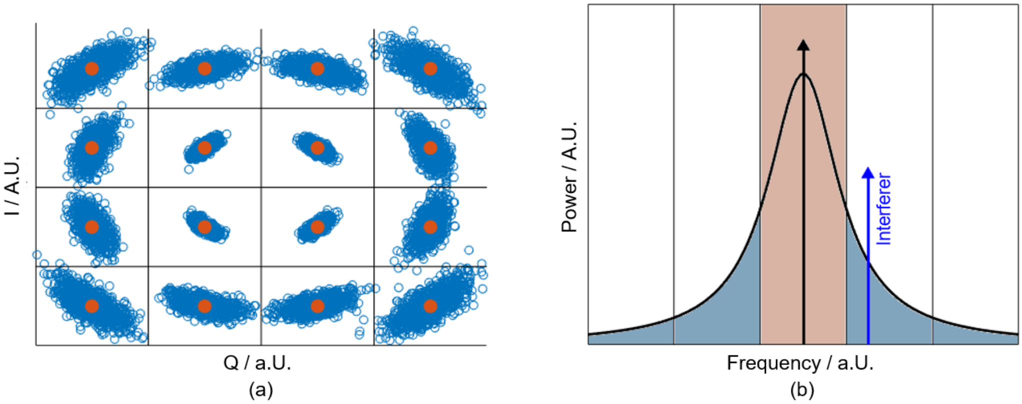


Figure 1.1: (a) Effect of phase and amplitude noise on quadrature amplitude modulation schemes. (b) Phase noise causing power leakage to adjacent channels for signal transmission and sensitivity degradation due to interferers for signal reception.

Due to these effects, various emerging applications require local oscillators with excellent phase noise performance. This includes quantum computing [21] and, naturally, increased bandwidth 5G/6G communication [22]. Here, the latest wireless standards pursue increased peak data rates, higher connection densities and lower latency, which is achieved by phase noise sensitive approaches like multiple-input multiple-output (MIMO) schemes and complex modulation techniques (e.g. 256 QAM) [23].

As for flicker noise also for phase noise on-chip measurement solutions can supplement laboratory measurements. In addition to fabrication monitoring, the focus here lies on in-field measurements of the aforementioned phase noise sensitive applications. As a build-in self-test (BIST) an on-chip measurement macro could for example evaluate LO performance and dynamically adjust the system in a phase noise/power trade-off [24], leading to more energy-efficient systems.

1.2 Thesis Outline

This work is organized as follows:

- Chapter 2 starts with the foundations of integrated circuits (ICs), including technology nodes, available devices, and their modeling. Afterwards, the nonidealities due to electronic noise are discussed, including the mathematical framework for its quantification, a closer look at thermal, flicker, shot, and random telegraph noise (RTN) processes, and measurement approaches.
- In Chapter 3 first electronic oscillators are discussed, followed by a section regarding the effects of noise on the oscillator's phase. Here, again first quantification approaches of phase noise are presented before several techniques for the calculation, simulation, and measurement of phase noise are discussed comparatively.
- Chapter 4 presents how the phase sensitivity and phase noise simulation flow are implemented in this work. Subsequently, an investigation is presented on the influence on transistor model accuracy on phase noise simulation results.
- In Chapter 5 flicker noise and phase noise measurement results for the most-recent Gate-All-Around (GAA) technology node are presented. Deviations from traditional understanding are investigated in detail and compared to measurements conducted on a fin field-effect transistor (FinFET) technology node.
- Chapter 6 deals with approaches for the on-chip measurement of flicker noise and phase noise. For both, after a comparative overview of previous methods, a novel technique is introduced. These are verified in simulation and the measurement of respective implemented test circuits.
- Chapter 7 contains a summary of the presented work and suggests paths for future investigations.

Chapter 2

Noise in Integrated CMOS

This chapter starts with an overview of relevant features of CMOS technology including available devices and transistor compact models. Since in real-world circuits noise is introduced by the devices, the mathematical framework used to characterize these nonidealities is presented. The physical origins of the noise processes are then described in detail (namely thermal noise, shot noise, random telegraph noise and flicker noise), including compact modeling approaches. Lastly, the framework for describing noise in two-port networks is presented.

2.1 Integrated Circuits

The process technology of integrated electrical circuits comes in many varieties, each suitable for a specific set of applications. Silicon, a group IV element, is typically used as the substrate material. While historically the reason was its ability to cleanly form the silicon dioxide layers required for dielectrically isolated MOSFET gates, today it is used mainly due to the mature processing technology and, therefore, low-cost. However, compound semiconductors made of III-V element combinations, such as gallium nitride (GaN) or indium phosphide (InP), exhibit physical properties advantageous for certain applications. Other than in silicon their energy band gap is direct, leading to a high electron mobility and saturation velocity, advantageous for high-frequency circuits. High power applications can also benefit from their larger energy band gap [25]. Furthermore, fully depleted silicon on insulator (FD-SOI) technology can be used for RF applications. Here, the electrical devices are separated from the substrate by an electrically insulating buried layer, thus reducing the leakage current and parasitic capacitances. Moreover, different transistor implementations might be used: Bipolar devices for high-frequency circuits or MOSFETs with their high input impedance for lower power consumption under switching operation [26].

While many variants show advantages for analog RF or high-power applications, bulk silicon CMOS remains the workhorse for the vast majority of applications. In mixed signal circuits, its low-power digital performance and low-cost production often outweigh the advantages of more niche semiconductor technologies. Therefore, in the rest of this thesis, the focus will be on bulk silicon CMOS. Apart from the device-specific noise measurements (Chapter 5), the presented measurement concepts (Chapter 6) are transferable between different technology options.

2.1.1 CMOS Technology Nodes

While the development of the first IC relies on the contributions of many, Jack Kilby and Robert Noyce are often credited as separate inventors of the first (monolithic) IC in 1959 [27, 28]. Since then, the number of transistors per chip has increased exponentially with time, an empirical observation already stated in 1965 by Gordon Moore, known as Moore's law [29]. During the first decades, the planar transistor geometry (see Fig. 2.1(a)) did not change, and downscaling relied mainly on improvements in manufacturing techniques and materials: Ion implantation (1972), dry etching (1974), the addition of silicides (1985), chemical-mechanical polishing (1993), copper interconnects (1997), strained silicon (2002), immersion lithography (2004) and high-k metal gates (2007) represent a few of the key milestones of early-day CMOS [30]. During this time, according to Dennard scaling, supply voltage reductions compensate feature size reductions to achieve constant electric fields and constant power consumption per unit area [31]. However, at too small dimensions, this relation brakes down: The reduction of the supply voltage necessitates a reduction of the threshold voltage, which entails prohibitively large leakage currents in the bulk of the transistor [32]. This increased power dissipation per area ("power crisis") led to the development of the FinFET transistor geometry introduced in 2011 (see Fig. 2.1(b)). Here, a vertical channel sticks up from the substrate and is enclosed by the gate on three sides, therefore improving electrostatic control. This concept is brought to completion in current state-of-the-art technology nodes with the introduction of the GAA geometry, where the gate surrounds the channel on all sides of multiple stacked channels (see Fig. 2.1(c)). The new transistor geometry is complemented by enhancements in the back end of line, such as putting the power delivery network on the backside of the wafer to avoid routing congestion. Furthermore, new techniques in lithography, such as extreme ultraviolet and multi-patterning, lower the minimum resolvable feature size and pave the way for ever smaller structures [33].

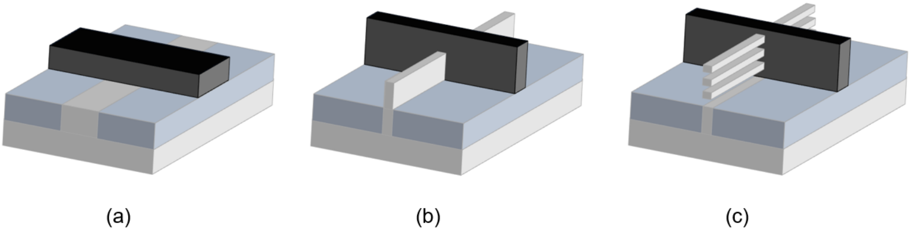
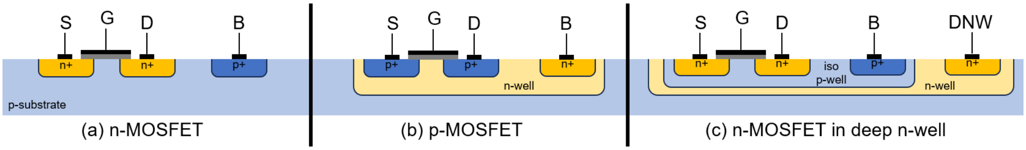


Figure 2.1: Evolution of transistor geometry from (a) planar to (b) FinFETs to (c) Gate-All-Around. The gate is displayed in black.

Different technology nodes were used for the experiments in this thesis: The on-chip measurement concepts (Chapter 6) are technology agnostic. The corresponding experiments were implemented in a $14\,\mathrm{nm}$ FinFET technology. Additionally, some more detailed investigations regarding the upconversion of device noise to phase noise in state-of-the-art technology nodes (Chapter 5) were conducted in the currently most advanced $2\,\mathrm{nm}$ GAA technology node with backside power distribution.

2.1.2 Available Devices in CMOS

Independent of technology node, the fabrication of a CMOS integrated circuit [26] can be split into two portions: In the front end of line (FEOL) semiconductor devices are formed on the substrate, which is typically a p-type silicon wafer with a lightly doped p-type epitaxial layer. By repeated implantation and deposition steps patterned by photolithography, n-/p-wells, diffusion regions and gate structures are shaped (see Fig. 2.2). Subsequently, in the back end of line (BEOL) multiple layers of metalization connected by vias are deposited to provide interconnects between the devices. In modern technology nodes the BEOL consists of 10 to 20 copper layers and additionally houses the majority of passive devices, such as capacitors, resistors and inductors. From the top-most metalization layer the chip can be connected to the external world, either via aluminum pads for wafer-level probing or via bumps connecting to semiconductor packages or other ICs (e.g. via the flip-chip method).



(a) n-MOSFET

(b) p-MOSFET

(c) n-MOSFET in deep n-well

Figure 2.2: Transistor structure in CMOS, for graphical simplicity a planer technology node is displayed. S, G, D and B are the source, gate, drain and bulk terminals of the transistor, respectively. DNW indicates the deep n-well contact.

2.1.2.1 Active Devices

The active devices [9] available in a typical CMOS process are n-/p-MOSFETs, diodes and, if supported, bipolar transistors. For the former two, which are used in the experiments in this thesis, the basic physics of their operation is described qualitatively in the following. Basic quantitative descriptions and second-order effects are addressed in Section 2.1.3.

The pn junction can be considered to be the fundamental building block of all semiconductor devices. It consists of p-type silicon (i.e. doped with electron acceptors like boron) in direct contact with n-type silicon (i.e. doped with electron donors like phosphorus). While n-type silicon exhibits an excess of electrons acting as majority charge carriers, the p-type exhibits a lack thereof, termed electron holes. Due to the concentration gradients, the respective charge carriers move across the junction in form of diffusion currents, where they recombine with their corresponding counterpart. In this process, they leave the oppositely charged core of the impurity atoms fixed in the silicon lattice behind. An electric field develops between them leading to a drift current opposing the diffusion movements of the charge carriers. An equilibrium develops and the region around the junction, called the depletion region, is void of free charge carriers.

Diodes, which are two-terminal semiconductor devices with a preferred current direction, utilize the properties of the pn junction. Applying a positive voltage at p-type silicon with respect to n-type silicon (i.e. a forward bias) opposes the intrinsic electric field in the depletion region and therefore causes more minority charge carriers to drift over the junction and recombine with their respectively opposite majority charge carriers. In contrast, applying a reverse bias to the junction leads to an increasing electric field in the depletion region, opposing the drift and therefore the recombination of minority charge carriers. In total, the current between the two terminals depends exponentially on the applied voltage within moderate limits. An excessive reverse voltage triggers breakdown mechanisms, such as avalanche breakdown due to current multiplication by collisions of strongly accelerated charge carriers or Zener breakdown due to charge carrier tunneling. In the experiments in this thesis, diodes are not used as elements during normal circuit operation. They are however employed as "antenna diodes" to protect the vulnerable gate oxide from excessive positive charge build-up during plasma etching steps in the fabrication of the IC. The respective antenna diode is formed between the grounded p-substrate and an n-diffusion, and is therefore in reverse bias during normal circuit operation, but can dissipate charge build-up via leakage/breakdown currents of the diode.

MOSFETs are semiconductor devices used to switch or amplify signals. The applied voltage at the gate terminal of the device modulates the current between the source and drain terminals. Fig. 2.2(a) shows the structure of an n-channel metal-oxide-semiconductor (NMOS) transistor: Two back-to-back pn junctions are formed between the source and drain n-type diffusion regions and the more lightly doped p-substrate. A conductive gate structure is formed on the silicon surface between the source and drain regions, which is insulated from the silicon by a dielectric material. The application of a positive voltage at the gate with respect to the source terminal repels holes into the bulk of the p-doped substrate, whereas electrons are attracted to the gate interface as minority charge carriers. At the threshold voltage V_T, sufficient electrons are attracted to the substrate surface to invert the silicon and form an n-type channel between the n-type source and drain regions, therefore allowing the flow of current. A fourth terminal termed bulk connects to the substrate of the device. While it is often tied to ground potential, it can also be used to tune the threshold voltage via the body effect. This modulating effect is strongly reduced in FinFET technology nodes due to the fully depleted channel region, and it is completely absent in GAA transistors due to the isolated channels. In modern technology nodes, the value of the threshold voltage can rather be adjusted by the selection of appropriate metal gate work functions [34], providing multiple discrete transistor "flavors" to the designer.

Depending on the applied gate-to-source voltage v_{gs} and drain-to-source voltage v_{ds} three operating regions of MOSFETs can be defined:

- Off-region for $v_{gs} < V_T$: Only marginal leakage current flows between source and drain due to the back-to-back pn junctions.
- Linear region for $v_{gs} > V_T$ and $0 < v_{ds} < v_{gs} - V_T$: Current can flow between the source and drain terminals through the above-described channel. Here, the transistor behaves as a resistor with a resistivity controlled by the gate voltage.
- Saturation region for $v_{gs} > V_T$ and $v_{gs} - V_T < v_{ds}$: High drain voltages reduce the effective potential in the channel close to the drain contact, leading to a pinch-off of the inversion channel. Due to the high electric field in the pinch-off region, current continues to flow, now at a saturated level independent of v_{ds},

In addition to applied voltages and material properties, the physical dimensions of the transistor determine the amount of current flow. As a first-order approximation, the current is proportional to the channel width W, and inversely proportional to its length L. In FinFET and GAA technology nodes the effective width cannot be continuously adjusted, but only in discrete steps corresponding to the number of fins/ribbon stacks comprising the channel. A further possibility to adjust the channel width is to form transistors with multiple fingers, that is multiple interweaving source/drain diffusion regions connected in parallel.

A p-channel metal-oxide-semiconductor (PMOS) transistor is formed equivalently, as can be seen Fig. 2.2(b), with two p-doped diffusion regions in an n-well. Here, a negative voltage needs to be applied to the gate with respect to bulk to achieve current conduction between the source and drain regions through an inversion channel consisting of electron holes. The bulk terminals of separate PMOS devices can be connected to different potentials according to circuit needs. This flexibility is missing in NMOS devices due to the common substrate connection, but can be regained by introducing a deep n-well, which isolates the NMOS p-well from the substrate, as shown in Fig. 2.2(c).

For sensitive circuitry (especially in analog designs) isolation techniques between neighboring transistors should be employed to prevent influences from external fluctuation, for example, the substrate potential. Apart from placing them in separate wells, guard rings can be used. These consist of a ring-shaped bulk connection around the protected group, providing a low-resistance connection to a stable potential.

2.1.2.2 Passive Devices

The resistors implemented in the conducted experiments consist of thin films of resistive material (e.g. tungsten) deposited within the metal stack. The width and length are chosen to reach a specific resistance value and comply with reliability requirements. Often the structures are protected by guard rings to ensure a stable environment and therefore stable parasitic effects toward the substrate.

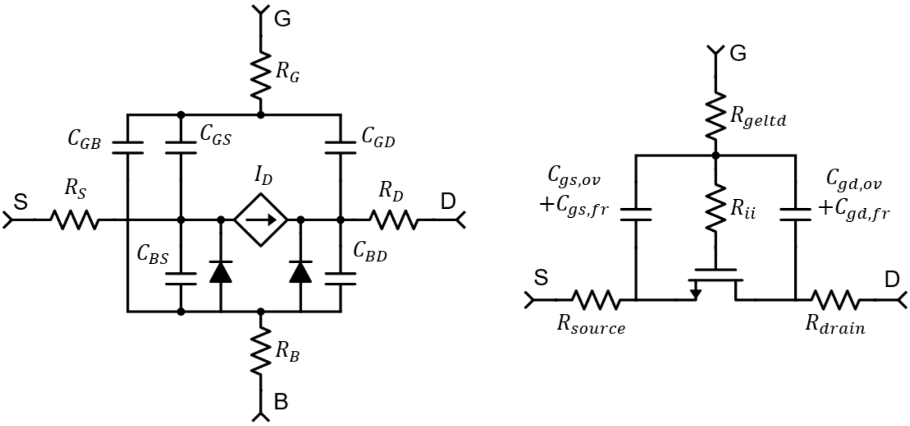
Capacitances can be manufactured using various approaches: metal-oxide-metal (MOM) capacitors consist of interdigitated fingers of multiple layers of the metal stack. In this thesis, this type of capacitor is used for all capacitors connected to signal nets. Another type is the metal-insulator-metal (MIM) capacitors, which consists of two metal plates separated by a thin insulating dielectric material. These are typically located higher up in the metal stack and require dedicated processing steps during fabrication. Due to its large series resistance, it is not suitable for higher signal frequencies. Lastly, there is the metal-oxide semiconductor (MOS) capacitor utilizing the inherent capacitance between a MOSFET's gate and channel. The source, drain and bulk terminals are shortened and should, in the case of a PMOS transistor, be connected to the higher voltage, since then an inversion layer is created, decreasing the distance between charges and, therefore, increasing the capacitance. Due to the MOS capacitor's voltage dependence and the MIM capacitor's frequency behavior these two types are used as decoupling capacitors, stabilizing power supply voltages.

Inductors are formed by planar spirals on the topmost metal layer. The reasons for this placement are mainly the low resistivity and large distance from the substrate to reduce parasitic capacitances. Typically, they consist of only few turns, since inner turns do not contribute much magnetic flux, do, however, increase parasitic resistance [8].

2.1.3 Modeling of MOSFETs

To predict the behavior of a circuit, the electrical properties of the devices need to be represented by mathematical models. Since the focus of this thesis is on the noise produced by transistors, a more detailed look will be taken at transistor compact models.

SPICE level 1 is a basic large-signal MOSFET model, that uses only around 20 parameters to describe a transistor's DC and AC behavior. The simplicity of its physics-based equations make it an instructive and intuitive, albeit limitedly accurate, model, especially for advanced nodes. Fig. 2.3(a) depicts the network employed to model parasitic resistances and capacitances. The latter consists of bias-dependent (e.g. depletion region capacitances) and bias-independent contributions (e.g. overlap capacitances). Additionally, the pn junction between the well/substrate and the diffusion region is modeled by a diode equation. The drain source current is represented by a bias-dependent current source. The underlying equations are adjusted for the respective region of operation discussed in Section 2.1.2.1:



(a) SPICE Level 1

(b) Version of BSIM-CMG

Figure 2.3: Parasitic networks of (a) SPICE Level 1 and (b) a version of BSIM-CMG. Adapted from [35].

$$i_D = 0 \qquad \text{for } v_{gs} < V_T \tag{2.1a}$$

$$i_D = \frac{\mu_0 C_{ox} W}{2L}\Big(2\big(v_{gs} - V_T\big)v_{ds} - v_{ds}^2\Big)\big(1 + \lambda v_{ds}\big) \qquad \text{for } 0 < v_{ds} < (v_{gs} - V_T) \tag{2.1b}$$

$$i_D = \frac{\mu_0 C_{ox} W}{2L}\big(v_{gs} - V_T\big)^2\big(1 + \lambda v_{ds}\big) \qquad \text{for } 0 < (v_{gs} - V_T) < v_{ds} \tag{2.1c}$$

In the off-region the current is approximated to be zero (Eq. 2.1a). In the linear region, it is described by the Sah equation (Eq. 2.1b), which is derived from first-principle considerations of device physics [36]. Here, μ_0 is the surface mobility of the channel and $C_{ox} = \epsilon_{ox}/t_{ox}$ is the gate oxide capacitance per unit area. These two physical parameters can be combined to an empirical transconductance model parameter. The threshold voltage V_T can either be supplied as a model parameter or calculated from material properties, such as substrate doping, intrinsic carrier concentration, oxide charge, etc., including shifts due to nonzero source bulk voltage. As discussed, in the saturation region pinch-off leads to a saturation of the current for $v_{ds} > v_{gs} - V_T$, resulting in Eq. 2.1c. Another consequence of pinch-off is an effective reduction of the transistor's channel length, leading to an increase in drain current. This effect is modeled by the parentheses at the end of the equations with the channel length modulation parameter λ. An example output characteristic as described by the model equations is depicted in Fig. 2.4.

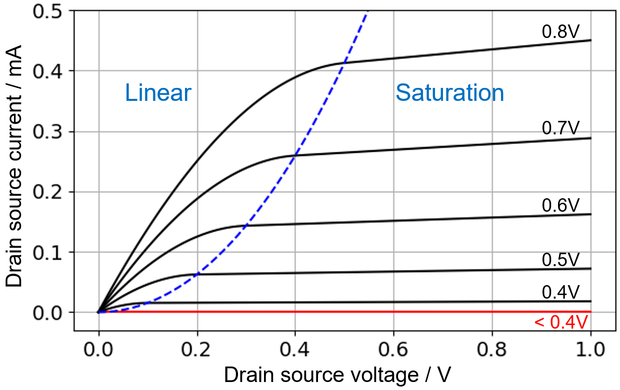


Figure 2.4: Transistor output characteristic as described by the SPICE level 1 transistor model with source and bulk terminals at ground potential or different gate voltages. The values are based on a standard threshold voltage transistor of an advanced FinFET technology node.

For small changes in the signal, linearized small-signal parameters can be defined. The transconductance g_m and output conductance g_{ds} describe how the drain current i_d reacts to small changes in the gate voltage and drain voltage, respectively:

$$g_m \equiv \frac{\partial i_d}{\partial v_g}, \quad g_{ds} \equiv \frac{\partial i_d}{\partial v_d}. \tag{2.2}$$

More accurate models have been developed to describe second-order effects. For example, subthreshold equations are used to describe the conduction of the transistor in weak inversion: In real devices, the drain current for $v_{gs} < V_{th}$ is not exactly zero but rather decreases exponentially with v_g, due to diffusion currents. Furthermore, many model corrections are necessary because of the high electric fields associated with small device dimensions. Velocity saturation is the most important short-channel effect, describing a saturation of charge carrier velocities with increasing electric field due to phonon scattering [8].

Currently, state-of-the-art technology nodes are typically based on BSIM-CMG, a model tailored to common multi-gate geometries as FinFETs or GAA transistors. It includes physical effects relevant for deeply scaled submicron dimensions, such as subthreshold conduction, mobility degradation, velocity saturation, velocity overshoot, temperature variation, quantum-mechanical effects, gate tunneling current, gate-induced-drain-leakage and physics specific to novel materials [37]. The resistive-capacitive (R-C) parasitic network of Berkley short-channel insulated gate field-effect transistor model - common gate (BSIM-CMG) depends on several model switches regarding, for example, the represented transistor geometry or the modeling of non-quasistatic effects. A commonly used version is shown in Fig. 2.3(b), where the transistor symbol represents the core DC model [35]. In total, hundreds of model parameters are needed to describe the transistor's behavior, a number often multiplied by so-called binning, where distinct parameter sets are used for different transistor length and width ranges. In addition, proprietary foundry models might be partially encrypted.

At high frequencies, the behavior of a transistor becomes more sensitive to its direct environment (routing, neighboring devices, etc.), since parasitic capacitances play a larger role. To guarantee accurate modeling also for RF applications, special high-frequency transistors are often used, which offer well-defined boundary conditions due to prescribed routing in the lower metals and the use of guard rings. Extensive parasitic R-C networks might be included in the respective transistor compact model to accurately describe the transistor's behavior over a large frequency range.

2.1.4 Digital and Analog Circuit Design Process

The same process technology is used for quite distinct families of electrical circuits: Analog and digital circuits. While analog circuits operate on a continuous range of signal values, digital circuits use an abstraction, where the signal is restricted to two discrete states (0 indicated with low voltage, 1 indicated with high voltage). The former includes among others the RF circuits discussed in Chapter 1 for communication and radar applications. With the later, general purpose or application-specific integrated circuits for signal processing can be realized. Both types rely on the same presented semiconductor devices, yet their design process differs greatly: While the digital design process is semi-automated relying on a high level of abstraction, analog layouting relies on a lot of manual effort (with automation efforts underway, e.g. [38]).

In the analog design process a schematic representation of the indented design is first created. Its behavior is then investigated and checked against the specifications by schematic-level simulations by using compact models of the utilized devices. Simulation types typically performed include DC, AC and transient simulations. Here process corner models for frontend and backend can be included to simulate deviations from nominal operation due to process tolerances, temperature and voltage deviations. An alternative to the worst-case corner approach are Monte Carlo simulations. Here, the variability is simulated in multiple runs by statistically drawing the model parameters from a given probability distribution. Since variations are simulated independently between devices this technique will reveal mismatch effects. Furthermore, reliability simulations can be carried out to flag exceedance of devices' voltage or current reliability limits. As a next step, the layout of the design is created. The single analog devices, which are often included as parameterized cells in the process design kit, are placed and routed manually by drawing the respective mask layers. Multiple physical verification steps ensure functionality of the produced circuit: The design rule check (DRC) ensures manufacturability, for example, by verifying that the minimum feature distance rules or via rules are respected. A layout versus schematic (LVS) check is run to ensure that the drawn layout matches the circuit described by the corresponding schematic. An antenna check calculates if parts of the circuit might be damaged during production by plasma charging, an effect that can be mitigated by antenna diodes or jumper connections. A fill flow is run, which draws unconnected shapes in empty areas of the layout to avoid uneven thickness of the layer due to irregularities in the layer densities. Finally, a parasitic extraction flow creates a netlist of the design layout, including parasitic capacitances and resistances due to the specific layout implementation. Simulations can be run to verify the performance of the finished design. In a hierarchical approach, basic building blocks are integrated into a system with complex functionalities.

In digital circuits, combinational logic gates can be build from NMOS and PMOS transistors, that carry out simple boolean operations (NOT, AND, OR, XOR, etc.) on the signals at their input terminals. Using feed back paths between logic gates, sequential logic functions are enabled, which depend not only on the current state of their input terminals but also on their history. The most important element with such a memory function is the D flip-flop, which in its basic version has two input terminals, data D and clock CLK, and one output Q. It functions in a way that a rising edge of the clock signal sets the value of Q to D and latches at this value until the next rising edge of CLK. Using both combinational and sequential building blocks more complex functions acting on binary numbers can be constructed, such as arithmetic circuits, shift registers, memory arrays or finite state machines. In a yet higher level of abstraction hierarchy, these are used to build the microarchitecture of a microprocessor [39].

In the digital design process, the schematic and layout of the circuit are generated semi-automatically. hardware description language (HDL) are used to describe how the circuit should operate. After functional verification, the behavioral description is translated into logic gates in the synthesis step. Taking into account floor planning, the corresponding standard cells are automatically placed. Here, in a speed/power trade-off variants with different drive strengths and threshold voltages exist. The power grid, signal routes, and clock tree are automatically routed. During the entire design process, timing analyses are performed to ensure compliance with timing limits. Finally the layout is streamed out as a graphic design system (GDS) file and sent for production.

In both digital and analog circuits, noise can impede the indented circuit operation. To ensure compliance with specifications, noise descriptions must be included in device compact models (see Section 2.2.3) and respectively implemented in circuit simulators.

2.2 Electronic Noise

In all semiconductor devices, active as well as passive, physical processes occur that lead to nonreproducible statistical current fluctuations around the described ideal behavior. Detailed investigations into its origin and careful modeling are essential due to its detrimental effects on desired circuit behavior, as described in Chapter 1.

2.2.1 Description of Noise

To characterize noise, a mathematical framework [40] is needed to describe the statistical fluctuations. Here, a noise process $a(t)$ is considered, where any DC value has been subtracted, leaving the pure statistical variations with a mean of $\overline{a(t)} = 0$. While the statistical variations due to noise are unpredictable, it is possible to make statements about the probabilistic properties of the process, for example about its probability distribution and related measures as the variance. In terms of physics the variance describes the power contained in $a(t)$ and can be calculated by the function's mean square value

$$\sigma^2 = \overline{a(t)^2} = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} a(t)^2 dt. \tag{2.3}$$

The variance does however not fully describe the noise process. For instance, Fig. 2.5 shows in the left column four noise processes, with each exhibiting the same mean square value. The

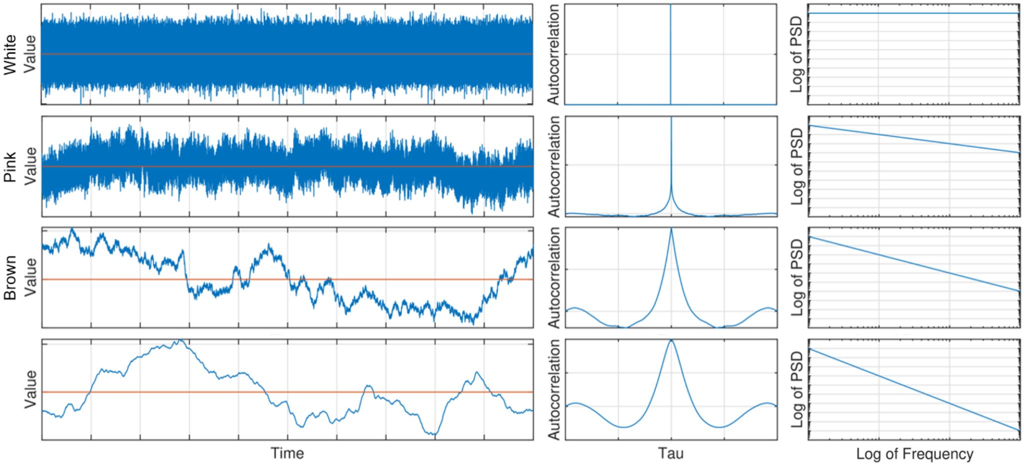


Figure 2.5: For white, pink, brown and $1/f^3$ noise processes the time evolution, auto-correlation function and power spectral density are shown.

difference between these processes lies in the correlation between values at different points in time. This notion is quantified with the auto-correlation function

$$\rho(\tau) = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} a(t)a(t+\tau)dt, \tag{2.4}$$

which calculates the correlation coefficient between the noise processes and a time-shifted version of itself (see middle column of Fig. 2.5). In case of white noise (see first row of Fig. 2.5) no information about a future value can be gained by the knowledge of past values, leading to an autocorrelation function, which is only nonzero at $\tau = 0$. The other depicted noise processes show an increasing correlation between its respective time-shifted values. Notably, the autocorrelation function contains information about the variance as $\rho(0) = \sigma^2$.

Changing the point of view, a noise process can also be described in frequency domain: The power spectral density (PSD) $S_a(f)$ describes the noise power contained in a 1 Hz frequency band around f. Therefore the total noise power is given as an integral over all frequencies

$$\sigma^2 = \rho(0) = \int_0^\infty S_a(f)df. \tag{2.5}$$

A connection between the PSD and the auto-correlation function can be made with the Wiener-Khinchin theorem, describing them as Fourier-transform pairs:

$$S(f) = 2\mathcal{F}[\rho(t)](f) = 2\int_{-\infty}^{\infty} \rho(\tau)exp(-2\pi i f\tau)d\tau. \tag{2.6}$$

The last column of Fig. 2.5 depicts the PSDs of white, pink, brown and $1/f^3$-noise. While the first is characterized by its flat PSD, the latter exhibit a spectrum inversely proportional to f,f^2 and f^3, respectively.

2.2.2 Physical Noise Processes

Different physical processes are at the root of current and voltage fluctuations. Here, the main mechanisms influencing integrated electronics are described with a focus on their effects in MOSFETs at conventional frequency ranges and temperatures (below THz, and at noncryogenic temperatures).

2.2.2.1 Thermal Noise

At nonzero temperatures the thermal energy manifests itself as random motion of the charge carriers. In case of an open circuit these statistical fluctuations lead to a voltage across the resistor with a mean square value of

$$S_u(f) = 4k_BTR, \tag{2.7}$$

where k_B is the Boltzmann constant, T the temperature and R the resistance [8]. As an equivalent circuit to the noisy resistor a noiseless resistor can be used with either a voltage noise source in series following Eq. 2.7 or a current noise source in parallel with a mean square value of

$$S_i(f) = 4k_BT\frac{1}{R}. \tag{2.8}$$

The PSD of the noise is constant with frequency, that is white. This result can be derived by first calculating the thermal noise current due to a single charge carrier, which can be related via the equipartition theorem to the temperature. The autocorrelation function of a single noise pulse can be calculated assuming a constant mean free time τ_c between collisions. Summing over all charge carriers, the spectrum of the total current can be calculated using Eq. 2.6. Limitations of this derivation arise for very high frequencies (necessarily, since $\int S(f)df$ must be finite). Here, and in the case of very low temperatures, quantum effects come into play. Both can be described with a multiplying factor, which causes the PSD to decrease exponentially toward zero for high frequencies, for example at room temperature in the terahertz regime [41]. Notably, frequency-dependent complex electrical impedances, for example due to capacitors or inductors, lead to a total nonwhite PSD of the passive network, since the purely reactive elements do not exhibit thermal noise.

In case of a MOSFET thermal noise is present in the channel. However, it can only be treated as a single resistive element with $R = \frac{1}{g_{ds}}$ in thermal equilibrium ($u_{ds} \approx 0$). Otherwise, the potential varies along the channel length, such that the noise voltage in an infinitesimal channel element modulates the transconductance g_m and output conductance g_{ds} of the preceding and subsequent channel regions. In a charge-based model these effects can be taken into account for each channel element and integrated over the channel length to find an equivalent parallel current noise source the whole transistor with [42]

$$S_i(f) = 4k_B T \frac{\mu_{eff}}{L_{eff}^2}(-Q_{inv}) \quad \text{in general,} \tag{2.9a}$$

$$S_i(f) = 4k_B T g_{ds} \quad \text{for small drain voltages,} \tag{2.9b}$$

$$S_i(f) = 4k_B T \frac{2}{3} g_m \quad \text{in saturation.} \tag{2.9c}$$

Here, μ_{eff} is the effective electron mobility, L_{eff} the effective channel length and Q_{inv} the total inversion charge in the body. While Eq. 2.9a is valid for all operating regions in strong inversion of long-channel transistors, Eqs. 2.9b and 2.9c can be shown to be equivalent for the stated operating points, where the former is consistent with expected results.

A further consequence of thermal noise in the channel is induced gate noise. This term describes the coupling of charge fluctuations in the channel through the gate capacitance to the gate terminal. Long-channel devices are more affected by this phenomenon, where increased channel resistance is combined with a large gate capacitance. The resulting capacitive noise current between the channel and the gate has a mean square value proportional to the squared frequency of the noise component f^2. Since the previously discussed drain current noise and the induced gate noise result from the same physical origin, they can be shown to be correlated with a partly imaginary correlation coefficient due to the phase shift of the effects [43].

In modern technology nodes with short channel transistors typically higher noise values are observed compared to theoretical predictions. Here, additional effects such as velocity saturation, channel length modulation and drain induced barrier lowering (DIBL) need to be considered for an accurate description of thermal noise [44, 45].

2.2.2.2 Shot Noise

When discrete charge carriers encounter a barrier, such as, for example, a pn junction, their transition occurs as statistically independent charge pulses with length τ_t. In a macroscopic view this leads to fluctuations in the current with a PSD of

$$S_i(f) = 2eI_0, \tag{2.10}$$

where e is the elementary charge and I_0 the average current. For high frequencies ($f \gtrsim \tau_t$) the PSD falls off to zero. As for thermal noise, the spectrum is therefore white, but in contrast does not depend on temperature.

Shot noise is of concern primarily in bipolar transistors, where it is observed in both the base and collector currents (due to the involved pn junctions). In MOSFETs it only appears in a comparatively small amount in the gate leakage current and subthreshold conduction, for example due to the tunneling of charge carriers [8]. The drain current in a device operated above threshold is, on the other hand, free of shot noise, since no potential barrier needs to be crossed by the charge carriers.

Recent investigations of transistors with short channel lengths point out linkages between the fundamental mechanisms of shot and thermal noise. The channel noise previously described as thermal effects is attempted to be modeled as shot noise, which is suppressed below the value of Eq. 2.10 due to scattering mechanisms, such as electron-electron interactions [46].

2.2.2.3 Random Telegraph Noise

In semiconductor devices electrons can be captured by trap states like interface states or defects, resulting in a fluctuation of the number of available charge carriers. In MOSFETs the trapped charges might additionally modulate the drain current by changing the channel potential. In case of a single trap the resulting drain current noise is termed RTN, and leads to a switching between two discrete states (see left panel of Fig. 2.6). The right panel of Fig. 2.6 shows the corresponding

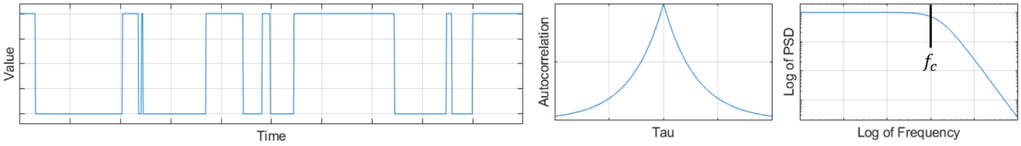


Figure 2.6: Random telegraph noise signal with its corresponding autocorrelation function and power spectral density.

PSD, which is white for low frequencies and drops with f^2 above the corner frequency f_c, which depends on the time constants τ of the trap:

$$S_i(f) = \frac{K}{1 + (2\pi f \tau)^2}, \tag{2.11}$$

where K is an empirical, bias-dependent constant subsuming physics regarding the trap's time constants and current modulation mechanism.

For multiple equivalent traps (e.g. due to doping atoms), the resulting current noise is a superposition of many individual RTN processes with identical time constants, where stochastic independence between transitions is assumed. Although the term is used inconsistently, the resulting noise is often called generation-recombination noise.

2.2.2.4 Flicker Noise

Additionally to the flat spectrum at high frequencies (shot and thermal noise), the drain current of a MOSFET exhibits a $1/f$-dependence for frequencies below a device-specific corner frequency. This phenomenon, generally called flicker noise, has not only been observed in electrical, but all kinds of systems: The amount of rainfall, the rate of traffic flow, nerve membrane voltages, and economic data exhibit fluctuations with the same spectral dependence [47]. In semiconductor devices, measurements have been conducted to a lower frequency limit with cycle times of up to three weeks with no sign of flattening. The fact that the integral of the spectrum tends toward infinity if the lower bound approaches DC does not necessarily imply that a lower frequency limit must exist. After all, DC corresponds to an infinitely long signal, where an infinite energy content should not surprise (and is furthermore not relevant in practice) [8, 48].

Regarding the underlying physical origin of flicker noise in semiconductor devices, no consensus has yet been reached. As first explanatory approaches two theories emerged, which still today lie at the basis of many models: The McWhorter model proposed in 1957 and Hooge model proposed in 1972.

The McWhorter model [49] explains the noise as the additive effect of many charge-trapping and detrapping processes at the channel-insulator-interface. Here, a trapped charge modulates the drain current by changing the surface potential and therefore the number of available charge carriers for current transport. Due to statistically distributed trap time constants the single RTN spectra according to Eq. 2.11 sum up to an overall $1/f$-slope (see Fig. 2.7(a)). The required reciprocal distribution of carrier lifetimes can be explained by the exponential time dependence of tunneling processes: Charges tunnel between the channel and trap states, which have a uniform spatial distribution in the gate oxide [50].

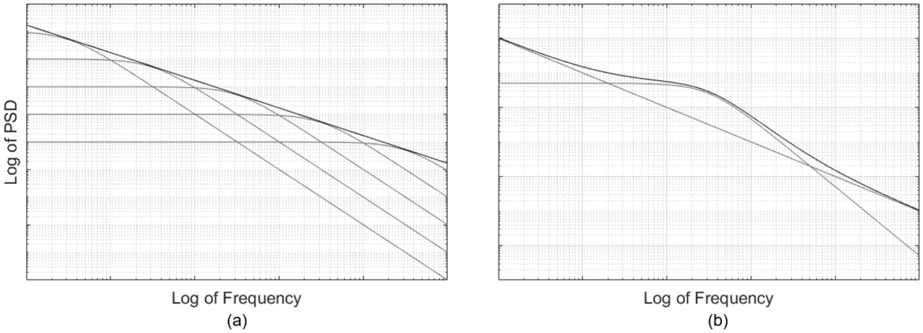


Figure 2.7: (a) WcWhorter model: Multiple random telegraph noise spectra with statistically distributed time constants some up to a $1/f$-spectrum. (b) A single random telegraph signal added to a background $1/f$-spectrum.

Hooge [51,52] acknowledges that a large part of the $1/f$-noise of MOSFETs can be explained by McWhorter's theory but points out that it is only applicable to situations, where surface effects play a major role. Since flicker noise is, however, observed also in bulk conduction (e.g. in resistors), a more general empirical model is introduced. Here, the conductivity fluctuations are experimentally related to mobility fluctuations rather than the number of charge carriers; however, the respective physical origin remains unclear.

In 1990 Hung et al. [53] developed a flicker noise model assuming that oxide traps modulate both carrier number and carrier mobility in a correlated manner (often termed "unified" model). As the source of the latter, changes in the scattering rate due to trapped charges are stated. A semi-empirical fitting function in dependence of the carrier density is used to describe an equivalent oxide trap density, as if all noise arose from carrier number fluctuation. The resulting analytical expressions are valid in all operating regions and can be fitted to transistors of different technologies. Therefore, many transistor compact models are still today based on this approach.

Ghibaudo et al. [54] rephrase the idea of correlated carrier number and mobility fluctuations and give a more general (but less practically applicable) expression. Here all physics related to the trapping mechanism is subsumed in fluctuations of the flat band voltage v_{fb}:

$$S_i = (g_m + \alpha \mu_{eff} C_{ox} i_d)^2 S_{v_{fb}}, \tag{2.12}$$

where α is a proportionality factor relating changes in the trapped charge to changes the effective mobility μ_{eff}.

In many experimental papers different transistor geometries and the influence of various processing steps are investigated. From TSMC's $0.13\,\mu\mathrm{m}$ planar bulk CMOS [55], to research level FD-SOI [56] and bulk FinFET [15,57] the correlated model is shown to best fit the measurement results. However, in some cases deviations are observed, as additional generation-recombination noise in FinFETs of varying channel/well architectures [15, 58] or a reduced flicker noise slope in FinFETs with Hf-based high-k gate stacks, which is attributed to a nonuniform trap distribution [59]. A common conclusion is the correlation between flicker noise and the surface roughness of the gate oxide, a connection confirmed by the observed reduction in noise after the inclusion of a hydrogen annealing processing step [60]. Due to this fact, $1/f$-noise can be used as a diagnostic tool to asses device reliability, where increased noise indicates crystal defects or impurities [61]. The observation of single RTN signals with their characteristic frequency as a function of temperature even allows the identification of specific defects types [62].

The flicker noise variability between different equivalent devices of one chip is another topic of interest. The measured spot noise values are found to follow a log-normal distribution, where the variance $\sigma[ln(S_{i_d})]$ increases with decreasing device area [63–65]. The functional dependence $\sigma[ln(S_{i_d})](W, L)$, for example for inclusion in a compact model, is either captured with an empirical fitting function based on matching theory [63] or based on subdividing the transistor area into many small pieces with the assumption that each individual contribution, as well as the total sum follow a log-normal distribution [64]. A different fundamental approach is the use of Monte Carlo simulations, where the total number of traps, as well as their respective space and energy positions, are chosen randomly and summed according to Eq. 2.11 [63]. Using this method, the effect of different trap localization profiles in the oxide is investigated, showing a strong influence of trap locations on the noise PSD especially for small gate areas [16]. da Silva et al. [65] relate the Monte Carlo approach to the analytical function, resulting in

$$\sigma[ln(S_{i_d}(f))] = \sqrt{ln(1 + \frac{K}{WL})}, \tag{2.13}$$

where K is a bias-dependent parameter related to the trap density at the Fermi level, and the current due to single traps. Careful modeling of the bias-dependence of flicker noise variability is shown to be crucial for circuit simulation: To achieve a correct prediction of the output signal variability of an oscillator, the parameters of the flicker noise compact model need to be scaled independently [66].

With the advancement of technology to production level FinFETs, deviations from the commonly accepted carrier number fluctuation with correlated mobility model begin to arise. An unforeseen dependence of the normalized flicker noise on drain current in the weak inversion region is observed. The discrepancy is attributed to a nonuniform distribution of the traps in energy space and the compact model equations adjusted accordingly [67]. In ultra-scaled technology nodes ($16\,\mathrm{nm}$ and beyond), only few traps contribute to a single device, such that some devices exhibit dominant traps (as shown in [68]), leading to severe device-to-device variations. Due to this fact corner models overestimate the noise variance. Additionally, deviations in bias-dependence and unphysical non-integer extracted trap numbers according to the conventional model are observed. Since conventional models cannot capture the random discrete nature of RTN Liu et al. [69] propose a statistical Monte Carlo model, where the parameters of each trap are chosen randomly. The statistical moments of the probability distribution of trap amplitude, energy, and relaxation energy can be extracted from measurement results. Notably, in their approach the trapping/detrapping mechanism is not based on the commonly employed elastic tunneling model, which was found by Campbell et al. [70] to predict capture/emission times inconsistent with measurement. Rather inelastic multi-phonon nonradiative transition theory is used, where the transition time constant is independent of trap location. Wu et al. [71] employ a similar approach, where again the trap-related RTN is statistically modeled based on the inelastic tunneling physics. Here, however, two additional processes are assumed to produce a purely $1/f$-shaped noise: Mobility fluctuations due to channel scattering and access resistance. Both processes are modeled with empirical formulas (the former based on Hooge's formula), and differ in their response to varying transistor geometries and bias conditions. The contributions of the three noise sources are added, resulting in a spectrum as depicted in Fig. 2.7(b). The relative contributions of each of the three noise processes depend on the bias conditions but are roughly equal for high gate voltages. Furthermore, it is shown that coupling between nearby trap states due to Coulomb interaction may reduce trap-induced noise (an effect previously observed for nanowire transistors [72]).

Another interesting flicker noise phenomenon is its response to rapidly changing bias conditions: It has been observed that a transistor at a specific constant bias exhibits more flicker noise than when it is repeatedly cycled between on and off states. It is supposed that switching to accumulation interferes with the occupancy of single trap states, when for example a trap is forced to release a charge carrier [73]. The consequent decrease of the emission time constant leads to the observed flicker noise reduction [74].

2.2.3 Noise in Transistor Compact Models

To accurately simulate how noise affects circuit operation, transistor compact models must capture the presented physical noise mechanisms. Additionally to the equivalent R-C parasitic networks and large signal core models current or voltage noise sources are introduced between the respective terminals. In BSIM-CMG thermal noise, shot noise, and flicker noise are included in the model.

Thermal noise is described by Eq. 2.9a, which is adjusted to take into account not only channel resistance, but additionally external contact resistances. The mentioned increase due to short channel effects is modeled by scaling with a model parameter [75]. Induced gate noise is included in the model if the corresponding model option is set. In this case, the correlation between channel noise and induced gate noise can be adjusted by means of a model parameter [37].

Shot noise is modeled according to Eq. 2.10 in the gate leakage current to the source, drain and bulk terminals.

Flicker noise used to be modeled in a simple approach (up to the BSIM3 model), where noise is assumed to be proportional to drain current and a scaling parameter is used to fit the model to the measurement [76]. In BSIM-CMG the presented unified approach is used with the adjustments due to nonuniform trap energy distribution. Four model parameters are used to empirically fit the trap distribution [37]. However, due to the described discrepancies in ultra-scaled technology nodes, new statistical approaches might be needed in the future for the modeling of flicker noise and its variability.

2.2.4 RF Device Noise Description

To characterize the behavior of semiconductor devices and circuits at high signal frequencies, a macroscopic two-port description is typically used. Here, the electrical network is described by a set of four frequency-dependent parameters. These parameters take, for example, the form of an impedance matrix, describing the relation between the voltages and currents at the ports, or the form of an equivalent S-parameter matrix, where the parameters describe the relations between incident and reflected waves at the two ports.

The effects of noise in the two-port framework are typically stated by the noise factor F, describing the deterioration of the signal-to-noise ratio S/N between the ports due to noise added by the two-port:

$$F \equiv \frac{(S/N)_i}{(S/N)_o} = \frac{N_o}{GN_i}, \tag{2.14}$$

where G is the gain between the two ports. This noise factor is dependent not only on frequency and applied bias, but notably also on the input impedance seen by the two ports. In a full impedance-independent form, the net effect of all the internal noise processes described can be represented by two noise sources at an ideal noiseless two-port, for example by a voltage noise source u_n and a current noise source i_n at one of the ports (see Fig. 2.8). A possible correlation

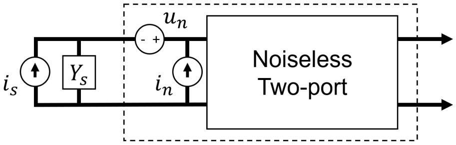


Figure 2.8: Equivalent description of a noisy two-port as a noiseless two-port with two external noise sources. Adopted from [8].

between the two noise sources needs to be considered and is captured by splitting the current source into an uncorrelated source i_u and a correlated source, where the latter is mathematically connected to the voltage noise via a complex correlation coefficient Y_c. Knowing the input impedance Y_s with its equivalent noise i_s at the input port the noise factor can be calculated as

$$F = \frac{\overline{i_u^2} + |Y_c + Y_s|^2 \overline{u_n^2}}{i_s^2} \tag{2.15}$$

For a specific optimum impedance Y_{opt}, the noise factor is minimized to F_{min}. Therefore, the noise factor can also be recast in terms of the optimum noise figure as

$$F = F_{min} + \frac{R_n}{\Re(Y_s)} \left| Y_s - Y_{opt} \right|^2, \tag{2.16}$$

where $R_n = \frac{\overline{u_n^2}}{4 k_B T \Delta f}$ is the equivalent resistance producing the thermal noise u_n, and describes therefore how fast the noise factor deteriorates due to deviations from the optimum impedance.

Notably, in both formulas always 4 parameters are needed for a complete two-port noise description [8].

2.2.5 Device Noise Measurement

Depending on the desired frequency range, different approaches are followed for the measurement of device noise. At low frequencies a flicker noise analyzer is used to record the drain current fluctuations of the DUT. At high frequencies thermal noise of the DUT's environment becomes significant, such that with RF noise measurements a different measurement technique must be employed.

2.2.5.1 Flicker Noise Measurement

The low-frequency noise of a DUT is typically measured by recording the current fluctuations in time domain and subsequently calculating the PSD. Fig. 2.9 displays a schematic measurement setup, where the terminals of the DUT are connected via two ground-signal-ground pads to external equipment. Two voltage sources with integrated ampere meter (source measurement unit (SMU)) set the gate and drain bias voltages at which flicker noise is measured. A low-pass filter is introduced between the SMU and the DUT to filter out unwanted noise from the voltage supply. With this setup the DC (output and transfer) characteristics of the device can be obtained. Fluctuations in the DUT's current will be visible as fluctuations of the voltage drop

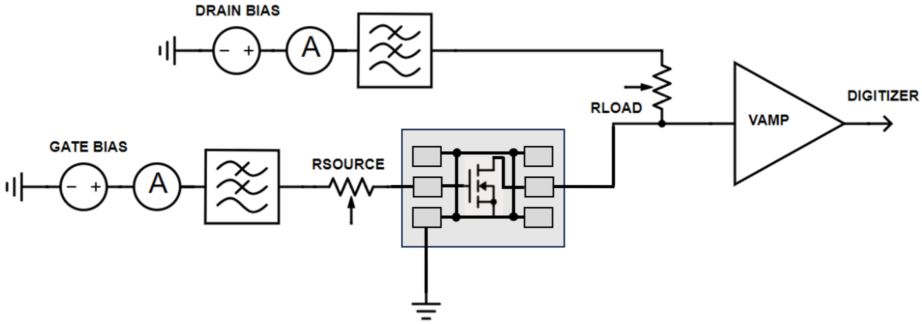


Figure 2.9: Block diagram of a flicker noise measurement system. Adapted from [77].

at the load resistor, which are then amplified with a voltage amplifier (VAMP), digitized and recorded. Depending on the drain current of the device at the chosen bias condition, a suitable load resistor (RLOAD) can be selected to achieve maximum sensitivity without overloading the voltage amplifier. From this time-domain measurement the voltage fluctuations spectrum at the load resistor $S_{vd}(f)$ can be obtained via an fast Fourier transform (FFT). From this the DUT's current noise spectrum $S_{id}(f)$ can be calculated: First, the theoretical thermal voltage noise of the load resistor and VAMP input impedance (R_{VAMP}) are subtracted from the measured voltage fluctuation spectrum. The current noise spectrum is then obtained by scaling the voltage noise spectrum with the equivalent resistance seen at the measurement node (RLOAD, VAMP input impedance and channel resistance r_{ds}):

$$S_{id}(f) = \frac{S_{vd}(f) - 4k_B T \frac{1}{1/R_{load}+1/R_{VAMP}}}{\frac{1}{1/R_{load}+1/R_{VAMP}+1/r_{ds}}}. \tag{2.17}$$

Typically, this process is repeated multiple times, so that the obtained spectra can be averaged and the variance of the spectral estimate reduced. The recorded time frame and the sampling frequency act as fundamental lower and upper limits of the PSD frequency range, respectively. Further distortions are caused by parasitic low-pass filtering of the load resistor and parasitic port capacitances/resistances (roll-off), and noise from the voltage amplifier and SMUs. If these characteristics are known, the measurement can be corrected or distorted frequency ranges excluded.

For all flicker noise measurements in this thesis the *Keysight E4727A Advanced Low-Frequency Noise Analyzer* was used with a frequency range from 0.03 Hz to 40 MHz.

2.2.5.2 RF Noise Measurement

Higher frequency noise components are typically measured in the two-port description of the noise figure with a network analyzer. This framework is used, since in contrast to flicker noise amplified contributions by the input port termination cannot be viewed as insignificant. To separate DUT noise contributions, two different methods might be employed: In the Y-factor method two different noise powers are applied at the input terminal (typically a room temperature $50\,\Omega$ termination and a reverse biased avalanche diode as a noise source). From the difference of the measured output powers, the contribution of the DUT can be calculated. The cold-source method on the other hand relies on only one noise measurement with room temperature 50 termination. Here, the gain of the DUT needs to be known (typically from S-parameter measurements), such that the input noise contributions can be subtracted from the measured output noise.

The noise power measurement itself is in principle similar to flicker noise measurements, yet with two conceptual differences that need to be noted: First, due to the higher frequency of the measured noise components, the signal is first downconverted with a local oscillator before digitization, entailing the need of additional filters to remove third-harmonic mixing products. And second, due to the small noise levels involved at the high frequency end of the DUT's noise spectrum amplification with a low-noise amplifier might be needed, making additional calibration steps necessary to remove excess noise from the instrument's noise receivers.

As described in Section 2.2.4 the measurement with a $50\,\Omega$ termination does not describe the noise behavior of DUT under all input impedance conditions. To mitigate this limitation, an impedance tuner can be added at the input port of the DUT to conduct noise figure measurements at different input impedance conditions. From these results, the full 4-parameter noise description of the DUT can be calculated.

Chapter 3

Phase Fluctuations in Oscillatory Systems

In this chapter, first the oscillator topologies employed in this thesis are described. Nonidealities, such as the device noise described in the previous chapter, lead to shifts of the oscillation's phase. After a description of how to quantify this phase noise, an overview of the mathematical approaches employed to relate phase noise to the underlying device noise is given. The chapter concludes with considerations about phase noise simulations.

3.1 Electronic Oscillators

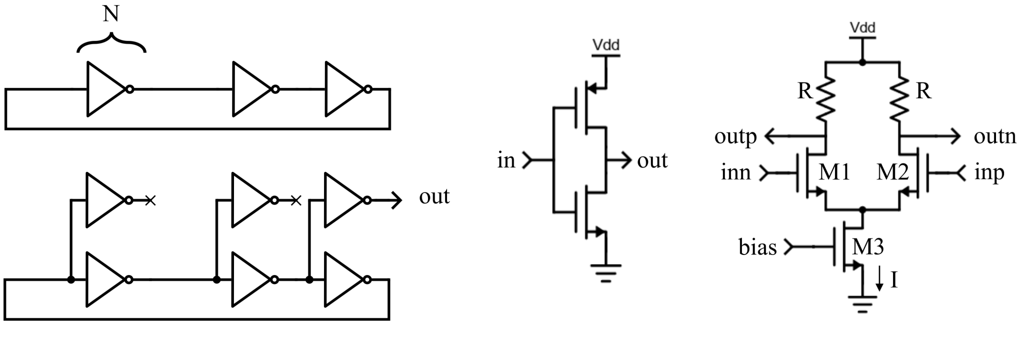
In electronics oscillators are a fundamental building block found in "just about everything" [78]: Heating food in a microwave oven, producing the sound waves coming from the radio, or keeping the time in an alarm clock may be rather basic tasks, but all require oscillators to serve as some form of time reference or to interact with the external world. Advanced applications alike use oscillatory circuits, whether it is to synchronize the execution of logic in a microprocessor or to transmit and receive radio signals (i.e. electromagnetic oscillations) to transmit data or detect objects with radar. Even in emerging applications like quantum computing, oscillators play a major role.

There are many ways to categorize electronic oscillators, one of which is to split them into harmonic oscillators, producing a sinusoidal output, and relaxation oscillators, producing a nonsinusoidal output [79]. Harmonic oscillators include among others crystal oscillators, RC oscillators and LC oscillators. In the latter case, the frequency of oscillation is determined by the resonance between a capacitor and an inductor, constituting a crucial component in high-frequency circuits. Depending on how dissipated energy is restored, different types of LC oscillators exist (Colpitts oscillator, Hartley oscillator, etc.). Relaxation oscillators, on the other hand, rely on nonlinear devices connected in a feedback loop. A common example is the ring oscillator, where an uneven number of inverters is connected in a ring. The type of oscillator used depends on the application and its specific requirements: While ring oscillators consume only a small area, are power efficient, and exhibit a wide tuning range, their noise performance is rather inferior [80]. LC oscillators perform better in that regard, but have the drawback of higher area consumption due to the coil. Quartz oscillators exhibit an even more stable oscillation, are, however, confined to a frequency range between 10 MHz and 100 MHz [81], and cannot be easily integrated monolithically in the CMOS process.

In the following, the two implementations of the LC and ring oscillator extensively used in this work will be examined in more detail.

3.1.1 Differential Ring Oscillator

Due to the aforementioned advantages, ring oscillators are used in various applications, including analog and digitally controlled oscillators, clock generators of digital circuits, ADCs and many more [82–84].



(a) (b) (c)

Figure 3.1: (a) General schematic of a ring oscillator without and with fan-out using (b) a single-ended and (c) a differential inverter architectures.

While more complex structures are possible (e.g. with feed forward coupling [85]), the basic ring oscillator architecture consists of a chain of inverters, which are connected in a ring-wise manner (see top of Fig. 3.1(a)): If the input of the first inverter is high, it will drive its output and therefore the input of the next inverter low. After an uneven number of stages, the output of the last inverter will be low, which is now fed back to the input of the first inverter. This information in turn will again propagate through the inverter chain. While for an even number of stages the circuit would latch up, no stable state exists for an uneven number and the circuit oscillates with a frequency f that depends on the total number of inverters N (with $N \geq 3$) and the propagation delay of a single stage t_{delay}:

$$f = \frac{1}{2Nt_{delay}} \tag{3.1}$$

The single inverter stages can be implemented in many ways. Fig. 3.1(b) shows a single-ended inverter consisting of an NMOS and a PMOS transistor. Due to its simplicity (only digital standard cells and no passive devices are needed), this implementation is often used as a characterization tool in digital circuits. The oscillation of such a single-ended ring oscillator is, however, very sensitive toward noise in the supply net, a fact that is unfavorable if the ring oscillator is used to characterize intrinsic device noise. Therefore, the more robust differential inverter architecture [86] will be used for the experiments conducted in this work. Another advantage of this structure is that only one type of transistor (here NMOS) is required. The basic architecture of a differential inverter cell is shown in Fig. 3.1(c). Due to its differential nature, it is possible to use also an even number of stages in the ring oscillator, if for one stage the differential input signals are reversed. Many different variations can be used for different performance optimizations [87], such as the use of an additional replica biasing in the delay cell to achieve a constant oscillation amplitude in the frequency tuning range [88].

The working principle of the basic differential delay cell can be understood in a simplified qualitative analysis, where the transistor M3 is viewed as an ideal current source with a current I: If one of the input voltages is much higher than the other (e.g. $v_{inp} \gg v_{inn}$) most of the current drawn by the current source will flow through the corresponding branch (here: right branch), leading to a voltage drop at the resistor and an output voltage of $v_{outn} = v_{dd} - IR$ and $v_{outp} = v_{dd}$. Due to the symmetry of the circuit, an inverse input leads to an inverse output, showing the inverting effect of the circuit. Furthermore, it can be easily determined that for an equal input ($v_{inp} = v_{inn}$) the current will split equally between both branches, such that the output voltages are equal: $v_{outp} = v_{outn} = v_{dd} - IR/2$. Since the output voltage of the delay cell is confined in the interval $[v_{dd} - IR, v_{dd}]$ the oscillation amplitude v_{op} of a corresponding ring oscillator is limited to IR (provided the single stages switch fully) [89].

When implementing this circuit, several sizing constraints derived by a quantitative analysis need to be respected to ensure the correct functioning of the inverter:

- The transistor M3 needs to be kept in saturation to act as a current source. Therefore, its drain voltage must always be larger than $v_{bias} - v_{th}$, which can be achieved either by using a suitable transistor geometry W_{M3}/L_{M3} for a given current (and therefore a suitable v_{bias}) or adjusting the supply voltage v_{dd}.
- To enable fast stage switching, the differential pair transistors should also be kept in saturation: $v_{gs,M1/M2} - v_{th,M1/M2} < v_{ds,M1/M2}$. At the most critical point for this condition, one transistor of the differential pair is switched on fully by the previous stage ($v_g = v_{dd}$), such that $v_d = v_{dd} - IR$, leading to a sizing constraint of the current and resistor (and therefore the oscillation amplitude v_{op}) of $v_{op} = IR \lesssim v_{th,M1/M2}$.
- When operating the delay cell as part of a ring oscillator, it is essential to ensure that the output voltage difference of one stage suffices to fully switch the next stage: $IR \geq \sqrt{2I/(\mu_n C_{ox}(W_{M1/M2}/L_{M1/M2}))}$ [90]. For a given transistor geometry, this again imposes a constraint for the current and resistor.
- The switching delay of a differential cell t_d can be approximated by the time constant of charging the input capacitance C_i of the following stage: $t_d \approx \frac{v_{op}C_i}{I} \approx RC_i$ [91]. Therefore, the oscillation frequency can be set by adjusting either the number of stages N, the resistance R, or input capacitance C_i (e.g. by explicitly adding capacitors between the inverter input nodes and ground). However, it should be noted that changes in each of these variables have additional effects on the oscillation waveform. A change in current I on the other hand (e.g. by changing the input bias v_{bias}), does in a first-order approximation not change the oscillation frequency, since the larger available charging current needs to charge the capacitors to a larger voltage, due to the increased oscillation amplitude v_{op}.
- To tap the oscillator signal without disturbing its operation, a common technique is to connect the output of each inverter stage not only to the next stage's input, but also to a second "fan-out" inverter stage (see bottom of Fig. 3.1(a)). The output of one of these inverters can then be forwarded to the following circuitry, and the operation of the ring oscillator is not disturbed since all stages are loaded symmetrically. Due to the doubled load capacitance, a slowdown of a factor of two has to be taken into account.

3.1.2 Cross-coupled Differential LC Oscillator

In an ideal parallel LC tank (see Fig. 3.2(a)) the energy of the system is periodically transferred from the electric field of the capacitor with capacitance C to the magnetic field of the inductor with inductance L and vice versa. While this transfer happens at the resonant frequency of $f = \frac{1}{2\pi\sqrt{LC}}$, the total energy stays constant over time, since there are no dissipative elements. Because real implementations always contain parasitic resistances, a mechanism is necessary to restore dissipated energy. One way this can be achieved is with a cross-coupled differential transistor pair, as depicted in Fig. 3.2(b), which acts as a negative resistance [92]. In high-frequency circuits this NMOS-only implementation is often preferred over its complementary counterpart containing an additional PMOS differential pair at the supply node. While the NMOS-only topology is easier to implement, it will be shown later that the inclusion of PMOS transistors can improve the oscillator's noise properties. Furthermore, the structure is preferred over the Colpitts oscillator due to its differential nature and, therefore, the concomitant supply and substrate noise rejection [93].

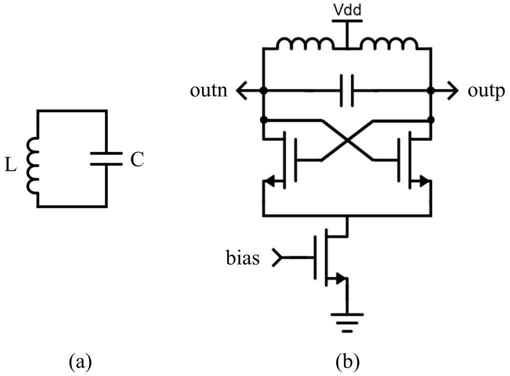


Figure 3.2: Schematic of (a) an ideal parallel LC tank circuit and (b) of a differential cross-coupled LC oscillator.

Depending on the current supplied by the tail transistor, the circuit operates in one of two operating regimes: For a lower supplied current, the oscillation amplitude is determined only by the equivalent parallel resistance of the circuit and the tail current (current-limited regime). For higher currents, the differential pair and the tail transistor will begin to operate in triode operation, effectively clipping the oscillation at ground potential (voltage-limited regime) [94]. For ease of implementation in the latter case, the tail current transistor may be replaced by a resistor.

3.2 Phase Fluctuations

In an idealized noiseless view the described electronic oscillators produce a 2π-periodic output signal voltage $v(t)$, which can be expressed as a Fourier series

$$v(t) = V_0 \sum_{n=0}^{\infty} \rho_n sin(n\omega_0 t + \theta_n), \tag{3.2}$$

where ω_0 and V_0 are nominal frequency and amplitude, respectively, and ρ_n and θ_n are the Fourier series coefficients. The voltage spectrum of this signal therefore consists of multiple weighted delta peaks at the fundamental frequency and its integer multiples (see black peaks in Fig. 3.3).

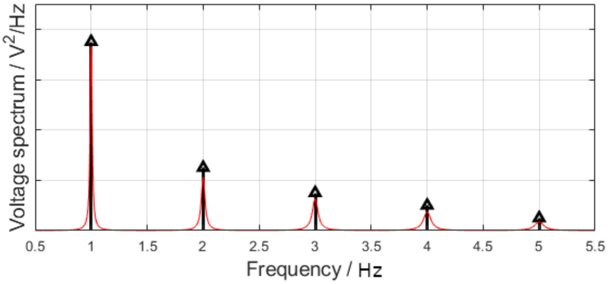


Figure 3.3: Voltage spectrum of an oscillator (black) without and (red) with phase noise.

In reality, however, the individual components constituting the oscillator circuit are subject to the electronic noise mechanisms described in Section 2.2. These random noise sources, as well as internal and external deterministic disturbances, cause deviations of the oscillators' phase and amplitude from their ideal values, that is a phase error $\phi(t)$ and an amplitude error $\epsilon(t)$ [95]:

$$v(t) = \big(V_0 + \epsilon\,(t)\big) \sum_{n=0}^{\infty} \rho_n sin\big(n\omega_0 t + \theta_n + n\phi\,(t)\big), \tag{3.3}$$

with the assumption that $|\epsilon(t)| < V_0$ and $\omega_0 t + \phi(t)$ is monotonically increasing. The corresponding voltage spectrum shows a broadening of the delta peaks (see red spectrum in Fig. 3.3). For a measured waveform $v(t)$ the phase function is uniquely defined at the zero-crossings t_n as $\phi(t_n) = \pi n - \omega_0 t_n$, providing a clear distinction from amplitude noise. However, at all other instances the effects of phase and amplitude noise cannot be separated, since an infinite combination of $\epsilon(t)$ and $\phi(t)$ result in the same voltage function.

In most applications, amplitude noise can be neglected, as it has no influence on circuit operation. In mixers for example, nonlinear effects cause a clipping of the output signal such that amplitude noise in the input is not transferred. In many other oscillator applications like clocks, ADCs, frequency dividers, etc. only the position of the rising edge (dependent on phase fluctuations, but not amplitude fluctuations) is relevant [95]. Independent of application, amplitude noise is furthermore suppressed by feedback paths of the oscillator, whereas phase fluctuations persist. As discussed in Section 1.1.2 phase noise can have implications on circuit operation and therefore merits careful characterization.

3.2.1 Description of Phase Noise

Different approaches to quantify phase noise exist: In frequency domain as a *PN spectrum*, in time domain as *jitter* or as the *Allan variance*. This section relies in many parts on the overview by Galton et al. [95].

3.2.1.1 Phase Noise Spectrum

From the phase deviation $\phi(t)$ the two-sided PSD can be calculated as

$$S_{\phi\phi}(f) = \lim_{T\to\infty} \frac{1}{T} |\mathcal{F}[\phi_T(t)]|^2, \tag{3.4}$$

where $\phi_T(t)$ is a windowed phase deviation function of length T (0 outside the window) and has the units $radians^2$ per Hz. Since the PSD is symmetric around zero, a one-sided PSD $S_\phi(f)$ can be defined for $0 < f < \infty$ as $S_\phi(f) = 2S_{\phi\phi}(f)$. This normalization by a factor of 2 ensures that the total integrated power is conserved.

The PN spectrum $\mathcal{L}(f)$, as measured by laboratory phase noise measurement instruments, is defined by IEEE [96] as

$$\mathcal{L}(f) = \frac{1}{2} S_\phi(f). \tag{3.5}$$

It is typically expressed in decibels $10\log_{10}(\mathcal{L}(f))$, with its units, due to the historic reasons described below, defined to be dBc/Hz. The phase noise value at a specific frequency is termed spot noise. Furthermore, single-tone deterministic components of phase noise show up as delta peaks in the spectrum and are referred to as spurious tones or spurs.

The shape of the typical PN spectrum was first described by Leeson [97] and is shown in Fig. 3.4. It consists of a region with $1/f^2$-dependence (i.e. $20\,\mathrm{dB}$ per decade slope), which falls off toward high-frequency components (far-off PN) until settling to a constant noise floor. Additionally, for

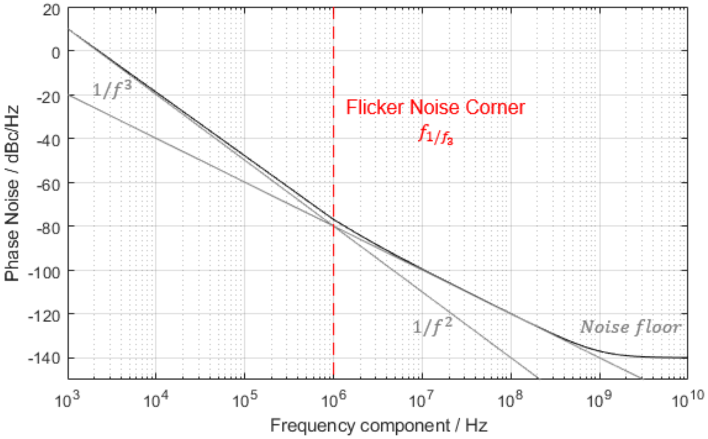


Figure 3.4: Typical shape of a phase noise spectrum as described by the Leeson equation. The values are based on the phase noise simulation of a ring oscillator in an advanced FinFET technology node.

close-in PN below an oscillator-specific corner frequency f_{1/f^3} a $1/f^3$-dependence (i.e. $30\,\mathrm{dB}$ per decade slope) is observed. The mechanisms leading to this shape will be discussed in Section 3.2.2.

Historically, phase noise was viewed as the fraction of the total signal power at a frequency offset Δf from the signal frequency ω_0:

$$\mathcal{L}_{old}(\Delta f) = \frac{S_v(\frac{\omega_0}{2\pi} + \Delta f)}{\int S_v df}. \tag{3.6}$$

Although the voltage spectrum contains effects both due to amplitude and to phase noise, it has the advantage that $S_v(f)$ can be easily measured with a spectrum analyzer (see Section 3.2.6). It can be shown that the old and new definition are equivalent under the condition $|\phi(t)| \ll 1$. However, in many practical cases the small signal approximation cannot be employed, especially when low offset frequencies (close-in PN) are considered. In this case S_v is an unsuitable measure for phase fluctuations, leading to the 2011 redefinition.

Common misconceptions due to the redefinition should be addressed: First, in the new definition values above 1 are not unphysical, since here phase noise is not a fraction of the total signal power. Even more than that: Since $\phi(t)$ does not correspond to a physical power, it is possible for $\mathcal{L}(f)$ to approach infinity, while the old definition flattens toward close-in PN in shape of a Lorentzian [8]. Further confusion arises from the meaning of the frequency variable in both old and new phase noise definitions. While previously the frequency offset from the carrier Δf was the relevant measure, in the current definition f refers to the Fourier frequency component of the underlying phase function (i.e. it does not relate to the signal frequency). However, often f and Δf are used interchangeably in both phase noise definitions.

3.2.1.2 Jitter

In a time-domain view, phase fluctuations are observed as shifts of oscillation edges, an effect called jitter. Different definitions of jitter exist depending on the reference used. The most common is the time-interval-error (TIE) jitter τ_n (see top of Fig. 3.5), quantifying the deviation of the signal's zero-crossings t_n from their ideal position:

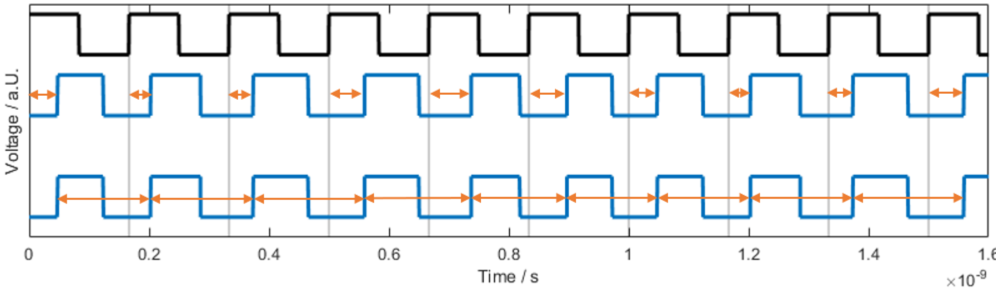


Figure 3.5: Oscillation with (blue) and without (black) phase fluctuations. Depending on the reference, the time-interval-error jitter (top) and the cycle-to-cycle jitter (bottom) can be defined.

$$t_n = n/f_0 + \tau_n^{TIE}, \text{ where } \tau_n^{TIE} = \frac{\phi(t_n)}{2\pi f_0}. \tag{3.7}$$

Therefore, the PSD of the TIE jitter function can be related to the phase fluctuation spectrum as

$$S_\tau^{TIE}(f) = \frac{1}{4\pi^2 f_0^2} S_\phi(f). \tag{3.8}$$

The jitter spectrum has the advantage that it is, for given timing variations, independent of the oscillator's nominal frequency. This is in contrast to the PN spectrum, where timing errors are represented as a fraction of the oscillation period, such that normalization is needed for a fair comparison between oscillators of different frequencies.

Often, the mean squared value of the jitter σ^2 (that is, the average of $(\tau^{TIE})^2$) is used as a figure of merit, called integrated jitter. It can be shown that its relation to the jitter spectrum is

$$\sigma^2 = \int_0^\infty S_\tau(f)\, df. \tag{3.9}$$

Since the jitter spectrum is unbounded for close-in PN, the result approaches infinity for a lower integration limit of zero. In practice, this limit is replaced by more relevant integration limits, since frequencies close to zero (and therefore observation times close to infinite) are typically not of interest in application. This measure can also be calculated from the probability distribution of τ^{TIE}, which can be estimated by plotting a histogram of a TIE jitter sequence.

A different type of jitter is the cycle-to-cycle (ctc) jitter (see bottom of Fig. 3.5, also called period jitter). Here, the zero-crossings are not compared to their ideal position, but rather to the respective previous zero-crossing:

$$\tau_n^{ctc} = t_{n+1} - t_n = 1/f_0 + \tau_{n+1}^{TIE} - \tau_n^{TIE}. \tag{3.10}$$

A more general version is the accumulated (or N-cycle) jitter, where the comparison is between oscillation edges spaced N cycles apart:

$$\tau_n^{\text{N-cycle}} = t_{n+N} - t_n = N/f_0 + \tau_{n+N}^{TIE} - \tau_n^{TIE}. \tag{3.11}$$

Here, other than in TIE jitter, effects of low-frequency phase variations do not accumulate over multiple periods. Mathematically, taking the first-difference corresponds to the application of a high-pass filter on the phase modulation function [98]. This is reflected in the scaling relation between the jitter and PN spectrum by a dependence on the frequency component f [86]:

$$S_\tau^{ctc}(f) = \frac{\sin^2(\pi N f/f_0)}{\pi^2 f_0^2} S_\phi(f). \tag{3.12}$$

A simplification employed by the preceding considerations should be mentioned: In practical oscillators the output waveform might be shifted with respect to ground by a baseband noise term additive to Eq. 3.3 (e.g. due to periodic deterministic effects of the output drivers). If the oscillation slew-rate is finite this leads to a change in the waveform's zero-crossing times, an effect which must be taken into account when determining jitter from time-domain waveform measurements.

3.2.1.3 Allan Variance

For completeness a further phase stability measure, the Allan variance is discussed. It focuses on the characterization of long-term (days to years) oscillator stability, and is therefore less used for RF oscillators, but rather for quartz oscillators or atomic clocks [99]. Here, not the phase, but the frequency is regarded as undergoing random modulations, defining an instantaneous normalized frequency:

$$y(t) = \frac{d\phi(t)}{dt} / \omega_0. \tag{3.13}$$

The Allan variance is then defined as the variance of the difference between two adjacent averages of the normalized instantaneous frequency with duration τ:

$$\sigma_y^2(\tau) = \frac{1}{2} E\left[(\overline{y}_1 - \overline{y}_2)^2\right] \tag{3.14}$$

3.2.2 Phase Noise Theory I: Traditional Approaches

Many approaches have been employed to calculate the phase noise or jitter from the noise contribution of single devices. These include the traditional frequency and time-domain techniques (this section), which are often tailored to a specific oscillator topology. General theories can be found in the impulse sensitivity function of Hajimiri et al. (see Section 3.2.3) and Demir's Floquet ansatz (see Section 3.2.4).

3.2.2.1 Frequency Domain

An intuitive understanding of the commonly observed PN spectrum shape can be obtained by considering an RLC tank as a band-pass filter applied to device noise: The impedance of an LC tank close to its resonance frequency ($\Delta\omega \ll \omega_0$) can be approximated as

$$Z(\omega_0 + \Delta\omega) \approx j \frac{\omega_0 L}{2 \frac{\Delta\omega}{\omega_0}} = j \frac{R\omega_0}{2Q\Delta\omega}, \tag{3.15}$$

where the quality factor is defined as $Q \equiv \frac{R}{\omega_0 L}$. Therefore, the tank suppresses thermal noise with a $1/f^2$-slope roll-off from the oscillation frequency:

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} |Z|^2 = 4kTR \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2. \tag{3.16}$$

The Leeson equation, qualitatively presented in Section 3.2.1.1, normalizes this output voltage to the signal power P_{sig} resulting in the full form of the single-sideband PN spectrum:

$$\mathcal{L}(f) = \frac{2Fk_BT}{P_{sig}} \left(1 + \left(\frac{f_0}{2Qf} \right)^2 \right) \left(1 + \frac{f_{1/f^3}}{f} \right). \tag{3.17}$$

Here, further effects are taken into account empirically: Additional noise sources (e.g. by active elements) raise the effective thermal noise (via noise figure F) and introduce flicker noise, leading to the $1/f^3$-slope for $f < f_{1/f^3}$. Furthermore, a noise floor is added due to the noise of devices outside the oscillator feedback path (e.g. buffers).

Notably, the derivation relies on the voltage spectrum rather than phase, with the assumption that the relevant frequency range is sufficiently far from the carrier. For other oscillator topologies, the qualitative shape of the Leeson equation holds, in spite of the different noise to phase noise conversion mechanisms.

A more general frequency-domain description, which is also applicable to ring oscillator was given by Razavi [100]. Here, it is shown that noise in a linear oscillatory system is shaped with a factor of

$$\frac{1}{(\Delta\omega)^2 \left|\frac{dH}{d\omega}\right|^2}, \tag{3.18}$$

where $H(j\omega)$ is the open-loop transfer function of the system and $\Delta\omega$ is the frequency offset from the closed-loop resonant frequency. A ring oscillator can be represented as a linear circuit consisting of a series of linear gain stages with RC parasitic elements, yielding an expression for the shaping of the power spectra of device noise. However, due to the strong simplification as a linearized system, nonlinear mixing and modulation effects (such as flicker noise upconversion) need to be treated separately.

3.2.2.2 Time Domain

For oscillators with switching elements, a time-domain analysis can be more intuitive. Here, the influence of noise on the switching time of the delay elements and therefore jitter is calculated. The obtained results are, however, always limited to a specific oscillator topology. Detailed examinations were carried out, for example, for versions of relaxation oscillators [101], differential bipolar ring oscillators [102] and CMOS ring oscillators with varying types of differential [86,103] and single-ended delay elements [86].

As an illustrative example, the approach is presented for a ring oscillator with single-ended delay cells (see Fig. 3.1(b)). When a rising edge reaches the input of such a delay element the NMOS transistor will be switched on fully and discharge the input capacitance of the following stage with the saturation current I_N. Assuming that the following stage switches at $V_{DD}/2$ and that the transistor stays in saturation the time delay t_{dN} can be related to the channel noise i_{nN} as

$$\int_0^{t_{dN}} \frac{I_N + i_{nN}}{C} dt = \frac{V_{DD}}{2}. \tag{3.19}$$

The single transition jitter spectrum $S_{t_{dN}}$ can be related to the noise spectrum $S_{i_{nN}}$

$$S_{t_{dN}} = \frac{t_{dN}^2}{I_N^2} \operatorname{sinc}^2(f t_{dN}) S_{i_{nN}}, \tag{3.20}$$

where the sinc-function results from the convolution with the rectangular noise integration window. This notably fits the expected $1/f^2$-shape PN spectrum, since the shift of a single transition corresponds to a form of ctc jitter. Similar considerations can be made for the falling oscillation edge and for the channel noise of the PMOS. Finally, the perturbations of the single edges are assumed to be uncorrelated and summed for all stages, yielding the PN spectrum due to device white noise.

For low-frequency perturbations (e.g. flicker noise) affecting the oscillation over many transitions, a different approach is needed, since the assumption of uncorrelated propagation delays is not fulfilled. Therefore, a sensitivity factor is introduced that relates changes in the respective current to changes in the oscillation frequency. The same technique can be used to investigate the effect of low-frequency supply and substrate voltage variations. It is used, for example, to investigate the effect on single-ended and differential ring oscillators, showing a higher resilience of the latter against these types of perturbations [104].

3.2.3 Phase Noise Theory II: Impulse Sensitivity

A first general theory of phase noise, applicable to all types of electronic oscillators and noise sources, was proposed by Lee and Hajimiri [105, 106]. Although some of its mathematical intricacies have later been shown to be incorrect, it pioneered the time-variant approach, successfully explaining several previously unaccounted-for phase noise phenomena and providing valuable circuit insight. Moreover, it serves as a basis for the more mathematically rigorous approach developed by Demir (see next section) and is therefore introduced hereinafter.

In a thought experiment, an infinitely short current pulse is introduced at a node of the oscillator circuit. The resulting phase shift is assumed to be proportional to the pulse current, an expectation that is shown in simulation to be valid for sufficiently small pulse magnitudes. While therefore the large-signal waveform may be governed by device nonlinearities, noise can be treated as small perturbations around a linearized steady-state solution. Furthermore, it is shown that the corresponding noise-to-phase transfer function depends on the current state of the oscillator. For instance, in Fig. 3.6 the response of an ideal parallel LC tank to an introduced current pulse is shown. The phase of the oscillation is very sensitive toward the current pulses at the oscillation's zero crossings, but insensitive at the maxima. The impulse sensitivity function (ISF) $\Gamma(t)$ is

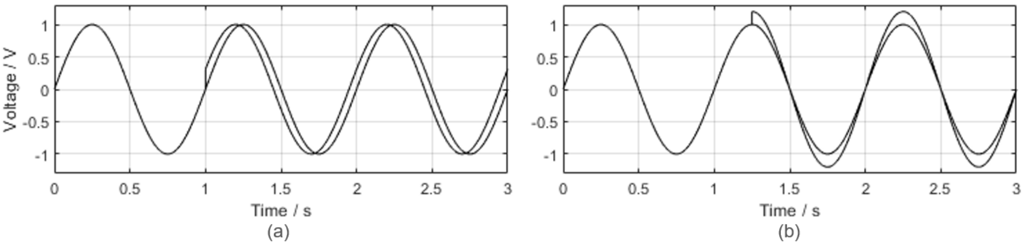


Figure 3.6: Response of an ideal parallel LC tank oscillation with a current pulse introduced at (a) the zero-crossing and (b) the oscillation maximum.

therefore defined to relate a unit current pulse at time τ to the corresponding phase change at time t

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}u(t-\tau), \tag{3.21}$$

where q_{max} is the maximum charge swing at the corresponding circuit noise, making the ISF independent of oscillation amplitude, and $u(t)$ is the unit step function. Exemplary ISFs of an ideal parallel LC tank and a ring oscillator are depicted in Fig. 3.7.

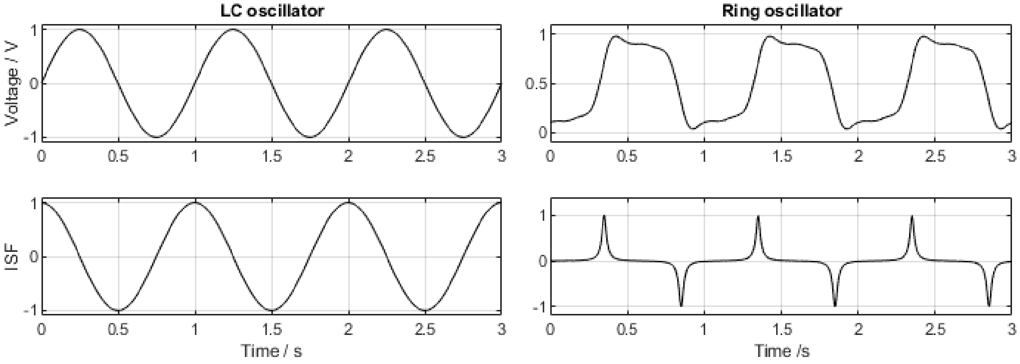


Figure 3.7: Oscillation waveform (top) and impulse sensitivity function (bottom) of an ideal parallel LC tank and a ring oscillator.

The phase response to an arbitrary noise function $i(t)$ is therefore given as the superposition integral

$$\phi(t) = \int_{-\infty}^{\infty} h_{\phi}(t,\tau)i(\tau)d\tau = \frac{1}{q_{max}}\int_{-\infty}^{t}\Gamma(\omega_0\tau)i(\tau)d\tau. \tag{3.22}$$

Since the ISF is periodic it can be expressed as a Fourier series yielding

$$\phi(t) = \frac{1}{q_{max}} \left[\frac{c_0}{2} \int_{-\infty}^{t} i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau) \cos(n\omega_0 \tau) d\tau \right], \tag{3.23}$$

where c_n are the Fourier coefficients.

For a sinusoidal noise current at a frequency close to an integer multiple m of the oscillation frequency $i(t) = I_n \cos((m\omega_0 + \Delta\omega)t)$, mainly the term $n = m$ of Eq. 3.23 contributes, leading to a sinusoidal phase fluctuation of

$$\phi(t) \approx \frac{I_m c_m \sin(\Delta\omega)}{2q_{max}\Delta\omega}, \tag{3.24}$$

and therefore to corresponding spurs in the PN spectrum $\mathcal{L}$ at the frequency $\Delta\omega$ with a power of

$$\mathcal{L}_{spur}(\Delta\omega) = 10 \log \left(\frac{I_n^2 c_n^2}{16 q_{max}^2 \Delta\omega^2} \right). \tag{3.25}$$

Noise near integer multiples of the oscillation frequency therefore gets downconverted to phase noise around DC weighted by the respective Fourier coefficient and falls off in power with the typical $1/\Delta\omega^2$-slope. This framework can now be extended to both white and flicker noise device sources. Here, multiple noise sources can be considered by superposition, which is valid due to the linearity of the system (taking into account possible correlations).

For a white noise source $\overline{i_n^2}/\Delta f$ all Fourier components will contribute, such that with Parseval's relation $\sum c_n = 2\Gamma_{rms}^2$ the PN spectrum is given as

$$\mathcal{L}_{white}(\Delta\omega) = 10 \log \left(\frac{\frac{\overline{i_n^2}}{\Delta f} \Gamma_{rms}^2}{2 q_{max}^2 \Delta\omega^2} \right), \tag{3.26}$$

where Γ_{rms} is the root mean square value of the ISF. Notably, in this phase noise expression in contrast to previous theories, no fitting parameters are used.

Flicker noise around dc of the form $\overline{i^2}_{n,1/f} = \overline{i_n^2} \frac{\omega_{1/f}}{\Delta\omega}$, where $\omega_{1/f}$ is the corner frequency where the device white and flicker noise are equal, contributes according to Eq. 3.23 weighted by the c_0 coefficient:

$$\mathcal{L}_{flicker}(\Delta\omega) = 10 \log \left(\frac{c_0^2}{q_{max}^2} \frac{\overline{i_n^2}/\Delta f}{8\Delta\omega^2} \frac{\omega_{1/f}}{\Delta\omega} \right). \tag{3.27}$$

Therefore, its intrinsic $1/\omega$ power spectrum is shaped to a $1/\Delta\omega^3$-slope for close-in PN[1]. The phase noise corner frequency $\Delta\omega_{1/f^3}$ between $\mathcal{L}_{white}$ and $\mathcal{L}_{flicker}$ was typically assumed to be equal to the device noise corner frequency $\omega_{1/f}$. However, within this framework it becomes apparent that the weighing factors (Fourier coefficients c_n) describing the frequency conversion need to be considered, resulting in a phase noise corner smaller than the device noise corner:

$$\Delta\omega_{1/f^3} = \omega_{1/f} \frac{c_0^2}{4\Gamma_{rms}^2}. \tag{3.28}$$

This equation is the basis for a key design insight of this theory: To reduce flicker noise upconversion, the c_0 (i.e. the dc value of the ISF) should be as small as possible. It is stated and experimentally validated that this can be achieved by symmetric rise and fall times of the waveform.

A further advantage of this approach is that the cyclostationary nature of the device noise sources can easily be incorporated into the framework. The power of many noise processes depends on the applied bias conditions (e.g. thermal channel noise of MOSFETs), such that the stochastic properties of the noise process vary periodically during the oscillation period. To include this effect, a periodic noise scaling function $\alpha(t)$ is introduced, which can be merged with $\Gamma(t)$ to define an effective ISF $\Gamma_{eff}(t) = \Gamma(t)\alpha(t)$ to be used in lieu of Γ in the preceding analysis.

As a practical example, the fact that a Colpitts LC oscillator exhibits lower phase noise than a typical ring oscillator can be attributed to the observed relation between the ISF and cyclostationary noise sources. In a Colpitts oscillator, energy is restored, and, therefore, device noise sources are active at the voltage maxima. In this state the oscillator's phase is insensitive toward noise, that is the absolute value of the ISF is low. In contrast, the stages of a ring oscillator are active during the oscillation edge, which corresponds to the maximum of the ISF.

For further design insight, the framework can be applied to specific oscillator topologies. In LC oscillators, for instance, the effect of various noise sources on the phase noise of a differential cross-coupled topology can be investigated [107]. Here, it is demonstrated that symmetry in the half-circuits should be achieved by proper device sizing. Also, for ring oscillators detailed calculations can be carried out using approximate ISF functions and transistor noise equations [108]. Approximate phase noise expressions can be derived as a function of stage number, power dissipation, and oscillation frequency for single-ended and differential delay cell topologies.

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[1] The standard terminology is to say flicker noise is *upconverted* to close-in PN. This comes from the fact that the low-frequency flicker noise at $\Delta\omega$ appears in the voltage spectrum S_v close to the carrier frequency at $\omega_0 + \Delta\omega$. However, since the phase noise redefinition S_ϕ is the relevant quantity, in which case flicker noise is not frequency shifted. Nonetheless, the terminology remained and it is common to speak of flicker noise upconversion.

For the remaining fundamental question, how the ISF can be calculated for a specific oscillator design, several approaches are presented. First, the ISF can be simulated in time domain by introducing a current pulse to a circuit node at a relative phase during the oscillation period and recording the phase response when the amplitude response is vanished. This is repeated with the pulse swept through the oscillation period to obtain the full ISF function. Additionally, a less computationally expensive approach in frequency domain was proposed for ISF simulation [109]. Second, a closed-form formula is derived for the ISF based on a state space representation of the investigated system. However, this approach was later shown by Demir [110] to lack general validity, as he presented the correct mathematical framework (see next section). For certain oscillator topologies, however, the results do not deviate significantly from accurate predictions. Third, an approximation based on the previous approach can be used (as, for example, in the investigations regarding the ring oscillator), which despite its unstable mathematical foundations, can still provide valuable circuit insights.

3.2.4 Phase Noise Theory III: Floquet

In this section, the Floquet theory for phase noise calculation is presented as introduced by Demir et al. [111–114]. The theory is general in the sense that it is applicable to all types of oscillators (electrical or otherwise) on the basis of their defining set of equations (see Section 3.2.4.1).

Similar to the ISF approach a periodic (vector) function is calculated to describe the sensitivity of the oscillation's phase toward noise, which is here, however, obtained by a rigorous mathematical derivation (see Section 3.2.4.2). Furthermore, the theory differs in how this function is used to obtain a PN spectrum (see Section 3.2.4.3). Subsequently, a comparison against the ISF approach is given in Section 3.2.4.4.

3.2.4.1 State Space Description

For the pursued mathematical analysis, a set of equations must be formed describing the investigated electrical circuit. Commonly applied approaches are the mesh analysis based on Kirchhoff's voltage law (the sum of all voltages around a mesh has to be zero) or nodal analysis based on Kirchhoff's current law (the sum of all current at a circuit node has to be zero). These techniques are, however, not well suited for an automated approach in circuit simulators. While for the former, nonplanar circuit topologies pose a challenge, for the latter voltage-defining devices, as voltage sources and inductors lead to complications, since their current is not a function of the applied voltages or their derivatives. This issue can be solved by using modified nodal analysis (MNA), where for each of these devices a separate state variable for the current is introduced with an additional equation to describe the corresponding circuit element.

The state of the electric circuit is therefore completely characterized by the voltages of the m circuit nodes and the current through the n voltage-defining circuit elements. These constitute in their entirety the system's state variables $\vec{x} = \{v_1, ..., v_m, i_1, ..., i_n\}$. Accordingly, the state of a system can be represented as a locus in a $m + n$-dimensional state space.

The dynamics of the system are given by the obtained set of equations, which in special cases (the general case is considered thereafter) can be transformed to the form of an ordinary differential equation (ODE)

$$\dot{\vec{x}} = \vec{f}(\vec{x}). \tag{3.29}$$

Fig. 3.8 shows the two-dimensional state space of three different circuits with the derivatives given by the stated ODE indicated as black arrows and orange streamlines. These examples are chosen to conceptually arrive at an example suitable for the Floquet framework: The first circuit (ideal LC) does oscillate, however, unlike real oscillators with an undefined nominal amplitude, such that amplitude noise is unphysically not decaying with time. Since adding parasitic resistance (second circuit) damps the oscillation, a nonlinear negative resistance with cubic current-voltage dependence is added (third circuit). This circuit will in the following be used as an illustrative example for the Floquet theory, since it is easily represented in 2D state space, but still exhibits a stable limit trajectory.

As stated above, the set of equations resulting from MNA cannot always be transformed to an ODE[2]. For example, if a resistor is added in series of the nonlinear negative resistance of the example circuit (see Fig. 3.9), none of the resulting equations contains the derivative of the v_2 voltage. The generally valid form is a differential algebraic equation (DAE)

$$\frac{d}{dt}\vec{q}(\vec{x}) + \vec{g}(\vec{x}) = 0. \tag{3.30}$$

In state-space the additional equations, not related to state variable derivatives, can be viewed as spanning a subspace of allowed state space loci in state space (see Fig. 3.9).

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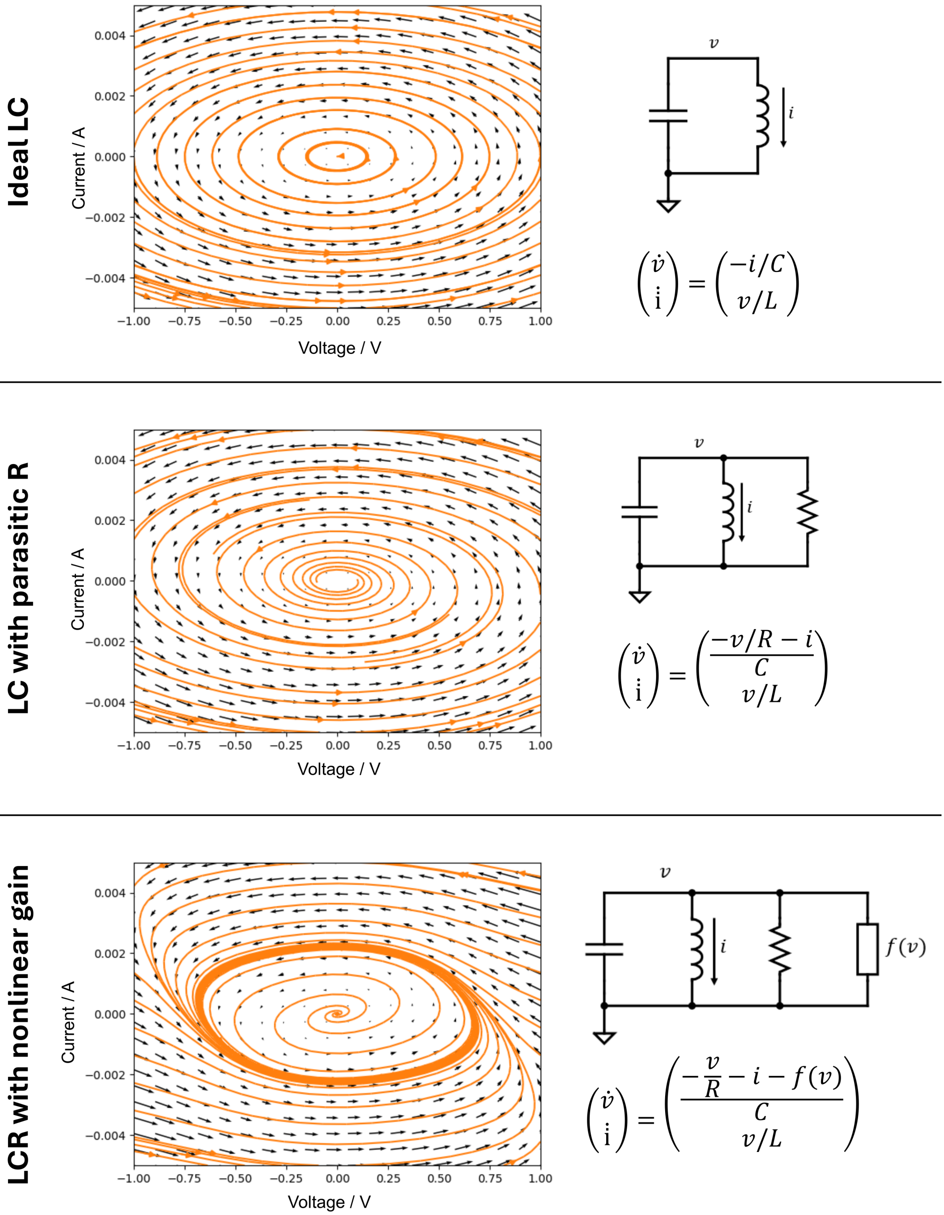
[2] It can be argued that actually any system can be represented by an ODE. One way is not to use redundant variables as obtained by the MNA approach, but rather transforming the state space to use a minimal set of unknowns. However, it is difficult to find this representation in an automated fashion, and state variables lose their physical significance. Another way is to regularize the DAE by including the effect of parasitic capacitances and inductances. Here, however, due to the small capacitances involved, numerical problems might arise [115]

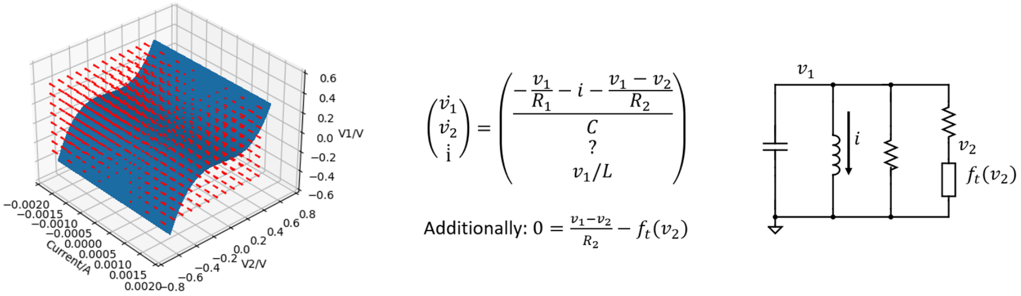


$$\begin{pmatrix}\dot{v}\\ \dot{\mathrm{i}}\end{pmatrix}=\begin{pmatrix}-i/C\\ v/L\end{pmatrix}$$

$$\begin{pmatrix}\dot{v}\\ \dot{\mathrm{i}}\end{pmatrix}=\begin{pmatrix}\frac{-v/R-i}{C}\\ v/L\end{pmatrix}$$

$$\begin{pmatrix}\dot{v}\\ \dot{\mathrm{i}}\end{pmatrix}=\begin{pmatrix}\frac{-\frac{v}{R}-i-f(v)}{C}\\ v/L\end{pmatrix}$$

Figure 3.8: State-space representation with corresponding the system of differential equations for three LC tank circuits. The derivatives of the state variables are represented as a black vector fields with orange streamlines. Shown are (top) an ideal LC oscillator, (middle) an LC oscillator with parasitic resistance, and (bottom) an LC oscillator with parasitic resistance and nonlinear negative resistance.



$$\begin{pmatrix} \dot{v_1} \\ \dot{v_2} \\ \dot{\mathrm{i}} \end{pmatrix} = \begin{pmatrix} \dfrac{-\dfrac{v_1}{R_1} - i - \dfrac{v_1 - v_2}{R_2}}{C} \\ ? \\ v_1/L \end{pmatrix}$$

Additionally: $0 = \frac{v_1 - v_2}{R_2} - f_t(v_2)$

Figure 3.9: State-space representation of a circuit described by a set of differential-algebraic equations (DAEs). The blue plane represents allowed loci according to the algebraic part of the differential algebraic equation. The derivatives are illustrated as red arrows and have no component along the v_2 dimension.

3.2.4.2 Calculation of Floquet Vector

As the next step, the system's response to perturbations is calculated. The derivation will be outlined for the case of ODEs, and the results later extended to DAEs. Dropping from here vector notation, the effect of p noise sources on a n-dimensional system can be described by

$$\dot{x} = f(x) + B(x)b(t), \tag{3.31}$$

where $b(t) : \mathbb{R} \to \mathbb{R}^p$ is a vector of stationary noise sources, which are mapped by the matrix $B(x) : \mathbb{R}^n \to \mathbb{R}^{n \times p}$ onto the corresponding equation. Furthermore, $B(x)$ scales the noise according to the state of the oscillator.

First, the response of the noiseless system responds to a singular, small perturbation is investigated, for example due to an infinitely short current pulse. This small deviation from the T-periodic unperturbed solution x_s is denoted with the error vector w, such that

$$\dot{x_s} + \dot{w} = f(x_s + w). \tag{3.32}$$

The state space can be linearized around unperturbed solution $x_s(t)$ with a first order Taylor series, resulting in

$$\dot{x_s} + \dot{w} = f(x_s) + \left.\frac{\partial f(x)}{\partial x}\right|_{x_s(t)} w + \mathcal{O}(w^2) \tag{3.33}$$

Subtracting the steady-state solution from both sides a differential equation for the evolution of w can be obtained:

$$\dot{w}(t) \approx A(t)w(t), \tag{3.34}$$

where $A(t)$ is the T-periodic Jacobian matrix.

For such a homogeneous linear system of differential equations, a matrix exists, called the state transition matrix $\phi(t, t_0)$, such that the solution to an initial condition $x_0 = x(t_0)$ can be written as $x(t) = \phi(t, t_0)x_0$. In case of a T-periodic coefficient matrix $A(t)$ it can be shown that the state transition matrix can be written in the form

$$\phi(t, s) = U(t)D(t - s)V(s), \tag{3.35}$$

where $D(t) = diag[exp(\mu_1 t), ..., exp(\mu_n t)]$ is a diagonal matrix with the Floquet exponents μ_i. $U(t)$ and $V(t)$ are T-periodic and satisfy $U(t) = V^{-1}(t)$. In more visually conceivable terms, the state space can be transformed to a different set of basis vectors, in which the derivatives of all components are mutually independent and evolve according to the exponential law with the respective Floquet exponent. If a stable nontrivial T-periodic solution exists for the investigated system of ODEs (Eq. 3.29), it can be shown that at least one of the Floquet exponents satisfies $exp(\mu_i T) = 1.0$, while all others decay exponentially, that is $|exp(\mu_i T)| < 1.0$. Without loss of generality, the stable Floquet vector can be defined as $\mu_1 = 0$, with the corresponding Floquet eigenvectors $u_1(t)$ and $v_1(t)$.

This basis change is shown for the example circuit in Figure 3.10. Here, the linearized state space around the stable trajectory is shown for a specific point in time. In Figure 3.10(a) this is represented in the original voltage/current basis (green vectors). Here, the derivatives (black arrows) are not constant in time, but perform a T-periodic oscillation. The Floquet vectors are calculated (blue vectors) and the state-space is represented in Figure 3.10(b) in the corresponding basis. Notably, here the derivatives are constant in time, and one dimension exists (here x-axis), where changes do not decay exponentially, corresponding to phase changes of the oscillation.

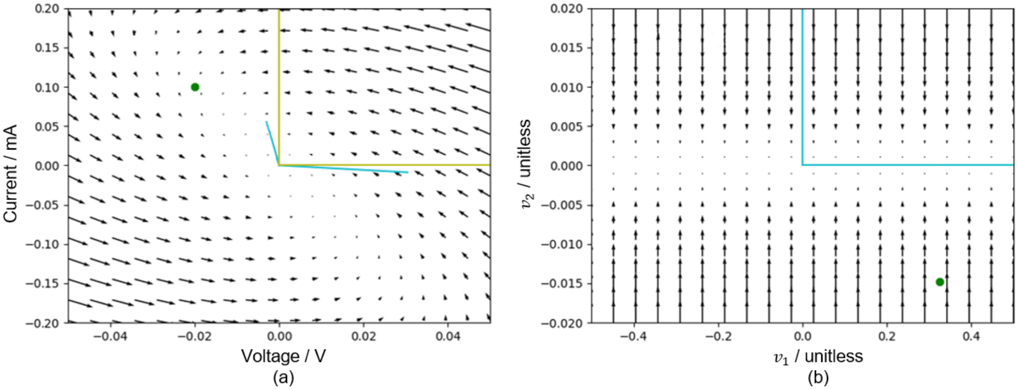


Figure 3.10: Linearized state space around the stable trajectory at one selected relative phase (a) in the original voltage/current basis and (b) in the transformed Floquet basis.

The original perturbation $B(x)b(t)$ from Eq. 3.31 can now be split into two parts: The first term $b_1(x,t)$ creates only phase deviation $\alpha(t)$ to the unperturbed solution, such that

$$x_s(t+\alpha(t)) \tag{3.36}$$

solves

$$\dot{x} = f(x) + b_1(x,t). \tag{3.37}$$

$\alpha(t)$ is related to the common phase description via $\phi(t) = 2\pi f_0 \alpha(t)$ and can grow unboundedly large. The second term $\tilde{b}(x,t)$ can be treated as a small perturbation to Eq. 3.36, and causes deviations from $x_s(t+\alpha(t))$ that decay exponentially with time and therefore remain small. The former term can be obtained by projecting the noise contribution onto direction of u_1:

$$b_1(x,t) = v_1^T(x, t+\alpha(t))B(x)b(t)u_1(t+\alpha(t)). \tag{3.38}$$

The resulting phase deviation $\alpha(t)$, which can be shown to solve Eq. 3.37, is hereby defined via its derivative

$$\frac{d\alpha(t)}{dt} = v_1^T(t+\alpha(t))B(x_s(t+\alpha(t)))b(t), \tag{3.39}$$

and the boundary condition $\alpha(0) = 0$. Therefore, the respective Floquet vector $v_1(t)$ again represents a type of oscillator phase sensitivity function to noise of the defining set of equations. Notably, this equation is nonlinear, since the arguments of the Floquet vector $v_1(t)$ and the noise matrix $B(x(t))$ are adjusted according to phase deviations due to previous perturbations. With this equation, the resulting phase deviation from a given realization of the noise vector $b(t)$ can be calculated.

An analogous derivation can be carried out for an n-dimensional set of DAEs. The linearization around the unperturbed solution (analog to Eq. 3.34) reads in this case

$$\frac{d}{dt}(C(t)x) + G(t)x = 0, \tag{3.40}$$

where $C(t)$ is a matrix with rank $m \leq n$. Here, $C(t)$ contains the coefficients of the derivative of the state variables, mainly due to capacitances, while $G(t)$ contains the coefficients of the state variables due to conductive effects.

The state transition matrix in this case is given as

$$\phi(t,s) = U(t)(D(t-s))V(s)C(s), \tag{3.41}$$

where D is a diagonal matrix with $D(t) = diag[exp(\mu_1(t)), ..., exp(\mu_m(t)), 0, ..., 0]$. In this case, only m entries in the state transition matrix contain the exponential dependence of the Floquet exponents, while the remaining $n - m$ diagonal entries corresponding to the kernel of the $C(t)$ matrix are zero. The further derivation, in particular Eq. 3.39 stays unchanged.

The implementation of the algorithm in this thesis to obtain $v_1(t)$ from a given electrical circuit is presented in Section 4.1.

3.2.4.3 Calculation of Phase Noise Spectrum

Typically, only statistical properties of the noise sources are known, instead of a concrete realization of the noise vector $b(t)$. Viewing Eq. 3.39 as a stochastic differential equation, statistical properties of the phase deviation $\alpha(t)$ can be derived from the power spectrum of the noise sources. It can be shown that the statistical phase deviations can be fully described by a properly determined average input from a noise source, encoded in a contribution factor c. How this noise source contribution is calculated depends on the correlation time of the noise source (and therefore on its spectrum), because different boundary conditions are relevant in the derivation.

In the system of equations (here exemplary for ODEs) it is therefore convenient to separate perturbations due to white and colored noise sources [112]:

$$\dot{x} = f(x) + B_w(x)b_w(t) + \sum_{m=1}^{M} B_{cm}(x)b_{cm}(t). \tag{3.42}$$

Here, all white noise sources remain in the noise vector $b_w(t)$. They are assumed to be Gaussian, normalized, and are again modulated via the state-dependent matrix $B_w(x)$. Colored noise sources, on the other hand, are now considered via the summation, where $B_{cm}(x)$ is a vector that modulates and relates the single noise source b_{cm} with the corresponding equation. The colored noise sources have spectra S_{cm}, which are assumed to describe a processes with correlation times much longer than the oscillation period.

For all white noise sources their aggregated contribution can now be calculated as

$$c^{white} = \left(\frac{1}{T} \int_0^T v_1^T(\tau) B(x_s(\tau)) B^T(x_s(\tau)) v_1(\tau) d\tau \right)^{1/2}. \tag{3.43}$$

For each colored noise source the result is:

$$c_m^{colored} = \frac{1}{T}\int_0^T v_1(\tau)B_{cm}(x_s(\tau))d\tau\,. \tag{3.44}$$

From the sum of white noise and colored noise source contributions the PN spectrum can be calculated as [116]

$$\mathcal{L}(f) = \frac{1}{2T^2f^2}\left((c^{white})^2 \cdot 1\,\frac{\mathrm{V}^2}{\mathrm{Hz}} + \sum_m (c_m^{colored})^2 \cdot S_{cm}(f)\right). \tag{3.45}$$

3.2.4.4 Comparison with Impulse Sensitivity

The Floquet and the ISF approach coincide in their ansatz to define a small signal phase response toward perturbations. While in the former the product $v_1(t)B(x)$ describes the oscillator's phase sensitivity and modulation, $\Gamma_{eff}(t) = \Gamma(t)\alpha(t)$ takes on the same role in the ISF approach.

One difference between the theories is the calculation of the sensitivity function. As previously mentioned, a state space derivation of the ISF was also suggested by Hajimiri [105]. In this approach the phase change is obtained by projecting the perturbation onto the steady state's direction of motion, that is the trajectory's tangent. In analogy to mechanical intuition, an orthogonal basis is used here. However, as shown by Demir [110], in reality an oblique basis has to be used, to guarantee that the remaining transversal perturbation components decay exponentially.

Furthermore, the techniques differ in how the sensitivity functions are related to phase changes. The phase equation of the ISF approach (Eq. 3.22) can be rewritten as a differential equation

$$\frac{d\phi(t)}{dt} = \frac{1}{q_{max}}\Gamma(\omega_0 t)i(t). \tag{3.46}$$

Unlike the Floquet approach (Eq. 3.39) previous phase changes are not considered in the right-hand side, resulting in an linear equation. The validity of this approximation depends on the noise input: It can be shown theoretically [117] and through simulation [118] that, in case of a stationary noise source, the statistical properties of the resulting phase function (i.e. the phase deviation spectra S_ϕ) are equal. The specific function $\phi(t)$, however, differs and is only accurately described by the nonlinear approach. In case of nonstationary input the results of both models diverge. An example is injection locking, where a sine wave is injected into a free-running oscillator, causing it to lock both frequency and phase with the input. While this behavior is correctly described by the nonlinear phase equation, the approximation is not able to capture this effect.

Despite these drawbacks, the ISF approach is popular for qualitative considerations, due to the more intuitive view. If the limitations of the employed approximations are known, that is the ISF is obtained via simulation and only stationary noise sources are considered, meaningful circuit insight can be obtained from the ISF (among others for flicker noise upconversion reduction in LC oscillators [93, 119–121], or for ring oscillators operating at liquid helium temperatures [122]). The Floquet approach and its nonlinear differential phase-change relation is, on the other hand, a mathematically rigorous approach which forms the basis for quantitative considerations. While it may be applied analytically (e.g. regarding phase noise calculations of ring oscillators [123]), its main area of application is as the algorithmic basis for the phase noise simulation of commercial circuit simulators, as *SpectreRF* [118].

Lastly, it should be noted that the Floquet approach suffers from open problems of its own. While the explicit calculation of the phase function is always valid (Eq. 3.39), the subsequent spectrum calculations (Eq. 3.45) might be invalid for certain oscillator types. For example, in phase-locked loops (PLLs) a fast oscillator is locked to a cleaner, but slower reference source. The observed PN spectrum for such a system is governed by the reference at low frequencies and by a voltage-controlled oscillator (VCO) at high frequencies with a transition region in between (where phase noise is not necessarily decreasing with frequency). The system as a whole can be viewed as an autonomous oscillator with a corresponding set of DAEs, for which the PN spectrum can be calculated according to Eq. 3.45. However, the resulting spectrum can inherently only consist of upconverted white and colored noise, and hence fails to describe the observed transition region. Another problematic case are coupled oscillators, where the noise causes a convection term (i.e. a frequency shift) in addition to the considered phase diffusion term [14]. In these examples, the theory has difficulties dealing with mechanisms with long time constants that are not explicitly identified as a current noise source, presenting a limitation that must be kept in mind when employing this framework.

3.2.5 Phase Noise Simulation

For a transistor-level simulation of an oscillator's phase noise, first the steady-state solution needs to be calculated, before the Floquet technique can be applied to the system of equations. Here, two methods are commonly used: The harmonic balance algorithm determines the steady-state solution in frequency domain. The shooting method, on the other hand, employs iterative transient simulations in time domain until a periodic initial condition is found. While the former method is better suited for linear oscillators with fewer contributing harmonics (e.g. LC oscillators), the latter has speed advantages for circuits with more nonlinear components (e.g. ring oscillators). Nowadays, the computational load during steady-state simulation does not constitute the simulation bottleneck, and both might be used for the most commonly encountered oscillator topologies [95].

The subsequent Floquet vector calculation can be carried out in frequency domain or in time domain [111, 113]. A short overview of the latter for DAEs is given here. The monodromy matrix $\Omega(-T, 0)$ (i.e. the state-transition matrix evaluated at one nominal oscillation period) can be obtained by numerically integrating the adjoint system

$$C^T(t)\frac{d}{dt}y - G^T(t)y = 0, \tag{3.47}$$

from the initial condition $Y(0) = I_n$ backwards in time to $Y(-T) = \Omega(-T, 0)$. This integration is not possible forward in time since for a stable system (Eq. 3.40) the adjoint Eq. 3.47 is unstable and numerical errors are amplified. The right eigenvector $u_1(0)$ can be shown to be equal to the time derivative of the steady state $u_1(0) = \dot{x_s}(t)$. Now, an eigenvalue decomposition of the monodromy matrix is carried out. The eigenvector corresponding to the eigenvalue 1 is the sought-after Floquet vector, which can be correctly scaled such that $v_1(0)C(0)u_1(0) = 1$. In case multiple eigenvalues are close to 1 (and the correct one cannot be identified due to numerical values), the inner product of the corresponding eigenvectors with $C(0)\dot{x_s}(0)$ can be consulted, which should equal zero except in the case of matching eigenvectors. Finally, the periodic time-dependent $v_1(t)$ for $0 \leq t \leq T$ is calculated by numerically solving the adjoint system (Eq. 3.47), again backward in time for stability starting from $v_1(T) = v_1(0)$. Once the Floquet vector is known, the contributions of the individual noise sources and their aggregated effect as a PN spectrum is easily obtained.

For accurate simulation results, it is important to provide realistic driving and loading conditions of the probed circuits, especially if these are partitioned to be simulated individually. This includes accurate modeling of layout effects, which can have a strong influence on waveforms and therefore on phase noise [95].

In systems with very long time scales (e.g. PLL-based oscillators) memory and computation constraints can be prohibitive to calculate a steady-state solution for the complete system. Here, behavioral modeling can be employed, where the jitter sequence is generated from the expected statistics of transistor-level simulations. The system-level jitter performance is then obtained by adding the individual behaviorally modeled sub-blocks [95].

3.2.6 Phase Noise Measurement

For the measurement of phase noise with laboratory equipment, different techniques can be employed.

The simplest approach is the use of a spectrum analyzer, where the power in a $1\,\mathrm{Hz}$ band at a specified offset from the oscillation frequency is measured and related to the carrier signal power. There are, however, various drawbacks: Multiple up- and downconversions of the signal, where phase noise of the spectrum analyzer's LOs may be added, limiting the measurement sensitivity. Furthermore, by measuring the voltage spectrum contributions of amplitude and phase modulations cannot be differentiated. Lastly, close-in frequencies cannot be resolved due to the limiting minimum resolution bandwidth of the spectrum analyzer (typically lower than $1\,\mathrm{Hz}$) [124].

In the phase-detector method depicted in Fig. 3.11 the signal of the DUT is mixed with a reference oscillation. A PLL hereby tracks the DUT's frequency ω_0 and additionally ensures a $90°$ phase offset between the mixer inputs. The mixing product contains a term with twice the oscillation frequency, which is filtered out by a low-pass filter (LPF), and a DC term, which due to the phase shift is sensitive toward the phase:

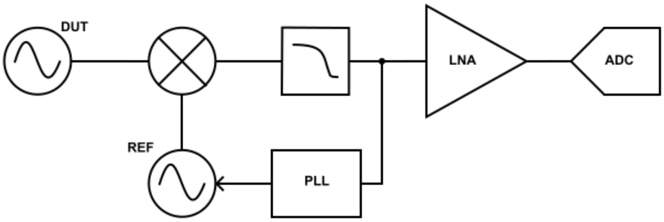


Figure 3.11: Block diagram of a phase detector circuit. Adapted from [124].

$$\begin{aligned} v_{mix}(t) &= V_{DUT}\sin\big(\omega_0 t + \phi\,(t)\big)V_{REF}\sin\big(\omega_0 t + \frac{\pi}{2}\big) \\ &= \frac{1}{2}V_{DUT}V_{REF}\Big(\sin\big(\phi\,(t)\big) - \underbrace{\sin\big(2\omega_0 t + \phi\,(t)\big)}_{\text{removed by LPF}}\Big) \\ &\propto \sin\big(\phi\,(t)\big), \end{aligned} \tag{3.48}$$

where V_{DUT} and V_{REF} are the amplitudes of the DUT's and reference oscillator's amplitude, respectively. The DC output voltage is then amplified with an low-noise amplifier (LNA) and can subsequently be digitized for further processing by an ADC. The measurable frequency range is therefore not limited by the resolution bandwidth, and very low offset frequencies can be reached. Here, only the PLL's bandwidth is a limiting factor, since it also tracks low-frequency phase noise. A further advantage is that only one frequency conversion of the signal takes place. The sensitivity is, however, still limited by the phase noise of the reference oscillator.

A variant of this technique replaces the reference oscillator with a delayed version of the signal itself by passing it through a delay line with fixed time delay, again adjusting the phase for quadrature. The low-pass-filtered voltage signal resulting from the mixing operation can again be related to the phase shifts. However, now the scaling relation contains a frequency-dependent sinc-function distorting the spectrum at frequencies close to the inverse delay time. Due to this drawback, this approach is rarely used.

Adding a cross-correlation technique can increase sensitivity of the reference oscillator-based phase detector approach beyond limitations due to noise of the measurement setup itself [125]: The signal of the DUT is fed into two identical phase detector circuits, each with its own reference oscillator. The respective outputs are then processed by an FFT analyzer, where a cross-correlation spectrum is calculated. Here, contributions from noncorrelated noise sources, as the two reference oscillators, will be reduced by $5\,\mathrm{dB}$ per factor 10 of performed cross-correlations [20]. The sensitivity of the measurement technique can therefore be drastically increased in a trade-off with measurement time.

A further improvement is presented by the digital phase demodulator technique [126]. Here, the phase detector is removed and the signal of the DUT is fed into an in-phase and quadrature mixer with a fixed-frequency reference oscillator. The amplified baseband signal is then digitized and the PN spectrum calculated. The advantage is that close-in PN is not tracked by the PLL and therefore no correction of this distortion is necessary. This measurement concept, in combination with the cross-correlation technique, is implemented in the *Rohde and Schwarz FSWP-26 Phase Noise Analyzer*, which is used for all off-chip phase noise measurements in this thesis.

Chapter 4

Theoretical Investigations on Phase Noise Simulation

To gain deeper insight into the phase noise mechanisms of a specific design it is beneficial to know the phase's sensitivity toward noise during the oscillation period, that is the Floquet vector. Since this information is not provided by commercial circuit simulators, it is shown in this chapter how it is obtained through a custom simulation flow. Subsequently, it is investigated how the accuracy of the underlying device models influences both the Floquet vector, as well as the corresponding PN spectra.

4.1 Implementation of Floquet Algorithm

In general the Floquet vector calculation is implemented according to the time-domain procedure described in Section 3.2.5. The corresponding flow is implemented to be executed in command line and consists of several steps described in the following.

First, to obtain a steady-state solution for the implemented circuit Cadence *spectreRF pss* is used. To relate the solutions to the underlying system of DAEs, as obtained by MNA, it is important to save the steady-state behavior of all state variables. This includes the voltages of all nodes, as well as the currents through *voltage-defining* circuit elements, such as voltage sources and inductors.

As a second step the linearization around the stable trajectory is simulated. While the full current-defining functions of the DAE ($g(x)$ and $q(x)$ for DC and AC behavior, respectively) are hidden in the proprietary compact models only their Jacobian matrices (the capacitance matrix $C(x)$ and conductivity matrix $G(x)$) are of interest. At each time point of the stable trajectory (i.e. each simulation time step) a *Perl* script sets up a simulation replicating the steady-state condition with DC voltage source added to all circuit nodes, and DC current sources added to replicate the current flowing through inductors and voltage sources. Now several *spectreRF AC* simulations are run, one for each state variable, where an AC stimulus is added at the corresponding voltage or current source, and the AC response of all state variables probed as a function of the stimulus frequency. The results for all time steps, all stimulus/probe state variable pairs, and frequency points are recorded in a results file.

In the next step, the AC simulation results file is evaluated by a *python* script to obtain the entries of the Jacobian matrices $C(x)$ and $G(x)$. For each stimulus/probe state variable pair, the AC simulation results versus frequency are fitted. The real part is fitted to a constant value, corresponding to the respective entry of the $G(x)$ matrix, and the imaginary part is fitted to a linear function, where the slope corresponds to the entry of the $C(x)$ matrix. Again, this procedure is repeated for all time steps, thus obtaining the full time-dependence of the Jacobian matrices. The quality of fit can be monitored to detect errors in the procedure.

Once the Jacobian matrices of the DAE are known, the Floquet vectors can be calculated as proposed by Demir [114] and described in Section 3.2.5.

The last step is to calculate the PN spectrum. In addition to the Floquet vectors, the noise matrices $B(x)$ for white and colored noise sources need to be known. In a similar approach as before, a *Perl* script is used to set up a simulation replicating the steady state at each time step. Now *spectre noise* simulations are carried out and the noise at each circuit node recorded, where distinct noise mechanisms (e.g. flicker noise, shot noise, etc.) can be separated. A *python* script uses the results to build the corresponding noise matrices. These can be used to calculate the phase noise contributions of the white and colored sources according to Eqs. 3.43 and 3.44, which are added up to the full PN spectrum according to Eq. 3.45.

The result of the Floquet vector calculation were verified for an exemplary $10\ \mathrm{GHz}$ ring oscillator. A transient simulation was carried out, where after a sufficient time to reach steady state ($50\ \mathrm{ns}$) a short current pulse ($1\ \mathrm{ps}$ of $1\ \mathrm{\mu A}$)[1] is injected. The resulting phase shift in simulation was

---

[1] A short and low amplitude current pulse is used to guarantee that the results don't exceed the validity of the Floquet theory's linearization. Although this specific pulse is at the limit of physical sensibility (it corresponds to ca. 6 electrons) it is suitable in simulation for verification purposes.

observed to be $0.75\,\mathrm{mrad}$. Calculating the phase shift via the Floquet vectors (Eq. 3.39) resulted is a well fitting result of $0.72\,\mathrm{mrad}$.

Transistor compact models merit special attention in the flow described above. As laid out in Section 2.1.3 these models typically contain internal circuit nodes due to the parasitic network around the core model. However, for the correct execution of the described Floquet vector simulation flow, all circuit nodes need to be explicitly addressable in the AC and noise simulation. In some cases, it is possible to modify the model parameters of the foundry-delivered model files to eliminate internal nodes. For example, RDSMOD can be set to include parasitic drain/-source resistances internally rather than externally, or RGATEMOD to switch off the external gate resistance. However, these patched-up models might also change the steady-state solution unpredictably, especially in light of typically incomplete documentation of model behavior.

4.2 Influence of Transistor Model Accuracy

A possible solution is to replace complex technology-specific transistor models by well-understood and well-documented general compact models, as SPICE level 1 or 3. In addition to avoiding the described workaround with its possibly unpredictable implications, simpler models can offer more intuitive insight into the underlying phase noise mechanisms, facilitating the design of LOs with tight phase noise specifications. Especially for early qualitative investigations of novel circuit topologies the use of simple, more accessible models might outweigh the accuracy of complex proprietary models with possible black-box behavior due to encrypted parts. To validate this approach, it is investigated how much complexity can be reduced, while still obtaining qualitatively correct simulation results for phase sensitivity (Floquet vector) and statistical phase deviations (PN spectrum).

Parts of the chapter have been extracted from [1].

4.2.1 Preparation of Compact Models

Two transistor models are prepared for the comparison describing the integrated devices with two different levels of complexity. As an accurate model, the foundry-delivered model for a $16\,\mathrm{nm}$ FinFET technology is used, which is based on BSIM-CMG and contains relevant physical effects for deep-submicron devices. At the other end of the complexity spectrum the SPICE level 1 model was used [127]. It is less accurate since many second-order effects are not considered, but its equations are therefore much more manageable and intuitive. For example, if no back-gate voltage is applied, the drain current of the device is only dependent on three model parameters: The threshold voltage, the transconductance, and the channel length modulation parameter.

The parameters of the SPICE model were fitted to the accurate model with the use of *IC-CAP*. This fitting is conducted for one specific transistor geometry, such that correct width and length scaling is not required. Fig. 4.1 shows a comparison of selected characteristics between the high-accuracy reference model and the simple fitted model. The DC behavior (upper row) shows a reasonable fit by the simple model, where the differences are mostly due to mobility saturation effects arising at high gate voltages. A further difference lies in the subthreshold regime, where leakage currents are not contained in the simple model (not visible in the figure due to scale). Regarding AC characteristics, the depletion layer capacitances between drain and bulk (lower left) and source and bulk (not shown) exhibit a very good agreement with the reference as a function of drain/source voltage. More drastic differences are observed in all gate capacitances (gate-drain, gate-bulk, and gate-source, where the latter is shown on the lower right) as a function of gate voltage, which is not too surprising, since the two models describe fundamentally different transistor geometries (planar versus tri-gate FinFET).

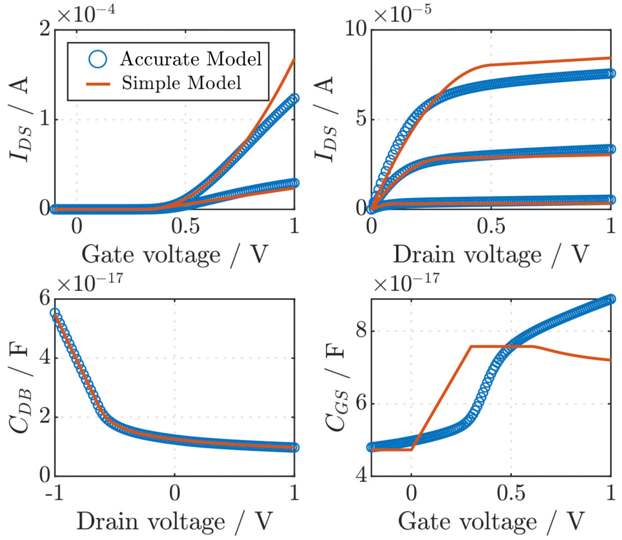


Figure 4.1: Comparison between accurate model and fitted simple model for selected transistor characteristics: (a) Transfer characteristic, (b) output characteristic, (c) drain-bulk capacitance, and (d) gate-source capacitance. Reprinted from [1] ©2023 IEEE.

4.2.2 Resulting Floquet Vectors and Phase Noise Spectra

Using both models the phase noise calculations were carried out according to the flow described in Section 4.1 for the two exemplary circuits depicted in Fig. 4.2: A three stage single-ended ring oscillator with the smallest allowed NMOS and PMOS transistor geometry and a Colpitts oscillator using larger NMOS transistors.

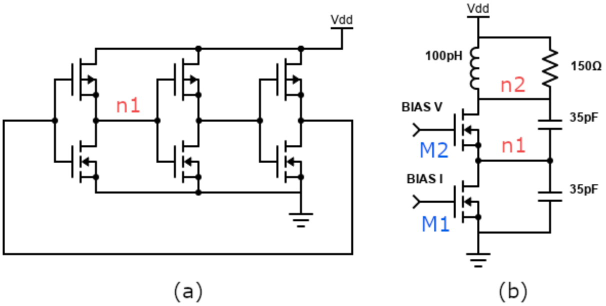
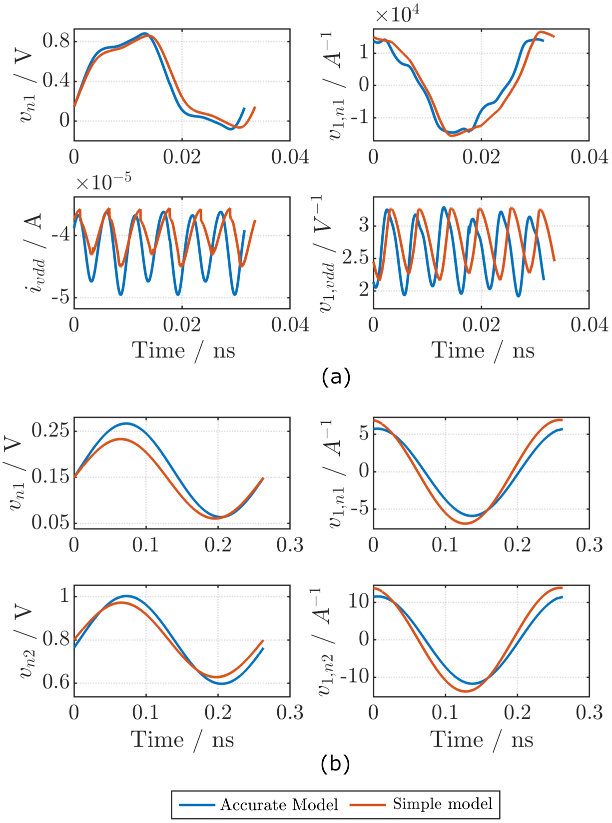


Figure 4.2: Schematics of the investigated circuits: (a) A single-ended ring oscillator, and (b) a Colpitts oscillator. Reprinted from [1] ©2023 IEEE.

The results after the steady-state simulation and Floquet vector calculation steps are shown in Fig. 4.3. Fig. 4.3(a) shows the depicted state variables for the ring oscillator, which are the voltage of the n1 net and the current through the supply voltage source. The other nets between the inverter stages are just phase-shifted versions of n1 and are therefore equivalent. The steady-state solution is qualitatively similar for both models used, with two notable distinct aspects: For the simple model, the oscillation period is slightly longer and sharp kinks are observed in the voltage supply current. The reason is discontinuities in the derivatives of the simple model's defining functions. Looking at the corresponding Floquet vector components $v_{1,n1}$ and $v_{1,vdd}$, a qualitative consistency can be certified, where, however, the accurate model seems to reveal more details of the phase-sensitivity function.

In case of the Colpitts oscillator, Fig. 4.3(b) depicts the steady-state solutions for the voltage nets n1 and n2, which show an almost equal oscillation period. The Floquet vectors are as well again qualitatively matching, with the main difference lying in a slightly scaled up noise sensitivity predicted by the simple model.

Based on the presented Floquet vectors the PN spectra are calculated and depicted in Fig. 4.4. For both oscillator topologies the spectra based on both models coincide for large parts of the frequency range. Differences are observed for the ring oscillator in the far-off PN, and for the Colpitts oscillator in the close-in PN region. Additionally to the results obtained from the



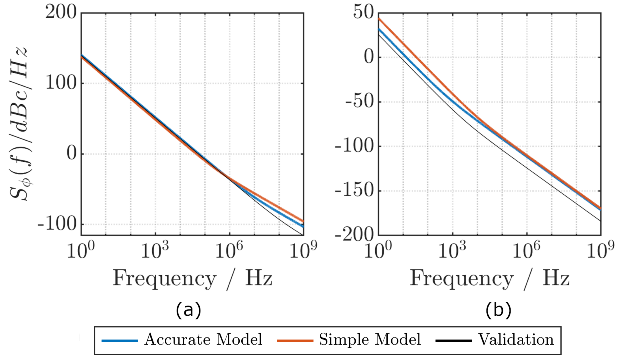
(a)

(b)

Figure 4.3: Comparison of simulation results for accurate and simple model. Steady-state solutions of selected state variables are shown in the left column with their corresponding component of the Floquet vector in the right column. (a) Ring oscillator. (b) Colpitts oscillator. Reprinted from [1] ©2023 IEEE.

implemented flow, a validation simulation with *spectreRF pnoise* is shown. While the results match in general, a small offset can be observed, which can be attributed to the previously mentioned necessary model file modifications.

A closer look is now taken at the observed differences for low-frequency phase noise of the Colpitts oscillator. Here, the close-in PN can be attributed to the flicker noise of the two transistors. According to Eq. 3.45 their relative contributions are proportional to $c_{c,n}^2$, with their respective value shown in Table 4.1 for both models. The contributions of M1 strongly dominate over M2 according to the accurate model. In the simple model the contributions of the M1 and M2 both increase by a factor of 4 and 1448, respectively. This leads to a total increase of close-in PN of a factor of 15.3, or 11.8 dB, as observed in the spectrum.



(a)

(b)

Figure 4.4: Comparison of simulated PN spectra for the accurate and simple model. (a) Ring oscillator. (b) Colpitts oscillator. Reprinted from [1] ©2023 IEEE.

Table 4.1: Phase noise contributions in the flicker noise regime of the transistors in the Colpitts oscillator. Reprinted from [1] ©2023 IEEE.

c_c^2 in $10^{-9}A^{-2}$	M1	M2	Sum
Accurate Model	6.38	0.05	6.42
Simple Model	25.9	72.4	98.3
Factor	4.05	1448	15.3 (11.8 dB)

The question arises why the contribution of M2 increases by more than three orders of magnitude, even if the differences in the Floquet vector are much smaller. Individual contributions are calculated according to Eq. 3.44 as the time average over one period of the Floquet vector noise matrix product $v_1(t)B(t)$. For the investigated case this function is shown for both models in Fig. 4.5. Here, the scaled-up noise sensitivity can again be observed, however, with a relative difference between the models of at most a factor of 2. Since the relevant average value is very close to zero, rather small differences can lead to large relative differences for the calculated contributions. This suggests that the PN spectrum simulation in the close-in region relies on a fragile balance between positive and negative phase contributions. Since this source of uncertainty is intrinsic to the mathematical theory and independent of circuit topology, accurate device models are essential for the calculations of statistical phase fluctuation properties.

4.2.3 Conclusion

In conclusion, the presented results increase confidence in phase-sensitivity simulations conducted with simplified device models, since they were shown to be qualitatively robust against omitting

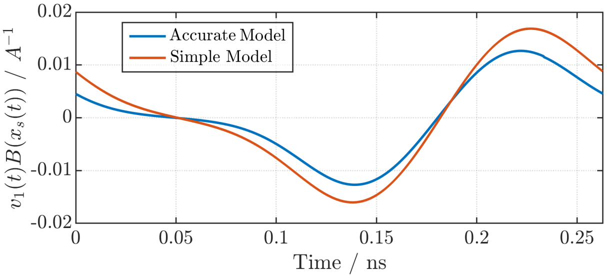


Figure 4.5: Floquet vector noise matrix product for flicker noise of the M2 transistor in the Colpitts oscillator. Reprinted from [1] ©2023 IEEE.

of second-order effects. This enables the investigation of phase noise upconversion in novel topologies decoupled from a specific technology node. On the other hand, it was shown that the resulting close-in PN spectrum can vary more strongly with model changes, suggesting that the most accurate available models should be used to increase confidence in the quantitative results.

Chapter 5

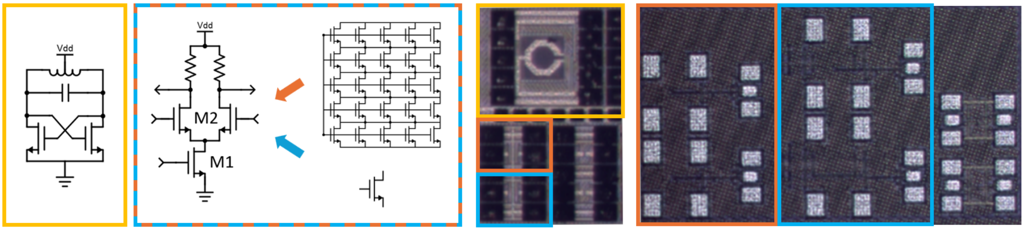
Phase Noise Upconversion in Advanced Technology Nodes

In advanced technology nodes, low-frequency noise might exhibit effects additional to the typical 1/f-shaped flicker noise spectrum. In this chapter an investigation is presented on how RTN and other such deviations influence the PN spectrum of oscillators in $2\,\mathrm{nm}$ GAA and $16\,\mathrm{nm}$ FinFET. In addition, statistical variations are studied in dependence on device size.

Parts of this chapter are extracted from a submitted publication [5].

5.1 Methodology

For the close-in PN of oscillators a $1/f^3$-slope is typically expected, and simulated, resulting from an upconversion of the ideally $1/f$-shaped flicker noise spectrum of the employed devices. However, in recent nanoscale technology nodes new effects in MOSFET low-frequency noise come into play: Due to their small area, only a few traps exist per transistor, such that the conventional understanding of flicker noise [54] as a superposition of many charge traps brakes down (for details, see Section 2.2.2.4). Instead other physical noise effects, such as RTN of single traps may dominate over a background $1/f$-spectrum due to access resistance and channel scattering effects [69, 71].



(a) (b) (c)

Figure 5.1: (a) Schematic diagram of implemented oscillator topologies: LC oscillator (left) and ring oscillator stage with unit transistor and 5x5 array (right). (b) Micrograph of Gate-All-Around and (c) FinFET dies: The LC oscillator is marked in yellow and ring oscillators with unit transistors and 5x5 transistor arrays in blue and red, respectively. Unmarked portions of the chip constitute test structures for single devices.

An experiment is designed to investigate the phase noise upconversion of these RTN spectra and other non-$1/f$ noise effects. Here, two oscillator topologies for phase noise measurement are implemented in the latest CMOS GAA technology node (see Fig. 5.1(b)), where the respectively employed transistors were additionally placed individually for flicker noise measurement:

- LCO: An LC oscillator with a differential transistor pair gain stage (see Fig. 5.1(a)). Here, the two transistors of ultra-low threshold voltage V_t flavor are relatively large with a high multiplicity and finger number of vertically stacked ribbons. The supply voltage is $0.7\,\mathrm{V}$.
- $\mathrm{RO_{unit}}$ and $\mathrm{RO_{array}}$: Two ring oscillators with differential amplifier stages (see Fig. 5.1(a)) and a fan out of 2. While for $\mathrm{RO_{unit}}$ the minimally allowed device size (1 finger of vertically stacked ribbons) with standard V_t is used for both the current source transistor M1, and the differential pair M2, $\mathrm{RO_{array}}$ uses a $5x5$-stacked array thereof, resulting in a 25-fold device area. The supply voltage is $0.7\,\mathrm{V}$ and the gate voltage of the current source transistors $0.5\,\mathrm{V}$.

For comparison purposes, the ring oscillator experiment was additionally conducted in a $14\,\mathrm{nm}$ FinFET technology node: $\mathrm{RO_{unit}}$ (here 4 fin of 4 finger) and $\mathrm{RO_{array}}$ were used in the delay cells of 3- and 17-stage ring oscillators, as well as individual transistors for flicker noise measurement (see. Fig. 5.1(c)).

5.2 Measurement

The measurements are conducted on bare-die in case of the GAA experiment and on-wafer in case of the FinFET experiment. In both cases, the terminals of the single transistors are directly connected to aluminum signal pads on the top-most metal layer. In case of the oscillators, increasingly large inverter stages are used to drive the signal to the output pads. The wafer/die is placed on a probe station (*Cascade Michrotech Elite 300*), where it is held in place by a vacuum. Probe needles fixed on the probe station bench with micropositioners can be adjusted with a microscope to contact the pads. From here cables can be connected to the measurement equipment. Phase noise measurements are conducted with a *Rohde & Schwarz FSWP Phase Noise Analyzer* with a cross-correlation number of 100 and a resolution bandwidth of $0.3\,\mathrm{Hz}$ and flicker noise measurements with a *Keysight Advanced Low-Frequency Noise Measurement System* (more details about the measurement methods are given in Sections 3.2.6 and 2.2.5.1, respectively). An exemplary measurement setup is depicted in Fig. 5.2.

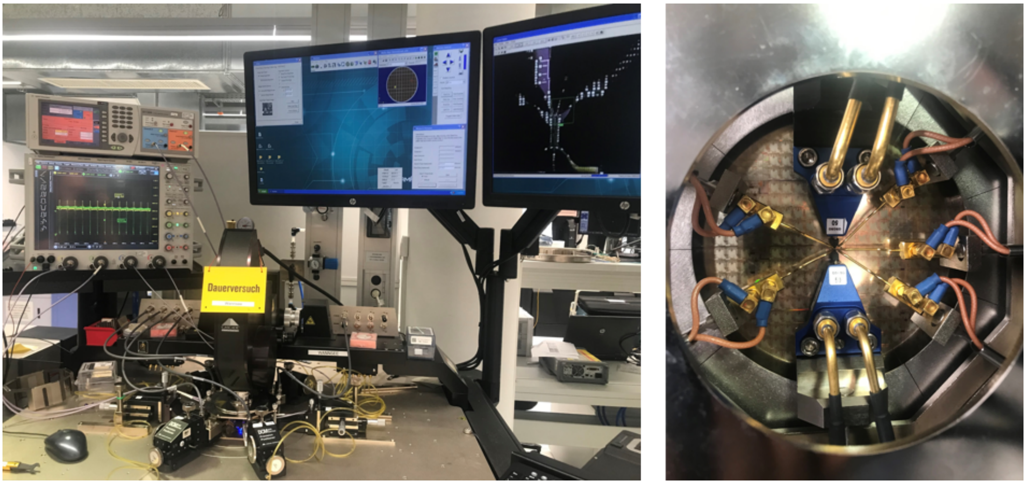


Figure 5.2: Exemplary laboratory measurement setup. (Left) The probe station bench with micropositioners and cables to measurement equipment: In this case a pulse generator and a RF oscilloscope. (Right) Top view of probe needles and wafer in the background. From north and south direction RF needles and from west and east direction DC probe needles.

Depending on the frequency range of the measured signal, particular attention must be paid to the connection network between DUT and laboratory measurement equipment, since parasitic capacitances are added. For low-frequency signals, such as the drain current of a transistor under DC conditions or flicker noise, these effects are less problematic. On the other hand, for RF signals, as RF noise or a high-frequency LO signal for phase noise measurement, techniques must employed to minimize parasitic capacity and shield the signal. For this reason, only the top-most metal is connected in the signal pads, and ground connections are added on either side. The corresponding RF needle probes exhibit therefore a ground-signal-ground configuration with a typical pitch of $50\,\mathrm{\mu m}$ (*Cascade Michrotech Infinity Probes* or *Z-Probes*). Just as the probes, the connecting cables need to be rated for the correct frequency range, where especially the signal connection has to be free of possible dirt and grease contamination.

The measurement of many dies on the same wafer can be automated by remotely controlling the measurement equipment and the probe station. A General Purpose Interface Bus (GPIB) connection and either proprietary software (flicker noise) or Python code (phase noise) can be used to automatically step to all dies on the wafer and perform the respective measurement.

5.3 Results

In the following the measurement results for the Gate-All-Around and FinFET experiments will be presented.

5.3.1 Gate-All-Around

The top of Fig. 5.3 shows the measured PN spectra for $\mathrm{RO_{unit}}$, $\mathrm{RO_{array}}$ and the LCO. Most surprisingly, in all circuits a reduction in slope is observed in the $1\,\mathrm{Hz}$ to $1\,\mathrm{kHz}$ frequency range, leading to a deviation from the conventionally expected $1/f^3$-slope in the upconverted flicker noise regime. The bottom plot of Fig. 5.3 displays these measurements scaled with f^3 and set to zero at the lower frequency limit. Here, the discrepancy between the expected horizontal line and the step in the measured phase noise is readily apparent and observed to be even more pronounced for the ring oscillators than for the LC oscillator.

Measurements of the ring oscillators on 25 dies show that the effect is consistently observed in the same frequency range (see Fig. 5.4(a)). Apart from this atypical slope-reduction, the measured spot noise distribution follows the commonly observed log-normal distribution for both $\mathrm{RO_{unit}}$ and $\mathrm{RO_{array}}$, as can be seen in the probability plot of phase noise measurements at $1\,\mathrm{kHz}$ (Fig. 5.4(b)). As flicker noise scaling with transistor size suggests, both the mean and variance of the measured spot noise are higher for the $\mathrm{RO_{unit}}$ circuit.

Looking at flicker noise measurements of the unit transistor and the transistor array (see Fig. 5.5), in each case a plateau can be observed in the respective frequency range. This effect is especially pronounced for high gate voltages, whereas the spectrum approaches a more ideal $1/f$-shape close to the threshold voltage. Interestingly, this observation is again consistent over many dies, as can be seen in Fig. 5.6 showing flicker noise measurements for fixed drain voltage ($v_d = 0.375\,\mathrm{V}$) and different drain currents. Again, the spot noise power at $1\,\mathrm{kHz}$ follows a log-normal distribution (see rightmost panel of Fig. 5.6).

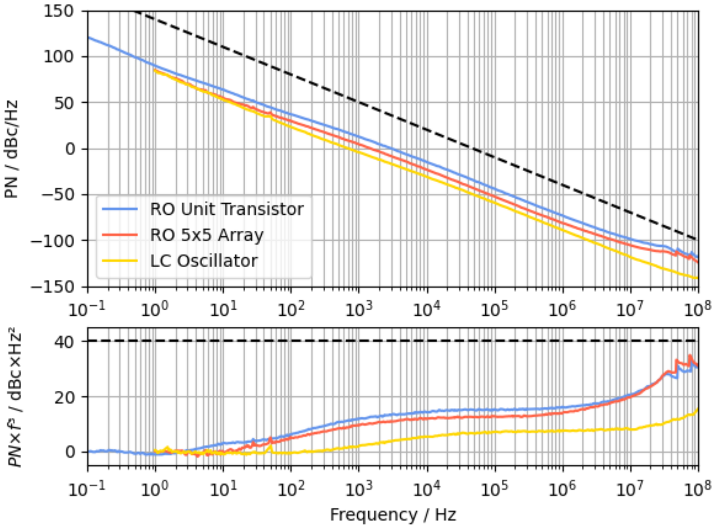


Figure 5.3: (Top) Measured phase noise of selected $\mathrm{RO}_{\mathrm{unit}}$, $\mathrm{RO}_{\mathrm{array}}$ and LC oscillator DUT of GAA experiment. (Bottom) Scaled with f^3. The dashed line provides a guide for the eye of the conventionally expected slope.

5.3.2 FinFET

In Fig. 5.7 the results of the analogous phase noise measurements of 80 dies are depicted for the FinFET experiment. In this technology, the behavior is different: The overall evolution of the phase noise measurements is close to the expected $1/f^3$-slope (the slightly shallower slope is a common observation across nonplanar technology nodes). Deviations in the form of upconverted RTN spectra show up as bumps in the frequency-scaled plot. In contrast to the GAA experiment, these observations are not consistent over many dies but rather statistically distributed over dies and frequency. The larger the contributing transistor area due to stage number or device size, the fewer deviations are observed.

Flicker noise measurements for the FinFET show the corresponding behavior: In addition to a stable $1/f$-background (see top of Fig. 5.8), deviations can be observed especially for the unit transistor. In the frequency-scaled plot (see bottom of Fig. 5.8) the statistical nature of these RTN contributions over the whole measured frequency range can be observed.

5.4 Discussion

Plateaus in the measured flicker noise can originate from the RTN of single charge traps added over a $1/f$-background: In case of the FinFET experiment the spectrum shape and statistical

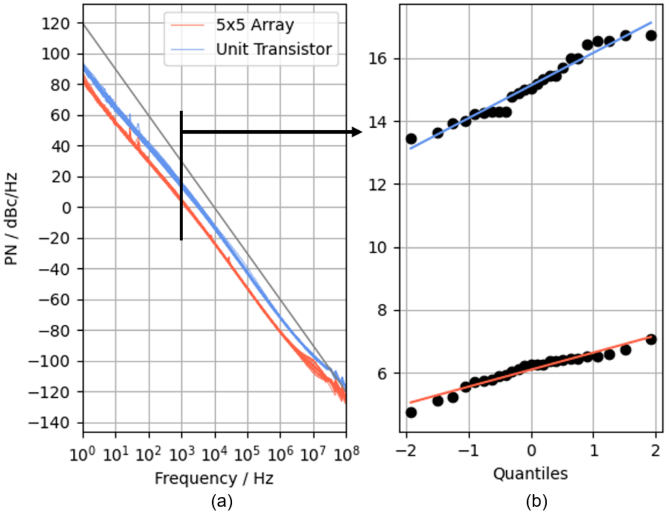


Figure 5.4: (a) Measured phase noise of GAA $\mathrm{RO_{unit}}$ and $\mathrm{RO_{array}}$ on 25 dies. (b) Probability plot of spot measurements of $\mathrm{RO_{unit}}$ and $\mathrm{RO_{array}}$ at 1 kHz.

nature suggest a charge trap origin of the observed bumps. In the GAA experiment only for one of the DUTs a clear trap could be separated from the background spectrum at low gate overdrives (see Fig. 5.9). The common plateau observed at high gate overdrives, on the other hand, does not conform to this noise source separation. The consistency over many dies and both transistor sizes does also not support statistically distributed charge traps as the origin of the plateau.

Concerning the phase noise in the FinFET experiment, the observed deviations from a $1/f^3$-slope can be attributed to a direct upconversion of the flicker noise spectra: The statistical RTN spectra appear as statistically distributed bumps in the phase noise. Here, a larger contributing transistor area leads to more averaging of flicker noise contributions to the PN spectrum, reducing the effect of single traps for ring oscillators with many stages and/or larger transistors.

In case of the phase noise in GAA experiment, the slope reduction can also be attributed to an upconversion of the measured flicker noise plateau. To understand why the phase noise of the ring oscillator is impacted more than the LC oscillator, the transistor bias conditions contributing to upconverted phase noise need to be considered. Fig. 5.10 shows the state space of the transistors (gate-to-source and drain-to-source voltage), where the bias conditions for flicker noise measurement (Fig. 5.5) are marked with a cross. The trajectory traversed by the ring oscillator transistors is shown in Fig. 5.10(a), where M1 denotes the current source transistor and M2 the two equivalent transistors of the differential pair. Likewise, the trajectory of the equivalent differential pair of the LC oscillator is shown in Fig. 5.10(b) reaching voltages outside the nominal operating voltages. The phase noise contributions along the stable trajectory were calculated with

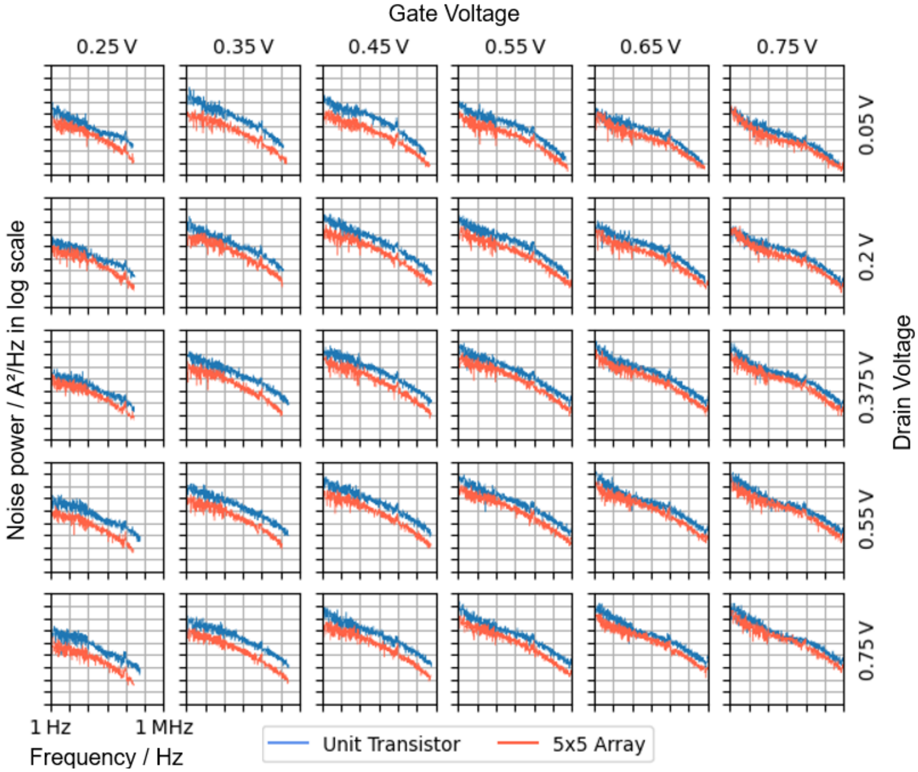


Figure 5.5: Measured low-frequency noise of the GAA unit transistor and 5x5 array for different gate and drain voltages.

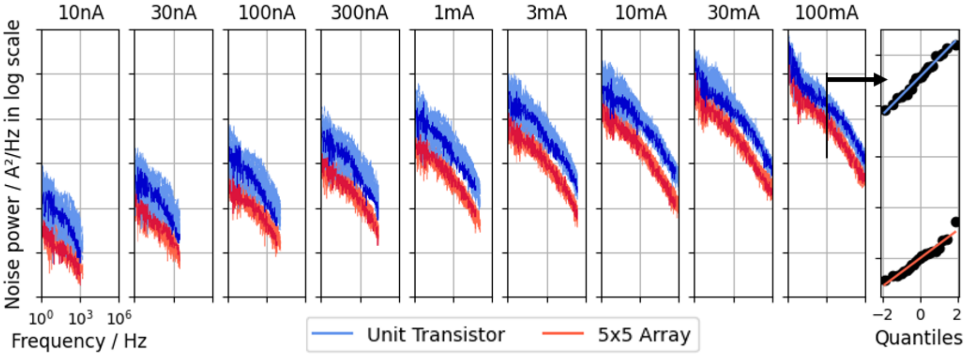


Figure 5.6: Measured low-frequency noise of GAA unit transistor and 5x5 array for 25 measured dies (bright value band), and their respective average (dark color) at a fixed drain voltage of $v_d = 0.375\,\mathrm{V}$. In the rightmost panel shows the respective probability plot of low-frequency noise measurements of unit transistor and 5x5 array at $1\,\mathrm{kHz}$ and drain current of $100\,\mathrm{mA}$.

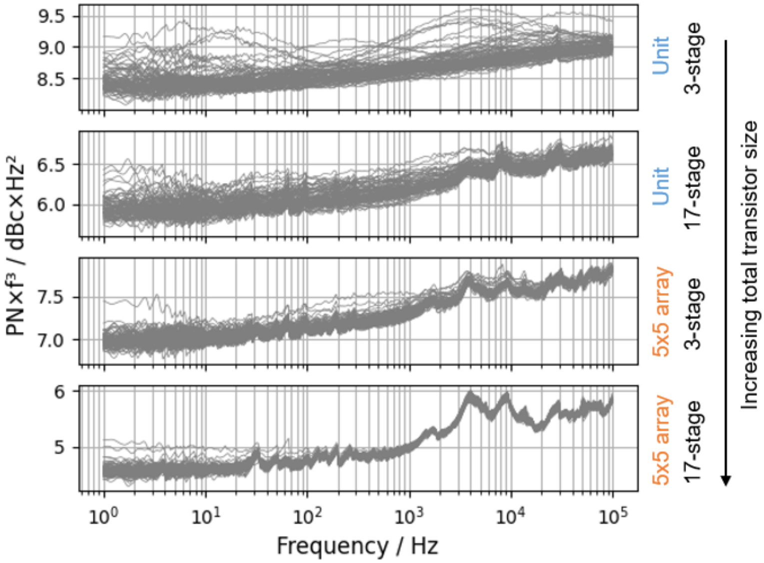


Figure 5.7: Frequency-scaled phase noise measurements of four ring oscillator variants ($\mathrm{RO}_{\mathrm{unit}}$ and $\mathrm{RO}_{\mathrm{array}}$, each with 3 and 17 stages) on 80 dies of the FinFET experiment.

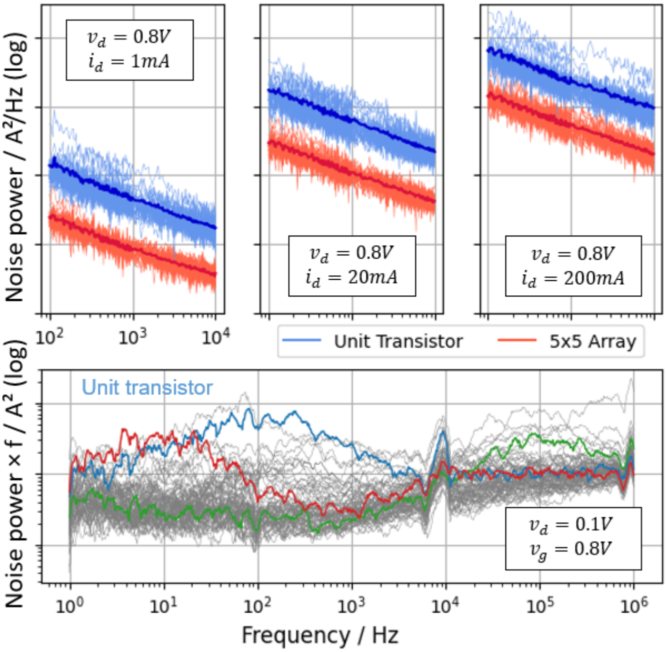


Figure 5.8: (Top) Statistical flicker noise measurements of the FinFET unit and 5x5 array on 80 dies at different biases with the respective average (dark color). (Bottom) Frequency-scaled measurements with 3 selected dies highlighted.

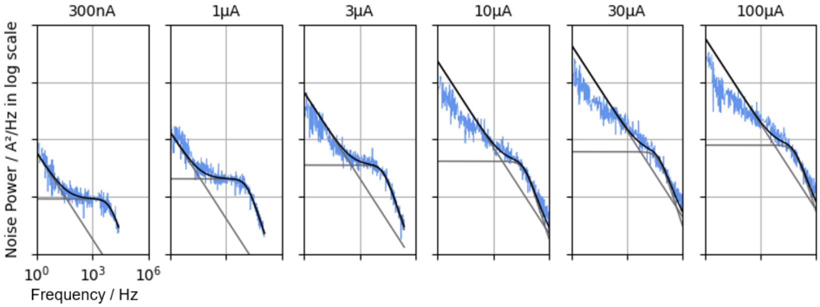


Figure 5.9: Measured low-frequency noise of a selected Gate-All-Around unit transistor and its best fit separation into a background $1/f$-noise and random telegraph noise.

the Floquet theory [111]: For each net of the circuit the Floquet vector was calculated, representing the sensitivity of the oscillation's phase toward noise during the oscillation period. By multiplying this sensitivity with the flicker noise generated by the transistors under the respective bias, a relative contribution to phase noise can be obtained. In state space, high relative contributions are marked with a brighter background color. The flicker noise upconversion can be observed to happen at different bias conditions for the two oscillator topologies: The ring oscillators' phase noise is dominated by upconverted flicker noise of the current source transistor M1, which has almost stable bias conditions. Notably, for this (and close-by) bias conditions, a rather prominent plateau is observed in the GAA flicker noise measurements. For the LC oscillator, on the other hand, a broader range of bias conditions contributes to phase noise. While some of them exhibit a flicker noise plateau other upconverted bias conditions (of lower gate voltage) already show a more ideal $1/f$-dependence in the flicker noise measurement. The total phase noise of the LC oscillator therefore still shows a reduction in slope due to the upconverted flicker noise plateau, this effect is however reduced compared to the ring oscillators due to the averaging with bias conditions where this effect is less pronounced.

5.5 Conclusion

Non-$1/f$ effects observed in the low-frequency noise spectrum of transistors - such as RTN or flicker noise plateaus - were shown to be upconverted to the phase noise of oscillators in GAA and FinFET technology nodes. The exact shape of the deviations from the typically expected $1/f^3$-slope for close-in PN was shown to depend on the FN spectrum at relevant bias conditions according to Floquet theory, which is dependent on the oscillator topology. Additionally, statistical RTN contributions to phase noise are observed to be dependent on the contributing transistor area.

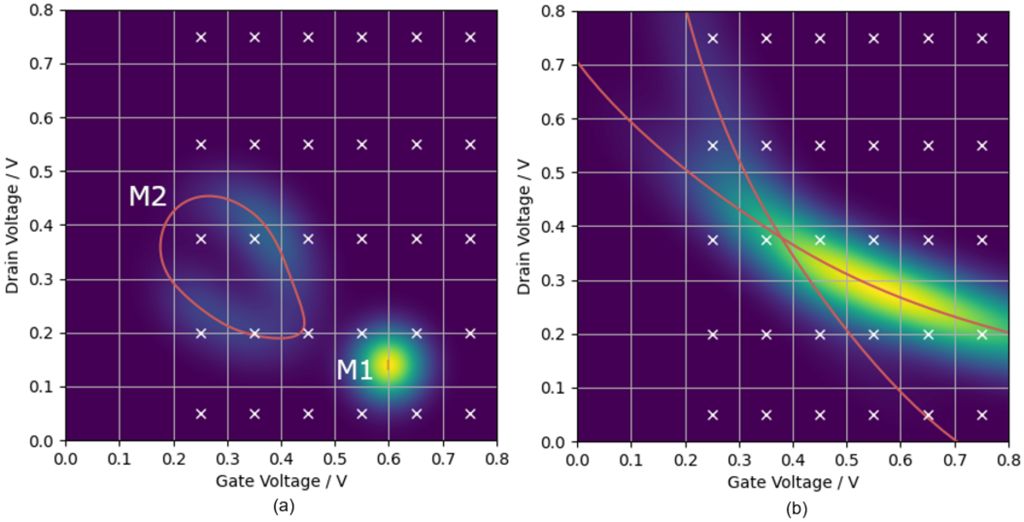


Figure 5.10: State space of transistors in (a) the ring oscillator and (b) the LC oscillator. Measured bias conditions for low-frequency noise are marked with a cross. The relative contribution of the traversed bias conditions (trajectory) are indicated by the background color (higher contributions are brighter).

While the variability due to RTN (FinFET experiment) can be reduced more easily by appropriate sizing, upconversion of the flicker noise plateau (GAA experiment), can only be mitigated by adjusting the biasing of the relevant transistors. Our results therefore underline that careful bias- and area-dependent statistical modeling of low-frequency noise effects is crucial for a good prediction of PN variability.

Chapter 6

On-chip Noise Measurement

Apart from laboratory measurements, noise parameters can also be obtained by integrated "on-chip" measurement macros. In this chapter, novel on-chip measurement techniques for both flicker and phase noise are presented. After an overview of previous approaches, the respective concept is introduced. Simulations and measurement results verify the proposed techniques.

6.1 Remarks on Spectral Estimation

Both in flicker noise and phase noise on-chip measurements the sought-after quantity is a power spectrum, that is a PSD. Since in many techniques (including the ones presented in this work) these spectra are calculated from time-domain data, a closer look should be taken at the corresponding signal processing techniques. Since the measured signals are inherently finite and consist of discrete sampling points the true PSD can only be estimated in form of a periodogram: From time series data, the periodogram can be calculated as the squared amplitude of an FFT. Here, multiple mathematical intricacies should be addressed:

As a first effect, it should be noted that due to the inherent sampling in jitter measurements with approximately frequency f_0, frequency components larger than $f_0/2$ will be aliased and in the spectrum folded to the $[0, f_0/2]$ range. Since the considered flicker noise and phase noise spectra fall off rapidly toward higher frequencies, the effects of aliasing are typically limited to the high-frequency end of the calculated periodogram.

Secondly, the sampling of jitter occurs at the zero-crossing and is therefore, as a consequence of jitter itself, not uniformly spaced. Theoretically, the spectrum estimation technique must be adjusted accordingly, for example by employing the Lomb periodogram [128]. In practice, the sampling point shifts due to jitter are so small that no effects on the spectrum can be observed.

As a third effect, spectral leakage spreads delta peaks in the spectrum over a wide frequency range if the measurement window is not a multiple of the corresponding signal period. This effect can be reduced by the multiplication of the data with window functions forcing periodicity and the boundaries. However, in smooth spectra without strong peaks (as generally observed in flicker noise and phase noise disregarding spurious tones), this effect is less important.

Lastly, the calculated periodogram exhibits a nonzero variance around the true PSD, even for a sample length approaching infinity [129]. Here, a common method is to average the PSDs of multiple data samples (Bartlett method), which might also be windowed and overlapping (Welch method). Especially if recording a large number of datasets is prohibitive, a smoothing of the PSD by averaging over small intervals in the frequency domain can also reduce the statistical variance (Daniel method).

6.2 On-chip Phase Noise

As discussed in Section 1.1.2, an on-chip integration of phase noise measurements has the advantage of being available in-field, such that BISTs can be implemented to dynamically monitor an LO’s performance, for example in a 5G/6G transceiver and radar systems, enabling PN/power trade-off techniques. Therefore, a novel technique termed *delta jitter* is introduced, which relies on comparing the signal under test to a second uncorrelated on-chip LO. This oscillator can be an identical replica of the oscillator under test (replica method, see Section 6.2.3), or in a generalized version an arbitrary uncorrelated LO (multiple local oscillator method, see Section 6.2.4).

Parts of this section have been extracted from [2, 3] and constitute a pending patent [4].

6.2.1 Previous Approaches

An overview of previously employed on-chip phase noise measurement techniques is given in Fig. 6.1. The phase is measured in frequency or time domain with either analog or digital circuitry. The approaches are discussed in detail in this section.

A natural starting point for on-chip measurement architectures is to emulate laboratory equipment. One such implementation [130] in frequency domain uses the previously discussed delay line

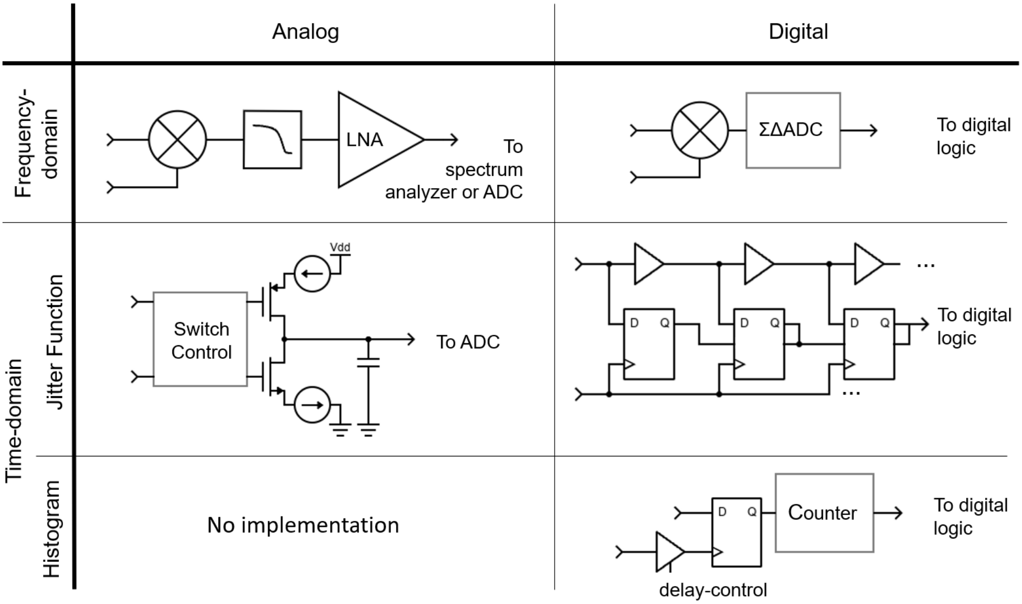


Figure 6.1: Overview of on-chip phase noise measurement concepts. One of the two inputs is in each case connected to the signal under test. The second input can be connected to a clean reference source or to a delayed version of the signal itself.

approach, where the delay elements, mixer, low-pass filter, as well as a subsequent baseband LNA are implemented as one integrated macro (Fig. 6.1 upper left). However, the proposed circuitry still relies on an off-chip spectrum analyzer to measure the resulting baseband signal (although basic spectrum analyzers may also be implemented on-chip [131]). The circuitry includes a calibration mechanism that keeps the mixer at the highest sensitivity operating point by adjusting the supply voltage of the inverter chain to result in a quadrature phase shift at the mixer. This is achieved by keeping the DC offset of the mixer at zero. As all delay line approaches, the circuit suffers from the inherent sinc-dependence of the sensitivity factor on the measured noise frequency component. An approach using a clean reference source does not show this dependence. Respective implementations have been shown, where an on-chip bulk acoustic wave resonator serves as a reference [132]. For the use-case of a BIST these implementations are, however, not viable due to the large area consumption.

In both implementations mismatch and noise sensitive analog blocks play a core role. A common technique is therefore to measure the output of a phase frequency detector with a $\Sigma\Delta$-ADC (Fig. 6.1 upper right), which as complete circuit block is often termed $\Sigma\Delta$-time-to-digital converter (TDC) [133, 134]. Here, possibly self-calibration techniques might be included in the setup [135]. In these approaches a high oversampling rate of the noise component of interest is needed to obtain a good measurement resolution. A drawback common to all mentioned approaches relying on phase detection in the frequency domain, whether digital or analog, is that phase and amplitude noise are not distinguished in the measurement.

Much simpler implementations can be achieved by measuring phase deviations in time domain by determining the time of oscillation edges. This approach has the advantage that at these times the phase is well-defined and not influenced by amplitude noise. One proposed approach is to measure the histogram of a signal's jitter (Fig. 6.1 lower right). This can be achieved by passing the signal and a reference clock through a delay line, connecting to the data and clock input of a flip-flop, respectively. By sweeping the delay of the reference via the inverter chain supply voltage, the cumulative jitter distribution, from which the rms value can be obtained, is measured [136]. In a similar approach, time difference amplifiers are added to increase the resolution of the measured histogram at the expense of the maximum sampling frequency [137]. A further version uses under-sampling making the comparison with a reference clock at scarce random times during the oscillation period [138]. This approach reduces power consumption for full integration, including data evaluation. The common application of these approaches is the characterization of jitter in digital circuits, where the time between edges, that is the ctc jitter, is crucial. Therefore, low-frequency components like flicker noise are neglected, such that the jitter can be fully characterized by the rms value. Due to missing timing information of the recorded jitter the PN spectrum cannot be calculated.

Instead of the histogram, the jitter function can be measured as a function of time. While many of the presented approaches are still developed to measure clock timing jitter of digital systems, here correlation information is captured, and therefore the corresponding spectrum can be calculated (see remarks on PSD estimation in Section 6.1). In general these approaches are based on the comparison of the signal's edges to either an external clean reference clock, resulting in TIE jitter, or against a delayed version of the signal itself, resulting in ctc jitter measurements.

The time difference measurement itself can be implemented digitally, for example with a flash TDC (Fig. 6.1 center right) [139, 140]: In this common architecture, the reference clock triggers a set of flip-flops, with its data inputs connected to subsequent stages of a delay chain. Therefore, at the rising edge of the reference, a snapshot of the signal's past is recorded in the flip-flops. Here, the resolution (i.e. bin size) is determined by the time delay of the delay elements. From the flip-flop data the position of the rising edges (i.e. the jitter function) can be obtained.

This basic concept has been improved in many details in several publications: For the flash-TDC also coarse and fine bins can be used in a range versus resolution trade-off [139]. Furthermore, a symmetric implementation of the flash-TDC might be employed to be able to measure in both directions of the reference edges [139]. The resolution of the TDC can be increased in different concept: First, a phase interpolator can be used in addition to the delay chain to achieve time shifts smaller than the delay by one delay element [140]. Second, Vernier delay techniques can be used in which not only one path is delayed but both with slightly different values by employing different load capacitances. To reduce the total runtime of the signal through the delay line, a hierarchical architecture can be used [141]. Third, oversampling techniques can be used to shape the quantization noise floor to higher frequencies, where it can be removed by filtering, for example by using phase interpolation [141]. In this approach, four 90° phase-shifted versions are created from both signal and reference. These linearly interpolate the jitter in two subsequent oscillation periods, such that the achievable sampling speed is essentially fourfold. Moreover, calibration techniques have been proposed to equalize bin width against process-voltage-temperature (PVT) variations [141]. A further indirect technique of digital time measurements is the use of a clocked comparator with a given threshold value (i.e. a 1-bit ADC) [142], where however sampling rates highly exceeding the signal frequency are needed.

For the readout of the flip-flops, several techniques are possible. They can be saved for later readout [139] or sent directly off-chip as an encoded binary number. In case a time frame longer than one oscillation period is recorded, multiple rising edge positions will be found, in which case a priority encoder (PE) can encode only the first occurrence [140]. From the jitter sequence the PN spectrum can be calculated via a Fourier transform. However, for the measurement in automated test equipment, this operation might be prohibitive due to time constraints. Therefore, approaches have been proposed, where only relevant frequency components are selected after the TDC via a filter, with the rms of the resulting signal being proportional to the selected spot noise [143].

Apart from the digital TDC implementation, the time difference measurement can be performed with analog circuitry. One such technique is to use charge pumps (Fig. 6.1 center left), which integrate charge on a capacitor [140, 144, 145], for example, with a positive sign when the signal is low and the reference high and vice versa. The voltage of the capacitor, which is reset every period, is then proportional to the time difference and can then be read out with an ADC. This architecture can be improved by using a programmable charge pump to improve measurement range and sensitivity and a programmable delay line to adjust for PVT variations [146].

6.2.2 Delta Jitter

In the discussed on-chip time-difference measurement techniques, a reference clock is always needed, independent of the architecture specifically chosen. Here, a stable reference clock, yielding TIE jitter data, has the disadvantage that it needs to be supplied externally rather than being available on-chip. For a completely independent solution, typically the ctc jitter measurement is chosen by comparing the signal under test with a delay version of itself. It will be shown that the latter approach suffers from the upscaling of TDC quantization noise, especially for high-frequency and low-phase noise oscillators.

6.2.3 Replica Method

In the replica method, the oscillator under test is compared to a second identical oscillator. The delta jitter measured is therefore the time difference between the positive edges of both oscillators. Under the condition that the noise caused by their devices is uncorrelated, the PSDs of both oscillators' phase functions are additive. Assuming both oscillators have comparable phase noise ($S_\phi^1(f) = S_\phi^2(f) = S_\phi(f)$) leads to the following relation between the PSD of the delta jitter S_τ^Δ and the spectrum of oscillator phase deviation S_ϕ:

$$S_\tau^\Delta(f) = \frac{S_\phi^1(f) + S_\phi^2(f)}{4\pi^2 f_0^2} = \frac{1}{2\pi^2 f_0^2} S_\phi(f). \tag{6.1}$$

Table 6.1 summarizes the reference choices and compares their respective relationship to the PN spectrum, as well as the drawbacks of the methods. The measurement of TIE jitter leads, according to Eq. 3.8, to a simple scaling relation to phase noise, is however as discussed not realizable on-chip. In the ctc jitter measurements obtained via delay line approaches, the effects of low-frequency noise do not accumulate over multiple periods, as in the case of TIE jitter. Therefore, the scaling relation to the PN spectrum (Eq. 3.12) shows a dependence on the observed phase noise frequency component f [86]. Here, low-frequency components close to DC are highly attenuated and would need to be scaled up accordingly. In reality, these components disappear below the TDC quantization noise floor, which after applying the scaling corrupts the resulting PN spectrum. While the generalized N-cycle jitter spectrum relaxes the attenuation issue, the problem is not solved in principle but rather transferred to lower frequency components. Furthermore, the N-cycle jitter spectrum exhibits strong attenuation not only close to DC, but now additionally at f_0/N and its multiples (zeros of the sine function). For delta jitter, the scaling factor is again independent of the measured frequency, causing no attenuation. It equals twice the TIE scaling factor, since here the two noisy oscillators contribute equally to the measured time differences. Although the integrated reference replica does make the technique independent from external stable references, it comes with a significant area overhead (especially for LC oscillator). This issue is addressed in the generalized approach for multiple-oscillator systems. Additionally in the delta jitter method correlated effects, such as temperature or supply voltage variations on a time scale much larger than the oscillation period, affect both oscillators equally and are therefore self-canceling. Whether this is a drawback or an advantage of the method depends on its intended application. For example, a monitoring structure for intrinsic noise benefits from this effect.

Table 6.1: Comparison of reference choices for jitter measurement: Time-interval-error (TIE), cycle-to-cycle (ctc) and delta jitter.

	TIE	ctc and N-cycle	Delta
Reference	stable reference	delayed signal	uncorrelated replica
Relation to $\mathcal{L}$	$\frac{1}{8\pi^2 f_0^2} S_\phi(f)$	$\frac{\sin^2(\pi N f/f_0)}{\pi^2 f_0^2} S_\phi(f)$	$\frac{1}{4\pi^2 f_0^2} S_\phi(f)$
Drawbacks	external signal needed	quantization noise upscaling	area-overhead (cancellation of correlated effects)

6.2.3.1 Simulation of Jitter Quantization Effects

To investigate possible differences in quantization effects for the various introduced jitter types, a synthetic noisy oscillatory waveform was analyzed based on the jitter definitions of Table 6.1 using MATLAB. For this purpose, first, a noisy phase function was generated with white, Gaussian characteristics using the *wgn*-function. For this function subsequently a Fourier transform was employed, and the frequency components scaled according to the phase noise characteristics expected for differential ring oscillators [32, 108, 147] ($\mathcal{L}(1\text{MHz}) \approx -90$dBc/Hz, with a flicker noise corner of $500\,\text{MHz}$). After transforming the phase function back to time domain (*ifft*) it is used to generate a noisy oscillatory waveform. For this an ideal ring oscillator waveform with frequency of $700\,\text{MHz}$ consisting of 21 harmonics is evaluated at the respectively phase-shifted points in time. For the delta jitter, a second uncorrelated waveform with identical statistical properties was produced. Subsequently, the positive edge positions and from these the different jitter types were determined. The jitter values were then discretized into bins, as would happen when measured with an on-chip TDC. Here, a bin width of $5\,\text{ps}$ was chosen, in accordance with values expected for the propagation delay of an inverter in current technologies.

The left side of Fig. 6.2 shows the evolution of the different jitter types over the simulated time of $100\,\mu\text{s}$ with their respective mean values subtracted. It can be observed that both TIE jitter and delta jitter wander over a wider range of values, since in their corresponding spectra the low-frequency components are dominant. The range of delta jitter values can be observed to be, as expected, roughly twice as large compared to the TIE jitter. The cycle-to-cycle jitter, on the other hand, is limited to a very narrow value band, several picoseconds around zero, which is caused by the attenuation of low-frequency components.

The quantization of the time series is plotted in the right side of Fig. 6.2. For the TIE and delta jitter, the range of values is large compared to the bin width and many different bins are activated.

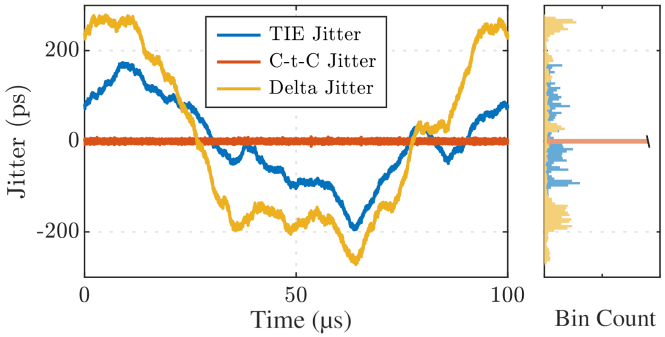


Figure 6.2: Evolution of different jitter types with time (left) and their corresponding binning (right). In the histogram of the cycle-to-cycle jitter the two center bins of the histogram are capped. Reprinted from [2] ©2023 IEEE.

In contrast to that, the ctc jitter values extend only over the range of four TDC bins, indicating that the quantization effects might have stronger impact.

The jitter spectra were computed from the time-domain data as discussed in Section 6.1. Here, the Bartlett method was used, as the generation of multiple sample PSDs is computationally inexpensive in simulation. The resulting PSDs were then related to the phase deviation spectrum with the corresponding scaling relation of Table 6.1.

Fig. 6.3 shows the calculated PN spectra. In black, the spectrum of the initial MATLAB-generated phase deviation is shown. Since measuring jitter is equivalent to sampling the phase deviations with the frequency of oscillation, aliasing of frequencies higher than f_0 is expected. This behavior is reflected in the spectrum calculated from the TIE jitter: For low offset frequencies, the spectrum fits to the oscillator phase spectrum very well, whereas a predictable deviation is observed when approaching the oscillation frequency. In the spectrum of the ctc jitter the effects of quantization are clearly visible: An offset to the expected spectrum is observed over almost the entire frequency range. The spectrum calculated from the delta jitter, on the other hand, is able to reproduce the phase deviation spectrum as accurately as the TIE jitter.

In further simulations it was observed that the quantization effects have a greater impact on the calculated PN spectrum for oscillators with lower phase noise (like typical LC oscillators) or higher frequency. In the first case, the phase deviations, and hence the jitter values, are smaller and, therefore, affected more by quantization. In the second case, the same effects are observed, since the phase deviations have less time to evolve between subsequent edges.

While a higher TDC resolution (e.g. by Sigma-Delta TDCs) or, as discussed, longer delay in the ctc jitter measurement (N-cycle jitter) can counteract the quantization effects arising with more spectrally pure and faster oscillators, these limitations are not solved in principle.

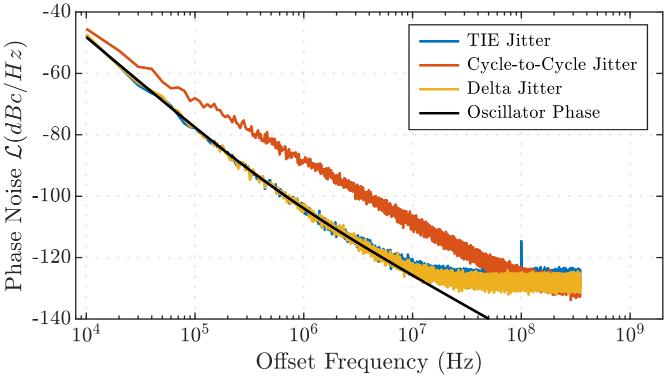


Figure 6.3: Phase noise spectra calculated from the different jitter types after quantization. Reprinted from [2] ©2023 IEEE.

6.2.3.2 Implementation of a Test Circuit

The robustness of the delta jitter method against quantization and its handling of correlated noise sources is investigated with a test circuit, which was designed and measured in a $16\,\mathrm{nm}$ FinFET CMOS technology. With the implemented circuit it is possible to measure the phase noise of both oscillators individually with high-accuracy off-chip laboratory equipment, and in addition to that, the delta jitter with an on-chip jitter measurement macro using a TDC. An overview of the complete system with schematics of selected subsystems is shown in Fig. 6.4.

The first components of the test circuit are the two ring oscillators of which the phase noise is to be measured. These consist of 17 differential inverter stages. While both oscillators share the same supply voltage net, their frequency can be tuned separately to allow for corrections of different oscillation frequencies due to process variations. This is accomplished with a bias voltage that controls the current through the differential stages. According to the simulation of the extracted layout, the outputs of the two ring oscillators oscillate between $450\,\mathrm{mV}$ and $800\,\mathrm{mV}$ with a frequency of $0.7\,\mathrm{GHz}$.

These signals are then processed by two AC-buffers (ACBs) to produce a rail-to-rail signal between $0\,\mathrm{V}$ and $0.8\,\mathrm{V}$ suitable for the following digital logic. Since these stages consist of comparatively small transistors to minimize the load on the ring oscillators, the drive strength of the signal must be amplified by subsequent drivers. These consist of seven inverter stages with increasing transistor sizes, additionally splitting the signal into two paths: One for off-chip phase noise measurement via the RF pads and one for on-chip jitter measurement. Special care was taken when designing the layout of the ACBs and the drivers, so that as little jitter as possible is added by this circuitry. A closer examination of different architectures has shown that in particular the first amplification stages of the driver are critical in that regard.

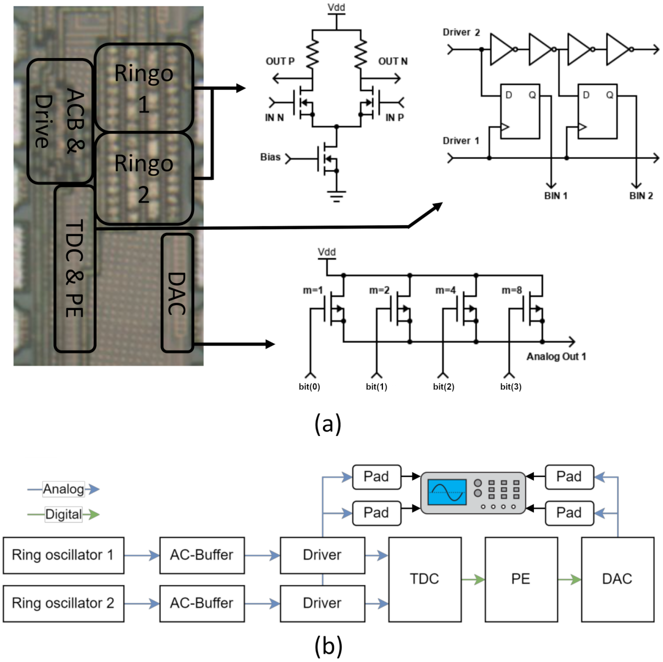


Figure 6.4: (a) Micrograph of the chip with schematics of the ring oscillator delay element, the first two bins of the time-to-digital converter, and the digital-to-analog converter. (b) Block diagram of the circuit. Reprinted from [2] ©2023 IEEE.

The measurement of delta jitter between both oscillators is realized with a flash TDC. It consists of 256 flip-flops that are triggered by the first oscillator. The signal of the second oscillator is connected to the flip-flop inputs via an inverter chain that delays the signal by a specific amount of time between the single stages. Therefore, each time the TDC triggers a snapshot of the second oscillator's past is stored in the 256 flip-flops from which the edge positions can be detected. Quantization is determined by the delay between two neighboring stages and has been simulated to be 5.1 ps for the architecture employed. Since the snapshot of the TDC covers a time longer than one oscillation period, it will contain multiple positive oscillation edges. The next stage, the PE, ignores all recorded edges except the most recent and encodes its position as an 8-bit binary number.

To retrieve this information and make it available for off-chip processing a DAC is used. It takes the binary number provided by the PE and converts it into a combination of two 16-level voltage signals that can be read out at the second pair of RF pads. In a complete on-chip implementation the DAC would be replaced by digital logic directly processing the PE output.

6.2.3.3 Test Circuit Measurement Results

To compare the characteristics of the different jitter types, both ctc and delta jitter were measured on the test circuit simultaneously. Wafer level probing (see Fig. 6.4(b)) was set up according to the measurement principles described in Section 5.2. Here, RF probes were used for the driver and DAC outputs, and DC probes for *vdd* and bias currents. To compensate for process variations, the frequency of both ring oscillators was matched as closely as possible by adjusting the bias current in the delay cells. The *Agilent Infiniium 92004Q* RF real-time oscilloscope was used to capture driver and DAC output waveform for a measurement time of 8 µs with a sampling rate of 80 GSamples/s.

From the recorded data, the ctc jitter was determined for both oscillators: First, the edge positions were calculated by interpolating the time points of threshold crossing. The ctc jitter was then calculated as the time difference between subsequent edges. The evolution of both oscillators' ctc jitter is shown in Fig. 6.5(a). Their apparent correlation is caused mainly by variations in the supply voltage.

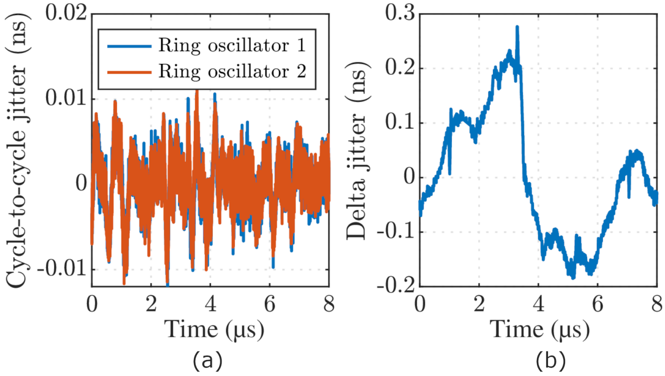


Figure 6.5: (a) Cycle-to-cycle jitter of both ring oscillators. (b) Delta jitter from TDC output. Reprinted from [2] ©2023 IEEE.

The on-chip TDC-recorded delta jitter was obtained from the output waveform of the DAC by mapping the voltage levels to their corresponding TDC bin. Data obtained from a stand-alone TDC characterization was used to determine the delta jitter for each bin. The remaining small frequency difference during the observation window results in a linear shift, which was subtracted in post-processing before spectral analysis. The resulting delta jitter is shown in Fig. 6.5(b). The correlated effects seen in the ctc jitter are canceled out and are not observed in the evolution of the recorded delta jitter values, which now depend solely on uncorrelated effects.

From the time series data the PN spectra were then calculated. For a clear comparison, the off-chip recorded ctc jitter was also quantized to 5 ps bins. The resulting ctc jitter of one ring oscillator and the delta jitter were then converted to a PN spectrum via the respective scaling relation. Due to measurement time constraints, both spectra were computed from a single measurement, such that the resulting PSDs are smoothed in frequency domain (Daniel method) to reduce the variance of the estimates. Although in principle the proposed method works for arbitrarily low offset frequencies, a limit is set in the current setup by the memory depth of the oscilloscope.

Fig. 6.6 shows the measured spectra, as well as the result of a *spectre* phase noise circuit simulation. For frequency components above 10 MHz, good agreement can be observed. However, on the lower end of the frequency range, the phase noise as calculated by the delta jitter method is considerably lower. This is because correlated disturbances between both oscillators do not appear in the spectrum due to self-cancellation. The delta jitter measurement results show the phase noise spectrum caused by the uncorrelated device noise, and therefore match more closely to the simulation.

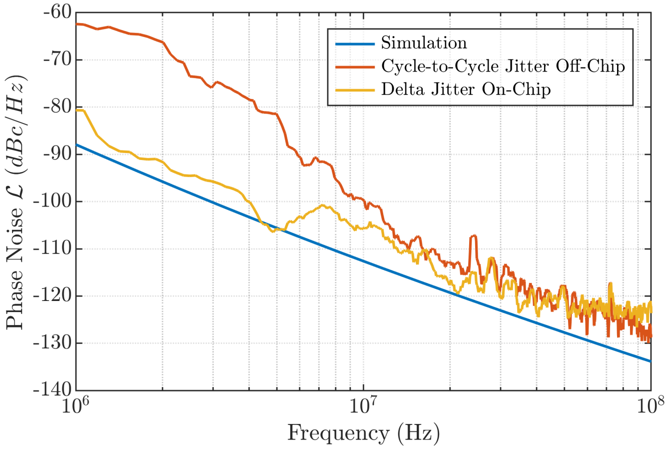
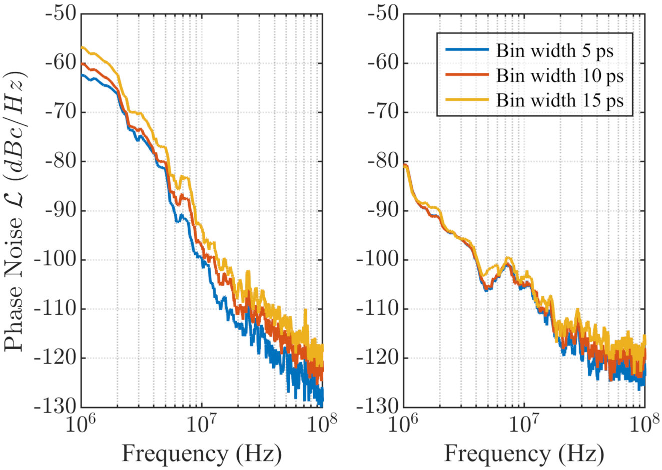


Figure 6.6: Comparison of the phase noise spectrum calculated from the cycle-to-cycle jitter of one single ring oscillator and from the delta jitter measured by the TDC with respect to simulation. Reprinted from [2] ©2023 IEEE.

Furthermore, the results of the simulation in Section 6.2.3.1 are confirmed when comparing the measured ctc jitter range to that of the delta jitter. As can be observed in Fig. 6.5, in spite of the rather short measurement time the latter evolves over a time range of several hundred picoseconds, making quantization into bin width of approximately 5 picoseconds negligible for the overall evolution of the delta jitter. The ctc jitter, on the other hand, evolves only over the range of approximately 20 picoseconds, indicating that quantization effects may arise in the spectrum.

A detailed investigation on how the measured PN spectra react to quantization is shown in Fig. 6.7. The TDC resolution is artificially reduced by merging neighboring bins, resulting in bin widths of $5\,\mathrm{ps}$, $10\,\mathrm{ps}$ and $15\,\mathrm{ps}$, respectively. For the ctc jitter (Fig. 6.7(a)) an increased bin width causes an offset in the measured phase noise over the entire frequency range (as expected from simulation). While for the delta jitter (Fig. 6.7(b)) an offset is observed for far-out PN, the lower frequency components are more robust against quantization and therefore can be measured accurately even with a TDC of lower resolution.



(a) Cycle-to-cycle

(b) Delta

Figure 6.7: Quantization effects in phase noise spectra calculated from (a) cycle-to-cycle jitter and (b) delta jitter. Reprinted from [2] ©2023 IEEE.

Our measurement and simulation results show that using the delta jitter concept phase noise due to device noise can be measured decoupled from correlated noise sources. Moreover, it is shown that the method achieves quantization-robust on-chip measurements without a stable reference.

6.2.4 Multiple Local Oscillator Method

The main drawback of the replica method presented is that an uncorrelated replica needs to be implemented on-chip, taking up valuable chip real estate. Some applications already contain by design multiple local oscillators, albeit of differing nominal frequency. An example for such an architecture are multi-band transceiver with multiple LOs, which aim to increase the aggregated bandwidth by using multiple distinct frequency ranges (e.g. sub-6-GHz and millimeter-wave frequency bands in case of 5G) [23, 148].

The delta jitter concept can be generalized to two oscillators of different frequencies f_1 and f_2 to achieve quantization-robust on-chip phase noise measurements with minimal area overhead. In this case, the measured quantity is again the time difference between the positive edges of the oscillations. To avoid double counting, the slower LO (hereinafter LO1) is the reference for the time difference measurement to the previous rising edge of the faster LO (hereinafter LO2). If the oscillation periods T_1 and T_2 of both oscillators LO1 and LO2 are not an integer multiple, a deterministic shift of the oscillation edges of $mod(T_1, T_2)$ occurs with every delta jitter measurement. This movement of the edge positions of LO2 through the period of LO1 can be observed in the top of Fig. 6.8. To reveal the delta jitter due to random fluctuation, this deterministic effect must be subtracted. Hence, the accumulated shift of $mod(N * mod(T_1, T_2), T_1)$ is subtracted from the N^{th} measured delta jitter value (see bottom of Fig. 6.8). For this illustration LO1 is assumed to be noiseless (without loss of generality), and for LO2 both the case of a noiseless oscillation and a sinusoidal phase modulation is shown.

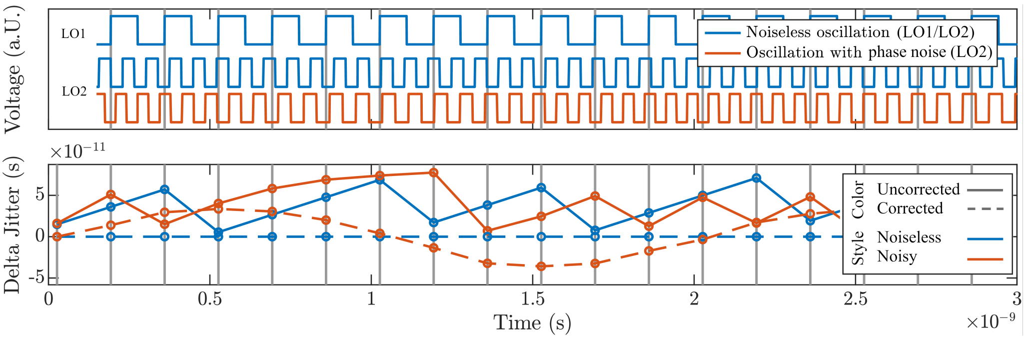


Figure 6.8: (Top) Waveform of the oscillation of two local oscillators, where LO1 is always noiseless and LO2 may contain a sinusoidal PN component. (Bottom) The corresponding delta jitter between LO1 and LO2 before and after correction for deterministic shifts. Reprinted from [3] ©2024 IEEE.

Once the deterministic shift is subtracted the delta jitter PSD can be related to the oscillators' PN spectra, which in this case takes the form of a frequency-weighted sum:

$$S_\tau^\Delta(f) = \frac{\mathcal{L}_1(f)}{2\pi^2 f_1^2} + \frac{\mathcal{L}_2(f)}{2\pi^2 f_2^2}. \tag{6.2}$$

When the phase noise of a single LO is of interest, the delta jitter can be measured between at least three LOs in a ring-wise manner. Eq. 6.2 can then be used to set up a system of equations that can be solved for the PN $\mathcal{L}_i(f)$ of each single LO.

Quantization errors introduced by TDCs in on-chip delta jitter measurements can lead to the fact that even hypothetical noiseless oscillations exhibit nonzero delta jitter after the correction algorithm is applied. While the specific form of this quantization error function depends on the nominal frequencies of both oscillators (specifically, the modulus of their periods) and the bin size, its amplitude is limited to one bin width. This also limits the effect of quantization noise in the delta jitter PSD and consequently the frequency-weighted PN spectrum to a constant noise floor, which can only be observed for high-frequency components where the PN of the measured oscillators is low.

6.2.4.1 Implementation of a Test Circuit

The feasibility of delta jitter measurements to quantify phase noise in systems with oscillators of differing frequency is investigated with a proof-of-concept test circuit designed and measured in a 16 nm FinFET CMOS technology. With the implemented circuit, it is possible to measure the phase noise of the oscillators with high-accuracy off-chip laboratory equipment, as well as the delta jitter with an on-chip jitter measurement macro using a TDC. An overview of the complete system is shown in Fig. 6.9. Although the architecture is similar to the test circuit presented in Section 6.2.3 for the replica method, there are differences, which are highlighted in the description of the respective subsystems.

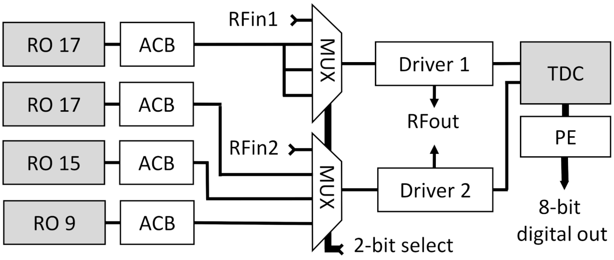


Figure 6.9: Block diagram of test circuit concept. Reprinted from [3] ©2024 IEEE.

The system contains in total four ring oscillators, of which the single stages are implemented as the same differential structure as in the replica method experiment (depicted in Fig. 6.4). Here, to achieve different oscillation frequencies, a different number of stages is used: Two ROs are implemented with 17 stages, one is slightly faster with 15 stages, and one has almost twice the frequency with 9 stages. Again, ACBs are placed to obtain a rail-to-rail signal for the following digital logic.

A new feature of the multi-LO test circuit are two 4:1 multiplexer (muxes), which are used to select two signals for the delta jitter measurement, allowing four different configurations: First, for TDC characterization the time difference between two signals coming from an off-chip input can be measured. The remaining mux configurations enable the measurement of delta jitter between two ring oscillators: While one of the 17-stage ring oscillators is always used as a reference, the second oscillation can be chosen between a nominally equal frequency, or one of the faster ring oscillators. Additional (not depicted) muxes supply only those ring oscillators with power that are measured, in order to not introduce additional switching noise.

As before, driver circuits after each mux increase the drive strength and split the signal: One path can be read out off-chip with high-precision laboratory equipment, and one path is routed to the on-chip jitter measurement macro.

The time difference between the positive edges of the signals is measured with a flash TDC with an identical architecture as in the replica method test chip (depicted in Fig. 6.4). In contrast to the replica method test chip, here no ADC is used to compress the resulting 8-bit binary number to two 16-level signals. In the increased available chip area, each bit is rather individually driven to a signal pad to reduce readout complexity. In application, this 8-bit signal again constitutes the interface for further digital processing in BISTs or power/PN optimization schemes.

6.2.4.2 Test Circuit Measurement Results

The general measurement setup follows the principles described in Section 5.2. A symbolic representation and a micrograph of the test circuit contacted for wafer-level probing can be seen in Fig. 6.10. The RF inputs are contacted via dual channel RF probes with a Keysight 81134A pulse generator, where the delay between the channels can be adjusted in $1\,\mathrm{ps}$ steps. The RF output is connected via dual channel RF probes with an Agilent Infiniium 92004Q RF real-time oscilloscope, used to capture the output of the two drivers for a measurement time of $100\,\mathrm{\mu s}$ with a sampling rate of 80 GSamples/s. Alternatively, the Rohde & Schwarz FSWP Phase Noise Analyzer can be connected for high-precision PN measurements. Custom-made multi-contact probes are used to connect to ground, DC supply and bias voltages, and digital output signals (*Cascade Michrotech Unity Probes*). From here, the 8 digital output bits are captured with a Tektronix MSO58 8-channel mixed-signal oscilloscope, which is triggered synchronously to the analog oscilloscope to capture the same time frame of $100\,\mathrm{\mu s}$ with a sampling rate of 12.5 GSamples/s.

First the TDC is characterized using a pulse generator, where the delay between the two channels is varied while recording the output bin of the TDC. Here, a good linearity of the TDC was found with a bin width of $7.45\,\mathrm{ps}$.

The first delta jitter measurement was performed by passing the signals of the two 17-stage ring oscillators (both with a frequency of $0.75\,\mathrm{GHz}$) to the TDC and RF output. The activated bins are determined from the waveform recorded by the digital oscilloscope, and with the determined

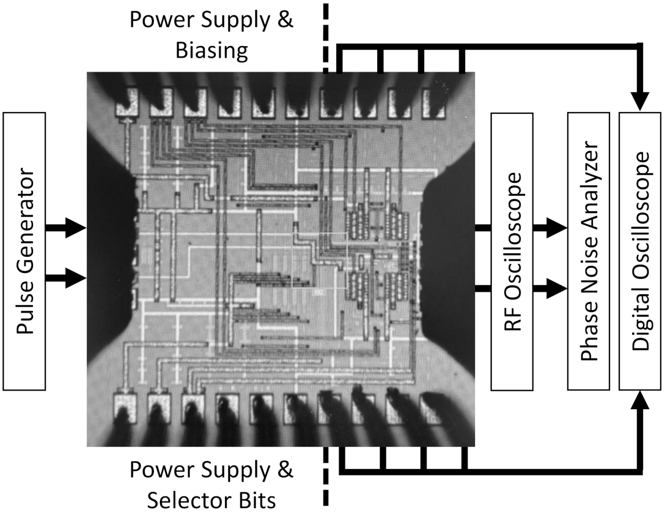


Figure 6.10: Chip micrograph with symbolized measurement setup. Reprinted from [3] ©2024 IEEE.

bin width, the delta jitter was calculated. From this time-domain data the PSD was obtained and is shown in Fig. 6.11. The lower frequency limit is hereby determined by the length of the recorded signal time (i.e. the memory depth of the oscilloscope) and the upper limit by the delta jitter sampling rate (frequency of the slower oscillator). As a reference, the delta jitter spectrum as expected by the direct phase noise measurements with the Phase Noise Analyzer and related to the jitter spectrum by Eq. 6.1 is also depicted. Here, a good overall fit can be observed without evident quantization effects. The apparent discrepancy in the vicinity of $1\,\mathrm{MHz}$ is caused by the applied smoothing (Daniel method) of the periodogram in frequency domain, which broadens the observed spurs.

The concept of delta jitter with oscillators of different frequency was tested by setting the muxes to pass through signals of the ring oscillator with 17 and 15 stages, resulting is oscillation frequencies of $0.74\,\mathrm{GHz}$ and $0.82\,\mathrm{GHz}$, respectively. The delta jitter from the on-chip TDC was recorded as before (DJ on-chip). Furthermore, for comparison without TDC quantization effects, the same quantity was calculated from the oscillation waveforms recorded by the RF oscilloscope (DJ off-chip). For both delta jitter measurements the deterministic edge shifts were subtracted as described in Section 6.2.4 to separate the purely random effects. Subsequently, the PSD was calculated for both on-chip and off-chip delta jitter measurements and compared to the frequency-weighted phase noise sum of the direct phase noise measurements (according to Eq. 6.2) and are displayed in Fig. 6.12 (top). The overall evolution again matches between the delta jitter measurements and the reference, where the spurious tones at and above $100\,\mathrm{MHz}$ are also reproduced. An offset between the on-chip and off-chip delta jitter PSDs can be observed in the far-off PN (the quantization error is shown Fig. 6.12 bottom), which is caused as illustrated before by the quantization of the TDC. For close-in PN, on the other hand, on-chip and off-chip measurements deliver the same results, without quantization effects, and therefore can be used as an indicator of close-in PN stability.

Lastly, the delta jitter measurement was tested using the ring oscillator with 17 stages and 9 stages, resulting in frequencies of $0.74\,\mathrm{GHz}$ and $1.43\,\mathrm{GHz}$, respectively. Data recording and processing was conducted as in the previous experiment, resulting in the delta jitter PSDs displayed in Fig. 6.13 (top). Again, a good match is achieved throughout the whole frequency range, with a small offset in far-off PN due to quantization errors in the on-chip delta jitter measurement (see Fig. 6.13 bottom).

6.2.5 Conclusion

The simulation of different jitter types shows that for certain combinations of phase noise, oscillation frequency and TDC resolution, the quantization of the measured jitter data can prevent a meaningful phase noise measurement. Therefore, an on-chip macro was designed that measures the time difference between the positive edges of the tested LO and those of an identical replica. The resulting *delta jitter* data enables quantization-robust phase noise measurements without a stable reference source, as validated in test circuit fabricated in $16\,\mathrm{nm}$ FinFET CMOS. Moreover, measurements show that the applied method is able to cancel correlated effects, and therefore enables the on-chip monitoring of the phase noise caused by intrinsic device noise.

A drawback of the replica method is the area overhead needed for the second oscillator. As a generalization, a quantization error robust on-chip PN monitoring concept was proposed for systems containing multiple high-frequency low-PN LOs. The technique compares the edge positions of the oscillations of possibly of different frequency and was implemented in a test circuit designed and manufactured in a $16\,\mathrm{nm}$ FinFET CMOS technology. Our measurements show a good agreement of the on-chip measured jitter spectra with the frequency-weighted phase noise measurements by high-precision laboratory equipment. Quantization noise is hereby not scaled up and therefore does not distort measurements results at close-in frequency components. While the presented test circuit operates at comparatively low frequencies, the concept extends to higher frequency ranges. Depending on the LOs' frequencies, phase noise and desired frequency measurement range, the TDC resolution/architecture (and therefore the area overhead and power consumption of the macro) need to be adjusted.

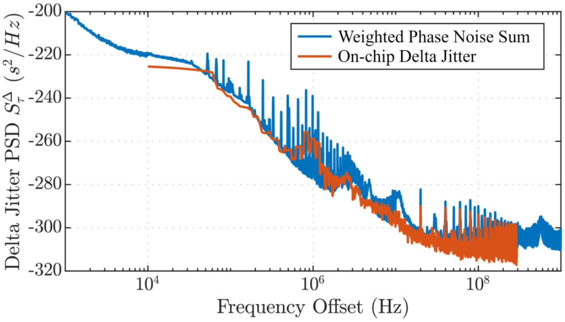


Figure 6.11: Delta jitter spectrum measured between two 17-stage ring oscillators. Comparison of on-chip measurement with the expectation from direct phase noise measurement. Reprinted from [3] ©2024 IEEE.

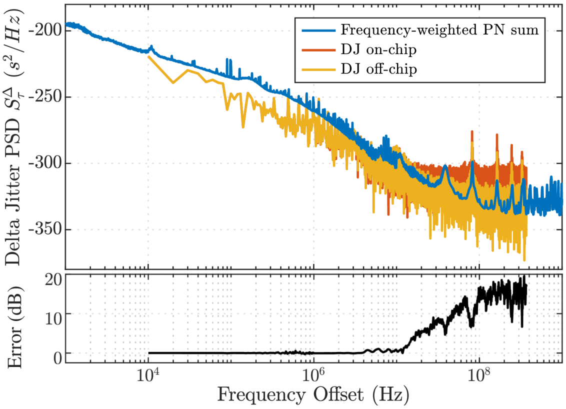


Figure 6.12: (Top) Delta jitter spectrum between a 17- and a 15-stage ring oscillator and reference by direct phase noise measurement. (Bottom) On-chip TDC quantization error. Reprinted from [3] ©2024 IEEE.

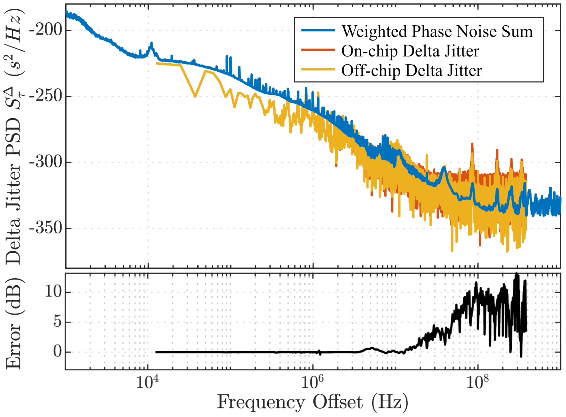


Figure 6.13: (Top) Delta jitter spectrum between a 17- and a 9-stage ring oscillator and reference by direct phase noise measurement. (Bottom) On-chip TDC quantization error. Reprinted from [3] ©2024 IEEE.

6.3 On-chip Flicker Noise

As discussed in Section 1.1.1, a high-throughput on-chip flicker noise measurement macro can serve as a valuable complement to the characterization methods currently used in fabrication monitoring, technology modeling and assessment. Therefore, a novel concept, termed flicker noise monitor (FNM) is presented, exhibiting high measurement sensitivity due to cross-correlation techniques.

Parts of this section are extracted from a submitted publication [6].

6.3.1 Previous Approaches

Only few techniques have been published, which allow to measure the noise spectrum of a DUT with an on-chip solution. The presented architectures are based on a direct measurement of current fluctuations or calculate the device noise spectrum from the upconverted phase noise of oscillators. Notably in the later case phase noise is not used merely as a qualitative proxy measurement, but rather as a vehicle to calculate the specific quantitative current noise spectrum of the DUT.

The first approach is technically not an on-chip solution, but should still be mentioned here as a method to increase the area efficiency of off-chip flicker noise measurements. In a typical off-chip laboratory measurement each single DUT is connected to two ground-signal-ground pads (totaling six pads), which constitute the majority of the test structure area usage. Instead, an addressable DUT array is used in the proposed approach [68], so that the signal pads can be shared for all tested devices. Switches consisting of pairs of NMOS and PMOS transistors connect the terminals of the DUTs with the common signal nets. One out of 2048 DUTs can be selected via an external 11-bit signal, which is decoded with on-chip digital logic to provide the correct control signal to the switches. An important aspect of this design is the sizing of the switch transistors, which must provide a low resistance in the on-state and exhibit minimal noise contributions (i.e. they must have wide but short channels). Separate classical test structures can be used as a reference to verify the measured results.

The second method is similar in concept, but aims for a full on-chip implementation by integrating both bias generation and flicker noise measurement in the macro [149, 150]. Here, again multiple DUTs of possibly different geometry and threshold voltage are arranged in an array. A bias generating circuit applies a defined drain voltage and a defined drain current to the DUT, where for DUT selection again switches can be used [150]. Another approach is to implement the bias generation in a way to allow individual addressing of all DUT terminals, such that all

DUTs can be connected in parallel with the nonselected DUTs being switched off ($v_g = 0\,\mathrm{V}$) during measurement. A replica biasing scheme is used with an external reference current to generate clean bias conditions. The voltage noise measurement is conceptually equal to an off-chip measurement: The channel voltage (here at the source node) is amplified by an LNA and subsequently digitized with an ADC. The LNA has a adjustable gain in a range versus resolution trade-off to adapt to different DUT variants. Subsequently, a $100\,\mathrm{MHz}$ oversampling $\Sigma\Delta$-ADC is used, which achieves a low noise floor in the measurement band ($1\,\mathrm{kHz}$-$100\,\mathrm{kHz}$) due to noise shaping. Another implementation [150] uses an ADC based on a VCO relying on voltage-to-phase conversion (similar to the proposed FNM). The measured data is sent off-chip in real time and the noise spectrum calculated with an FFT. An on-chip decimation filter reduces the amount of transferred data to relax memory requirements of the off-chip evaluation system. A main drawback of the approach is that the noise measurement circuitry consists of the same devices as the DUTs. To ensure therefore that noise added by the biasing, LNA and ADC can be neglected, careful noise analysis is necessary. The measurement circuitry is tailor-made to the DUT and extensive redesign is necessary for new (especially lower noise) DUTs. Furthermore, the design is orders of magnitude more complex than the previous method and can therefore only be employed on more mature process nodes, where no yield problems arise. Lastly, for certain biasing circuits, the bias conditions cannot be chosen from a continuous set of values, but are limited to a predefined set.

The third type of technique measures the phase noise of a ring oscillator to calculate the underlying flicker noise of the devices. In one implementation a relation is established between the phase and flicker noise corner frequencies [151] for a specific ring oscillator architecture. By deriving an approximation of the oscillator's ISF (see Section 3.2.3) this relation can be made explicitly dependent on circuit parameters. However, some of the parameters are still unknown, such as the asymmetry factor between the edges' rise and fall slopes and the proportionality factor between the signal slope and the stage delay time. The concept therefore implements multiple ring oscillators with varying stage number and the possibility to tune the rise and fall times of the signal. Using the results of multiple phase noise corner frequencies the unknown parameters can be eliminated and the device noise corner calculated. A second implementation [152] focuses on calculating the thermal noise level from phase noise by using a ring oscillator with inverters of two different sizes. This has the advantage that the devices of the small inverters, which mainly contribute to phase noise, are held at a constant bias during noise upconversion. A third implementation [153] uses flip-flops and counters to measure changes in the frequency of a ring oscillator under test and a reference. The focus here lies in finding stepwise changes due to RTN. Although these circuits can be designed in such a way that only one specific transistor variant contributes nonnegligibly to phase noise, still only an average measurement over all equivalent contributing transistors (and in the first and third implementation over multiple bias conditions) is obtained. Furthermore, instead of obtaining the complete noise spectrum, only single parameters are measured (flicker noise corner frequency, average thermal noise level, or time constants of RTN traps, respectively).

6.3.2 Proposed Flicker Noise Monitor Technique

In the proposed measurement technique the DUT's flicker noise is measured via its effects on the phase fluctuations of two isolated ring oscillators, where unwanted effects of the sensor circuitry are suppressed by cross-correlation (see Fig. 6.14). The fact that vanishingly small voltage fluctuations accumulate to measurable deviations in the oscillator's phase is utilized to build a precision ADC. In contrast to other ADC architectures, this approach eases the requirements on the sensor circuitry's manufacturing and model accuracy. Compared to the previous techniques, the proposed architecture combines three main advantages presented in the following.

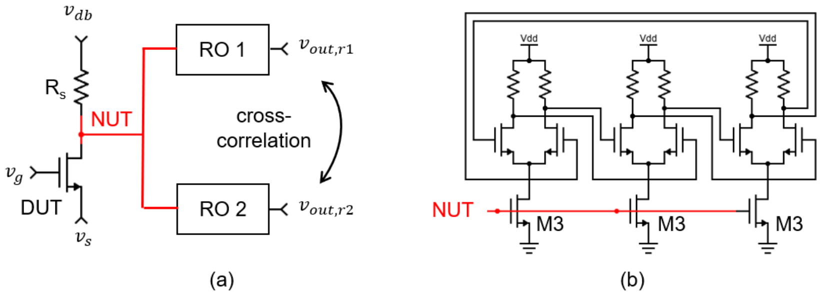


Figure 6.14: (a) Schematic overview of the proposed concept. Current noise of the DUT is upconverted to phase noise of (b) two isolated ring oscillators via the constant biasing of the differential delay cells. Additional capacitors to tune the oscillation frequency are here omitted. Effects of the sensor circuitry are removed via cross-correlation.

First, the DUT experiences steady bias conditions, allowing distinct noise characterizations of a single device under freely selectable bias conditions, that is, without averaging over multiple devices or bias conditions. As can be seen in Fig. 6.14(a) a constant bias can be set at the gate and source of the transistor directly via pads to the voltages v_g and v_s, respectively. The drain terminal is connected in series to a resistor, where a constant drain bias v_{db} is applied. Consequently, a steady voltage will appear at the net under test (NUT), that is at the drain of the DUT. The NUT voltage is used to supply the differential delay stages of two ring oscillators with a bias voltage (see Fig. 6.14(b)). Since the DUT is placed in a separate deep n-well v_g, v_s and v_{db} can be shifted with respect to *vss* and *vdd* of the ring oscillator to set a specific required bias voltage.

The second advantage, representing the core enhancement of this work, consists in a cross-correlation technique between the two ring oscillator signals to increase measurement sensitivity and therefore enable the characterization of low-noise DUTs (e.g. large transistors) and low-noise bias conditions (e.g. at low drain current): Current noise of the DUT drops off at the resistor R_s as voltage noise on the NUT, which is in turn upconverted to phase noise of both ring oscillators. Their overall phase fluctuations are caused by common, correlated noise sources (i.e. by the DUT, but also by the series resistor) and the uncorrelated noise of the ring oscillators' internal devices. The latter contributions can be suppressed in a measurement time versus sensitivity trade-off by averaging over many cross-correlation spectra of both ring oscillator signals. Furthermore, noise preamplification stages, potentially contributing parasitic noise, can therefore be omitted.

The third enhancement lies in a novel derivation of mathematical connection between the oscillators' phase noise spectrum and the corresponding DUT flicker noise spectrum: Using an approach based on Floquet theory (see Section 3.2.4) the flicker noise spectrum as a function of frequency can be calculated, instead of merely obtaining the flicker noise corner frequency. The approach moreover enables a sensitivity calibration of the FNM reducing reliance on model accuracy.

The next section presents more details on specific test chip implementation of the FNM.

6.3.3 Test Chip Implementation

Based on the presented core concept two test chips have been produced in $14\,\mathrm{nm}$ and $16\,\mathrm{nm}$ FinFET technology nodes, respectively. The first experiment serves as a proof of concept, where a single DUT can be characterized with the proposed FNM technique, as well as for verification with conventional off-chip laboratory equipment. In a second test chip the FNM concept is implemented with multiple DUTs which can be individually addressed to demonstrate the feasibility of fast, area-efficient high-volume characterization.

6.3.3.1 Proof-of-concept Experiment

The proof-of-concept experiment serves to verify the FNM concept by comparing the obtained results to conventional off-chip laboratory measurements. It represents the most elementary implementation possible of the proposed technique. Its block diagram is therefore given by the representation in Fig. 6.14, where only ACBs and drivers are added to amplify the ring oscillator output signals for wafer-level probing. The layout is shown in the chip micrograph of Fig. 6.15: The DUT with the series resistor is placed in the center. This structure can be contacted individually via the corresponding source (S), gate (G), and drain bias (DB) pads. To the left and right of the DUT the two ring oscillators are placed symmetrically, each with an ACB and driver block to drive the signal to the pads S1 and S2. Furthermore, pads are placed on the top and bottom for a separated power supply of the circuit blocks.

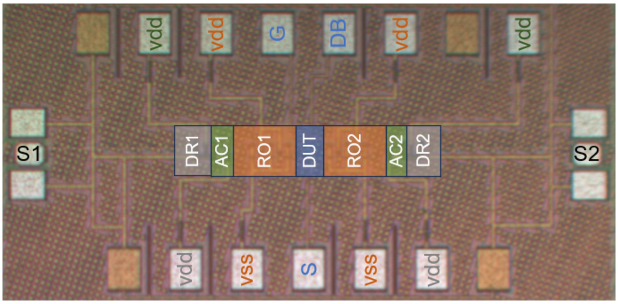


Figure 6.15: Chip micrograph of the proof-of-concept test chip with circuit blocks highlighted. The design consists of the device-under-test (DUT), two ring oscillators (RO) with their corresponding AC-Buffer (AC) and drivers (DR).

The experiment is carried out with two different DUTs: An RF transistor with the minimal available area (hereinafter $\mathrm{DUT_s}$), and a scaled up transistor, where the channel length and width are increased proportionally (hereinafter $\mathrm{DUT_l}$). Hence, both transistors are expected to exhibit comparative DC characteristics with larger flicker noise for the smaller $\mathrm{DUT_s}$. For the resistor in series with the DUT, a value of $1\,\mathrm{k}\Omega$ is chosen. Large resistances are here preferable to increase the sensor's sensitivity, since the voltage fluctuations on the NUT, and therefore the ring oscillators' upconverted phase noise scale with R_s for a given DUT current noise. This argument still holds even with the increasing thermal noise of the resistor, since this unwanted noise floor on the NUT only scales with $\sqrt{R_s}$. The upper boundary of the resistance value is set by reliability considerations, since large resistances call for large externally applied voltages.

The two ring oscillators consist of three differential delay stages, as depicted in Fig. 6.14(b). For all delay stages, the gate of the current biasing transistor M3 is connected to the NUT by a ground-shielded connection to avoid interference from nearby signals. To increase sensitivity, transistors with long and wide channels are chosen for both M3 and the differential pair to minimize flicker noise and therefore the ring oscillator intrinsic phase noise. Resistors of $500\,\Omega$ are chosen to ensure full switching of the stage, as well as saturation of M3. According to simulation with layout parasitic extraction, the frequency of the ring oscillator is $0.7\,\mathrm{GHz}$. This frequency should not be set too low since it corresponds to the upper frequency limit of the measured noise spectrum and not too high due to bandwidth and sampling rate limitations of the laboratory equipment. Any noise source influencing both ring oscillators (other than the DUT) must be avoided, since it cannot be suppressed by cross-correlation and therefore limits the sensitivity. To achieve isolation, both ring oscillators are placed in separate deep n-wells. Furthermore, the *vss* and *vdd* supply voltages are not shared, but are connected to separate pads. To avoid asymmetric loading when tapping the signal, the ring oscillators use a stage fan-out of 2.

A subsequent amplification is needed for wafer-level probing: Since the ring oscillator output signal does not reach *vss* due to the voltage drop at the biasing transistor, ACBs are used to achieve a rail-to-rail oscillation. The following drivers consist of several inverter stages with increasing drive strengths. Here, only the *vdd* supply voltages are separated, while the *vss* supplies are merged to a common ground connection. In case of the amplification circuitry a common supply net is viable, since noise effects outside of the oscillator feedback loop do not accumulate in the phase conversion and therefore constitute a negligible noise floor.

Decoupling capacitors are used at the *vdd* and *vss* pads to stabilize the supply voltage. For the gate, drain bias and source pads, on the other hand, these are omitted to avoid low-pass filtering of noise during the off-chip validation measurements.

6.3.3.2 Multi-DUT Experiment

The multi-DUT experiment serves to demonstrate the feasibility of the FNM concept for fast, area-efficient, high-volume characterization. Building on the proof-of-concept design, two enhancements are implemented: As can be seen in Fig. 6.16(a) multiple DUTs including the evaluation circuitry, collectively hereinafter referred to as a test unit (TU), are placed in parallel and can be selected via a shift register (SR). Since the area per test unit is small (see chip micrograph in Fig. 6.16(b) and (c)) and the number of pads does not scale, high-density characterization circuits can be implemented. As a further enhancement, the phase measurement is moved on-chip with TDCs. In contrast to driving out the ring oscillator waveform, this approach has several advantages: First, once the phase information is digitized, it is robust against errors from subsequent multiplexing and driving circuitry. Second, it reduces the amount of data that needs to be read out from the chip, since only phase information is relevant. This ultimately increases readout and evaluation speed. And third, it prepares the data for possible further on-chip evaluation circuitry. According to simulation, the quantization noise by the TDC only has an effect for frequencies higher than the flicker noise range of interest. Moreover, a quantization noise suppression using the cross-correlation technique is possible, since it constitutes an uncorrelated noise source between RO1 and RO2.

In each test unit a DUT is placed with its corresponding series resistor R_s. As before, these are placed in a deep n-well for isolation and the possibility to shift biasing with respect to the supply voltages (see Section 6.3.4.4). The source, gate and drain bias terminals of all TUs are connected in parallel to pads with decoupling capacitors. In 12 test units (TU14-TU25) identical DUTs of the smallest available transistor geometry and of the standard threshold voltage are placed. The value of the corresponding series resistors is chosen according to the considerations mentioned above to be $4.1\,\mathrm{k\Omega}$. The other test units contain DUTs with size and threshold voltage variations.

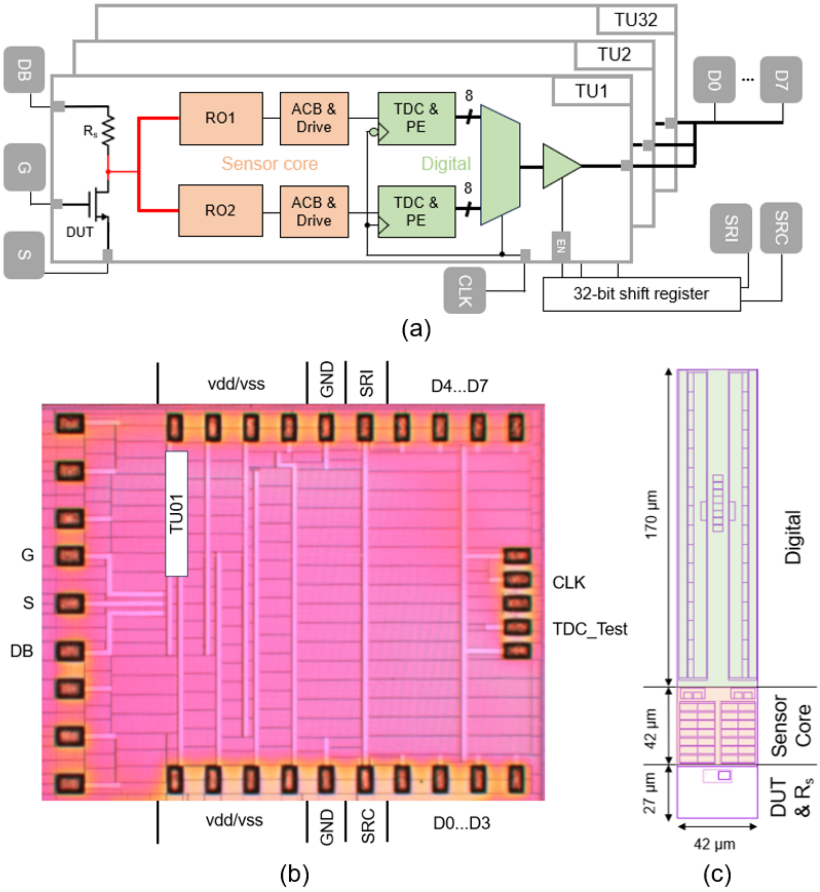


Figure 6.16: (a) Block diagram of the multi-DUT experiment. 32 test units (TUs) are placed in parallel and can be selected via a shift register. Each TU contains a DUT with series resistor, the noise sensor core (i.e. two ring oscillators (ROs) with AC-buffers (ACBs) and drivers), and the digital evaluation logic (i.e. time-to-digital converters (TDCs), priority encoders (PEs), multiplexers and tri-state buffers). (b) Micrograph of the chip with one test unit highlighted. (c) Layout of one test unit with sub block sizes.

To ensure all DUTs stay withing safe operating voltage limits at all bias conditions, the resistors are scaled according to the respective maximum DUT current.

The subsequent ring oscillators of the sensor core are designed according to the same considerations as for the proof-of-concept experiment. This notably includes separate *vdd*/*vss* nets and pads, as well as deep n-wells for improved isolation. As before, the output signal is then processed by ACBs to achieve a rail-to-rail oscillation suitable for the following digital logic. In the next step, inverters with increasing channel widths are used to drive the relatively high capacitive load of the following TDC.

To measure the phase noise of the ring oscillator signal an on-chip a TDC is used to determine the time points of the oscillations' positive edges. At these instances, the oscillation phase is uniquely defined as it is unaffected by amplitude noise (see Section 3.2). In this test chip, as in the delta jitter experiments in Section 6.2, a simple flash-TDC architecture is used (see Fig. 6.4). It consists of 256 flip-flops, which are in this case triggered by an external clock signal. The two ring oscillator signals coming from the drivers are connected to the flip-flop inputs via an inverter chain, delaying the signal from stage to stage. Therefore, when the TDC is triggered, a snapshot of the oscillators' past is stored in the 256 flip-flops from which the edge positions can be detected. The bin width is determined by the buffer delay, which according to simulation is in the range of $8\,\mathrm{ps}$ for the employed architecture, giving a dynamic range of around $2\,\mathrm{ns}$. Since this is longer than one oscillation period, the stored time frame will contain multiple positive oscillation edges. Therefore, a PE is used, which ignores all recorded edges except the most recent one and encodes its position as an 8-bit binary number.

The two 8-bit buses obtained from the TDCs of both ring oscillators are then merged by a multiplexer to reduce the number of required output pads. The input selection is controlled by the clock signal such that for each half clock period the TDCs' output signals are alternatingly forwarded. This operation essentially halves the number of bits by doubling the data rate. Here, it needs to be considered that after triggering the TDC the signals need time to propagate through the logic of the TDC and PE. A time shift of half a clock period between the TDCs is therefore introduced, by triggering one TDCs on the falling edge and one on the rising edge. The multiplexer is connected in such a way that the rising-edge triggered TDC is forwarded during a logical clock low, and vice versa, giving the signals time to settle before being forwarded.

The multiplexer output is then processed by a tri-state buffer: If the enable bit of the test unit is a logical high the multiplexer output is written on a 8-bit bus shared across all test units. In case the test unit is not enabled, the buffer is in a high-impedance state, permitting other test units to write on the bus. Lastly, drivers are used to amplify the signals to 8 output pads.

For test unit selection, a shift register is used. The data is populated via the external shift register clock (SRC) and data-in (SRI) signals. Apart from setting the tri-state buffer to a high-impedance state, a low enable bit will additionally switch off other circuit blocks of the test unit to not disturb the measurement of the activated DUT: The differential delay cells of both ring oscillators contain an additional transistor in series with M3 to enable or disable the ring oscillator. To avoid correlated noise effects in both ring oscillators via the enable signal, the enable bit from the shift register is passed through several buffers powered by the ring oscillators' separate *vdds* before contacting the delay cell. Furthermore, using digital gates, the external clock signal is only passed to the TDCs if the corresponding test unit is enabled.

In addition to the functionality described above, a *test mode* of the test units' TDCs can be activated. By setting a dedicated bit on the shift register, instead of the ring oscillator signal an external test pulse is transferred to the data input of the TDC, allowing to characterize the accuracy (bin width, nonlinearity, etc.) of the TDCs.

6.3.4 Measurement Methodology

From the ring oscillator waveform (specifically from its phase information), the flicker noise spectrum of the DUT can be calculated. The required measurement steps and evaluation methodology are presented in detail for the proof-of-concept experiment, and the necessary adjustments for the multi-DUT FNM thereafter. The measured data of an exemplary DUT are used for illustration with statistical results for many devices and in-depth analysis presented in Section 6.3.5.

6.3.4.1 Laboratory Setup

For the proof-of-concept experiment, the top and bottom DC pads (see Fig. 6.15) were contacted with multi-needle probes, which are connected to laboratory power supplies. For the *vdd* and *vss* of the circuit blocks, the *Keithley 2636A* source meter was used. For the DUT terminal contacts (S, G, DB), noise is more critical, since it cannot be suppressed by the cross-correlation technique. Therefore, here the *Keysight B2962A* low noise power sources were used. From the left and right, the ring oscillator output waveforms were probed with ground-signal-ground RF needles connecting to a *Agilent Infiniium DSA-X 92004Q* RF oscilloscope. The oscilloscope and low-noise power sources were connected to a PC via USB/GPIB for remote programming.

For the multi-DUT experiment the chip was contacted from top and bottom with custom-configured multi-needle probes containing additional decoupling capacitors on the power supply pads. The power supply contacts were connected to a *Keysight N6705B* DC power analyzer. The shift register clock and data input were connected to an *Agilent Technologies 81160A* pulse generator, which was used to write the desired bit sequence to the SR flip-flops. The digital outputs were connected to a *Tektronix MSO58* mixed-signal oscilloscope. From the left a 3-needle probe was used to contact the DUTs' gate, source and drain bias terminals, which were also powered by the *Keysight N6705B* DC power analyzer. Finally, from the right, the clock and TDC test signals were provided via a twin RF probe from a *Keysight 81134A* pulse generator. All laboratory instruments were connected via GPIB to the PC for remote programming.

6.3.4.2 Step I: Series Resistor Calibration

As a first step, the R_s series resistor is calibrated. Even though the resistor is drawn with a large area to reduce relative production variances, errors in the range of 10% must be expected due to layer thickness variations. The calibration procedure utilizes the fact that the ring oscillators' frequency is dependent on the NUT voltage. The oscillation frequency is recorded with the oscilloscope as a function of the drain bias voltage, once with the DUT being switched off ($v_s = v_g = 0\,\mathrm{V}$), and once switched on ($v_s = 0\,\mathrm{V}$ and $v_g = 0.8\,\mathrm{V}$). The resulting frequency curves are shown in Fig. 6.17. In the former case, the voltage on the NUT v_{NUT} is identical to the applied drain bias voltage, since no current flows through R_s. Here, a frequency maximum was observed for $v_{db} = v_{NUT} = 0.380\mathrm{V}$. In the latter case, where a current flows through R_s and the DUT, v_{NUT} can be inferred from the ring oscillator frequency: The maximum frequency is reached at $v_{db} = 1.094\,\mathrm{V}$, which implies that for this bias the NUT voltage is again at $v_{NUT} = 0.380\,\mathrm{V}$. By measuring the current flow at the drain bias terminal i_{db} with the source meter the calibrated resistance can be calculated:

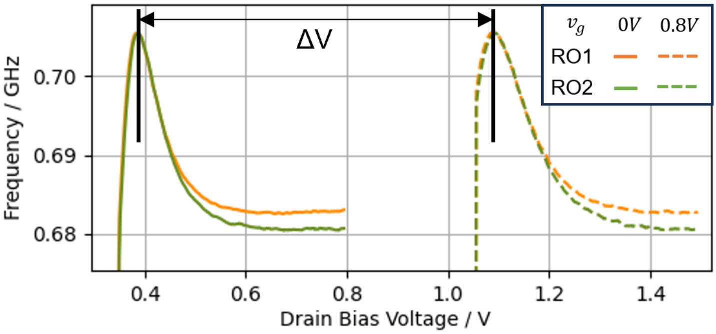


Figure 6.17: Ringo frequency as a function of the drain bias voltage for switched on and off DUT for series resistor calibration.

$$R_{s,calib} = \frac{v_{db,max,on} - v_{db,max,off}}{i_{db,max,on}} \tag{6.3}$$

For the exemplary DUT a value of $1055\,\Omega$ was calculated.

6.3.4.3 Step II: DC Current Measurement

The next step is to measure the current of the DUT at the bias condition of the intended flicker noise characterization. While v_s and v_g can be directly set to the desired voltages, at the v_{db} terminal the voltage drop at R_s needs to be considered to reach a given drain voltage v_d. Since however the respective drain current is not yet known an iterative approach is chosen: v_{db} is increased from zero step-wise, while the respectively reached drain voltage v_d is calculated from the measured drain bias current i_{db}:

$$v_d = v_{db} - i_{db} R_{s,calib} \tag{6.4}$$

Once the desired v_d is reached, the drain current corresponding to the investigated bias condition is known. Furthermore, from the measured currents (and the corresponding calculated v_d) the DUT's output conductance g_ds at the specified bias is calculated, which is needed later for the flicker noise spectrum calculation.

For the flicker noise characterization, this procedure needs to be carried out only for the investigated bias condition. For 5 exemplary DUTs however, a full output characteristic with a drain and gate voltage sweep was recorded. Fig. 6.18 shows that the measured results show a good agreement with the nominal simulated data.

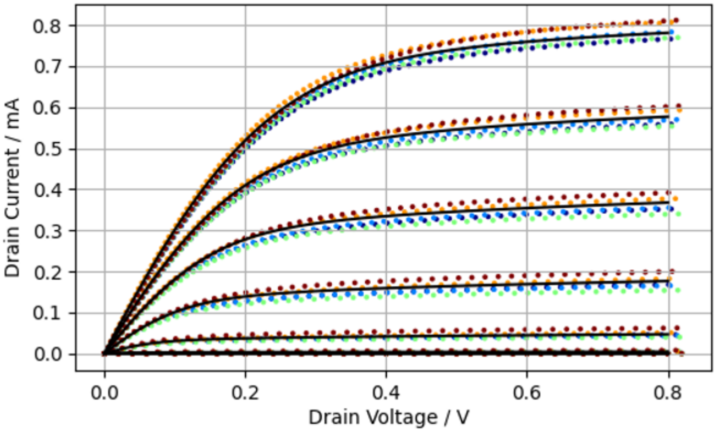


Figure 6.18: Output characteristic of 5 exemplary DUTs compared to the nominal simulated values.

6.3.4.4 Step III: Optimum Offset Search

The third step is to find the optimum offset voltage between the DUT terminals and the sensor circuitry. After the previous DC current measurement for the investigated bias, the required gate and drain bias voltages are known with respect to the source voltage (that is, $v_g - v_s$ and $v_{db} - v_s$ are fixed). A common offset of all three DUT terminals with respect to the substrate ground is possible due to the employed deep n-well and does not influence the transistor's operating conditions (e.g.

DC drain current or flicker noise). It should therefore be selected such that the sensor circuitry is most sensitive to noise, that is such that the ring oscillators exhibit maximum phase noise upconversion for a given noise on the NUT. Intuitively, this condition is expected when the ring oscillator frequency is most sensitive to changes in the NUT voltage. This understanding is correct and will be made quantitatively explicit in Section 6.3.4.6 and the appendix, which addresses the quantitative mathematical connection between flicker and phase noise spectrum.

To find the optimal value, a sweep of the offset voltage is performed while recording the corresponding ring oscillator frequencies f_{RO}. The resulting data for RO1 and the calculated derivative $\frac{df_{\mathrm{RO}}}{dV_{\mathrm{offset}}}$, is shown in Fig. 6.19. The offset voltage where the maximum absolute frequency derivative is reached corresponds to the sought-after optimum value. The frequency and the derivative at this offset play an important role in the following flicker noise spectrum calculation. Therefore, the accuracy of the measurement is increased by averaging several frequency measurements at and close to the optimum offset (see crosses in Fig. 6.19).

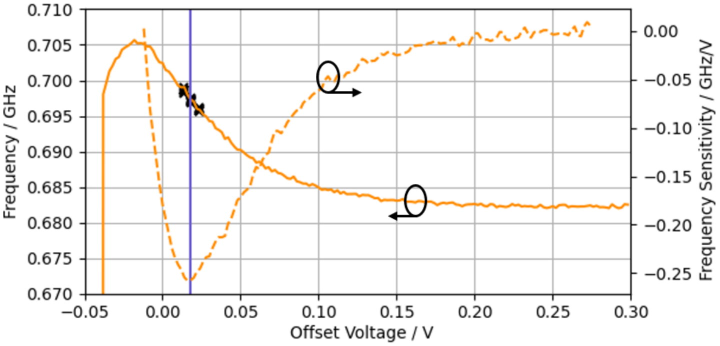


Figure 6.19: Ring oscillator frequency at different offset voltages for a specified DUT bias. The second y-axis shows the frequency's derivative with respect to the offset voltages. The optimum, that is the absolute maximum offset voltage, is marked with a blue line. At this point multiple measurements are taken (marked with crosses) to increase accuracy.

6.3.4.5 Step IV: Cross-correlation Phase Noise Spectrum

With the optimal DUT terminal voltages set, the next step is to record the cross-correlation phase noise spectrum of the two ring oscillators.

For this purpose, the waveforms of both ring oscillators are recorded with the oscilloscope for a time frame of $10\,\mathrm{ms}$. This corresponds to a calculable lower frequency limit of the DUT noise spectrum of $100\,\mathrm{Hz}$. To reduce the amount of transferred data, the sampling rate is reduced to 2 GSamples/s, that is just enough to capture every oscillation edge. The accompanying resolution reduction is negligible for the low-frequency phase fluctuations stretching over multiple oscillation periods. A section of the recorded waveforms is shown in Fig. 6.20. After transferring the data to the PC the time points of the positive edges are calculated. As mentioned previously, at these instances the phase of the oscillation is uniquely defined. From the average oscillation period the distance of each positive edge from its respective ideal position, that is its TIE jitter can be determined. The resulting jitter as a function of time is shown for both ring oscillators in Fig. 6.21. It can be seen that some phase fluctuations of RO1 and RO2 are correlated, while other effects only influence one oscillator.

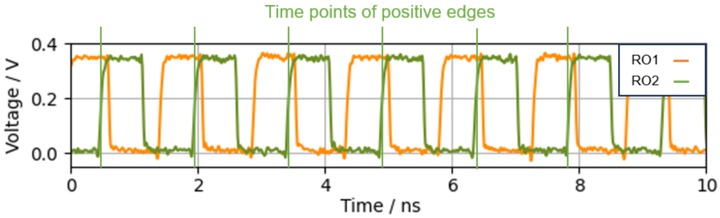


Figure 6.20: Section of the recorded ring oscillator waveforms. The time points of positive edge positions of RO2 are indicated with vertical lines.

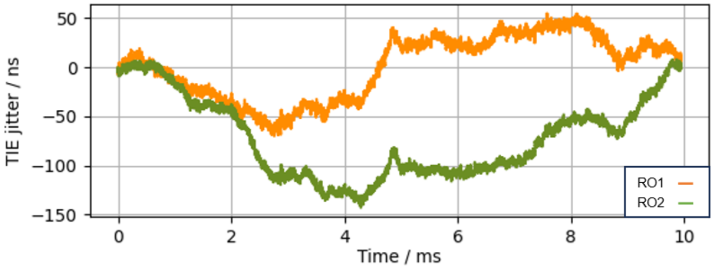


Figure 6.21: Time-interval-error jitter of both ring oscillators for a time frame of 10 ms.

Since only the correlated effects on the phase of both ring oscillators are of interest, the cross-correlated phase fluctuation spectrum $S_{\phi,cc}$ is calculated from the two recorded TIE jitter functions. To reduce spectral leakage, the blackman windowing function is multiplied with the TIE jitter waveforms before an FFT is applied. The results for RO1 and the complex conjugate of RO2 are then multiplied

$$S_{\phi,cc} = 4\pi^2 f_{RO}^2 (\mathrm{FFT}[\tau_{\mathrm{RO1}}^{\mathrm{TIE}}] \times \mathrm{FFT}[\tau_{\mathrm{RO2}}^{\mathrm{TIE}}]^*), \tag{6.5}$$

where the preceding scaling factor $4\pi^2 f_{RO}^2$ serves to express the TIE jitter in terms of phase. To suppress the noise floor by uncorrelated contributions, the described measurement has to be repeated multiple times and the resulting cross-correlation spectra $S_{\phi,cc}$ averaged. A cross-correlation number of M reduces the correlated noise floor by a factor of $5 * \log(M)\,\mathrm{dB}$ [20]. Furthermore, averaging reduces the intrinsic variance of spectral estimation by PSDs (see Section 6.1). Fig. 6.22 shows the resulting cross-correlation spectrum of 60 averages for the barely switched on exemplary DUT ($v_{gs} = 0.3\,\mathrm{V}$ and $v_{ds} = 0.8\,\mathrm{V}$). For comparison the PSDs without cross-correlation of both RO1 and RO2 are shown. Since the DUT exhibits only low flicker noise at this bias condition the cross-correlation spectrum can be seen to effectively suppress the intrinsic ring oscillator noise floor below their individual noncorrelated PSDs. The resulting cross-correlation phase noise spectrum only contains correlated effects from the DUT.

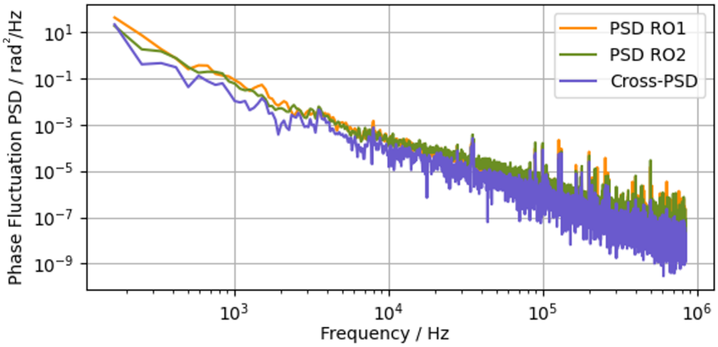


Figure 6.22: Cross power spectral density between RO1 and RO2, and individual power spectral densities.

The number of necessary cross-correlations depends on the measured DUT bias condition. For high drain current conditions (i.e. high flicker noise) only few averages are needed, since the ring oscillator phase noise is dominated by contributions from the DUT. On the other hand, at bias conditions with low flicker noise more averages are needed to reduce the oscillator-intrinsic phase noise below the DUT contributions. An estimate can be obtained from the difference between *spectre PN* simulations with contributions from the DUT being switched on and off, respectively.

6.3.4.6 Step V: Calculation of FN Spectrum

As the last step a connection is established between the measured cross-correlated phase fluctuation spectrum $S_{\phi,cc}$ and the underlying current noise spectrum of the DUT $S_{i,DUT}$. In general the phase fluctuation of an oscillator can be related to the underlying device noise sources via Eq. 3.45, which adjusted for the obtained cross-correlation spectrum reads:

$$S_{\phi,cc}(f) = \frac{1}{4T_{RO}^2 f^2}\left((c^{white})^2 \cdot 1\,\frac{\mathrm{V}^2}{\mathrm{Hz}} + \sum_m (c_m^{colored})^2 \cdot S_{cm}(f)\right), \tag{6.6}$$

where T_{RO} is the ring oscillator oscillation period. Since the presented FNM concept focuses on the measurement of flicker noise the white noise term can be disregarded due to its negligible contributions at low frequencies. Furthermore, the cross-correlation suppresses the noise contributions of all devices except the DUT and the series resistor. These two are at first combined as voltage noise on the NUT, such that only one term remains in the sum. Rearranging the equation for the sought-after NUT voltage noise spectrum yields

$$S_{v,NUT}(f) = \frac{4T_{RO}^2 f^2}{(c_{NUT}^{colored})^2} S_{\phi,cc}(f). \tag{6.7}$$

As previously mentioned the phase noise contribution $c^{colored}$ of a given noise source can be related to the ring oscillator frequency sensitivity at the respective bias point. The quantitative connection can be shown (see appendix) to be

$$c_{NUT}^{colored} = \frac{df_{RO}}{dV_{offset}} \frac{1}{f_{RO}}, \tag{6.8}$$

such that the contribution factor can be calculated from the ring oscillator frequency and its derivative recorded during the offset sweep measurement step (Section 6.3.4.4).

The current noise spectrum of the DUT can now be calculated from the NUT voltage noise. Simulations show that the contributions of the series resistor can be neglected for all DUT biases except subthreshold conditions. This is especially the case at the considered low frequencies, where flicker noise dominates. The DUT's current noise drops off as voltage at the series resistor, but also at the DUT's output conductance itself, yielding

$$S_{i,DUT}(f) = S_{v,NUT}(f)\left(\frac{1}{R_{calib}} + g_{ds}\right)^2, \tag{6.9}$$

with R_{calib} and g_{ds} known from the resistor calibration and DC measurement steps, respectively (Sections 6.3.4.2 and 6.3.4.3.).

The final resulting current noise spectrum $S_{i,DUT}$ of the fully switched on exemplary DUT ($v_{gs} = 0.8\,\mathrm{V}$ and $v_{ds} = 0.4\,\mathrm{V}$) is displayed with its validation measurement (see next section) in Fig. 6.23.

6.3.4.7 Validation: Off-chip Measurements

The DUT current noise spectrum obtained via the FNM methodology can be validated with conventional laboratory measurement. For this, the gate, source, and drain bias terminals of the DUT are contacted with single-needle probes. The *Keysight E4727A Advanced Low-Frequency Noise Analyzer* is then used for flicker noise measurement. Here, again the voltage drop at the series resistor needs to be considered to set the correct drain bias voltage. Possible low-pass filtering effects of the noise by the series resistor and parasitic capacitances are negligible in the considered low-frequency range.

Fig. 6.23 shows the corresponding measured noise spectrum compared to the result obtained via the FNM technique. For the validation data, the typical flicker noise $1/f$-slope can be clearly seen for the whole measured frequency range. A good fit is achieved by the FNM concept at the lower frequency half of the spectrum. At higher frequencies a bump can be observed (between 20 kHz and 200 kHz), which can be attributed to correlated noise effects from the DUT power supplies. It was observed that different power supplies influence the severity of the bump, while other parts of the spectrum remain unchanged. The white noise floor above 200 kHz can be explained by upconverted white noise of oscillator-intrinsic devices, which begins to play a role in this frequency range. A higher number of averaged cross-correlations would be needed to suppress these noise contributions, which comes at the cost of longer measurement times.

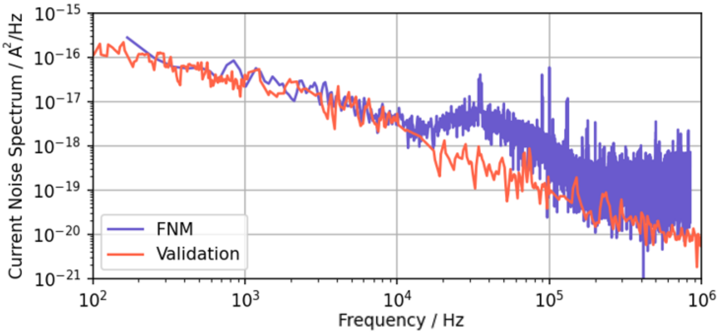


Figure 6.23: Calculated current noise spectrum of the DUT compared to the validation measurement.

6.3.4.8 Multi-DUT Adjustments

In case of the multi-DUT FNM a different technique is needed for measurement steps I and II. Since many DUTs are connected in parallel, the current flowing through a single DUT cannot be obtained, inhibiting both the resistor calibration and the DC current measurement. An alternative is to take for both R_{calib} and the DUT current at the investigated bias the nominal simulated value. Although some error is introduced, this technique still delivers reliable results, since the expected flicker noise variations between different DUTs are much larger than the errors introduced. A second alternative is to use values from close-by test structures for a separate resistor and DUT. Global (wafer-wide) production variations can therefore be corrected and only local variations remain as an error. In the proof-of-concept experiment, for instance, it was observed that the series resistance deviation from the nominal value was mainly due to a global offset ($\mu = 60\,\Omega$) with only small local standard deviation around this global mean ($\sigma \approx 10\,\Omega$).

One of the main enhancements of the multi-DUT experiment is the on-chip jitter measurement with a TDC, entailing adjustment to the data readout of measurement steps III and IV. First, the TDCs of the test units are calibrated for later use in the jitter measurement. Here, the TDC test mode bit of the shift register is set and the pulse generator is used to generate pulses on the clock and TDC test signal with a defined delay. The corresponding activated bins for multiple repeated pulses can then be read out while sweeping over the applied pulse delay. A subsection of the results is plotted Fig. 6.24, where the size of the dots represents the number of activations at the given delay. The general behavior of the TDC shows good linearity, with small variances in the bin sizes. The partial overlap of the bins does not necessarily stem from inaccuracies of the TDC, since the pulse generator delay also shows a variance of 3 ps for a defined delay.

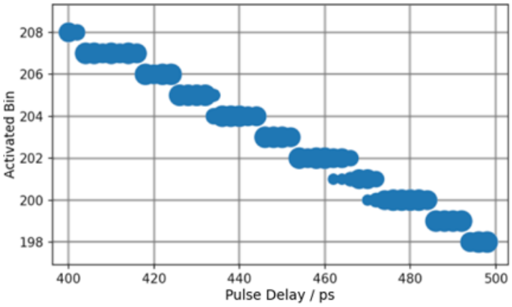


Figure 6.24: TDC calibration by applying a defined pulse delay to the inputs, while recording the corresponding activated bins.

For the flicker noise measurement with the FNM concept a bias of $v_g s = 0.8\,\mathrm{V}$ and $v_d s = 2.3\,\mathrm{V}$ was applied. Taking into account the voltage drop at the series resistor the DUT was measured at a drain voltage of $v_{ds} = 0.4\,\mathrm{V}$. The test measurement bit in the shift register is now set to logical low to measure the edges of the ring oscillators by the corresponding TDCs. Here, ideally a TDC clock signal frequency larger than the ring oscillator frequency would be used, so that each oscillation edge is captured by the TDC. However, the bandwidth of the output chain is limited due to the large capacitances associated with the signal pads, needles, cables, and the

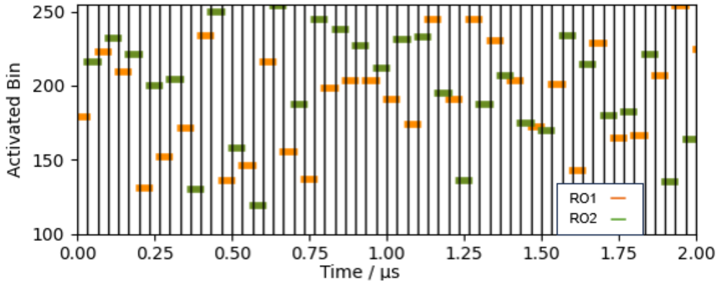


Figure 6.25: Activated bins for a time frame of 2 µs.

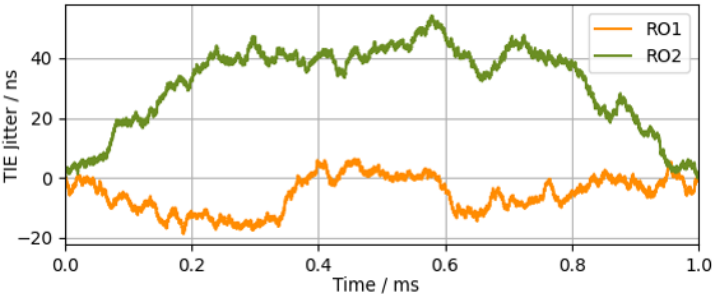


Figure 6.26: TIE jitter for RO1 and RO2 calculated from the TDC output.

oscilloscope. Therefore, a lower TDC clock frequency of 15 MHz was chosen. Consequently, some of the oscillation edges are skipped by the TDC, essentially resulting in an undersampled measurement. At the low frequencies intended for the flicker noise measurement, the resulting aliasing can, however, be neglected due to the $1/f$-slope of the measured spectrum. Fig. 6.25 shows the activated bins for an oscillation time frame of 2 µs, with the previously described alternating output for RO1 and RO2. Notably, bins below approximately 100 are not activated, since the ring oscillator oscillation period is shorter than the corresponding measurement range.

The TIE jitter of both ring oscillators can now be calculated. The time points of the measured edges are calculated from TDC clock edge positions and the calibrated TDC data. Since not every oscillation edge is captured the ring oscillator frequencies can be obtained from the time differences between subsequent measured edges, which are a multiple of the oscillation period fluctuating by ± 1. Taking this effect into account, the ideal edge positions and therefore also the TIE jitter of both ring oscillators can be calculated (see Fig. 6.26).

The following measurement methodology of step V is equivalent to the proof-of-concept experiment. The noise spectrum obtained from the exemplary DUT is shown in Fig. 6.27. For the lower frequency end of the spectrum, the typical $1/f$-slope of flicker noise can be observed. It is lower than the simulated value, but well within expected variances. At the higher frequency end, white

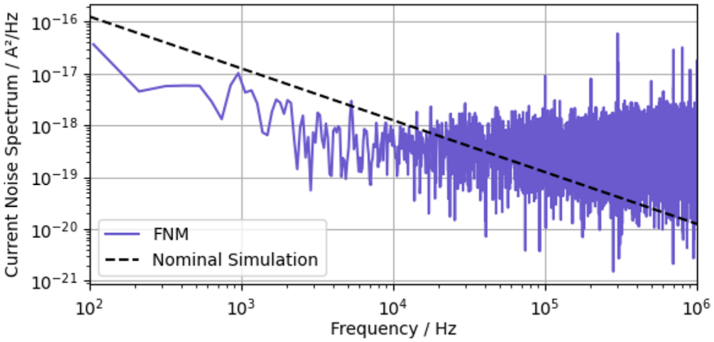


Figure 6.27: Calculated current noise spectrum of the DUT compared to nominal simulation.

noise is observed, which can be explained, as previously, by upconverted oscillator-intrinsic white noise. This effect, as well as the high variance of the spectrum at high frequencies, is removable at the cost of increased measurement time by a higher number of cross-correlations.

6.3.5 Statistical Results

With the presented measurement methodology, a multitude of DUTs has been measured: For the proof-of-concept test chip this entails stepping the wafer to different dies. For the multi-DUT measurement several DUTs can be measured by switching through test units via the shift register.

6.3.5.1 Proof-of-concept: Validation Bias Sweep

For three DUTs the flicker noise spectrum was recorded for a gate voltage sweep from $300\,\mathrm{mV}$ to $800\,\mathrm{mV}$ in $100\,\mathrm{mV}$ steps with $v_{ds} = 400\,\mathrm{mV}$. The spot noise value at $100\,\mathrm{Hz}$ was calculated by fitting the function $S_i(f) = a/f$ to the data in the frequency range between $100\,\mathrm{Hz}$ and $1\,\mathrm{kHz}$. This procedure was carried out both for the FNM data, as well as for the validation data. Fig. 6.28 shows the comparative results. In general, a good fit is achieved between the FNM and validation. Although for some measurements an error of up to factor 4 is observed, most of the FNM measurements do not differ more than factor 2 from the validation, which is a small uncertainty compared to the range of measured values over almost two orders of magnitude (see next section for more considerations regarding measurement error). Furthermore, for each DUT the measured noise as a function of gate voltage shows a slightly different trend, which is well-matched between both measurement techniques.

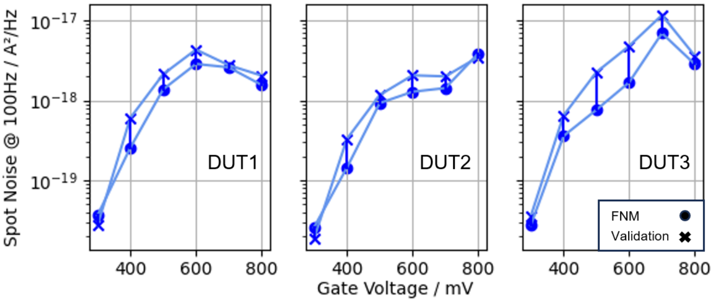


Figure 6.28: Spot noise measurement at 100 Hz of 3 DUTs at different gate bias conditions with $v_{ds} = 400\,\mathrm{mV}$. Results from the FNM technique and validation results are marked with a dot/cross, respectively.

6.3.5.2 Proof-of-concept: Multi-Die Validation

To validate the FNM results a multitude of DUTs was measured with both the FNM and validation technique. The measurements are conducted for the small $\mathrm{DUT_s}$ and the large $\mathrm{DUT_l}$ for the bias condition of a fully switched on transistor ($v_{ds} = 400\,\mathrm{mV}$ and $v_{gs} = 800\,\mathrm{mV}$). Here, for the small $\mathrm{DUT_s}$ all available dies on the wafer were measured (52 dies), and for the large $\mathrm{DUT_l}$ a subset of 10 dies. The spot noise at 100 Hz was again fitted to the obtained spectra. The resulting correlation plot is shown in Fig. 6.29. A good match between FNM and validation is observed for

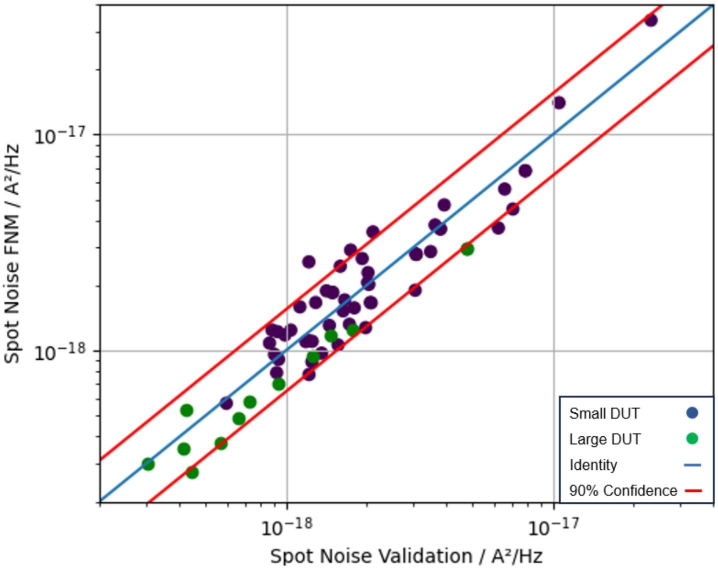


Figure 6.29: Spot noise measurement at 100 Hz of 52 small $\mathrm{DUT_s}$ and 10 large $\mathrm{DUT_l}$ at the bias of $v_{ds} = 400\,\mathrm{mV}$ and $v_{gs} = 800\,\mathrm{mV}$. The red lines indicate the 90% confidence interval.

both the small $\mathrm{DUT_s}$ and the large $\mathrm{DUT_l}$. As expected the large $\mathrm{DUT_l}$ shows a lower flicker noise compared to the smaller transistor. The confidence interval around the validation measurements containing 90% of the FNM results was calculated to be a factor of 1.55. It is therefore much smaller than the observed variance between DUTs, which spans almost two orders of magnitude. Furthermore, the fact that also the validation measurement exhibits a nonzero measurement error needs to be considered. The FNM technique is, therefore, shown to deliver reliable results for flicker noise characterization.

6.3.5.3 Proof-of-concept: Random Telegraph Noise

One of the advantages of the FNM concept compared to some of the previous approaches is that the full noise spectrum is measured instead of spot noise at a single frequency point. This can be demonstrated well for DUTs exhibiting non-$1/f$ low-frequency noise, for example RTN due to single charge traps. For two DUTs with particularly distinct deviations from a $1/f$-slope the FNM measurement results are compared to the validation measurements in Fig. 6.30. A good fit of the FNM measurement is observed, including non-$1/f$ kinks in the spectrum.

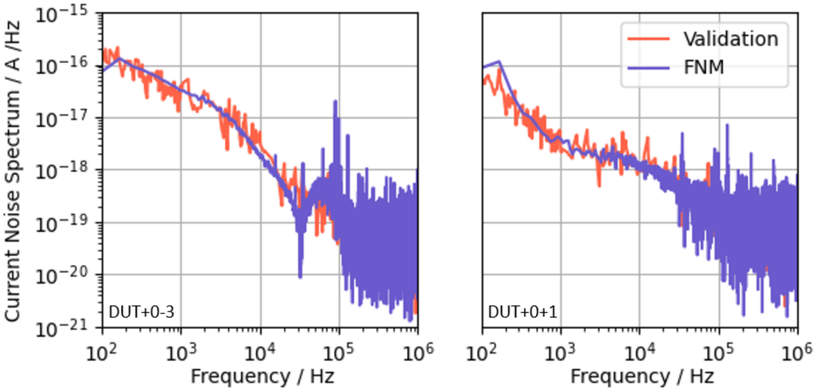


Figure 6.30: Noise spectrum measured by FNM technique and validation measurement for two DUTs with distinct non-$1/f$ noise effects.

6.3.5.4 Multi-DUT Results

For the multi-DUT experiment the 12 identical test units with the smallest available DUTs were measured. Here, the advantage is that the DUTs can be measured in rapid succession without required stepping. As bias condition $v_{ds} = 400\,\mathrm{mV}$ and $v_{gs} = 800\,\mathrm{mV}$ was chosen. As before, the spot noise at 100 Hz was obtained by a fit to the lowest measured frequency decade. The probability plot of the common logarithm of the spot noise values is shown in Fig. 6.31. Even though more data points would be needed to draw more statistically significant conclusions, it can be observed that the data approximately follows a normal distribution around the simulated value. The spot noise itself therefore follows an expected log-normal distribution (see Section 2.2.2.4).

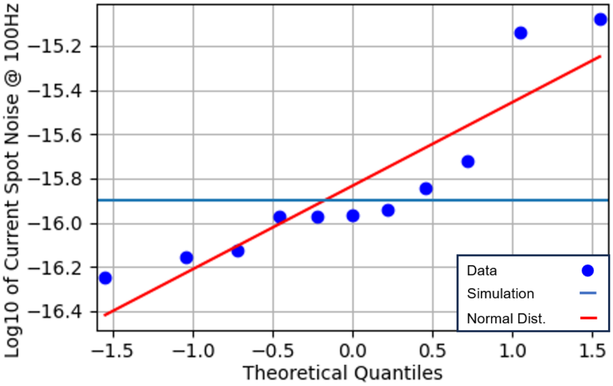


Figure 6.31: Probability plot of the base 10 logarithm of measured spot noise values at 100 Hz

6.3.6 Conclusion and Outlook

The presented measurement results show that with the introduced FNM concept reliable flicker noise spectra at defined bias conditions can be obtained with a fully integrated high-throughput macro. The attributes of the multi-DUT FNM are presented in comparison with previous works in Table 6.2.

With the FNM concept significant area savings can be achieved compared to conventional off-chip laboratory measurements. While a single test unit is still rather large in future implementations the digital circuitry could be shared by all sensor cores, since after the oscillator the effects of further noise sources on the signal's phase are limited. Furthermore, in this implementation, the sensor core was not yet optimized for area, leaving plenty of room for possible size reductions.

The technique exhibits quick measurements for biases where low sensitivity, and therefore only few cross-correlations, are required. Due to quick DUT selection via the shift register and on-chip data preprocessing, the results can be obtained in only a few seconds. For low-noise bias conditions or low-noise DUTs the measurement time increases linearly with the required number of cross-correlations.

Compared to some of the previous techniques, the FNM concept shows the advantage that the full FN spectrum (instead of only the corner frequency) can be measured for freely selectable biases and without averaging over multiple DUTs.

The main enhancement of the FNM concept is the cross-correlation technique and the consequential increase in sensor sensitivity. Compared to several other previous techniques that implement noise measurement via integrated ADCs, noise preamplification is not required. Furthermore, noise from the ADC itself and its quantization noise can be effectively suppressed by the technique, leaving only the thermal noise of the series resistor as parasitic contributions. Therefore, careful noise analysis requiring accurate compact models is not needed. Moreover, all relevant values for the spectrum calculation can be obtained via calibration and do not rely on simulated values.

Further developments of the FNM structure can be carried out in several aspects: The digital readout circuitry might be adjusted to make the macro compatible with scribeline measurements for production monitoring. For this, cross-correlation and spectrum calculation might be integrated on-chip. Furthermore, as previously discussed, the area per DUT can be minimized using several techniques. Another intriguing possibility is to measure high-frequency noise with the FNM concept, which is enabled in principle by the ps-range resolution of the TDC (and even higher resolutions more sophisticated TDC architectures). The theoretical upper frequency limit is set by the oscillator frequency, where several GHz might be feasible with ROs, and even higher frequencies with LC VCOs. Due to a different noise-to-phase upconversion mechanism for white noise (see Section 3.2.4) the sensitivity calibration would need to be revised and high-bandwidth data readout (or on-chip processing) implemented. The resulting solution would, however, bridge the frequency gap of conventional noise measurement solutions [154] and therefore merits further investigation.

Table 6.2: Comparison of this work with previous approaches.

	FNM [this work]	Laboratory	Switchable Matrix [68]	Integrated $\Sigma\Delta$-ADC	Integrated VCO-ADC [150]	PN-based [151, 152]
Area per DUT	Moderate 2900 μm^2 Core 10 000 μm^2 TU	High 50 000 μm^2	Low 200 μm^2	Medium Each DUT with LNA/ADC	Medium Each DUT with LNA/ADC	- No Single DUT Measurement
Measurement Time	Fast @ high noise Depends on sensitivity	Slow Due to averaging / stepping	Medium Defined by lab instrument	Fast	Fast	Fast
Single DUT and Bias	Yes	Yes	Yes	Selected biases	Yes	No
Noise Spectrum	Yes	Yes	Yes	Yes	Yes	FN Corner
Parasitic Noise	Series resistor	-	Switch transistors	Biasing, LNA, ADC	Preamp, biasing, ADC	Avg. over all RO transistors
Noise Model Requirements	Low	-	Moderate	High	High	Low
ADC Calibration	Yes	-	-	No	Yes	-
RF Noise	In principle to be shown	Gap	Limited	In principle	No	Yes

Chapter 7

Conclusion

The tension between increasing device flicker noise and the applications' tighter phase noise specifications is not expected to subside: The requirements posed to oscillator stability will rather increase with future technological advancements. Simultaneously in even smaller devices singular defects in the atomic lattice will have an increasing effect on the observed noise spectrum. The resulting design challenge needs to be addressed by a joint approach from contributors across the integrated circuit development value chain:

Starting at the technology and process-design kit development stage, low-frequency noise variations must be accurately characterized and respective models developed. The conducted flicker and phase noise measurements of leading-edge technology nodes (Chapter 5) show that inclusion of a simple *worst noise corner* to capture novel effects will no longer be sufficient, since it heavily overestimates noise in large parts of the spectrum. The model must instead be able to represent noise effects differing from the common flicker noise spectrum, such as random telegraph noise. This includes an accurate description of statistical variations with correct device geometry and bias dependence. Techniques such as the presented flicker noise monitor (Section 6.3) can be employed to enable the collection of the required statistically relevant data.

Schematic designers can then make use of the provided models in the development of local oscillator circuits. Here, the investigations on phase noise simulation and its sensitivity to model accuracy can support oscillator topology exploration (Chapter 4). Above all, the findings point out that novel approaches are required to clear the fog over the oscillator design space, particularly in light of noise models increasing in complexity. For example, new simulation tools that establish connections between changes in design parameters and phase noise might be of help.

Lastly, the increased expected variance between the noise of multiple devices should already be considered in higher level design of the system. Build-in self-tests as the presented delta jitter macro (Section 6.2) can be employed to dynamically adjust circuit operation according to changing requirements (e.g. in a power versus noise trade-off).

While significant effort is required to push phase noise toward the boundaries of what is possible, the potential to enable exciting emerging applications makes it a worthwhile pursuit.

Chapter 8

Appendix

This appendix shows the derivation of the equation relating the phase noise contribution factor $c^{colored}$ to the frequency sensitivity toward voltage changes of the respective circuit node.

Without loss of generality, suppose a small change b in bias voltage v_{bias} changes the oscillation frequency from f_1 to a slightly higher f_2. The new oscillation with increased frequency can be viewed as "phase noise" $\phi(t)$ to the original oscillation, where however $\phi(t)$ is a function increasing with time (while $\phi(t)$ does not need to increase monotonically, the change during one new oscillation period $T_2 = 1/f_2$ needs to be constant: $\phi(nT_2) - \phi((n-1)T_2) = \text{const.} > 0$). One period of the new oscillation corresponds to a 2π phase increase by the original underlying oscillation plus the additional phase modulation: $2\pi = \frac{2\pi T_2}{T_1} + \phi(T_2) = \frac{2\pi(T_2+\alpha(T_2))}{T_1}$, where in the last term the phase modulation is scaled to a corresponding time modulation $\alpha(t) = \frac{T_1}{2\pi}\phi(t)$. Therefore, new and old oscillation period can be connected via the time modulation $\alpha(t)$ by

$$T_1 = T_2 + \alpha(T_2). \tag{8.1}$$

The derivative of the time modulation can be brought into relation with the voltage/current fluctuations of a noise source $b(t)$ via Floquet theory according to Eq. 3.39, which assuming only the single noisy circuit node reads:

$$\frac{d\alpha(t)}{dt} = v_1\big(x_s(t+\alpha(t))\big)B\big(x_s(t+\alpha(t))\big)b(t). \tag{8.2}$$

Combining Eqs. 8.1 and 8.2 yields

$$T_1 = T_2 + \int_0^{T_2} v_1\big(x_s(t+\alpha(t))\big)B\big(x_s(t+\alpha(t))\big)b(t)dt. \tag{8.3}$$

In the considered case of a small change of bias voltage $b(t)$ is a constant and can therefore be removed from the integral. The remaining integral can be recognized as T_1 times the contribution factor $c^{colored}$ for colored noise sources (Eq. 3.44). Therefore, Eq. 8.3 can be simplified to $T_2 = T_1 - b(c^{colored})T_1$. For infinitesimal changes ($T_1 \approx T_2$), the derivative of the oscillation period can be obtained $\frac{dT}{db} = \frac{dT}{dv_{bias}} = -(c^{colored})T$, yielding an expression for the colored contribution factor in terms of frequency sensitivity:

$$c^{colored} = -\frac{dT}{dv_{bias}}\frac{1}{T} = \frac{df}{dv_{bias}}\frac{1}{f}. \tag{8.4}$$

List of Publications

[1] L. Schramm, P. Baumgartner, and J. Aghassi-Hagmann, “Influence of transistor compact model accuracy on phase noise simulation,” in *2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. IEEE, Jun. 2023, p. 329–332, ©2023 IEEE. [Online]. Available: http://dx.doi.org/10.1109/PRIME58259.2023.10161796

[2] L. Schramm, P. Baumgartner, and J. Aghassi-Hagmann, “On-chip quantization- and correlation-robust jitter measurement for low phase noise and high frequency oscillators,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 11, p. 3958–3962, Nov. 2023, ©2023 IEEE. [Online]. Available: http://dx.doi.org/10.1109/TCSII.2023.3282817

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[5] L. Schramm, P. Baumgartner, and J. Aghassi-Hagmann, “Phase noise upconversion of non-1/f device noise in gate-all-around technology nodes,” 2026, submitted.

[6] L. Schramm, P. Baumgartner, and J. Aghassi-Hagmann, “An integrated measurement macro for rapid high-sensitivity flicker noise characterization,” 2026, submitted.

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