

Printed Devices and Circuits in Hybrid Systems on Foils

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Kurzfassung

Gedruckte Elektronik bietet gegenüber konventionellen siliziumbasierten CMOS-Technologien überzeugende Vorteile, darunter eine kosteneffiziente additive Fertigung, Niederspannungsbetrieb der Bauelemente sowie mechanische Nachgiebigkeit. Der Übergang von einzelnen gedruckten Bauelementen hin zu zuverlässigen Systemimplementierungen stellt jedoch weiterhin eine Herausforderung dar, insbesondere aufgrund inhärenter Bauelement-zu-Bauelement-Variabilität sowie der Komplexität der Schnittstellenbildung zwischen gedruckter Elektronik und rechnerisch leistungsfähigen siliziumbasierten Systemen. Diese Dissertation adressiert diese Herausforderungen durch die Herstellung und Charakterisierung gedruckter elektronischer Bauelemente, deren Nutzung auf Schaltungsebene sowie die Realisierung hybrider System-in-Folie-Integrationsstrategien zur sicheren Identifikation und Temperaturmessung für automobiler Anwendungen.

In dieser Arbeit werden zwei komplementäre Architekturen elektrolyt-gesteuerter Transistoren (EGTs) entwickelt. Hybrid-gedruckte EGTs auf Glassubstraten, realisiert durch laserablatierte Indium Zinn Oxid (ITO) Elektroden in Kombination mit tintenstrahlgedruckten Indiumoxid-Halbleiterschichten und kompositen festen Polymerelektrolyten, ermöglichen einen stabilen Betrieb bei Spannungen unter 1 V bei gleichzeitig verbesserter Bauelementuniformität. Diese Architektur bildet eine robuste Grundlage für die Schaltungsrealisierung und die nachfolgende Systemintegration. Parallel dazu werden vollständig gedruckte EGTs auf Glas- und flexiblen Polyimid-Substraten unter Verwendung aerosolstrahlgedruckter Goldelektroden in Kombination mit tintenstrahlgedruckten Funktionsschichten realisiert. Die vollständig gedruckten EGTs auf Glas dienen als Prozess- und Leistungsreferenz und ermöglichen die Übertragung auf Polyimid-Substrate, auf

denen flexible Bauelemente mit Betriebsspannungen unter 1 V demonstriert werden. Die gezeigte Funktionalität dieser Bauelemente belegt die grundsätzliche Eignung für eine Schaltungsimplementierung auf flexiblen Substraten.

Basierend auf der hybrid-gedruckten EGT-Architektur wird ein Inverter-Array unter Verwendung von EGTs in Kombination mit resistiven Pull-up-Lasten realisiert und als Physikalisch Unklonbare Funktion (PUF) eingesetzt. Die PUF nutzt analoge Variabilitäten der Übertragungskennlinien der Inverter als Entropiequelle und ermöglicht die Generierung von 36-bit Identifikatoren mittels relativer Vergleichung der Ausgangsspannungen. Parallel dazu werden tintenstrahlgedruckte, platinbasierte Widerstands-Temperatursensoren in *Pt100*- und *Pt1000*-Konfigurationen entwickelt und über einen automotiv-relevanten Temperaturbereich von 20 °C bis 80 °C charakterisiert. Aufgrund der besseren Kompatibilität mit ASIC-basierter Ausleseelektronik sowie der geringeren Empfindlichkeit gegenüber Leitungswiderständen wird der *Pt1000*-Sensor für die hybride System-in-Folie-Integration ausgewählt.

Auf Systemebene werden die gedruckte PUF und die Temperatursensoren mit einem kundenspezifischen 180 nm-CMOS-ASIC integriert, der auf eine Dicke von etwa 30 µm rückseitig verdünnt und in eine Polyimidfolie eingebettet ist. Das resultierende hybride System-in-Folie ermöglicht eine zuverlässige Auslese, Digitalisierung und Schnittstellenanbindung gedruckter Bauelemente, die in einem mechanisch robusten T-förmigen Modul zusammengeführt sind, das realistische automobiler Systembedingungen repräsentiert. Ein Sicherheitsdemonstrator ergänzt die hybride System-in-Folie-Architektur, indem Entropie aus dem Kommunikationskanal zur Ableitung eines gemeinsamen 256-bit Sitzungsschlüssels genutzt wird, wodurch eine sichere Identifikation sowie eine authentifizierte Sensordatenübertragung ohne Speicherung statischer kryptographischer Schlüssel ermöglicht wird.

Insgesamt zeigt diese Dissertation einen kohärenten Entwicklungspfad von gedruckten Bauelementen bis hin zur hybriden System-in-Folie-Integration und demonstriert, wie Niederspannungs-gedruckte Elektronik in Kombination mit folieeingebetteten ASICs eine systemweite Temperaturmessung und PUF-basierte Identifikation innerhalb eines automobilorientierten Sicherheitsrahmens ermöglicht.

Abstract

Printed electronics offer compelling advantages over conventional silicon CMOS technologies, including cost-efficient additive fabrication, low-voltage device operation, and mechanical compliance. However, the transition from standalone printed devices to reliable system-level implementations remains challenging due to inherent device-to-device variability and the complexity of interfacing printed electronics with computationally performant silicon-based systems. This thesis addresses these challenges through the fabrication and characterization of printed electronic devices, their circuit-level utilization, and the realization of hybrid system-in-foil integration strategies enabling secure identification and temperature sensing for automotive applications.

Two complementary electrolyte-gated transistor (EGT) architectures are developed in this thesis. Hybrid-printed EGTs on glass substrates, implemented using laser-ablated indium tin oxide (ITO) electrodes combined with inkjet printed indium oxide semiconductor and composite solid polymer electrolyte layers, enable stable sub-1 V operation with improved device uniformity. This architecture provides a robust basis for circuit realization and subsequent system-level integration. In parallel, fully-printed EGTs on glass and flexible polyimide substrates are realized using aerosol jet printed gold electrodes together with inkjet printed functional layers. Fully-printed EGTs on glass serve as a process and performance reference, facilitating transfer to polyimide substrates, where flexible devices with sub-1 V operation are demonstrated. The demonstrated operation of these devices establishes the feasibility of circuit implementation on flexible substrates.

Based on the hybrid-printed EGT architecture, an inverter array is realized using EGTs in combination with resistive pull-up loads and employed as a physically unclonable function (PUF). The PUF exploits analog variability in inverter transfer characteristics as an entropy source, enabling the generation of 36-bit identifiers using their relative output voltage comparison. In parallel, inkjet printed platinum-based resistive temperature sensors are developed in both *Pt100* and *Pt1000* configurations and characterized over an automotive-oriented temperature range (20 °C to 80 °C). The *Pt1000* sensor is selected for hybrid system-in-foil integration due to its compatibility with ASIC-based readout and reduced sensitivity to interconnect resistance.

At the system level, the printed PUF and temperature sensors are integrated with a custom 180 nm CMOS ASIC, backside-thinned to approximately 30 μm and embedded in a polyimide foil. The resulting hybrid system-in-foil enables reliable readout, digitization, and interfacing of printed devices assembled into a mechanically robust T-piece module representative of automotive systems. A security demonstrator further complements the hybrid system-in-foil architecture by leveraging communication-channel entropy to derive a shared 256-bit session key, illustrating system-level secure identification and authenticated sensor data exchange without storing static cryptographic keys.

Overall, this thesis presents a coherent development pathway from printed devices to hybrid system-in-foil integration, demonstrating how low-voltage printed electronics combined with foil-embedded ASICs enable system-level temperature sensing and PUF-based identification within an automotive-oriented security framework.

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1 Introduction

The increasing deployment of electronics in automotive and industrial systems has shifted the requirements for secure identification, component authenticity, and reliable sensing toward the hardware level, as modern vehicles integrate distributed electronic subsystems that must operate reliably under physical access, mechanical stress, and thermal variations^[1,2]. Under such conditions, automotive components must remain uniquely identifiable, resilient against tampering, cloning and unauthorized replacement^[3], and capable of reliable operation over long operational lifetimes^[4]. Consequently, hardware-embedded security for identification, authentication, and sensing have become a fundamental requirement for next-generation automotive electronic systems^[1,2].

1.1 Limitations of Conventional Silicon-Based Security Approaches

Conventional hardware security solutions are predominantly realized using CMOS-based integrated circuits, employing primitives such as non-volatile memory for key storage, silicon-based physically unclonable functions, and algorithmic cryptographic security blocks^[5]. While these approaches are technologically mature, they inherently increase silicon area, power consumption, manufacturing cost, and system rigidity. More importantly, advanced CMOS fabrication is deliberately optimized to minimize device-to-device variability in order to ensure high yield, which limits the availability of intrinsic physical entropy^[6]. As a result, achieving unique and physically bound identification often necessitates additional circuitry, thereby limiting efficiency, scalability, and suitability for lightweight,

mechanically constrained automotive components^[7]. Addressing these limitations requires a hardware platform in which physical variability is intrinsic rather than engineered, while remaining compatible with planar device fabrication and enabling integration into automotive electronic systems.

1.2 Printed Electronics as a Complementary Method

Printed electronics provides a complementary hardware platform that employs additive, mask-less, and non-contact fabrication while remaining compatible with planar device architectures^[8,9,10]. Printing techniques such as inkjet printing, aerosol jet printing, electrohydrodynamic jet printing, and screen printing enable digitally controlled deposition on a wide range of substrates, including rigid and mechanically compliant surfaces, which is advantageous for integration into automotive electronic systems^[11,12,13,14]. Unlike conventional silicon fabrication, printed electronics inherently introduces stochastic process variations arising from ink rheology, droplet formation, nozzle dynamics, substrate wetting, and post-deposition processing^[8,13]. Rather than being detrimental, this intrinsic variability provides a physically bound entropy source that can be exploited for hardware identification primitives.

1.3 Harnessing Process Variability for Hardware Security

Electrolyte-gated transistors (EGTs) provide a suitable device architecture for printed electronics, as they are compatible with solution-processed materials and enable low-voltage operation ($\leq 2\text{ V}$)^[15,16], which is well suited for energy-efficient operation in distributed automotive electronic subsystems. Importantly,

printed EGTs exhibit pronounced device-to-device intrinsic variability in electrical parameters such as threshold voltage, carrier mobility, semiconductor morphology, and electrode resistance. These fabrication-induced variations constitute a non-deterministic and physically embedded entropy source^[17,18]. When EGTs are combined into higher-order circuits such as inverter arrays, this intrinsic device-level variability can be harnessed to implement physically unclonable functions (PUFs)^[19]. PUFs exploit inherent physical variations to generate unique and reproducible digital responses, forming a hardware fingerprint that is inseparably linked to the physical device^[18]. PUFs implemented using printed electronics are therefore particularly suitable for automotive applications, as they embed device uniqueness directly into the hardware without requiring non-volatile key storage or additional circuitry^[20].

1.4 Printed Temperature Sensors as Complementary Functional Elements

In addition to hardware security, localized temperature sensing is essential in automotive and safety-critical systems to ensure reliable operation^[13,21]. Platinum-based resistive temperature sensors are well suited for this purpose due to their highly linear response, stable temperature coefficient of resistance, and compatibility with printed fabrication^[22,23], making them suitable for automotive-oriented sensing applications. The co-integration of printed PUFs and printed temperature sensors therefore enables a multifunctional hardware platform in which security and sensing are intrinsically linked at the device level, without increasing system complexity.

1.5 Hybrid Integration of Printed and Silicon Electronics

To translate printed devices into system-level functionality, this thesis introduces a hybrid integration strategy^[24,25] in which printed PUF and temperature sensors are interfaced with a custom silicon ASIC embedded in a flexible polyimide substrate (**Figure 1.1**), enabling automotive system-level demonstrations. This architecture combines the complementary strengths of both domains:

- Printed components provide entropy-rich security primitives and sensing, operating within an automotive-oriented temperature range of 20 °C to 80 °C.
- The silicon ASIC provides stable biasing, signal conditioning, digitization, and system-level interfacing.

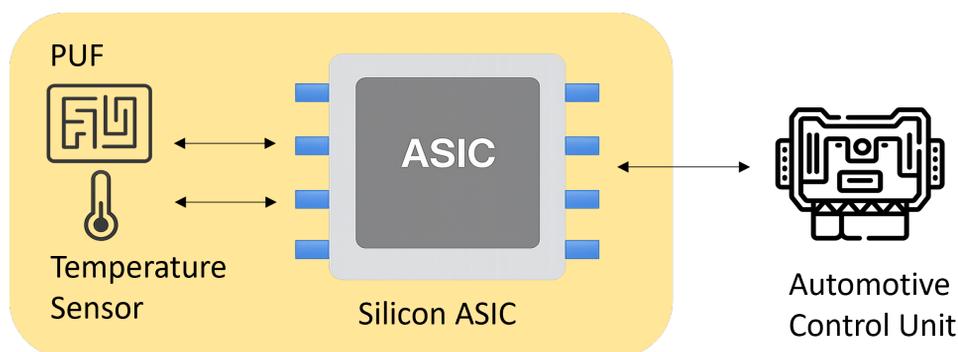


Figure 1.1: Conceptual schematic of the hybrid system-in-foil architecture combining a printed PUF and a printed temperature sensor with a silicon ASIC embedded in a flexible polyimide substrate. The printed devices are electrically interfaced bidirectionally with the ASIC for biasing and readout, while the ASIC provides the system interface to an external automotive electronic control unit.

This hybrid system-in-foil architecture deliberately combines the intrinsic variability and scalability of printed electronics with the reliability and controlled readout capability of silicon technology, enabling application-relevant demonstrations under realistic automotive system.

1.6 Scope and Contributions of the Thesis

The objective of this thesis is to establish a complete development flow from printed devices to hybrid system-level integration for hardware security and temperature sensing in automotive systems. To achieve this goal:

- Two EGT architectures are investigated to support printed PUF implementation. Hybrid-printed EGTs are realized on ITO-coated glass substrates, where electrodes are defined by laser ablation and functional layers are deposited by inkjet printing, providing a stable and reproducible architecture for PUF circuit realization. In parallel, fully-printed EGTs are realized on both glass and flexible polyimide substrates using aerosol jet printing of gold electrodes combined with inkjet printing of semiconducting and electrolyte layers. This architecture enables evaluation of process transfer from rigid to flexible substrates and feasibility analysis for mechanically compliant printed circuits.
- Printed platinum-based resistive temperature sensors are developed on polyimide substrates for automotive-oriented sensing.
- Printed PUF and temperature sensors are interfaced with a custom ASIC embedded in a polyimide substrate, enabling system-level validation under automotive applications.

This architecture bridges printed electronics and silicon systems, establishing a foundation for secure, lightweight, and mechanically compliant hardware platform for future automotive and industrial applications.

1.7 Structure of the Thesis

The remainder of this thesis is organized as follows:

- Chapter 2 introduces the theoretical background and state of the art relevant to this thesis, including the operating principles of electrolyte-gated transistors, hardware security primitives with emphasis on physically unclonable functions, printed resistive temperature sensors, and hybrid system-in-foil concepts. The chapter establishes the scientific foundation for secure and multifunctional printed electronic systems.
- Chapter 3 describes the materials, fabrication processes, and characterization techniques employed in this thesis. It covers the selection and preparation of conductive, semiconducting, and electrolyte inks, substrate preparation, post-processing approaches such as hotplate and furnace sintering, and the structural, morphological, and electrical characterization methods used to evaluate printed devices and hybrid systems.
- Chapter 4 focuses on the fabrication and electrical characterization of both fully-printed and hybrid-printed electrolyte-gated transistors, establishing the device-level performance and variability required for subsequent security and system-level integration.
- Chapter 5 addresses printed security and sensing components, detailing the realization and evaluation of printed physically unclonable function architectures and printed platinum-based resistive temperature sensors. Device-to-device variability is analyzed as an entropy source, key PUF performance metrics are evaluated, and temperature sensing characteristics are investigated.
- Chapter 6 demonstrates hybrid system-level integration by interfacing printed PUFs and printed temperature sensors with a silicon ASIC embedded in a flexible polyimide substrate. The resulting hybrid system-in-foil architecture enables combined hardware security and temperature sensing functionality and validates the co-integration of printed and silicon technologies under application-relevant conditions.
- Chapter 7 summarizes the main findings and contributions of this thesis and outlines technical limitations and perspectives for future research.

2 Theoretical Background and State-of-the-art

This chapter introduces the theoretical background relevant to the devices developed in this thesis, including EGTs, printed resistive temperature sensors, and hardware security primitives such as PUF circuits. In addition, the chapter outlines the system-level concept in which printed PUFs and temperature sensors are interfaced with embedded silicon components in a hybrid system-in-foil architecture, providing the theoretical basis for the device fabrication, characterization, and integration presented in the subsequent chapters.

2.1 Background and State-of-the-Art

2.1.1 Electrolyte-Gated Transistor

The evolution of printed electronics toward secure, low-power, and lightweight systems has created strong demand for transistor architectures that go beyond conventional solid-state device paradigms. Traditional thin-film transistors (TFTs) employing solid dielectric gate insulators such SiO_2 , Al_2O_3 , and HfO_2 typically require gate voltages ranging from a few volts to tens of volts to achieve full channel modulation when combined with solution-processed semiconductors such as In_2O_3 , ZnO , IGZO, and SnO_2 [16,26,27]. This behavior arises primarily from the limited gate capacitance and the non-ideal semiconductor–dielectric interface, which reduce effective electrostatic control of the channel. In addition, achieving high gate capacitance with solid dielectrics requires dielectric thicknesses on the

order of tens of nanometers or below, which is difficult to implement uniformly using printed or solution-based fabrication techniques^[16,17]. As a result, the areal capacitance of printed solid dielectrics is typically limited to the range of 10-100 nF cm⁻²^[16,26]. Consequently, reducing the operating voltage of TFTs necessitates aggressive dielectric scaling or the use of high-permittivity materials. While ultra-thin dielectric layers and high- k oxides^[16,26] can increase gate capacitance, their integration becomes increasingly challenging due to leakage currents, thickness non-uniformity, and interface roughness, particularly under the low-temperature, large-area processing conditions intrinsic to printed electronics. These constraints limit the compatibility of solid-dielectric TFTs with low-power printed circuitry and system-level integration.

To overcome these voltage and process limitations, EGTs have emerged as a distinct class of field-effect transistors in which the conventional solid dielectric is replaced by an ionically conductive electrolyte^[17,26]. Under an applied gate voltage, mobile ions in the electrolyte redistribute and form electric double layer (EDL) at the gate–electrolyte and semiconductor–electrolyte interfaces, enabling efficient electrostatic channel modulation at low gate voltages^[17,27]. The EDL behaves as an ultra-thin capacitive layer with an effective thickness on the order of 1–2 nm, resulting in areal capacitances typically in the range of 1–100 μ F cm⁻²^[16,28], which is several orders of magnitude higher than those achievable using printed solid dielectrics. This high interfacial capacitance enables efficient channel modulation at gate voltages below 2 V^[16,29,27], even for moderate-mobility solution-processed semiconductors.

EGTs have been demonstrated in a variety of device geometries, including top-gate, side-gate (lateral), planar, and vertical configurations^[30,27,17,28], each offering distinct trade-offs in gate coupling efficiency, interface control, fabrication complexity, and compatibility with printing processes. The top-gate architecture^[28,26], adopted in this thesis for its compatibility with printing technologies, enables efficient EDL formation by allowing the electrolyte to conform uniformly to the semiconductor surface and by minimizing ion-migration distances, resulting in a well-defined electrolyte–semiconductor interface that typically exhibits reduced hysteresis. **Figure 2.1** illustrates the conceptual cross-section the top-gated EGT

and the corresponding equivalent circuit.

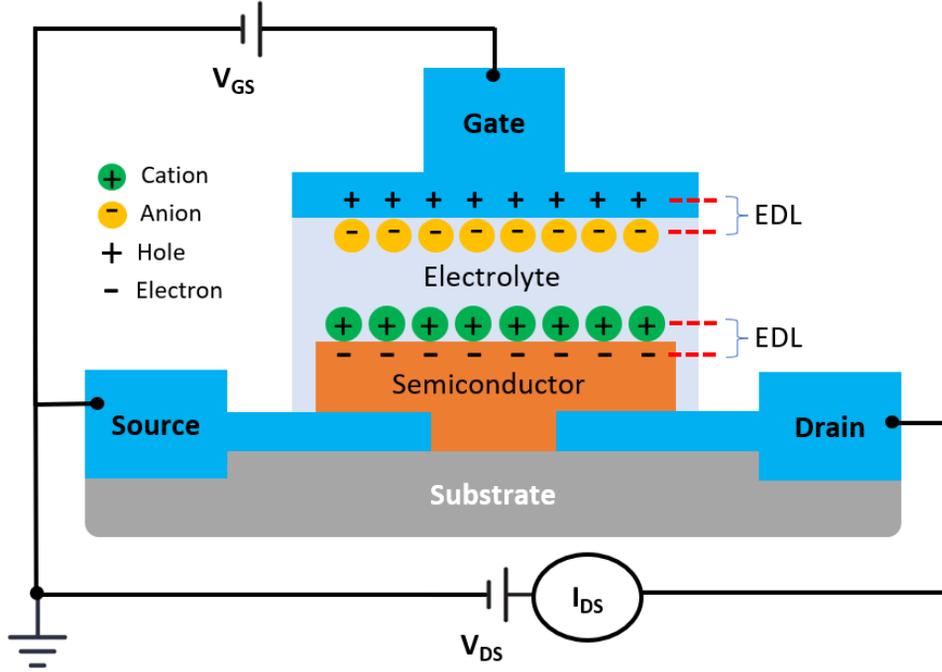


Figure 2.1: Schematic representation of a top-gated EGT, showing the source and drain electrodes, semiconductor channel, electrolyte, and gate electrode. The corresponding equivalent circuit illustrates the formation of EDL at the gate–electrolyte and semiconductor–electrolyte interfaces under an applied gate–source voltage V_{GS} , enabling electrostatic modulation of the drain current I_{DS} under an applied drain–source voltage V_{DS} .

In this structure, the EGT consists of source and drain electrodes defining the channel, a semiconductor layer, an electrolyte acting as the gate dielectric, and a gate electrode positioned on top of the electrolyte. Under an applied gate voltage V_{GS} , mobile ions in the electrolyte redistribute and accumulate at the gate–electrolyte and semiconductor–electrolyte interfaces according to the applied voltage polarity, leading to the formation of two EDLs in series^[17,27]. The resulting effective gate capacitance C_G can be expressed as^[27,26]:

$$\frac{1}{C_G} = \frac{1}{C_{\text{EDL,gate-electrolyte}}} + \frac{1}{C_{\text{EDL,semiconductor-electrolyte}}} \quad (2.1)$$

The gate-side EDL is typically large due to efficient ionic accumulation on the conductive gate surface, while the electrolyte also forms a conformal interface

with the semiconductor, enhancing ionic–electronic coupling. Since the series combination is governed by the interfacial modulation at the semiconductor side, the total gate capacitance is effectively determined by the semiconductor-side EDL. The accumulated channel charge per unit area is then given by Q ^[26,16], reflects purely capacitive field-effect modulation of the channel.

$$Q = C_G (V_{GS} - V_T) \quad (2.2)$$

The channel behavior can therefore be described using a modified field-effect expression incorporating the EDL capacitance. In the linear regime, the drain current^[26,27] can be approximated as:

$$I_{DS} = \mu C_G \frac{W}{L} (V_{GS} - V_T) V_{DS} \quad (2.3)$$

where μ is the field-effect carrier mobility, C_G is the EDL capacitance per unit area, W and L are the channel width and length, V_{GS} is the applied gate voltage, V_T is the threshold voltage, and V_{DS} is the drain voltage.

Key performance metrics follow directly from these expressions and provide a quantitative basis for evaluating EGT operation, enabling consistent and reliable extraction of device parameters. Key device parameters are obtained from the transfer (I_{DS} – V_{GS}) and output (I_{DS} – V_{DS}) characteristic curves^[26,17,26]. The threshold voltage is extracted from the I_{DS} – V_{GS} characteristics using the linear-region approximation, whereby the linear portion of I_{DS} versus V_{GS} is extrapolated to $I_{DS} = 0$ and the corresponding intercept yields the V_T . The V_T marks the onset of channel conduction, indicating the gate voltage at which measurable I_{DS} begins to flow. The field-effect mobility is extracted from the slope of I_{DS} versus V_{GS} in the linear regime using a known value of C_G . The transconductance (g_m)^[26,31], which quantifies how effectively the gate voltage modulates the drain current, is defined as:

$$g_m \equiv \frac{dI_{DS}}{dV_{GS}} \quad (2.4)$$

The mobility^[31,16] can be expressed as:

$$\mu = \frac{L}{W C_G V_{DS}} \left(\frac{dI_{DS}}{dV_{GS}} \right) \quad (2.5)$$

The on-current (I_{ON}) and off-current (I_{OFF}) ratio (I_{ON}/I_{OFF}), which defined as the ratio between the maximum on-state current and the minimum off-state current^[16], provides a measure of the switching capability of the EGT. A high I_{ON}/I_{OFF} ratio indicates effective channel modulation and low off-state leakage, both of which are important for EGT operation. The subthreshold swing quantifies the gate-voltage efficiency in the weak-inversion regime, reflecting how sharply the device transitions from the off-state to the on-state. The subthreshold swing S_S ^[26] can be expressed as:

$$S_S = \left(\frac{d \log_{10} I_{DS}}{dV_{GS}} \right)^{-1} \quad (2.6)$$

A steeper S_S enables a faster rise in drain current with gate voltage, while S_S close to the theoretical limit (e.g., 60 mV dec⁻¹ at room temperature) indicates minimal interface trapping and highly efficient gate control. The theoretical minimum $S_{S,min}$ ^[26,16] at room temperature arises from the thermal limit of carrier injection in an ideal transistor, given by:

$$S_{S,min} = \ln(10) \frac{kT}{q} \quad (2.7)$$

where k is the Boltzmann constant ($k = 1.38 \times 10^{-23}$ J K⁻¹), T is the absolute temperature ($T \approx 300$ K), and q is the elementary charge ($q = 1.602 \times 10^{-19}$ C). Hysteresis in EGT is quantified as the voltage shift between forward and reverse sweeps of the I_{DS} - V_{GS} characteristics, arising from ionic relaxation dynamics and interfacial charge trapping within the electrolyte and semiconductor layers. Overall, the combination of low-voltage operation, solution-processability, and inherent variations in electrical characteristics motivates the selection of EGTs as the principal active devices in this thesis.

Extensive research on EGTs has established the foundations for low-voltage operation through EDL gating. Foundational work by Frisbie and co-authors^[32,33], using ion-gel dielectrics with Au and ITO source/drain electrodes, demonstrated sub-2 V EDL gating with large interfacial capacitance and high transconductance, validating the efficiency of EDL-induced charge modulation. Kim *et al.*^[34] further clarified the key electrical mechanisms of electrolyte gating, showing that interfacial capacitance and ionic relaxation govern hysteresis, subthreshold behavior, and switching speed, while also emphasizing the compatibility of electrolyte with solution-processed and printed semiconductors. Complementing these general insights, Torricelli *et al.*^[35] reviewed EGT architectures and interfacial processes, emphasizing the strong coupling and low-voltage operation achievable across printed devices. Park *et al.*^[36] demonstrated aqueous electrolyte-gated IGZO transistors using Au/Cr electrodes, operating below 1 V, highlighting the effectiveness of EDL gating in oxide semiconductor channels.

Parallel electrolyte research has shown that composite solid polymer electrolytes (CSPEs) combine high ionic conductivity, low leakage, and mechanical stability. Temperature-dependent measurements of CSPE-gated indium oxide (In_2O_3) transistors have demonstrated minimal threshold-voltage drift and stable subthreshold behavior over wide temperature ranges. Complementing these material studies, Singaraju *et al.*^[31] demonstrated fully-printed metal-oxide EGTs employing printed In_2O_3 channels and solid electrolytes, reporting mobilities of $\sim 2\text{--}16 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and consistent sub-1 V operation suitable for flexible and large-area systems integration. Beyond individual devices, circuit-level demonstrations by Marques *et al.*^[29] highlighted the practical viability of oxide-based transistors with ITO electrodes, showing that printed CSPE-gated n-type In_2O_3 EGTs can be integrated into functional low-voltage circuits (operating at 0.6 V to 1 V) such as inverters, ring oscillators, and early hardware-security primitives that leverage intrinsic device variability.

Across these studies, device-to-device variations in threshold voltage, mobility, and current arising from interfacial ionic processes, electrolyte composition, and printed-film morphology are consistently reported, providing a natural entropy source for EGT-based circuit integration. Collectively, the literature establishes

CSPE-gated, n-type In_2O_3 -based top-gated transistor as highly adopted combination in EGT research, offering low-voltage operation, solution-processability, mechanical stability, and inherent-variability that make them well-suited to realize large-area printed electronics. However, the lack of stable p-type EGTs, together with the intrinsically low hole mobility (typically $< 0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)^[37] of printed p-type oxide semiconductors, limits the realization of complementary circuit architectures and therefore this thesis focuses on n-type EGT devices.

In this thesis, two complementary EGT architectures are employed, and their synergy enables reliable circuit benchmarking while supporting the long-term scope of fully-printed security primitives. Hybrid-printed EGTs, incorporating laser-ablated ITO source, drain, and gate electrodes together with inkjet-printed In_2O_3 , CSPE, and PEDOT:PSS gate contact layers on glass substrate, provide controlled geometry and electrical stability required to implement and characterize inverter-based PUF circuit. Fully-printed EGTs, combining aerosol jet printed Au electrodes with inkjet-printed functional layers on glass and polyimide substrate, are explored in parallel as a feasibility demonstration toward future fully-printed PUF.

2.1.2 Physically Unclonable Functions

The PUFs are device-level hardware security primitives that leverage intrinsic process-induced physical variations to generate identifiers that are unique, reproducible, irreversible, and resistant to cloning^[38]. These characteristics make PUFs effective primitives for secure identification, authentication, and trust establishment in electronics at the hardware level. In principle, a PUF implements a physical one-way function that maps an input as challenge C to a corresponding response R , reflecting the underlying physical randomness that serves as the device's entropy source. A conceptual illustration of fundamental characteristics of a PUF is shown in **Figure 2.2**. In the first block, a PUF implements the mapping $R = f_{\text{PUF}}(C)$ ^[38,39], where the forward evaluation is straightforward but the inverse mapping is computationally infeasible, reflecting the one-way nature of the

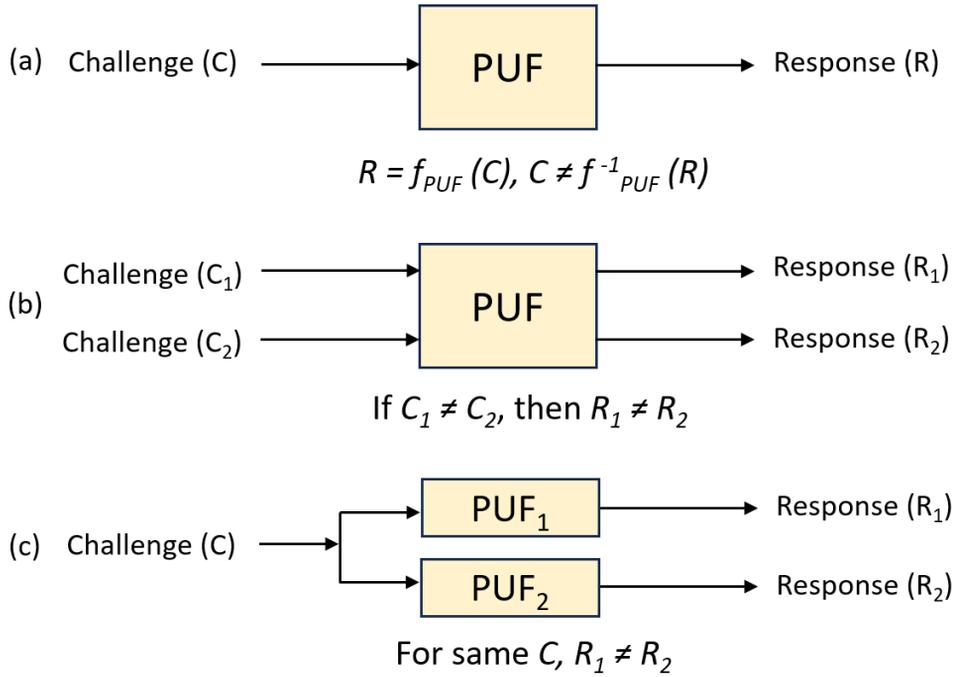


Figure 2.2: Conceptual illustration of key PUF behavioral properties.

- (a) Challenge–response mapping: PUF implements the one-way function $R = f_{PUF}(C)$, where the forward mapping is easy but inversion is computationally infeasible.
- (b) Challenge uniqueness: different challenges C_1 and C_2 applied to the same PUF generate distinct responses R_1 and R_2 .
- (c) Device uniqueness: applying the same challenge C to two nominally identical PUF instances yields different responses due to inherent physical variations, enabling device-level unclonability.

PUF. In the second block, two different challenges C_1 and C_2 applied to the same PUF yield distinct responses R_1 and R_2 , demonstrating challenge uniqueness and contributing to unpredictability as the responses to new challenges cannot be inferred from previously observed pairs. In the third block, the same challenge applied to two nominally identical PUF instances produces different responses due to intrinsic fabrication-induced variations, demonstrating device uniqueness, which underpins the unclonability of the PUF.

Depending on the mechanism by which the entropy is extracted, device-based electronic PUFs can be broadly categorized into analog and digital architectures^[40,41] (**Figure 2.3**). Digital PUFs^[41,40] rely on bistable elements or precise timing differences, such as latches, flip-flops, or delay paths, to generate discrete binary responses. These approaches typically require tight control over switching

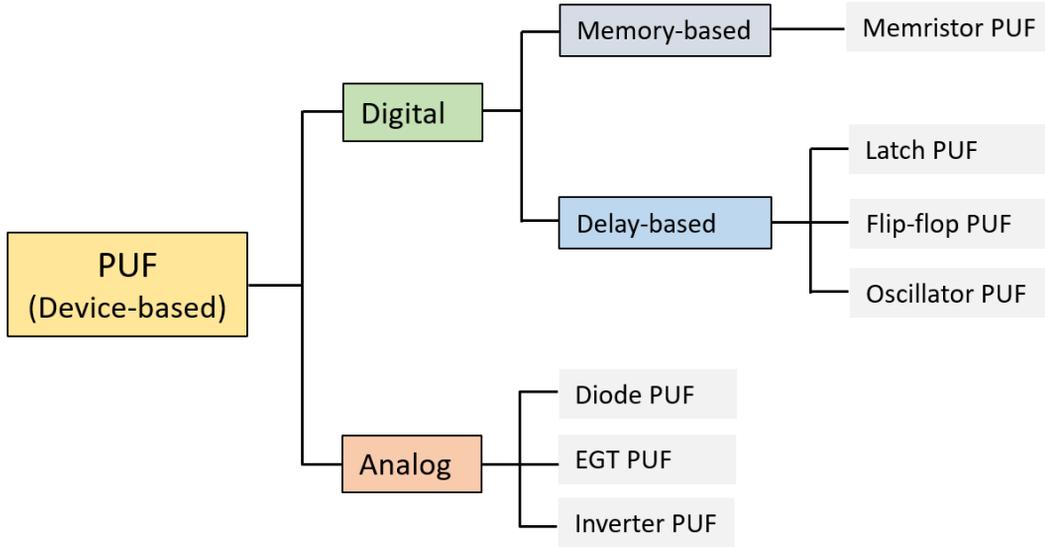


Figure 2.3: Classification of device-based PUFs into analog and digital architectures, based on the underlying entropy-extraction mechanism.

thresholds, noise margins, and timing resolution, which is challenging to achieve reliably using printed electronics and electrolyte-gated devices. In contrast, analog PUFs^[40] derive their entropy from continuous-valued device characteristics, such as transistor threshold voltage shifts, current–voltage variations, or steady-state inverter output levels. This makes analog PUFs inherently more compatible with printed electronics, where process-induced variations are pronounced and continuous in nature. Within this category, single-device structures (e.g., diode or single-transistor PUFs) offer limited entropy, whereas inverter-based PUFs combine an EGT with a load resistor, thereby incorporating local variations of two independently varying elements and providing a multidimensional robust entropy source.

To clarify the operating principle underlying the inverter-based PUF employed in this thesis, the behavior of a single resistor-loaded inverter is first considered. **Figure 2.4a** illustrates a single inverter stage comprising an n-type EGT and a pull-up resistor R_D , which forms the fundamental building block of the PUF architecture. In this circuit, the source terminal (S) of the EGT is connected to circuit ground (GND), while the gate (G) is driven by the input voltage V_{in} , and the drain node (D) serves as the inverter output V_{out} , connected to the supply voltage V_{DD} through the pull-up resistor R_D .

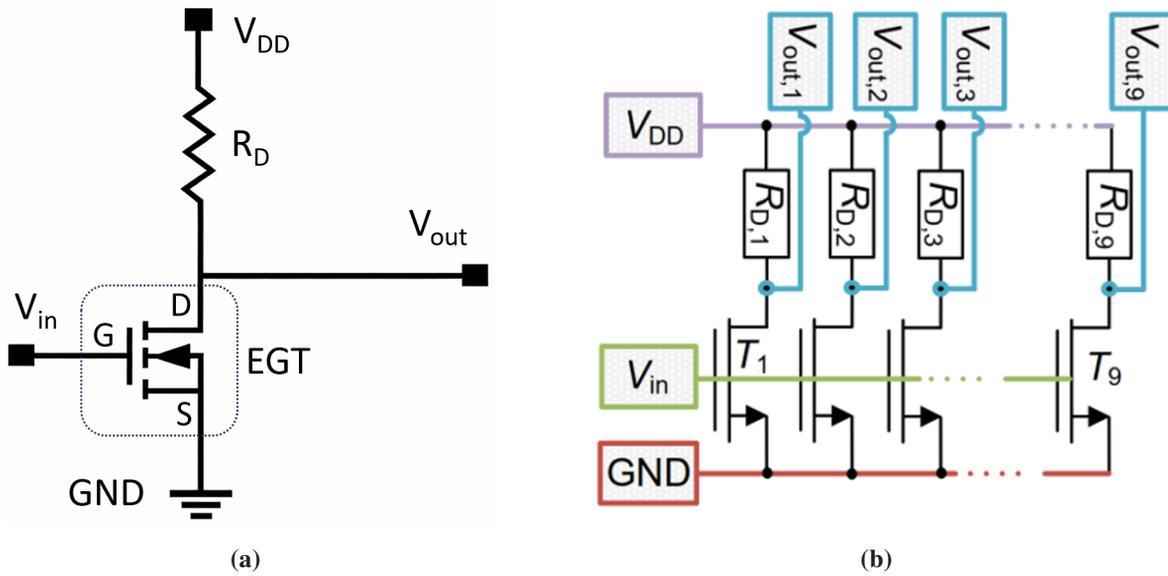


Figure 2.4: Schematic representation of the inverter-array PUF architecture. (a) Single inverter circuit consisting of an n-type EGT and a pull-up resistor R_D . The gate (G) is driven by V_{in} , the source (S) is connected to GND, and the drain (D) forms the output node V_{out} , which is pulled up to V_{DD} through R_D . (b) Nine-inverter array driven by a common V_{in} and supplied by shared V_{DD} and GND connections, providing individual output nodes $V_{out,i}$ ($i = 1, \dots, 9$) for analog PUF extraction. *Reproduced with permission from^[19], © IEEE 2023.*

When V_{in} is below the effective threshold voltage of the EGT, the transistor remains in the off-state and conducts negligible current. Under this condition, the output node V_{out} is pulled toward V_{DD} through R_D , resulting in a high output level. When V_{in} exceeds the threshold voltage, the EGT turns on and provides a conductive path from V_{out} to GND. As a result, current flows from V_{DD} through R_D and the EGT channel, pulling V_{out} down to a lower steady-state voltage. This inversion behavior defines the basic operation of the resistor-loaded inverter, where the resistor defines the high output state and the EGT actively drives the output low when conducting.

Building upon this single-inverter operation, the PUF architecture extends the concept to an array of nominally identical inverter stages. **Figure 2.4b.** illustrates a nine-inverter array in which all inverters share a common input voltage V_{in} , supply voltage V_{DD} , and ground (GND), while each inverter produces an independent output voltage $V_{out,i}$ ($i = 1, \dots, 9$). Under a fixed input voltage V_{in} , each inverter in the array settles to a steady-state output voltage determined

by its individual electrical characteristics. Although all inverters are fabricated using the same design and material stack, intrinsic process-induced variations in transistor threshold voltage, carrier mobility, and pull-up resistor geometry lead to measurable differences in $V_{\text{out},i}$ ($i = 1, \dots, 9$) across the array. These analog output variations form a reproducible entropy source that is intrinsic to the hardware.

To convert these analog output levels into a PUF identifier key, the outputs are processed using pairwise comparison^[18,39]. Each pair of inverter outputs (i,j) yields one binary value ($b_{i,j}$) according to:

$$b_{ij} = \begin{cases} 1, & V_{\text{out},i} > V_{\text{out},j} \\ 0, & V_{\text{out},i} \leq V_{\text{out},j} \end{cases} \quad (2.8)$$

For an array containing $N = 9$ inverters, this results in PUF key with bit length (L)^[19]:

$$L = \frac{N(N-1)}{2} = 36 \quad (2.9)$$

This 36-bit response represents an effective trade-off between entropy for distinguishing devices, circuit complexity, and the readout compatibility of the ASIC-in-foil architecture targeted in this thesis.

PUF Evaluation Metrics

The quality of an inverter-array PUF is commonly assessed using established PUF metrics that describe the entropy, robustness, and stability of the response generation mechanism. Standard metrics include uniqueness, reliability, bit aliasing, and bit error rate (BER)^[38]. Uniqueness characterizes how well responses from different PUF instances can be distinguished and is typically evaluated using the average inter-device Hamming distance, with an ideal value close to 50 %. Bit aliasing evaluates whether individual bit positions exhibit a statistical bias toward logical ‘0’ or ‘1’ across a population of devices^[38]. Both metrics inherently require evaluation across multiple PUF instances. In this thesis, a single printed

inverter-array PUF instance is investigated as part of a hybrid system-in-foil architecture. Consequently, the evaluation focuses on reliability-related metrics, which are directly relevant for system-level operation and repeated readout under varying environmental conditions.

Reliability is quantified using the BER, which captures the stability of the PUF response when the same challenge is applied repeatedly. For a given PUF instance n , a reference response $R_{\text{ref},n}$ is defined as the most frequently occurring response among a set of repeated measurements obtained under a fixed challenge condition. In this thesis, the challenge corresponds to a fixed inverter input bias voltage V_{in} . The reference response serves as the baseline against which all repeated responses are compared. The Hamming distance (HD)^[39] between two binary response vectors R_a and R_b , each of length L , is defined as:

$$\text{HD}(R_a, R_b) = \sum_{i=1}^L R_a[i] \oplus R_b[i] \quad (2.10)$$

where \oplus denotes the XOR operation. The HD therefore represents the number of bit positions at which the two responses differ. The BER for PUF instance n is computed by averaging the normalized HD between the reference response and W repeated response measurements^[39]:

$$\text{BER}_n = \frac{1}{W} \sum_{w=1}^W \frac{\text{HD}(R_{\text{ref},n}, R'_{n,w})}{L} 100 \% \quad (2.11)$$

where n denotes the PUF instance index (with $n = 1$ in this thesis), $R'_{n,w}$ is the response obtained in the w -th repetition, L is the response length (36 bits), and W is the number of repeated measurements. The bit error rate represents the probability of bit flips caused by noise, temperature variation, or system-level perturbations^[39]. It is a widely accepted metric for assessing PUF reliability, particularly in embedded and hybrid systems where repeated readout stability is critical. The bit error rate directly reflects the robustness of the analog entropy originating from device-to-device and intra-array variability of the inverter transfer characteristics.

However, in the domain of printed electronics, the state of the art still lacks systematic investigations into how array size, layout compactness, and device uniformity influence entropy extraction in EGT-based PUF architectures. A printed inverter-array PUF closely related to this thesis was previously reported by Scholz *et al.*^[19], validating that printed EGT-based inverters provide sufficient device-to-device variation for stable analog PUF identifiers. Their thesis established the feasibility of using a printed inverter array as a PUF. Building on that conceptual foundation, this thesis develops a printed inverter-array PUF tailored for integration with an ASIC-in-foil architecture. For this purpose, the inverter layout and contact pad pitch are redesigned to match the ASIC's input interface, and a conductive PEDOT:PSS-based gate contact is employed in EGTs, resulting in modified inverter operating points and output-voltage distributions. These adaptations preserve the overall nine-inverter architecture while preparing the printed PUF for reliable analog readout and system-level operation within the hybrid system-in-foil architecture.

2.1.3 Temperature Sensor

Temperature sensors are essential components in modern systems ranging from wearable electronics^[42,43] and biomedical devices^[44,45] to automotive and industrial applications. In the automotive sector, flexible temperature sensors play a vital role in real-time monitoring of thermal variations along soft polymeric tubes, curved housings, and confined surfaces where conventional rigid sensors cannot be integrated^[46,43]. Among the various types of temperature sensors such as thermocouples, thermistors, and resistive temperature sensors (RTSs)^[47,42,43], the RTS is particularly attractive due to its simple design, linear response, and compatibility with printed and flexible electronics^[48,49]. The operation of an RTS is based on the temperature-dependent variation in the electrical resistance of a conductive material, which follows an approximately linear relationship within a moderate temperature range. This dependence can be expressed as^[50,45]:

$$R(T) = R_0 [1 + \alpha(T - T_0)] \quad [\Omega] \quad (2.12)$$

where $R(T)$ is the resistance at a measured temperature T , R_0 is the initial resistance at a defined reference temperature ($T_0 = 20\text{ }^\circ\text{C}$ in this thesis), and α is the temperature coefficient of resistance (TCR). The TCR quantifies the fractional change in resistance per unit temperature and is defined as^[50,43]:

$$\alpha_T = \frac{1}{R_0} \frac{R - R_0}{T - T_0} = \frac{1}{R_0} \frac{\Delta R}{\Delta T} \quad [^\circ\text{C}^{-1}] \quad (2.13)$$

where α_T is the TCR of the RTSs in $^\circ\text{C}^{-1}$, R denotes the resistance at the maximum reference temperature ($T_{\text{max}} = 80\text{ }^\circ\text{C}$ in this thesis), and ΔR and ΔT represent the change in resistance and temperature, respectively. The sensitivity (S) of the RTSs is defined as the absolute change in resistance per degree Celsius and can be expressed as^[45]:

$$S = \frac{R_{\text{max}} - R_0}{T_{\text{max}} - T_0} = \frac{\Delta R}{\Delta T} = \alpha_T R_0 \quad [\Omega \cdot ^\circ\text{C}^{-1}] \quad (2.14)$$

A higher TCR or a larger baseline resistance R_0 results in greater sensitivity, demonstrating the importance of material selection in determining the accuracy and stability of the printed RTSs.

Various conductive materials, including copper (Cu), nickel (Ni), silver (Ag), gold (Au), and platinum (Pt), have been investigated as temperature-sensing elements^[51,44,42]. However, their suitability depends on oxidation resistance, thermal stability, and compatibility with flexible substrates^[44,52]. Cu and Ni offer relatively high TCRs but are highly susceptible to oxidation and long-term instability, while Ag provides excellent conductivity but suffers from surface migration and oxidation^[49,53]. Au is chemically inert but demands high sintering temperatures and exhibits moderate TCR values^[49].

In contrast, Pt as a temperature-sensing element has drawn significant attention due to its superior combination of electrical and thermal properties such as stable positive TCR ($\sim 3.85 \times 10^{-3}\text{ }^\circ\text{C}^{-1}$), high sensitivity ($0.385\text{ } \Omega \cdot ^\circ\text{C}^{-1}$ for bulk *Pt100* and $3.85\text{ } \Omega \cdot ^\circ\text{C}^{-1}$ for bulk *Pt1000*)^[22,23], linear resistance change with temperature over a broad range, and oxidation stability owing to its high

melting point^[44,54]. These attributes make Pt as the preferred choice for accurate and repeatable temperature measurements across a wide range of operating environments, including automotive and industrial systems.

Conventional Pt temperature sensors, such as rigid wire-wound *Pt100* / *Pt1000* elements, exhibit bulk-like density and conductivity serve as reference benchmarks^[11], but their fabrication involves resource-intensive, high-temperature vacuum processes that are incompatible with flexible substrates^[46]. In contrast, the ability to process Pt nanoparticles into conductive films at low sintering temperatures offers a lightweight and cost-effective route toward flexible temperature sensing^[55]. Nanoparticle-based Pt inks can be precisely deposited using additive manufacturing techniques, particularly inkjet printing, which enables accurate control over geometry and layer thickness, while minimizing material waste and process complexity. Upon sintering, the printed Pt forms dense metallic networks that preserve the intrinsic thermal linearity and stability of Pt, ensuring reliable integration onto polymeric surfaces. This approach bridges the high accuracy of conventional Pt sensors with the mechanical flexibility required for emerging soft electronic and automotive applications.

In this thesis, low-temperature inkjet-printed Pt based resistive temperature sensors are developed and optimized to achieve stable, linear operation between 20 °C and 80 °C, suitable for attachment to soft polymeric automotive tubes for localized thermal monitoring. The sensors are fabricated on polyimide substrates, chosen for their high temperature tolerance, mechanical robustness, and dimensional stability, which allow reliable operation under thermal cycling and bending. This combination of material properties, process compatibility, and functional stability establishes printed Pt as a promising candidate for flexible, high-precision temperature sensing in automotive applications.

2.1.4 Hybrid System-in-Foil

Hybrid system-in-foil technology enables the co-integration of high-performance silicon integrated circuits (ICs) with the material versatility and mechanical compliance of printed electronics, allowing both domains to operate synergistically within a single flexible foil^[25,24]. Its core principle is to combine the computational strength and reliability of silicon ICs with the geometric flexibility, low-power operation, and large-area scalability of printed electronics^[56], yielding lightweight, energy-efficient, and highly conformable systems suitable for automotive, wearables, biomedical interfaces, and emerging IoT applications.

However, a fundamental barrier arises from the mechanical properties of bare silicon CMOS dies or chips as delivered from foundries, which remain inherently bulky and rigid, making them incompatible with thin flexible substrates such as polyimide. The bare dies typically retain thicknesses on the order of a few hundred micrometers after dicing, with reported values ranging 400–500 μm ^[24,57,58] depending on the foundry process and application requirements, reflecting their origin from standard CMOS wafers (e.g., 200 mm / 300 mm wafers, processed at an initial thicknesses of $\approx 725 \mu\text{m}$ / $790 \mu\text{m}$)^[57,59]. At these thicknesses, silicon exhibits a bending radius of several centimeters, creating a severe stiffness mismatch between the die and the polymer foil and inducing interfacial stress that can lead to metallization cracking, delamination, and interconnect failure. Packaged ICs are even bulkier, often reaching millimeter-scale thicknesses, and are entirely incompatible with thin-foil. Furthermore, bare CMOS dies are normally designed for rigid packaging (e.g., wire-bond, flip-chip bond)^[57] rather than direct contact with printed components, whose relatively large contact pitch must be accommodated. For these reasons, transforming a bulky CMOS die into a mechanically compliant ultra-thin chip through backside thinning is essential for reliable hybrid system-in-foil implementation. Thinning is carried out through a controlled sequence of mechanical grinding to remove bulk silicon, followed by fine grinding to minimize subsurface damage, and chemical–mechanical polishing to eliminate micro-cracks and restore a smooth, defect-free backside^[60,59].

Additional etching steps may be applied to remove residual stress-inducing layers and improve mechanical resilience.

Literature consistently reports that bare-die thinning process effectively reduces silicon thickness into the ultra-thin chip regime to tens of micrometers, typically 20–60 μm [24,61,62,57,59], where the chips become bendable to millimeter-scale radii and remain compatible with flexible polyimide foil integration and electrical interfacing with printed components for creating functional hybrid systems. In this thickness range, the bending stiffness decreases by orders of magnitude compared to the bare die, enabling the chip to conform to the foil without inducing harmful mechanical loads. Burghartz *et al.* demonstrated the embedding of CMOS dies thinned below 50 μm into polyimide foils, achieving reliable performance under bending and thermal cycling [56]. In related work, Elsobky *et al.* [63] implemented an electronic-skin that employs CMOS dies thinned to about 20–30 μm , integrated into polyimide foil and interconnected with sensor elements. A broader technological perspective was presented by Khan *et al.* [60], who reviewed multiple thinning approaches capable of producing dies thinner than 25 μm and even reported semitransparent flexible silicon for hybrid electronic applications. Malik *et al.* [57] demonstrated die-level thinning of 500 μm wafers down to 60 μm for flip-chip bonding onto flexible substrates using conductive adhesives, achieving reliable interconnect performance. Together, these studies establish the scientific and technological foundation for integrating ultra thin CMOS chips with printed electronics directly within polyimide foils, enabling hybrid systems that preserve mechanical integrity and stable operation.

To illustrate the concept of hybrid system-in-foil, **Figure 2.5** depicts a representative architecture in which an ultra-thin silicon chip is embedded within a flexible polymer substrate and electrically connected to distributed functional elements on the foil. The embedded chip together with a wireless microcontroller provides core functionalities such as digital processing, sensor readout, and communication, while the surrounding foil integrates on-foil sensors, printed circuits, an on-foil antenna, a thin-film battery, photovoltaic energy-harvesting elements, and a flexible display. Electrical interconnection is achieved through foil-level interconnects that route power and signals throughout the flexible foil. This architecture

demonstrates how silicon-level computation can coexist with printed sensing, energy management, and interface elements within a mechanically compliant foil. Despite these advances, previously reported hybrid system-in-foil remain predominantly sensing-oriented, typically integrating ultra-thin CMOS chips with humidity or strain sensors, bio-monitoring patches, printed antennas or logic circuit^[58,63,60]. However, the literature has not demonstrated the co-integration of printed hardware-security primitives and printed temperature sensing within a single embedded ASIC-in-foil architecture.

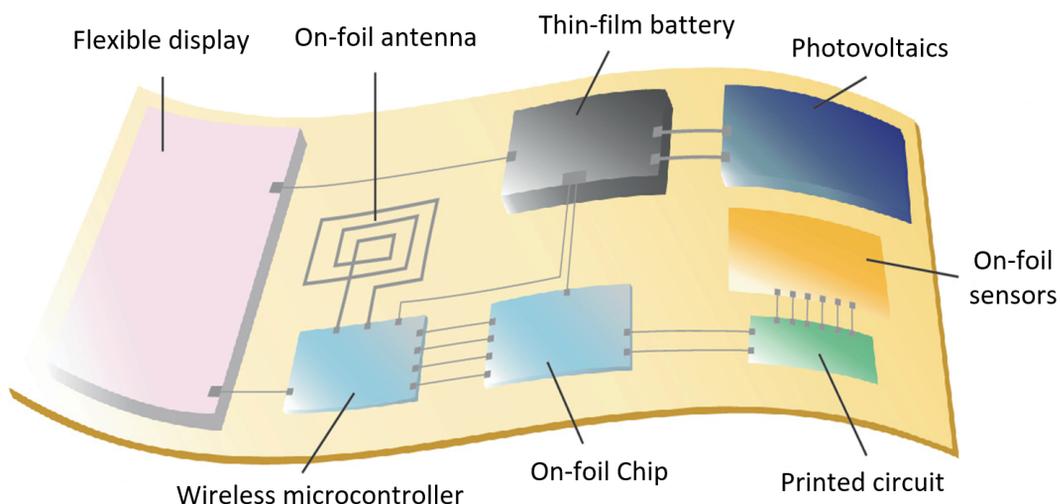


Figure 2.5: Conceptual hybrid system-in-foil architecture showing an embedded ultra-thin silicon chip and wireless microcontroller interconnected with printed and thin-film components, including on-foil sensors, printed circuits, antenna, thin-film battery, photovoltaic energy-harvesting elements, and a flexible display, integrated on a flexible polymer substrate. The schematic illustrates the core principle by which ultra-thin chip and printed electronics coexist within a mechanically compliant foil architecture. *Reproduced with permission from^[25], © Springer Nature 2022.*

In this thesis, the hybrid system-in-foil concept is advanced toward secure and multifunctional systems for automotive applications. A custom 180 nm CMOS ASIC (bare die), delivered at 230 μm and backside-thinned to 30 μm , is embedded into a polyimide foil as the processing core. On the same foil, a printed inverter-array PUF and a printed Pt-based resistive temperature sensor for automotive sensing in the 20°C – 80°C range are co-integrated. Together, these components combine the flexibility of printed electronics with the security and

computational capability of thinned silicon ASIC, forming a hybrid system-in-foil architecture. This thesis demonstrates the first foil-embedded ASIC that directly interfaces with both printed security and sensing elements, enabling low-power PUF-based secure identification and automotive-oriented sensing.

2.2 Summary

This chapter outlined the theoretical foundations and state-of-the-art developments of the printed and hybrid electronic devices investigated in this thesis. It discussed the operating principles, material requirements, and technological progress in EGTs and hardware security primitives such as PUFs, along with RTSs for flexible sensing applications. Furthermore, the chapter reviewed recent advances in hybrid system-in-foil integration, emphasizing the combination of printed functional layers with embedded silicon ASICs. The literature analysis identified key challenges such as achieving stable electrolyte gating, reliable printed device and circuit performance, and robust multifunctional integration, which motivate the experimental investigations presented in the subsequent chapters. Finally, the concept of hybrid integration bridging printed front-end devices with silicon back-end electronics was established as the technical framework for the system-in-foil architecture developed in this thesis.

3 Materials and Methods

This chapter describes the experimental framework for the fabrication and characterization of the printed and hybrid electronic devices developed in this thesis. It details the printing and patterning techniques used to define device structures, including inkjet printing, aerosol jet printing, and laser ablation. The preparation of functional inks and substrates, along with thermal and furnace-based post-processing steps, is described. In addition, the structural, morphological, and electrical characterization methods employed for device evaluation are outlined. This chapter establishes the methodological basis for the fabrication and analysis of the printed transistors, security circuits, and sensors presented in the following chapters.

3.1 Techniques for Printed Electronics

3.1.1 Inkjet Printing

Inkjet printing (IJP) is a non-contact, maskless, and digitally controlled additive manufacturing technique that deposits picoliter-sized droplets of functional inks onto a wide range of substrates with high spatial precision^[11,64]. It has emerged as a key technology in printed and flexible electronics, enabling cost-effective, scalable deposition of conductive, semiconductive, and electrolyte layers for electronic devices and circuits. Inkjet printing operates by ejecting controlled ink droplets through micron-sized nozzles, where droplet formation, trajectory, and deposition depend on the combined effects of ink rheology, surface tension, substrate surface energy, and the actuation waveform driving the printhead^[9,64,65].

Inkjet systems are generally classified into Continuous Inkjet (CIJ) and Drop-on-Demand (DoD) modes^[8,65]. In CIJ printing, a continuous stream of ink is generated and electrostatically deflected towards or away from the substrate according to the desired pattern. Although suitable for high-throughput printing, CIJ is less common in printed electronics due to material waste and limited compatibility with functional inks^[8]. In contrast, DoD printing ejects droplets only when required, allowing precise material deposition and minimal ink consumption. DoD actuation is achieved either through thermal actuation, where localized heating forms a vapor bubble that expels the droplet, or piezoelectric actuation, where a piezoelectric element deforms under a voltage pulse, generating a pressure wave that ejects the droplet through the nozzle^[8,65,11]. The latter is preferred due to its precise droplet control without thermal stress, making it compatible with temperature sensitive inks and substrates. The ejected droplet's velocity and volume depend on the waveform amplitude, pulse frequency, drop spacing, and nozzle geometry^[9,66]. **Figure 3.1** illustrates the working principle of piezoelectric inkjet printing, where a pulsed voltage applied to the actuator enables precise droplet ejection and deposition on the substrate.

Following ejection, stable droplet formation requires balancing inertial, viscous, and surface-tension forces, typically represented by three key dimensionless numbers such as Reynolds number (Re), Weber number (We), and Ohnesorge number (Oh). A combined printability parameter, the inverse Ohnesorge number Z ^[11,65], is used to evaluate the printability of an ink.

$$Z = \frac{1}{Oh} = \frac{Re}{\sqrt{We}} \quad (3.1)$$

For stable jetting without satellite droplets, the optimal regime lies within $1 < Z < 10$. Inks with $Z < 1$ are too viscous to eject, whereas those with $Z > 10$ tend to form satellite droplets, resulting in poor resolution^[14]. Therefore, careful tuning of ink viscosity (typically $8\text{--}20 \text{ mPa}\cdot\text{s} \approx 8\text{--}20 \text{ cP}$) and surface tension ($25\text{--}40 \text{ mN}\cdot\text{m}^{-1}$) is essential for reliable jetting^[65,11].

After ejection, each droplet undergoes flight, impact, and spreading before solidifying on the substrate. The substrate's surface energy and contact angle govern the

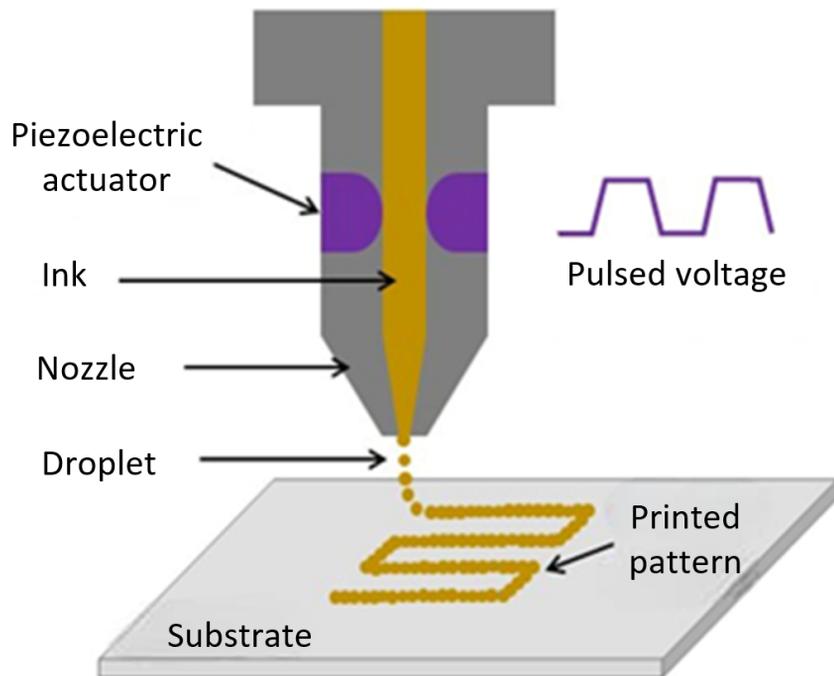


Figure 3.1: Schematic illustration of the piezoelectric drop-on-demand inkjet printing mechanism. A pulsed voltage applied to the piezoelectric actuator deforms the ink chamber, generating a pressure pulse that ejects picoliter droplets through the nozzle to form a printed pattern on the substrate. *Reproduced (modified labels) with permission from^[67], © IOP Publishing 2019.*

wetting behavior, while parameters such as droplet spacing, substrate temperature, and applied waveform influence film continuity and morphology^[8]. Defects such as nozzle clogging, satellite droplets or coffee-ring effects may appear due to improper ink-substrate interaction or non-uniform drying^[67,9]. These are mitigated by tuning ink rheology, employing solvent mixtures, viscosity modifiers, applying surface treatments (cleaning) and post-processing (thermal treatment) to achieve dense and crack-free films.

Overall, inkjet printing provides a versatile, digitally reconfigurable, and material-efficient route for fabricating multilayer, fully-printed electronic devices, offering precise patterning, low material waste, and compatibility with a wide range of functional inks essential for scalable printed and flexible electronic systems.

3.1.2 Aerosol Jet Printing

Aerosol jet printing (AJP) is an advanced non-contact, mask-less additive manufacturing technique used for the high-resolution deposition of functional materials. Unlike inkjet printing, AJP enables patterning with feature sizes down to sub-10 μm under optimized conditions and accommodate inks with viscosities ranging from 1 to 1000 cP^[12,68,69]. This versatility makes it particularly suitable for defining metallic electrodes, circuit interconnects, and other micro-structures with precise thickness and line-width control. The overall working principle of the AJP process is illustrated in **Figure 3.2**, showing the key components involved in aerosol generation, gas transport, focusing, and deposition.

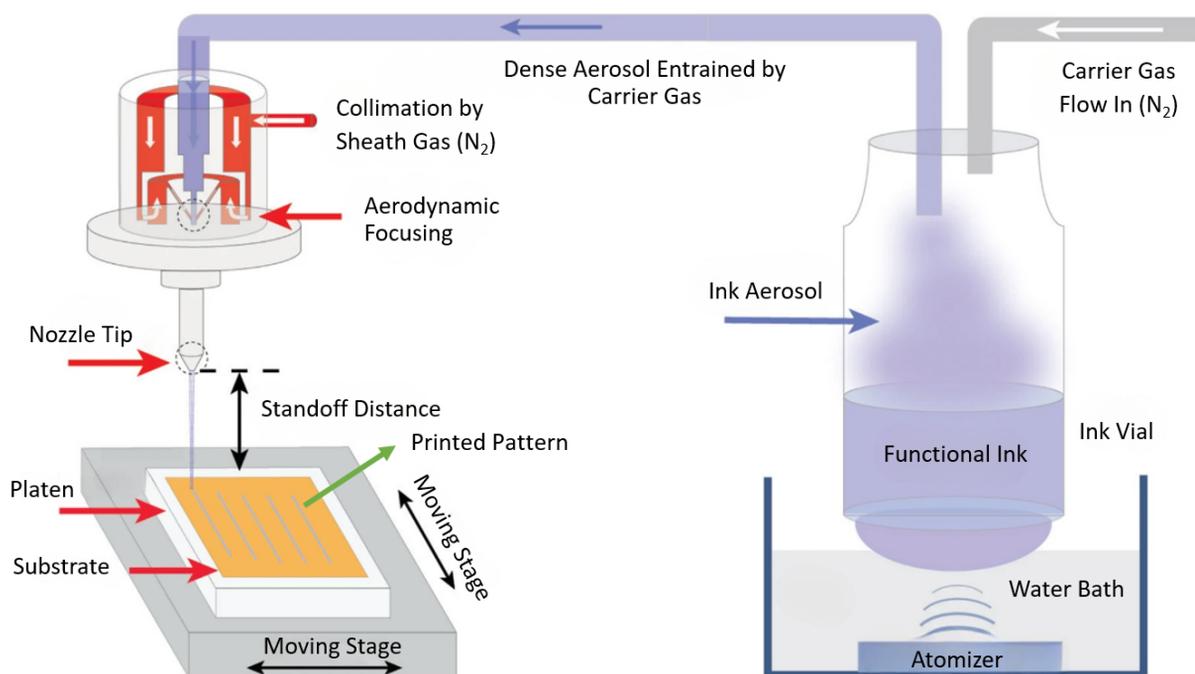


Figure 3.2: Schematic of aerosol jet printing systems showing ink atomization, carrier and sheath gas flow, and focused jet impingement on the substrate. *Reproduced (minor labeling modification) with permission from^[66], © Springer Nature 2024.*

The AJP process begins with aerosol generation, where the functional ink is atomized using either an ultrasonic or pneumatic atomizer to create a dense mist of microdroplets typically 1 μm to 5 μm in diameter^[70,68]. The resulting aerosol is

entrained in a carrier gas, commonly nitrogen, and transported toward the deposition head. A concentric sheath gas flow surrounds the aerosol stream, providing aerodynamic focusing that collimates it into a narrow, well-defined beam with a controllable diameter between 10 and 100 μm ^[12,68]. The focused aerosol jet is then deposited onto the substrate without any physical contact, allowing conformal printing on rigid, flexible, and planar or slightly curved surfaces. The substrate is mounted on a computer-controlled moving stage, enabling precise pattern definition with controlled standoff distance and printing speed. It can be heated between 25 and 200 °C to promote solvent evaporation and improve film uniformity.

During deposition, several process parameters critically influence the printed feature quality, including the sheath-to-carrier gas ratio, standoff distance, printing speed, and substrate temperature, which collectively determine aerosol jet focus, line width, edge definition, and film morphology^[68,12,70,66]. Ultrasonic atomizers are typically employed for low-viscosity inks, while pneumatic atomizers are preferred for higher-viscosity formulations^[12]. AJP is compatible with a wide range of materials such as metal nanoparticle inks, semiconducting oxides, and polymers, making it a versatile platform for printed and flexible electronics^[66,12]. Despite its advantages, several challenges can affect the printing quality, including droplet coalescence, coffee-ring formation, nozzle clogging, and instabilities in aerosol flow^[12,70]. Process optimization involves adjusting ink rheology, gas flow ratios, and substrate surface energy to achieve uniform, defect-free films with consistent electrical and morphological properties.

Overall, the non-contact and maskless nature of AJP bridges the gap between inkjet printing and microfabrication, offering a controllable, high-resolution, and material-flexible deposition process for printed and flexible electronic systems.

3.1.3 Laser Ablation

Laser ablation is a mask-less, no-contact micro-fabrication process that enables the precise removal of thin films or material layers from a substrate using high-energy laser pulses. In printed electronics, it serves as an essential subtractive process for defining electrode geometries and isolating conductive paths in metallic or oxide films without direct contact or chemical etchants^[71,72]. The sequence of physical events involved in this process is schematically illustrate in **Figure 3.3**.

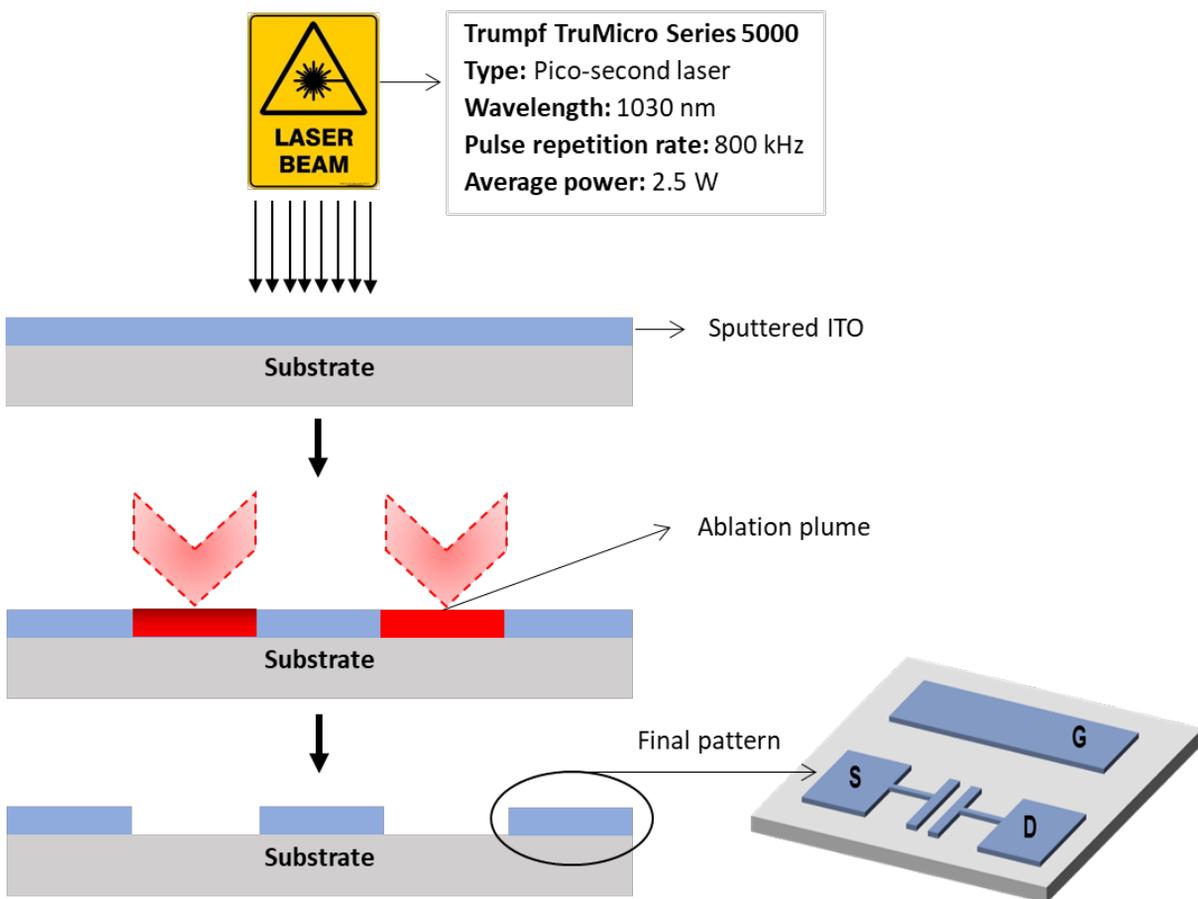


Figure 3.3: Schematic of the laser-based patterning of sputtered ITO films. A picosecond laser locally removes the ITO layer, generating a transient material plume and electrically isolating predefined regions on the substrate. The remaining ITO defines the final electrode geometry, forming the source (S), drain (D), and gate (G) electrodes used in EGT fabrication.

As shown schematically, a collimated, focused laser beam impinging on the ITO-sputtered film layer on glass substrate. Once the laser fluence exceeds the ablation

threshold of the material, rapid energy absorption induces localized heating and vaporization of the target area^[73,71]. The ejected vaporized material forms an ablation plume, thereby removing the film from irradiated regions and creating finely defined electrode patterns electrode geometries (e.g., source, drain, and gate) with excellent edge quality^[72,71]. The process was performed using a pico-second laser system operating at a wavelength of 1030 nm, with a pulse repetition rate of 800 kHz and an average power of 2.5 W.

The quality and precision of the ablation process are governed by several interdependent parameters, including laser wavelength, pulse duration, fluence, repetition rate, scanning speed, and spot size^[73,71]. In this thesis, the near-infrared wavelength of 1030 nm was chosen to achieve efficient absorption in ITO film, while the pico-second pulse regime ensured localized energy confinement within the irradiated region and minimal thermal diffusion on the substrate. The repetition rate and scanning speed were optimized to control pulse overlap and ablation depth, and accurate beam focusing was maintained to achieve consistent feature definition and high lateral resolution. Under optimized conditions, laser ablation yields trench widths of 10 μm to 30 μm and depths of 100 nm to 300 nm, depending on film thickness and applied laser fluence^[71]. This process is inherently reproducible, scalable, and compatible with both rigid and flexible substrates, making it highly suitable for advanced printed electronics. Despite its precision, laser ablation may induce undesired effects such as local thermal damage, debris re-deposition, or substrate delamination^[73,74]. These can be mitigated by maintaining the fluence slightly above the ablation threshold, performing multiple low-energy scans instead of a single high-energy exposure, and employing assist gases such as nitrogen or argon to remove ejected particles efficiently. With appropriate process optimization, smooth edges and defect-free pattern transfer can be consistently achieved, ensuring electrical and structural integrity of the patterned features.

In summary, laser ablation provides a versatile, mask-less, and non-contact approach for the fine structuring of thin-film electrodes in printed electronics. Its integration with inkjet printing enables hybrid additive–subtractive fabrication

workflows, which are crucial for realizing printed circuits with high precision and reliable interconnect architectures.

3.2 Materials for Printed Electronics

This section describes the functional materials employed for the fabrication of printed electronic devices and circuits in this thesis. The materials are grouped according to their electrical function, including conductive materials for electrodes and interconnects, semiconducting materials for active device channels, and electrolyte for gate electrical isolation. For each material, the ink formulation, key physical properties such as viscosity, and suitability for the selected printing techniques (e.g., inkjet and aerosol jet printing) are discussed to establish a clear link between material choice, process compatibility, and device functionality.

3.2.1 Conductive Materials

Pt Ink

The Pt nanoparticle ink, used as the active sensing element for printed temperature sensors, was synthesized in-collaboration with Leibniz Institute for New Materials [Saarbrücken, Germany] via a bottom-up chemical reduction process. Platinum(II) bis(acetylacetonate) [360 mg] and branched polyethyleneimine [1.5 g, $M_w = 25$ kDa] were dissolved in a solvent mixture of 2-(2-ethoxyethoxy) ethanol [48 mL] and ethylene glycol [12 mL], heated to 200 °C at a rate of 10 °C · min⁻¹ for 30 minutes to ensure complete reduction of the platinum precursor. The resulting nanoparticles (15–25 nm, TEM confirmed in **Figure 3.4**) were isolated by centrifugation (10,000 rpm, 60 minutes) and redispersed at a concentration of 30 mg · mL⁻¹ in a 1:1 water–ethylene glycol mixture, yielding a stable ink (solid content ~ 2.9 wt.%, viscosity ~ 10 cP) suitable for inkjet printing.

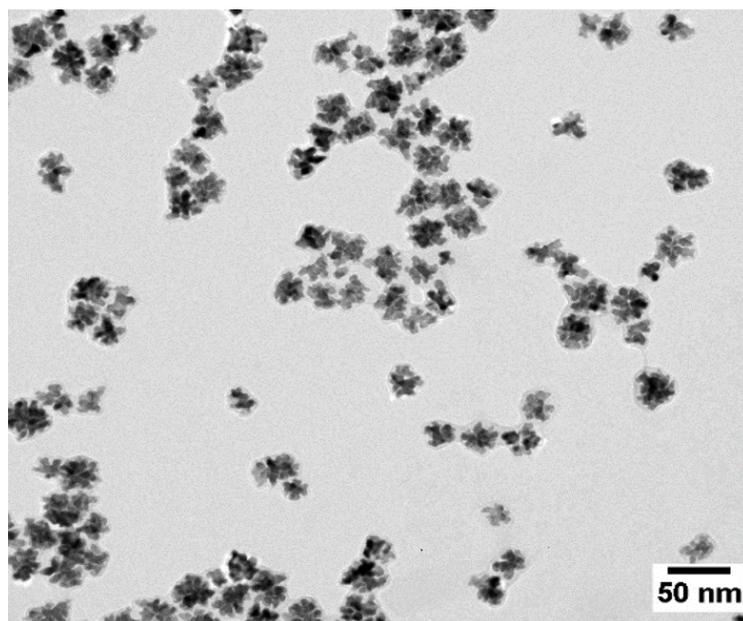


Figure 3.4: Transmission electron microscopy (TEM) image of the Pt NPs, showing well-dispersed clusters with average particle size is in the range of 15 - 25 nm.

Ag Ink

A commercial Ag nanoparticle ink [viscosity 13 cP, Sigma-Aldrich GmbH, Germany] was employed to print the outer contact pads of the temperature sensors, providing low-resistance and stable electrical contacts for sensor probing and mechanical robustness in flexible sensing.

Au Ink

The Au nanoparticle ink [Metalon JG-024UA, NovaCentrix, USA] was used for printing EGT electrodes and circuit interconnects by aerosol jet printing. The ink comprises of 40 wt.% Au nanoparticles with an average particle size of 30–50 nm, dispersed in an aqueous fluoropolymer binder that provides strong adhesion and water resistance on various substrates. The ink exhibits a viscosity of 6–10 cP, making it compatible with aerosol jet printing process.

Sputtered ITO

Sputtered ITO-coated glass substrates served as pre-patterned conductive layers for hybrid-printed device fabrication. The 100 nm ITO film exhibits a sheet resistance of $16 \Omega/\square$, corresponding to a resistivity of $1.6 \times 10^{-6} \Omega \cdot \text{m}$ and a conductivity of $6.3 \times 10^5 \text{ S} \cdot \text{m}^{-1}$. These values lie within the typical range

reported for ITO (10^5 – 10^6 S · m⁻¹)^[75], depending on the doping concentration, oxygen vacancy content, and crystallinity of the film. Such performance confirms the suitability of the laser-ablated ITO electrodes as conductive materials in printed electronic devices.

PEDOT:PSS Ink

The PEDOT:PSS conductive polymer ink [viscosity 10 cP, Sigma-Aldrich GmbH, Germany] was used for gate contacts and interconnect layers, offering high transparency, mechanical flexibility, and compatibility with both metallic electrodes and electrolyte interfaces.

3.2.2 Semiconducting Material

In₂O₃ Ink

The n-type In₂O₃ semiconductor ink was derived from a solution-based precursor comprising indium nitrate hydrate (In(NO₃)₃ · *x*H₂O) dissolved in deionized water with glycerol as a viscosity modifier. The resulting precursor ink had a viscosity of 8–12 cP, suitable for inkjet printing of uniform precursor films.

3.2.3 Electrolyte and Insulating Material

CSPE Ink

The CSPE served as the gate isolator for the electrolyte-gated devices. It was formulated by intermixing two solutions: (1) polyvinyl alcohol (PVA) dissolved in dimethyl sulfoxide (DMSO) and (2) lithium perchlorate (LiClO₄) dissolved in propylene carbonate (PC). The combined solution formed a homogeneous electrolyte with a viscosity of 10 cP, suitable for inkjet printing.

PVA Ink

Poly(vinyl alcohol) (PVA) dissolved in DMSO was used as an insulating crossover layer in printed PUF circuits, yielding a solution viscosity of approximately 12 cP suitable for uniform film formation during inkjet printing. After deposition, the

films were cured at 90 °C for 30 min, resulting in smooth and defect-free layers with good insulating strength and strong adhesion to the underlying metal layers.

3.3 Substrates and Processing

3.3.1 Substrate

In printed and flexible electronics, the substrate serves as the foundation for all deposited material layers functionality because of its physical, chemical, and thermal properties strongly influence film formation, adhesion, sintering, and electrical performance of the printed devices and circuits. Two main substrate types were employed in this thesis, selected according to the device architecture and processing requirements. The ITO-coated glass substrates [ITO thickness 130 nm, Sigma-Aldrich GmbH, Germany] were used for the fabrication of both the hybrid-printed EGT and the PUF circuits. The ITO layer provided a conductive, thermally stable, chemical inertness, and smooth surface suitable for laser ablation, electrical interfacing, and hybrid system integration.

For the fabrication of the printed platinum temperature sensors, polyimide [thickness 300 μm, DuPont GmbH, Germany] substrates were employed due to their lightweight, superior thermal stability (up to 360 °C), mechanical robustness, and flexibility^[46,14]. These characteristics make polyimide particularly suitable for flexible temperature-sensing applications, where repeated bending and thermal cycling demand a mechanically resilient and thermally stable substrate without compromising electrical or structural integrity. However, its surface roughness and lower surface energy can affect film uniformity and adhesion, necessitating careful surface pre-treatment before printing.

3.3.2 Substrate Pre-processing

Prior to printing, the substrates were subjected to surface cleaning and activation to enhance ink wettability and adhesion. The ITO-coated glass substrates were cleaned in a 1:1 mixture of acetone and isopropanol in an ultrasonic bath, followed by rinsing in deionized water and nitrogen drying to remove organic residues and particulates. The polyimide substrates were cleaned with isopropanol and dried under nitrogen to eliminate surface contaminants and improve wettability.

3.3.3 Thermal Processing and Sintering

After printing, post-processing steps were performed to stabilize the printed layers and remove solvent residues to achieve structural and electrical properties of functional materials^[76]. Sintering methods were selected depending on the material type and substrate compatibility.

Hotplate Sintering

Hotplate heating was used for materials that require moderate temperatures for solvent evaporation and film densification. The Pt inks printed on polyimide substrates for temperature sensor fabrication, were sintered at 250 °C for 30 minutes to remove organic stabilizers and form a continuous, conductive Pt network. The CSPE and PEDOT:PSS layers, used as intermediate functional layers regardless of the substrate, were also processed on a hotplate. The CSPE layer was cured at 60 °C for 30 minutes to remove residual solvents and promote film uniformity while maintaining ionic conductivity and mechanical integrity. The PEDOT:PSS as gate contacts were cured at 50 °C for 20 minutes to enhance film adhesion, reduce residual moisture, and preserve polymer conductivity.

Furnace Annealing

High-temperature furnace annealing was employed for metallic and semiconducting oxide films that require complete decomposition of precursors and nanoparticle densification. The Au electrodes, printed using aerosol jet deposition on both polyimide and glass substrates, were sintered at 300 °C for 1 hour in an ambient

atmosphere, resulting in dense, highly conductive metal traces. The In_2O_3 semiconductor films, derived from $\text{In}(\text{NO}_3)_3 \cdot x\text{H}_2\text{O}$ precursors, underwent a two-step annealing process: (1) pre-drying at 100°C for 10 minutes to remove residual water and glycerol, followed by (2) poly-crystallization at 300°C for 2 hours to form a uniform In_2O_3 layer. This stepwise thermal profile minimized crack formation while preserving sufficient electron transport for stable EGT operation.

3.3.4 Sintering Optimization by In-situ Resistance and TGA Analysis

The sintering behavior of the inkjet printed Pt RTS on polyimide substrates was investigated using in-situ resistance measurements, complemented by thermogravimetric analysis (TGA) of the nanoparticle Pt ink, as shown in **Figure 3.5**.

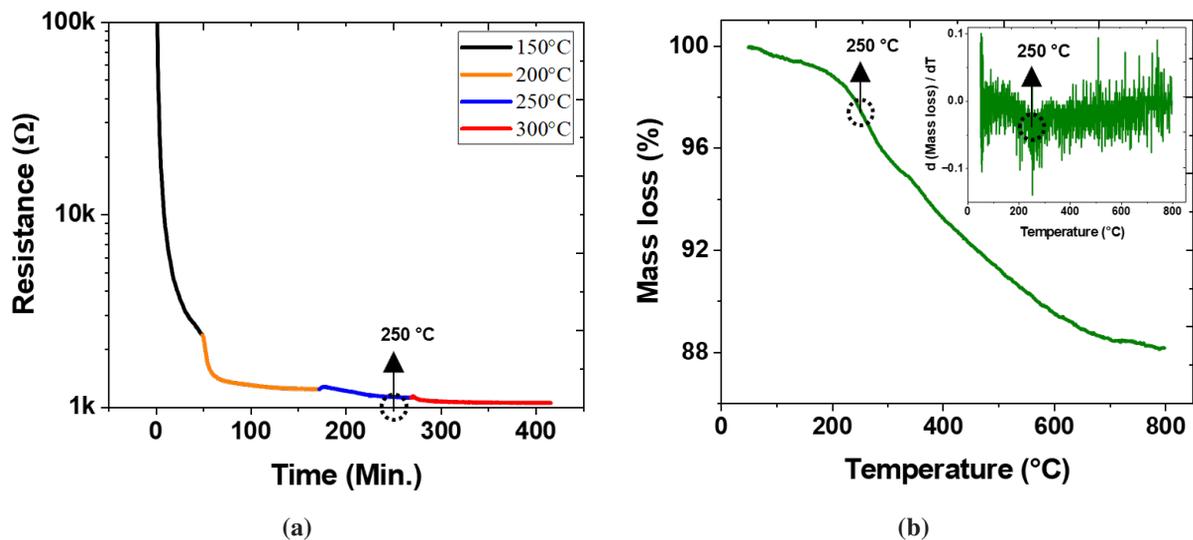


Figure 3.5: (a) In-situ resistance evolution and (b) TGA analysis of the printed Pt resistive temperature sensor, confirming 250°C as the optimal sintering temperature for achieving stable electrical performance.

During stepwise heating (**Figure 3.5a**), the resistance decreased from an open connection (no conductivity) at 150°C to approximately $2500\ \Omega$, indicating partial removal of solvents and organic stabilizers. Further heating to 200°C reduced the resistance to about $1230\ \Omega$, reflecting improved particle connectivity. At 250°C , a

pronounced resistance drop followed by a stable plateau ($\sim 1110 \Omega$) was observed, confirming the formation of a continuous conductive Pt network. Increasing the temperature to 300°C resulted in only a minor additional change, indicating no significant resistance change beyond 250°C .

The TGA analysis (**Figure 3.5b**) of nanoparticle Pt ink shows a gradual mass loss of approximately 12% up to 800°C , attributed to the evaporation of residual solvents (deionized water–ethylene glycol binary mixture) and the decomposition of organic stabilizers. Given the low Pt loading of 2.9 wt.%, the majority of the ink mass originates from solvent and organic components, and the observed mass-loss is therefore physically consistent. The derivative curve (inset) indicates that the dominant mass-loss processes occur between 150°C and 300°C , with a markedly reduced mass-loss rate above this temperature range. This behavior suggests that most volatile organic components are evaporated by 250°C , while further heating provides limited additional mass-loss.

Together, the in situ electrical measurements and supporting TGA results identify 250°C as the optimal sintering temperature for nanoparticle Pt ink (2.9 wt.%), enabling stable electrical conductivity while remaining compatible with the thermal limits of the polyimide substrate.

3.4 Characterization Overview

This section summarizes the experimental characterization techniques employed to evaluate the material properties, structural quality, and electrical performance of the fully-printed and hybrid-printed electronic devices developed in this thesis. A combination of structural, morphological, thermal, and electrical characterization methods was used to establish correlations between material processing conditions, printed film quality, and device-level performance. Structural and morphological techniques were applied to assess ink rheology, film continuity, surface roughness, and microstructure, which are critical for reliable printing and device reproducibility. Electrical characterization was carried out to quantify conductivity, transistor performance, inverter behavior, and PUF response stability. Finally, dedicated data analysis tools were used to process and visualize the experimental results in a consistent and reproducible manner.

3.4.1 Structural and Morphological Characterization

Viscosity Measurements

Viscosity measurements [RheoSense μ VISC, San Ramon, CA, USA] were carried out to evaluate the rheological properties of the inks for inkjet printing. Viscosity is a key parameter governing the jetting behavior, droplet formation, and printability of functional inks, where optimizing viscosity ensures stable droplet ejection, minimizes satellite formation, and promotes uniform film deposition on the substrate. The RheoSense instrument operates on a microfluidic capillary-based principle and measures the pressure drop across a calibrated microchannel at a controlled flow rate, providing precise viscosity values for low-volume inks under isothermal conditions.

Thermogravimetric Analysis (TGA)

TGA [TA Instruments TGA Q5000, New Castle, USA] was employed to evaluate the thermal stability and decomposition behavior of the printed film. In this technique, the sample mass is continuously monitored as a function of temperature or

time under a controlled atmosphere, typically nitrogen or air. The measurement provides quantitative information about solvent evaporation, ligand removal, and residual mass content, which are essential for optimizing the sintering processes. In this thesis, TGA was used to determine the thermal decomposition profile of the nanoparticle Pt dispersion to identify the temperature range at which organic stabilizers and solvents are removed without oxidation, required to achieve continuous and conductive Pt films.

Optical Microscopy

Optical microscopy [Hirox Digital Microscope, Tokyo, Japan] was used for alignment verification, inspection of printed layer uniformity, and detection of defects. The technique employs visible light reflection and magnification optics to provide rapid visualization of pattern quality on both glass and polyimide substrates.

Atomic Force Microscopy (AFM)

A tapping mode AFM [Bruker Nanodimension, Ettlingen, Germany] was used to assess the surface topography and roughness of the printed films. The method operates by scanning a sharp tip over the film surface to measure atomic-scale height variations. The AFM was employed to analyze the surface morphology of inkjet printed Pt film based temperature-sensing elements. The measurements provided insight into the film continuity, grain formation, and roughness evolution after thermal curing.

Scanning Electron Microscopy (SEM)

SEM [FEI Technologies Quanta 400 ESEM, Oregon, USA] was employed to analyze the microstructural and morphological properties of the printed films. The technique uses a focused electron beam to produce high-resolution images ranging from sub-nanometer to tens of nanometers, depending on the instrument and operating conditions. SEM imaging was used to examine the microstructure and sintering quality of the metallic films such as aerosol jet printed Au and inkjet printed Pt layers, offering complementary insights to AFM measurements.

Transmission Electron Microscopy (TEM)

TEM [JEOL JEM-2100F, Tokyo, Japan] was employed to analyze the morphology, size distribution, and agglomeration state of the synthesized platinum (Pt)

nanoparticles. It provides high-resolution imaging by transmitting a focused electron beam through an ultrathin sample, enabling direct visualization of nanoparticle shape, grain boundaries, and interparticle spacing. This analysis was carried out to verify the dispersion quality and uniformity of the nanoparticles, which are critical factors influencing the printability, film continuity, and electrical performance of the printed Pt layers.

Surface Profilometry

Film thickness was measured using a surface profilometer [Veeco Dektak 6M Stylus Profilometer, California, USA]. It employs a stylus-based contact method to scan across the surface and generate step height variations with nanometer-scale vertical resolution. The system is capable of measuring step heights ranging from approximately 10 nm up to 260 μm with uncertainties of ± 5 nm, enabling accurate measurements of both thin semiconductor films and thicker printed electrolyte or conductive layers. The profiler was used to determine the thickness of printed Au electrodes, In_2O_3 semiconductor layers, and electrolyte layers, ensuring reproducibility across multiple samples.

3.4.2 Electrical Characterization

Sheet Resistance and Conductivity Measurements

The sheet resistance (R_S) of the printed metallic layers (Au, Pt, and ITO) was measured using the four-probe Van der Pauw method with a semiconductor parameter analyzer [Keysight 4156C, Santa Rosa, USA]. Measurements were conducted under ambient conditions, and the electrical conductivity (σ_{el}) was determined using the corresponding film thickness (t) values obtained from surface profilometry using **Equation 3.2**^[77]. These measurements were used to evaluate the influence of sintering parameters on film conductivity, ensuring optimal electrical performance of the printed metallic layers.

$$\sigma = \frac{1}{R_S \cdot t} \quad (3.2)$$

Transistor Characterization

Electrical characterization of the EGTs was performed using the semiconductor parameter analyzer described above. The analyzer incorporates built-in analysis models, which were employed for parameter extraction and performance evaluation. All EGT measurements were carried out under ambient conditions with a relative humidity of approximately 50%^[78].

PUF Circuit Testing

The printed inverters integrated into the PUF circuits were characterized using the aforementioned semiconductor parameter analyzer. Measurements were conducted under ambient conditions with a relative humidity of approximately 50%. The voltage transfer characteristics (VTC) of the inverters were analyzed to evaluate device-to-device variability under different operating conditions, including input voltages and humidity levels. These variations in the VTC responses were used to generate and assess the PUF responses, providing insight into the circuit's uniqueness and stability for hardware security applications.

Temperature Sensor Characterization

A hotplate integrated into a probe station, together with the semiconductor parameter analyzer described above, was used to characterize the printed Pt-based temperature sensors. Measurements were performed over a temperature range of 20 °C to 80 °C with a step size of 20 °C, under ambient conditions and a constant relative humidity of approximately 50%. The temperature-dependent resistance was recorded at each step to evaluate the printed sensor sensitivity, linearity, and stability.

3.4.3 Data Analysis

MATLAB

MATLAB was used for the processing and analysis of data obtained from the EGTs, inverters, and PUF. In addition, MATLAB was employed to represent and analyze the hybrid system data, including PUF bit and temperature sensor readout

from the ASIC, enabling comprehensive and integrated performance evaluation across the printed and hybrid devices.

OriginLab

OriginLab was used for the visualization and analysis of experimental data related to the platinum temperature sensors and the metal–semiconductor contact measurements. The software facilitated the plotting of resistance–temperature (R–T) characteristics to evaluate sensor performance, as well as current–voltage (I–V) characteristics to assess contact behavior and electrical conduction across metal–semiconductor interfaces. All plots were formatted for clarity and consistency in data presentation throughout this thesis.

3.5 Summary

This chapter described the materials, fabrication processes, and characterization techniques employed throughout this thesis. Conductive, semiconducting, and electrolyte inks were introduced together with their compositional properties, printing parameters, and sintering conditions relevant to printed device fabrication. Structural, morphological, and electrical characterization approaches were detailed to enable reproducible and quantitative evaluation of printed films and devices. Collectively, these methods establish the experimental framework required for the realization and validation of printed EGTs, PUF circuits, and platinum-based temperature sensors presented in the subsequent chapters.

4 Printed Electrolyte Gated Transistors

This chapter presents the fabrication and experimental validation of hybrid- and fully-printed EGTs architectures. Both device architectures are investigated as fundamental building blocks for low-voltage printed electronics, with emphasis on device design, fabrication, and electrical characterization as a foundation for subsequent circuit-level implementations. The first part of the chapter focuses on hybrid-printed EGTs fabricated on ITO-coated glass substrates by using laser ablation and inkjet printing. The second part of the chapter investigates fully-printed EGTs, in which all functional layers are deposited by using inkjet printing and aerosol jet printing, enabling a fully additive fabrication approach. Fully-printed EGTs on glass substrates are first used as a reference to allow direct comparison with the hybrid-printed EGTs and to ensure reliable process transfer. Subsequently, the same fully-printed EGT architecture is implemented on polyimide to demonstrate compatibility with flexible substrates and to establish the feasibility of an additive fabrication route toward scalable and low-cost printed security circuits. Parts of this chapter are based on results previously published in^[79], which have been adapted and extended through additional analysis for this thesis.

4.1 Hybrid-Printed EGTs on Glass Substrate

4.1.1 Fabrication and Structural Characterization of Hybrid-Printed EGT

The fabrication sequence and physical structure of the hybrid-printed EGTs are shown in **Figure 4.1**, combining the process workflow, an optical microscopy image of a representative device, and a schematic cross-section illustrating the layer stack and thicknesses. As illustrated in Figure 4.1a, the fabrication process begins with an ITO-coated glass substrate, in which the ITO layer serves as the source, drain, and gate electrodes and is patterned by laser ablation.

After electrode definition, all functional layers were deposited using inkjet printing. The semiconductor channel was formed by printing an indium oxide (In_2O_3) precursor ink across the channel area between the ITO source and drain electrodes. The channel geometry was defined by the laser-patterned electrodes, resulting in a channel width $W = 200 \mu\text{m}$ and a channel length $L = 30 \mu\text{m}$. The printed In_2O_3 layer was subsequently annealed at $300 \text{ }^\circ\text{C}$ for 2 hours to convert the precursor into a semiconducting oxide film. Following semiconductor formation, a CSPE was inkjet-printed to serve as the gate isolation layer. The electrolyte layer was dried at $50 \text{ }^\circ\text{C}$ for 30 minutes to promote film stabilization and uniform morphology, while avoiding excessive solvent evaporation that could degrade electrolyte gating performance. To improve gate coupling and provide a uniform top interface for electrolyte gating, a PEDOT:PSS layer was printed on top of the electrolyte and annealed at $50 \text{ }^\circ\text{C}$ for 20 minutes.

An optical microscopy image of a hybrid-printed EGT is shown in **Figure 4.1b**. The image clearly reveals the laser-patterned ITO source/drain/gate electrodes, printed channel region ($W = 200 \mu\text{m}$, $L = 30 \mu\text{m}$), and functional layers. The scale bar of $250 \mu\text{m}$ highlights the overall device dimensions and confirms accurate alignment between laser-patterned and inkjet-printed layers.

A schematic cross-section of the hybrid-printed EGT is presented in **Figure 4.1c**. The ITO electrodes on glass has a thickness of approximately 110 nm. The inkjet

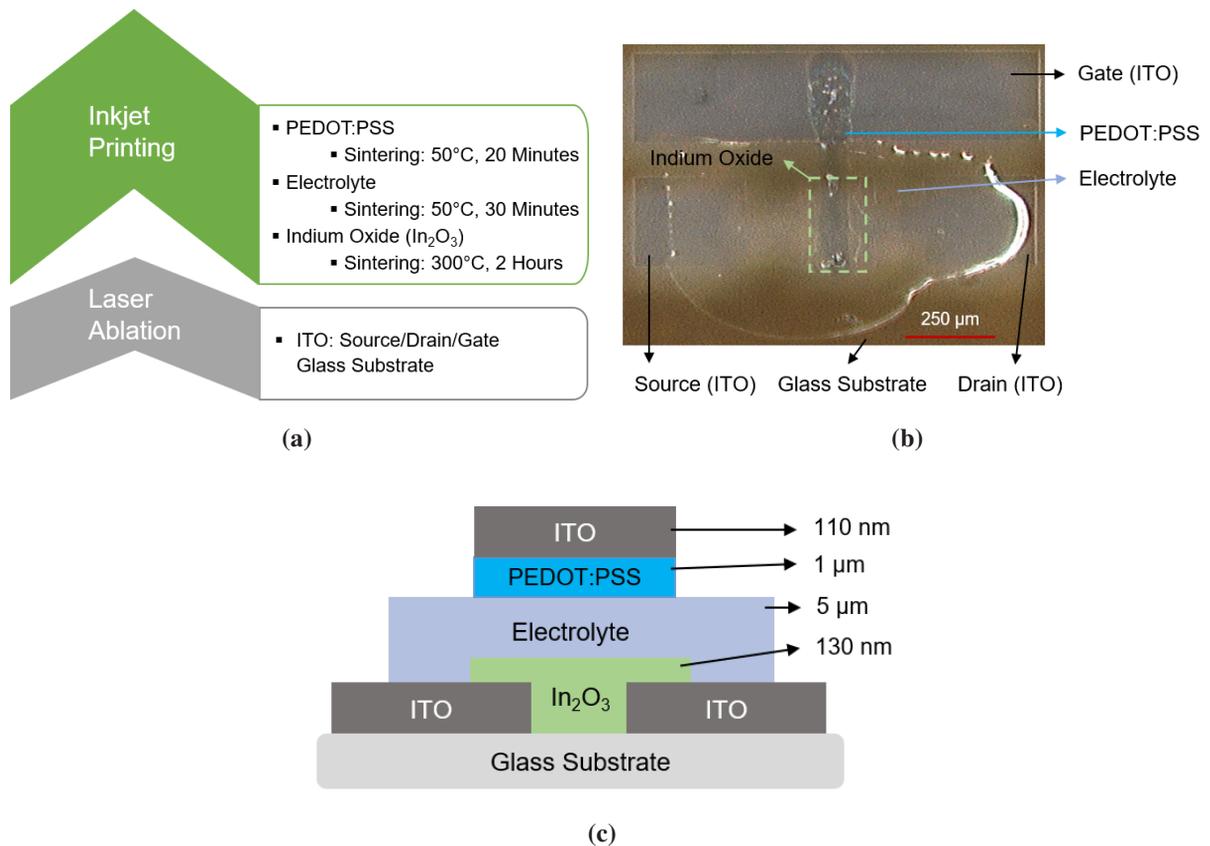


Figure 4.1: (a) Fabrication workflow of the hybrid-printed EGTs combining laser ablation of ITO electrodes on glass substrate and inkjet printing of In_2O_3 , electrolyte, and PEDOT:PSS layers, including post-deposition annealing conditions. (b) Optical microscopy image of the hybrid-printed EGT showing laser-patterned ITO source/drain/gate electrodes and the printed functional layers. (c) Schematic cross-section of the hybrid-printed EGT illustrating the device layer stack and nominal layer thicknesses (± 5 nm).

printed PEDOT:PSS layer is approximately 1 μm thick, while the CSPE layer has a thickness of about 5 μm . The printed In_2O_3 semiconductor layer exhibits a thickness of approximately 130 nm. These thickness values represent typical measurements obtained from surface profilometry and provide a structural basis for correlating the device geometry with the electrical characteristics discussed in the following section.

4.1.2 Electrical Characterization of Hybrid-Printed EGT

The electrical characteristics of the hybrid-printed EGTs were first evaluated using a representative device in order to establish the baseline transistor behavior of the fabricated structure prior to device-to-device analysis. The transfer characteristics, output characteristics, and gate leakage current measured for this device are shown together in **Figure 4.2**.

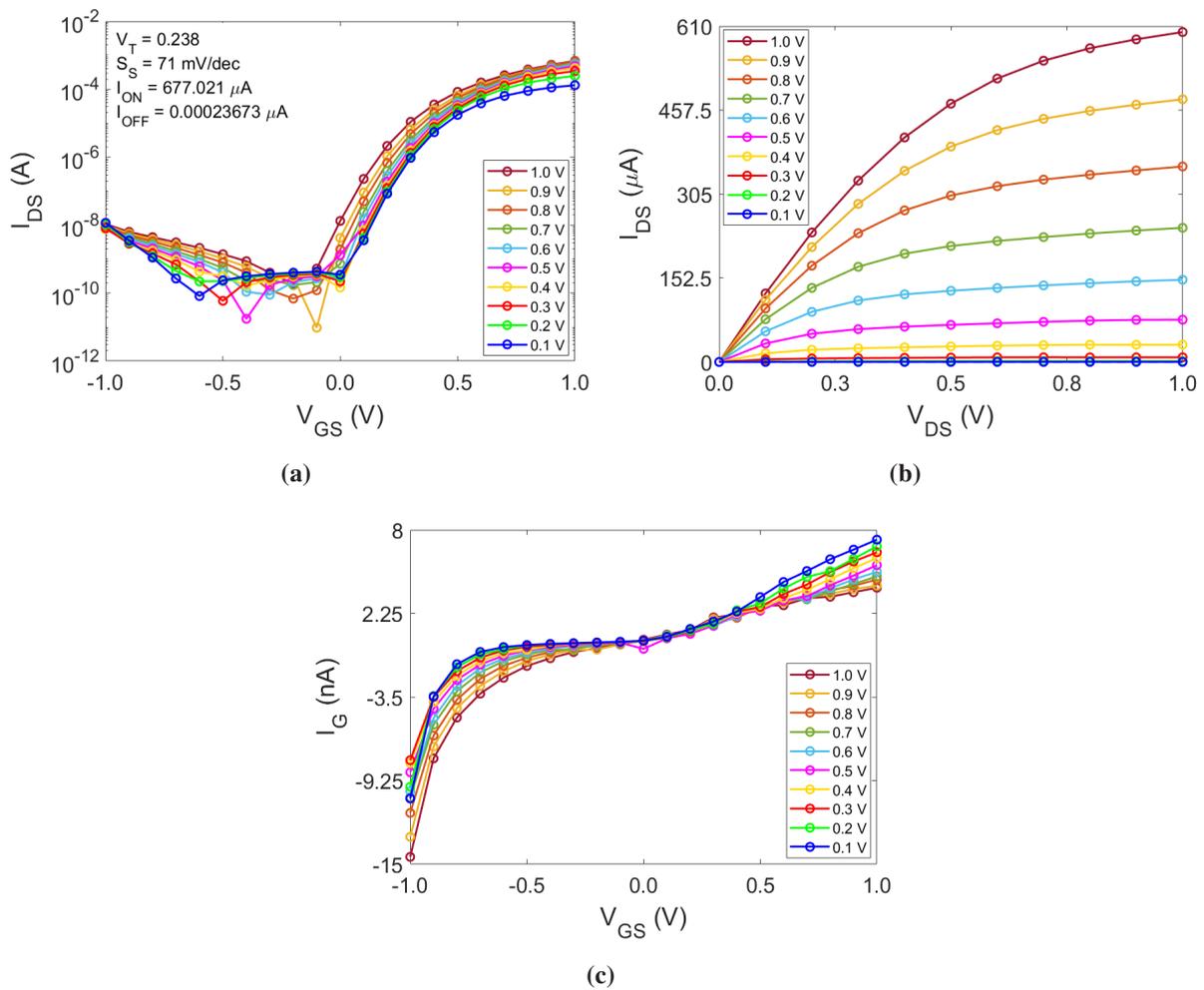


Figure 4.2: Electrical characteristics of the hybrid-printed EGT on glass substrate. (a) Transfer (I_{DS} - V_{GS}) characteristics measured at $V_{DS} = 1$ V, showing n-type accumulation behavior and low-voltage operation. (b) Output (I_{DS} - V_{DS}) characteristics measured with V_{GS} stepped from 0.1 V to 1 V, demonstrating quasi-linear behavior at low drain voltage and gradual current saturation at higher drain voltage. (c) Gate leakage (I_G - V_{GS}) characteristics measured during the transfer sweep, remaining in the nanoampere range across the entire V_{GS} range.

The transfer characteristics were measured by sweeping the gate voltage V_{GS} from -1 V to 1 V at a fixed drain–source voltage of $V_{DS} = 1$ V. As shown in **Figure 4.2a**, the hybrid-printed EGT exhibits clear n-type accumulation behavior with strong gate modulation at low operating voltages, characteristic of electrostatic EDL gating. A threshold voltage of approximately 0.24 V is extracted, together with a subthreshold slope of 71 mV/dec, indicating efficient electrostatic control of the channel enabled by EDL gating. The drain current (I_{ON}) reaches approximately 677 μ A, while the I_{OFF} current remains in the sub-nanoampere range, resulting in an I_{ON}/I_{OFF} ratio exceeding 10^6 , which is similar to the EGTs reported elsewhere^[15,31]. This large current modulation confirms that the hybrid-printed EGT provides well-defined static operating states, which are essential for later integration into inverter-array PUF circuit.

The output characteristics measured with stepped V_{GS} from 0.1 V to 1 V are shown in **Figure 4.2b**. The drain current I_{DS} increases monotonically with increasing drain–source voltage V_{DS} , exhibiting quasi-linear behavior for $V_{DS} < 0.2$ – 0.3 V, followed by gradual current saturation at higher V_{DS} range. At $V_{GS} = 1$ V, the drain current reaches approximately 610 μ A for $V_{DS} = 1$ V. The smooth output curves demonstrates that the hybrid-printed EGT is well suited for analog circuit operation.

The gate leakage current measured simultaneously during the transfer sweep is shown in **Figure 4.2c**. Across the full V_{GS} range, the gate current I_G remains in the nanoampere regime, with a maximum magnitude of approximately 10 – 15 nA at $V_{GS} = -1$ V and below 5 nA near the operating region around $V_{GS} = 0$ – 1 V.

However, the strong gate modulation observed in the transfer characteristics is enabled by the high effective gate capacitance of the electrolyte. Based on prior characterization of the same CSPE formulation and processing conditions, a gate capacitance of approximately $C_G = 4.5$ μ F cm^{-2} ^[80] is assumed for the hybrid-printed EGTs. Using this gate capacitance value, an effective field-effect mobility was estimated for the representative device from the transconductance extracted from the transfer curve. With a channel length of 30 μ m, channel width of 200 μ m, and $V_{DS} = 1$ V, the extracted mobility is approximately 2.9 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. The

extracted values are consistent with those reported in our previous work on EGTs employing the identical In_2O_3 semiconductor and CSPE layer, confirming that the hybrid-printed devices operate within the established material and process window.

4.1.3 Device-to-Device Variability in Hybrid-Printed EGTs

To quantify intrinsic device-to-device variations in the hybrid-printed EGTs, five nominally identical devices (H1–H5) were electrically characterized under identical measurement conditions. The extracted key electrical parameters relevant for static analog operation are summarized in **Table 4.1**.

Table 4.1: Summary of key electrical parameters extracted for hybrid-printed EGTs on glass substrate (H1–H5). I_{OFF} extracted at $V_{\text{GS}} = 0$ V and $V_{\text{DS}} = 1$ V; I_{ON} extracted in the linear regime at $V_{\text{GS}} = 1$ V and $V_{\text{DS}} = 0.1$ V. For consistency, the I_{OFF} values are converted to nA in this table, while the corresponding transfer characteristics are plotted in μA . Measurement uncertainty is on the order of ± 0.01 – 0.02 V, limited by the gate-voltage step size and probe-contact repeatability for the extracted parameters.

Device ID	V_T (V)	S_S (mV/dec)	I_{ON} (μA)	I_{OFF} (nA)	$I_{\text{ON}}/I_{\text{OFF}}$ Ratio	$ I_G _{\text{max}}$ (nA)
H1	0.24	71	677	0.24	2.86×10^6	15
H2	0.13	76	812	0.43	1.88×10^6	20
H3	0.11	66	1071	0.24	4.52×10^6	17
H4	0.26	73	889	0.26	3.38×10^6	11
H5	0.05	75	967	0.20	4.79×10^6	13

Across the device set, the threshold voltage V_T spans a range from 0.05 V to 0.26 V, corresponding to a total spread of approximately 210 mV. This variation reflects small but irreducible differences in printed semiconductor thickness, electrolyte coverage, and local interface conditions introduced during fabrication. Despite this spread in V_T , all devices operate within the similar low-voltage regime. The subthreshold slope remains relatively consistent across the devices,

with values between 66 and 76 mV/dec, indicating comparable electrostatic gate control for all transistors. The I_{ON} current varies between 677 μA and 1071 μA , while the I_{OFF} current remains in the sub-nanoampere range (0.20–0.43 nA), resulting in $I_{\text{ON}}/I_{\text{OFF}}$ current ratios consistently exceeding 10^6 for all EGTs. The maximum gate leakage current remains below 25 nA for all devices and is several orders of magnitude smaller than the corresponding I_{ON} current. This confirms stable and predominantly capacitive electrolyte gating across the entire device set and excludes leakage-driven variability. Overall, the hybrid-printed EGTs exhibit stable analog behavior with reproducible electrical characteristics, while maintaining device-to-device variations, primarily manifested as shifts in threshold voltage and current drive. These variations are intrinsic to the fabrication process and remain stable across repeated measurements, making the hybrid-printed EGT approach a suitable reference for integration into inverter array PUF in the subsequent chapter, where device-level mismatch is exploited at the circuit level to generate unique and repeatable responses.

4.2 Fully-Printed EGTs on Glass and Polyimide Substrates

4.2.1 Fabrication and Structural Characterization

The fabrication process and structural realization of the fully-printed EGTs are summarized in **Figure 4.3**. The device architecture is implemented exclusively using additive printing techniques, combining aerosol jet printing for metallic electrodes deposition and inkjet printing for the semiconductor, electrolyte, and gate contact layers. The EGTs were fully-printed on both glass and polyimide substrates, where glass serves as a reference benchmark and polyimide demonstrates compatibility with flexible substrates.

As illustrated in **Figure 4.3a**, the fabrication sequence starts with aerosol jet printing of Au source, drain, and gate electrodes on the substrates. The source and drain electrodes define a channel width and length of $W/L = 200 \mu\text{m}/30 \mu\text{m}$, while the printed metal features exhibit linewidth below $20 \mu\text{m}$, demonstrating the fine patterning capability of AJP. After deposition, the printed Au electrodes were thermally annealed at $200 \text{ }^\circ\text{C}$ for 30 minutes to improve electrical conductivity and adhesion to the substrates. Subsequently, an inkjet printed In_2O_3 precursor layer was deposited to form the semiconductor channel bridging the Au source and drain electrodes. The printed precursor was thermally annealed under the same conditions used for the hybrid-printed EGTs in **Section 4.1**, ensuring direct comparability between the EGT architectures. Likewise, a CSPE was inkjet-printed to function as the gate isolator, followed by deposition of a PEDOT:PSS layer, with sintering conditions identical to those employed for the hybrid-printed EGTs.

Optical microscopy images of fully-printed EGTs on glass and polyimide substrates are shown in **Figure 4.3b** and **Figure 4.3d**, respectively. The images clearly reveal the printed Au source/drain/gate electrodes, the printed channel region, and the overlap with the electrolyte and gate contact layers. Precise alignment between aerosol jet printed metal electrodes and inkjet printed functional

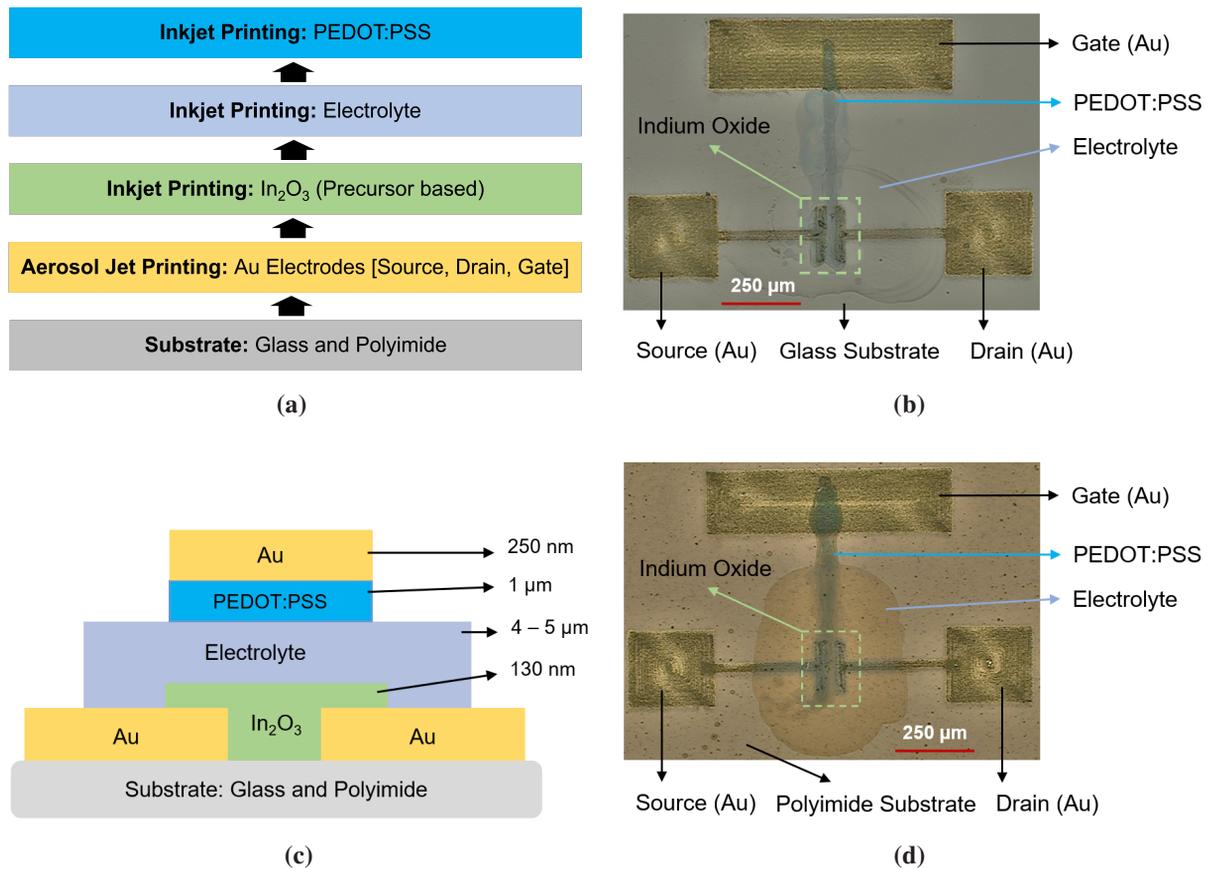


Figure 4.3: (a) Fabrication sequence of fully-printed EGTs combining aerosol jet and inkjet printed layers. (b,d) Optical microscopy of a fully-printed EGTs on glass and polyimide substrates, showing AJP and IJP layers. (c) Schematic cross-section of the fully-printed EGTs with approximate layer thicknesses (± 5 nm). *Reproduced with permission from*^[79], © IEEE 2025.

layers is observed on both substrates, confirming reliable process transfer from rigid to flexible architectures.

A schematic cross-section of the fully-printed EGTs is shown in **Figure 4.3c**. The aerosol jet printed Au electrode has a thickness of approximately 250 nm, while the inkjet-printed PEDOT:PSS layer is about 1 μm thick. The CSPE thickness lies in the range of 4–5 μm , and the printed In_2O_3 semiconductor layer has a thickness of approximately 120 – 130 nm. These thickness values are representative and were extracted from a contact surface profilometry measurements. Minor variations in layer thickness are inherent to the printing process and, in the case of polyimide substrates, are further influenced by the intrinsic surface roughness

of the substrate. Such variations are therefore considered intrinsic characteristics of the fully-printed device architecture.

4.2.2 Electrical Characterization of Fully-Printed EGTs

The electrical performance of the fully-printed EGTs were evaluated using representative devices on glass and polyimide substrates. Transfer characteristics, output characteristics, and gate leakage current were measured at a fixed drain voltage of $V_{DS} = 1$ V, with the V_{GS} swept between -1 V and 1 V, enabling a direct comparison of substrate-dependent electrical behavior. The measured characteristics are shown in **Figure 4.4**.

Both fully-printed EGTs exhibit n-type accumulation behavior, confirming effective electrostatic EDL gating within the V_{GS} window. For the fully-printed EGT on glass (**Figure 4.4a**), the transfer characteristics show a well-defined threshold voltage of $V_T = 0.28$ V and a steep subthreshold slope of 72 mV/dec (as annotated directly in the plot), indicating strong electrostatic control of the channel. The I_{OFF} remains in the sub-nanoampere range, while the I_{ON} reaches several hundred microampere at $V_{GS} = 1$ V, resulting in an I_{ON}/I_{OFF} ratio exceeding 10^6 indicates effective channel modulation. The transfer behavior closely reproduces that of the hybrid-printed EGTs, establishing the fully-printed EGTs on glass substrate as a transferable electrical benchmark. In contrast, the fully-printed EGT on polyimide (**Figure 4.4d**) exhibits a shifted transfer characteristic with a threshold voltage of $V_T = -0.26$ V. This threshold-voltage shift indicates that the device turns on at a lower V_{GS} compared to devices on glass, thereby reducing the usable gate-voltage margin and increasing sensitivity to device-to-device variability. The device also shows a broader subthreshold region corresponding to a subthreshold slope of 124 mV/dec, indicating reduced gate control. Despite this shift, the device exhibits extracted I_{OFF} values in the low-tens-of-nanoampere range and reaches a substantially higher I_{ON} within the same V_{GS} window, yielding an I_{ON}/I_{OFF} ratio exceeding 10^5 . Measurements across additional EGTs on

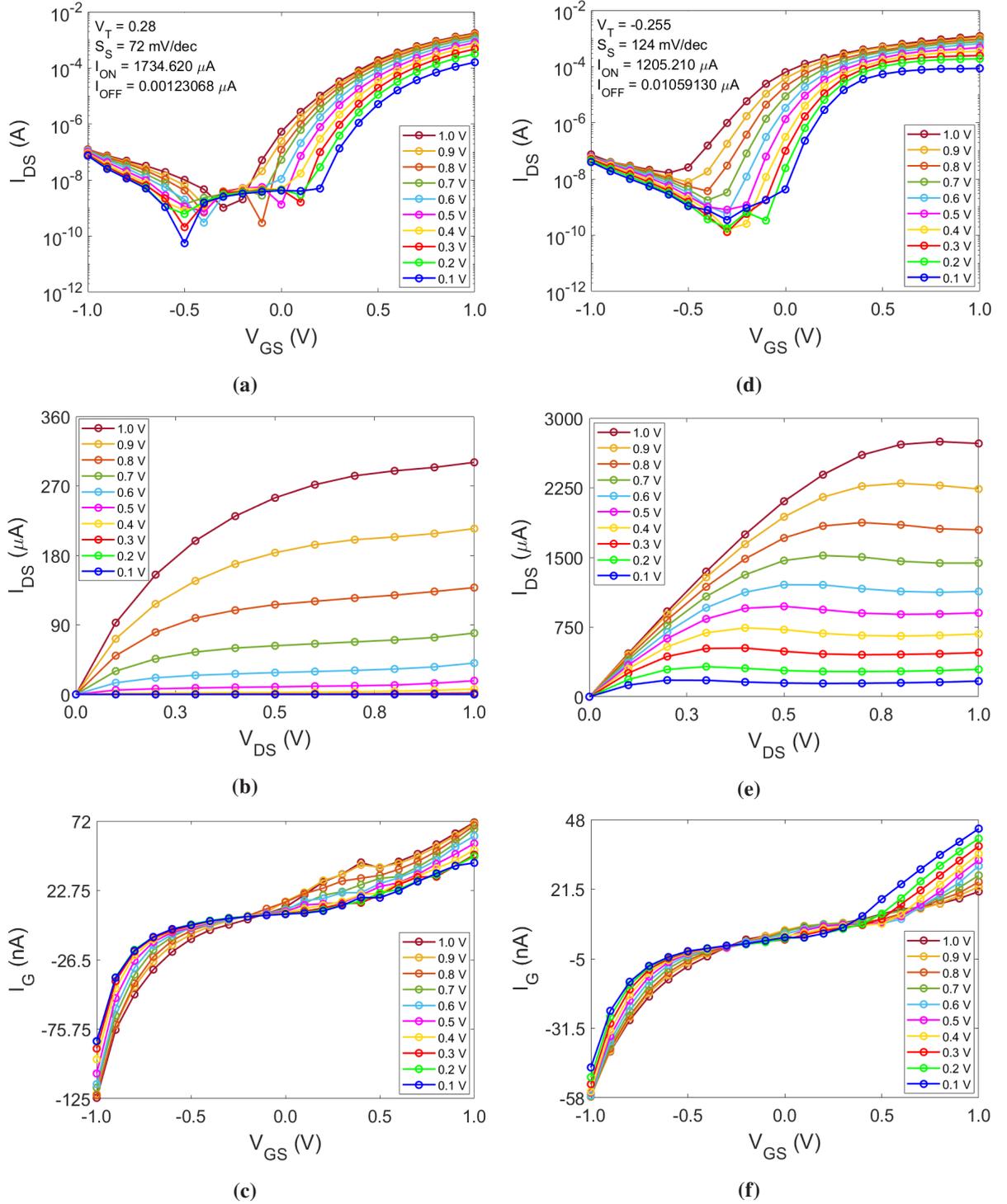


Figure 4.4: Electrical characteristics of fully-printed EGTs on glass and polyimide substrates. (a–c) Transfer curves measured at $V_{DS} = 1$ V, output curves measured for stepped V_{GS} , and gate leakage current as a function of V_{GS} for EGT on glass. (d–f) Corresponding transfer, output, and gate leakage curves of EGT on polyimide. The devices exhibit n-type accumulation behavior and low-voltage operation, with substrate-dependent differences in threshold voltage, drain current level, and subthreshold slope. *Reproduced with permission from*^[79], © IEEE 2025.

polyimide (**Table 4.2**) show a spread in V_T , indicating that the negative threshold observed here reflects device-to-device variability rather than an intrinsic limitation of the substrate.

The output characteristics further highlight the substrate dependence of the fully-printed EGTs. For fully-printed EGT on glass (**Figure 4.4b**), the drain current I_{DS} increases smoothly with V_{DS} and exhibits clear saturation behavior. At $V_{GS} = 1$ V and $V_{DS} = 1$ V, I_{DS} reaches approximately $300 \mu\text{A}$, which is comparable to the current levels observed in the hybrid-printed EGT on glass with identical channel dimensions. This indicates that the fully-printed EGT on glass preserves the expected current drive and can therefore serve as a reliable electrical reference. In contrast, the fully-printed EGT on polyimide (**Figure 4.4e**) exhibits a pronounced increase in I_{DS} levels, reaching approximately 2.5 mA under identical electrical measurement conditions, corresponding to nearly an order of magnitude higher compared to the fully-printed EGT on glass. The higher I_{DS} observed for the EGT on polyimide correlates with the shifted transfer characteristics and is attributed to substrate- and interface-related electrical effects rather than differences in device geometry. In particular, the negative shift in threshold voltage causes the device to turn on at a lower V_{GS} , resulting in higher drain current within the same gate-voltage range. Although a larger subthreshold slope indicates reduced effectiveness of gate-voltage control, the increased I_{DS} on polyimide is consistent with the observed threshold-voltage shift, which places the device deeper in the conductive regime within the same applied V_{GS} range. Despite this reduced control, the output characteristic curves remain smooth and free of abrupt current increases, indicating stable electrical operation on the flexible substrate.

Gate leakage characteristics for both substrates are shown in (**Figure 4.4c** and **Figure 4.4f**). For the fully-printed EGT on glass, the gate leakage current I_G varies approximately between -125 nA and 72 nA over the full gate-voltage sweep, whereas for the fully-printed EGT on polyimide exhibits a lower leakage currents ranging between -58 nA and 48 nA. In both cases, I_G remains at least two orders of magnitude smaller than the corresponding I_{ON} , confirming that

device operation is dominated by effective EDL gating. Compared to the hybrid-printed EGT, which exhibits gate leakage currents below approximately 20 nA, the higher leakage observed in fully-printed EGTs are attributed to electrical and structural non-idealities associated with printed Au electrode-electrolyte layer combination, local gate electrolyte thickness variations, and its overlap with the effective channel region, leading to increased leakage pathways under identical measurement conditions.

To further interpret the observed current differences, an effective field-effect mobility was extracted from the transconductance g_m in the linear regime, adopting a gate capacitance of $C_G = 4.5 \mu\text{F cm}^{-2}$ ^[80], consistent with the same $\text{In}_2\text{O}_3/\text{CSPE}$ material system used for the hybrid-printed EGTs. Based on this approach, the extracted effective mobility approximately $0.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for the fully-printed EGT on glass and $9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for the device on polyimide. For comparison, the hybrid-printed EGT on glass exhibits an effective mobility of approximately $2.9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is higher than that of the fully-printed EGT on glass but lower than that of the fully-printed EGT on polyimide, consistent with the corresponding I_{DS} levels in the output characteristics observed across the EGTs architecture. The observed mobility trend reflects a combination of substrate- and interface-related electrical effects, including differences in printed film morphology, effective electrostatic EDL gating efficiency, and charge injection efficiency at the Au– In_2O_3 interface rather than intrinsic improvements in semiconductor charge transport.

4.2.3 Device-to-Device Variability in Fully-Printed EGTs

Table 4.2 summarizes the key electrical parameters of fully-printed EGTs on glass (G1–G4) and polyimide (P1–P4) substrates. A direct comparison reveals clear similarities in overall device functionality, while also highlighting systematic differences that arise from substrate- and interface-related effects.

Table 4.2: Summary of key electrical parameters extracted for fully-printed EGTs on glass (G1–G4) and polyimide (P1–P4) substrates. The I_{OFF} was extracted at $V_{\text{GS}} = 0$ V and $V_{\text{DS}} = 1$ V, while the I_{ON} was extracted in the linear regime at $V_{\text{GS}} = 1$ V and $V_{\text{DS}} = 0.1$ V. Although transfer characteristics are plotted in μA , I_{OFF} values are reported in nA for consistency. Measurement uncertainty is on the order of ± 0.01 – 0.02 V, limited by the gate-voltage step size and probe-contact repeatability for the extracted parameters.

Device ID	V_T (V)	S_S (mV/dec)	I_{ON} (μA)	I_{OFF} (nA)	$I_{\text{ON}}/I_{\text{OFF}}$ Ratio	$ I_G _{\text{max}}$ (nA)
G1	0.28	72	1735	1.23	1.41×10^6	125
G2	0.20	101	1734	4.81	3.61×10^5	212
G3	0.26	74	1061	0.61	1.73×10^6	62
G4	0.14	73	1267	0.71	1.79×10^6	44
P1	-0.25	124	1205	10.6	1.14×10^6	58
P2	0.02	89	6749	8.10	8.34×10^5	63
P3	0.02	108	3844	6.21	6.20×10^5	101
P4	0.43	114	2107	1.10	1.93×10^6	59

The fully-printed EGTs on glass substrate exhibit relatively tight parameter distributions. The threshold voltage V_T remains positive and clustered between 0.14 and 0.28 V, whereas the subthreshold slope S_S is close to the theoretical limit for EGTs, with three out of four devices exhibiting values in the range of 72–74 mV/dec. The I_{ON} current ranges from approximately 1.0 to 1.7 mA, while I_{OFF} currents remain below 5 nA for all devices, resulting in $I_{\text{ON}}/I_{\text{OFF}}$ ratios consistently exceeding 10^6 for most devices. These characteristics indicate strong electrostatic control and stable EGT operation printed on glass substrate.

In contrast, fully-printed EGTs on polyimide substrates exhibit a broader spread in electrical parameters. The threshold voltage varies from -0.25 V to 0.43 V, with two devices operating close to zero threshold voltage. The subthreshold slopes are generally higher, ranging from 89 to 124 mV/dec, which indicate reduced electrostatic control compared to fully-printed EGTs on glass. Despite this, EGTs on polyimide reveals significantly higher I_{ON} currents, reaching up to 6.7 mA, while the I_{OFF} currents remain below 11 nA. As a result, the $I_{\text{ON}}/I_{\text{OFF}}$ ratios remain comparable to those observed on glass substrates, despite the increased variability.

The maximum absolute gate leakage current $|I_G|_{\text{max}}$ remains in the tens to low hundreds of nanoampere range for fully-printed EGTs on both glass and polyimide substrates, with the highest value of 212 nA observed across the dataset. Although these values exceed those reported for hybrid-printed EGTs (below 20 nA), the leakage currents remains consistently at least two orders of magnitude smaller than corresponding I_{ON} for all devices. This indicates that gate leakage is sufficiently small relative to the I_{ON} current and therefore EGT operation within the investigated voltage range is governed by effective EDL gating.

Overall, the electrical properties of the fully-printed EGTs are strongly influenced by substrate- and interface-related effects. The EGT on glass exhibit more uniform characteristics, providing a stable electrical reference that closely matches the behavior of the hybrid-printed EGT architecture. In contrast, fully-printed EGT on polyimide demonstrates substantially higher drain currents, accompanied by increased variability in threshold voltage and subthreshold slope, reduced effectiveness of gate-voltage control, and higher gate leakage. Nevertheless, these results demonstrate that fully-printed EGTs on polyimide substrates can provide sufficient current drive and low-voltage operation for feasibility studies of flexible inverter-based PUF, while highlighting the need for further optimization of electrostatic control and device variability.

4.3 Summary

This chapter demonstrated the realization of EGTs using two complementary fabrication architectures: a hybrid-printed architecture based on laser-ablated ITO electrodes on glass substrates with inkjet printed functional layers, and a fully-printed architecture combining aerosol jet printing for Au electrode patterning with inkjet printed functional layers on both glass and polyimide substrates.

Hybrid-printed EGTs on glass exhibit stable and reproducible low-voltage operation, with threshold voltages in the range of 0.05 V to 0.26 V, subthreshold slopes of 66–76 mV/dec, on/off current ratios exceeding 10^6 , and gate leakage currents below 20 nA. Across nominally identical devices, variations in threshold voltage and current drive are observed, arising from intrinsic variations associated with the printed semiconductor and electrolyte layers and their interfaces introduced during fabrication. Despite this variability, the hybrid-printed EGTs exhibit stable and well-controlled electrical characteristics, which are directly exploited in the subsequent implementation of inverter-array based PUF circuits.

Fully-printed EGTs on glass closely reproduce the electrical characteristics of the hybrid-printed devices, exhibiting threshold voltages of 0.14–0.28 V, subthreshold slopes of 72–74 mV/dec, I_{ON} values of approximately 1.0–1.7 mA, I_{OFF} below 5 nA, and $I_{\text{ON}}/I_{\text{OFF}}$ ratios above 10^6 . This confirms effective process transfer to a fully additive fabrication route while maintaining electrical performance comparable to the hybrid-printed architecture. When implemented on polyimide substrates, fully-printed EGTs exhibit significantly higher drain currents, with I_{ON} values reaching up to 6.7 mA, while maintaining $I_{\text{ON}}/I_{\text{OFF}}$ ratios on the order of 10^5 – 10^6 . This behavior is accompanied by increased variability in threshold voltage (–0.25 to 0.43 V) and subthreshold slope (89–124 mV/dec). The gate leakage currents remain in the tens to low hundreds of nanoamperes range with a maximum value of 212 nA. These variations reflect substrate- and interface-related effects inherent to flexible substrates. Together, these results establish the feasibility of fully-printed EGTs on flexible substrate, with

further optimization required for integration into inverter-array based PUF circuit implementations.

5 Printed PUF and Temperature Sensor

This chapter presents the fabrication and experimental validation of printed PUF and temperature sensors. Both devices are realized using printing techniques and are investigated as device-level building blocks for secure identification and reliable sensing. The chapter focuses on device design, fabrication, and electrical characterization, providing the basis for subsequent hybrid system-in-foil integration. The first part of the chapter investigates a printed analog PUF based on inverter-array, implemented based on hybrid-printed EGTs and laser-ablated ITO electrodes on a glass substrate. The PUF employs the hybrid-printed EGTs demonstrated and electrically characterized earlier. The second part of the chapter addresses inkjet printed platinum-based resistive temperature sensors on polyimide substrates, with the content adjusted from the previous publication^[81] to ensure clarity and coherence within this thesis. The electrical and thermal characteristics of the sensors are evaluated, including their stability and performance over an automotive-relevant temperature range from 20 °C to 80 °C.

5.1 Printed PUF

5.1.1 Fabrication of PUF

The inverter-array based PUF is fabricated on an ITO-coated glass substrate using a combination of laser ablation and inkjet-printing processes. In a first step, laser ablation is used to define the ITO layout of the PUF circuit, including the

source and drain electrodes of EGT_1-EGT_9 , the channel dimensions ($W/L = 200 \mu\text{m}/60 \mu\text{m}$), the shared supply rails (V_{DD} , V_{in} , and GND), interconnects, and inverter output contact pads ($V_{out1}-V_{out9}$). The pull-up resistors ($R_{D1}-R_{D9}$) exhibit a mean resistance of $8.35 \text{ k}\Omega$ with a standard deviation of $0.1 \text{ k}\Omega$, selected to ensure sufficiently high load resistance for low-voltage inverter operation.

Following laser patterning, the active EGT stack is formed by sequential inkjet printing at each inverter, employing the identical hybrid-printed EGT architecture introduced earlier and integrated here as EGT_1-EGT_9 . The process consists of printing the In_2O_3 semiconductor channel, followed by a PVA-based insulating layer above V_{DD} rails, and subsequently the CSPE and PEDOT:PSS layers. The PVA layer is processed prior to the CSPE because it requires sintering at 90°C , whereas the CSPE layer is restricted to 50°C in this thesis.

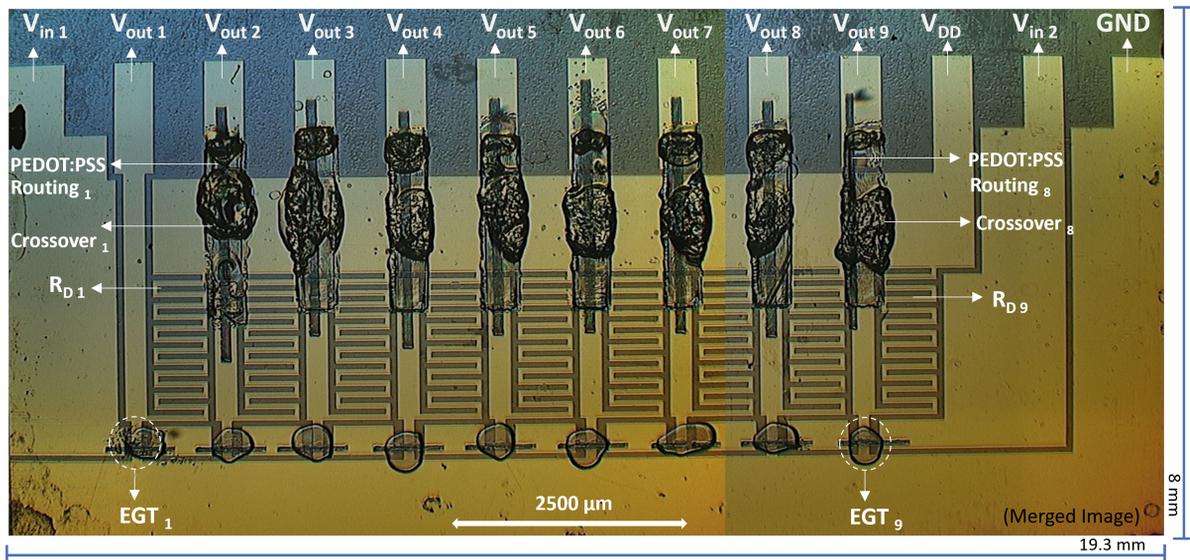


Figure 5.1: Microscopy image of the fabricated inverter-array based PUF array on an ITO-coated glass substrate after completion of laser ablation and inkjet printing steps. The image shows the nine EGTs (EGT_1-EGT_9), pull-up resistors ($R_{D1}-R_{D9}$), individual inverter output pads ($V_{out1}-V_{out9}$), shared supply rails (V_{DD} , V_{in} , and GND), and PEDOT:PSS routing lines implemented via PVA-based crossover structures for independent output probing. *Reproduced with permission from^[82], © IEEE 2025.*

To enable independent access to $V_{out1}-V_{out9}$ while avoiding electrical shorting with the shared V_{DD} rail, printed crossover structures are incorporated. PE-DOT:PSS lines are printed atop the PVA layer to route each inverter output across V_{DD} to the corresponding V_{out} contact pad. This routing strategy enables independent probing of all inverter outputs and supports subsequent hybrid system-in-foil integration. The printed inverter-array based PUF is shown in **Figure 5.1**.

5.1.2 Electrical Characterization of PUF

The electrical performance of the printed inverter-array based PUF was evaluated to determine the operating conditions suitable for extracting stable PUF responses. All electrical measurements were performed at room temperature and approximately 50% relative humidity using a semiconductor parameter analyzer configured in a shared-rail architecture, in which all inverters were operated with a common supply voltage $V_{DD} = 1$ V, a common input voltage V_{in} , and a shared circuit ground reference. The input voltage was swept from -0.5 V to 1.0 V, and for each inverter the corresponding output voltage V_{out} , gate leakage current I_G , and supply current I_{DD} were recorded (**Figure 5.2**).

The measured transfer curves, shown in **Figure 5.2a**, reveal pronounced device-to-device variability in both switching threshold and output saturation levels, despite all inverters having identical layout geometry, channel dimensions, and material stack. Each inverter transitions at a slightly different input voltage and exhibits distinct voltage-response characteristics, reflecting manufacturing-induced stochastic variations originating from both the laser-ablated circuit structures and the inkjet printed semiconductor, electrolyte, and crossover layers. These variations constitute the analog entropy source exploited for PUF bit generation.

To identify the input voltage V_{in} range at which the inverter output voltages exhibit the largest spread, the standard deviation of the nine inverter output voltage curves was computed as a function of V_{in} and is shown in **Figure 5.2b**. A well-defined maximum appears between $0.5-0.7$ V, corresponding to the inverters collective transition region, where small variations in device parameters yield large

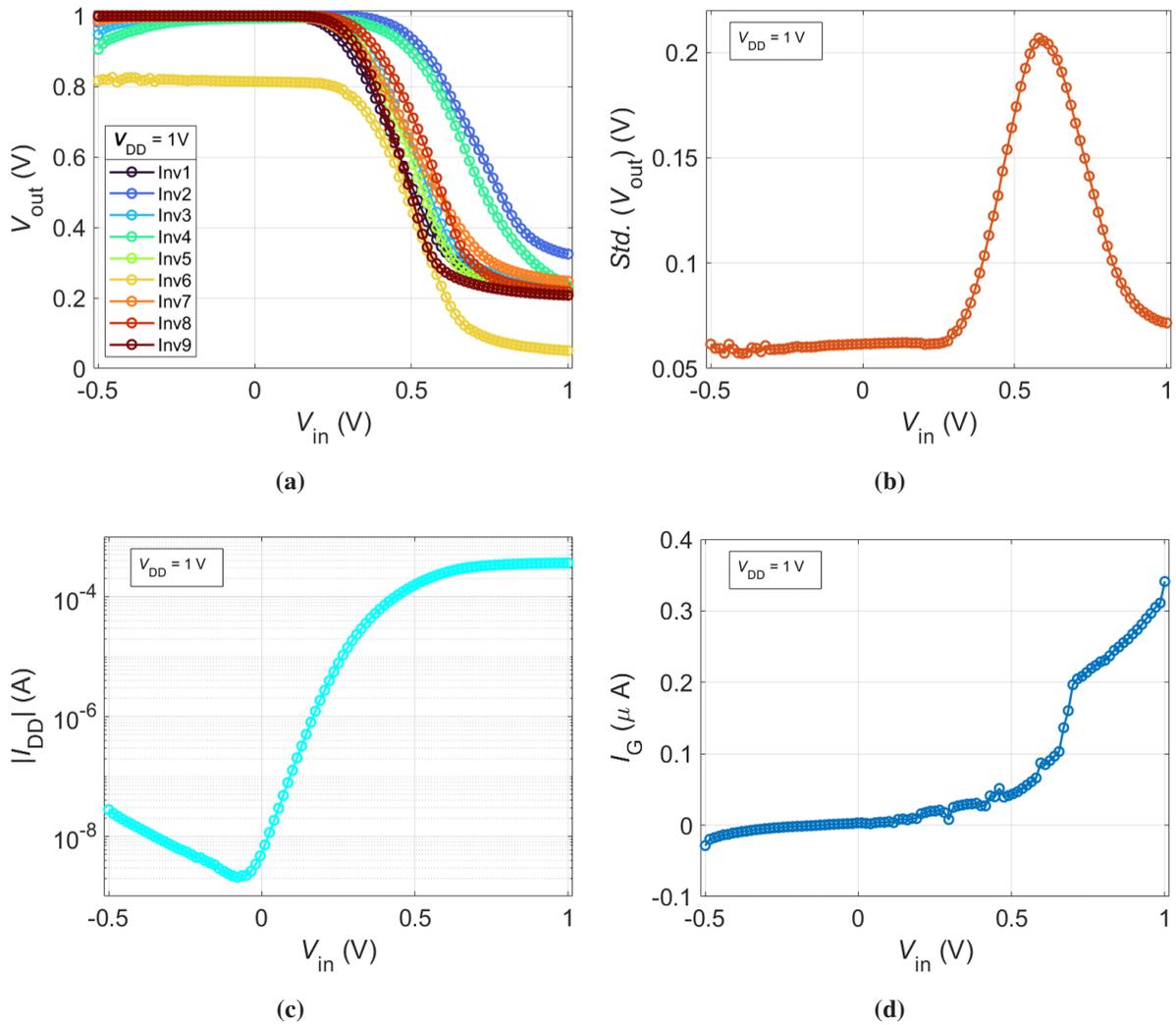


Figure 5.2: (a) Transfer curves $V_{out}(V_{in})$ for nine inverters at $V_{DD} = 1\text{ V}$, showing device-to-device variation. (b) Standard deviation (σ) of the nine inverter outputs, identifying the entropy-rich window between 0.5–0.7 V. (c) Supply current $|I_{DD}|$ versus V_{in} , demonstrating low-power operation. (d) Accumulated gate leakage current I_G versus V_{in} , confirming effective CSPE gate isolation.

differences in output voltage. Below approximately 0.4 V the outputs cluster near the high state with limited separation, while above 0.7 V they approach saturation in the low state. The 0.5–0.7 V interval therefore represents the entropy-rich operating window for extracting PUF responses.

The output and leakage current curves support stable operation within this window. The measured supply current, shown in **Figure 5.2c**, remained in the nA– μA

range across the full V_{in} sweep with a maximum current draw $I_{DD} \approx 163 \mu\text{A}$ at $V_{in} = 0.5 \text{ V}$ and $I_{DD} \approx 366 \mu\text{A}$ at $V_{in} = 1 \text{ V}$, consistent with low-power PUF operation. The accumulated gate leakage current for nine-inverters, plotted in **Figure 5.2d**, remains low $\approx 340 \text{ nA}$ at $V_{in} = 1 \text{ V}$, confirming effective isolation of the printed electrolyte layer. The extracted power consumption remains below $370 \mu\text{W}$ at $V_{DD} = 1 \text{ V}$, with leakage power contributing less than 0.1% of the total consumption. This energy-efficient behavior is essential for lightweight hardware-security circuits and subsequent hybrid system-in-foil integration.

5.1.3 PUF Bit Extraction

The analog variability observed across the nine-inverters transfer curves serves as the entropy source for generating PUF response. Based on the measured transfer characteristics and $\sigma(V_{out})$, four operating points of $V_{in} = \{0.4, 0.5, 0.6, 0.7\} \text{ V}$, corresponding to different regions of the inverter transfer characteristics, were selected for PUF response extraction. For each V_{in} , the analog outputs $V_{out,i,j} = \{V_{out,1}, \dots, V_{out,9}\}$ were recorded and pairwise compared to generate a 36-bit PUF response using **Equation 2.8 and 2.9**. The resulting bitstrings are shown in **Table 5.1**.

Table 5.1: PUF response for $V_{in} = \{0.4, 0.5, 0.6, 0.7\} \text{ V}$ and $V_{DD} = 1 \text{ V}$. Each bit is generated from a pairwise comparison of inverter output voltages, where ‘1’ denotes $V_{out,i} > V_{out,j}$ and ‘0’ denotes $V_{out,i} \leq V_{out,j}$.

V_{in}	36-bit PUF response
0.4 V	000010001111111011101111111001000011
0.5 V	000010011111111011001111111001000011
0.6 V	000010011111111011001111111001000011
0.7 V	000110011111111011001111111001000111

The Hamming-distance (HD) analysis of the four 36-bit PUF responses reveals a controlled V_{in} dependent variation, with differences in bit flips as the inverter input voltage is varied. The smallest difference is observed between the responses

at $V_{in} = 0.5$ and 0.6 V, which yield identical bitstrings (HD = 0), corresponding to a highly robust ordering of the inverter outputs. In contrast, the largest difference occurs between $V_{in} = 0.4$ and 0.7 V (HD = 6). A limited number of bit flips are observed when stepping $V_{in} = 0.4$ to 0.5 V and again from 0.6 to 0.7 V, with HD = 2 in both cases. This trend is consistent with the measured inverter transfer characteristics. At lower input voltages, the inverter outputs are closely clustered, resulting in limited entropy. Within the transition region, the output voltages diverge significantly due to device-to-device variability, leading to increased entropy. At higher input voltages, the outputs gradually reconverge as the inverters approach saturation, and therefore reducing entropy. Consequently, the optimal operating window for this PUF lies in the mid-transition regime, approximately between $V_{in} = 0.5$ and 0.7 V, where sufficient output variability is achieved while maintaining stable response. This observation is further supported by the standard deviation of V_{out} and the smooth variation of I_{DD} and I_G in this voltage range, indicating a favorable trade-off between entropy generation and electrical stability for reliable PUF bit extraction.

However, analog PUF operation is inherently sensitive to temporal and environmental variations, particularly in printed EGT-based circuits where humidity and small V_{in} shifts can influence inverter output levels and modify the pairwise voltage comparisons between inverter outputs used for PUF bit generation. These effects make stable PUF response non-trivial and require operation within a region where device-to-device variability is maximized. By restricting PUF evaluation within the mid-transition regime around $V_{in} = 0.5$ – 0.7 V, the inverter-array based PUF maintains low intra-device Hamming distance, demonstrating that PUF-based reliable identification is achievable despite the temporal sensitivities of EGTs.

5.2 Printed Temperature Sensor

5.2.1 Design and Fabrication Overview

Two resistive temperature sensor (RTS) geometries corresponding to the *Pt100* and *Pt1000* standards were designed through geometric scaling of the sensing element as a proof of concept to evaluate the feasibility of inkjet printed platinum films for flexible sensing applications. The sensor layouts, shown in **Figure 5.3**, were created using open-source CAD software (Inkscape, GIMP) and exported in monochrome bitmap format suitable for inkjet printing.

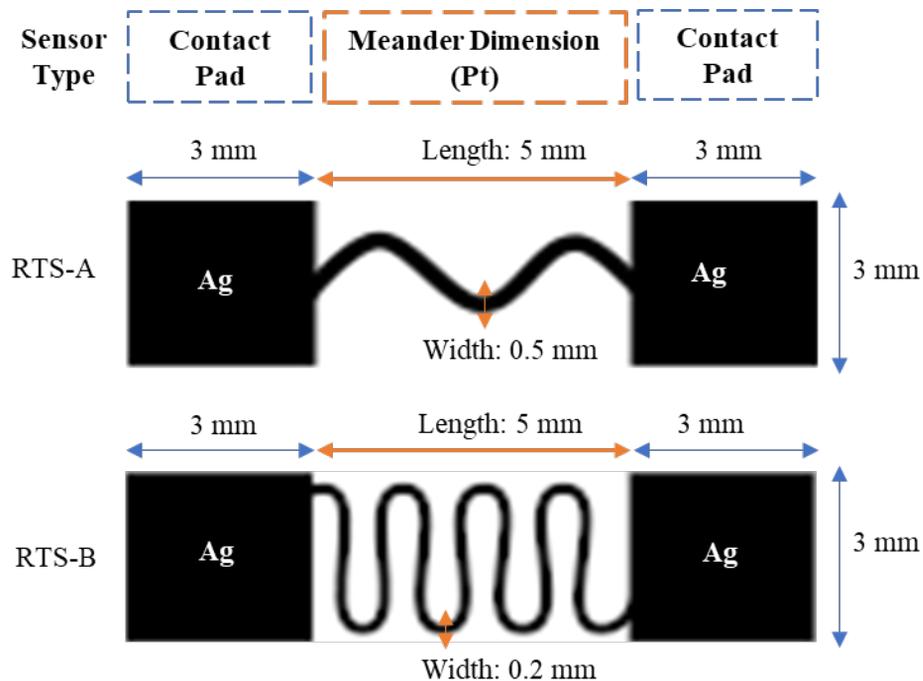


Figure 5.3: The layout and dimensions of two RTSs designs. RTS-A consists of a single-meander Pt sensing element with a track width of 0.5 mm, corresponding to a *Pt100*-type geometry. RTS-B employs a multi-meander Pt sensing element with a reduced track width of 0.2 mm, corresponding to a *Pt1000*-type geometry. The effective meander length depend solely on the number of meander and the geometry, while the overall sensor footprint and Ag contact spacing remain unchanged. In both designs, Ag contact pads with dimensions of 3 mm × 3 mm are used for electrical interfacing. Adapted from^[81] under the Creative Commons CC BY license.

Meander-type geometries were employed to achieve high resistance within a compact area while ensuring homogeneous temperature distribution and mechanical compliance during bending^[49,83]. The *Pt100*-type sensor (RTS-A) employs a single-meander geometry with a linewidth of 0.5 mm. The *Pt1000*-type sensor (RTS-B) utilizes a multi-meander geometry with narrower lines of 0.2 mm, resulting in an increased effective conductive path length. Both sensor designs incorporated identical Ag contact pads ($3 \times 3 \text{ mm}^2$) to facilitate reliable probing and to provide stable, low-resistance electrical contacts while minimizing mechanical wear of the Pt sensing layer.

The fabrication process, summarized schematically in **Figure 5.4**, employed inkjet printing followed by thermal sintering steps to form the functional sensor structures. The Pt nanoparticle ink was deposited first to form the sensing element, followed by Ag nanoparticle ink to create contact pads. Prior to printing, polyimide substrates were cleaned with isopropanol and dried under nitrogen to improve wettability and adhesion. Both Pt and Ag inks were ultrasonicated before use to prevent nozzle clogging and ensure consistent droplet formation. The printed Pt films were sintered at $250 \text{ }^\circ\text{C}$ for 30 minutes (as established by in-situ resistance measurements and TGA analysis in **Section 3.3.4**) to achieve a continuous conductive network. The Ag pads were subsequently printed and sintered at $100 \text{ }^\circ\text{C}$ for 30 minutes to preserve the underlying Pt structure and maintain strong interfacial adhesion. This sequential printing and low-temperature sintering strategy yielded fully-printed and electrically reliable sensors suitable for flexible sensing.

Following sintering, the printed Pt films exhibited an electrical conductivity of approximately $8.47 \times 10^5 \text{ S} \cdot \text{m}^{-1}$ ($\approx 8.5\%$ of bulk Pt^[22,75]), providing stable film resistance and reliable current flow ($\approx 1 \text{ mA}$), both essential for accurate and repeatable temperature sensing. The Ag contact pads, sintered under milder thermal conditions, exhibited a conductivity of $0.95 \times 10^7 \text{ S} \cdot \text{m}^{-1}$ ($\approx 15\%$ of bulk Ag^[75]), ensuring reliable electrical interfacing with the printed Pt layer and stable probe contacts during characterization. Overall, the achieved conductivities represent an optimal balance between electrical performance and substrate compatibility, validating the effectiveness of the processing strategy for flexible temperature sensing.

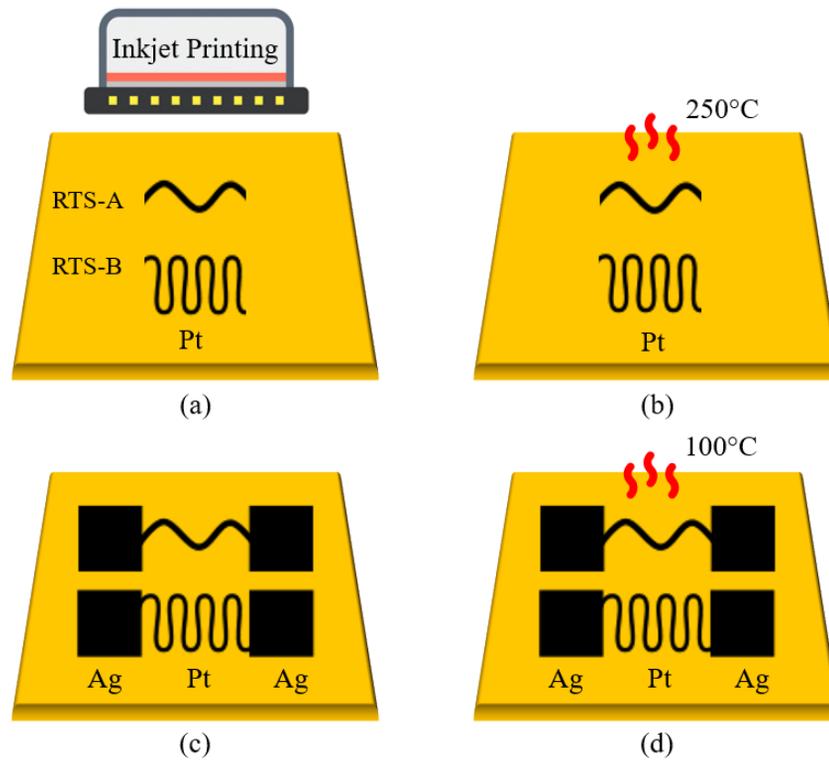


Figure 5.4: Schematic illustration of the fabrication process for printed Pt-based RTSs. (a) Inkjet printing of Pt nanoparticle inks in two meander geometries (RTS-A and RTS-B) on polyimide substrates. (b) Thermal sintering of the printed Pt structures at 250 °C to form conductive networks. (c) Inkjet printing of Ag contact pads for electrical interfacing. (d) Low-temperature sintering of Ag contacts at 100 °C to ensure reliable electrical probing without degrading the sensing element Pt. Adapted from^[81] under the Creative Commons CC BY license.

5.2.2 Structural and Morphological Characterization

The inkjet printed RTSs were geometrically and morphologically characterized to validate the fidelity of the printed designs and assess film quality. The printed meander structures exhibited precise alignment with the CAD layouts, confirming the dimensional accuracy achievable through inkjet printing. Optical microscopy (**Figure 5.5a**) revealed well-defined Pt meanders in continuous contact with the Ag contact pads, ensuring reliable electrical interfacing for sensor characterization. No visible discontinuities, spreading defects, or delamination were observed, indicating proper sintering and solvent removal.

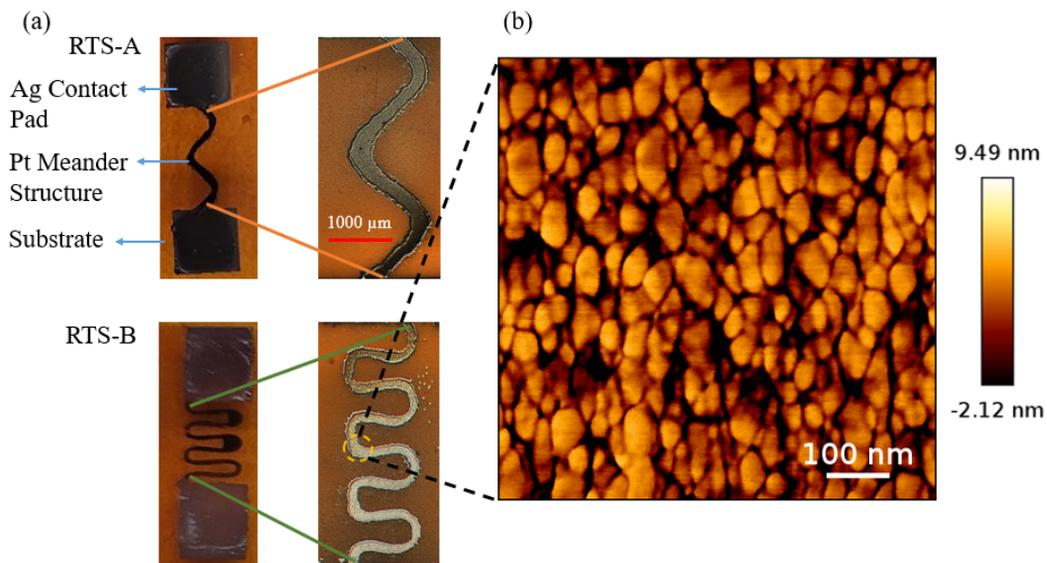


Figure 5.5: (a) Optical microscopy image of an inkjet-printed Pt (type-A and type-B) temperature sensors on a polyimide substrates, showing sensor layout and meander geometry. (b) AFM image of the printed Pt film, revealing a dense and continuous nanoparticle network formed after sintering. Adapted from^[81] under the Creative Commons CC BY license.

AFM analysis (**Figure 5.5b**) revealed smooth and uniform Pt films with interconnected nanoparticle grains, which enhances electrical conductivity and supports efficient charge transport while maintaining stable temperature-dependent resistance. These features collectively improve the sensing performance by increasing the TCR and providing greater structural stability to the sensing element.

5.2.3 Electrical Characterization and Temperature Response

The electrical performance of the printed RTSs was evaluated under ambient conditions (relative humidity $\approx 50\%$) using a temperature-controlled hotplate between $20\text{ }^{\circ}\text{C}$ and $80\text{ }^{\circ}\text{C}$ under steady-state conditions. The resistance–temperature (R–T) characteristics of the *Pt*100-type (RTS-A) and *Pt*1000-type (RTS-B) sensors are presented in **Figure 5.6**. Both sensor types exhibited highly linear R–T responses across the investigated temperature range, with average regression coefficients ($R^2 \approx 0.999$), indicating stable and reproducible device operation.

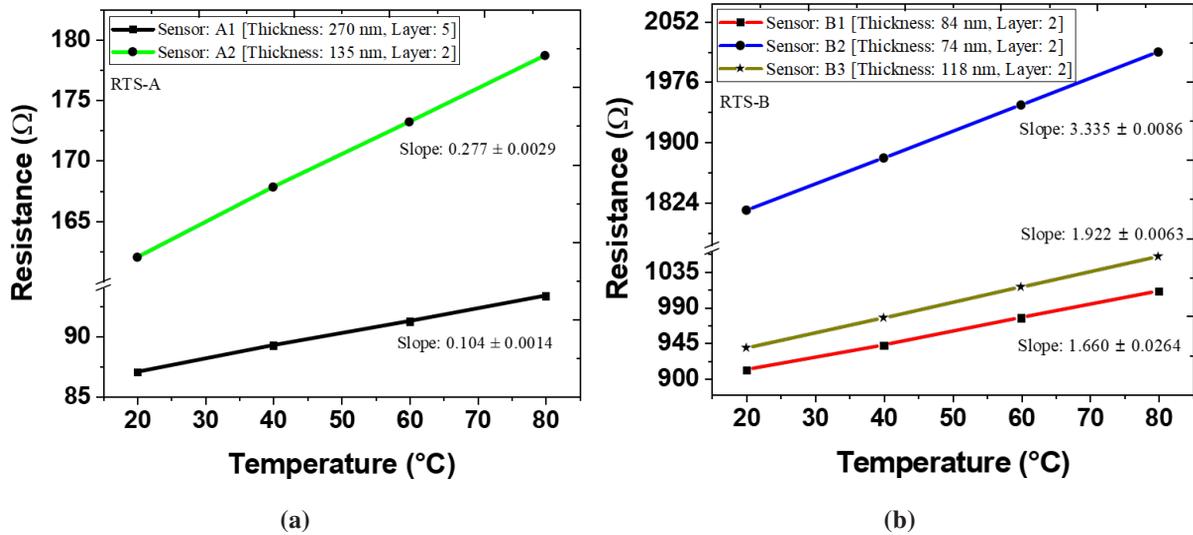


Figure 5.6: Resistance–temperature characteristics of inkjet printed (a) *Pt*100 (RTS-A) and (b) *Pt*1000 (RTS-B) sensors measured between $20\text{ }^{\circ}\text{C}$ and $80\text{ }^{\circ}\text{C}$. The resistance and thickness measurements were performed with uncertainties of $\pm 0.1\ \Omega$ and $\pm 5\ \text{nm}$, respectively. Adapted from^[81] under the Creative Commons CC BY license.

For RTS-A, devices fabricated with two (A2) and five (A1) printed Pt layers resulted in film thicknesses of approximately 135 nm and 270 nm, respectively, on a fixed meander geometry ($5\ \text{mm} \times 0.5\ \text{mm}$). For RTS-B, all devices (B1–B3) were fabricated using two printed layers on a narrower meander geometry ($5\ \text{mm} \times 0.2\ \text{mm}$), yielding film thicknesses between 74 nm and 118 nm. The Ag contact pads, with an average thickness of approximately $500\ \mu\text{m}$, ensured robust adhesion and stable electrical contacts during RTSs probing.

From the linear fits of the R–T curves in **Figure 5.6**, the nominal resistance, TCR, and sensitivity were extracted for the printed RTSs and are summarized in **Table 5.2**. The nominal resistance of RTS-A sensors ranged from 87 Ω to

Table 5.2: Summary of nominal resistance, TCR, and sensitivity values for inkjet printed RTS-A (*Pt100*) and RTS-B (*Pt1000*) sensors, compared with reported literature values and bulk Pt standards. Resistance values are subject to an uncertainty of approximately $\pm 0.1 \Omega$, limited by measurement resolution and probe-contact repeatability. *Adapted from*^[81] *under the Creative Commons CC BY license.*

Sensor Label	Nominal Resistance $R_{20^\circ\text{C}}$ [Ω]	TCR, α [$^\circ\text{C}^{-1}$]	Sensitivity S [$\Omega^\circ\text{C}^{-1}$]	Sensing Range T [$^\circ\text{C}$]	References
<i>Pt100</i>	107.7	0.00357	0.385	0–80	Bulk <i>Pt100</i> ^[22]
R1	463	0.000576	0.255	28–80	Timothy <i>et al.</i> ^[84]
A1	87	0.00121	0.104	20–80	This Thesis
A2	162	0.00172	0.277	20–80	This Thesis
<i>Pt1000</i>	1077.9	0.00358	3.850	0–80	Bulk <i>Pt1000</i> ^[23]
B1	911	0.00181	1.660	20–80	This Thesis
B2	1814	0.00184	3.335	20–80	This Thesis
B3	938.5	0.00205	1.922	20–80	This Thesis

162 Ω , while RTS-B sensors exhibited resistances between 911 Ω and 1814 Ω . Compared to RTS-A, a larger spread in nominal resistance was observed among RTS-B sensors, even for devices with comparable average film thickness. This increased resistance variation is primarily attributed to the narrower meander geometry employed for RTS-B (5 mm \times 0.2 mm), which increases the effective conductive path length and is sensitive to local process-induced variations during inkjet printing and subsequent sintering. Despite these variations in nominal resistance, the extracted TCR values remained highly consistent across devices.

The printed RTS-A sensors exhibited TCR values ranging from 0.00121 to 0.00172 $^\circ\text{C}^{-1}$ and sensitivities between 0.104 and 0.277 $\Omega^\circ\text{C}^{-1}$ over 20 $^\circ\text{C}$ to 80 $^\circ\text{C}$, which are higher than those reported by Timothy *et al.*^[84], highlighting the influence of meander geometry on the effective conductive path length and

sensor response. The maximum measured TCR ($0.00172\text{ }^{\circ}\text{C}^{-1}$) and sensitivity ($0.277\text{ }\Omega^{\circ}\text{C}^{-1}$) correspond to approximately 48% and 72%, respectively, of the bulk *Pt*100 reference values. Similarly, the printed RTS-B sensors showed TCR values between 0.00181 and $0.00205\text{ }^{\circ}\text{C}^{-1}$ and sensitivities ranging from 1.66 to $3.34\text{ }\Omega^{\circ}\text{C}^{-1}$ over the same temperature range. The highest recorded TCR ($0.00205\text{ }^{\circ}\text{C}^{-1}$) and sensitivity ($3.34\text{ }\Omega^{\circ}\text{C}^{-1}$) reached approximately 57% and 87%, respectively, of the bulk *Pt*1000 standards^[23]. These results demonstrate the strong performance of inkjet printed *Pt*1000-type sensors on polyimide substrates and establish benchmark data for printed Pt-based sensors operating in the $20\text{ }^{\circ}\text{C}$ to $80\text{ }^{\circ}\text{C}$ range, for which quantitative reports remain limited.

The deviation in nominal resistance, TCR and sensitivity values of the printed RTSs (RTS-A and RTS-B), compared to their bulk counterparts, attributed to several intrinsic and process-related factors that directly influence $\Delta R/\Delta T$ and the effective TCR. First, the Pt nanoparticle composition (particle size 15 nm to 25 nm , $2.9\text{ wt.}\%$ solid content) introduces enhanced surface scattering and size-dependent conductivity effects that lower the effective TCR compared to bulk Pt. Second, incomplete nanoparticle coalescence after sintering leads to grain boundary resistance, further reducing conductivity. Third, printing-induced variations such as droplet coalescence, film thickness, and substrate wetting characteristics introduce microstructural inhomogeneities that affect resistance uniformity. Finally, the sintering temperature ($250\text{ }^{\circ}\text{C}$) governs the extent of nanoparticle necking and film densification. Although higher sintering temperatures could further enhance electrical connectivity and shift the TCR toward bulk values, the thermal limits of polyimide substrates impose a trade-off between electrical performance and substrate compatibility.

However, repeated heating-cooling cycles produced nearly identical R–T characteristics with negligible loop opening, confirming minimal hysteresis and stable sensor operation under cyclic thermal loading (**Figure 5.7**). This behavior indicates uniform heat distribution and good thermal coupling between the Pt film and the polyimide substrate, conditions typically associated with fast and reversible response in thin-film Pt sensors.

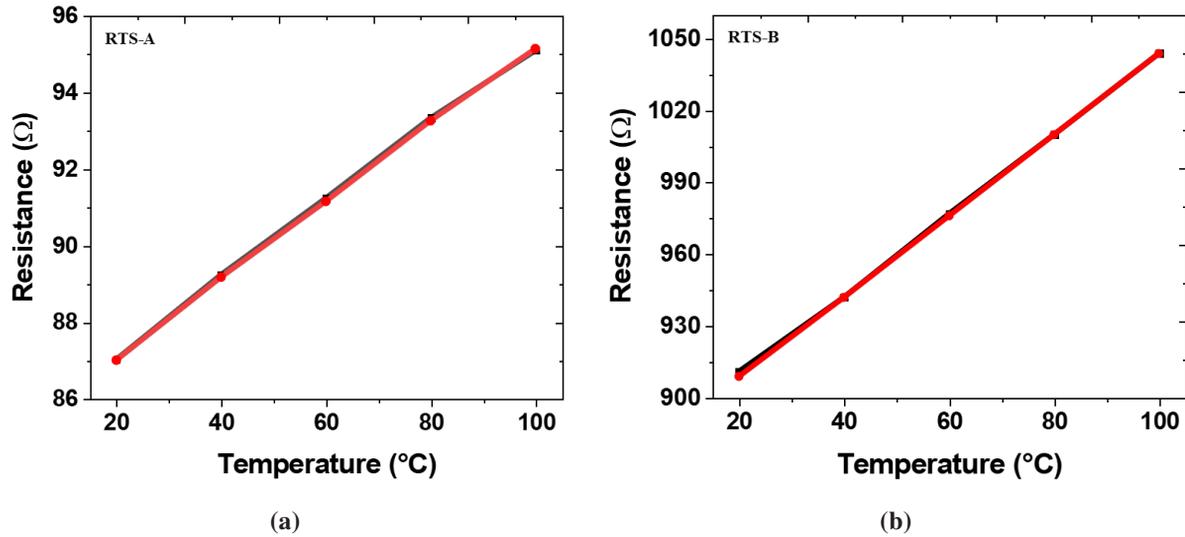


Figure 5.7: Resistance–temperature characteristics of Pt sensors (a) RTS-A (*Pt*100) and (b) RTS-B (*Pt*1000) measured between 20 °C and 100 °C to evaluate hysteresis behavior. The heating (black) and cooling (red) curves overlap, indicating negligible hysteresis and stable thermal response. Adapted from^[81] under the Creative Commons CC BY license.

5.2.4 Mechanical Flexibility and Bending Stability

The mechanical durability of the printed *Pt*1000-type RTS-B was evaluated to assess their stability under repeated bending, which is critical for flexible and conformal applications. The sensor printed on polyimide substrate was mounted on a cyclic bending apparatus that repeatedly flexed the devices over a spherical surface with a bending radius of 8 mm, illustrated in **Figure 5.8**. The electrical resistance was continuously monitored in real time during mechanical cycling at room temperature to quantify the change in resistance under strain.

As shown in **Figure 5.9a**, the resistance of the printed *Pt*1000 meander structures increased marginally from 912 Ω to 920 Ω during a single bending cycle, corresponding to a drift of less than 1 %. Over 400 bending cycles, the resistance remained nearly constant, indicating that the meander geometry effectively distributes mechanical strain and suppresses crack initiation within the Pt conductive path. In contrast, single printed Pt-line structures without meanders showed more pronounced resistance fluctuations during the first 50 cycles, followed by

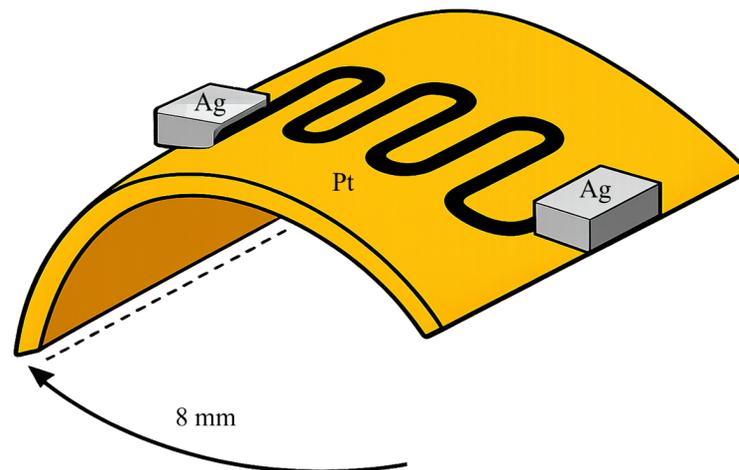


Figure 5.8: Schematic illustration of the bending test configuration used to evaluate the mechanical flexibility of the printed $Pt1000$ resistive temperature sensor on a polyimide substrate. The sensor is cyclically bent over a curved surface with a bending radius of 8 mm, while the Pt sensing element and Ag contact pads remain electrically connected during deformation.

a gradual, linear increase with a total drift of less than 1 % even after 400 cycles (**Figure 5.9b**), confirming mechanical stability and adhesion of the Pt films on polyimide substrates. This behavior demonstrates that the interconnected Pt nanoparticle network retains mechanical integrity and electrical continuity even under cyclic deformation.

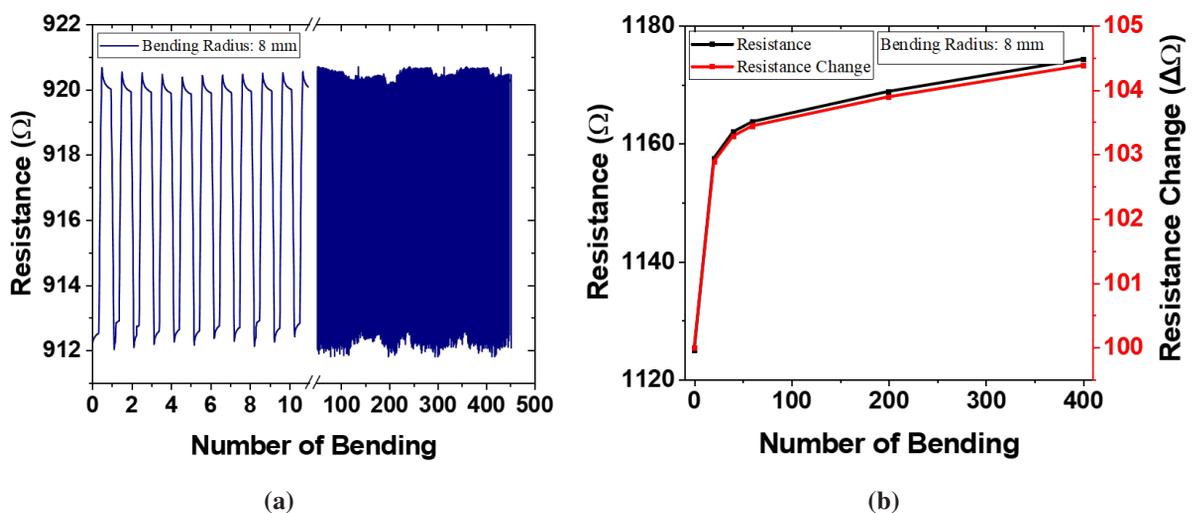


Figure 5.9: (a) Bending test of an inkjet printed meander structured $Pt1000$ RTS on a polyimide substrate. (b) Effect of cyclic bending on a single printed Pt-line, showing more pronounced resistance variations during the first 50 cycles. Adapted from^[81] under the Creative Commons CC BY license.

Furthermore, microstructural inspection using SEM (**Figure 5.10**) revealed that the *Pt*1000 meander films retained continuous conductive pathways after repeated bending. Only localized, nanoscale microcracks were observed post-cycling, which likely originate from transient strain but do not propagate through the entire trace. These minor surface defects have no measurable impact on the overall sensor resistance or performance stability, consistent with the negligible drift observed electrically. Although extended cyclic bending tests up to 1000 cycles would provide deeper insight into long-term reliability, the results up to 400 cycles sufficiently confirm the mechanical stability of the printed sensors within this proof of concept study.

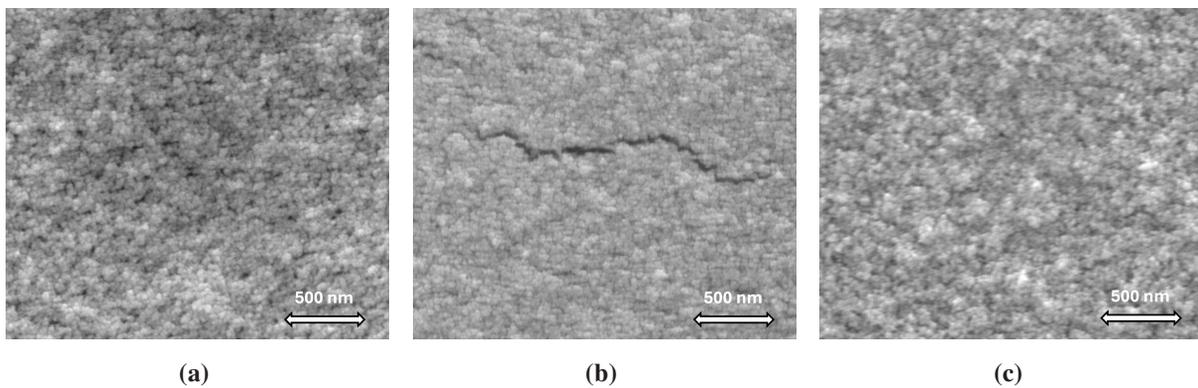


Figure 5.10: SEM images of the inkjet printed *Pt*1000 meander structures (a) before, (b) during, and (c) after bending, showing the structural integrity and surface morphology evolution under mechanical stress. Adapted from^[81] under the Creative Commons CC BY license.

However, compared to the $\sim 10\text{--}12\%$ resistance variation observed over the $20\text{--}80\text{ }^{\circ}\text{C}$ sensing range of the printed *Pt*1000 RTS, the bending-induced resistance drift ($< 1\%$) was negligible, indicating that mechanical strain has minimal influence on sensor performance. Based on this performance, the *Pt*1000 sensor was selected for hybrid system-in-foil integration in automotive sensing applications, as its higher nominal resistance yields a larger resistance change per degree Celsius, thereby minimizing the relative impact of interconnect resistances and ensuring robust compatibility with the foil-embedded ASIC readout circuitry.

5.3 Summary

This chapter demonstrated the fabrication and experimental validation of a printed inverter-array based PUF and platinum-based resistive temperature sensors. The printed PUF exhibits pronounced device-to-device variability arising from intrinsic process-induced differences in EGTs and resistor geometries, which serve as the analog entropy source for PUF bit extraction. Electrical analysis identified the inverter transition region at $V_{\text{in}} = 0.5\text{--}0.7$ V as the optimal operating window, where pairwise comparison of inverter output voltages yields stable 36-bit PUF responses with low intra-device Hamming distance variation. Within this operating regime, the supply current remains low due to partial channel accumulation in the EGT and resistor-controlled current flow. At $V_{\text{in}} = 0.5$ V, the maximum supply current is $I_{\text{DD}} \approx 163$ μA , corresponding to a power consumption of ≈ 163 μW at $V_{\text{DD}} = 1$ V, compared to ≈ 366 μW at $V_{\text{in}} = 1$ V. In this range, the accumulated gate leakage current of the nine-inverter array remains small (≈ 340 nA at $V_{\text{in}} = 1$ V), contributing less than 0.1% to the total power consumption. These results confirm the suitability of the printed EGT-based PUF as an effective low-voltage, low-power device-level analog entropy source for PUF operation.

In parallel, inkjet printed nanoparticle platinum-based resistive temperature sensors were realized on polyimide substrates. An optimized sintering process at 250 °C for 30 minutes enabled stable conductive Pt networks while maintaining substrate compatibility. Two sensor geometries corresponding to *Pt100*- and *Pt1000*-type designs were fabricated, and both sensor types exhibited linear resistance–temperature characteristics over an automotive-relevant range from 20 °C to 80 °C. For the *Pt100* sensor, the maximum measured TCR of 0.00172 °C⁻¹ and sensitivity of 0.277 Ω °C⁻¹ correspond to approximately 48% and 72%, respectively, of the bulk *Pt100* reference values. The *Pt1000*-type sensors achieved a maximum effective TCR of 0.00205 °C⁻¹ and a sensitivity of 3.335 Ω °C⁻¹, corresponding to approximately 57% and 87% of bulk *Pt1000* standards. Mechanical reliability was confirmed through cyclic bending tests, with resistance

drift remaining below 1 % after 400 bending cycles at an 8 mm bending radius, which is negligible compared to the $\sim 10\text{--}12\%$ resistance change across the $20\text{ }^{\circ}\text{C}$ to $80\text{ }^{\circ}\text{C}$. Based on the higher nominal resistance and enhanced sensitivity, the *Pt1000*-type sensor was selected for subsequent system-level integration and ASIC-based readout.

Overall, this chapter established printed inverter-array based PUF and *Pt1000*-type resistive temperature sensors as complementary device-level building blocks for hardware security and sensing, forming the basis for subsequent hybrid integration with a foil-embedded ASIC.

6 Hybrid System-in-Foil Integration of Printed PUF and Temperature Sensor

This chapter presents the system-level realization of the hybrid system-in-foil architecture, integrating the printed PUF and temperature sensors with a custom backside-thinned ASIC embedded in a polyimide foil. The hybrid system is mechanically assembled into an automotive-relevant T-piece module, enabling reliable system-level access and validation of temperature sensing and hardware identification, and demonstrating compatibility with automotive-oriented security framework. For completeness and transparency of the hybrid system-in-foil realization, supplementary information on workflow and the scope of external contributions is provided in **Appendix A.3**. Parts of this chapter build upon results previously published in^[85,82]. The content has been restructured and expanded in accordance with the scope of this thesis.

6.1 Hybrid System-in-Foil Architecture and ASIC Integration

This section describes the design and realization of the hybrid system-in-foil architecture based on polyimide foil. The foil defines the physical layout, electrical interfaces, and metal routing required to interconnect the printed PUF, the printed temperature sensor, the embedded ASIC, and the backend peripheral interface within a compact and mechanically compliant structure suitable for automotive

integration. An overview of the foil layout and the fabricated foil is presented in **Figure 6.1**, which combines the designed foil architecture with annotated dimensions and interface regions, as well as the physically realized foil. This representation demonstrates the consistency between layout design and fabrication outcome and serves as a reference for the subsequent architectural description.

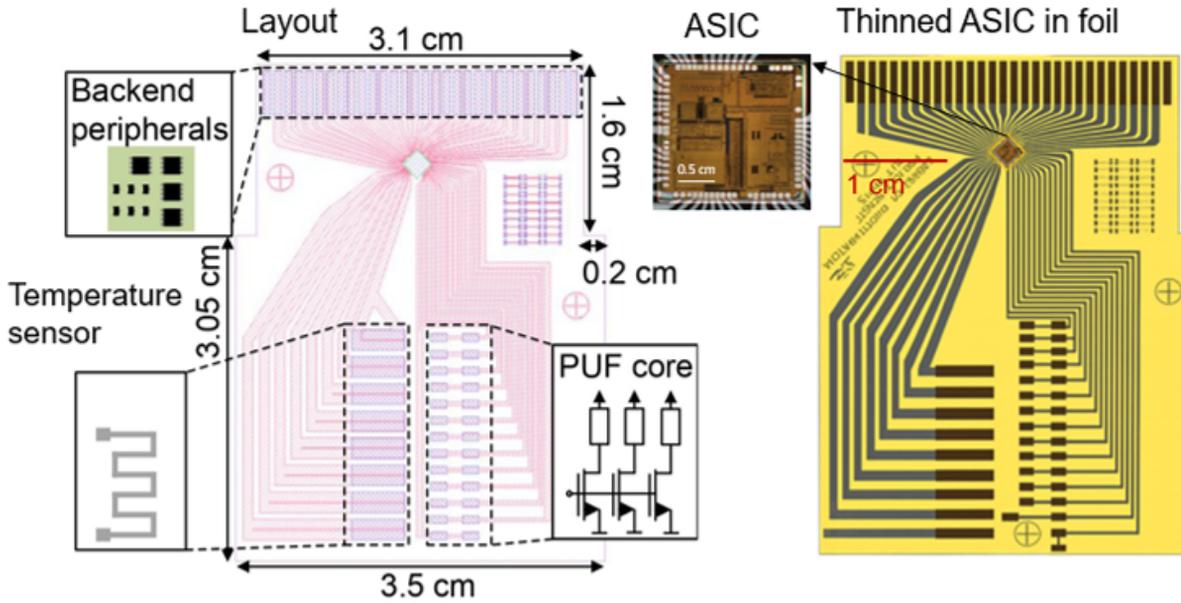


Figure 6.1: Polyimide foil architecture and physical realization for the hybrid system-in-foil.

Left-side: Designed polyimide foil layout showing the interface regions for the printed PUF core, printed temperature sensor, ASIC placement and interconnection area, and backend peripheral interface, including key dimensions and routing structure. Right-side: Manufactured foil illustrating the realized Au contact pads, in-foil metal routing, and ASIC interface zones corresponding to the layout design. *Reproduced with permission from^[82], © IEEE 2025.*

The polyimide foil is structured into three spatially separated functional interface regions, namely the printed PUF interface, the printed temperature sensor interface, and the backend peripheral interface, with a centrally reserved ASIC placement and interconnection area. This spatial partitioning reduces routing congestion, limits mechanical stress coupling between interfaces, and enables efficient interconnection without multilayer crossovers. The overall foil footprint is approximately $3.5\text{ cm} \times 3.1\text{ cm}$. Within this area, 49 in-foil interconnects provide the required electrical connections between the ASIC, printed frontend devices

(PUF and temperature sensor), and the backend interface. The in-foil metal interconnects are electrically isolated by an additional spin-coated polyimide top layer, while gold-coated contact pads form the accessible electrical terminals for physical connection.

6.1.1 PUF Interface on Foil

The PUF core is interfaced on the right-hand side of the foil layout, as indicated by the dashed region in **Figure 6.1**. The designated placement area for the PUF core has dimensions of $19.3\text{ mm} \times 8\text{ mm}$, matching the footprint of the PUF developed in this thesis. Electrical interfacing is provided through 13 pre-defined Au contact pads, designed for flip-chip-derived mounting using conductive adhesive. Each pad has a size of $700\text{ }\mu\text{m} \times 1.5\text{ mm}$ with a pitch of 1.55 mm , offering sufficient alignment tolerance while maintaining compact routing. The metal traces connecting the PUF pads to the ASIC interface are routed symmetrically with increased line width where required. As the PUF interface carries no high-speed or dynamic signals, this routing strategy minimizes parasitic mismatch while allowing longer interconnect lengths without compromising functionality.

6.1.2 Temperature Sensor Interface

The interface to the temperature sensor is located on the left-hand side of the foil. To facilitate robust electrical and mechanical integration, the foil incorporates 8 parallel Au contact pads, each with a size of $940\text{ }\mu\text{m} \times 5\text{ mm}$ and a pitch of 2.56 mm . The extended pad length and parallel routing are chosen to support the use of stretchable conductive interconnects during hose-embedding and to reduce contact resistance under bending and strain. Compared to the PUF interface, the temperature sensor routing is less critical with respect to parasitic effects, allowing increased interconnect length to be compensated by wider metal lines.

6.1.3 ASIC Placement and Backend Peripheral Interface

The ASIC placement area occupies the central region of the polyimide foil and provides the electrical connection between the ASIC and in-foil interconnects. The ASIC I/O pads interfacing with the foil metallization have dimensions of $63\ \mu\text{m} \times 66\ \mu\text{m}$ with a minimum pitch of $80\ \mu\text{m}$. The allocated ASIC footprint on the foil is approximately $2\ \text{mm} \times 2\ \text{mm}$, with additional clearance provided for adhesive bonding and routing symmetry. To minimize in-foil interconnect length and resistance while avoiding routing crossovers, the ASIC is arranged at a 45° orientation with respect to the backend peripheral interface. This orientation also provides sufficient spacing between neighboring metal lines within the single-layer routing scheme.

The backend peripheral interface is implemented on the top side of the foil and comprises 28 Au contact pads, including 2 unconnected dummy pads, designed to be compatible with standard single-row flexible printed circuit (FPC) connectors with 30 positions. Each backend pad has a size of $700\ \mu\text{m} \times 4.1\ \text{mm}$ and a pitch of $1\ \text{mm}$, enabling reliable electrical contact and repeated connection cycles. Routing priority is given to electrically critical lines, including power supply, ground, and serial parallel interface (SPI)/ general-purpose input/output (GPIO) communication lines, which are implemented with short path lengths and increased line width. Connections to the PUF and temperature sensor interfaces are electrically less critical and are routed accordingly to optimize layout efficiency and mechanical robustness.

6.1.4 In-Foil Interconnect Resistance

The electrical quality of the in-foil interconnects is characterized by their resistance between the ASIC pads and the respective interface regions. The average resistance between the ASIC-in-foil and the backend peripheral interface is $1.38\ \Omega$ with a standard deviation of $0.47\ \Omega$. For the ASIC-in-foil to temperature sensor interface, an average resistance of $2.26\ \Omega$ with a standard deviation of $0.50\ \Omega$ is

obtained. The full interconnect path between the PUF interface and the ASIC, which is the electrically least critical interface, exhibits an average resistance of $4.38\ \Omega$ with a standard deviation of $1.08\ \Omega$. These values confirm that the foil-based metallization and contact strategy provide sufficiently low resistance for reliable system-level operation, while preserving mechanical compliance and layout flexibility^[85].

6.1.5 ASIC Technology and System-Level Role

The hybrid system employs a custom CMOS ASIC fabricated in TSMC 180 nm technology and operates at a supply voltage of 3.3 V, allowing direct compatibility with standard automotive electronics. To enable mechanical embedding into a flexible foil, the ASIC is backside-thinned from an initial bare die thickness of approximately $230\ \mu\text{m}$ to about $30\ \mu\text{m}$. The thinned ASIC is embedded into a polyimide foil, which acts as a mechanically compliant carrier with integrated electrical routing. The ASIC integrates functional blocks for resistive sensor readout, PUF addressing and evaluation, as well as digital configuration for data access. These capabilities define the system-level electrical functionality of the ASIC and are described on block level in **Appendix A.1**.

6.2 Printed Device Integration into ASIC in Foil

This section describes the physical and electrical integration of the printed PUF and the printed $Pt1000$ temperature sensor into the hybrid system-in-foil architecture introduced in **Section 6.1**. The focus of this section is on the integration strategy, mechanical compatibility, and electrical interfacing, while the standalone feasibility of the printed devices were addressed earlier.

6.2.1 Integration of the Printed PUF into ASIC-in-Foil

The printed PUF is integrated into the ASIC-in-foil architecture by aligning its dimensions with the pre-defined PUF interface described in **Section 6.1**. The PUF, fabricated on a glass substrate with an initial size of $20\text{ mm} \times 10\text{ mm}$, is adjusted to an active area of $19.3\text{ mm} \times 8\text{ mm}$, matching the PUF integration region reserved in the foil layout. Electrical interconnection between the printed PUF and the foil is realized using conductive Ag paste applied between the ITO contact pads of PUF and the gold-coated in-foil pads. This interconnection approach tolerates alignment inaccuracies and surface non-planarity inherent to printed electronics while providing reliable electrical contact. The Ag-filled conductive paste exhibits a volume resistivity of $1 \times 10^{-4}\ \Omega\text{ cm}$ to $5 \times 10^{-4}\ \Omega\text{ cm}$, corresponding to an electrical conductivity of approximately $2 \times 10^5\ \text{S m}^{-1}$ to $1 \times 10^6\ \text{S m}^{-1}$, which is sufficient to ensure low-resistance interconnection for printed PUF readout. No fine-pitch bonding or high-temperature processing is required, ensuring compatibility with flexible substrates and scalable assembly. The integrated printed PUF is shown as part of the fully assembled hybrid system-in-foil assembled in the T-piece module, as presented in **Figure 6.4 (Top left)**.

6.2.2 Integration of the Printed Sensors into ASIC-in-Foil

The printed temperature sensors were integrated differently from the PUF into the hybrid system-in-foil architecture to enable distributed temperature sensing within an automotive coolant hose. The sensors were electrically interfaced using screen-printed, stretchable elastomer–Ag interconnects fabricated on a thermoplastic polyurethane (TPU) substrate. The paste used for manufacturing these stretchable interconnects exhibits a typical sheet resistance of 0.010–0.013 Ω/\square , ensuring low series resistance and thereby negligible influence on the subsequent sensor readout. Electrical connection between the Pt sensor contact pads and the stretchable interconnects is achieved using electrically conductive adhesive, providing both mechanical stability and low contact resistance. The Ag contact pads prevent strain-induced resistance changes in the Pt sensing element, while the stretchable TPU interconnects accommodate mechanical deformation. Strain-related resistance variations in the elastomer–Ag interconnects are compensated by a four-wire measurement configuration, with two dedicated interconnect lines per sensor routed over lengths of 10 cm and 20 cm, respectively. This configuration avoids rigid wiring and reduces mechanical stress at the sensor interface, which is critical for reliable operation in automotive environments. An image of the heterogeneous integration prior to hose-embedding is shown in **Figure 6.2 (top)**. The Pt sensing element has an average linewidth of approximately 300 μm , a total meander length of 5.5 mm, and an average thickness of 120 nm.

In a subsequent processing step, the sensor assemblies, including the stretchable Ag-patch interconnects, are embedded into the layer stack of an industrial coolant hose with an inner diameter of 18 mm. The outer Ag contact pads of the TPU-based interconnects remain outside the hose and are accessible for subsequent electrical connection to the ASIC-in-foil architecture, as shown in **Figure 6.2 (bottom)**. To verify that mechanical hose-embedding does not degrade the electrical functionality required for subsequent ASIC-based readout, the resistance–temperature behavior of both sensing elements is evaluated after hose-embedding.

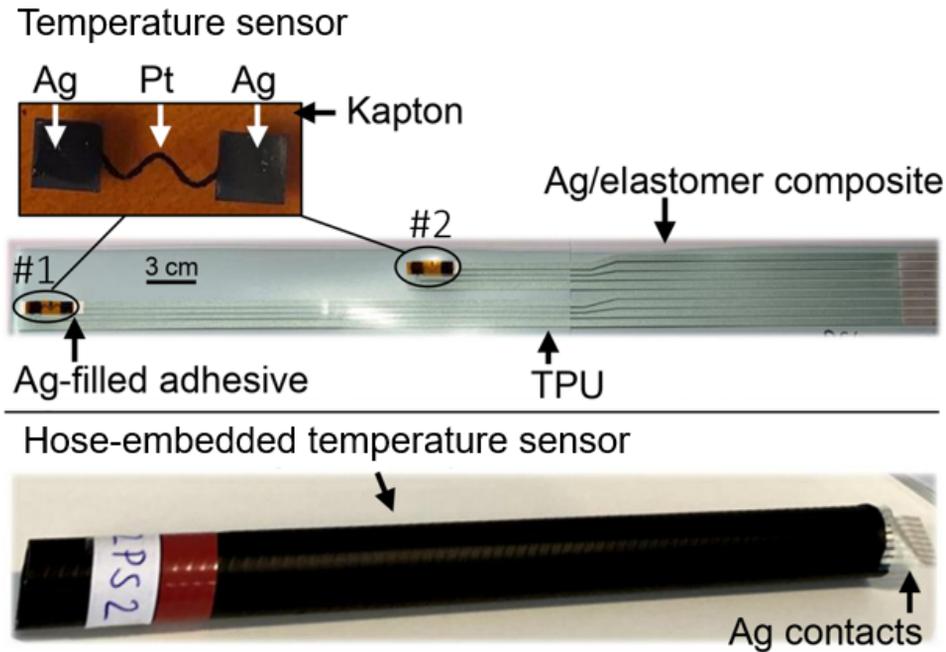


Figure 6.2: Printed Pt1000 temperature sensor and subsequent hose-embedding.

Top: Inkjet-printed Pt temperature sensor on polyimide substrates electrically and mechanically connected to screen-printed stretchable elastomer–Ag interconnects on TPU substrate using Ag-filled conductive adhesive. Bottom: printed sensor embedded into a coolant hose with accessible Ag contact pads for connection to the ASIC-in-foil interface. *Reproduced with permission from^[82], © IEEE 2025.*

Both Pt sensing elements are designed for a nominal resistance of approximately $1\text{ k}\Omega$ at $25\text{ }^\circ\text{C}$, ensuring compatibility with the ASIC readout circuitry. The measured resistance–temperature characteristics are shown in **Figure 6.3**. Both sensing elements exhibit a linear resistance–temperature relationship with high goodness of fit. The measured resistance values (blue markers) closely follow a linear regression model (solid black line) over the investigated temperature range from $20\text{ }^\circ\text{C}$ to $80\text{ }^\circ\text{C}$. The corresponding coefficients of determination reach $R^2 = 0.999$ for sensor #1 and $R^2 = 0.997$ for sensor #2, confirming excellent linearity despite mechanical embedding into the hose. The relative deviation between measured values and linear fit remains below $\pm 0.1\%$ across the full temperature range for both sensors, indicating that neither the stretchable interconnects nor the hose-embedding introduce significant non-linearities.

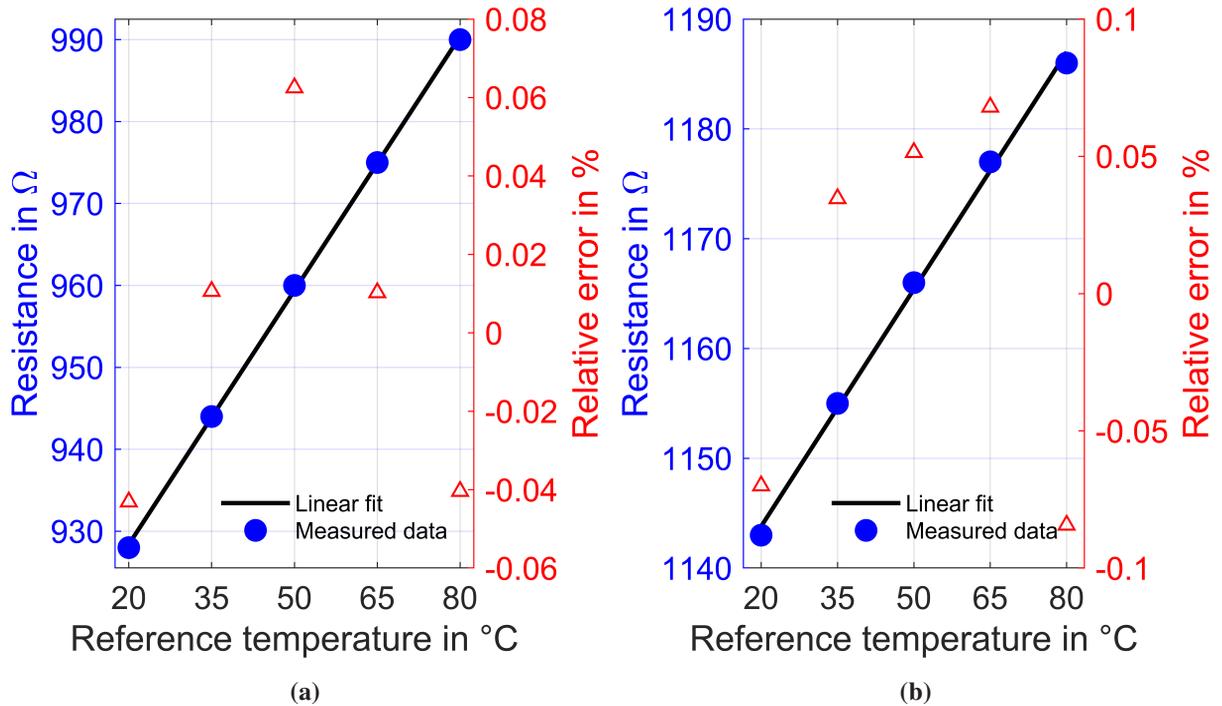


Figure 6.3: Resistance–temperature characteristics of two temperature sensors after hose-embedding. Measured resistance values (blue circles) and linear regression fits (solid black lines) for two sensors over a temperature range from 20 °C to 80 °C. The relative deviation between the measured data and the linear fit is shown as red triangles on the secondary y-axis. (a) For sensor #1, the relative error remains within -0.043% to 0.062% , while (b) sensor #2 exhibits a slightly larger but still limited deviation ranging from -0.084% to 0.068% . Adapted from^[82], © IEEE 2025.

The extracted sensitivities of $1.033 \Omega \text{ } ^\circ\text{C}^{-1}$ for sensor #1 and $0.717 \Omega \text{ } ^\circ\text{C}^{-1}$ for sensor #2 reflect the expected spread due to geometric variations and integration tolerances. Importantly, the observed linear behavior and low relative error confirm the electrical stability of the printed Pt-based temperature sensors after hose-embedding. The outer Ag contact pads of the hose-embedded temperature sensors are integrated into the hybrid system-in-foil architecture using the conductive adhesive, as illustrated in **Figure 6.4 (Top left)**.

6.2.3 T-Piece Assembly of the Hybrid System-in-foil

Following the individual integration of the printed PUF and the hose-embedded temperature sensors into the hybrid system-in-foil architecture, the system is mechanically assembled into a custom T-piece module, forming a compact and mechanically realistic automotive demonstrator. The fully assembled hybrid system-in-foil in the T-piece is shown in **Figure 6.4**.

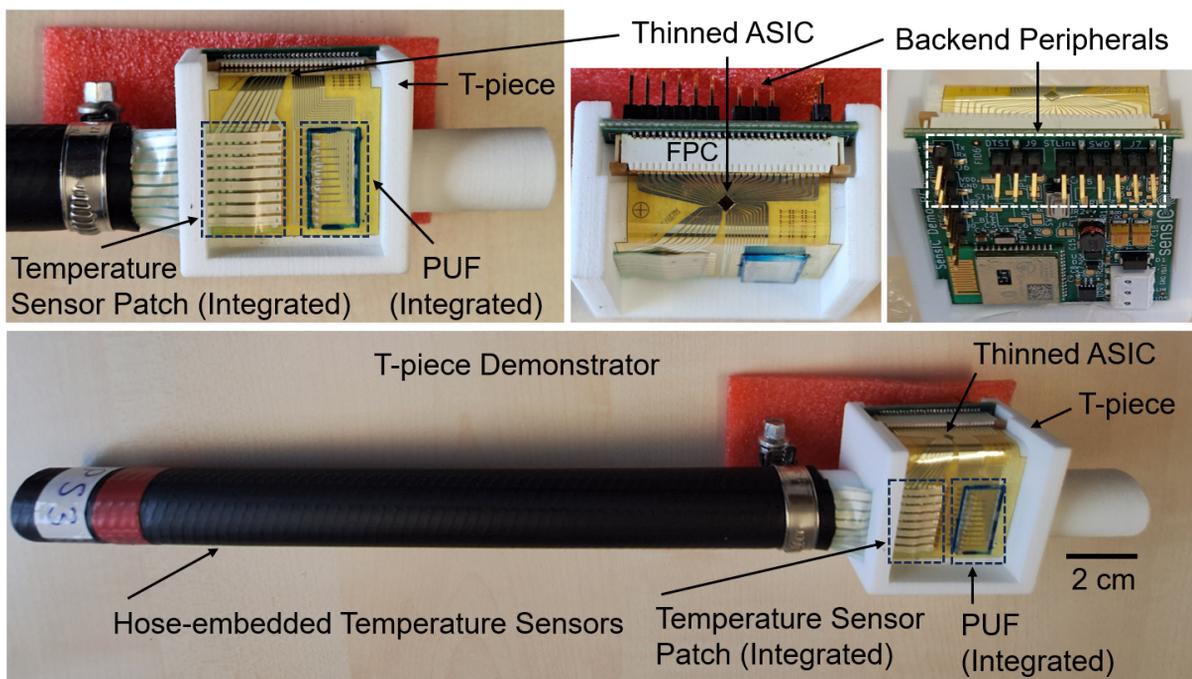


Figure 6.4: Full hybrid system-in-foil assembled into the T-piece module.

Top left: Front side of the T-piece cavity showing the ASIC-in-foil together with the integrated printed PUF and the hose-embedded temperature sensor interface. Top center: ASIC-in-foil mounted laterally within the T-piece cavity with backend interfacing through an FPC connector. Top right: Backside of the T-piece with the backend peripheral PCB connected to the foil interface. Bottom: Full hybrid system-in-foil T-piece assembly including hose, integrated devices, and backend electronics. *Reproduced with permission from^[82], © IEEE 2025.*

The T-piece serves as a mechanically robust carrier that co-locates the ASIC-in-foil, the printed PUF, the hose-embedded temperature sensors, and backend peripherals within a single module, while providing defined mechanical housing for the system components. The front side of the T-piece cavity accommodates the printed elements and the ASIC-in-foil interface. The printed PUF, integrated

on the foil, is positioned within the front cavity and aligned with the predefined foil pads, allowing direct electrical connection to the ASIC-in-foil interface with minimal interconnect length. The coolant hose passes axially through the T-piece, maintaining an uninterrupted fluid path through the module. The outer stretchable interconnect of the hose-embedded temperature sensor is routed through a dedicated lateral opening into the T-piece cavity, enabling direct integration into the foil interface without imposing mechanical strain on the sensor. The ASIC-in-foil is placed laterally inside the T-piece cavity and mechanically constrained to prevent displacement during handling and hose mounting. This placement ensures direct electrical paths to both the printed PUF and the temperature sensor interfaces. The rear side of the T-piece hosts the backend peripherals printed circuit board (PCB), which provides power supply, control, and communication access to the ASIC-in-foil via the FPC connector. This arrangement separates the printed frontend elements from the backend readout circuitry while maintaining direct electrical access. Overall, the T-piece assembly enables a mechanically robust integration of printed sensing, identification, and silicon-based readout electronics under realistic automotive system, while maintaining modularity and accessibility for system-level evaluation.

6.3 Hybrid System-in-Foil Readout and Security Operation

This section evaluates the system-level electrical operation and ASIC-based readout of the hose-embedded temperature sensors and PUF integrated into hybrid system-in-foil. Furthermore, a system-level security framework is presented to illustrate the application relevance of the hybrid system-in-foil for secure identification and communication in automotive-oriented security framework. All measurements are acquired by triggering the ASIC via the backend peripheral microcontroller, enabling accesses to the digital temperature readings, PUF responses, and security-relevant data for system-level evaluation (**Figure 6.7**). Details of the power supply information is provided in **Appendix A.2**.

6.3.1 System-Level Temperature Response

Two hose-embedded temperature sensors were implemented as redundant sensing elements to ensure robust system-level operation following full hybrid system-in-foil assembly into the T-piece module. Of the two hose-embedded sensors, one temperature-sensing channel remained fully functional and was therefore used for subsequent system-level evaluation, whereas the second channel did not exhibit a temperature-dependent response. This behavior is attributed to hybrid system-in-foil integration related effects, including ASIC thinning, foil embedding, mechanical handling, and subsequent T-piece assembly, which together adversely affected the sensitive analog front-end of the ASIC temperature readout circuitry. The observed partial channel failure underscores the importance of redundant sensor integration for ensuring robust operation of hybrid system-in-foil architecture. The system-level response of the functional sensing channel (#2), measured using the ASIC-based readout over a reference temperature range from 30 °C to 90 °C covering the relevant operating range for automotive-relevant environment, is shown in **Figure 6.5**.

A predominantly linear temperature response is observed over the investigated temperature range, confirming system-level functionality of the hose-embedded sensor integrated in hybrid system-in-foil architecture. One pronounced outlier occurs at 40 °C, where a relative error of approximately 15 % is observed between the reference and the measured temperature values. This deviation is likely associated with system-level measurement conditions, including incomplete temperature stabilization, local thermal gradients within the hybrid system, and integration-related effects influencing the sensitivity of the ASIC based temperature readout circuitry. Excluding this single data point, the maximum relative error remains below 4 %, decreasing further at elevated temperatures above 50 °C. For the remaining measurement points, the relative error lies between -1% and 0.7% , demonstrating stable temperature readout in the fully integrated hybrid system-in-foil. Overall, the results demonstrate system-level readout of hose-embedded temperature sensors integrated in hybrid system-in-foil architecture for automotive applications. The predominantly linear temperature response indicates functional

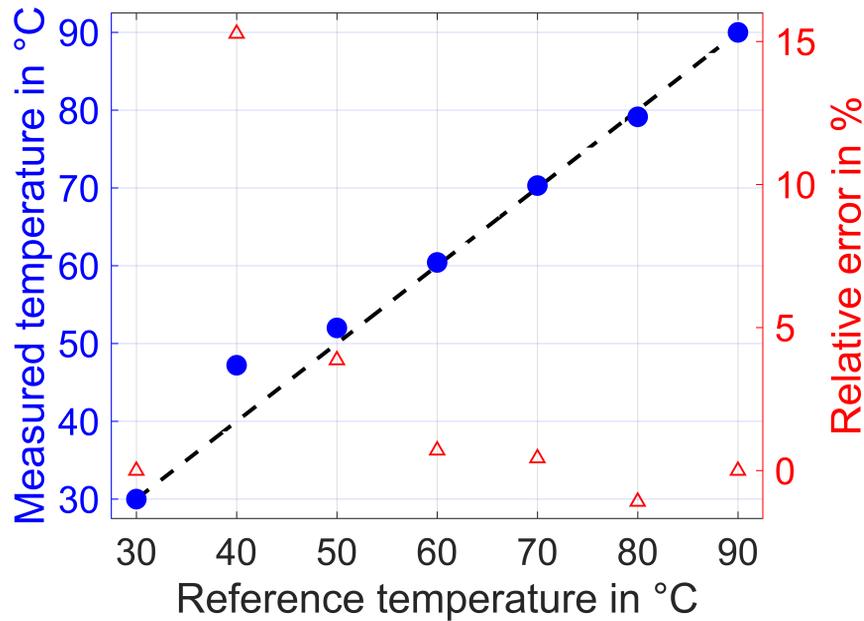


Figure 6.5: System-level temperature response of the hose-embedded sensors integrated in hybrid system-in-foil. Measured temperature values obtained via the ASIC temperature readout channel #2 (blue markers) compared to reference temperature (dashed black line). Relative error between the measured and reference temperature is shown as red triangles on the secondary axis. *Adapted from^[82], © IEEE 2025.*

integration, while an isolated outlier and single-channel failure points to system-level effects such as thermal gradients and mechanical integration effects within the assembled T-piece module, highlighting the importance of robust interconnect design and calibration strategies in future automotive implementations.

6.3.2 System-Level PUF Evaluation and Stability Analysis

The system-level identification capability is evaluated after hybrid system-in-foil integration of the printed inverter array based PUF. System-level measurements reveal distinct inverter-to-inverter variations in the output characteristics, which enable PUF response generation through pairwise comparison of the inverter output voltages. During system-level evaluation, the inverter input voltage is defined by the on-chip digital-to-analog converter (DAC), while inverter output pairs are sequentially selected using the address signals a_k and b_k . For each

selected inverter pair, the corresponding output voltages are routed through on-chip multiplexers to a comparator, which converts their relative voltage difference into a binary PUF sub-response bit. In parallel, the inverter output voltages present at the comparator inputs are recorded using the backend microcontroller's analog-to-digital converters (ADCs) for analysis and visualization.

The inverter transfer characteristics were recorded over an input voltage range from 90 mV to 1.35 V at three operating temperatures $T = \{25, 45, 65\}^\circ\text{C}$, representing an automotive-relevant sensing range. The resulting inverter output voltages and corresponding spatial heat maps are shown in **Figure 6.6**. The transfer curves (**Figure 6.6 a–c**) represent the inverter output voltage V_{out} as a function of the input voltage V_{in} . The observed variation between individual transfer curves, which is significantly larger than the short-term fluctuations, is attributed to inherent inverter-to-inverter variability and constitutes the analog entropy source of the PUF. The inverter output voltage saturates at approximately $V_{\text{out}} \approx 0.5\text{ V}$, arising from residual channel resistance of the EGT and voltage drop along the ground line interconnect of the inverter-array at system-level. The achieved inverter output voltage range is sufficient for PUF operation as the response generation depends on relative differences between inverter output voltages rather than rail-to-rail voltage levels. In contrast, the heat maps (**Figure 6.6 d–f**) visualize the spatial distribution of inverter output voltages at a fixed $V_{\text{in}} = 0.63\text{ V}$, providing discrete snapshots of inverter-to-inverter variability at operating points relevant for PUF response generation. Each heat-map column corresponds to one temperature condition, while each colored cell represents the output voltage of a specific inverter at its physical position within the inverter-array PUF.

PUF stability is evaluated by repeating the complete PUF response generation procedure 1000 times at an input voltage of 0.63 V, selected as a representative operating point within the inverter transition region where device-to-device variability is most pronounced. The bit error rate was calculated using **Equation 2.11** to quantitatively evaluate the reliability of the PUF responses. At 25°C , a bit error rate of 0.0084 % is obtained, with almost no observed bit flips. At 45°C and 65°C , no bit flips are observed across all repetitions, confirming robust intra-temperature stability of the PUF responses

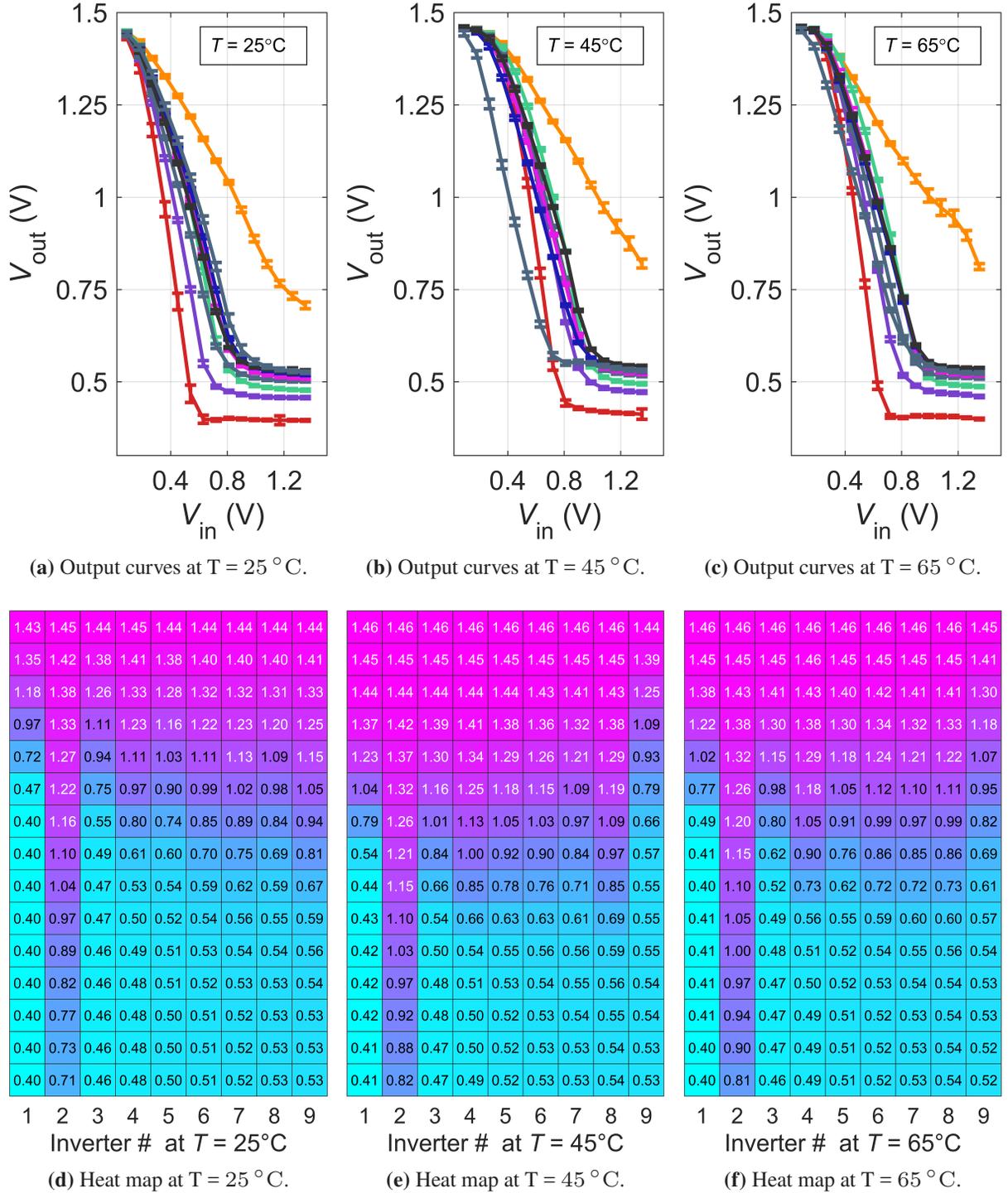


Figure 6.6: System-level inverter-array PUF readout of the hybrid system-in-foil.

(a–c) Inverter output curves at 25°C , 45°C , and 65°C , showing V_{out} as a function of DAC-defined V_{in} , with error bars indicating standard deviation. (d–f) Corresponding heat maps visualizing the spatial distribution of inverter V_{out} across the PUF at $V_{\text{in}} = 0.63\text{ V}$, corresponding to an operating region dominated by inverter-to-inverter variability. The color scale (cyan - low values, purple - high values) highlights these variability and the data represent median values over 1000 repetitions. Adapted from^[82], © IEEE 2025.

under varying thermal conditions. While the absolute PUF responses differs across $T = \{25, 45, 65\}^{\circ}\text{C}$ due to temperature-induced shifts in inverter output characteristics, the responses remain stable within each temperature point, confirming reliable system-level identification. A representative 36-bit PUF identifier, for example $R_{36} = 1111111100000001111110111111111101011$ is extracted at 25°C and demonstrates the successful generation of a unique and repeatable system-level response after full hybrid system-in-foil demonstration. Overall, the integrated PUF core and the thinned ASIC readout circuitry embedded in foil demonstrate reliable system-level operation. Temperature-dependent shift in the inverter transfer characteristics remain an open challenge and will require dedicated compensation strategies in future, to ensure stable PUF operation over the targeted temperature range.

6.3.3 System-Level Security Operation

To demonstrate system-level feasibility beyond sensing and device-level identification, the T-piece system demonstrator is evaluated within an automotive-oriented security framework. The security concept is included for system-level completeness and illustrates how the integrated PUF and temperature sensor interface with a realistic secure communication architecture, without relying on stored static cryptographic keys. An overview of the automotive system configuration and communication interfaces, in which the T-piece system demonstrator acts as a secure peripheral connected to an automotive host, is shown in **Figure 6.7**.

The T-piece system demonstrator incorporates a hybrid system-in-foil, which interfaces the printed PUF and the hose-embedded temperature sensor within a mechanically compliant foil assembly. A backend microcontroller (MCU) coordinates overall system operation by triggering ASIC readout sequences, acquiring digital PUF responses and temperature data, and managing secure communication with the automotive ECU.

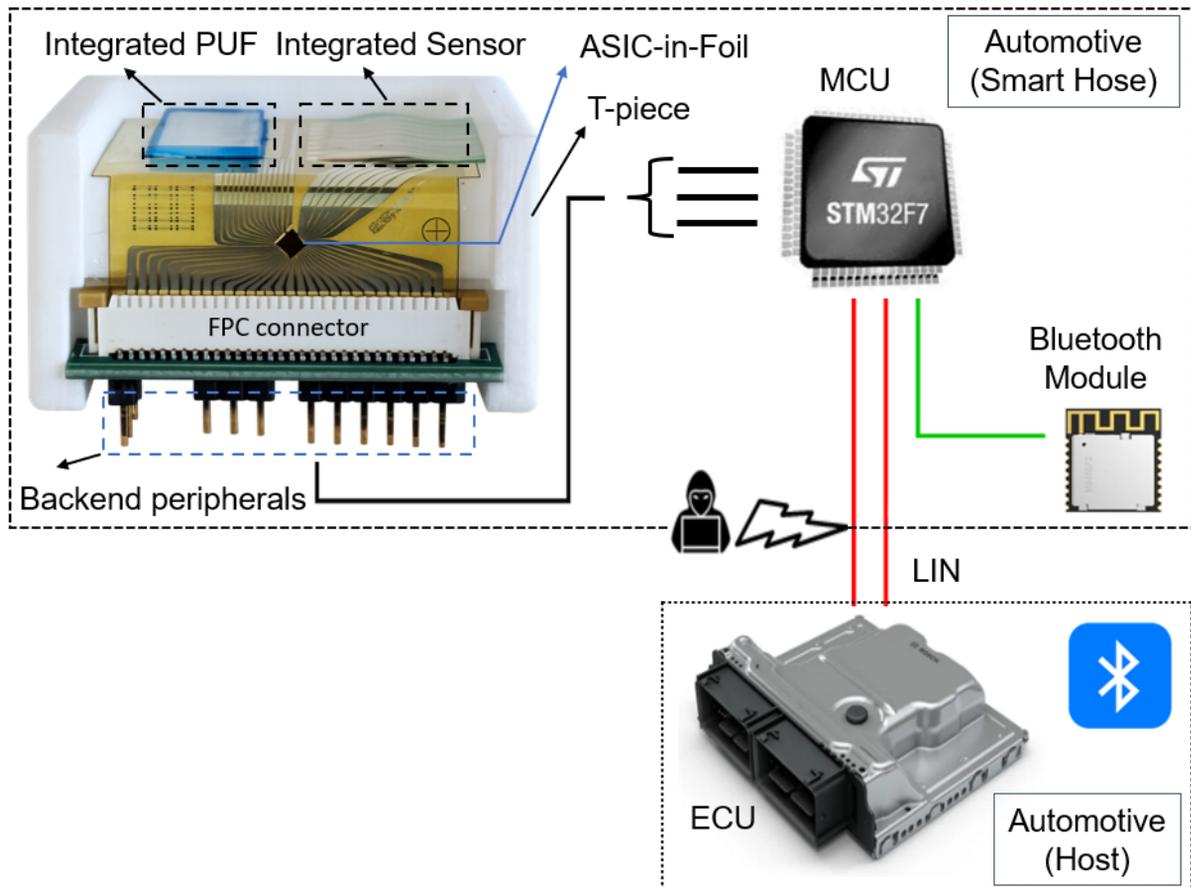


Figure 6.7: Automotive system-level security configuration illustrating the interaction between the smart hose T-piece module and the automotive host ECU. The smart hose T-piece module incorporates hybrid system-in-foil, connected to a microcontroller by backend peripherals. The microcontroller coordinates ASIC readout and manages external communication. Bluetooth enables proximity-based session initialization, while LIN provides communication interface between automotive host and smart hose T-piece module.

Two communication interfaces are employed with complementary roles. Bluetooth Low Energy (BLE) is used for proximity-based session initialization and secure pairing, while the Local Interconnect Network (LIN) provides an automotive-compatible communication interface. Following system-level validation, the T-piece system demonstrator is hereafter referred to as the smart hose T-piece module.

6.3.3.1 BLE-Based Shared Secret Key Generation

Bluetooth Low Energy (BLE) communication is employed during system initialization to verify physical proximity between the automotive smart hose T piece module and the automotive ECU. The corresponding processing flow is illustrated in **Figure 6.8**.

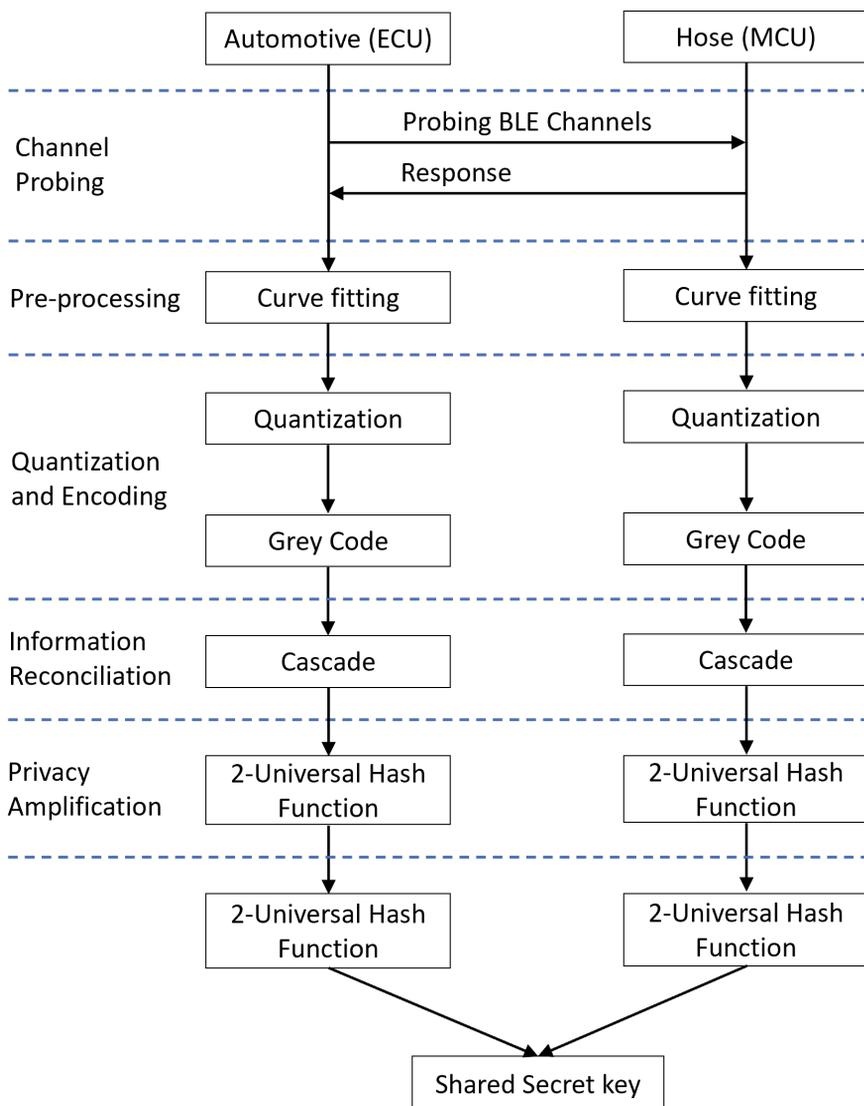


Figure 6.8: Shared secret key generation workflow based on BLE RSSI measurements.

Generation of a shared secret key between the smart hose T-piece module and the automotive host based on correlated RSSI measurements acquired during BLE communication. The extracted RSSI values are processed by curve fitting, quantization, Grey coding, information reconciliation, and privacy amplification using universal hashing to obtain a 256-bit shared secret key.

During initialization, both devices exchange random probe packets and independently measure the received signal strength indicator (RSSI) of the BLE channel. Due to channel reciprocity and close physical proximity, both endpoints observe highly correlated RSSI variations, while an external observer at a different location cannot reproduce the same measurements. The measured RSSI sequences are locally pre-processed and quantized at both endpoints. Gray-code encoding is applied to reduce bit mismatches caused by small RSSI fluctuations. Based on the chosen quantization resolution and the number of statistically usable channel samples obtained during the probing phase, each side independently extracts an initial 62-bit raw key sequence. This sequence represents shared channel-derived entropy and is generated without transmitting any secret information.

Due to measurement noise, the extracted bit sequences are similar but not identical. To correct residual mismatches, information reconciliation is performed using the Cascade protocol that employs parity checks. Only parity information is exchanged during this process, while raw key bits remain undisclosed. Any information potentially leaked during reconciliation is explicitly addressed in the subsequent processing stage. To remove residual leakage and strengthen the key, privacy amplification is applied symmetrically at both endpoints using two successive universal hash functions. The first hash suppresses information revealed during reconciliation, while the second uniformly randomizes the remaining entropy and maps the reconciled sequence to a cryptographically suitable length. Through this process, the reconciled 62-bit input is transformed into a synchronized 256-bit shared secret key (e.g., $K_{256} = 1010010011010110010\dots\dots0100101110101$) at both end points, which is never transmitted and not-stored permanently. The resulting 256-bit secret key is private, session-based, refreshable, used exclusively to secure the automotive communication channel.

Following secure channel establishment, LIN communication is enabled between the smart hose T-piece module and the automotive host ECU. During initial system verification, the backend microcontroller of the smart hose T-piece module reads the PUF response from the ASIC and, upon host request, transmits the derived identifier over the LIN bus, enabling the automotive host to recognize the physical hardware instance associated with the established communication session. After

successful hardware verification, the backend microcontroller continues to acquire and transmit temperature sensor data from the ASIC over the LIN interface during normal operation.

Scope of Contribution and Attribution

The security concept presented in this section, including BLE-based session establishment, cryptographic processing, and shared secret key generation was developed by the Institute of Reliable Embedded Systems and Communication Electronics at Hochschule Offenburg within the collaborative project. This thesis contributes the development and hybrid system-in-foil integration of the printed PUF and hose-embedded temperature sensor (T-piece demonstrator), together with their system-level ASIC-based readout, as part of the automotive-relevant security framework.

6.4 Summary

This chapter demonstrated the system-level feasibility of integrating printed identification and sensing elements with a foil-embedded thinned ASIC using a hybrid system-in-foil architecture, followed by evaluation within a T-piece module assembly for an automotive-oriented security framework. A custom 180 nm CMOS bare die ASIC was backside-thinned from 230 μm to approximately 30 μm and embedded into a polyimide foil, enabling short interconnect paths, flexible handling, and stable electrical interfacing to printed frontend elements. The foil-embedded ASIC was integrated, together with the printed PUF and temperature sensor, to realize a hybrid system-in-foil assembled into a T-piece module. The ASIC provided stable biasing, reliable addressing, digitization, and system-level access for both the printed devices.

System-level readout of the temperature sensor showed a predominantly linear response over 30 °C to 90 °C, with a single outlier observed at 40 °C. For all remaining measurement points, the relative error remained below 4 %, confirming reliable temperature sensing after full mechanical assembly. System-level PUF

evaluation yielded a 36-bit response based on relative voltage comparison of printed inverter outputs. Stability analysis over 1000 repeated readouts resulted in a bit error rate of 0.0084 % at 25 °C, with no bit flips observed at 45 °C and 65 °C, demonstrating reproducible identification within fixed temperature conditions. In addition, the hybrid system-in-foil was shown to be compatible with the security framework, in which RSSI-based communication channel entropy measurements between the smart hose T-piece module and automotive host ECU are used to derive a 256-bit shared secret key for secure communication. This security concept is included to demonstrate system-level compatibility and integration capability, while the design and implementation of the cryptographic mechanisms remain outside the scope of this thesis. Overall, the results validates the hybrid system-in-foil architecture as an effective strategy for bridging printed electronics and foil-embedded thinned ASICs, enabling system-level temperature sensing, PUF-based identification, and compatibility with automotive-oriented security framework.

7 Conclusion and Outlook

7.1 Conclusion

This thesis demonstrated the systematic development and integration of printed electronic devices with a foil-embedded custom ASIC into a hybrid system-in-foil architecture, assembled within a mechanically robust T-piece module for automotive systems. Through a structured progression from low-voltage printed device fabrication, to circuit-level utilization, and finally to system-level electrical interfacing enabled by a backside-thinned and foil-embedded ASIC, the thesis illustrates how printed devices can be transitioned from standalone components to system-level accessible functional modules.

At the device level, two complementary EGT architectures were developed, reflecting a clear progression toward system-level applicability. First, hybrid-printed EGTs on glass substrates, based on laser-ablated ITO electrodes combined with printed functional layers, enabled stable operation below 1 V with improved device uniformity. This architecture supported reliable circuit realization and served as the technological basis for the successful implementation of PUF circuits. Second, fully-printed EGTs on glass and polyimide substrates, employing aerosol jet printed gold electrodes and inkjet printed indium oxide semiconductor as well as composite solid polymer electrolyte layers, demonstrated sub-1 V operation. Additional investigations on polyimide substrates highlighted process transferability, substrate-dependent electrical behavior, and mechanical compliance, thereby validating the scalability of the fabrication approach toward fully printed circuit implementations.

At the circuit level, an inverter-array based on EGTs with resistive pull-up loads was implemented and utilized as a hardware-security PUF. The inverter array exploits intrinsic device-to-device variability of printed EGTs as a source of analog entropy, which is converted into digital responses through their relative output voltage comparison. This approach enabled the generation of stable 36-bit PUF identifiers, demonstrating that low-voltage EGT-based circuits can serve as viable security primitives without relying on complex digital circuitry. In particular, stable PUF operation is achieved when the inverter array is operated within the transition region ($V_{in} \approx 0.5\text{--}0.7\text{ V}$), where intrinsic device-to-device variability is maximized while maintaining low supply current and negligible gate leakage. This operating regime therefore enables energy-efficient hardware security. In parallel, inkjet printed platinum-based *Pt100* and *Pt1000* resistive temperature sensors demonstrated stable and predominantly linear resistance–temperature characteristics over the range from $20\text{ }^{\circ}\text{C}$ to $80\text{ }^{\circ}\text{C}$, corresponding to automotive-relevant operating range targeted in this thesis. Based on this performance, the *Pt1000* sensor was selected for hybrid system-in-foil integration, as its higher nominal resistance results in a larger resistance change per degree Celsius, reducing the influence of interconnect resistances and ensuring compatibility with the ASIC-based readout interface, thereby confirming its suitability for automotive and industrial applications.

At the system level, the printed PUF and temperature sensors were integrated with a custom 180 nm CMOS ASIC, backside-thinned down to approximately $30\text{ }\mu\text{m}$ and embedded in flexible polyimide foil, to realize the hybrid system-in-foil architecture. The ASIC provided stable biasing, relative comparison, and digitization of the analog signals from printed devices, enabling reliable readout after hybrid system-in-foil was assembled into an automotive-relevant T-piece module. System-level evaluation confirmed a stable 36-bit PUF response with no significant bit flipping over 1000 repeated readouts under fixed operating conditions, demonstrating reproducible identification after full hybrid system-in-foil integration. Temperature sensing at system-level exhibited predominantly linear behavior across the investigated range, with an outlier observed at lower temperature point, attributed to system-level influences introduced by mechanical

integration and sensitivity of the *Pt1000* to integration-related effects. Finally, the hybrid system-in-foil was evaluated within an automotive-oriented security framework, in which RSSI-based channel entropy measurements were used to establish a shared 256-bit session key between the smart hose T-piece module and the automotive host ECU. This mechanism enables secure communication without storing static cryptographic keys and links the established communication session to the physical hardware via the PUF-derived identifier and authenticated transmission of temperature sensor data.

Overall, this thesis establishes hybrid system-in-foil architecture integrating printed devices with a foil-embedded custom ASIC, forming a unified architecture that enables reliable system-level access to temperature sensing, PUF-based identification, and compatibility with automotive security frameworks after integration into an automotive-compatible T-piece module.

7.2 Outlook

The long-term vision of this thesis is the realization of fully-printed hardware-security primitives, specifically PUFs and ring oscillator circuits, based on EGTs on flexible substrates. Fully-printed implementations are particularly attractive for conformal and embedded applications, where mechanical compliance, low-voltage operation, and additive manufacturing are essential requirements. While this thesis demonstrates a complete and coherent pathway from printed devices to hybrid system-in-foil integration, several challenges and opportunities remain for future research, especially toward fully-printed and large-area flexible electronics realizations.

At the device level, future work should focus on improving the stability and reproducibility of fully-printed EGTs on polyimide substrates. Electrolyte gated operation inherently introduces device-to-device variability, hysteresis, bias-stress effects, and long-term drift, which may become more pronounced under mechanical deformation. Addressing these limitations will require optimized electrolyte

formulations, improved encapsulation strategies, and tighter control over semiconductor conversion and densification processes for solution-processed indium oxide channels. In addition, refinement of electrode geometries and interconnect layouts is expected to reduce parasitic effects and improve device uniformity in flexible implementations.

At the circuit level, the development of variability-tolerant and yield-optimized design methodologies is essential. For EGT-based inverter array PUFs, future studies should identify operating regimes and readout strategies that maximize response separability while maintaining robustness against temperature variations, aging, and supply voltage fluctuations. Beyond PUFs, fully-printed EGT-based ring oscillators represent a natural extension of the gold electrode based flexible EGTs demonstrated in this thesis. Ring oscillators are particularly well suited for fully-printed circuits, as they rely on relative delay variations rather than absolute voltage levels, making them inherently tolerant to device variability.

At the system level, the demonstrated hybrid system-in-foil integration provides a practical and scalable pathway for deploying flexible printed security primitives in real applications. The combination of flexible printed PUFs with foil-embedded ASICs enables robust readout, digitization, and system integration within realistic automotive systems. While fully-printed systems remain a long-term objective, hybrid system-in-foil architecture allows system-level compensation of residual device and circuit non-idealities through stable readout and configurable evaluation strategies. Future work may extend foil-level architectures and interconnect concepts to support larger security primitives and increased system complexity.

Overall, future research should pursue a co-design strategy across materials, devices, circuits, and systems, enabling a gradual transition from hybrid system-in-foil implementations toward fully-printed, flexible, and intrinsically secure electronic systems. The concepts established in this thesis provide a solid foundation for this progression, particularly for automotive and industrial applications requiring lightweight integration, mechanical compliance, and intrinsic hardware security.

A Appendix

A.1 ASIC Functional Blocks for System Operation

The ASIC integrates functional blocks for temperature sensor readout, PUF addressing and evaluation, and digital system interfacing for data access. These blocks are described conceptually below, guided by the schematic representations in **Figures A.1 and A.2**, while transistor-level detail remain out of the scope of this thesis.

Resistive Sensor Readout Block

The ASIC provides two identical readout channels for resistive sensor elements (**Figure 6.2**). The block-level operating principle is illustrated in **Figure A.1**. Each channel forces a defined reference current through an external resistive element and senses the resulting voltage drop. This voltage is amplified and compared against a time-dependent reference voltage generated internally by charging a capacitor with a controlled ramp current. A comparator detects the instant at which the ramp voltage equals the amplified sensor voltage. The time required for the reference ramp to reach the sensed voltage is captured by an on-chip counter, producing a digital counter value that represents the resistance of the connected sensor element. This resistance-to-time conversion avoids direct high-resolution voltage digitization at the interface and is inherently robust against series resistance introduced by foil interconnects. The counter value constitutes the primary digital output of the sensor readout block.

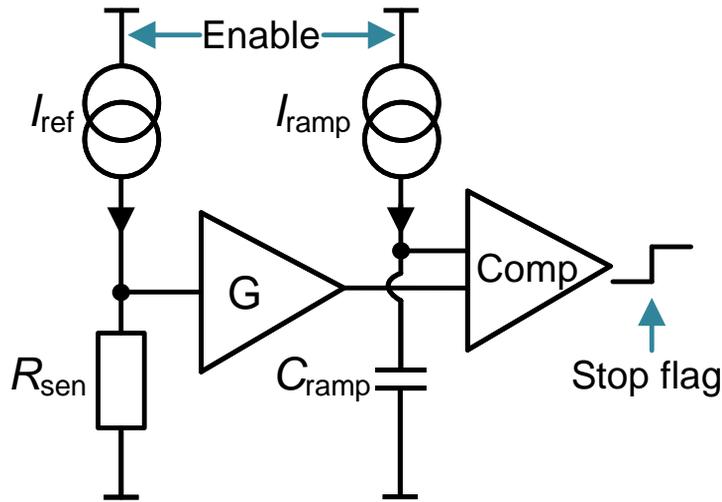


Figure A.1: Block-level schematic of the ASIC resistive sensor readout circuit. A current-driven voltage sensing path combined with a ramp-based time measurement produces a digital counter output proportional to resistance. Adapted from^[82], © IEEE 2025.

PUF Addressing and Readout Logic

For PUF operation, the ASIC implements a pairwise comparison-based readout architecture, as shown in **Figure A.2**. Multiple external analog node voltages are accepted by the ASIC and buffered by on-chip operational amplifiers internally to decouple the external circuitry from the readout logic.

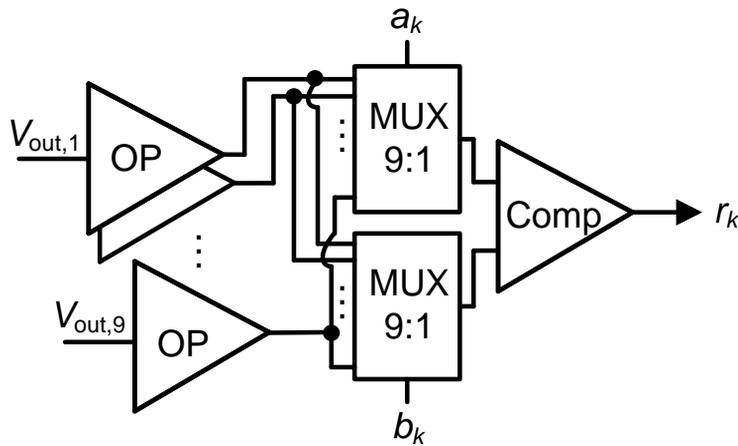


Figure A.2: Block-level schematic of the ASIC PUF addressing and readout logic. Buffered external node voltages are selected by multiplexers addressed by a_k and b_k and compared pairwise to generate digital PUF response bits. Adapted from^[82], © IEEE 2025.

Two analog multiplexers select a pair of buffered voltages according to digital address signals a_k and b_k . The selected voltages are applied to a comparator, which generates a digital output bit r_k based on their relative magnitude. Each address pair (a_k, b_k) therefore defines a PUF sub-challenge, and the comparator output represents the corresponding sub-response. The ASIC provides on-chip supply and input voltage to bias the external circuitry at a defined operating point. By sequentially configuring the address pairs and triggering the comparison, the ASIC enables systematic generation of challenge–response pairs (CRPs).

ASIC Digital Interface and System-Level Capability

The ASIC is configured and read out via SPI and GPIO interfaces, which enable external system components to configure temperature sensor readout, select PUF addresses, trigger measurement sequences, and retrieve digitally encoded output data. The ASIC provides digitally accessible physical data derived from the printed temperature sensor and the printed inverter-based PUF, which can be utilized at system level for sensing, identification, and security-relevant functionality. During system operation in this thesis, the ASIC is electrically supplied, configured, and read out by backend electronics interfaced through the defined SPI and GPIO signals, with a compact custom interfacing PCB providing the regulated supply and the FPC connection to the ASIC-in-foil. Detailed descriptions of ASIC port counts, backend hardware implementation, communication stacks, and external interfaces are beyond the scope of this section and are addressed only where required for system-level demonstration.

A.2 ASIC Power Supply and Consumption

The custom ASIC operates at a supply voltage of 3.3 V. The ASIC integrates internal low-dropout (LDO) regulators to generate dedicated internal supply rails. In particular, the digital core and selected analog blocks are supplied at 1.8 V, while a dedicated on-chip LDO provides a regulated supply of 1.5 V for the printed PUF core. For biasing of the printed inverter array based PUF, the ASIC incorporates

an on-chip digital-to-analog converter (DAC) that generates an adjustable inverter input voltage in the range of 0.2 V to 1.5 V. During hybrid system operation, the printed inverter-based PUF exhibits a power consumption of approximately 450 μW , while the ASIC power consumption during combined temperature sensor and PUF readout is approximately 26.4 mW.

The focus of this thesis remained on the functional realization of the hybrid system-in-foil architecture and reliable system-level readout, rather than on power supply optimization. Detailed aspects of the backend power-supply implementation are therefore out of the scope of this thesis, are not discussed, and are not referenced further.

A.3 Hybrid System-in-Foil Workflow

This section summarizes the workflow used to realize the hybrid system-in-foil architecture demonstrated in this thesis. The overview clarifies the sequence of fabrication, integration, and validation steps and distinguishes the contributions carried out within this thesis from externally provided components and processes. The contributions of the collaborative partners and the associated structured workflow are summarized in **Table A.1**.

Table A.1: Hybrid system-in-foil integration workflow, showing the sequence of process steps and the corresponding responsibilities attributed to this thesis and external contributors.

Step	Contributions	Responsibility
1	Foil system architecture and interface design	This thesis
2	Custom bare die ASIC (TSMC 180-nm CMOS)	AnSem GmbH
3	ASIC backside thinning and in foil-embedding	IMS Chips
4	Fabrication of PUF and Temperature sensor	This Thesis
5	Integration of PUF into foil-embedded ASIC	KIT / IAI Institute
6	Sensor interfacing using stretchable interconnects for hose-embedding and integration with foil-embedded ASIC	Leibniz INM / Continental AG
7	T-piece module design and 3D printing	Continental AG
8	T-piece assembly of hybrid system-in-foil	This Thesis
9	System-level readout of PUF and sensor	This Thesis
10	Automotive-oriented security demonstration	Hochschule Of-fenburg

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Acronyms and Symbols

Acronyms

ASIC	Application-Specific Integrated Circuit
CMOS	Complementary Metal–Oxide–Semiconductor
TSMC	Taiwan Semiconductor Manufacturing Company
EGT	Electrolyte-Gated Transistor
PUF	Physically Unclonable Function
AJP	Aerosol Jet Printing
IJP	Inkjet Printing
CIJ	Continuous Inkjet
DoD	Drop-on-Demand
RTS	Resistive Temperature Sensor
TCR	Temperature Coefficient of Resistance
TFT	Thin-Film Transistor
EDL	Electric Double Layer
VTC	Voltage Transfer Characteristic
BER	Bit Error Rate

BLE	Bluetooth Low Energy
RSSI	Received Signal Strength Indicator
HD	Hamming Distance
PCB	Printed Circuit Board
AFM	Atomic Force Microscopy
SEM	Scanning Electron Microscopy
TEM	Transmission Electron Microscopy
TGA	Thermogravimetric Analysis

Symbols and Variables

V_T	Threshold voltage
S_S	Subthreshold swing
I_{ON}	On-state current
I_{OFF}	Off-state current
I_G	Gate leakage current
I_{DS}	Drain current
V_{DS}	Drain voltage
V_{GS}	Gate voltage
W	Channel width
L	Channel length / response length
C_G	Gate Capacitance
R_D	Pull-up resistor

C	Challenge input (PUF)
N	Number of inverters
Q	Channel charge density
R_{36}	PUF response
K_{256}	Session key
V_{DD}	Voltage supply rail
V_{in}	Input voltage
V_{out}	Output voltage
GND	Circuit ground
T	Temperature
T_0	Reference temperature
T_{max}	Maximum temperature
$R(T)$	Resistance at temperature T
R_0	Resistance at reference temperature
S	Sensitivity
t	Film thickness
R_S	Sheet resistance
Re	Reynolds number
We	Weber number
Oh	Ohnesorge number
Z	Inverse Ohnesorge number

Greek Symbols and Variables

λ	Wavelength
α	Temperature coefficient of resistance
μ	Field-effect mobility
σ	Standard deviation
σ_{el}	Electrical conductivity
ρ	Electrical resistivity

Operators and Math Symbols

\approx	Approximately equal
\leq	Less than or equal to
\geq	Greater than or equal to
\oplus	XOR operation

General Indices

i, j	Inverter index
n	PUF instance index
w	Measurement repetition index
ref	Reference value
Rh	Relative humidity
High-k	High-permittivity

I–V	Current–voltage characteristics
R–T	Resistance–temperature characteristics

Units

Ω	Ohm
A	Ampere
V	Volt
μm	Micrometer
nm	Nanometer
Ω/\square	Ohms per square
S m^{-1}	Siemens per meter
$^{\circ}\text{C}$	Degree Celsius
cm^{-2}	Per square centimeter
cP	Centipoise
kDa	Kilodalton
wt. %	Weight percent
mL	Milliliter
mPa s	Millipascal second
mN m^{-1}	Millinewton per meter
$\mu\text{F cm}^{-2}$	Microfarad per square centimeter
$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$	Square centimeter per volt per second

Materials and Chemical Compounds

Ag	Silver
Au	Gold
Pt	Platinum
Cu	Copper
Ni	Nickel
ZnO	Zinc oxide
IGZO	Indium gallium zinc oxide
ITO	Indium tin oxide
$\text{In}(\text{NO}_3)_3 \cdot x\text{H}_2\text{O}$	Indium nitrate hydrate
In_2O_3	Indium oxide
SiO_2	Silicon dioxide
SnO_2	Tin oxide
HfO_2	Hafnium oxide
Al_2O_3	Aluminum oxide
LiClO_4	Lithium perchlorate
DMSO	Dimethyl sulfoxide
PC	Propylene carbonate
PVA	Poly(vinyl alcohol)
CSPE	Composite solid polymer electrolyte
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene):polystyrene sulfonate

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List of Publications

Journal Articles

- [1] **S. Alam**, T. Kister, A. Scholz, S. Sauva, M. Lay, T. Kraus, and J. Aghassi-Hagmann, “An inkjet-printed platinum-based temperature sensing element on polyimide substrates,” *Advanced Engineering Materials*, p. e202501740, 2026.
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- [3] A. Scholz, **S. Alam**, W. Hadrich, A. Schröder, T. Wolfer, M. Friedrich, T. Kister, M. Lay, S. Sauva, U. Passlack, M. Campana, L. Koker, A. Sikora, T. Kraus, and J. Aghassi-Hagmann, “Hybrid system in foil containing secure identification and temperature sensing units,” *IEEE Journal on Flexible Electronics*, vol. 4, no. 6, pp. 242–250, 2025.
- [4] **S. Alam**, X. Wang, M. K. Saghafi, G. C. Marques, A. T. Neffe, F. M. Toma, and J. Aghassi-Hagmann, “Electrolyte-gated indium oxide based transistor on pet substrate enabled by hybrid process,” in *2024 IEEE International Flexible Electronics Technology Conference (IFETC)*, 2024, pp. 1–3.

Conference Contributions

Oral Presentation

- [1] **2024 Tage der vertrauenswürdigen Elektronik**, Munich, Germany
“Tamper-proof cryptographic keys generation for identification and authentication”

Poster

- [1] **2024 IEEE International Flexible Electronics Technology Conference (IFETC)**, Bologna, Italy
“Electrolyte-gated indium oxide based transistor on PET substrate enabled by hybrid process”

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ALD Process Development for Multilayer HfO₂/SiO₂ films

Scientific Publications

Ph.D. Publications

- The complete list of PhD publications is provided in the **List of Publications** section of this dissertation.

M.Sc. Publications

- **S. Alam**, P. Paul, V. Beladiya, P. Schmitt, O. Stenzel, M. Trost, S. Wilbrandt, C. Mühlig, S. Schröder, and G. Matthäus, “Heterostructure Films of SiO₂ and HfO₂ for High-Power Laser Optics Prepared by Plasma-Enhanced Atomic Layer Deposition,” *Coatings*, vol. 13, no. 2, pp. 278–288, 2023.

B.Sc. Publications

- N. S. Ashraf, **S. Alam**, and M. Alam, *New Prospects of Integrating Low Substrate Temperatures with Scaling–Sustained Device Architectural Innovation*, Springer Cham., Switzerland, 2016.

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C Declaration

I, Shawon Alam, hereby declare that this thesis has been independently composed by myself and that the work presented herein is original, except where explicit reference is made to the work of others. This thesis has not been submitted, in whole or in part, for any other degree or professional qualification at this or any other institution.

All sources of information and data have been properly acknowledged, and contributions from collaborators and project partners are clearly stated in the relevant chapters. Parts of this thesis are based on previously published journal and conference papers authored or co-authored by me, which are appropriately referenced. This thesis was prepared in compliance with the rules of good scientific practice and the doctoral regulations of the Karlsruhe Institute of Technology (KIT).