









## On-chip stencil lithography for superconducting qubits

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## ABSTRACT

Improvements in circuit design and, more recently, in materials and surface cleaning have contributed to a rapid development of coherent superconducting qubits. However, organic resists commonly used for shadow evaporation of Josephson junctions (JJs) pose limitations due to residual contamination, poor thermal stability, and compatibility under typical surface-cleaning conditions. To provide an alternative, we developed an inorganic SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> on-chip stencil lithography mask for JJ fabrication. The stencil mask is resilient to aggressive cleaning agents and it withstands high temperatures up to 1200 °C, thereby opening new avenues for JJ material exploration and interface optimization. To validate the concept, we performed shadow evaporation of Al-based transmon qubits followed by stencil mask liftoff using vapor hydrofluoric acid, which selectively etches SiO<sub>2</sub>. We demonstrate an average  $T_1 \approx 75 \pm 11 \mu\text{s}$  over a 200 MHz frequency range across multiple cooldowns for one device, and  $T_1 \approx 44 \pm 8 \mu\text{s}$  for a second device. These results confirm the compatibility of stencil lithography with state-of-the-art superconducting quantum devices and motivate further investigations into materials engineering, film deposition, and surface cleaning techniques.

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## I. INTRODUCTION

Superconducting quantum circuits have been engineered for a broad range of applications,<sup>1</sup> ranging from photon<sup>2</sup> and particle detectors<sup>3</sup> to the current technological push for quantum computing.<sup>4–7</sup> In particular, superconducting qubits have steadily improved due to

advancements along several axes.<sup>8–14</sup> One of the most important aspects is fabrication process engineering, aiming to understand and reduce the density of two-level systems (TLSs),<sup>15–17</sup> and improving surfaces<sup>18–21</sup> and interfaces.<sup>22,23</sup> This includes the introduction of tantalum (Ta) ground planes and capacitors<sup>24–26</sup> or the investigation of

new capping materials.<sup>27</sup> The key non-linear element, the Josephson junction (JJ), has predominantly relied on double-angle evaporation techniques.<sup>28–30</sup> However, there are other approaches being explored to make the process more reproducible and scalable with optical lithography.<sup>31,32</sup> In addition to that, recent improvements in gap engineering to suppress quasiparticle tunneling,<sup>33–35</sup> simplified integration with surrounding circuit elements,<sup>36</sup> and the exploration of all-nitride electrodes,<sup>37</sup> all contributing to more robust and scalable JJ implementations.

Despite significant research and development efforts, resist-based lithography has remained the most commonly used method for fabricating superconducting quantum devices.<sup>18,38</sup> One of its key advantages is the easy processing through either liftoff<sup>39</sup> or etching<sup>40</sup> of the desired circuit element geometry. However, in the case of liftoff, the presence of the relatively fragile polymer mask limits pre-growth cleaning methods such as hydrofluoric acid (HF) treatments and deposition temperatures above  $\sim 300^\circ\text{C}$ . This could lead to amorphous or polycrystalline layers,<sup>41,42</sup> oxidized substrate surfaces,<sup>21,23</sup> and resist residues (sometimes called “veil of death”).<sup>43,44</sup> In the case of etching, better substrate preparation and high-temperature deposition are possible. However, structuring the layout requires *ex-situ* material-specific and highly selective dry or wet etching,<sup>26,37,45</sup> which may affect the film or substrate quality, especially in the vicinity of the junction. While using polymer masks has enabled high-performance qubit devices,<sup>22,25–27</sup> their shortcomings are becoming increasingly critical toward even higher coherence, calling for new strategies that preserve their respective benefits.

Stencil lithography<sup>46</sup> has recently emerged as a resist-free fabrication method, with distinct off- and on-chip implementations. Off-chip approaches decouple substrate preparation from the patterning of free-standing silicon (Si) membranes,<sup>47</sup> aiming to mitigate dielectric loss.<sup>18,21</sup> This decoupling allows for extensive substrate cleaning while avoiding post-processing. However, off-chip methods rely on delicate lateral spacers for alignment, making them sensitive to tilt between the mask and the wafer. Even small misalignment can lead to imprecise shadowing and blurring effects, ultimately limiting reproducibility and scalability. In addition, the membranes can be affected by tensile strain/stress in the membrane at elevated temperatures ( $> 600^\circ\text{C}$ ). In contrast, on-chip stencil lithography integrates the mask directly on the substrate, enabling precise shadowing and compatibility with aggressive cleaning, high-temperature processes and ultrahigh vacuum (UHV) conditions, depending on the material stack. On-chip masks have been successfully applied to various DC devices.<sup>48,49</sup> However, to our knowledge, on-chip masks have not yet been applied to the fabrication of coherent superconducting quantum devices. This is likely due to the robustness of the mask, which complicates liftoff after junction fabrication, and the potential performance limitations introduced by lossy dielectrics in high-frequency circuits if the stencil mask is not lifted off.

In this work, we develop an on-chip stencil lithography technique based on a pre-patterned silicon oxide/silicon nitride ( $\text{SiO}_2/\text{Si}_3\text{N}_4$ ) inorganic mask,<sup>50,51</sup> with the goal of making it compatible with the fabrication of coherent superconducting qubits. Our stencil mask enables aggressive cleaning chemicals and has been tested to withstand high-temperature annealing up to  $1200^\circ\text{C}$  in UHV conditions (see Fig. S1 in [supplementary material](#)), making it well suited for future material exploration and interface investigation. The crucial chip-wide

liftoff of the stencil mask is achieved by selectively etching the  $\text{SiO}_2$  with vapor hydrofluoric acid (V-HF) through openings in the  $\text{Si}_3\text{N}_4$  layer, without attacking the deposited materials. As a validation of the concept we show data on the coherence of two frequency-tunable aluminum (Al)-based transmon qubits fabricated with this approach.

The paper is structured as follows: Sec. II presents the developed stencil lithography technique. Section III shows the characterization of Al-based tunable transmon qubits fabricated via the stencil mask. Finally, in Sec. IV, we provide a conclusion and discuss possible applications for this technology.

## II. STENCIL FABRICATION

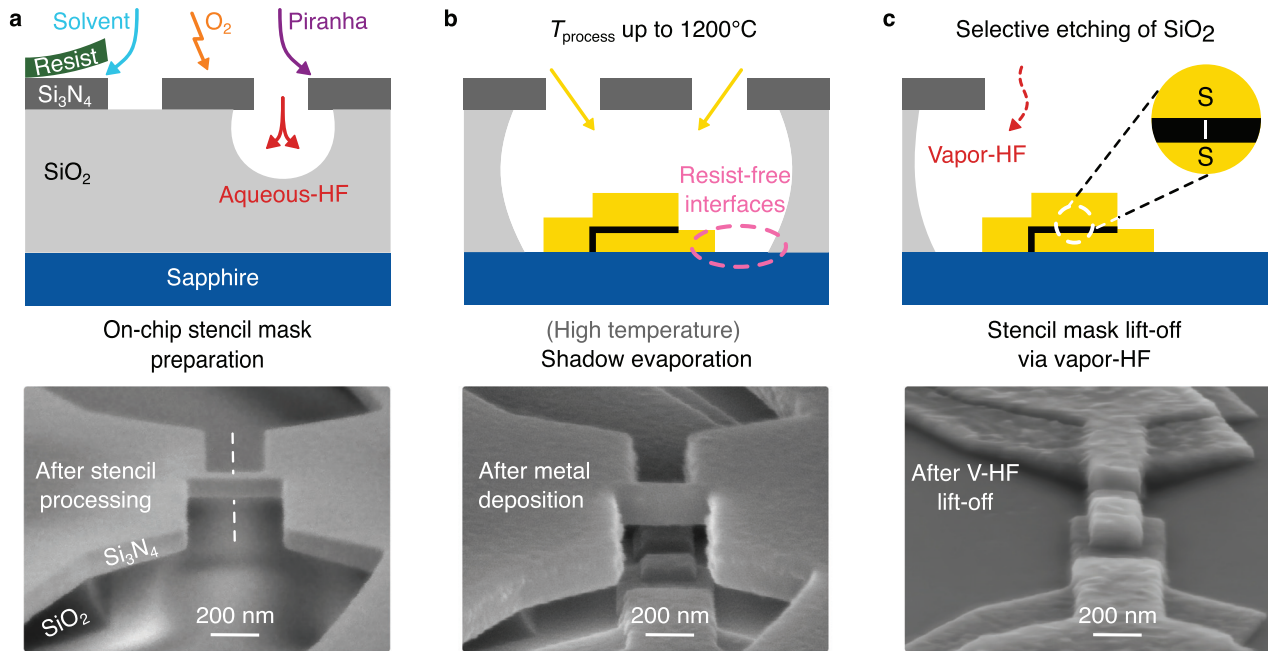
To pattern our qubit devices, we developed an inorganic on-chip mask fabrication. We initially deposit two layers via low-pressure chemical vapor deposition (LPCVD): a 300 nm  $\text{SiO}_2$  used as a sacrificial layer and a 100 nm  $\text{Si}_3\text{N}_4$  used as a mask layer. Both layers are deposited on a c-plane sapphire ( $\text{Al}_2\text{O}_3$ ) wafer following  $\text{HNO}_3$  cleaning (see [supplementary material](#)). This specific material combination enables two key fabrication steps:  $\text{SiO}_2$  can be selectively etched over  $\text{Si}_3\text{N}_4$  using aqueous hydrofluoric acid (A-HF 1%) prior to deposition, and over  $\text{Al}/\text{AlO}_x$  for mask liftoff via vapor-HF after deposition.

As shown in Fig. 1(a), the  $\text{Si}_3\text{N}_4$  is patterned using a standard, resist-based, electron beam (e-beam) lithography technique. To shape the mask layer, the top  $\text{Si}_3\text{N}_4$  layer is anisotropically etched via reactive ion etching (RIE) using a  $\text{CHF}_3/\text{O}_2$  gas mixture. Afterward, the e-beam resist is dissolved in AR 600–71 solvent, followed by an additional  $\text{O}_2$  plasma ashing step.

At this stage, the wafer is diced into the desired sample size after applying a protective dicing resist. The diced samples are cleaned and exposed to another  $\text{O}_2$  plasma ashing step. It is worth noting that, although polymer resists are used in these steps, they do not come into contact with the sapphire surface, as the sacrificial layer is not removed yet. To further clean any organic leftovers on the mask, the samples are dipped in a Piranha solution [ $\text{H}_2\text{SO}_4(96\%):\text{H}_2\text{O}_2(31\%)$  (2:1)]; which attacks neither the  $\text{SiO}_2$  nor  $\text{Si}_3\text{N}_4$  layers.

From this point onward, our technique ensures a *resistless*, single-step *in situ* stencil lithography. To expose the surface of the substrate and release the mask, the  $\text{SiO}_2$  is isotropically and selectively etched against the  $\text{Si}_3\text{N}_4$  via A-HF 1% [see Fig. 1(a)]. This creates an under-etch region around the edges of the  $\text{Si}_3\text{N}_4$  mask structures, thus preventing sidewall fencing during deposition and liftoff procedures. See [supplementary material](#) for more information. We have tested the stability of the inorganic stencil mask up to  $1200^\circ\text{C}$ . This high-temperature resilience can be leveraged in future experiments to add another surface treatment prior to deposition (see [supplementary material](#)). Once the stencil mask is prepared, we perform standard double-angle shadow e-beam evaporation to fabricate transmon qubits with Al superconducting electrodes (S) and  $\text{Al}/\text{AlO}_x/\text{Al}$  junctions, where the *in situ* formed, non-stoichiometric  $\text{AlO}_x$  serves as the insulating layer (I). The stencil mask is shown to be compatible with both Dolan (Fig. 1) and Manhattan-style junction layouts (Fig. 2).

Finally, for superconducting qubit applications, in contrast to DC devices, it is crucial to liftoff the stencil mask<sup>48</sup> to eliminate the dielectric losses and parasitic capacitive coupling induced by having the inorganic stack and the metal on top of it. Therefore, the mask is removed by selectively etching the  $\text{SiO}_2$  via V-HF<sup>52</sup> against the now functional SIS layers; shown in Fig. 1(c). This method has been previously shown to have a minimal impact on the performance of Al



**FIG. 1.** On-chip stencil lithography fabrication steps of a Josephson junction. The top row schematically presents the stencil fabrication steps, while the bottom row shows scanning electron microscopy (SEM) images of a stencil Dolan bridge for a JJ device. (Due to the dielectric nature of the stencil layers and sapphire substrate, SEM imaging prior to metal deposition is prone to charging, resulting in the observed shadowing from elevated stencil structures under the tilted incidence of the electron beam.) (a) After LPCVD deposition of the inorganic  $\text{SiO}_2/\text{Si}_3\text{N}_4$  bi-layer, the  $\text{Si}_3\text{N}_4$  is dry-etched, following a standard e-beam lithography and resist development, to form the stencil mask. This resist is then cleaned using solvent AR 600–71, an  $\text{O}_2$  plasma ashing step and a subsequent dip in Piranha solution [ $\text{H}_2\text{SO}_4$  (96%): $\text{H}_2\text{O}_2$  (31%) (2:1)]; none of which affect the stencil stack. The stencil mask is then released by selectively etching the  $\text{SiO}_2$  sacrificial layer against the  $\text{Si}_3\text{N}_4$  mask layer using aqueous hydrofluoric acid 1% (A-HF 1%). The dotted line in the SEM image indicates the planar cross section of the corresponding illustrations above. (b) The junction is fabricated by a standard double-angle evaporation using the shadow stencil mask. In contrast with resist-based methods, the stencil mask can survive temperatures up to  $1200^\circ\text{C}$ , allowing surface preparation and annealing in UHV conditions. (c) Finally, the stencil mask is lifted off via an anhydrous vapor-HF (V-HF) process, which isotropically and selectively etches  $\text{SiO}_2$  against the Al-based JJ trilayer (SIS).

resonators<sup>53</sup> and has more recently been explored for scaffolding-assisted junction fabrication,<sup>32</sup> as  $\text{AlO}_x$  acts as an effective etch-stop material for V-HF.<sup>54</sup> The sample is finally dipped in de-ionized (DI) water followed by isopropanol (IPA) to rinse off etching residues from the lift-off. Scanning electron microscopy (SEM) images of a stencil-made JJ before and after mask removal are also presented in Fig. 1. More details on the stencil process and its compatibility with different materials and substrates can be found in [supplementary material](#).

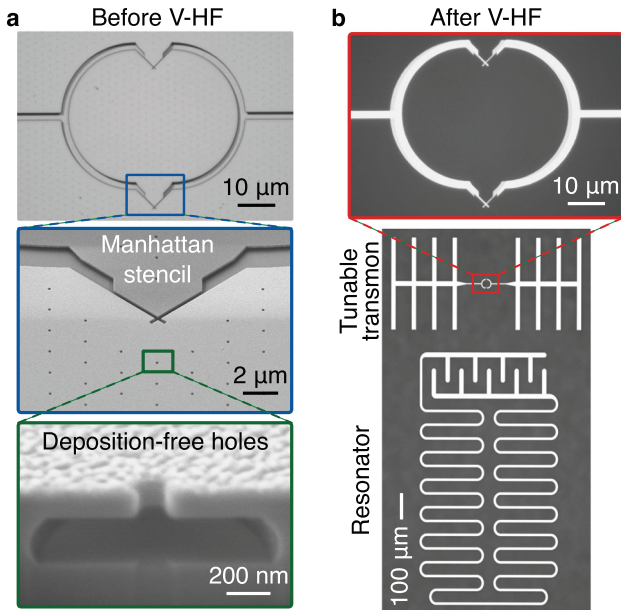
### III. STENCIL QUBIT

To test the validity of the on-chip stencil lithography fabrication, we use a tunable transmon qubit layout, as shown in Figs. 2(a) and 2(b). The design features a lumped element resonator capacitively coupled to two islands connected through a superconducting quantum interference device (SQUID) with two nominally identical Manhattan-style Al/ $\text{AlO}_x$ /Al junctions (see [supplementary material](#) for additional details on the design simulations). The chip contains four resonator-qubit pairs and one test resonator. To enable the V-HF lift-off, we integrate a hexagonal grid of holes across the sample. Their size is optimized to block unwanted deposition while allowing isotropic etching via V-HF as explained in [supplementary material](#).

After V-HF exposure and mask lift-off, we characterize the stencil-based qubits via standard circuit quantum electrodynamics

measurements in the dispersive readout regime.<sup>55</sup> The sample is mounted in a three-dimensional copper waveguide (as shown in Fig. S6) with a 6 GHz cutoff frequency, similar to Refs. 56 and 57. The waveguide is equipped with a global flux tuning bias coil, a qubit drive port, and a readout port through which the sample is measured in reflection via a circulator. After assembly, the waveguide is placed inside an aluminum and mu-metal magnetic shield and attached to the mixing chamber stage of the cryostat for thermalization to base temperature ( $\approx 20$  mK). See [supplementary material](#) for more details on the cryogenic setup.

We report here the measurement results on two qubits on the same chip, Q1 and Q2, summarized in Table I. The two additional qubits on the chip were not operational due to suspected electrostatic discharge during handling or measurement. In Fig. 3, we show the measured  $T_1$  energy relaxation times for the stencil qubits. For Q1, we observe an average energy relaxation time of  $\bar{T}_1 \approx 75.37 \pm 7.42 \mu\text{s}$  over a 60-h measurement period (see [supplementary material](#)). The exponential decay of the maximum (red), median (blue), and minimum (green) lifetimes are measured to be 140, 77, and  $52 \mu\text{s}$ , respectively. The mean value corresponds to a qubit quality factor of  $\sim 1.5 \times 10^6$ . The Ramsey dephasing time is measured to be  $T_2^{\text{Ramsey}} \approx 15 \mu\text{s}$ , and a  $T_2^{\text{Echo}} \approx 28 \mu\text{s}$ . Similar experiments were also performed on Q2, which exhibits  $\bar{T}_1 \approx 44.28 \pm 8.23 \mu\text{s}$  and  $T_2^{\text{Ramsey}} \approx 4 \mu\text{s}$ . The low  $T_2^{\text{Ramsey}}$  values could be attributed to charge



**FIG. 2.** Stencil fabrication of an Al/AIO<sub>x</sub>/Al transmon qubit. (a) The tunable transmon consists of two superconducting islands connected via a superconducting loop interrupted by two JJs, forming a SQUID device. Zoom-in (blue): The design features Manhattan-style junctions and a hexagonal grid of holes for faster V-HF liftoff (see Fig. S4). Their size is optimized to block unwanted deposition while allowing the V-HF gas to penetrate through. Zoom-in (green): A focused-ion-beam (FIB) cut showing the deposition-free substrate underneath one of the holes after Al-evaporation. See [supplementary material](#) for more details. (b) Gray-scaled microscope images of the entire transmon qubit circuit after V-HF liftoff. The white areas correspond to the deposited Al-trilayer, while the black area is the sapphire substrate. Zoom-in (red): The SQUID loop with both JJs and the superconducting ring after mask removal.

noise of the qubits. Complementary measurements are provided in [supplementary material](#).

In the following, we focus the discussion on Q1 to study its flux and time stability in more details. We apply an external flux to

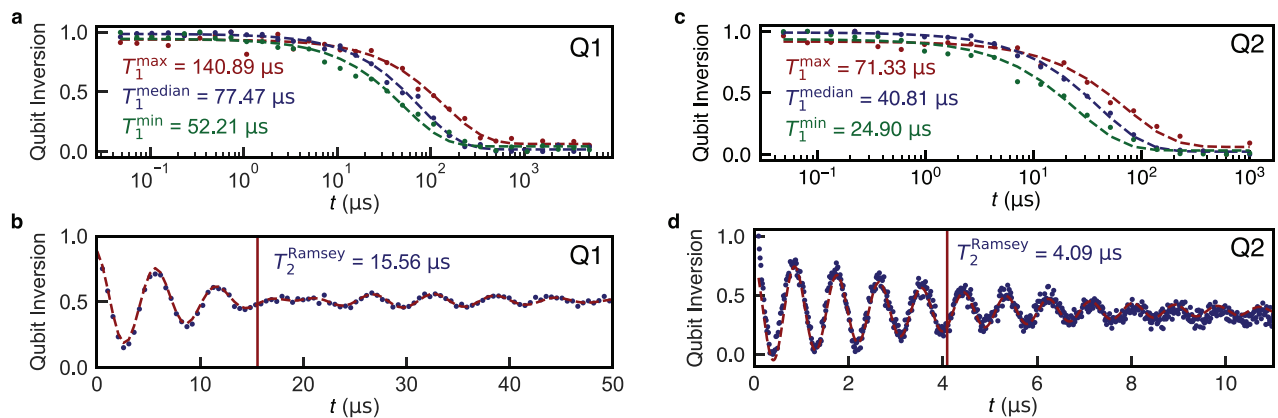
**TABLE I.** Extracted parameters for Q1 and Q2: transition frequency  $\omega_{01}$ , anharmonicity  $\alpha$ , resonator frequency  $f_r$ , resonator linewidth  $\kappa$ , dispersive shift  $\chi$ , Josephson energy  $E_J$ , charging energy  $E_C$ , and estimated SQUID asymmetry.

Parameter	Q1	Q2
$\omega_{01}/2\pi$ (GHz)	3.112	3.480
$\alpha/2\pi$ (MHz)	-202	-350
$f_r$ (GHz)	7.323	6.471
$\kappa/2\pi$ (MHz)	0.223	0.544
$\chi/2\pi$ (MHz)	-0.35	-1.5
$E_J/2\pi$ (GHz)	7.81	6.45
$E_C/2\pi$ (GHz)	0.17	0.28
SQUID asymmetry (max.)	5%	...

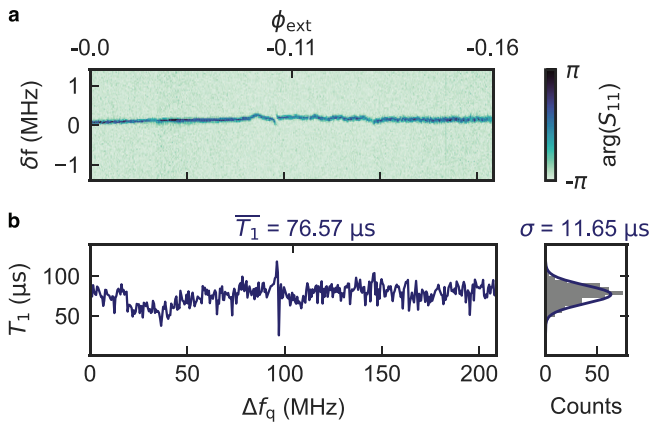
measure its response away from the zero-flux sweet spot. We track the 01 transition of Q1 across 200 MHz using two-tone spectroscopy [see Fig. 4(a)]. Within this range, we observe two avoided level crossings on the order of a few kilohertz. At each flux point, we measure the qubit's relaxation time  $T_1$ , as shown in Fig. 4(b). The measured  $T_1$  values remain relatively stable across the frequency range, similar to Ref. 58, indicating that our stencil method is compatible with state-of-the-art surface-engineered superconducting qubits. The average relaxation time across all flux points is  $\bar{T}_1 = 76.57 \pm 11.65 \mu\text{s}$ .

In a different cooldown of the same chip, we spectrally and temporally resolve  $T_1$  over a period of 8 h and a 125 MHz frequency range in Fig. 5. Each decay time is extracted by averaging over sequences of 50 stroboscopic qubit measurements, separated by  $10 \mu\text{s}$ , after preparing the qubit in the excited state with an initial  $\pi$ -pulse. As shown in the line-cuts in Fig. 5(b), these values remain rather stable over time as a function of flux. However, we notice that  $T_1$  fluctuates by almost an order of magnitude vs flux in Fig. 5(c), yet it consistently remains above  $\approx 20 \mu\text{s}$ .

A detailed analysis of the energy relaxation mechanisms is beyond the scope of this work and will be investigated in future studies.



**FIG. 3.** Time-domain measurement of two stencil transmon qubits on the same chip, Q1 and Q2, operated at their zero-flux sweet spot. (a) and (c) Decay curves of maximal, median, and minimal qubit  $T_1$  lifetimes (red, blue, and green, respectively) within a measurement period of 60 and 3.5 h for Q1 and Q2, respectively. The measurements are taken at zero external flux bias. (b) and (d)  $T_2^{\text{Ramsey}}$  coherence measurement where a beating pattern is visible due to a 0.028 and 2.5 MHz charge dispersion for each qubit, respectively. More measurements are provided in [supplementary material](#).

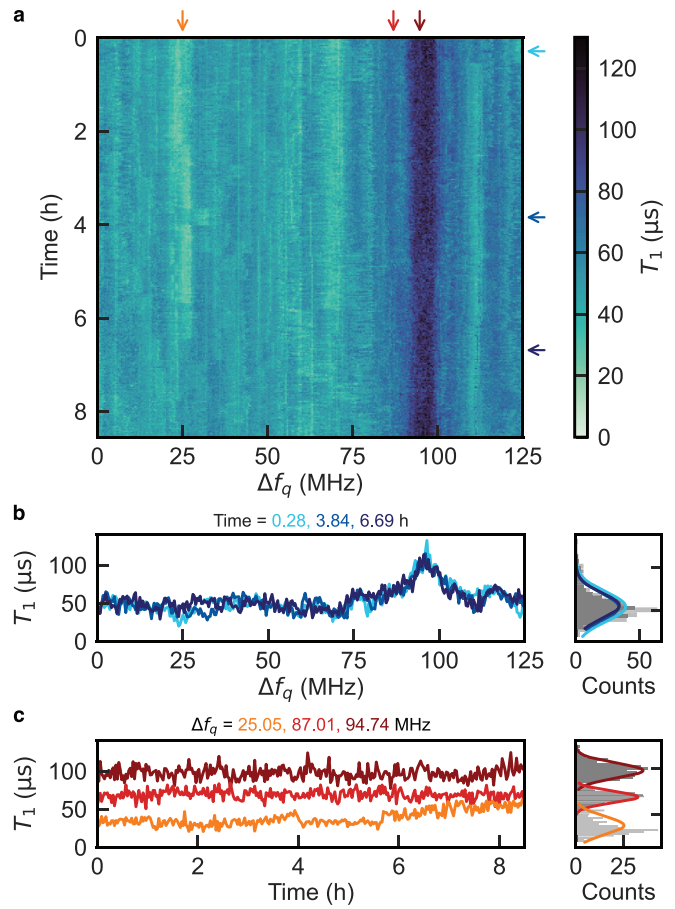


**FIG. 4.** Two-tone spectroscopy over flux of Q1. (a) Two-tone spectroscopy of the transmon qubit while tuning its frequency [ $f_q(\phi_{\text{ext}} = 0) = 3.114$  GHz] with an external flux ( $\phi_{\text{ext}}$ ) over 200 MHz. The qubit frequency is continuously tracked with a 3 MHz span range. The characteristic parabolic curve is here converted to a linear one for better visibility: The x axis shows the expected qubit frequency  $\Delta f_q$  from the circuit model, defined such that  $\Delta f_q = 0$  corresponds to 3.112 GHz, and the y axis is its deviation from the measured spectrum, defined as  $\delta f = f_{\text{measured}} - \Delta f_q$ . This allows us to resolve kilohertz-scale features, and the absence of pronounced peaks indicates a smooth spectrum consistent with a low density of parasitic coupling modes. (b) For every flux-point, we perform a  $T_1$  measurement and extract its value. The mean  $T_1$  is around  $76.57 \pm 11.65 \mu\text{s}$  over the same frequency range.

Possible explanations include defects within the junction materials,<sup>41</sup> short-term fluctuations in the TLS environment,<sup>58,59</sup> non-equilibrium quasi-particle poisoning,<sup>60,61</sup> or other loss mechanisms.

#### IV. CONCLUSION AND OUTLOOK

To summarize, we implemented on-chip stencil lithography based on a  $\text{SiO}_2/\text{Si}_3\text{N}_4$  material stack to fabricate and investigate Al-based coherent transmon qubits. The combination of this inorganic stack, together with aggressive cleaning like Piranha and aqueous-HF solutions, ensures resist-free substrate interface prior to material deposition. The mask can be lifted off via vapor-HF through the integrated grid of holes, without etching the functional Al-trilayer. We measured an average lifetime of a transmon qubit of  $T_1 \approx 76 \mu\text{s}$  and a coherence time  $T_2^{\text{Ramsey}} \approx 15 \mu\text{s}$ , which are similar to conventional transmons with resist-based fabrication.<sup>36</sup> Furthermore, we measured the spectral purity and the stability of  $T_1$  over time and frequency (see [supplementary material](#)), which showed similar characteristics as reported in the literature.<sup>17,58,62</sup> To conclude, we demonstrated that replacing organic resist with our inorganic mask does not compromise the functionality of standard SIS transmons and yields results comparable to resist-based qubits fabricated in the same chamber,<sup>63</sup> even without exploiting the thermal stability of the stencil. The presented technique opens the way for the exploration of new junction materials and surface cleaning methods and is also compatible with commonly used Si-substrates. By enabling high-temperature processing and aggressive cleaning steps, it may play an instrumental role in overcoming the decoherence bottleneck currently limiting superconducting qubit technology. In future work, we aim to leverage the stencil's thermal and chemical robustness to further push the limits of qubit performance.



**FIG. 5.** Spectral and time-resolved coherence measurements of Q1. (a) Spectral and temporal resolution of  $T_1$  in a different cooldown than before. Every point in this plot represents the lifetime of a decay curve measured with 50 stroboscopic projective qubit measurements spaced  $10 \mu\text{s}$  apart. (b) and (c) Line-cuts of  $T_1$  as a function of flux and time, shown for three representative points each with the corresponding distributions shown in right panels. The sigma values are reported in [supplementary material](#).

#### SUPPLEMENTARY MATERIAL

See the [supplementary material](#) for additional details on the stencil fabrication process of the presented qubits, together with supporting simulation and measurement data.

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## AUTHOR DECLARATIONS

### Conflict of Interest

The authors have no conflicts to disclose.

### Author Contributions

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## DATA AVAILABILITY

The data that support the findings of this study are openly available in Zenodo at <https://doi.org/10.5281/zenodo.15976967>, Ref. 64. Raw data as well as all measurement, data-analysis, and simulation code used in the generation of main and supplementary figures are also available in Zenodo.

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