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Validation of the SiPM-on-Tile readout chain for the CMS High Granularity Calorimeter

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Abstract: For the upcoming High-Luminosity LHC, the endcap calorimeters of the CMS detector will be replaced by the High-Granularity Calorimeter (HGCAL), a sampling calorimeter using silicon sensors in the front and plastic scintillators read out by SiPMs in the back. We have built and tested a slice of scintillator tile modules and readout electronics under realistic installation, grounding and powering conditions. Using this system, we validated the powering scheme, assessed the system stability and demonstrated data readout with the Serenity back-end hardware. The successful validation of the SiPM-on-Tile front-end as a complete system is an important milestone towards the construction and operation of HGCAL.

Keywords: Data acquisition circuits; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Front-end electronics for detector readout

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1 Introduction

The High Granularity Calorimeter (HGCAL) [1] will replace the current endcap calorimeters of the CMS detector [2] for the High-Luminosity LHC phase. While the front and inner part of HGCAL consists of silicon sensors, the outer part of the endcap is instrumented with plastic scintillator tiles and Silicon Photomultipliers (SiPMs), the so-called SiPM-on-Tile technology.

The active layers of the hadronic section of HGCAL are partitioned into 30-degree cassettes that are inserted into the absorber structure. Each cassette houses up to 15 scintillator tile modules, as well as silicon modules. The tile modules in the cassettes are arranged in three slices each covering 10° and read out independently from one another.

The commissioning of the SiPM-on-Tile readout chain with a Serenity FPGA board [3, 4] was presented at TWEPP 2024 [5]. That system only used two tile modules in a setup optimized for beam tests, and the prototype version of the motherboard was still missing one data concentrator ASIC. In parallel, the mechanical integration of HGCAL's tile modules into a cassette geometry was tested in the cassette assembly facility at FermiLab.

In this contribution, we present the electrical validation of the SiPM-on-Tile system as it is integrated in HGCAL's cassettes. This system — resembling a slice of the HGCAL detector — allows for a range of tests. Firstly, we validated the powering and grounding scheme, as described in section 3. Secondly, we verified that the system allows reading out all sensor cells completely and in the correct order (section 4). And finally, we measured the clock jitter and set upper limits for bit error rates (section 5).

2 Test setup

For the system tests we consider the largest independent unit of the SiPM-on-Tile readout chain, a string of 5 tile modules connected to one motherboard shown in figure 1.

The tile modules for the HGCAL detector are printed circuit boards with SiPMs, scintillator tiles and front-end ASICs. One plastic scintillator tile is placed on top of each SiPM. Each HGCAL tile module carries between 24 and 144 scintillator tiles and SiPMs, which are read out by one or two HGCAL readout chips (HGCROCs) [6]. The tile modules also contain a GBT-SCA ASIC [7] and DC/DC converters.

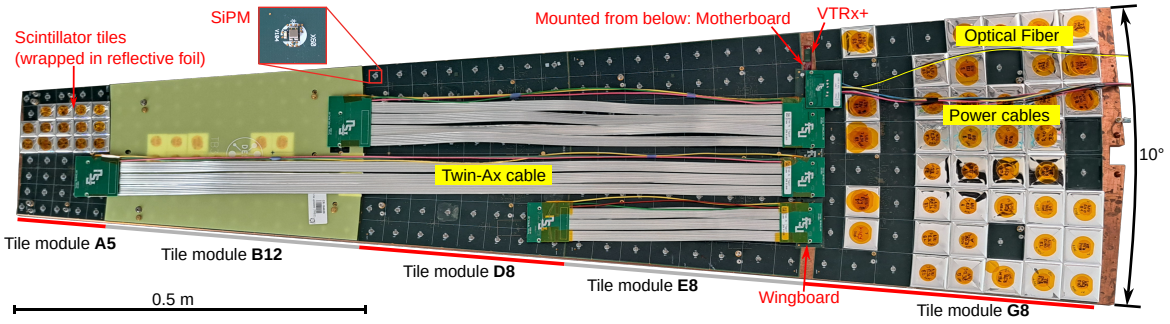

Figure 1. This setup is similar to a slice of the HGCAL detector and was used to validate HGCAL's SiPM-on-Tile readout chain. Five tile modules are mounted on a copper plate, which is approx. 1.5 m long and provides a realistic grounding scheme. Connectivity to the back-end is provided through a motherboard located between the detector modules. The optical fiber is highlighted for better visibility.

The motherboard houses three data concentrator ASICs: two ECON-T chips for aggregating trigger data, and one ECON-D chip for full event information [8]. Additionally, there are two lpGBTs [9] to serialize the data, one VTRx+ [10] for communication with the back-end, as well as a clock fan-out chip (called RAFAEL) and DC/DC converters. All five tile modules are connected to a wingboard, which is a passive fan-out board connecting to the motherboard.

The motherboard and wingboard are located between the two largest tile modules, E8 and G8. These two modules are connected to the wingboard via flexible printed circuit boards (flex PCBs). The other three tile modules are connected to the wingboard via twin-ax cables.

Just like in a real cassette, the tile modules are mounted on a copper plate. The plate has cutouts for the electronic components on the back side of the boards, such as the HGCROCs on the tile modules. The motherboard is mounted from below. The tile modules are electrically isolated from the copper plate by a Kapton foil.

The readout system used for these tests is based on a Serenity-Z 1.1 [3] board with a KU15P FPGA and data are read out via direct 10 Gb/s User Datagram Protocol (UDP) links to a data acquisition (DAQ) PC. This system was already used for the integration of the SiPM-on-Tile readout chain described in [5].

3 Powering and noise studies

The test setup was powered using realistic cable lengths and prototypes of power supplies described below that are foreseen for use at CMS. The common ground of the system is connected to the edge of the copper plate (which would be the patch panel PP0 in a cassette). There are two voltages that need to be provided to the SiPM-on-Tile system:

- The 10 V DC supply for the ASICs is provided from racks that would be located in the CMS cavern. In our test setup, we used a prototype power supply from Wiener [11], 20 m of cable until PP1 (the patch panel on the HGCAL endcap) and another 3 m of cables until the detector setup.
- The SiPM bias voltage V_{bias} of up to 50 V is provided by a CAEN A2554 [12] power supply which would be located in a low-radiation environment outside the CMS cavern. Therefore, we tested with a cable length of 100 m between the power supply and PP1, and another 6 m between PP1 and the detector.

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Using an oscilloscope, we recorded the voltage transients for switching on and off 10 V and V_{bias}. In all cases, we observed clean voltage ramps without overshoot nor undershoot.

When all ASICs are fully configured, the test setup with five tile modules and one motherboard draws approximately 14.5 W of power from the 10 V supply. We observed a voltage drop of roughly 2 V on the 23 m long cables. This voltage drop is acceptable, and it can be mitigated by supplying a slightly higher input voltage of 11.5 V.

As a benchmark for possible impacts on the detector performance, we use the pedestal (average) and noise (standard deviation) of the values measured with the analog to digital converter (ADC) of each HGCROC channel. Both values are computed from 10 k randomly triggered events with no particle signals present.

The difference in ADC pedestal and noise for the system powered with the scheme described above, compared to using a lab power supply (AimTTI MX100TP) and short cables of approx. 1 m, is less than 0.4 % (averaged over all channels) and not statistically significant. The same applies when the detector modules are mounted on the copper plate, compared to operating the system on a desk without copper plate.

4 Data readout and mapping

Data from the detector modules are read out in two separate paths. For each bunch crossing, reduced event information are sent on the trigger path. If an event is accepted by the level 1 trigger of CMS, then the full event information are read out through the DAQ path. These two readout paths with their respective data concentrators ECON-T (trigger) and ECON-D (DAQ) are visualized in figure 2.

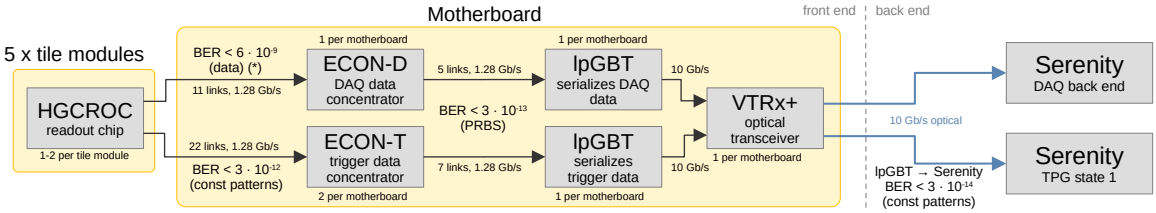

Figure 2. Flow of DAQ and trigger data from the HGCROCs to the back-end. For the validation of the data integrity described in section 5, each link was monitored for bit errors. The measurement method and the BER limit at 95 % confidence level are indicated next to each link in the figure.

To test our understanding of the data mapping, the HGCROCs of all tile modules were configured to send constant ADC values which then were compared to the data readout. This way, we verified that the data are correct and complete for both readout paths.

Figure 3 displays ADC data read out on the DAQ path, from the HGCROCs through the DAQ data concentrator (ECON-D), to the Serenity back-end. Plotting the received data into a 2D map of the tile modules leads to the desired test pattern (a readable text), demonstrating that our understanding of the data flow and mapping is correct. Four sensor cells are missing on the leftmost tile module (A5). This is due to a limitation of the readout system used for these tests, and not a problem of the front-end.

On its trigger outputs, the HGCROC sends sums of 2×2 sensor cells to the two trigger data concentrators ECON-T. In the SiPM-on-Tile system, the ECON-T then again forms sums of 4, leading to super trigger cells (STCs) of 16 sensor cells.

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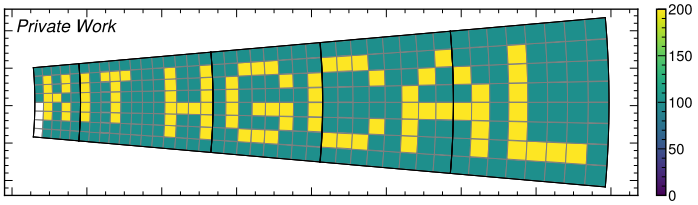

Figure 3. When the HGCROCs are configured to send constant values, the desired pattern (a readable text) is reproduced in the data arriving in the back-end.

In figure 4, the trigger data received in the back-end are compared with the DAQ readout for each channel. The STCs are arranged as slices of 2×8 sensor cells. This way, each STC corresponds to one electrical link from an HGCROC to one of the two ECON-Ts. Figure 4 demonstrates that the trigger data sent from the HGCROCs arrive in the correct order at the two ECON-T chips and are correctly reconstructed in the back-end. One super trigger cell is not read out on the trigger path. This is because one electrical link is routed to the wrong ECON-T on the motherboard. This issue is fixed in the production version motherboards.

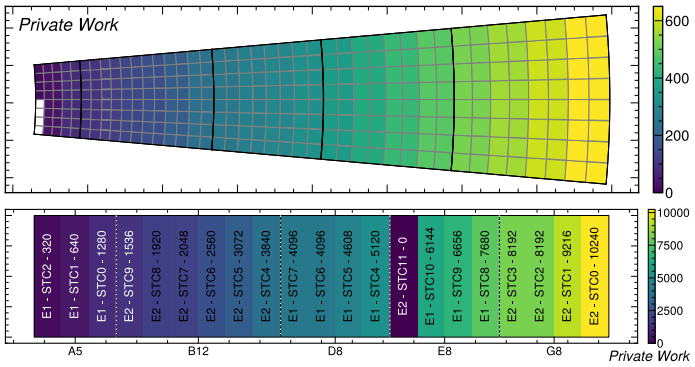

Figure 4. The value of each super trigger cell (STC) read out on the trigger data stream (bottom panel) corresponds to the sum of 16 sensor cells (top panel). The HGCROCs are configured to send constant data.

5 Clock distribution and data integrity

We consider three different methods to assess that the data transmission in the system is reliable. Firstly, we measured the jitter of the 320 MHz fast clock, which is used as the input clock of HGCROCs and ECONs. Secondly, we measured the eye diagrams at the inputs of the ECONs, probing data sent by the HGCROCs. And finally, we calculated a bit error rate (BER) upper limit for each data link in the system.

The lpGBT recovers the reference clock from the serial data stream sent on the optical link to the front-end. This clock signal is distributed as a 320 MHz "fast clock" to the other ASICs. The HGCROCs on the tile modules use their own phase-locked loop (PLL) to recover this clock signal. The A5 tile module is located at the end of the 10° scintillator sector and is connected via a 1 m long twin-ax cable to the motherboard and wingboard. We therefore consider the A5 tile module the "worst case" for clock distribution.

We used a Tektronix MSO 64 Oscilloscope (6 GHz, 25 GS/s) and a Tectronix TDP 3500 differential probe (3.5 GHz). We define the clock jitter as the standard deviation of the time interval error (TIE)

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on a 1 ms long acquisition with 25 M points. On the A5 tile module, we measured a clock jitter of 5.8 ± 0.1 ps at the 320 MHz fast clock input of the HGCROC, and a jitter of 17.6 ± 0.1 ps at the HGCROC's 160 MHz PLL probe output. Both values agree with the specifications defined in the HGCAL TDR [1] and are consistent with the clock jitter measured in HGCAL's silicon section.

The HGCROCs and the ECON-D both have independent counters for event number, bunch crossing number and orbit number. We did not observe any disagreement between these counters across 100 k events, which is another indication of successful clock and fast command distribution.

Using the same oscilloscope and probes, we measured the eye diagrams of all electrical links sending DAQ or trigger data from the A5, B12 and D8 tile module to the motherboard. The signals were probed through vias on the twin-ax cable connectors using a differential probe. The flex PCBs connecting the E8 and G8 board do not have these kind of vias and could not be probed. The differential signals of all probed links had a differential amplitude of more than 140 mV, which is required by the electrical receivers that are used in the lpGBT and ECON ASICs [9].

To estimate an upper limit for the BER, we configured the ASICs in the readout chain to send known bit patterns (either constant patterns or PRBS). The next ASIC in the readout chain or the back-end receives these patterns and compares against the expected values. The connection from the HGCROC to ECON-D cannot be probed this way, instead the ECON-D indicates whether data packets were received correctly.[1]

We did not observe bit errors in any of the probed links. Figure 2 illustrates the flow of DAQ and trigger data from the HGCROCs to the back-end, and shows the BER upper limit at 95 % confidence level for each link.

6 Conclusion and outlook

For the validation of HGCAL's SiPM-on-Tile system, we have built a test setup that emulates a realistic installation, powering and grounding environment. The setup consists of five tile modules, one wingboard and one motherboard mounted on a copper plate.

We verified that the powering and grounding scheme works as expected and does not impact the detector performance. The readout of DAQ and trigger data was demonstrated for the complete system. Finally, the clock distribution agrees with the specifications and we have set BER upper limits on all data links in the system.

The successful commissioning and testing of HGCAL's SiPM-on-Tile system is an important milestone towards the construction of cassettes and the operation of the full detector system.

The operation of the front-end in cold environment (−35 °C), as well as SiPM-on-Tile and silicon modules together on one cassette is ongoing with dedicated test stands at the cassette assembly facility at FermiLab.

In parallel to the validation of the front-end, the integration of the SiPM-on-Tile system into the new Serenity-S back-end is being pursued. In terms of system validation, a more powerful Serenity-S back-end will allow to refine some of the above tests and to set lower BER limits on the electrical links in the front-end.

[1] Since the currently used data acquisition system can parse ECON-D packets only at a limited rate, we can only set a BER upper limit on the 10^{-9} level for the HGCROC to ECON-D links. All other links were checked to a BER upper limit on the 10^{-12} level or better.

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Acknowledgments

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