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MightyPix — A novel HV-CMOS sensor for the LHCb Mighty-Tracker

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Abstract: MightyPix is a High Voltage Monolithic Active Pixel Sensor (HVMAPS) for the proposed LHCb Mighty-Tracker. It is designed to handle hit rates of over 32 MHz cm^{-2} with 3 ns timing precision and a high radiation tolerance with NIEL of 3×10^{14} neq/cm^2 and 40 Mrad total ionising dose. Building on prior prototypes, MightyPix1 and LF-MightyPix, MightyPix2 integrates a segmented matrix architecture with enhanced readout and control systems, including LHCb specific Timing and Fast Control (TFC) and Experiment Control System (ECS) interfaces, a synthesized double data rate (DDR) serializer, and an improved column-drain architecture with hit preloading. Designed in AMS' aH18 process, MightyPix2 achieves over 99.9 % readout efficiency in simulations and supports serial powering.

Keywords: Digital electronic circuits; Particle tracking detectors (Solid-state detectors); Pixelated detectors and associated VLSI electronics

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1 MightyPix for the Mighty-Tracker

A novel High Voltage Monolithic Active Pixel Sensor (HVMAPS) [1] named MightyPix is currently being developed for the planned Mighty-Tracker at LHCb. The inner part of the Sci-Fi tracker is set to be replaced by pixel sensors during LS4 due to their higher radiation hardness, rate capability, and better granularity [2]. The sensor requirements are given by [3]. The maximum hit rate is specified to be $32\,\mathrm{MHz\,cm^{-2}}$ which, together with the maximum number of four 1.28 Gbps output links, results in a maximum number of 40 bit per hit dataframe, while the readout time may not exceed the time-of-arrival (ToA) counter overflow period of $12.8\,\mu\mathrm{s}$. Due to the use of serial powering all data links, as well as the LHCb specific Experiment Control System (ECS) and Timing and Fast Control (TFC) interface to the chip, must be AC coupled and therefore DC-balanced.

Section 2 gives a design overview over the newest reticle size prototype submitted in October 2025, with a focus on the preloading enhanced column-drain architecture. In section 3, simulation results of the old and new architecture are discussed and compared.

2 MightyPix2 design overview

2.1 Sensor matrix

The block diagram of MightyPix2 is shown in figure 1. The sensor matrix comprises 122 columns, each containing two sub-columns with 194 pixels. The sensing element in each pixel is a p-n diode formed by the deep n-well implant and the high-resistivity p-substrate ($> 300\,\Omega\,\mathrm{cm}$). This diode is reverse-biased below the expected breakdown of 200 V, creating a depletion region of approximately $100\,\mu\mathrm{m}$. Charge generated by incident particles or photons is transported to the deep n-well via drift and is subsequently processed by in-pixel electronics housed in shallow n-wells and p-wells.

The collected charge is converted into a voltage pulse by a charge sensitive amplifier (CSA), which features a cascode amplifier utilizing a combination of NFET and PFET input devices to enhance the transconductance g_m. The voltage pulse is shaped by a bandpass filter and fed into a comparator to produce a digital pulse. The comparator consists of a cascade of three NFET differential amplifiers with NFET loads, placed in an isolated p-well. The cascade is needed because the NFET load has low output impedance $1/g_{\mathrm{m,load}}$ and therefore the voltage gain is only $g_\mathrm{m}/g_{\mathrm{m,load}}$. PFET transistors cannot be used here, as they would be placed in an n-well which cannot be isolated from the deep n-well

acting as the sensing electrode. Therefore, there would be no way to prevent capacitive coupling of large signals on metal lines or diffusions into the sensing n-well. Nevertheless, a PFET could be used as input transistor as the presence of a cascode reduces the voltage swing on the drain of the input transistor. This reduces the parasitic charge injected into the sensing electrode, and hence the corresponding negative feedback, to negligible levels.

2.2 Matrix readout

The output of each comparator is separately connected to a hit buffer, which uses asynchronous logic to prevent hit information from being overwritten by subsequent hits. The buffer also includes priority logic that gives preference to rows with lower numbers. At the leading edge of the pulse, a 12 bit 320 MHz ToA timestamp with an overflow period of 12.8 µs is stored in Dynamic Random Access Memory (DRAM) cells. An additional 4 bit timestamp is captured at the trailing edge to determine the time-over-threshold (ToT), available for timewalk compensation. The DRAM outputs of each hit buffer are connected to a shared bitline. Driven by the readout finite state machine (FSM), data from the highest priority hit buffer in each column is loaded into an End-Of-Column (EoC) buffer. Four readout FSMs manage the matrix, with each controlling a segment of 30 or 31 columns.

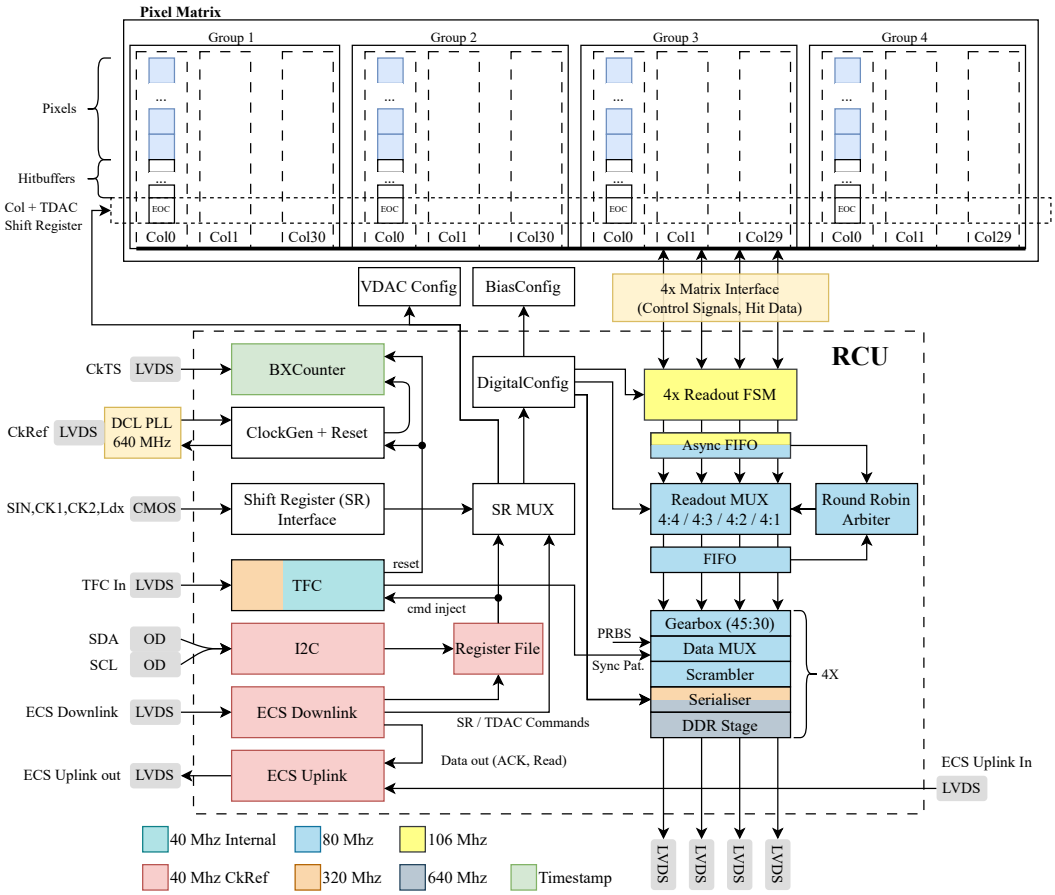

Figure 1. MightyPix2 block diagram showing the connections between the segmented pixel matrix and the digital readout control unit (RCU).

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2.3 Readout Control Unit (RCU)

The data from the EoCs is retrieved by the readout FSMs and stored as 30 bit or 32 bit data words in asynchronous first in, first outs (FIFOs). These FIFOs are connected to a multiplexer controlled by a round-robin arbiter, ensuring fair distribution of data across the selected output links. The data is then forwarded to serializer trees, which include a gearbox to split data words larger than 30 bits into the 30 bit data format. A multiplexer is used to inject special data words required for the time alignment of the detector or Pseudorandom Binary Sequence (PRBS) data for link quality testing. The data is scrambled using a parallel multiplicative scrambler to improve DC balance and then serialized. Depending on the configured output data rate of 320, 640, or 1280 Mbps, the data is first serialized by a shift register based serializer to 1, 2, or 4 bits at 320 MHz. A second stage operating at 640 MHz serializes the 4 bit data at 320 MHz into 2 bit data at 640 MHz. The final stage consists of latch-based double data rate (DDR) multiplexers operating at 640 MHz for the 1.28 Gbps rate and 320 MHz for the 640 Mbps rate.

The chip incorporates two slow control interfaces primarily used for configuring and monitoring the device, as well as reading back status registers and on-chip ADC data. The main interface is the serial ECS downlink operating at 10 Mbps, utilizing 8b10b encoding for DC balance, and an oversampling receiver. It employs an I2C-like protocol with a header containing a chip ID, enabling multiple chips to share a single LVDS bus, a register address, and a burst write/read bit. During read/write operations, data is transferred from and to a central register file and transmitted via the ECS uplink daisy-chain interface. This uplink interface features a receiver, an 8b10b decoder for data received from the previous chip, and an arbiter to select between internal data and data from the chain. The output data is 8b10b encoded and sent via an LVDS driver at 10 Mbps. Additionally, an acknowledgment is sent for every received command. For debugging purposes, a 1 Mbps I2C interface is also available, which is connected to the same register file.

The TFC interface is a LHCb-specific 320 Mbps serial interface that supports 8 bit commands for time alignment, ToA counter resets, calibration, and front-end resets. Commands are 6b8b encoded to ensure single-bit error detection and maintain DC balance. Since this module can reset sensitive parts of the chip, it is implemented with triple modular redundancy, similar to all configuration registers and reset synchronizers, except for the deserializer.

The chip operates with multiple clock domains. An external 40 MHz clock serves as the reference for the integrated PLL and directly drives the ECS and I2C modules. This design ensures that the interfaces used for chip configuration do not rely on PLL-generated clocks, as the PLL requires initial configuration. The clock manager divides the VCO clock by 16 to generate a 40 MHz feedback clock, resulting in a 640 MHz VCO clock. It also provides a 80 MHz clock for most of the logic, a 320 MHz clock for the serializer, and a 106.67 MHz clock for the FSM.

2.4 Improved End-Of-Column (EoC) readout

To enhance the previous maximum hit rate capability and reduce the readout time of the column-drain architecture [4], MightyPix2 has been improved with a preloading mechanism. The state diagram of the readout FSM is shown in figure 2c and the working principle is explained below. States with suffix 2 are wait states, to avoid hold violations in the latch based hit buffer and EoC logic.

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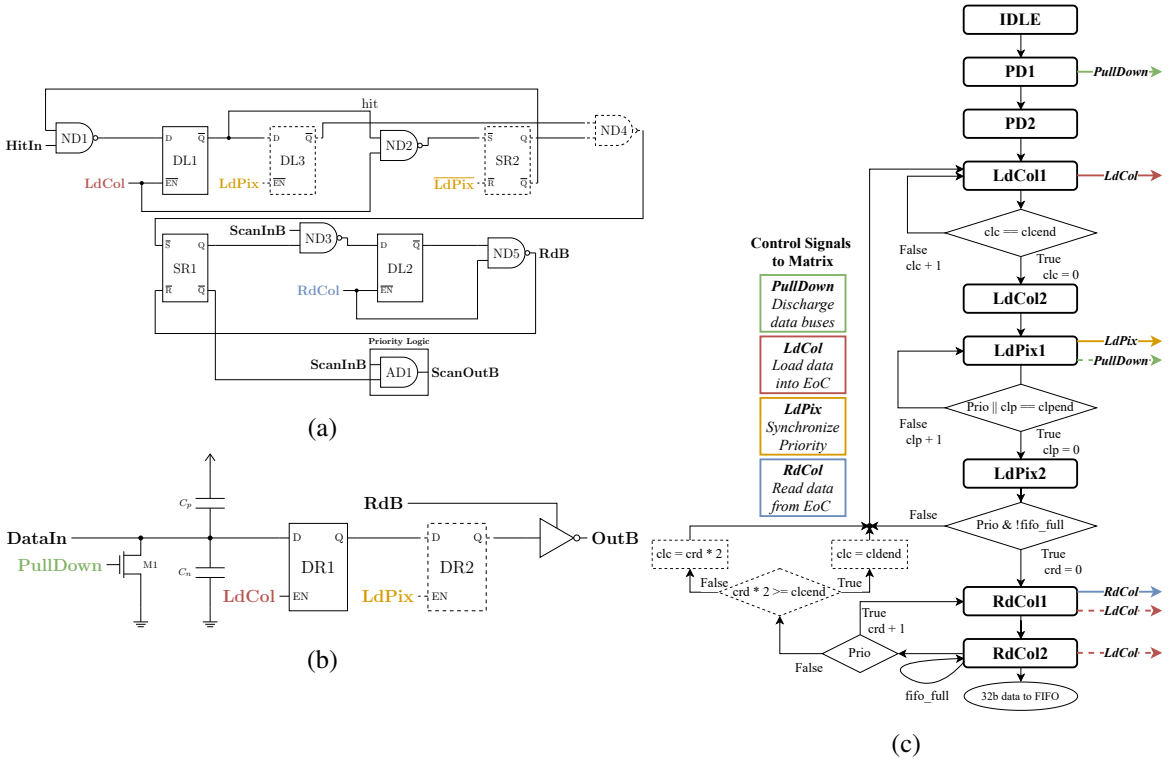

Figure 2. (a) EoC logic with additional registration for preloaded data. (b) Column data receiver with additional latch. (c) State diagram of the modified readout FSM. PD discharges bitlines; LdCol transfers the highest-priority hit buffer into the EoC; LdPix synchronizes priority logic; RdCol reads the column data receiver while pre-loading the next word.

1. *PD1*: All hit buffer bitlines are discharged to 0 V, because the PFET-based DRAM can only pull it up to logic 1.

2. *LdCol1*: Data is loaded from the highest priority hit buffer into the EoC. The high output impedance of the DRAM cells causes the bit lines to take up to 100 ns to charge, requiring the FSM to wait for 11 cycles, until the clc counter reaches 11.

3. *LdPix1*: Synchronizes the priority logic in the hit buffers to ensure that hits arriving during the LdCol1 state are read only in the next cycle. If the Prio signal is active, it is signalized that at least one EoC stores data ready for readout.

4. *RdCol1*: Data is retrieved from the column data receiver, as illustrated in figure 2b. The pull-down NFET, the bit line capacitance, and the first data D-Latch DR1, controlled by the LdCol1 signal, is shown. An additional D-Latch DR2 has been introduced to capture the data from DR1 during the LdPix1 state. This allows the preloading of new data into DR1 already in RdCol1 state, but makes it necessary that the previous state LdPix1 also discharges the bitlines. The FSM stays in RdCol states as long as there are columns to read out, simultaneously, the LdCol signal remains active to initiate data preloading into DR1.

Once all columns have been read, Prio is inactive, the FSM transitions back to the LdCol1 state. However, the preloading time during the RdCol states is subtracted from the wait time. For instance,

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if six hits are read out, the preloading time spans (RdCol1 + RdCol2) × 6 = 12 cycles, allowing the FSM to immediately proceed to the LdPix1 state. This reduces the number of non-RdCol cycles used for data preparation from PD1 + PD2 + 11 × LdCol1 + LdCol2 + LdPix1 + LdPix2 = 16 to just 2 cycles. Consequently, in scenarios where every column contains a hit, the ratio of readout to total cycles improves from 60/76 to 60/62. If at least 6 columns have a hit, all wait states are skipped in the next cycle, increasing the efficiency from 12/28 to 12/14. Additionally, the readout FSM reads data at 53 MHz, exceeding the 40 MHz output-link bandwidth and thus compensating for the remaining non-readout cycles due to 12/14 × 53 MHz/40 MHz > 1.

The modified EoC logic is depicted in figure 2a. If the Prio input is active and no data is already stored in DR1, the hit flag is set by DL1. To avoid premature changes in the priority output, DL3 delays the priority output update until the synchronization by LdPix. This ensures that the column data receiver is not read out before the data is transferred to the newly added latch DR2. Simultaneously, SR2 resets the hit flag after the transfer, enabling new data to be loaded into DR1.

3 Hit rate capability simulation

To verify the hit rate capability of MightyPix2 and quantify the improvements described in section 2.4, the design is simulated with the verification framework presented in [5, 6]. The actual digital design is simulated together with a behavioural model of the analogue pixel matrix in a Verilog simulator. An event driver generates random Poisson distributed hits at a rate of 35 MHz cm^{-2} and a fixed worst-case ToT of 2 µs. The efficiency and the readout delay from hit occurrence to readout is then analysed with a Python tool. The results for the readout time vs column are shown in figure 3 for the old (left) and new (right) readout scheme.

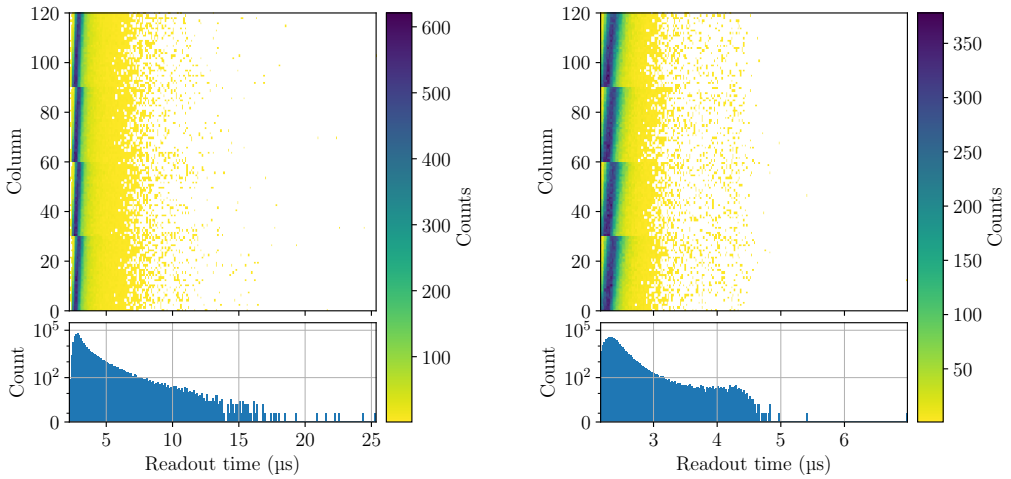

Figure 3. Simulated readout time at a hit rate of 35 MHz cm^{-2} for old (left) and the new (right) readout scheme.

It is clearly visible that the maximum readout time has decreased from 26 µs to 7 µs, Whereas the mean readout time has improved from 3.1 µs to 2.4 µs, fulfilling the requirement of maximum 12.8 µs. The readout efficiency, the ratio of read hits over the number of injected hits, improved from 99.74 to 99.92 %, due to a lower number of hits exceeding the maximum readout time and fewer hits lost due to pileup inside the pixel.

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4 Summary and outlook

MightyPix2 introduces a segmented matrix, enhanced column-drain readout with hit preloading, and serial powering compatible digital interfaces. Simulation studies demonstrate a reduction in the maximum readout time from 26 µs to 7 µs, and an increase in readout efficiency to above 99.9 % under high-rate conditions, fulfilling the requirements of the Mighty-Tracker.

A further improved readout delay, realized by a higher number of readout groups and reduced pixel ToT, opens the door to implementing output data compression. Aggregating hits with similar ToA in one data frame, can potentially enable a rate capability over 40 MHz cm^{-2}.

Acknowledgments

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