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Towards a scalable data readout system for $\overline{\text{P}}$ANDA

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Abstract: The $\overline{\text{P}}$ANDA experiment at FAIR employs a trigger-less data acquisition (DAQ) concept, requiring a scalable and high-performance readout architecture. In this contribution, a scalable data readout system for the $\overline{\text{P}}$ANDA Micro-Vertex Detector (MVD) is presented. The readout architecture consists of the Torino Amplifier for silicon Strip detector (ToASt) front-end ASIC, the Module Data Concentrator (MDC) ASIC and the custom back-end electronics card based on the Advanced Mezzanine Card (AMC) standard. Based on an established prototype, the MVD readout chain was further developed through incremental integration, including its extension to multiple detector modules to demonstrate scalability. In addition, the system was operated over an extended period at high data throughput, showing stable and error-free operation. Moreover, the status of the design and production

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of the MDC ASIC and the back-end electronics card are reported in this work. The design progress and prototype results represent a step toward integration of the full readout chain into the $\overline{\text{P}}$ANDA experiment. Furthermore, the back-end electronics card has been conceived as a flexible platform, enabling potential applications beyond this specific application.

KEYWORDS: Data acquisition concepts; Digital electronic circuits; Electronic detector readout concepts (solid-state); Large detector systems for particle and astroparticle physics

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1 Introduction

The Facility for Antiproton and Ion Research (FAIR) at GSI in Darmstadt is currently under construction and will host the antiProton ANnihilation at DArmstadt ($\overline{\text{P}}$ANDA) experiment [1]. $\overline{\text{P}}$ANDA aims to investigate the properties of hadronic matter and the dynamics of the strong interaction using antiproton-proton annihilations. The $\overline{\text{P}}$ANDA data acquisition (DAQ) system operates in a free-running, trigger-less mode at estimated data rates of up to 100 GB/s [2], posing demanding requirements in the DAQ system design. The innermost $\overline{\text{P}}$ANDA sub-detector, the Micro-Vertex Detector (MVD), consists of silicon pixel and double-sided microstrip sensors and is designed for tracking primary interactions and secondary vertices of short-lived particles, as well as for particle identification. In previous work, a DAQ concept for the MVD has been developed, focusing on the microstrip sensor readout, and system-level validation was performed with a prototype setup [3, 4]. This setup was extended to assess scalability, and was operated at high data throughput, with the results reported in section 2.1. Within this prototype setup, the MDC was validated at system level as a central element of the readout chain during its design phase. The status of the MDC-ASIC design and production is presented in section 2.2. Significant development effort has also been devoted to another key component of the readout chain, namely the back-end electronics card. Its current design status is reported in section 3.

2 Readout chain for the $\overline{\text{P}}$ANDA Micro-Vertex Detector

As the innermost component of the $\overline{\text{P}}$ANDA detector, the MVD consists of silicon pixel and double-sided microstrip sensors for precise tracking and particle identification. The schematic overview of the MVD microstrip readout chain, which is the focus of this paper, is shown in figure 1.

The readout chain includes the Torino Amplifier for silicon Strip detector (ToASt) [5, 6] front-end ASICs that readout the sensor data and stream them to the MDC. The MDC collects and processes data from multiple ToASt chips and transfers them over an low power GigaBit Transceiver (lpGBT) [7] link to the back-end electronics, which perform data reduction, interface with the experiment's timing and control system, and forward the data via 100 GbE link to the computing network for event building and storage. A detailed description of the MVD readout chain architecture and its main features has been presented in previous work [3, 4], together with the establishment of a prototype setup of the MVD readout chain as a proof of concept.

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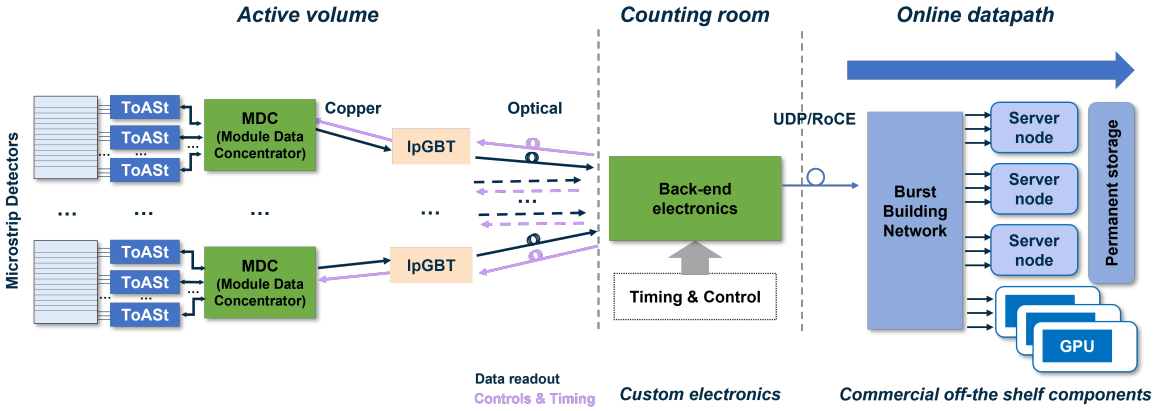

Figure 1. Architecture of the PANDA MVD microstrip sensor readout chain. Reproduced from [3]. The Author(s). CC BY 4.0.

2.1 Micro Vertex Detector readout chain prototype setup and tests

The MVD readout chain prototype consists of four microstrip sensors, each connected to a ToASt (v1) front-end module. The configuration represents two independent detector modules. Each module is managed by an MDC, which in this setup is emulated as a Field-Programmable Gate Array (FPGA) implementation on a custom readout card. Each MDC interfaces via an lpGBT link on a Versatile Link+ Demo Board (VLDB+) [8] with an AMD-Xilinx ZCU102 [9] card. This card was selected to emulate the future back-end electronics card since it features an MPSoC of the same family. The MPSoC combines FPGA firmware for data collection with an embedded processor that handles slow control, sensor configuration, and data consistency checks. The setup of the readout prototype is shown in figure 2.

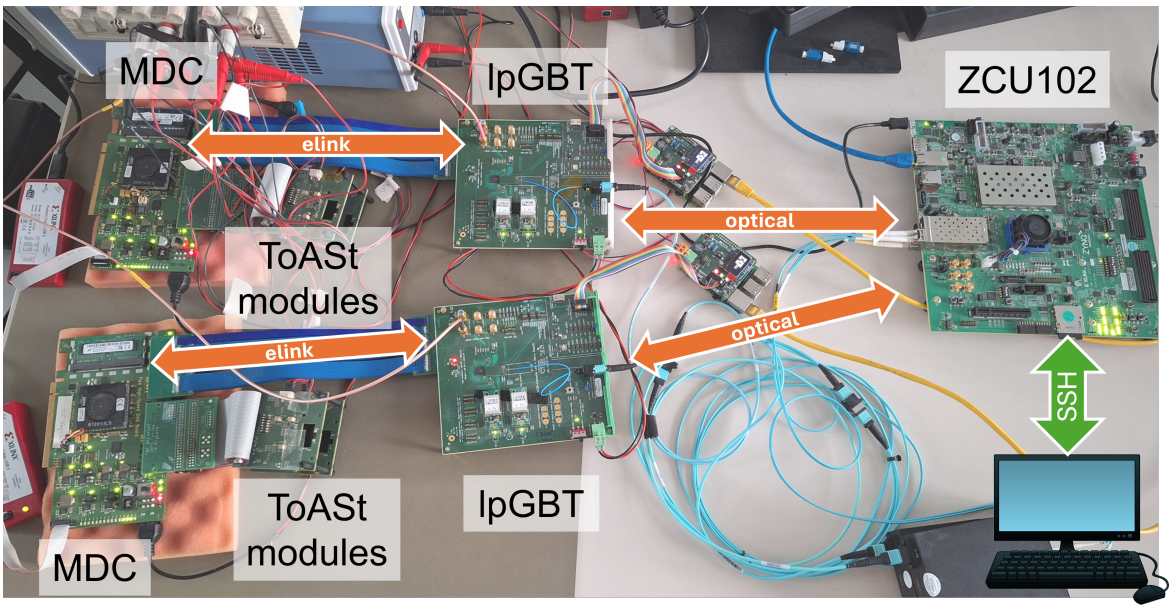

Figure 2. Prototype setup of the PANDA-MVD readout chain with four ToASt modules and two MDCs emulated on FPGA connected via lpGBT to the ZCU102 back-end.

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The firmware implemented on the ZCU102 integrates the lpGBT FPGA IP block [10] interfacing to the lpGBT links running at 10.24 Gbit/s. Data from individual streams are packed into uplink packets, which are temporarily stored in First-In-First-Out (FIFO) buffers. These buffers feed a multiplexer managed by a finite state machine (FSM) that ensures that only complete frames are read out from each link. The frames are stored into a second-level FIFO buffer, before being transmitted into the processor memory via Direct Memory Access (DMA). On the processor, the received data are processed and made accessible for evaluation on a host PC connected via SSH. Control and configuration commands are issued via Advanced eXtensible Interface (AXI) [11] from the command line toward the front-ends and sensors. Each of the four ToASt modules has two links operating at 160 Mbit/s, yielding a data rate of 1.28 Gbit/s. To simulate a high-occupancy scenario, test pulses were injected simultaneously on all ToASt channels, corresponding to 100 % detector occupancy. This occupancy level is significantly higher than expected during experiment operation, however demonstrates stable readout behavior. The prototype was operated continuously over several days. For each acquisition, the data were checked for bit errors. No transmission errors were observed, confirming stable operation at full throughput. These results verify the robustness and scalability of the readout chain, demonstrating that the system can reliably handle the data rates expected in the $\overline{\text{P}}$ANDA experiment. The successful performance indicates suitability for integration into larger and more complex detector setups in the $\overline{\text{P}}$ANDA experiment.

2.2 Module Data Concentrator ASIC design and status

The MDC-ASIC implements the central data aggregation and control functions between the front-end chips and the off-detector electronics. It is integrated directly on the sensor module within the active volume and operates in the same radiation environment as the front-end ToASt-ASICs. Critical components are protected against Single Event Upsets (SEUs) based on including Triple Modular Redundancy (TMR). Developed in the same 110 nm CMOS technology as the ToASt-ASIC, the MDC will be produced in the same engineering runs. It handles key tasks including data readout, decoding, performing time-ordering and multiplexing, and combining data streams. An efficient zero-suppression algorithm minimizes data volume transmitted to the off-detector electronics. The MDC interfaces the detector module to the DAQ system via two parallel high-speed serial links based on lpGBT link at 320 MB/s. A programmable logic block generates test pulses for gain calibration and S-curve based noise measurement, enabling module-level characterization, precise timing, and accurate charge measurement without external equipment. The final version of the MDC chip submitted to the foundry for production is shown in figure 3.

The MDC features 16 input channels and is compatible with all detector module geometries, with additional spare connections for flexible configurations. The chip has been designed with a power consumption of 72 mW at 1.2 V and 333 MHz, making it suitable for modules with limited cooling. Its compact die ($< 4 \times 4$ mm^2) minimizes the material budget in the active area of the detector, maintaining a low logic occupancy of 3.6 %. Each of the four clock drivers features individual phase adjustment with 150 ps resolution over a 6 ns range, reducing module-level timing issues and simplifying high-density flex-PCB routing for easier integration. The produced ASIC has been delivered and characterization and testing are scheduled in the following months (at the time of writing).

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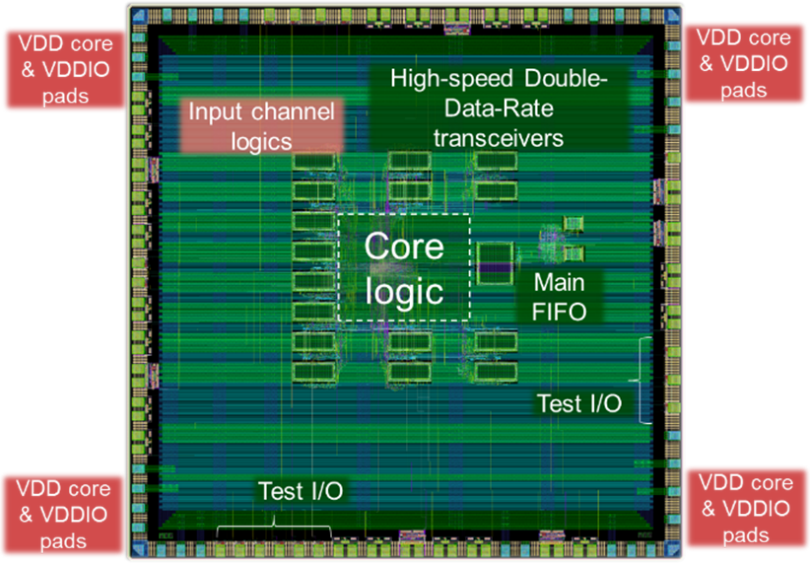

Figure 3. Final design of the MDC-ASIC submitted for production. The final die dimensions including the seal-ring are $3.38 \times 3.38\,\mathrm{mm}^2$ [4].

3 Common readout electronics for $\overline{\mathrm{P}}$ANDA

The back-end electronics card for the MVD readout chain was designed to meet the requirements of the readout architecture while also enabling integration with the DAQ systems of other $\overline{\mathrm{P}}$ANDA sub-detectors. As these are based on the MicroTCA (µTCA) standard, the Advanced Mezzanine Card (AMC) standard was chosen as the design basis. Through an ATCA carrier card, compatibility with ATCA-systems can be achieved, while stand-alone operation is supported via standard interfaces such as ETH. As a result, the card is also applicable for a broad range of experiments employing DAQ systems based on the mentioned standards. The detailed hardware architecture of the platform has already been described in previous work [3] while key design aspects and recent developments are summarized in this contribution. The 3D rendering of the complete layout is shown in figure 4.

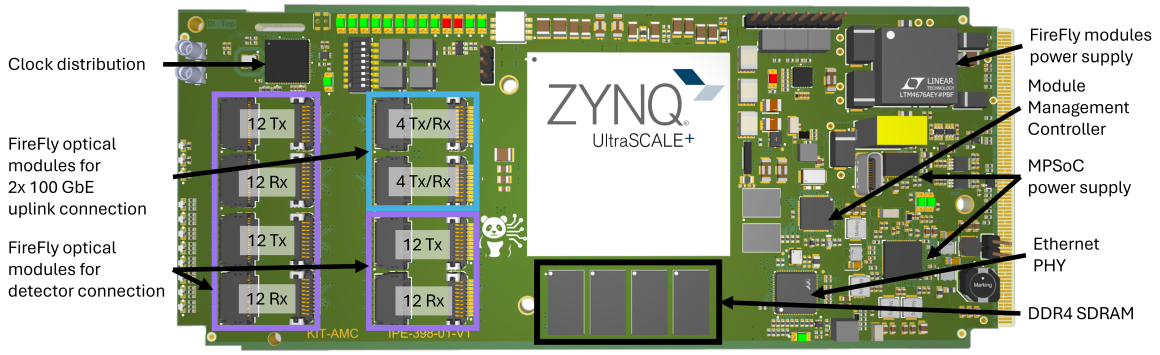

Figure 4. 3D rendering of the final layout of the Common DAQ Platform and its main components.

The platform design is based on the AMD-Xilinx XCZU11EG Zynq Ultrascale+ Multi-Processor System-on-Chip (MPSoC). The MPSoC combines FPGA fabric with embedded processors, enabling the implementation of powerful signal-processing algorithms, such as tracking or feature extraction,

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a well as deployment of data-quality monitoring and slow-control on the device. Commands, configuration, and readout data are transmitted to and from the detectors via optical lpGBT links. The platform provides two 100 GbE uplinks to a Commercial Off-The-Shelf (COTS) computing node, offering a scalable and economical approach to data processing in high-energy physics (HEP) experiments. The optical links are implemented as Samtec FireFly optical modules [12], providing high-density optical connectivity within a compact footprint. For local data buffering and intermediate processing, a 4 GB, 64-bit DDR4 memory is connected to the processor. Additional backplane interfaces include PCIe Gen2 and a 4-GTY link for full-mesh connectivity between AMCs, as well as SATA, and GbE for timing and slow-control distribution. The Printed Circuit Board (PCB) design was optimized for high-speed signal integrity. A low-loss material with a low dielectric constant was required. Therefore, Megtron 6 [13] was selected, combining the required high-bandwidth performance with high-density interconnection capability. The stack-up consists of 24 metal layers. The routing strategy was optimized for impedance control and minimal skew across differential pairs and multi-gigabit serial lanes. To tackle the challenge of high-density interconnection, tailored via types and geometries were employed to balance manufacturing complexity with signal performance. A prototype AMC was assembled to evaluate the power supply architecture and verify the mechanical form factor of the card. The design employs the TPS650864 and TPS543C20 [14, 15] from Texas Instruments for the SoC and peripherals, and the LTM4676 [16] from Analog Devices for the high-speed optical links. Tests verified voltage levels and correct power-sequencing, providing feedback to the final layout. At the time of writing, the production and tests of the finalized hardware are scheduled for the following months. Further work will focus on the deployment of the full MVD readout chain with the finalized readout card.

4 Conclusion and outlook

In this work, a scalable readout concept for the $\overline{\text{P}}$ANDA MVD has been presented and evaluated by continuously expanding on a established prototype implementation. The extension of the MVD readout chain prototype to multiple detector modules demonstrated the scalability of the architecture, while prolonged operation at high data throughput showed stable and error-free system behavior. These results support the suitability of the proposed DAQ concept for a scalable MVD readout concept and indicate that the architecture meets the experiment's data rate and reliability requirements. The prototype establishes a solid foundation for the incremental integration of hardware components and firmware in subsequent development phases. Recent progress in the design and production of the MDC ASIC and back-end readout electronics design represent an important step towards the finalization of the complete MVD readout chain. Future work will focus on deploying the full system, comprising both the produced MDC ASIC and the finalized off-detector back-end readout card. This system will be used as the readout for a large-scale beam test at GSI in 2027. Beyond the $\overline{\text{P}}$ANDA experiment, the back-end electronics card is conceived as a flexible and modular platform. Its compatibility with µTCA and ATCA infrastructures, as well as standalone operation, provides a basis for broader applicability in detector readout systems for other physics experiments and related applications.

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