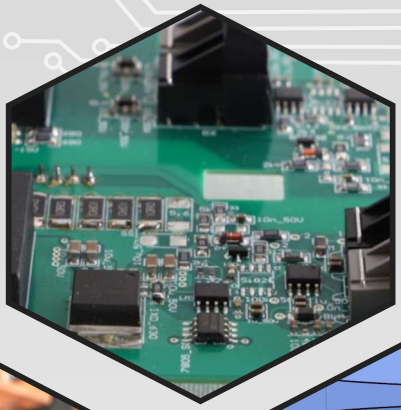

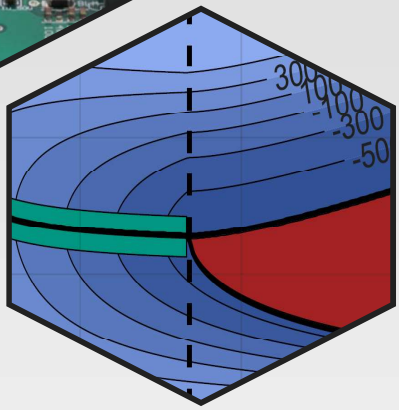

Modeling, Design and Operation of a High Power Dual Active Bridge with Focus on Parasitic Effects

Fabian Sommer

Karlsruher Institut für Technologie

Elektrotechnisches Institut

Modeling, Design and Operation of a High Power Dual Active Bridge with Focus on Parasitic Effects

Zur Erlangung des akademischen Grades eines

Doktors der Ingenieurwissenschaften (Dr.-Ing.)

von der KIT-Fakultät für
Elektrotechnik und Informationstechnik
des Karlsruher Instituts für Technologie (KIT)
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M.Sc. Fabian Sommer

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Hauptreferent: Prof. Dr.-Ing. Marc Hiller
Korreferent: Prof. Dr.-Ing. Gerd Griepentrog
(TU Darmstadt)

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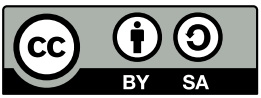

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Vorwort

Die vorliegende Arbeit entstand während meiner Tätigkeit als wissenschaftlicher Mitarbeiter am Elektrotechnischen Institut (ETI) des Karlsruher Institut für Technologie (KIT). Der Fokus meiner Forschungsarbeit lag auf der Erforschung möglicher Komponenten für eine kosten- und wirkungsgradkompetitive Integration von Niederspannungs-DC-Netzen. In diesem Rahmen wurde die potentialtrennende Stufe in Form eines DC/DC-Wandlers untersucht.

Die erfolgreiche Fertigstellung meiner Forschungsarbeit wäre ohne vielfältige Unterstützung im privaten und beruflichen Umfeld nicht möglich gewesen, weshalb ich mich bei allen beteiligten Personen herzlich bedanken möchte.

Im Besonderen gilt mein Dank meinem Doktorvater Prof. Dr.-Ing. Marc Hiller, der mir die Möglichkeit gegeben hat, mit großer Freiheit und fokussiert zu forschen und meine Dissertation anzufertigen. Für die fachliche und persönliche Unterstützung sowie das mir entgegengebrachte Vertrauen möchte ich mich im Besonderen bedanken.

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Ein großes Dankeschön richte ich an meine Teammitglieder Tobias und Nikolas. Ohne eure tatkräftige Unterstützung und euer kritisches Feedback wären viele Ideen nicht umsetzbar gewesen.

Auch gilt allen Studierenden mein Dank, die mit ihren Abschlussarbeiten einen wichtigen Beitrag zu dieser Dissertation geleistet haben.

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Zudem möchte ich meiner Freundin Larissa für ihr Verständnis, ihre Unterstützung und ihren Rückhalt danken.

Fabian Sommer

Achern, im März 2026

Kurzfassung

Die zunehmende Durchdringung des elektrischen Energiesystems mit erneuerbaren Erzeugern wie Photovoltaik und Windkraft sowie die wachsende Verbreitung stationärer Speichersysteme und von Ladeinfrastruktur für die Elektromobilität führen zu einer Verschiebung hin zu dezentralen Energiequellen und -senken mit intrinsischen DC-Schnittstellen. Dadurch geraten DC-Netze als Alternative oder Ergänzung zu klassischen AC-Verteilnetzen zunehmend in den Fokus. Im Vergleich zu AC-Netzen ermöglichen sie geringere Wandlungsverluste und eine höhere Effizienz beim Verbinden mehrerer DC-gekoppelter Quellen und Speichersysteme, da sich die Anzahl notwendiger Wandlerstufen reduziert. Um diese Vorteile technisch nutzbar zu machen, ist jedoch die Entwicklung leistungsfähiger und effizienter DC/DC-Wandler unverzichtbar, insbesondere im Leistungsbereich mehrerer hundert kW, wie er in modernen DC-Infrastrukturen typisch ist.
Diese Dissertation befasst sich mit der Modellierung, dem Design und dem Betrieb einer galvanisch getrennten Dual Active Bridge (DAB) mit einer Nennleistung von 500 kW unter Berücksichtigung parasitärer Effekte für zukünftige Hochleistungsanwendungen im Niederspannungsnetz. Dazu werden zunächst die theoretischen Grundlagen vorgestellt. Darauf aufbauend wird ein Regelkonzept für jeweils eine Leistungs- und Spannungsregelung hergeleitet. Der Hauptteil der Arbeit untersucht die verschiedenen parasitären Effekte und ihren Einfluss auf das Betriebsverhalten der DAB. Im besonderen der resonante Kommutierungsvorgang bei entlastetem Schalten wird modelliert und detailliert beschrieben. Aufbauend auf diesem Modellierungansatz werden Verfahren vorgestellt, mit denen sich diese Effekte zur Effizienzsteigerung nutzen und das dynamische Verhalten verbessern lassen. Abschließend wird die entwickelte Theorie anhand eines Prototyps voller Leistung experimentell validiert.

Abstract

The increasing penetration of the electrical energy system with renewable generators such as photovoltaic and wind power, together with the growing deployment of stationary storage systems and charging infrastructure for electromobility, is driving a shift toward decentralized energy sources and sinks featuring intrinsic DC interfaces. As a result, DC grids are gaining attention as an alternative or complement to traditional AC distribution grids. Compared with AC systems, they offer lower conversion losses and higher efficiency when interconnecting multiple DC-coupled sources and storage systems, primarily due to the reduced number of required conversion stages. To fully exploit these advantages, however, the development of high-performance and efficient DC/DC converters is essential, particularly in the power range of several hundred kilowatts, as commonly found in modern DC infrastructures.
This dissertation addresses the modeling, design, and operation of a galvanically isolated 500 kW Dual Active Bridge (DAB), with specific consideration of parasitic effects relevant to future high-power applications in the low voltage grid. The work starts by introducing the theoretical foundations. Building on this, a control concept for both current and voltage controller is derived. The main part of the dissertation examines various parasitic effects and their impact on the operating behavior of the DAB. In particular, the resonant commutation process for soft switching is modeled and described in detail. Building on that model, methods are presented that exploit these effects to improve efficiency and enhance the dynamic performance of the converter. Finally, the proposed theory is validated experimentally using a full scale hardware prototype.

Contents

Chapter 1

Introduction

This chapter gives a brief introduction to applications of galvanically isolated DC/DC converters with high power in the kW to MW range. Different topologies suitable for these applications are presented, in particular non-resonant topologies represented by the Single Active Bridge (SAB), Dual Active Bridge (DAB) and resonant topologies consisting of the LLC and CLLC converter. This is followed by the structure and goal as well as the scientific contribution of the dissertation.

1.1 DC/DC Converter Applications

Grid Applications

In order to transmit and distribute electrical power efficiently, the energy grid of today is structured with layers corresponding to different tasks. Long distance transmission is achieved using the High Voltage (HV) levels of multiple hundreds of kV while energy distribution and often also the generation is achieved in the Low Voltage (LV) and Medium Voltage (MV) levels. The HV does enable low conduction losses but necessitates advanced isolation and protection whereas LV and to some extend MV reduces the isolation effort and complexity of the protection systems while increasing the conduction losses of the system. This structure leads to a top down energy distribution. Typically, large centralized power plants are generating the electric energy from coal, oil or nuclear fission and the electric energy is then transferred and distributed to industrial and domestic loads. For the most part, this structure is unidirectional by design

and a provision of electrical energy from the distribution grid is not intended. Of course, there are renewable energies such as wind and solar integrated in the distribution grid, however these have no significant influence on the overall power flow in the traditional grid structure. This structure is shown in Fig. 1.1. The increasing shift from a centralized to a decentralized generation from renewable energies such as wind and solar poses a major challenge for this grid structure. On the one hand, a bidirectional power flow must be possible, as there are not only consumers but also prosumers and producers in the distribution grid, and on the other hand, the connection points are increasingly burdened by rising energy consumption and fluctuation due to the electrification of various sectors such as mobility and heating.

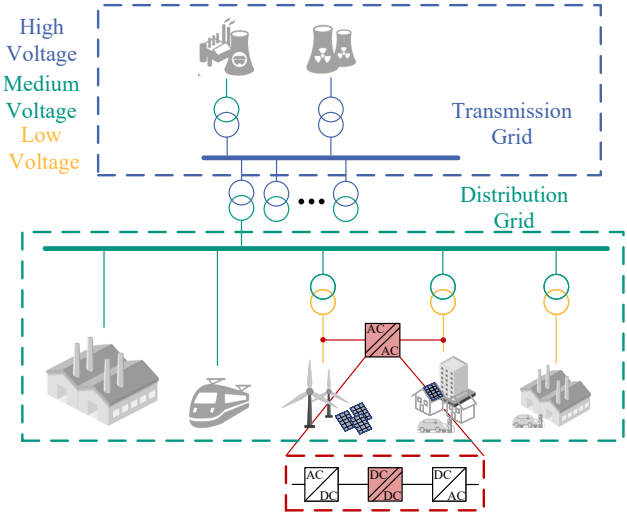


Figure 1.1: Traditional AC grid structure with unidirectional power flow

A possible solution to these challenges is an increased meshing of the distribution grid to prevent the power flow from having to take place via the MV level of the grid as shown in Fig. 1.1 with the red highlighted interconnection. This enables a power flow from areas with a high proportion of generators to an area with a high proportion of loads without further burdening the MV connection points.

Which leads to a reduced stress on both the LV grid and the MV connection point. Such a system must be galvanically isolated as well as controllable in frequency and voltage level due to the possible mismatch of both separate LV grids. A simple solution for this AC/AC grid coupling using a galvanic isolated DC/DC converter is shown in Fig. 1.1. The DC/DC converter in this examples enables more controllability as well as a galvanic isolation with reduced cost in the transformer due to a Medium Frequency Transformer (MFT) [1].
Another solution for the integration of decentralized energy producers are DC microgrids replacing the existing LV sections of the distribution grid as shown in Fig. 1.2 [2]. Since most of the decentralized renewable energy sources and storages often have a DC output, a DC grid can reduce losses caused by multiple steps of the power conversion process. For the traditional AC grid, a AC/DC stage is necessary whereas for the DC grid only a DC/DC stage or no stage at all is required [3, 4]. Additionally, DC microgrids have various advantages such as increased stability, reliability and controlability of the distribution grid during power blackout or grid disturbances. For them there is no need for a reactive power control [5] and the utilization of the AC connection points can be increased [6]. In order to connect these DC microgrids to the AC distribution grid, a Solid State Transformer (SST) can be used for the AC/DC conversion and galvanic isolation as well as the voltage transformation [7]. However, due to safety reasons, a galvanic isolation is still necessary within the DC grid, hence galvanic isolated DC/DC converters are crucial for these applications in order to safely operate a DC grid. Additionally, an interconnection of different DC microgrids, using galvanic isolated DC/DC converters, is also possible to further reduce stress on the AC MV distribution grid [8, 9]. However, multiple challenges for DC grids should not be unmentioned, such as the protection and grounding using DC is more difficult compared to AC since no zero crossing can be utilized. Additionally, not enough standardization is currently present to enable full DC microgrids in a larger scale [7].

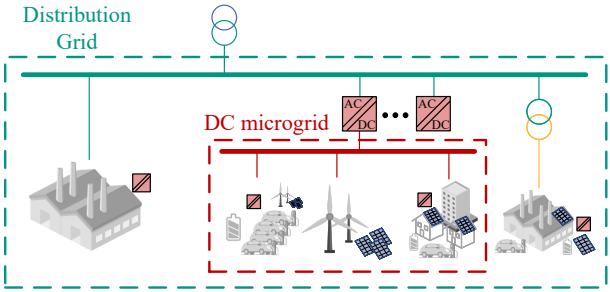


Figure 1.2: Possible distribution grid structure using DC microgrids

Charging Infrastructure

The rapid adoption of Electric Vehicles (EVs) has driven significant advancements in fast charging technology. Fast charging infrastructure must handle high power levels while ensuring efficiency, safety, and reliability. Traditionally, charging parks are designed by using an LV AC grid with a connection to the MV distribution grid via a line frequency transformer. Each charging port has its own AC/DC and DC/DC converters. Due to safety reasons a galvanic isolation is required in the IEC 61851 and can be implemented using a galvanic isolated DC/DC converter. The structure is shown in Fig. 1.3 [10]. In order to reduce conversion steps and therefore increase the efficiency of the system, a DC grid is proposed. Additionally, many renewable energy sources (e.g., solar photovoltaic systems and wind power) as well as battery storage inherently generate DC power. A DC grid simplifies their integration, minimizing conversion losses and improving system-level efficiency [10–12]. This DC grid is connected to the AC grid by an AC/DC SST. The resulting topology is shown in Fig. 1.4. The DC/DC converter in this application performs several important functions. First, the voltage transformation and galvanic isolation required by safety standards. Additionally, due to the bidirectional characteristic of both the DC/DC converters and the SST a vehicle-to-grid (V2G) operation is possible, allowing the support of the connected distribution grid by supplying reactive and active power. This way it is evident, that the galvanically isolated DC/DC converter does not only provide advantages for the charging port itself but also for the de-

sign and topology of the whole charging station by reducing component effort and costs.

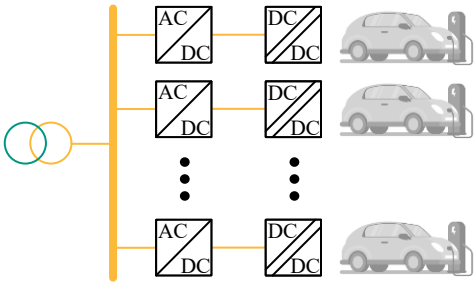


Figure 1.3: Traditional topology of a fast charging station with AC grid and 50/60 Hz transformer

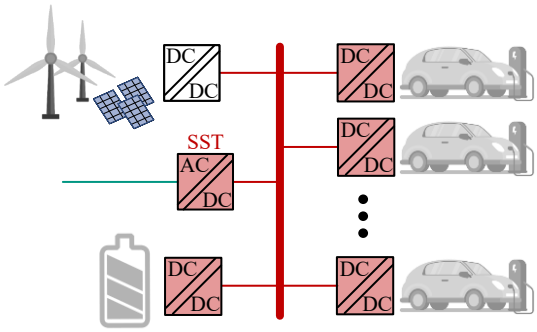


Figure 1.4: Proposed topology of a fast charging station with DC grid, SST and integrated renewable energy sources

Solid State Transformer

For the previously mentioned applications, an SST was introduced as a critical component for AC/AC and AC/DC connection points [13, 14]. Such an SST has the main goal to enable a galvanic isolation and voltage transformation without using traditional line frequency transformer technology. This is achieved by using power electronics in order to increase the operation frequency of the transformer. This enables less material effort due to reduced copper and iron in the transformer. Additionally, the controllability of the system at the connection point can be increased due to the power electronics. This allows to control the voltage levels, reactive power and active power on the AC side independently. Lastly, the flexibility is increased due to the multiport configurations and dnamic reconfiguration of the system. A common AC/DC SST topology is shown in Fig. 1.5. Here, a serial input parallel output AC/DC converter is shown. N amount of cells are connected in series on the AC distribution grid side to generate the required MV, a galvanic isolated DC/DC converter in each of the cells provides a voltage control of the DC link voltage side. The serial interconnection enables a scalability of the voltage level by increasing the amount of cells. On the output side the power can be scaled with the current rating of each cell due to the parallel configuration. In addition to the presented topology, there are many other configurations that can be applied depending on the specific application. However, most concepts share the common feature of a modular, cell-based architecture. It is clear, that the cell design and therefore the galvanic isolating DC/DC converter is a key component of such a system [15]. In order to compete with line frequency transformers and provide substantial advantages, the DC/DC converter must be controllable, highly efficient and small. The typical power rating of each SST cell has to be > 100 kW with medium or low voltage DC links.

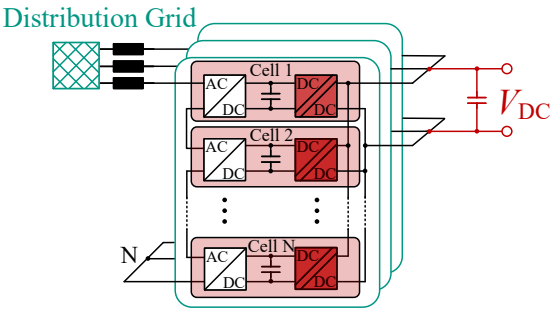


Figure 1.5: Proposed topology of a SST as input serial output parallel AC/DC converter for grid coupling of MV and LV grids

1.2 DC/DC Converter Topologies

Selecting the appropriate galvanically isolated DC/DC converter topology for the presented applications is essential for the efficiency, controllability and component stress. Different applications require different optimizations to ensure maximum performance. However, the most common topologies for high power applications can be divided into two fundamental different groups of converter. The first group of converters are the non-resonant converters. This category of converter is mainly represented by the Single Active Bridge (SAB) and the Dual Active Bridge (DAB). Other topologies are possible but have significant drawbacks at higher power levels which is why they are not further investigated in this work. The second category are the resonant converters with the most common ones beeing the LLC converter and CLLC converter. Even though many topologies are possible and the resonant circuit in particular has great variations, only the two mentioned above will be considered in this work, as they provide a good impression of the strengths and weaknesses of resonant inverters.

Non-resonant Converter

The most prominent topologies for non-resonant DC/DC converters are the SAB and the DAB shown in Fig. 1.6 and Fig. 1.7 respectively. Both topologies have

a low requirement for passive components as the transformer can be used for galvanic isolation and as the inductance and therefore no other passive components are required in the AC circuit. The SAB features a single-side full bridge combined with a diode rectifier. The main advantage of this topology is its simple control scheme using a phase shifted full bridge, making it easy to implement. Additionally, it can achieve high efficiency due to soft switching and a low amount of switches. However, its operational flexibility is more limited compared to the DAB, since no unity and boost operation is possible and the converter is unidirectional. In contrast, the DAB enables bidirectional power transfer, unity as well as buck and boost operation by employing phase-shift modulation between the primary and secondary full bridges. The transfer function for the most common modulation scheme Single Phase Shift (SPS) of the DAB is shown in (1.1). Using SPS, the DAB operates as a current source and controls the output current and hence the output power. However, ensuring soft switching operation is not trivial and a complex control is necessary to ensure high efficiency especially under partial load conditions. Additionally, high circulating currents are present for buck and boost operation. The basic operation principle and a more in detail analysis of the advantages and disadvantages of the DAB are given in chapter 2. For very high power operation, a three phase DAB might be beneficial to decrease the current stress for each switch and reduce the voltage ripple for the DC link capacitors. An example of a three phase DAB is shown in Fig. 1.8. However, the control for a three phase DAB is more complex and ensuring high efficiency is more challenging since achieving soft switching for all switching events is difficult in buck and boost operation.

$$P_{\mathrm{SPS}}(\varphi) = \frac{V_{\mathrm{DC1}} \cdot V'_{\mathrm{DC2}} \cdot \varphi(\pi - |\varphi|)}{2\pi^2 f_{\mathrm{sw}} L_\sigma} \tag{1.1}$$

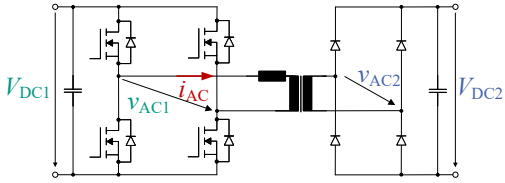


Figure 1.6: Equivalent Ciruit Diagram of a Single Active Bridge (SAB)

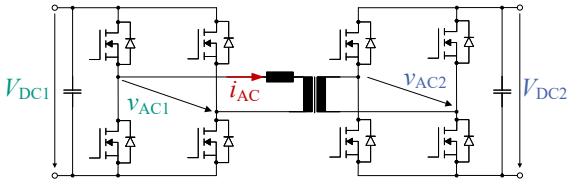


Figure 1.7: Equivalent Ciruit Diagram of a single phase Dual Active Bridge (DAB)

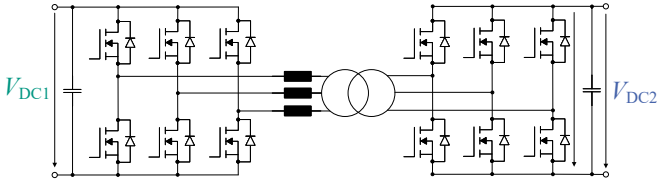


Figure 1.8: Equivalent Ciruit Diagram of a three phase Dual Active Bridge (DAB)

Resonant Converter

In contrast to non-resonant converters, resonant topologies leverage soft switching techniques to reduce switching losses and electromagnetic interference. One of the most prominent resonant converters is the LLC resonant converter shown in Fig. 1.9, which utilizes a resonant tank consisting of an inductor and a ca-

pacitor as well as the transformer with its stray and main inductance. The LLC resonant converter achieves soft switching inherently and due to the sinusoidal waveform it does provide low current stress on the transformer. However, a major challenge of the LLC resonant converter is that it has a voltage transfer function which is dependent on the load characteristics. This means that depending on the load the transfer functions changes and increases complexity of the design and control of the LLC. Additionally, the voltage is regulated by changing the switching frequency f_{sw} of the converter which is limited due to design of the passive components and the maximum allowable losses. In addition the ratio m between stray L_σ and main inductance L_{m} of the transformer in (1.6) influences the transfer function of the LLC converter. To achieve a wide operation range for the LLC, a ratio of m between 1..10 is necessary which results in high magnetizing current i_{m} (shown in Fig. 1.11) compared to the load current and reduces the efficiency of the transformer. The transfer function is shown in (1.2) with the impact of m in Fig. 1.12 (a) and the equivalent load resistance R_{L} in Fig. 1.12 (b). For both parameters, a significant impact is observable which reduces the possible operation range of the converter and necessitates a challenging control structure and a complex design of the AC circuit. Additionally, the resonant capacitances have to handle the full load current, which reduces the lifetime and necessitates expensive special high frequency and high current capacitors. To achieve bidirectional operation, the LLC converter can be extended for an additional L and C and a second full bridge shown in Fig. 1.10. The main operation principle as well as advantages and disadvantages remains the same but a symmetrical bidirectional operation is possible.

$$G_{\mathrm{LLC}}(f) = \frac{V'_{\mathrm{DC2}}}{V_{\mathrm{DC1}}} = \frac{f_{\mathrm{x}}^2\,(m-1)}{\sqrt{(m f_{\mathrm{x}}^2 - 1)^2 + f_{\mathrm{x}}^2 (f_{\mathrm{x}}^2 - 1)^2 (m-1)^2 Q^2}} \tag{1.2}$$

with

$$Q = \frac{\sqrt{L_\sigma / C}}{R_{\mathrm{L}}} \tag{1.3}$$

$$f_{\mathrm{res}} = \frac{1}{2 \cdot \pi \sqrt{C L_\sigma}} \tag{1.4}$$

$$f_{\mathrm{x}} = \frac{f_{\mathrm{sw}}}{f_{\mathrm{res}}} \tag{1.5}$$

$$m = \frac{L_{\sigma} + L_{\mathrm{m}}}{L_{\sigma}} \tag{1.6}$$

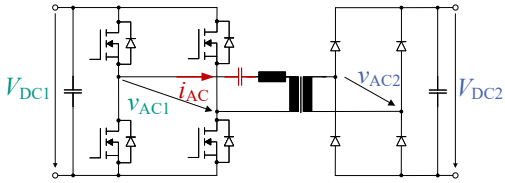


Figure 1.9: Equivalent Ciruit Diagram of a LLC resonant converter

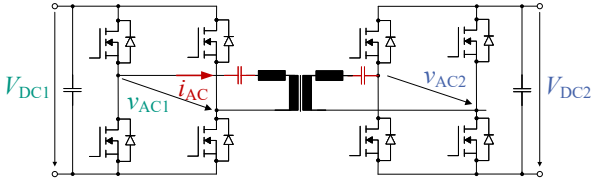


Figure 1.10: Equivalent Ciruit Diagram of a CLLC resonant converter

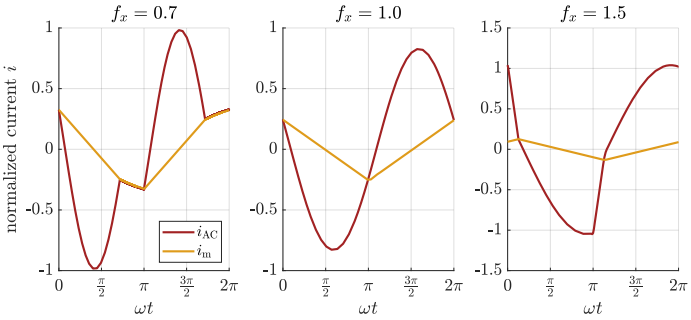


Figure 1.11: LLC current waveform for operation below, in and over resonant frequency

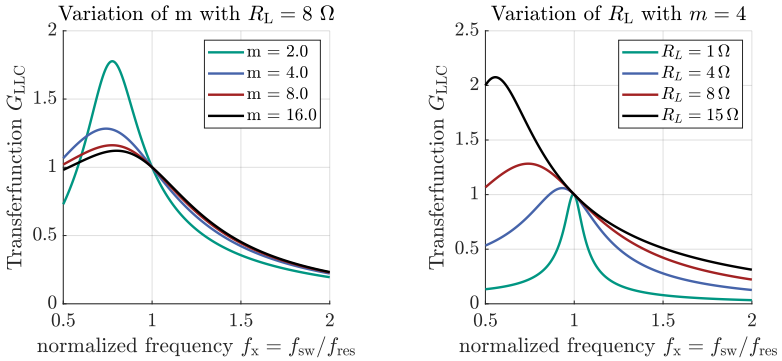


Figure 1.12: LLC transfer function for (a) variation of the transformer characteristic m and $R_L = 8\ \Omega$ (b) variation of the load characteristics R_L and $m = 4$

The presented parameters of both resonant and non-resonant topologies are summarized in table 1.1. In this dissertation a single phase Dual Active Bridge (DAB) is further investigated since this topology is suitable for all presented applications and has the lowest component effort while maintaining high efficiency, controllability, wide operation range and bidirectional operation. Additionally, no extra passive components are necessary which makes this topology cheaper and more reliable compared to the resonant converters.

1.3 Structure and Goal of this Dissertation

In this work, a DAB is investigated as a possible galvanically isolated DC/DC converter. The focus is on evaluating its suitability for the aforementioned applications, particularly regarding the feasibility of achieving high power levels at low voltage. The investigation aims to identify the advantages and disadvantages of the DAB topology under these conditions and to give a comprehensive overview about the challenges which occur at high power levels in particular. To match the target applications, the voltage range is set between 500 V and 800 V DC with a transformer turn ratio of 1. This configuration enables the representation of ultra-fast charging systems with 800 V architectures, as well as applications in SSTs with input parallel output serial configurations. The target power level is set to 500 kW, which allows the reduction of the number of cells in MW-scale SSTs while enabling ultra-fast charging with a single converter. Additionally, these ratings represent the power level of the existing distribution transformers present in the low voltage grid. The switching frequency is set to $f_{\mathrm{sw}} = 20$ kHz. This frequency is chosen to ensure operation outside the audible

Table 1.1: Comparison of different galvanic isolated DC/DC converter topologies suitable for high power applications

	SAB	DAB	LLC	CLLC
Bidirectional	-	+	-	+
Passive Components	++	++	0	-
Active Components	++	0	++	0
Output voltage quality	-	++	+	+
Voltage range	only buck	full operation range	limited range	limited range
Soft Switching	not ensured	not ensured	inherent	inherent

spectrum, making the converter suitable for deployment in densely populated areas. Additionally, the selected frequency allows the use of ferrite as the core material, which reduces both the transformer costs and core losses. This dissertation is structured as follows:

Chapter 2 presents the ideal operation of the DAB converter without considering non-ideal effects. It derives the relationship between key operational parameters, such as the inductance and its influence on the operating behavior. The two primary modulation schemes, Single Phase Shift (SPS) and Triangular Current Modulation (TCM), are derived in detail. A comparison of both SPS and TCM are presented to evaluate the advantages and disadvantages of both modulation schemes. Additionally, an overview of other modulation schemes found in the literature is provided, offering a comprehensive understanding of possible control methods.

The control system of the DAB is introduced in chapter 3. Based on the ideal model, the control design aims to achieve maximum dynamic performance without exceeding system limits. Both, the power and voltage control loops are presented. The control scheme features a dynamic setpoint limitation, enabling full coverage of the operating range without sacrificing dynamic performance. Experimental results show, that improving the DAB model by considering parasitic effects, increases control performance.

In chapter 4, the non-ideal behavior of the DAB is analyzed. Parasitic effects such as the transformer's magnetizing inductance and winding resistance are introduced and their influence investigated. Special focus is placed on the resonant commutation process of the semiconductors, which significantly impacts efficiency and operating behavior especially for high power DABs. Based on the commutation model, an efficiency improvement method for TCM called Circular Current Injection (CCI) is presented. Additionally, a linearization method for the DAB's transfer characteristic is derived. The influence of the transformer's high-frequency behavior is modeled, and an optimized winding design is proposed based on this model.

The experimental setup is presented in chapter 5, including the hardware implementation of the DAB converter and the measurement equipment. The design choices for the testbench and the specifications of the components are

discussed.

In chapter 6 the theoretical findings from the previous chapters are validated through experimental measurements. The experimental results confirm the predicted behavior of the DAB, including the impact of non-ideal effects and the performance improvements achieved by the proposed methods.

The final chapter summarizes the key findings of the dissertation.

1.4 Scientific Contribution

The primary contributions of this dissertation are as follows:

Demonstration of High Power Dual Active Bridge (DAB) Operation

This work successfully demonstrates that a DAB converter is capable of operating at power levels up to 500 kW in low-voltage applications while maintaining a high switching frequency (> 10 kHz) necessary for the reduction of passive components. This power level significantly exceeds the power range typically associated with DAB converters in the literature which is typically below 100 kW [12, 16–20]. The challenges associated with high-power low-voltage operation are systematically analyzed. A full-scale 500 kW DAB prototype is designed, built, and experimentally validated. The prototype fulfills the requirements of the targeted applications, such as DC grids, solid-state transformers, and DC fast charging systems. The experimental results confirm that the DAB topology is a viable solution for these applications, proving that the converter architecture is suitable for high-power low-voltage systems when the identified commutation effects are properly considered in the design phase.

Accurate Modeling of Resonant Commutation Effects

A novel and detailed model of the resonant commutation process for the DAB converter is developed. The model captures the non-ideal switching behavior and accurately reflects the influence of resonant commutation on the converter operation. It is shown that the commutation effects become increasingly significant with rising power levels and cannot be neglected in high-power applications,

unlike at lower power ranges where such effects are typically disregarded due to the minimal effect at low power operation. Even if the model presented is only applied for a DAB, it can also be adapted to other soft switching topologies such as the LLC/CLLC resonant converter and therefore proposes a versatile approach to predict the behavior of the DAB.

Impact Analysis of Resonant Commutation on High-Power DAB Operation

The dissertation presents a comprehensive analysis of how resonant commutation affects the efficiency of the DAB converter. It is demonstrated that the increasing influence of the resonant commutation process does alternate the efficiency significantly and does necessitates an adaption in typically applied modulation schemes to achieve highest efficiency possible. Additionally, the transfer characteristic is investigated and the nonlinear behavior compensated to achieve maximum dynamic for the controller of the DAB.

These contributions represent a significant step toward the application of DAB converters in emerging high-power DC systems, addressing both theoretical and practical challenges associated with their operation at large power levels.

Chapter 2

Steady State Model of a Dual Active Bridge with ideal Conditions

This chapter provides a comprehensive examination of the Dual Active Bridge (DAB) and its operational principles. An ideal DAB model in steady-state operation is presented. Relevant variables of the DAB are defined, and a fundamental framework is introduced to analyze various control and modulation schemes. The most common modulation schemes, Single Phase Shift (SPS) and Triangular Current Modulation (TCM), are presented and compared in terms of performance concerning the relevant variables for a DAB. Furthermore, an overview of more advanced modulation schemes is presented and analyzed in terms of their respective advantages and limitations.

2.1 Ideal DAB Model

In chapter 1, the DAB converter emerges as the most promising topology for the given applications, exhibiting superior characteristics in terms of power density, efficiency and flexibility. The DAB configuration comprises two voltage source full bridges interconnected via a medium or high frequency transformer (MFT/HFT). This transformer incorporates elements such as a stray inductance L_σ, the transformer ratio n, and the main inductance L_m, thereby operating as an inductive load bridging the two capacitive voltage sources. The resulting equiv-

alent circuit diagram is illustrated in Fig. 2.1. When considering solely the ideal lossless scenario, the DAB can be simplified to the model depicted in Fig. 2.2, wherein the full bridges are represented as ideal rectangular AC voltage sources and the transformer is only modeled by its stray inductances.

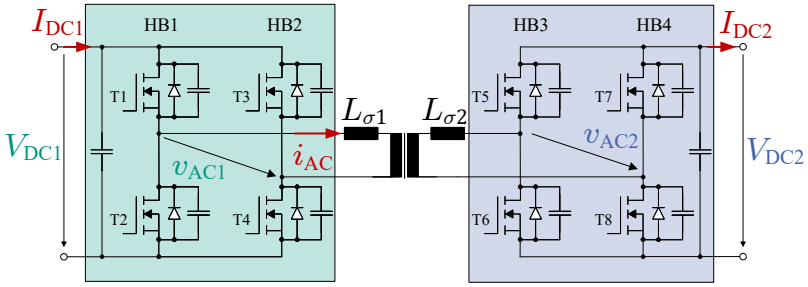


Figure 2.1: Equivalent circuit diagram of a Dual Active Bridge (DAB) Converter

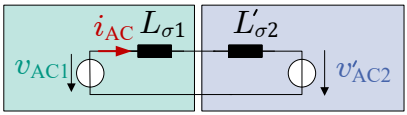


Figure 2.2: Lossless DAB model

For this ideal lossless model the following simplifications are considered:

1. all losses are neglected,
2. the voltage sources $v_{AC1/2}$ have perfectly rectangular waveforms (i.e. no switching transients and infinite fast commutation),
3. the transformer main inductance L_m is infinitely large,
4. no transformer winding and coupling capacitances are considered.

2.1.1 Power Flow and Steady State operation

Using the Full Bridge (FB) converter configuration the AC voltages v_{AC1} can provide three voltage levels. Similarly to v_{AC1}, v_{AC2} can also provide three voltage levels:

$$v_{AC1} = \begin{cases} +V_{DC1} & \text{Case 1: T1, T4 on} \\ 0 & \text{Case 2: T1, T3 on} \\ 0 & \text{Case 3: T2, T4 on} \\ -V_{DC1} & \text{Case 4: T2, T3 on} \end{cases} \tag{2.1}$$

The voltage difference between v_{AC1} and v_{AC2} is used to calculate the inductor voltage v_L in (2.2) and consequently the AC current i_{AC} in (2.3). Steady state conditions are attained only when the following condition holds true for the AC current: $i_L(t_0) = i_L(t_0 + T)$. Additionally, the average voltage at the transformer has to be zero to avoid saturation. Consequently, this results in an average AC voltage level $\bar{v}_{AC1} = \bar{v}_{AC2} = 0$, effectively yielding a zero voltage average.

$$v_L = v_{AC1} - v'_{AC2} \tag{2.2}$$

$$i_{AC}(t) = i_{AC}(t_0) + \frac{1}{(L_{\sigma 1} + L'_{\sigma 2})} \int_{t_0}^{t} v_{AC1} - v'_{AC2} \mathrm{d}t \tag{2.3}$$

The resulting instantaneous power P can be calculated according to (2.4) and (2.5). Integrating $p_{1/2}(t)$ yields the average power over one period, with a duration of T, denoted as P and expressed in (2.6). Under the assumption of a lossless DAB converter, the average powers are equal, thus, $P_1 = -P_2$.

$$p_1(t) = v_{AC1}(t) \cdot i_{AC}(t) \tag{2.4}$$

$$p_2(t) = v'_{AC2}(t) \cdot i_{AC}(t) \tag{2.5}$$

$$P_{1/2} = \frac{1}{T} \int_{t_0}^{t_0+T} p_{1/2}(t) \mathrm{d}t \tag{2.6}$$

As discussed previously, maintaining a steady state necessitates both v_{AC1} and v_{AC2} to have an average value of zero. Consequently, unlike conventional converters, the average output voltage does not serve as a direct control variable. In the case of the DAB, phase shifts between the half bridges (HBs) 1..4 are manipulated to regulate the power flow and current waveform of i_{AC}. Three phase shift angles, correlating to three degrees of freedom, can be defined (cf. Fig. 2.3):

1. $\varphi \in [-\pi; \pi]$: Outer phase shift between the fundamental frequency component of v_{AC1} and v_{AC2},
2. $\delta_1 \in [0; \pi]$: Inner phase shift of v_{AC1} between HB1 and HB2,
3. $\delta_2 \in [0; \pi]$: Inner phase shift of v_{AC2} between HB3 and HB4.

Here, $\delta_{1/2} = 0$ corresponds to the maximum achievable RMS voltage $v_{AC} = V_{DC}$, while $\delta_{1/2} = \pi$ corresponds to the minimum achievable RMS voltage $v_{AC} = 0$.

2.1.2 Modulation

The transferred power of the DAB, denoted as $P(\varphi, \delta_1, \delta_2)$, is a function of the three phase shift angles (assuming constant switching frequency f_{sw}). This results in multiple triplets $[\varphi, \delta_1, \delta_2]$ that achieve equal power levels with different AC voltages $v_{AC1/2}$ and AC current i_{AC} waveforms. Consequently, various modulation strategies can be employed to optimize different aspects such as the minimum switching current $\hat{i}_{AC}$, conduction losses and therefore the RMS current i_{rms}, soft-switching capability, or overall power losses P_v. The two most commonly utilized modulation schemes, Single Phase Shift (SPS) and Triangular Current Modulation (TCM), are presented in this section and further compared in terms of their characteristics in Section 2.2. Additionally, an overview of more advanced modulation schemes is provided.

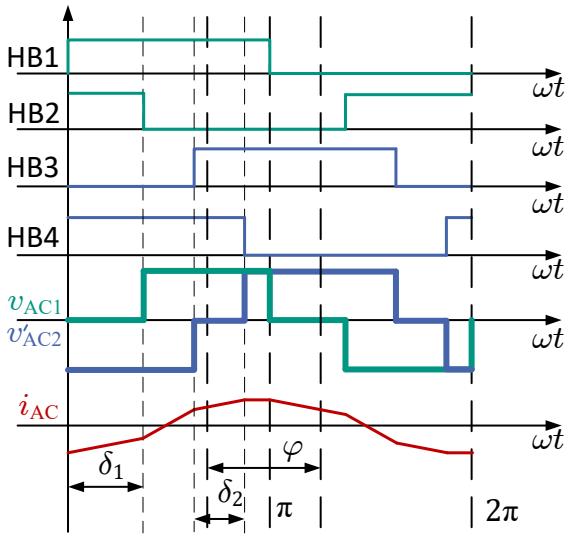


Figure 2.3: Phase shift definition with arbitrary current waveform

Single Phase Shift (SPS) Modulation

SPS modulation was initially introduced in [21]. For SPS modulation, only φ is utilized to control the power flow of the converter, represented as $P(\varphi, \delta_1 = 0, \delta_2 = 0)$. This approach reduces modulation efforts, defining it as the simplest modulation scheme. With $\delta_{1/2} = 0$, the AC voltages $v_{AC1}(t)$ and $v_{AC2}(t)$ are equal to $\pm V_{DC1}$ and $\pm V_{DC2}$ respectively. Hence, no free-wheeling states are possible. The resulting waveforms are illustrated in Fig. 2.4. Due to its simplicity, SPS finds widespread usage [22], albeit exhibiting significantly poorer performance in terms of RMS current and soft switching operation compared to other modulation schemes, particularly in buck and boost operations.
For steady state operation, ensuring the DC bias of i_{AC} equal to zero is crucial to prevent saturation within the transformer core. Hence, (2.3) can be employed to compute the starting current $i_{AC,0}$ such that the DC bias is nullified. The resulting current can be calculated in (2.7).

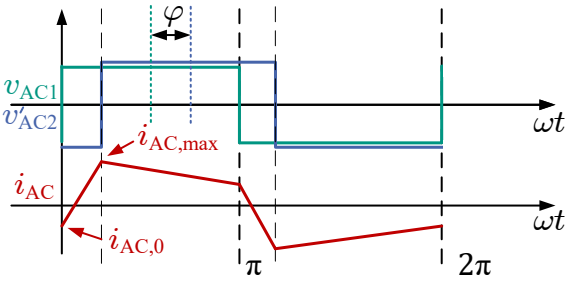


Figure 2.4: Single Phase Shift (SPS) modulation voltage v_{AC} and current i_{AC}

$$i_{AC,0} = \frac{\pi(V'_{DC2} - V_{DC1}) - 2\varphi V'_{DC2}}{4\pi f_{sw} L_\sigma} \tag{2.7}$$

By utilizing (2.6) and (2.7), the transferred power in SPS modulation can be computed, dependent solely on the phase shift φ. If the DC voltages V_{DC1}, V_{DC2}, the switching frequency f_{sw}, and the leakage inductance $L_\sigma = L_{\sigma 1} + L'_{\sigma 2}$ remain constant, the maximum power $P_{SPS,max}$ occurs at $\pm\frac{\pi}{2}$ and can be determined according to (2.9). Here, a positive phase shift $\varphi > 0$ corresponds to a positive power transfer $P_{SPS} > 0$, while a negative phase shift $\varphi < 0$ yields a negative power transfer $P_{SPS} < 0$ (cf. Fig. 2.1). The resulting transfer characteristic is illustrated in Fig. 2.5.

$$P_{SPS}(\varphi) = \frac{V_{DC1} \cdot V'_{DC2} \cdot \varphi(\pi - |\varphi|)}{2\pi^2 f_{sw} L_\sigma} \tag{2.8}$$

$$P_{SPS,max}(\pm\frac{\pi}{2}) = \pm\frac{V_{DC1} \cdot V'_{DC2}}{8 L_\sigma f_{sw}} \tag{2.9}$$

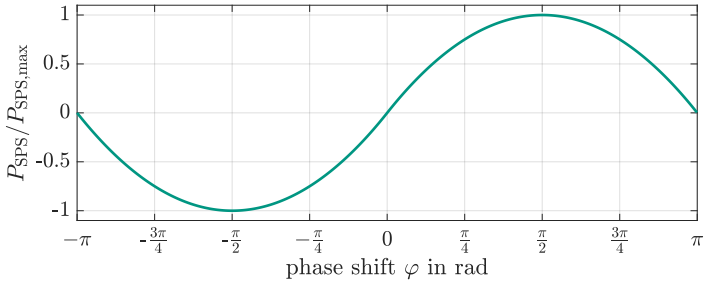


Figure 2.5: Transfer characteristic of the DAB for SPS modulation

To calculate the necessary phase shift $\varphi(P_{\mathrm{SPS}})$, (2.8) can be rearranged to (2.10).

$$\varphi(P_{\mathrm{SPS}}) = \mathrm{sgn}(P_{\mathrm{SPS}})\frac{\pi}{2}\left(1-\sqrt{1-\frac{8L_\sigma f_{\mathrm{sw}}|P_{\mathrm{SPS}}|}{V_{\mathrm{DC1}}\cdot V'_{\mathrm{DC2}}}}\right) \tag{2.10}$$

The maximum AC current $\hat{i}_{\mathrm{AC}}$ is an important design aspect for the DAB and will be further discussed in Section 2.2. For SPS modulation it can be calculated according to (2.11).

$$\hat{i}_{\mathrm{AC,SPS}} = \begin{cases} \dfrac{V'_{\mathrm{DC2}} - V_{\mathrm{DC1}}\sqrt{1-|P_{\mathrm{SPS}}|\dfrac{8L_\sigma f_{\mathrm{sw}}}{V_{\mathrm{DC1}}\cdot V'_{\mathrm{DC2}}}}}{4L_\sigma f_{\mathrm{sw}}} & V_{\mathrm{DC1}} < V'_{\mathrm{DC2}} \\ \dfrac{V_{\mathrm{DC1}} - V'_{\mathrm{DC2}}\sqrt{1-|P_{\mathrm{SPS}}|\dfrac{8L_\sigma f_{\mathrm{sw}}}{V_{\mathrm{DC1}}\cdot V'_{\mathrm{DC2}}}}}{4L_\sigma f_{\mathrm{sw}}} & V_{\mathrm{DC1}} > V'_{\mathrm{DC2}} \end{cases} \tag{2.11}$$

Triangular Current Modulation (TCM)

An alternative modulation scheme to the SPS modulation is the TCM, where not only φ but also δ_1 and δ_2 are used as degrees of freedom. It was first introduced in [23]. The main goal for TCM is to have a triangular shaped current as shown

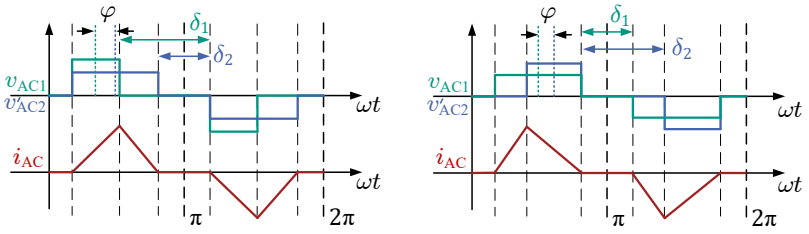


Figure 2.6: Triangular Current Modulation (TCM) voltages $v_{AC1/2}$ and current i_{AC} in (a) boost operation and (b) buck operation

in Fig. 2.6 since this does provide the lowest RMS currents while maintaining soft switching. To achieve the triangular shaped current i_{AC}, the voltage time areas of v_{AC1} and v'_{AC2} have to be equal. This results in shorter pulses for the higher DC link voltage side and longer pulses for the lower DC link voltage side. However, this modulation scheme is only applicable if $V_{DC1} \neq V'_{DC2}$ and therefore the DAB transfer ratio is not equal to one, hence $M = v_{DC1}/v'_{DC2} \neq 1$. Additionally, two different cases have to be considered, buck operation with $V_{DC1} > V'_{DC2}$ and boost operation with $V_{DC1} < V'_{DC2}$.

Case 1: Buck operation $V_{DC1} > V'_{DC2}$

The necessary phase shift angles $\varphi_{TCM,buck}$, $\delta_{1,TCM,buck}$ and $\delta_{2,TCM,buck}$ to achieve a triangular current in buck operation are shown in (2.12), (2.13) and (2.14), respectively.

$$\varphi_{TCM,buck} = \operatorname{sgn}(P_{TCM}) \sqrt{\pi^2 |P_{TCM}| f_{sw} L_\sigma \frac{V_{DC1} - V'_{DC2}}{V_{DC1} \cdot \left(V'_{DC2}\right)^2}} \tag{2.12}$$

$$\delta_{1,TCM,buck} = \pi - \frac{V'_{DC2}}{V_{DC1} - V'_{DC2}} \cdot 2 \cdot |\varphi| \tag{2.13}$$

$$\delta_{2,\mathrm{TCM,buck}} = \pi - \frac{V_{\mathrm{DC1}}}{V_{\mathrm{DC1}} - V'_{\mathrm{DC2}}} \cdot 2 \cdot |\varphi| \tag{2.14}$$

Just like for SPS, the power P_{TCM} only depends on the outer phase shift φ between the two DAB sides and can be calculated according to (2.15). The resulting transfer characteristic for $M = 0.5$ in TCM mode is shown in Fig. 2.7.

$$P_{\mathrm{TCM,buck}} = \mathrm{sgn}(\varphi) \frac{\varphi^2 V_{\mathrm{DC1}} \cdot (V'_{\mathrm{DC2}})^2}{\pi^2 f_{\mathrm{sw}} L_\sigma (V_{\mathrm{DC1}} - V'_{\mathrm{DC2}})} \tag{2.15}$$

In Section 2.1.1, it was shown that the inner phase shift $\delta_{1/2}$ can range between $[0;\pi]$. According to (2.13) and (2.14), this leads to a maximum phase shift $\varphi_{\mathrm{TCM,buck,max}}$ possible in (2.16), to still achieve a triangular shaped current i_{AC}. Consequently, the maximum power $P_{\mathrm{TCM,buck,max}}$ transferable is limited in TCM mode. The maximum power is shown in (2.17) and depends on the voltage difference $V_{\mathrm{DC1}} - V'_{\mathrm{DC2}}$. With a decrease in voltage difference, the maximum power is also decreasing.

$$\varphi_{\mathrm{TCM,buck,max}} = \frac{\pi}{2} \cdot \left(1 - \frac{V'_{\mathrm{DC2}}}{V_{\mathrm{DC1}}}\right) \tag{2.16}$$

$$P_{\mathrm{TCM,buck,max}} = \pm \frac{(V_{\mathrm{DC1}} - V'_{\mathrm{DC2}}) \cdot V'^2_{\mathrm{DC2}}}{4 \cdot L_\sigma \cdot f_{\mathrm{sw}} \cdot V_{\mathrm{DC1}}} \tag{2.17}$$

Similarly to SPS the peak current $\hat{i}_{\mathrm{AC,TCM,buck}}$ can be calculated according to (2.18).

$$\hat{i}_{\mathrm{AC,TCM,buck}} = \sqrt{\frac{V_{\mathrm{DC1}} - V'_{\mathrm{DC2}}}{L_\sigma \cdot f_{\mathrm{sw}} \cdot V_{\mathrm{DC1}}} \cdot |P_{\mathrm{TCM,buck}}|} \tag{2.18}$$

Case 2: Boost operation $V_{\mathrm{DC1}} < V'_{\mathrm{DC2}}$

TCM mode under boost operation is similar to buck operation and is shown in Fig. 2.6 (a). The main difference is that the voltages V_{DC1} and V'_{DC2} are reversed. This results in a symmetry of boost and buck operation around the transfer ratio of $M = 1$. Therefore, the transfer characteristic shown in Fig. 2.7 is also true

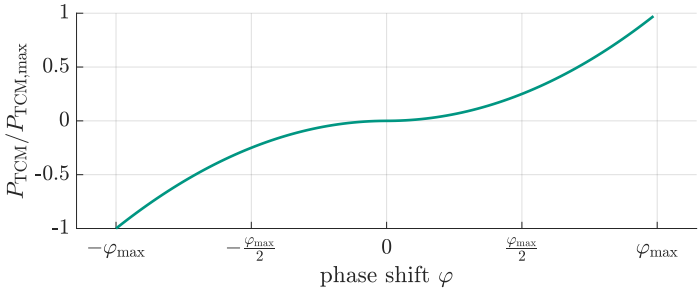


Figure 2.7: Transfer characteristic of the DAB in TCM with transfer ratio of $M = 0.5$

for boost operation. The resulting necessary phase shift angles are shown in (2.19-2.21).

$$\varphi_{\mathrm{TCM,boost}} = \mathrm{sgn}(P_{\mathrm{TCM}})\sqrt{\pi^2|P_{\mathrm{TCM}}|f_{\mathrm{sw}}L_\sigma\frac{V'_{\mathrm{DC2}}-V_{\mathrm{DC1}}}{V_{\mathrm{DC1}}^2\cdot V'_{\mathrm{DC2}}}} \tag{2.19}$$

$$\delta_{1,\mathrm{TCM,boost}} = \pi - \frac{V'_{\mathrm{DC2}}}{V'_{\mathrm{DC2}}-V_{\mathrm{DC1}}}\cdot 2\cdot|\varphi| \tag{2.20}$$

$$\delta_{2,\mathrm{TCM,boost}} = \pi - \frac{V_{\mathrm{DC1}}}{V'_{\mathrm{DC2}}-V_{\mathrm{DC1}}}\cdot 2\cdot|\varphi| \tag{2.21}$$

The resulting power $P_{\mathrm{TCM,boost}}$ is shown in (2.22) with a maximum phase shift $\varphi_{\mathrm{TCM,boost,max}}$ (2.23) and maximum transmittable power $P_{\mathrm{TCM,boost,max}}$ (2.24).

$$P_{\mathrm{TCM,boost}} = \mathrm{sgn}(\varphi)\frac{\varphi^2 V_{\mathrm{DC1}}^2\cdot V'_{\mathrm{DC2}}}{\pi^2 f_{\mathrm{sw}}L_\sigma(V'_{\mathrm{DC2}}-V_{\mathrm{DC1}})} \tag{2.22}$$

$$\varphi_{\mathrm{TCM,boost,max}} = \frac{\pi}{2}\cdot\left(1-\frac{V_{\mathrm{DC1}}}{V'_{\mathrm{DC2}}}\right) \tag{2.23}$$

$$P_{\mathrm{TCM,boost,max}} = \pm \frac{(V'_{\mathrm{DC2}} - V_{\mathrm{DC1}}) V_{\mathrm{DC1}}^2}{4 L_\sigma f_{\mathrm{sw}} V'_{\mathrm{DC2}}} \tag{2.24}$$

The peak current $\hat{i}_{\mathrm{AC,TCM,boost}}$ is given in (2.25).

$$\hat{i}_{\mathrm{AC,TCM,boost}} = \sqrt{\frac{V'_{\mathrm{DC2}} - V_{\mathrm{DC1}}}{L_\sigma \cdot f_{\mathrm{sw}} \cdot V'_{\mathrm{DC2}}} \cdot |P_{\mathrm{TCM,boost}}|} \tag{2.25}$$

Advanced Modulation Methods

Even though this work only deals with the two modulation schemes SPS and TCM and variations of these two, the numerous advanced modulation methods that attempt to eliminate the shortcomings of SPS and TCM in various ways should not go unmentioned. Depending on the applications there are different optimization criteria. The most common design criterion is the reduction of RMS current $i_{\mathrm{AC,RMS}}$ and therefore a reduction of the conduction losses. To reduce switching losses, a soft switching optimization (typically in order to improve the Zero Voltage Switching (ZVS) behavior) is possible. It is also possible to combine both optimization criteria to reduce overall losses in a DAB which, however, is not possible in a mathematical closed form due to the high complexity of the multiple degrees of freedom. In Section 2.1 three degrees of freedom are presented in form of the outer phase shift φ and the inner phase shifts δ_1 and δ_2. However, the option to vary the switching frequency still exists. Consequently, all modulation schemes can be differentiated according to the degree of freedom used [24].

A. Double Phase Shift

For Double Phase Shift (DPS) modulation the two inner phase shifts are equal on both sides $\delta = \delta_1 = \delta_2$. For power control the outer phase shift φ is utilized [25–27]. This additional degree of freedom in δ can decrease circular current (and therefore the RMS current) for i_{AC} and improve soft switching capabilities. The resulting arbitrary DPS waveforms are shown in Fig. 2.8 (a).

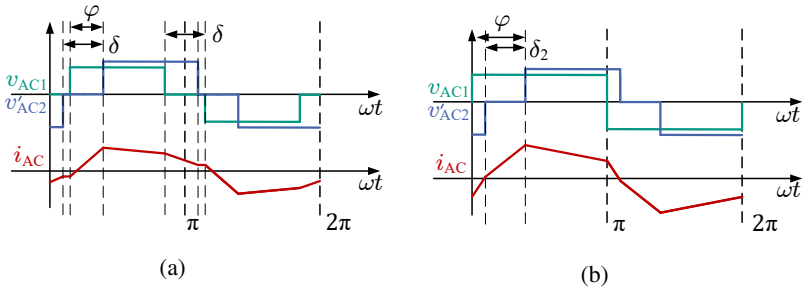


Figure 2.8: Arbitrary waveforms for (a) Double Phase Shift (DPS) modulation (b) Extended Phase Shift (EPS) modulation in boost operation

B. Extended Phase Shift

The Extended Phase Shift (EPS) modulation utilizes only one inner phase shift δ_1 or δ_2 while the other one is set to zero. For boost operation δ_2 is applied to reduce the RMS voltage v_{AC2} whereas δ_1 is used for buck operation to reduce the RMS value of v_{AC1}. The outer phase shift φ is used for power control similar to DPS [28, 29]. EPS has comparable advantages and disadvantages as DPS. The resulting arbitrary EPS waveforms for boost operation with $\delta_1 = 0$ are shown in Fig. 2.8 (b).

C. Triple Phase Shift

For Triple Phase Shift (TPS) modulation both inner phase shifts δ and the outer phase shift φ shown in Fig. 2.3 are used to control power and optimize the waveforms. In contrast to DPS modulation, in TPS modulation the inner phase shifts can be different from each other $\delta_1 \neq \delta_2$ and therefore all three degrees of freedom are utilized. This represents a complex optimization problem which is highly dependent on the hardware used in the DAB for optimal operation. This is the reason why usually specific parameters are optimized. For example the AC current stress i_{AC} [30–32] or the ZVS range [33]. However, by optimizing the overall losses of the system, the best results in terms of efficiency can be achieved using TPS[17, 34]. The previously presented modulation scheme TCM is a special case of the TPS modulation. Additionally, TPS is the most general

modulation scheme and all other phase shift modulation schemes can be included in the TPS category by setting individual phase shift angles to a constant value.

D. Frequency Modulation

In (2.3) and (2.6) it was shown that the power transfer and current waveform highly depends on the inductance L_σ and the switching frequency f_{sw}. Therefore, for all modulation schemes the maximum transmittable power is limited similar to SPS and TCM. The reason for that is the limited time to increase and decrease the energy stored in the inductance L_σ for one switching period T. Therefore the switching frequency f_{sw}, and with that the switching period T, can be adjusted to increase the operation range of a given modulation scheme. This is called Frequency Modulation (FM). If it is combined with TPS for a hybrid modulation scheme the operation range and efficiency can be increased. This modulation scheme is presented in [35–37]. However, it is important to note that a variation in switching frequency f_{sw} can lead to higher stress for passive components especially the MFT. In addition, it must be ensured that saturation does not occur for all operation points.

E. Burst Mode/Pulsed Power Mode

Typically modulation schemes have low efficiency for low load situations due to the loss of soft switching operation. It is possible to avoid these inefficient operation points by using burst mode or pulsed power mode modulation schemes [16, 38]. The main idea is to have a Pulse Width Modulation (PWM) on top of the phase shifted modulation scheme. This results in higher transferred power in the burst time frame and zero power for the free wheeling. This avoids low transferred power altogether, however the DC link voltages V_{DC} have an increased ripple or must have increased passive component effort for the same voltage ripple in order to buffer the power ripple caused by the burst mode.
A comparison of the discussed modulation schemes in terms of the most critical performance indicators is shown in table 2.1. A more detailed comparison of SPS and TCM is shown in the next section.

2.2 Comparison of Modulation Schemes

In Section 2.1 different modulation schemes, primarily SPS and TCM, are presented with their characteristic parameters like $i_{\mathrm{AC,max}}$, i_{RMS} and P_{max}. To put the

Table 2.1: Comparison of different modulation schemes

	Degrees of Freedom	maximum Power	passive component effort	optimization effort
SPS	1	high	low	very low
DPS	2	medium	medium	medium
EPS	2	medium	medium	medium
TPS	3	high	low	high
FM	4	very high	high	very high
Pulsed Power Mode	4	low	high	medium

advantages and disadvantages of the modulation schemes into perspective, they are compared with normalized values, which gives a comprehensive overview of both SPS and TCM. The normalized power is calculated according to (2.26) and represents a tenth of the maximum power for SPS for all normalized values equal to one. The operation point dependent parameter are normalized in a similar way. This is done to achieve a comparison of the modulation schemes independently of the DAB ratings.

$$P_{\text{norm}} = \frac{1}{10} P_{\text{max,SPS}}(V_{\text{DC1,norm}} = 1, V_{\text{DC2,norm}} = 1, L_{\sigma,\text{norm}} = 1) \tag{2.26}$$

Maximum transferable power

As shown in (2.9) and (2.17/2.24) the maximum power P_{max} is limited for both SPS and TCM. The defining parameter for this limitation on the one hand the product of switching frequency and inductance $L_\sigma \cdot f_{\text{sw}}$ and on the other hand the product of both DC link voltages V_{DC} in case of SPS. For TCM the difference between the DC link voltages V_{DC} is the defining parameter. Figure 2.9 compares the maximum possible normalized power $P_{\text{max,norm}}$ for SPS and TCM for different voltages $V_{\text{DC1/2}}$ and two different inductances. It can be seen, that SPS is able to transmit significantly more power compared to TCM for the same operation points. Especially with similar voltages $V_{\text{DC1}} \approx V'_{\text{DC2}}$ SPS performs

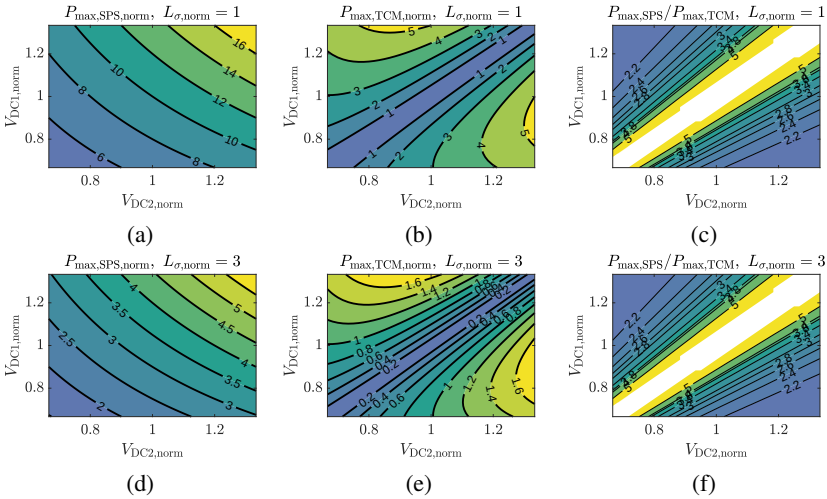


Figure 2.9: Normalized maximum transmittable power $P_{\max,\mathrm{norm}}$ depending on the normalized inductance $L_{\sigma,\mathrm{norm}}$ for (a,d) SPS and (b,e) TCM (c,f) ratio of $P_{\max,\mathrm{SPS}}/P_{\max,\mathrm{TCM}}$

much better, since the main operation principle of TCM is to use the voltage difference $V_{\mathrm{DC1}} - V'_{\mathrm{DC2}}$ to achieve a triangular current i_{AC}. By altering the inductance the maximum power $P_{\max}$ is changed with $P_{\max} \propto \dfrac{1}{L_\sigma \cdot f_{\mathrm{sw}}}$ for both SPS and TCM. Therefore, a reduction in inductance L_σ and switching frequency f_{sw} is necessary to achieve an increase in maximum power ratings $P_{\max}$.

RMS Current

The RMS current $i_{\mathrm{AC,rms}}$ is an important benchmark to evaluate the conduction losses for different modulation schemes independently of the semiconductor or transformer parameter. The normalized RMS current is given in (2.27) for SPS and in (2.28) for TCM. The resulting normalized RMS current $i_{\mathrm{AC,rms,norm}}$ is shown in Fig. 2.10 for SPS and TCM with different power level P_{norm}. For a transfer ratio $M = \dfrac{V_{\mathrm{DC1,norm}}}{V_{\mathrm{DC2,norm}}}$ that deviates from one, the RMS current $i_{\mathrm{AC,rms,SPS,norm}}$ does not scale with power significantly but remains constant. The reason for that

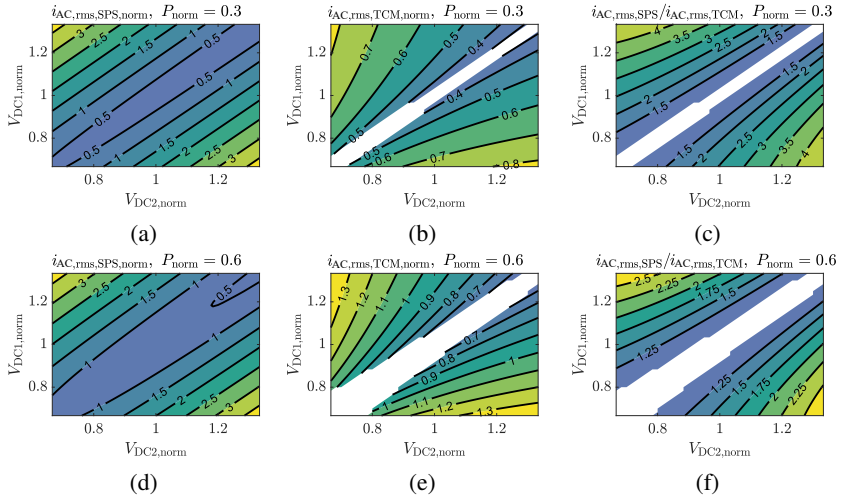


Figure 2.10: Normalized RMS Current $i_{AC,rms,norm}$ (a,d) SPS (b,d) TCM (c,f) ratio $i_{AC,rms,SPS}/i_{AC,rms,TCM}$

is, that the RMS current dominantly consists of circular currents which are independent of the power P. In contrast, TCM scales with the transferred power of the DAB. By looking at Fig. 2.10 (c) and (f) the difference in RMS current between SPS and TCM can be seen. For all possible operation points of TCM, the RMS current can be reduced by using TCM instead of SPS. Only for transfer ratios M_{DAB} close to one, SPS is the better solution in terms of RMS current optimization since TCM cannot achieve the necessary power anymore.

$$I_{AC,SPS,RMS} = \frac{\sqrt{3}}{12} \cdot \sqrt{\frac{(V_{DC1} - V'_{DC2})^2\pi^3 + 12V_{DC1}V'_{DC2}\varphi^2\pi - 8V_{DC1}V'_{DC2}\varphi^3}{\pi^3 L_\sigma^2 f_{sw}^2}} \tag{2.27}$$

$$I_{AC,TCM,RMS,buck/boost} = \frac{i_{AC,TCM,max}}{\sqrt{3}} \sqrt{1 - \frac{\delta_{2/1}}{\pi}} \tag{2.28}$$

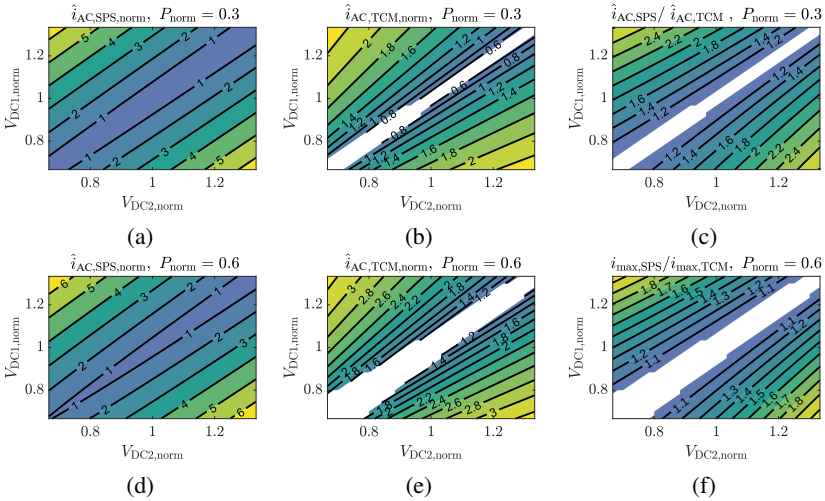


Figure 2.11: Normalized peak Current $\hat{i}_{\mathrm{AC,norm}}$ (a,d) SPS (b,d) TCM (c,f) ratio $\hat{i}_{\mathrm{AC,SPS}}/\hat{i}_{\mathrm{AC,TCM}}$

Peak Current

Another important value for design of a DAB is the maximum peak current $\hat{i}_{\mathrm{AC\,AC}}$ calculated in (2.11) for SPS and in (2.18/2.25) for TCM. It defines the maximum current that has to be turned off by the transistors and therefore imposes a limitation of the operation range of the DAB. They are shown in Fig. 2.11 and the behavior is very similar to the previously discussed RMS current. SPS is only preferred for transfer ratio M_{DAB} near to one. In all other operation points TCM is the better option due to lower maximum currents at the same operation point.

Soft Switching Analysis

An important criterion for efficiency of a medium/high frequency DC/DC converter is the soft switching capability. For a DAB, soft switching is not inherently achieved. That means, the modulation scheme has to be optimized for soft switching capabilities. To evaluate SPS for its soft switching behavior, the waveforms in 2.12 (a) are used. Two switching events occur at two different switching currents, $i_{\mathrm{sw,DC1}}$ for the DC1 side and $i_{\mathrm{sw,DC2}}$ for the DC2 side. It is not feasible

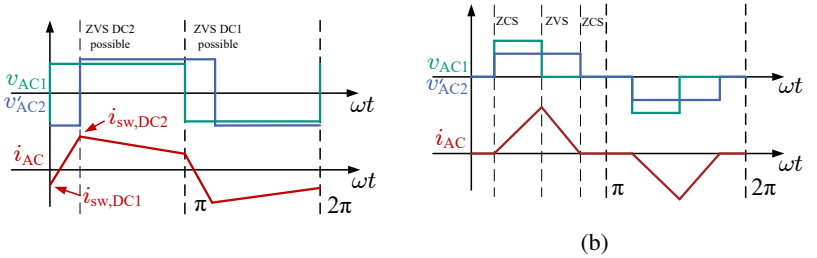


Figure 2.12: Soft Switching Events for (a) SPS(b) TCM

to achieve Zero Current Switching (ZCS) with SPS. In order to achieve ZVS the switching current $i_{\mathrm{sw,DC1}} < 0$ has to be smaller than zero and $i_{\mathrm{sw,DC2}} > 0$ has to be bigger than zero. This will lead to a negative current through the turned-on MOSFETs. Due to that, the diodes will conduct the current within the deadtime. When the MOSFET is turned on, no voltage remains which will lead to ZVS. To achieve this condition the currents in (2.29) and (2.30) are necessary. The resulting ZVS range is shown in Fig. 2.13 for different power level P_{norm}. With an increase in power the ZVS range is increasing for a wider range of DC-Link voltages $V_{\mathrm{DC1/2}}$. The same behavior can be observed by increasing the inductance L_σ or increasing the switching frequency f_{sw}. The dependency on the AC inductance is shown in Fig. 2.14 with two different AC inductances. By looking at TCM mode, it can be noticed that either ZVS or ZCS is always achieved (cf. Fig. 2.12 (b)).

$$i_{\mathrm{sw,SPS,DC1}} = i_{\mathrm{AC,0,SPS}} < 0 \tag{2.29}$$

$$i_{\mathrm{sw,SPS,DC2}} = i_{\mathrm{AC,0,SPS}} + \frac{\varphi(V_{\mathrm{DC1}} + V'_{\mathrm{DC2}})}{2\pi f_{\mathrm{sw}} L_\sigma} > 0 \tag{2.30}$$

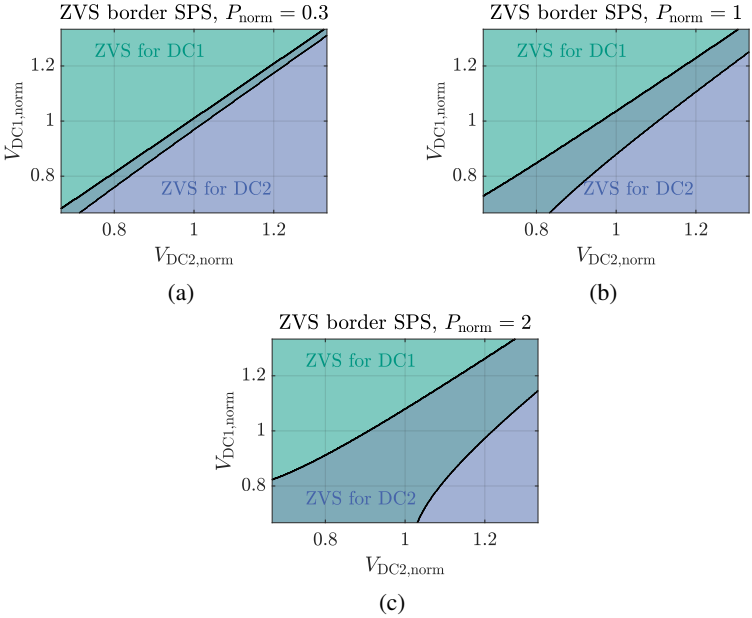


Figure 2.13: ZVS border for SPS with different normalized power P_{norm} (Green: ZVS for DC1, blue: ZVS for DC2 and cyan: ZVS for DC1 and DC2)

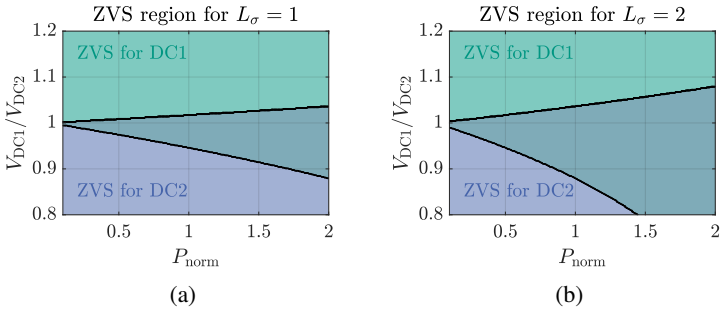


Figure 2.14: ZVS border for SPS with different AC inductances $L_{\sigma,\text{norm}}$ (Green: ZVS for DC1, blue: ZVS for DC2 and cyan: ZVS for DC1 and DC2)

2.3 Conclusion

In this chapter the DAB model with ideal conditions was presented. The influence of important system parameter on the operation behavior of the DAB are derived and presented. Two main modulation schemes are presented. SPS modulation is applied for operation near unity ratio and TCM for buck and boost operation of the DAB. A comparison of both modulation schemes gives a comprehensive overview of the corresponding advantages and disadvantages of both. Additionally, more advanced modulation schemes are categorized, presented and compared. However, previous research has shown that a large portion of the operating range of a DAB can be covered using SPS and TCM. Only in the transition region between SPS and TCM other control schemes may become necessary [34]. It is evident that the TCM operation of the DAB does provide significant advantages over SPS modulation for buck and boost operation. Only for unity operation or operation points with similar DC link voltages, SPS is the preferred modulation scheme, otherwise TCM should be used. For the following chapter, only SPS and TCM is further investigated since these two can cover the entire operating range while maintaining high efficiency due to soft switching and reduced RMS current.

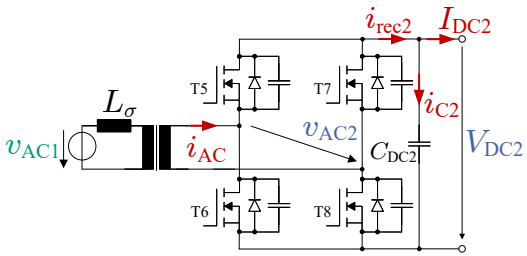
Chapter 3

Dynamic Voltage and Power Control for a Dual Active Bridge

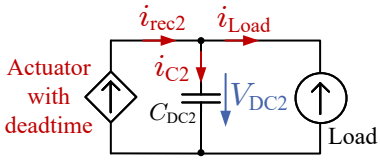
This chapter presents a novel dynamic voltage and power controller for a DAB, which is a crucial part of making sure this converter works efficiently and accurately. The main goal is to achieve a precise and dynamic control. Various different control strategies have been presented in the past. A common strategy is using the small-signal model by linearizing the DAB around a specific operating point [39][40]. However, this approach reduces the possible operation range around the linearized operation point which reduces dynamic and controller performance if the converter is operated at different operation points. This problem is tackled by using a hybrid control of a real-time small-signal linearization in combination with a large-signal model [41]. Other control schemes using a boundary control strategy to achieve high dynamic have been presented [42]. However, this approach requires measuring the AC current, which is especially challenging with high-power DAB because of the combination of high amplitude and high frequency. The control strategy presented in this dissertation uses a mean value model based controller design with feedforward extensions and a novel dynamic limitation of the control output to achieve maximum dynamic while respecting the system boundaries [S1][E1]. This approach does combine the simplicity of a PI control with a high dynamic response time. Both a power as well as a voltage controller is presented using this method.

3.1 Mean Value Model of a Dual Active Bridge

Assuming the lossless and ideal model in 2.1, the DAB as the actuator can be modeled as a controlled current source with the current i_{rec2} which is the rectified AC2 current on the DC2 side of the DAB. This current source is including all semiconductors, the MFT and the inductor, only the DC2 side has to be considered for the mean value model. The result is shown in Fig. 3.1. The DAB controls the DC voltage V_{DC2} by adjusting the controlled variable i_{rec2}, i.e., by influencing the capacitor current i_{C2} at C_{DC2} for the voltage controller and the load current i_{load} for the power controller



(a)



(b)

Figure 3.1: (a) Equivalent Circuit Diagram for the Controller with controlled variable on DC2 side (b) Mean Value Model of the DAB

For the controller design, the resulting time delay T_d is an important variable. Therefore, a typical DAB system is used to demonstrate the determination of the time delay T_d. The timing diagram is shown in Fig. 3.2. The measurement of the input values starts at $t = 0$ and takes one control cycle. At $t = T = 1/f_{sw}$ the controller is able to start the calculation of the necessary control variable i^*_{rec2} and

the triplet of phase shift angles $[\varphi\ \delta_1\ \delta_2]$ to achieve the required current. At $t = 2T$ the actuator starts to change the phase shifts accordingly. Because of the half period symmetry of the DAB, the necessary value is achieved after approximately half a control cycle at $T_{\mathrm{dt}} = 5/2T$. Therefore, the controlled system includes a non-compensable time delay which should be considered in the controller design and reduces the dynamics of the DAB control.

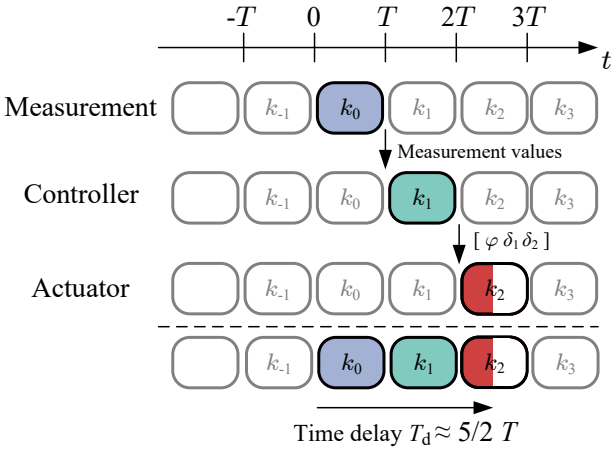


Figure 3.2: Timing diagram of a DAB including controller- and actuator time delay

3.2 Dynamic limitation of Control Output

Chapter 2.2 demonstrates that the significant variables for the operation of a DAB, including the peak current $\hat{i}_{\mathrm{AC}}$, the rms current $i_{\mathrm{AC,rms}}$ and the ZVS behaviour, are highly dependent on the operation point $[V_{\mathrm{DC1}}\ V_{\mathrm{DC2}}\ P]$. Therefore, a static limitation of the transmitted power is not feasible if a high exploitation of the DAB hardware is required. The design goal of a dynamic limitation of the control output i^*_{rec2} and correspondingly the maximum transmittable power P_{max} is to achieve highest possible dynamic and transmittable power without ex-

ceeding system limits defined by the hardware used. Five different limitations are considered in this chapter. However, this method can be extended to every limitation necessary. The considered limitations are shown in table 3.1.

Table 3.1: Limitation for Control Output

	Limitation	Reason for limitation	Equation
a)	P_{max}	Transmittable power defined by system	
b)	$I_{\text{DC1,max}}$	DC1 current defined by semiconductor and neighboring systems	$P_{\text{max,DC1}} = V_{\text{DC1}} \cdot I_{\text{DC1,max}}$
c)	$I_{\text{DC2,max}}$	DC2 current defined by semiconductor and neighboring systems	$P_{\text{max,DC2}} = V_{\text{DC2}} \cdot I_{\text{DC2,max}}$
d)	$P_{\text{max,modulation}}$	Transmittable power defined by modulation	SPS (2.9) TCM (2.17,2.24)
e)	$\hat{i}_{\text{AC,max}}$	AC peak current defined semiconductor, inductor and current measurement	SPS (3.1) TCM (3.2)

a) Maximum transferred Power P_{max}

The first limitation is the maximum transmittable power defined by the DAB or more often by the surrounding systems connected to the DC links of the DAB. This is the weakest boundary and the last to become active if all other limitations are inactive.

b) and c) Maximum DC current $I_{\text{DC1,max}}$ and $I_{\text{DC2,max}}$

The limitaton of the maximum DC current $I_{\text{DC,max}}$ on both sides of the DAB might be necessary to avoid overloading critical system components like the semicondcutors, the current measurements and the cable connections to neighboring systems. This value is a dynamic, DC link voltage dependent power limitation.

d) Maximum Power due to Modulation Scheme $P_{\mathrm{max,modulation}}$

As shown in 2.1, the DAB has a maximum transmittable power $P_{\mathrm{max,modulation}}$ depending on the modulation scheme used. A higher power is not physically possible and therefore can not be used as a control output. The necessary equations for SPS and TCM are presented in (2.9) and (2.24, 2.17), respectively.

e) Maximum Peak AC current $\hat{i}_{\mathrm{AC,max}}$

The last limitation for the control output i^*_{rec2} and the maximum power P_{max} is the peak current in the AC circuit $\hat{i}_{\mathrm{AC}}$. It must not exceed a maximum value of $\hat{i}_{\mathrm{AC,max}}$ to avoid operation points outside of the Safe Operating Area (SOA) of the AC system of the DAB. Limiting factors are the maximum switching current of the semiconductors, the saturation current of the inductor and the maximum current of the current sensors. Using (2.11) and (2.18, 2.25) the resulting maximum power ratings $P_{\mathrm{max,lim}}$ are calculated in (3.1) and (3.2).

$$P_{\mathrm{SPS,max,lim}} = \frac{V_{\mathrm{DC1}} V'_{\mathrm{DC2}}}{8 L_\sigma f_{\mathrm{sw}}} \cdot \begin{cases} 1 - \dfrac{\left(V'_{\mathrm{DC2}} - 4 L_\sigma f_{\mathrm{sw}} \min\left[\hat{i}_{\mathrm{AC,max}}, \dfrac{V'_{\mathrm{DC2}}}{4 L_\sigma f_{\mathrm{sw}}}\right]\right)^2}{{V_{\mathrm{DC1}}}^2} & \text{for } V_{\mathrm{DC1}} < V'_{\mathrm{DC2}} \\ 1 - \dfrac{\left(V_{\mathrm{DC1}} - 4 L_\sigma f_{\mathrm{sw}} \cdot \min\left[\hat{i}_{\mathrm{AC,max}}, \dfrac{V_{\mathrm{DC1}}}{4 L_\sigma f_{\mathrm{sw}}}\right]\right)^2}{V'^2_{\mathrm{DC2}}} & \text{for } V_{\mathrm{DC1}} > V'_{\mathrm{DC2}} \end{cases} \tag{3.1}$$

$$P_{\mathrm{TCM,max,lim}} = \begin{cases} \dfrac{L_\sigma f_{\mathrm{sw}} {\hat{i}_{\mathrm{AC,max}}}^2 V'_{\mathrm{DC2}}}{V'_{\mathrm{DC2}} - V_{\mathrm{DC1}}} & \text{for } V_{\mathrm{DC1}} < V'_{\mathrm{DC2}} \\ \dfrac{L_\sigma f_{\mathrm{sw}} {\hat{i}_{\mathrm{AC,max}}}^2 V_{\mathrm{DC1}}}{V_{\mathrm{DC1}} - V'_{\mathrm{DC2}}} & \text{for } V_{\mathrm{DC1}} > V'_{\mathrm{DC2}} \end{cases} \tag{3.2}$$

$$i^*_{\mathrm{rec2,lim,max}} = \frac{1}{V'_{\mathrm{DC2}}} \min[P_{\mathrm{max}}, P_{\mathrm{max,DC1}}, P_{\mathrm{max,DC2}}, \max[P_{\mathrm{max,SPS}}, P_{\mathrm{max,TCM}}], \max[P_{\mathrm{SPS,max,lim}}, P_{\mathrm{TCM,max,lim}}]] \tag{3.3}$$

The resulting active control output limitation is shown in Fig. 3.3 (a) for the DAB presented in chapter 5 and can be calculated according to (3.3) which chooses the lowest possible boundary. The resulting maximum power transfer $P_{\mathrm{max,c}}$ is shown in Fig. 3.3 (b). For high transfer ratio M_{DAB}, the peak current is the limiting factor and reduces the possible power P drastically.

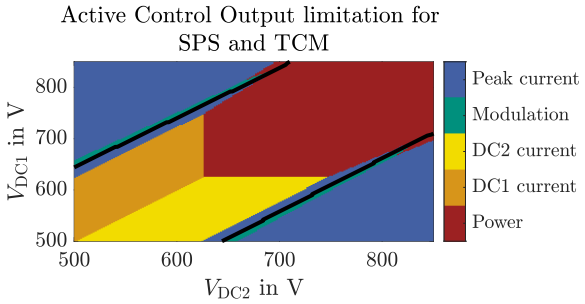
3.3 Voltage Control

The voltage transfer characteristic of the DAB can be deduced by analyzing the model in Fig. 3.1. The model consists of a controlled current source and the output capacitance C_{DC2} which results in a integrating behavior for the transfer characteristic shown in (3.4)

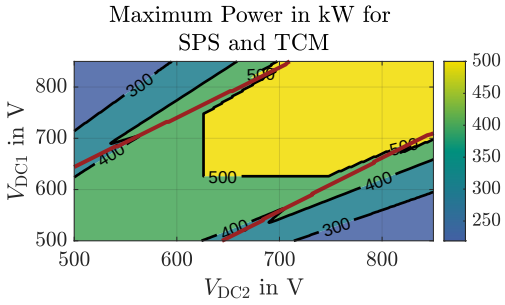
$$F_{\mathrm{V,tc}}(s) = \frac{V_{\mathrm{DC2}}(s)}{i_{\mathrm{C}}(s)} = \frac{1}{C_{\mathrm{DC2}} \cdot s} = \frac{k_{\mathrm{s}}}{s} \tag{3.4}$$

Including the time delay of the system T_{d} shown in Section 3.1 leads to the control diagram for the voltage controller in Fig. 3.4. In the following, indices marked with M denote the measured values. The applied controller is a PI controller which is designed in accordance to the symmetrical optimum. The resulting controller transfer function $F_{\mathrm{V,R}}(s)$ is shown in (3.5) with a the tuning parameter $\alpha = 4$ to achieve a robust and resilient controller with regard of parameter deviations while also maintaining an high dynamic response. A higher α will result in a lower dynamic but higher stability and vice versa.

$$F_{\mathrm{V,R}}(s) = \frac{i^*_{\mathrm{rec2}}(s)}{\Delta V_{\mathrm{DC2}}} = k_{\mathrm{R}} \left(1 + \frac{1}{T_{\mathrm{n}} \cdot s}\right) = \frac{C_{\mathrm{DC2}}}{10T} \left(1 + \frac{1}{40T \cdot s}\right) \tag{3.5}$$



(a)



(b)

Figure 3.3: (a) Active Control Output limitation for SPS and TCM with the same color scheme shown in table 3.1 (b) Maximum power for SPS and TCM using the system limits presented, the black and red lines denotes the transition between SPS and TCM operation

with

$$k_{\mathrm{R}} = \frac{1}{k_{\mathrm{s}}} \cdot \frac{1}{\alpha \cdot T_{\mathrm{d}}} = \frac{C_{\mathrm{DC2}}}{10T}$$

and

$$T_{\mathrm{n}} = \alpha^2 T_{\mathrm{d}} = 40T$$

It is possible to improve the controller performance in regards of dynamic behavior and stability by including additional controller extensions which are discussed

in the following. The resulting control structure of the voltage controller with all extensions is shown in Fig. 3.8.

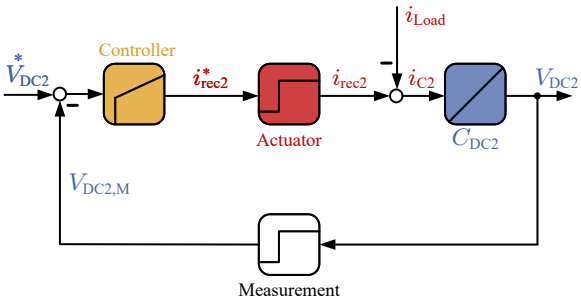


Figure 3.4: Control diagram for the voltage controller

Disturbance Feedforward Control

For highly dynamic loads, a disturbance feedfoward control might be necessary to ensure that the voltage controller can achieve a higher dynamic and therefore a reduced dynamic deviation of the DC link voltage V_{DC2}. However, in order to achieve this behavior, a load current i_{load} measurement with low latency is necessary. If this is available, the measured load current $i_{\mathrm{load,M}}$ can be added to the output of the PI controller i_{PI}. This will result in a faster response of $i^*_{\mathrm{rec2,lim}}$ in case of a load step.

Feedforward Control of the Capacitor Voltage

To improve the dynamic response in case of a setpoint change of the secondary side voltage V_{DC2}, a feedforward control of the capacitor voltage V_{DC2} can be included. The block diagram of the feedforward controller is shown in Fig. 3.5. The main idea is to feedforward the maximum possible voltage change ΔV_{DC} within one period T. The necessary current i^*_{C2} can be calculated according to (3.6). This current should not be exceeded to avoid an intervention by the PI controller and thus to avoid the integration of an error due to the feedforward path. That is why in the next step a setpoint limiter is introduced.

$$i^*_{C2} = \frac{C_{DC2}}{T}(V^*_{DC2,lim}(k_0) - V^*_{DC2,lim}(k_{-1})) = \frac{C_{DC2}}{T}\Delta V^*_{DC2,lim} \tag{3.6}$$

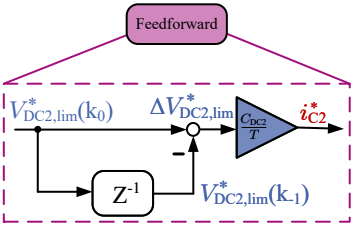


Figure 3.5: Block diagram of the feedforward controller

Setpoint Limiter

It was previously shown that the feedforward control current i^*_{C2} depends on the setpoint voltage step $\Delta V^*_{DC2,lim}$. If these steps are high, the necessary current i^*_{C2} and therefore the control output i^*_{AC2} exceed the limits introduced in section 3.2. Because of that, the PI controller has to compensate the remaining error for static accuracy. To avoid that problem, the rate of change of the setpoint V^*_{DC2} has to be limited to the maximum voltage change of $\Delta V^*_{DC2,max}$ for the given limits in section 3.2. Since the load current i_{load} has a significant impact on the maximum voltage change $\Delta V_{DC2,max}$ it has to be considered as well for maximum dynamics. The resulting maximum setpoint step is given in (3.7).

$$\Delta V^*_{DC2,max} = \frac{T}{C_{DC2}}\left(\bar{i}^*_{AC2,max} - \mathrm{sign}(\Delta V^*_{DC2}) \cdot i_{load,M}\right) \tag{3.7}$$

To calculate the resulting limited setpoint $V^*_{DC2,lim}$, (3.8) is used and depicted as a block diagram in Fig. 3.6. For the ideal lossless DAB model in chapter 2.1, the feedforward control and setpoint limiter in combination will result in maximum dynamic response, by fully utilizing the DAB system limits in each control step, and no remaining permanent error in the DC link voltage V_{DC2}. The PI controller

is therefore not necessary anymore. However, model inaccuracies, like parameter deviations or non ideal behavior of the DAB will result in a persisting error which has to be compensated by the PI controller.

$$V^*_{\mathrm{DC2,lim}} = V_{\mathrm{DC2,lim}}(k_{-1})^* + \mathrm{sign}(\Delta V^*_{\mathrm{DC2}}) \cdot \min[|\,\Delta V^*_{\mathrm{DC2}}\,|, \Delta V^*_{\mathrm{DC2,max}}] \tag{3.8}$$

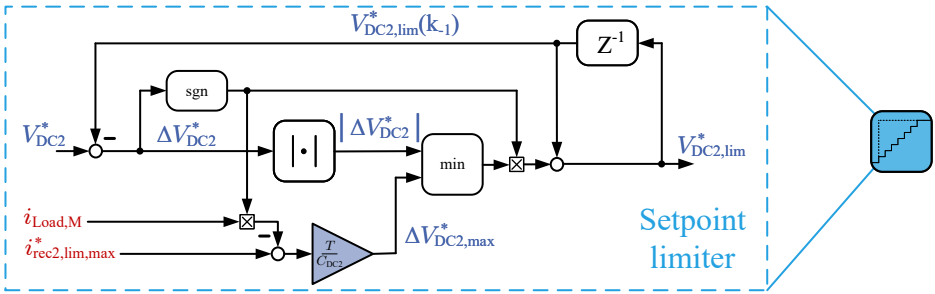


Figure 3.6: Block diagram of the setpoint limiter

An additional advantage of the setpoint limiter and the feedforward control in combination is that no additional effort is necessary for a start up of the DAB. This is shown in Fig. 3.7 for a simulation with the DAB parameters presented in chapter 5 with a DC1 voltage of $V_{\mathrm{DC1}} = 600$ V. The limiting parameter is shown in this figure using the same color code as in table 3.1 and maximum dynamic between $V_{\mathrm{DC2}} = 0$ V and $V_{\mathrm{DC2}} = 800$ V is achieved using feedforward control in combination with the setpoint limiter.

3.4 Power Control

For various applications with defined voltage levels on both sides (eg. DC grid coupling, battery charging), a power control P of the DAB might be necessary. This power control can be designed based on the mean value model and the timing diagram in section 3.1. Using that, the controlled system transfer function can be reduced to a time delay with $T_{\mathrm{d}} = 5/2T$ in (3.9) since only the current source is still active. For an ideal DAB, no controller is necessary. But to take non

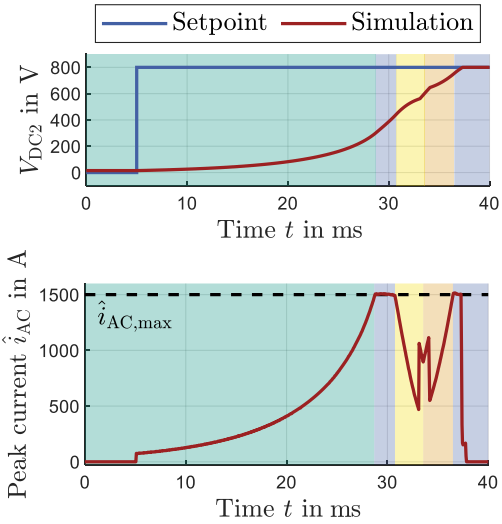


Figure 3.7: Simulation for start up of the DAB with dynamic limitation of the Control Output ($V_{DC1} = 600$ V)

ideal behavior and parameter deviations into account, an I-controller is used to compensate a static deviation of the system. Additionally, a feedforward control, similar to the voltage controller, is used to increase the dynamic response. Again, the comparison between setpoint value i^*_{DC2} and measurement value $i_{load,M}$ must be delayed by T_d to prevent oscillations between the I-controller and the feedforward control. To achieve a delay of half a switching cycle, a sub-cycle averaging is applied. In this case, only half of the signal is delayed by one time step and summed with half of the non-delayed signal which results in an approximate delay of 1/2. The resulting control structure of the power controller is shown in Fig. 3.9. The same dynamic limitation of the control output from section 3.2 is used for the power controller as well but a setpoint limiter is not necessary since the transferred power can be changed in just two control periods from $-P_{max}$ to P_{max} and vice versa (cf. section 3.5). For an ideal system, the input of the I controller Δi_{AC2} is always zero even for transient steps.

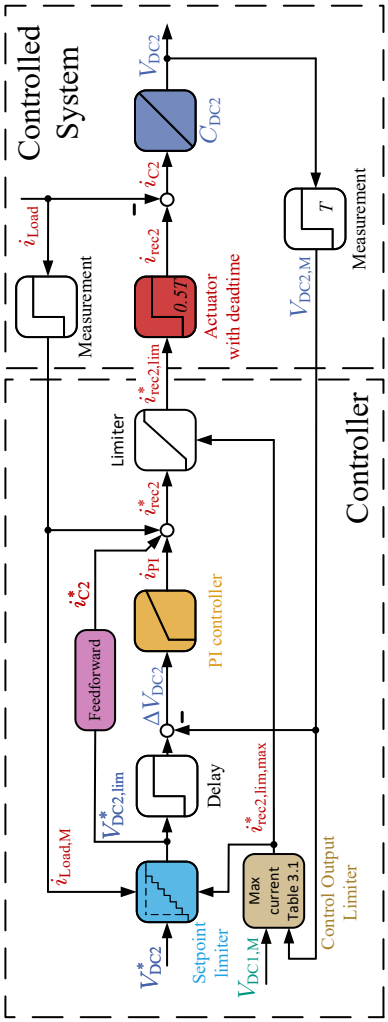


Figure 3.8: Control structure of the voltage controller

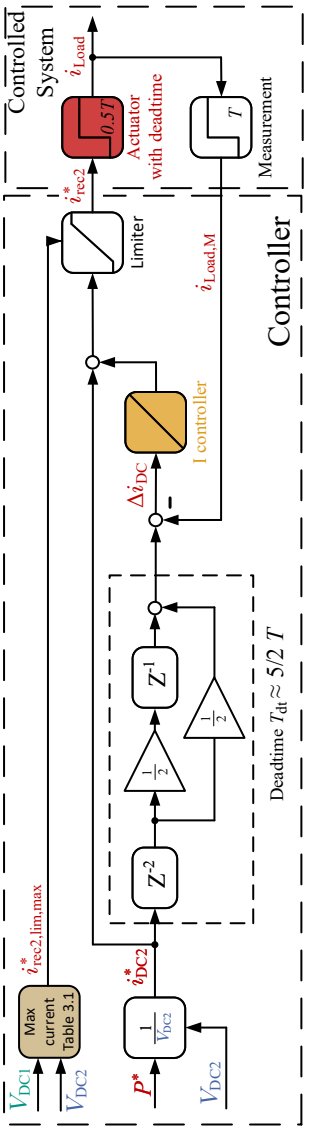


Figure 3.9: Control structure of the power controller

$$F_{\mathrm{P,tc}}(s) = e^{-T_{\mathrm{d}}s} \tag{3.9}$$

Since the I-controller only eliminates model inaccuracies and parameter deviations, its dynamic can be designed very slow to increase stability of the system. In order to abtain this behavior, the open control loop has to have integrating behavior and the phase margin is choosen as $\varphi_{\mathrm{r}} = 68°$. To achieve that, the controller gain is calculated according to (3.11). The resulting bode plot is shown in Fig. 3.10.

$$F_{\mathrm{P,o}}(s) = F_{\mathrm{P,tc}}(s) \cdot F_{\mathrm{P,C}}(s) = e^{-T_{\mathrm{d}}s} \frac{k_{\mathrm{P}}}{s} \tag{3.10}$$

$$k_{\mathrm{P}} = \frac{1}{\omega_{\mathrm{D}}} = \frac{1}{0.0243 \cdot 2\pi f_{\mathrm{sw}}} = 6.56T \tag{3.11}$$

3.5 DC Bias Suppression

Using the feedforward control approach for the power and the voltage controller can lead to high setpoint changes and therefore a steep step in the transferred power P. However, a jump in the power setpoint, and therefore also in the control angle φ, will lead to a DC bias in the AC current i_{AC} with SPS operation. The reason for that is the calculated control angle φ does only lead to a DC bias free AC current in the steady state operation. For transient operation, the starting point of the period does not match to the new steady state. In Fig. 3.11, a reduction of the transferred power for SPS is shown. A significant DC bias is present. This DC bias can saturate the transformer core and therefore will result in increased losses without participating in the power transfer. Additionally, depending on the operation points, this DC bias can result in increased switching currents which can violate the SOA of the switches. Therefore, this should be avoided. To suppress this DC bias, a transition phase has to be included in the setpoint change. In this transition phase, the first phase shift is replaced with the transition phase angle φ_2' in (3.12). The second phase shift of the period is similar to the steady state control angle φ. This leads to a asymmetric waveform and will result in a small DC bias within the AC voltages (cf. Fig. 3.12). It should be noted, that this DC

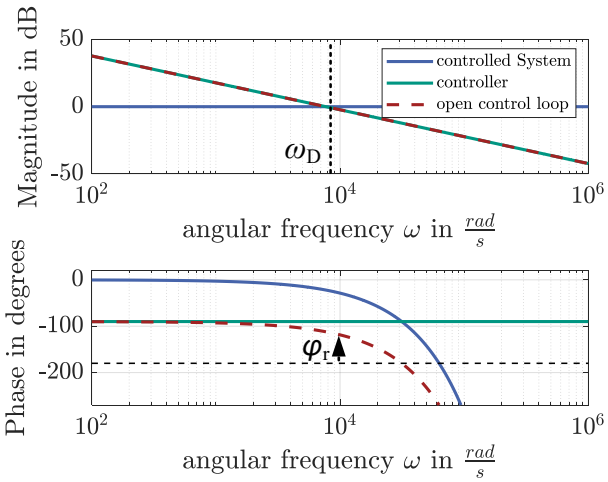


Figure 3.10: Bode plot of the power controller and the controlled system

bias in the AC voltages can also lead to transformer saturation due to a slightly increased magnetizing current. However, the dynamic response is drastically improved since every power setpoint change between maximum power $P_{\max}$ and negative maximum power $-P_{\max}$ can be achieved in only two periods without exceeding the system limits. Additionally, the efficiency for transient operation is highly improved. Similar approaches have already been presented in [43], [44] and [45]. In [E2], an improved version is presented which can also control the power flow within the transition phase in order to further increase dynamic.

$$\varphi_2' = \frac{\varphi_1 + \varphi_2}{2} \tag{3.12}$$

For TCM operation, a DC bias is inherently suppressed if a setpoint transition only occurs at the free wheeling stages where the current is 0 no matter how high the transferred power level is. For a transition from TCM to SPS the transition phase angle has to be half of the new phase angle $\varphi_2' = \varphi_2/2$. Whereas, for a

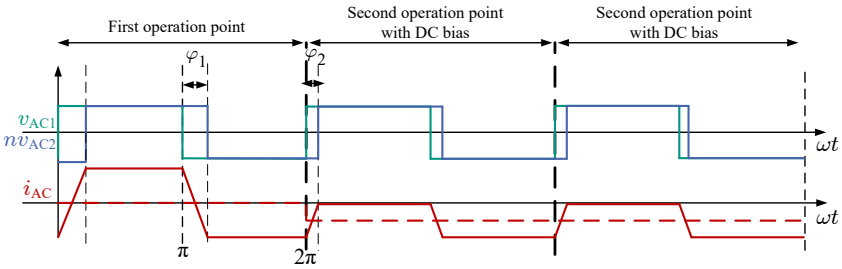


Figure 3.11: Change of operation point using SPS without DC bias suppression

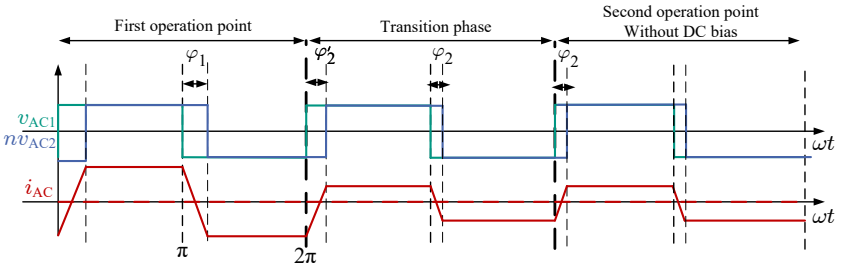


Figure 3.12: Change of operation point using SPS with DC bias suppression

transition from SPS to TCM the last half cycle is extended for $\varphi_2' = \varphi_1/2$ to reach the free wheeling state of the start of the TCM period.

3.6 Conclusion

In this chapter an easy to implement control structure with maximum achievable dynamic is presented. Using a novel dynamic limitation of the control output, the maximum transferable power can be calculated and applied to the DAB while considering the system limits such as maximum power, maximum DC current, maximum power of the modulation scheme and peak current in the AC circuit. An extension with other system limitations such as maximum losses is also pos-

sible to consider. Based on this control output limitation, a voltage and power controller using the PI- and I-structure respectively are presented. Both controllers are designed such that a maximum dynamic is possible without violating the system limits. In contrast to existing controller schemes, using these controllers, an operation between 0 V and $V_{\mathrm{DC,max}}$ is possible without any additional special cases and with maximum dynamic response. Additionally, the PI- and I-controller is not designed for maximum dynamic since the dynamic feedforward path regulates load steps which results in a more stable controller design compared to traditional methods. In the last step, a DC bias suppression method is presented to reduce DC biases in the AC current in case of high setpoint changes for SPS and TCM operation. This is important to avoid increased losses and a reduced dynamic due to higher peak currents in the AC circuit, transformer and inductor saturation and exceeding the system limits. Both controller designs necessitate a precise and accurate DAB model to improve dynamic and stability.

Chapter 4

Steady State Model of a Dual Active Bridge with non-ideal Conditions

The previous chapter showed that an accurate and detailed DAB model provides advantages in terms of control dynamics and stability. Moreover, a detailed model facilitates an improved converter design. Therefore, this chapter provides a detailed analysis and modeling approach for the steady-state operation of a DAB, accounting for the relevant non-ideal effects.
First, the impact of AC resistance and magnetizing inductance on steady-state behavior is discussed. It is shown that AC resistance significantly affects both the transferable power and the ZVS behavior of the DAB, particularly at high power levels. However, magnetizing inductance can generally be neglected when the ratio of magnetizing inductance to stray inductance (L_m/L_σ) is sufficiently high (a typical threshold is around 100). Furthermore, a novel and detailed model of the resonant ZVS commutation process in the DAB is provided. The effects of this commutation on both the power transfer and the loss characteristics are presented, along with a mathematical model for determining the optimal deadtime to minimize switching losses. In contrast to existing modelling approaches, a universal mathematical framework is provided which can be used to calculate every switching state and every relevant parameter of the ZVS transition (eg. optimal deadtime, operation point dependent minimal switching current, residual voltage for partial ZVS operation). Based on this model, a linearization method for the

transfer characteristic and an advanced modulation scheme for buck and boost operation is introduced. Finally, the chapter examines the impact of a non-ideal transformer on DAB performance. An improved winding design is proposed to minimize the impact of the transformer on system operation.

4.1 Impact of AC resistance

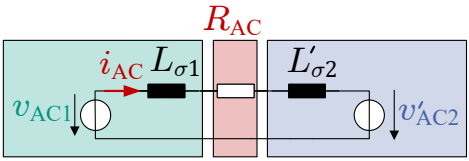


Figure 4.1: DAB model considering conduction losses

In chapter 2.1 the ideal lossless DAB model is presented. However, under realistic conditions a lossless model cannot represent the behavior of the DAB accurately [46][E3][E4]. Therefore, in this section the impact of an additional AC resistance R_{AC} on the DAB model is analyzed. The resulting equivalent circuit diagram for a DAB with consideration of conduction losses is shown in Fig. 4.1. The equivalent AC resistance R_{AC} contains all existing resistances as well as additional linear losses of the DAB. The main contributor are the MOSFET on state resistance $R_{DS,on}$ and the transformer winding resistance R_w. It is important to mention that especially the winding resistance R_w can be highly frequency dependent due to skin and proximity effects [47][48]. However, this effect is not considered in this section since a closed-form analytical expression is not possible anymore with frequency dependent resistances (in section 4.2, an approach for addressing frequency-dependent effects is presented). However, in practice it is usually sufficient to calculate the resistance at the fundamental frequency of the AC circuit. The resulting differential equation for this DAB model is given in (4.1) with the solution for $i_{AC}(t)$ in (4.2). For this a time constant $\tau = {}^{L_\sigma}/_{R_{AC}}$ with $L_\sigma = L_{\sigma 1} + L'_{\sigma 2}$ can be defined and gives a measure of the influence of the AC resistance R_{AC} on the DAB behavior. The smaller and closer τ (4.3) gets to the period length T the bigger the impact on the DAB is.

$$0 = -v_{\mathrm{AC1}}(t) + v'_{\mathrm{AC2}}(t) + L_\sigma \frac{\mathrm{d}i_{\mathrm{AC}}(t)}{\mathrm{d}t} + R_{\mathrm{AC}} \cdot i_{\mathrm{AC}}(t) \tag{4.1}$$

$$i_{\mathrm{AC}}(t) = i_{\mathrm{AC},0} \cdot e^{-t/\tau} + \frac{v_{\mathrm{AC1}} - v'_{\mathrm{AC2}}}{R_{\mathrm{AC}}}\left(1 - e^{-t/\tau}\right) \tag{4.2}$$

$$\tau = {}^{L_\sigma}/_{R_{\mathrm{AC}}} \quad \text{and} \quad T_\varphi = \frac{\varphi}{2\pi f_{\mathrm{sw}}} \tag{4.3}$$

Impact on Single Phase Shift Modulation

The universally valid current i_{AC} for all modulation methods in a model including conduction losses is calculated in (4.2). However, the initial current $i_{\mathrm{AC},0}$ is dependent on the modulation scheme. For SPS, the mean value has to be zero for a steady state operation (cf. chapter 2.1) which is achieved if $-i_{\mathrm{AC}}(T_0) = i_{\mathrm{AC}}\left({}^{(T+T_0)}/_2\right)$. The resulting starting current $i_{\mathrm{AC,SPS},0}$ is shown in (4.4).

$$i_{\mathrm{AC,SPS},0} = \frac{-\left(V_{\mathrm{DC1}} + V'_{\mathrm{DC2}}\right) e^{-(T/2-T\varphi)/\tau}\left(1 - e^{-T\varphi/\tau}\right) - \left(V_{\mathrm{DC1}} - V'_{\mathrm{DC2}}\right)\left(1 - e^{-(T/2-T\varphi)/\tau}\right)}{R_{\mathrm{AC}}\left(1 + e^{-(T/2-T\varphi)/\tau} e^{-T\varphi/\tau}\right)} \tag{4.4}$$

An exemplary waveform of the resulting current of i_{AC} in SPS modulation is shown in Fig. 4.2 for a positive power from DC1 to DC2. Compared to the lossless model, the switching current of the DC2 side $i_{\mathrm{sw,DC2}}$ is increased while the switching current the DC1 $i_{\mathrm{sw,DC1}}$ is decreased. Additionally, the circular currents of i_{AC} (and therefore the reactive power) are increased which results in higher RMS current compared to the lossless model.
The resulting instantaneous power $p_{1,2}(t)$ can be calculated by multiplying the current i_{AC} with the respective voltage $v_{\mathrm{AC1/2}}$, the resulting power is shown in (4.5). Similar to the lossless model, the average power P_2 can be calculated by integrating $p_2(t)$ over one period. The resulting average power is shown in (4.6). However, for a model with conduction losses the assumption of $P_1 = P_2$ is not

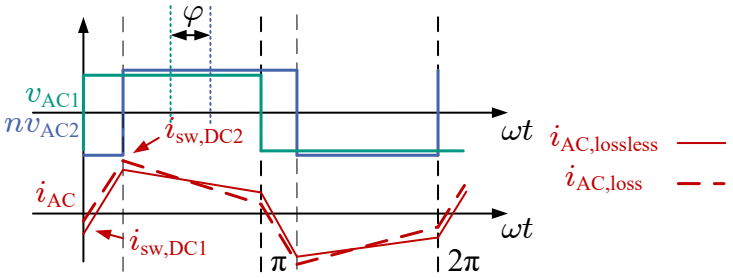


Figure 4.2: SPS modulation voltage v_{AC} and current i_{AC} considering conduction losses

true anymore and both average powers are different. Figure 4.3 shows the transfer characteristic for $V_{DC1} = V'_{DC2}$ for the whole operation range of the DAB.
It can be observed that the peak power on the DC2 side $P_{2,max}$ is smaller in case of a power transfer from DC1 to DC2 side (corresponds to a positive power transfer). However, for a a power transfer from DC2 to DC1 side (corresponds to a negative power transfer) the peak power on the DC2 side $P_{2,max}$ is increased compared to the lossless assumptions. The difference between P_1 and P_2 represents the ohmic losses of the DAB. This leads to a reduced operation range of the DAB. Furthermore, the maximum power is not achieved at $\varphi/2$ anymore.

$$p_{1/2}(t) = v_{AC1/2} \begin{cases} \pm i_{AC,0} \cdot e^{-t/\tau} \pm \dfrac{V_{DC1} + V'_{DC2}}{R_{AC}} \left(1 - e^{-t/\tau}\right) & 0 \le t \le T_\varphi \\ i_{AC}(T_\varphi) \cdot e^{-(t-T_\varphi)/\tau} + \dfrac{V_{DC1} - V'_{DC2}}{R_{AC}} \left(1 - e^{-(t-T_\varphi)/\tau}\right) & T_\varphi \le t \le \dfrac{T}{2} \end{cases} \tag{4.5}$$

$$P_{1/2} = \frac{2}{T}\int_{T_0}^{T_0+T/2} p_{1/2}(t)\mathrm{d}t = \Bigg[\pm\tau\cdot i_{\mathrm{AC},0}(1-e^{-T\varphi/\tau}) \pm \frac{(V_{\mathrm{DC1}}+V'_{\mathrm{DC2}})(e^{-T\varphi/\tau}\tau-\tau+T\varphi)}{R_{\mathrm{AC}}} + \tau\cdot i_{\mathrm{AC}}(T\varphi)(1-e^{-(T-2T\varphi)/2\tau}) + \frac{(V_{\mathrm{DC1}}-V'_{\mathrm{DC2}})(\frac{T}{2}-T\varphi)-\tau(V_{\mathrm{DC1}}-V'_{\mathrm{DC2}})(e^{-(T-2T\varphi)/2\tau}-1)}{R_{\mathrm{AC}}}\Bigg]\frac{2V_{\mathrm{DC1/2}}}{T} \tag{4.6}$$

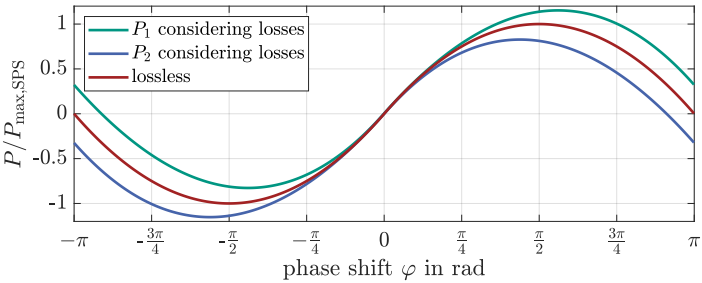
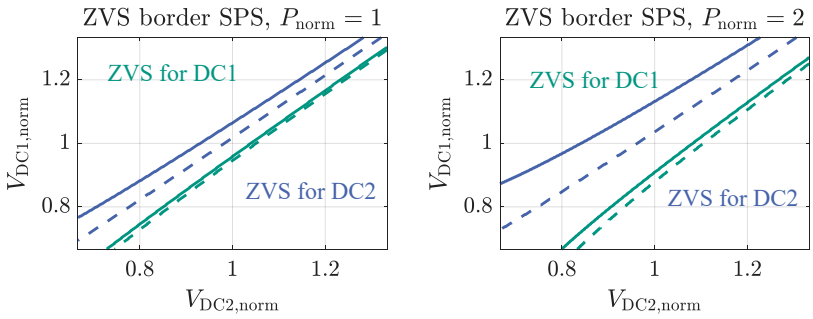


Figure 4.3: Transfer characteristic of the DAB in SPS modulation with consideration of conduction losses for $V_{\mathrm{DC1}} = V_{\mathrm{DC2}}$

As discussed earlier and shown in Fig. 4.2, the switching currents i_{sw} for a lossy DAB model are changing depending on the power direction. Therefore, the discussed ZVS border of both DC1 and DC2 side is changing. By using the same assumptions as for the ideal model, mainly the sign of the current at start of each switching event, the ZVS border can be calculated according to (4.7) and (4.8) for DC1 and DC2, respectively. The resulting change of the ZVS regions is shown in Fig. 4.4 for different normalized power levels. It can be observed, that with positive power the ZVS region of DC1 is decreasing and the ZVS region for DC2 increasing. This is due to the increasing current $i_{\mathrm{sw,DC2}}$ and decreasing current



(a) (b)

Figure 4.4: ZVS border for SPS with different normalized power P_{norm}: (——)lossy model (– –)ideal model

$i_{\text{sw,DC1}}$ (cf. Fig. 4.2). For negative power transfer this behavior is mirrored with an increased ZVS region for DC1 and decreased region for DC2.

$$i_{\text{sw,SPS,DC1}} = i_{\text{AC,0}} < 0 \tag{4.7}$$

$$i_{\text{sw,SPS,DC2}} = i_{\text{AC,0}} \cdot e^{-\tau\varphi/\tau} + \frac{V_{\text{DC1}} + nV_{\text{DC2}}}{R_{\text{AC}}} \left(1 - e^{-\tau\varphi/\tau}\right) > 0 \tag{4.8}$$

Impact on Triangular Current Modulation

Since there is no closed-form solution for the expressions of the current $i_{\text{AC}}(t)$ and consequently the transferred power of the DAB with TCM, only the qualitative impact of the AC resistance R_{AC} on the DAB is investigated. However, in section 4.2 a modeling approach using the frequency domain is presented. Using that idea, the calculation of the lossy DAB is possible. In Fig. 4.5 the AC current $i_{\text{AC,loss}}$ is compared with the lossless AC current $i_{\text{AC,lossless}}$. Using the same control angles φ, δ_1 and δ_2 introduced in chapter 2.1 will lead to a non zero circular current in the freewheeling state. The reason for this is that the voltage

time area for the inductor voltage v_L is changed due to the ohmic voltage drop. This will lead to an increased switching current $i_{sw,2}$ and a non zero switching current $i_{sw,1} \neq 0$ and $i_{sw,3} \neq 0$. Therefore the assumption of ideal ZCS does not hold anymore with a lossy DAB model. However, ZVS is possible on the DC2 side whereas the DC1 side will experience hard switching and thus full switching losses. Additionally, the RMS current is increasing due to a higher circulating current.

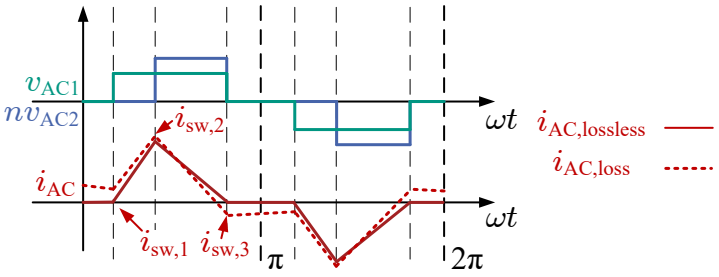


Figure 4.5: TCM modulation voltage v_{AC} and current i_{AC} considering conduction losses for boost operation

4.2 Impact of the magnetizing inductance

With increasing complexity of the DAB model by including the magnetizing inductance or more complex transformer models, the modeling method using a Time Domain Model (TDM) approach is not feasible anymore. The reason for that is the increased complexity of the differential equations where a solution is not guaranteed to exist or is difficult to find and the TDM can lead to an extensive amount of case distinctions and a high amount of different time intervals that have to be analyzed [49]. Using the frequency domain modeling approach, these problems can be avoided and the complexity for high accurate DAB models is decreased [E4][50][51]. Such a Frequency Domain Model (FDM) is used in multiple applications. Most commonly it is used for optimizing the applied modulation scheme by reducing the RMS current [52][53] or to increase the ZVS operation range [51][54]. The equivalent circuit diagram used to investigate the

impact of the magnetizing inductance L_m is shown in Fig. 4.6 and consists of the lossy T-equivalent circuit of a transformer combined with the DC1 side stray inductance $L_{\sigma 1}$ and the DC2 side stray inductance $L_{\sigma 2}$. The AC resistances $R_{\mathrm{AC}1/2}$ introduced in the previous chapter are also included for this modeling approach. Assuming periodic rectangular voltage waveforms for $v_{\mathrm{AC}1}$ and $v_{\mathrm{AC}2}$ with varying duty cycle, the voltage can be expressed using a complex fourier series in (4.9) to transform them in the frequency domain. The resulting complex fourier coefficients $V_{\mathrm{AC}1,k}$ and $V_{\mathrm{AC}2,k}$ for $v_{\mathrm{AC}1}$ is shown in (4.10) and for $v_{\mathrm{AC}2}$ in (4.11) with k being the frequency index and K the highest considered harmonic. The control parameters φ, δ_1 and δ_2 of every arbitrary modulation scheme are included in these complex coefficients. Thus, all modulation schemes can be applied using the FDM without a distinction of multiple cases. To acquire the coefficients for the two AC currents $\underline{I}_{\mathrm{AC}1,k}$, $\underline{I}_{\mathrm{AC}2,k}$ and the magnetizing current $\underline{I}'_{\mathrm{m}k}$ the superposition principle is applied (this does require the assumption of a linear transformer, i.e. no saturation occurs). The two source currents $\underline{I}_{\mathrm{q,AC}1,k}$ and $\underline{I}_{\mathrm{q,AC}2,k}$ caused by their respective source are given in (4.12) and (4.13).

$$x(t) = \sqrt{2} \sum_{k=-\infty}^{\infty} \underline{C}_k e^{j\omega k} \tag{4.9}$$

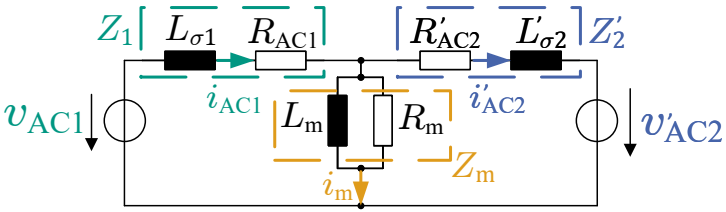


Figure 4.6: DAB model considering conduction losses and magnetizing inductance

$$\underline{V}_{\mathrm{AC}1,k} = \frac{2\sqrt{2}V_{\mathrm{DC}1}}{k\pi} \sin\left(k\frac{\pi - \delta_1}{2}\right) \qquad ,k = 1,3,5,...K \tag{4.10}$$

$$\underline{V}'_{\mathrm{AC2},k} = \frac{2\sqrt{2}V'_{\mathrm{DC2}}}{k\pi}\sin\left(k\frac{\pi-\delta_2}{2}\right)e^{-\mathrm{j}k\varphi} \qquad ,k = 1,3,5,...K \tag{4.11}$$

$$\underline{I}_{\mathrm{q,AC1},k} = \frac{2\sqrt{2}V_{\mathrm{DC1}}}{k\pi\left(\underline{Z}_{1,k}+\underline{Z}'_{2,k}||\underline{Z}_{\mathrm{m},k}\right)}\sin\left(k\frac{\pi-\delta_1}{2}\right) \tag{4.12}$$

$$\underline{I}'_{\mathrm{q,AC2},k} = \frac{2\sqrt{2}V'_{\mathrm{DC2}}}{k\pi\left(\underline{Z}'_{2,k}+\underline{Z}_{1,k}||\underline{Z}_{\mathrm{m},k}\right)}\sin\left(k\frac{\pi-\delta_2}{2}\right)e^{-\mathrm{j}k\varphi} \tag{4.13}$$

The superposition of the source currents leads to the AC currents

$$\underline{I}_{\mathrm{AC1},k} = \underline{I}_{\mathrm{q,AC1},k} - \frac{\underline{Z}_{\mathrm{m},k}}{\underline{Z}_{1,k}+\underline{Z}_{\mathrm{m},k}}\underline{I}'_{\mathrm{q,AC2},k} \tag{4.14}$$

$$\underline{I}'_{\mathrm{AC2},k} = \underline{I}'_{\mathrm{q,AC2},k} - \frac{\underline{Z}_{\mathrm{m},k}}{\underline{Z}'_{2,k}+\underline{Z}_{\mathrm{m},k}}\underline{I}_{\mathrm{q,AC1},k} \tag{4.15}$$

and the magnetizing current.

$$\underline{I}_{\mathrm{m},k} = \underline{I}_{\mathrm{AC1},k} - \underline{I}'_{\mathrm{AC2},k} \tag{4.16}$$

The resulting transferred power $P_{1/2}$ can be easily calculated using (4.17,4.18).

$$P_1 = \Re\left(\sum_{k=-K}^{K}\underline{V}_{\mathrm{AC1},k}\cdot\underline{I}^{*'}_{\mathrm{AC1},k}\right) \tag{4.17}$$

$$P_2 = \Re\left(\sum_{k=-K}^{K}\underline{V}'_{\mathrm{AC2},k}\cdot\underline{I}^{*'}_{\mathrm{AC2},k}\right) \tag{4.18}$$

The FDM does not only reduce (computational) complexity of the model but also enables the integration of the frequency dependent resistances $R_{\mathrm{AC}}(f)$ and inductances $L_\sigma(f)$ to accurately include non-ideal effects if necessary. Additionally, all modulation schemes are inherently included and nonlinear effects like the resonant commutation explained in section 4.3 can be included with minimal additional effort.

Single Phase Shift Modulation

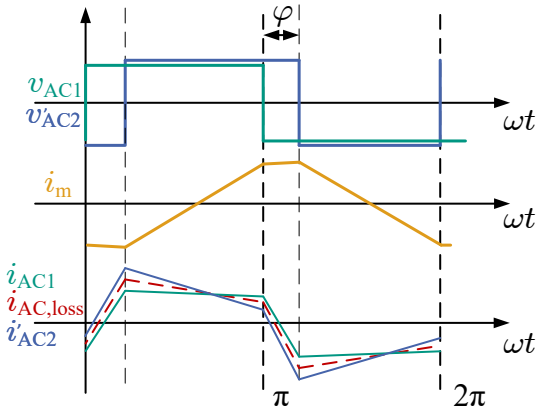


Figure 4.7: SPS modulation voltage $v_{\mathrm{AC1/2}}$, AC current $i_{\mathrm{AC1/2}}$ and magnetizing current i_{m} considering conduction losses and the magnetizing inductance compared to the lossy model

The resulting waveforms of i_{AC1} and i_{AC2} as well as i_{m} with consideration of the magnetizing inductance are shown in Fig. 4.7 for SPS. The resulting ZVS borders corresponding to the waveform shown in Fig. 4.7 are shown in Fig. 4.8 for a very low ratio $m = {}^{L_{\mathrm{m}}}/_{L_\sigma} = 10$ between stray and magnetizing inductance. Corresponding to the increased switching current $i_{\mathrm{sw,SPS,DC1/2}}$ in the waveforms, the ZVS region is increased slightly depending on m. However, for high ratios $m > 100$ the impact of the magnetizing inductance on the DAB AC current $i_{\mathrm{AC1/2}}$ waveform is negligible and does not influence the ZVS operation in a significant

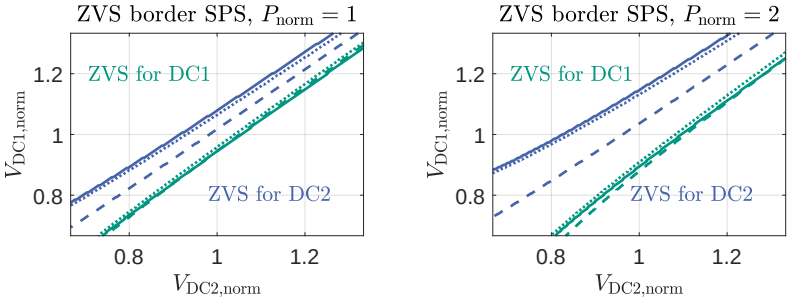


Figure 4.8: ZVS border for SPS with different normalized power P_{norm} and a small magnitizing inductance ($m = {}^{L_{\text{m}}}/_{L_\sigma} = 10$): (——)lossy model with magnetizing inductance (– –)ideal model (·····)lossy model

way. It is common to have a higher ratio than 100 but especially for high current low voltage applications, this ratio can be violated due to the very low stray inductance requirements for a DAB with low DC link voltages (cf. chapter 2.2). Therefore, an analysis of the impact of the magnetizing indutance is necessary. Additionally, it is still important to calculate the peak magnetizing current $\hat{i}_{\text{m}}$ for the design of the transformer to avoid high magnetizing losses and saturation. If it can be assumed that the time constant of the magnetizing inductance and the AC resistance $\tau_{\text{m}} = {}^{L_{\text{m}}}/_{R_{\text{AC}} \gg {}^{1}/_{f_{\text{sw}}}}$ is much larger compared to the switching period. The peak magnetizing current $\hat{i}_{\text{m}}$ can be calculated according to (4.19). It is evident, that the magnetization is at its maximum for low power P and is decreasing with an increase in power P. The resulting peak magnetizing current $\hat{i}_{\text{m,SPS}}$ is shown in Fig. 4.9 (a).

$$\hat{i}_{\text{m,SPS}} \approx \frac{\pi - \varphi}{2\pi f_{\text{sw}}} \cdot \left[\left(1 - \frac{L_{\text{m}}}{L_{\sigma 2} + L_{\text{m}}} \right) \frac{V_{\text{DC1}}}{L_{\sigma 1} + L_{\sigma 2} || L_{\text{m}}} + \left(1 - \frac{L_{\text{m}}}{L_{\sigma 1} + L_{\text{m}}} \right) \frac{V_{\text{DC2}}}{L_{\sigma 2} + L_{\sigma 1} || L_{\text{m}}} \right] \tag{4.19}$$

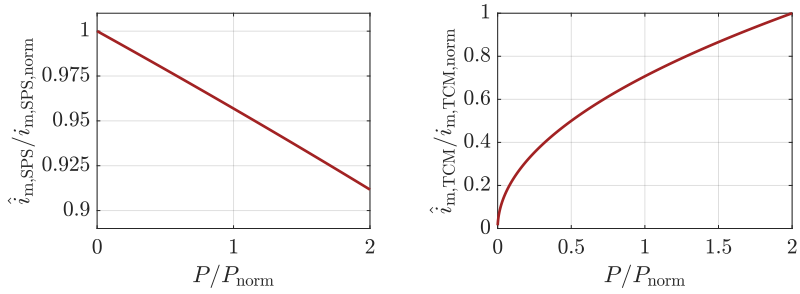


Figure 4.9: $\hat{i}_{\mathrm{m}}$ with different transferred power for (a) SPS with $V_{\mathrm{DC1}} = V_{\mathrm{DC2}} = V_{\mathrm{DC,norm}}$ and (b) TCM with $V_{\mathrm{DC1}} = V_{\mathrm{DC,norm}} = 0.75 \cdot V_{\mathrm{DC2}}$

Triangular Current Modulation

In case of TCM the impact of the magnetizing inductance is shown in Fig. 4.10. Similar to SPS the current in DC1 and DC2 side i_{AC1} and i'_{DC2} is changed according to (4.16). This results in a slightly higher circular current in the DC2 side compared to DC1. However, similar to SPS the impact is negligible if the ratio $m = {}^{L_{\mathrm{m}}}/_{L_\sigma} > 100$ is high enough.
Similar to the SPS operation, the peak magnetizing current $\hat{i}_{\mathrm{m,TCM}}$ for TCM can be calculated in (4.20) if the time constant $\tau_{\mathrm{m}} = {}^{L_{\mathrm{m}}}/_{R_{\mathrm{AC}}}$ is large.

$$\hat{i}_{\mathrm{m,TCM}} \approx \left[\left(1 - \frac{L_{\mathrm{m}}}{L_{\sigma 2} + L_{\mathrm{m}}}\right) \frac{V_{\mathrm{DC1}}}{L_{\sigma 1} + L_{\sigma 2} || L_{\mathrm{m}}}\right] \frac{\delta_2 - \delta_1}{2 \cdot 2\pi f_{\mathrm{sw}}} + \left[\left(1 - \frac{L_{\mathrm{m}}}{L_{\sigma 2} + L_{\mathrm{m}}}\right) \frac{V_{\mathrm{DC1}}}{L_{\sigma 1} + L_{\sigma 2} || L_{\mathrm{m}}} + \left(1 - \frac{L_{\mathrm{m}}}{L_{\sigma 1} + L_{\mathrm{m}}}\right) \frac{V_{\mathrm{DC2}}}{L_{\sigma 2} + L_{\sigma 1} || L_{\mathrm{m}}}\right] \frac{\pi - \delta_2}{2 \cdot 2\pi f_{\mathrm{sw}}} \tag{4.20}$$

The resulting peak magnetizing current is shown in Fig. 4.9 (b). In contrast to SPS operation, for TCM the magnetization is increasing with the transferred power P.

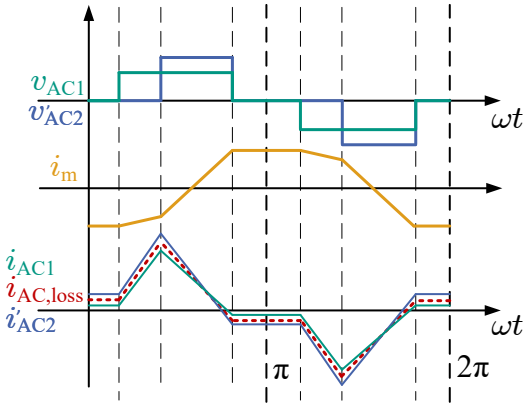


Figure 4.10: TCM modulation voltage v_{AC} and current i_{AC} considering conduction losses and the magnetizing inductance

4.3 Resonant ZVS commutation

In this section the impact of resonant ZVS commutation on the efficiency and operation of the DAB is analyzed. An analytical time-domain model is presented, which uses an equivalent capacitance model to represent the nonlinear MOSFET output capacitances. This time-domain model is applied to determine different ZVS cases, the optimal deadtime T_{dt} depending on the operating point, and its influence on the transfer characteristics of the DAB.

4.3.1 Nonlinear MOSFET Capacitance C_{OSS}

The p-n junction structure of the vertical power MOSFET, depicted in Fig. 4.11 (a), results in unavoidable parasitic capacitances due to the parallel areas. These capacitances, along with their representation in an equivalent circuit diagram, are illustrated in Fig. 4.11 (b). For applications involving soft switching and ZVS modeling, the output capacitance C_{OSS}, as defined in (4.21) (see Fig. 4.11 (b)), is the most relevant. This is because this parasitic capacitance has to be fully charged and discharged for ZVS operation. Therefore, only the Drain-Source C_{DS} and Gate-Drain C_{GD} capacitances are considered in the following analysis

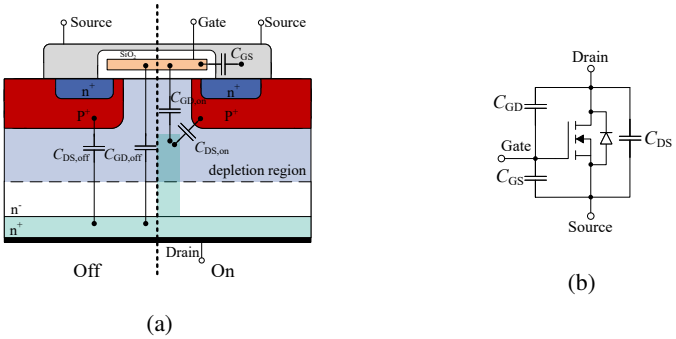


Figure 4.11: (a) Cross section of a vertical power MOSFET with parasitic capacitances in off (left hand side) and on (right hand side) state (b) equivalent circuit diagram with parasitic capacitances of a MOSFET

[55]. Both C_{DS} and C_{GD} are highly dependent on the thickness and width of the depletion region. Since the depletion region is determined by the applied Drain-Source voltage V_{DS}, the capacitances exhibit significant nonlinearity relative to this voltage. A reduction in V_{DS} increases the internal surface area of the n+ to p+/gate region and decreases the spacing of the p-n junction in the depletion region. Consequently, both capacitances increase, as demonstrated for C_{OSS} in Fig. 4.12 (a) [56].

$$C_{OSS}(V_{DS}) = C_{DS}(V_{DS}) + C_{GD}(V_{DS} - V_{GS}) \tag{4.21}$$

The voltage-dependent output capacitance $C_{OSS}(V_{DS})$ of the first- and second-generation 1200V/1200A SiC MOSFET modules FMF12001200DX1-24A and FMF1200DXZ-24B, respectively [D1] [D2], by *Mitsubishi Electric*, is shown in Fig. 4.12 (a). A significant nonlinearity in the output capacitance can be observed, which prevents the derivation of a closed-form analytical expression for the ZVS behavior of the DAB, considering this nonlinear and voltage-dependent characteristic. Therefore, an equivalent capacitance is introduced in order to simplify the system. Two types of equivalent capacitances are distinguished: a charge equivalent capacitance $C_{Q,eq}$, which stores the same charge at a given voltage V_{DS} as the nonlinear capacitance, and an energy equivalent capacitance

$C_{\mathrm{E,eq}}$, which stores the same energy as the nonlinear capacitance [57]. $C_{\mathrm{Q,eq}}$ and $C_{\mathrm{E,eq}}$ are given in (4.22) and (4.23), respectively. The resulting equivalent capacitances $C_{\mathrm{eq}}(V_{\mathrm{DS}})$ and the corresponding charge $Q_{\mathrm{OSS}}(V_{\mathrm{DS}})$ at a specific voltage V_{DS} are shown in Fig. 4.12 (b) and (c).

$$C_{\mathrm{Q,eq}}(V_{\mathrm{DS}}) = \frac{\int_0^{V_{\mathrm{DS}}} C_{\mathrm{OSS}}(v)\mathrm{d}v}{V_{\mathrm{DS}}} \tag{4.22}$$

$$C_{\mathrm{E,eq}}(V_{\mathrm{DS}}) = \frac{2 \cdot \int_0^{V_{\mathrm{DS}}} v \cdot C_{\mathrm{OSS}}(v)\mathrm{d}v}{{V_{\mathrm{DS}}}^2} \tag{4.23}$$

Using the corresponding value, the nonlinear voltage-dependent output capacitance $C_{\mathrm{OSS}}(V_{\mathrm{DS}})$ can be approximated by a constant equivalent capacitance C_{eq}, which behaves similarly at a specific DC link voltage V_{DC}. This approximation eliminates the voltage dependency for the charging and discharging of the output capacitance. However, this can introduce inaccuracies in the modeling process, particularly when analyzing the time course of the Drain-Source voltage V_{DS}. As shown in Fig. 4.12, both the energy- and charge-based capacitances vary due to the nonlinear nature of the output capacitance. The ratio between these two capacitances can range from $C_{\mathrm{E,eq}}/C_{\mathrm{Q,eq}} = 1.5..5$, depending on the MOSFET technology investigated. For example, superjunction MOSFETs exhibit a higher ratio, typically around 4..5 [57], whereas the applied FMF1200 modules are showing a ratio of only 1.5 for both generations. When calculating a ZVS switching event, the charge-based capacitance $C_{\mathrm{Q,eq}}$ has to be used, as the corresponding amount of charge is required to fully discharge or charge the MOSFET's output capacitance C_{OSS} [58].

4.3.2 Capacitance based Time Domain Model

To investigate the resonant ZVS transition for a DAB, a switching event on the DC1 side during the turn-off of switch T1 and turn-on of switch T2 is discussed. However, all other switching events can also be calculated by adjusting the initial conditions accordingly and transforming all relevant variables to the transformer side of the switching event. To model the resonant commutation process for ZVS operation, all relevant values are calculated in the time domain based on the equivalent nonlinear output capacitance discussed earlier. The Capacitance based Time Domain (CTD) model is based on [E5], [59], and [E6]. All calcula-

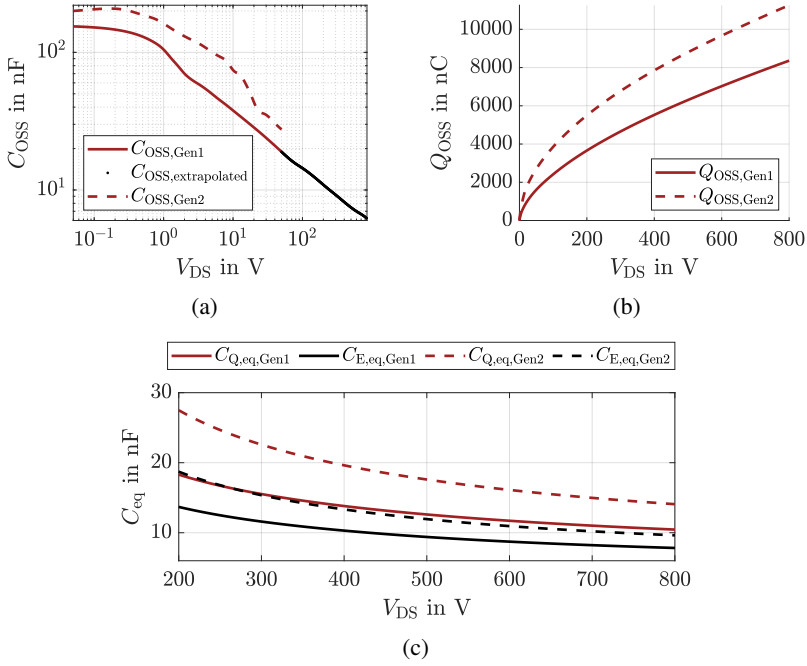


Figure 4.12: (a) Extrapolated nonlinear output capacitance $C_{\mathrm{OSS}}(V_{\mathrm{DS}})$ (b) Drain Source charge $Q_{\mathrm{OSS}}(V_{\mathrm{DS}})$ (c) Equivalent capacitances $C_{\mathrm{Q,eq}}(V_{\mathrm{DS}})$ and $C_{\mathrm{E,eq}}(V_{\mathrm{DS}})$

tions in this chapter are valid only within the range of the deadtime $0 \leq t \leq T_{\mathrm{dt}}$, as modeling the switching behavior after the turn-on instant is not possible using the CTD model. This is because the switching behavior of the MOSFET dominates beyond that point. Additionally, the AC resistance R_{AC} is not considered to simplify the analysis. While it is possible to include the resistance, for all relevant DAB designs, the resistance does not meaningfully affect the commutation process since the time constant of L_σ/R_{AC} is much higher than the deadtime T_{dt}.

Modeling in Time Domain

Figure 4.13 shows the equivalent circuit diagram of the DAB. For a switching event on the DC1 side, without overlap of a DC2-side switching event, the FB on the DC2 side can be modeled as a constant voltage source and is defined as the opposing voltage v'_{opp} of the commutation process. The DC1 side (switching side) can be reduced to a capacitance network with the initial condition of $v_{\mathrm{AC1}} = V_{\mathrm{sw}}$ and the initial switching current $i_{\mathrm{AC}} = i_{\mathrm{sw}}$. This results in an LC-series resonant circuit with a constant voltage source, where the inductance is $L = L_\sigma$ and the capacitance is C_{eq}, which includes all transistor capacitances $C_{\mathrm{T}} = C_{\mathrm{Q,eq}} + C_{\mathrm{par}}$ involved in the commutation process. Here, $C_{\mathrm{Q,eq}}$ represents the charge-equivalent output capacitance of each switch, while C_{par} refers to additional external capacitances parallel to the switches, caused by components such as the snubber circuit, transformer, inductor, PCB, or cables. The ratio between $C_{\mathrm{Q,eq}}$ and C_{par} can vary significantly depending on the power level. In PCB-based DAB systems, the capacitance between the DC and AC layers have values comparable to the switches' output capacitance $C_{\mathrm{Q,eq}}$. In high-power DAB systems without a PCB design in the power circuit, the switch capacitance dominates the ZVS behavior. However, when a snubber is applied, the additional capacitance C_{par} must be considered in all systems, as it typically ranges from two to ten times the value of $C_{\mathrm{Q,eq}}$. The resulting equivalent capacitance C_{eq} for each possible switching event is shown in Table 4.1 (for $C_{\mathrm{DC}} \gg C_{\mathrm{Q,eq}}$ and identical switches in each FB) and is the only capacitance needed to model all active capacitances for each commutation process. The possible switching events are as follows:

- HB: Only one HB is switching at the same time (typical for TCM)
- FB: Only one FB is switching at the same time (typical for SPS)
- FB + HB: One FB on one of the DAB sides and one HB on the other side is switching at the same time

Table 4.1: Equivalent capacitances $C_{\mathrm{eq,DC1}}$ for different switching events on the DC1 side with $C_{\mathrm{DC}} \gg C_{\mathrm{Q,eq}}$ and identical switches on each FB

	C_{eq}	$C_{\mathrm{eq}}\vert_{C_{\mathrm{T,DC1}}=C'_{\mathrm{T,DC2}}=C_{\mathrm{T}}}$
HB	$2 \cdot C_{\mathrm{T,DC1}}$	$2 \cdot C_{\mathrm{T}}$
FB	$C_{\mathrm{T,DC1}}$	C_{T}
FB + HB	$\frac{2C_{\mathrm{T,DC1}}C'_{\mathrm{T,DC2}}}{C_{\mathrm{T,DC1}}+2C'_{\mathrm{T,DC2}}}$	$\frac{2}{3}C_{\mathrm{T}}$
HB + HB	$\frac{2C_{\mathrm{T,DC1}}C'_{\mathrm{T,DC2}}}{C_{\mathrm{T,DC1}}+C'_{\mathrm{T,DC2}}}$	C_{T}
FB + FB	$\frac{C_{\mathrm{T,DC1}}C'_{\mathrm{T,DC2}}}{C_{\mathrm{T,DC1}}+C'_{\mathrm{T,DC2}}}$	$\frac{1}{2}C_{\mathrm{T}}$

- HB + HB: One HB on one of the DAB sides and one HB on the other side is switching at the same time (typical for TCM)
- FB + FB: One FB on one of the DAB sides and one FB on the other side is switching at the same time (can appear in SPS operation at low load)

In order to reduce complexity, the magnetizing inductance L_{m} is not considered in this modeling approach. This is due to the fact that in real-world systems, the ratio between the magnetizing and stray inductances $m = L_{\mathrm{m}}/L_{\sigma} > 100$ is sufficiently large to assume a minimal impact. Using this LC-series resonant circuit, the AC current $i_{\mathrm{AC}}(t)$ can be calculated as shown in (4.24). The current consists of two resonant oscillations, which depend on the current at the start of the commutation i_{sw} and the voltage difference between the initial voltage and the opposing voltage $V_{\mathrm{sw}} - v'_{\mathrm{opp}}$. The defining system parameters for the ZVS behavior of the DAB are the MOSFET capacitances, described by C_{eq} (which is the whole capacitance network), and the inductance of the AC circuit L_{σ}.

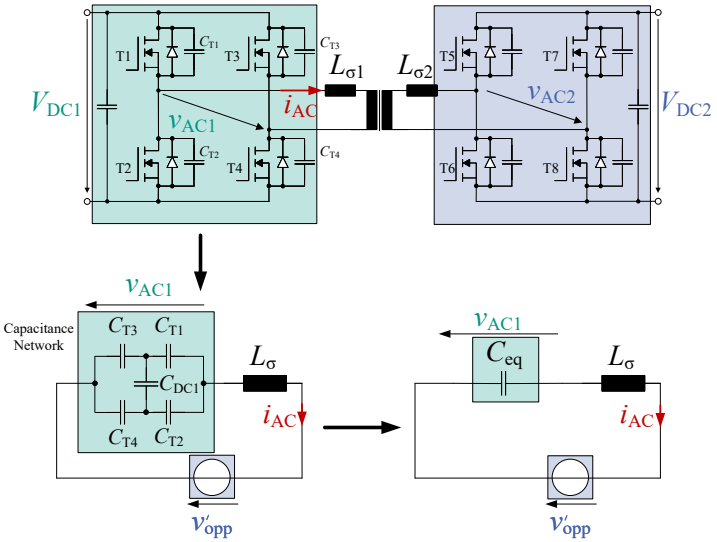


Figure 4.13: Equivalent circuit diagram for the resonant commutation of DC1 side with full bridge commutation

$$i_{AC}(t) = i_{sw} \cdot \cos\left(\frac{t}{\sqrt{L_\sigma C_{eq}}}\right) + \sqrt{\frac{C_{eq}}{L_\sigma}}(V_{sw} - v'_{opp}) \sin\left(\frac{t}{\sqrt{L_\sigma C_{eq}}}\right) \quad (4.24)$$

The resulting AC voltage v_{AC1} can be obtained by integrating the current from (4.24) over the time t and dividing it by the equivalent capacitance C_{eq}:

$$v_{AC1}(t) = -\sqrt{\frac{L_\sigma}{C_{eq}}} \cdot i_{sw} \cdot \sin\left(\frac{t}{\sqrt{L_\sigma C_{eq}}}\right) + (V_{sw} - v'_{opp})\left(\cos\left(\frac{t}{\sqrt{L_\sigma C_{eq}}}\right) - 1\right) + V_{DC1} \quad (4.25)$$

Using (4.25) gives the corresponding transistor voltage $v_{\mathrm{T,on/off}}$ of the turned-on/off MOSFET:

$$v_{\mathrm{T,on}}(t) = \frac{1}{2}\left[-\sqrt{\frac{L_\sigma}{C_{\mathrm{eq}}}} \cdot i_{\mathrm{sw}} \cdot \sin\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) + (V_{\mathrm{sw}} - v'_{\mathrm{opp}})\left(\cos\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) - 1\right)\right] + V_{\mathrm{DC1}} \quad (4.26)$$

$$v_{\mathrm{T,off}}(t) = -\frac{1}{2}\left[-\sqrt{\frac{L_\sigma}{C_{\mathrm{eq}}}} \cdot i_{\mathrm{sw}} \cdot \sin\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) + (V_{\mathrm{sw}} - v'_{\mathrm{opp}})\left(\cos\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) - 1\right)\right] \quad (4.27)$$

However, these equations only hold true if the LC-resonant circuit has a linear behavior. If the anti-parallel diodes of the MOSFETs are conducting, the ZVS gets nonlinear and the commutation process cannot be described as a resonant circuit anymore. This happens if the AC current i_{AC} does not provide a natural commutation process due to having the wrong sign at the start of the commutation process ($t = 0$) or the output capacitance C_{OSS} is fully charged/discharged at $T = T_{\mathrm{d,cond}}$. The resulting equations in order to piece-wise calculate the resulting transistor voltages $v_{\mathrm{T,on/off}}$ are given in (4.28,4.29). To simplify the equations, the forward voltage of the diodes is assumed to be zero. The resulting AC current i_{AC} is given in (4.30).

$$v_{\mathrm{T,on}} \approx \begin{cases} 0\,\mathrm{V} & \text{fully charged} \\ V_{\mathrm{DC1}} & \text{no natural commutation} \end{cases} \quad (4.28)$$

$$v_{\mathrm{T,off}} \approx \begin{cases} V_{\mathrm{DC1}} & \text{fully charged} \\ 0\,\mathrm{V} & \text{no natural commutation} \end{cases} \quad (4.29)$$

$$i_{\mathrm{AC}} = \frac{v_{\mathrm{AC1}} - v'_{\mathrm{opp}}}{L_\sigma} t \begin{cases} i_{\mathrm{AC}}(t = T_{\mathrm{d,con}}) & \text{fully charged} \\ i_{\mathrm{AC}}(t = 0) & \text{no natural commutation} \end{cases} \quad (4.30)$$

Based on the presented expressions in (4.24)-(4.29) three system parameters can be defined which have a decisive influence on the ZVS resonant transition:

- L_σ: AC circuit stray inductance
- C_T: Equivalent semiconductor output capacitance including external capacitances
- T_dt: Deadtime between turn-off and turn-on

as well as three operation point dependent parameter:

- i_sw: semiconductor current at start of the resonant commutation
- V_sw: semiconductor voltage at start of the resonant commutation (usually the DC link voltage)
- v'_opp: Opposing voltage of the other fullbridge

Depending on these parameters different ZVS cases can occur and are analyzed in the following.

Possible ZVS cases

1. complete Zero Voltage Switching (cZVS)
2. incomplete Zero Voltage Switching due to current (iZVS-C)
3. incomplete Zero Voltage Switching due to deadtime (iZVS-D)

cZVS occurs when the output capacitance of the MOSFET being turned on is fully discharged before the turn-on event. This significantly reduces turn-on losses, making it the preferred switching behavior. An example of the waveform for cZVS can be seen in Fig. 4.14, where the turn-on occurs between the black dotted line and approximately $t = 280$ ns with zero turn on losses due to no voltage drop at the turned-on MOSFET.

iZVS-C occurs when the energy stored in the inductor L_σ is insufficient to fully charge or discharge the equivalent capacitance C_eq, and thus the fundamental equation (4.31) is not satisfied. This leads to a remaining voltage $v_\mathrm{T,on}(T_\mathrm{dt}) \neq 0$ for the MOSFET being turned on at the end of the deadtime T_dt. As a result, turn-on losses are reduced but not completely eliminated, making these operating points undesirable for achieving maximum efficiency.

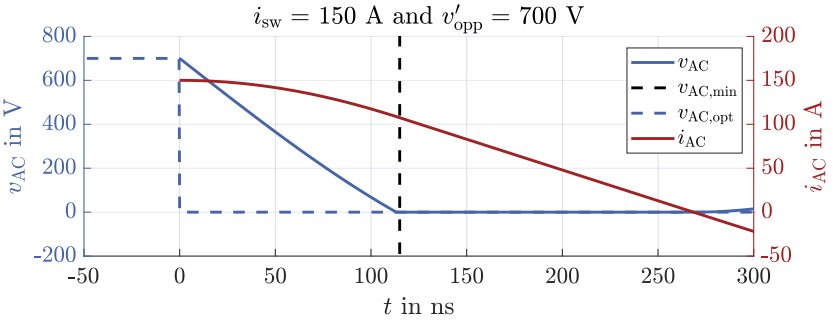


Figure 4.14: FB resonant commutation process for cZVS

$$\frac{1}{2}L_\sigma i_{sw}^2 \geq \frac{1}{2}C_{eq}(V_{DC})V_{DC}^2 \tag{4.31}$$

Starting with (4.31) and (4.27), the minimal necessary current $i_{sw,min}$ for HB and FB commutation can be calculated. The FB resonant commutation process for iZVS-C is illustrated in Fig. 4.15, where the minimum voltage $v_{AC,min}$ is higher than V_{DC}, resulting in a residual voltage at the turned-on MOSFET and consequently leading to turn-on losses higher than 0. For HB, the necessary current $i_{sw,min,HB}$ is given in (4.32). For opposing voltages below $v'_{opp} < 1/2 V_{sw}$, cZVS is always achieved since the energy provided by the DC2 side is enough to fully charge/discharge the output capacitances on the DC1 side and achieve cZVS (if the deadtime T_{dt} is sufficient cf. section 4.3.3). For FB commutation the same behavior can be observed but the opposing voltage has to be smaller than zero $v'_{opp} < 0$ to always achieve cZVS. The minimal current $i_{sw,min,FB}$ is shown in (4.34) if the previous condition is not fulfilled. In Fig. 4.16 the minimal switching current $i_{sw,min}$ for cZVS is shown for different ratios of V_{sw}/v'_{opp}. With an increase in V_{sw} more charge is necessary which results in an increase in the minimal current. For HB commutation, the minimal current is decreasing at around $V_{sw} = v_{AC}$ because the secondary side provides more energy to the system to further charge the capacitances than the total charge of the output capcitance is increasing. Figure 4.17 does show the resulting minimal current $i_{sw,min}$ to achieve cZVS with a constant initial switching voltage V_{sw}. The minimal switching current for HB switching is always smaller compared ot FB even

with the higher equivalent capacitance C_{eq}. This is due to the doubled voltage amplitude in case of FB commutation.

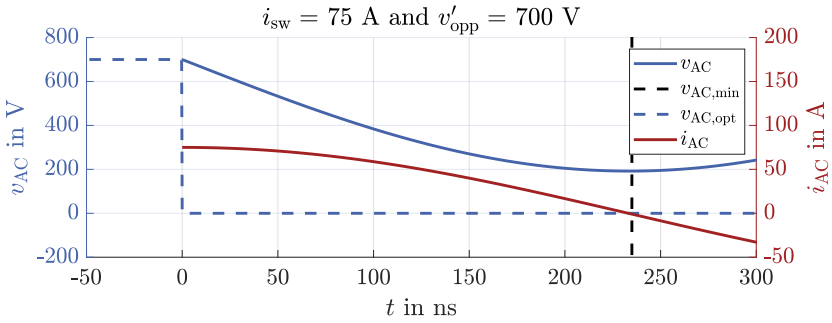


Figure 4.15: FB resonant commutation process for iZVS-C

$$i_{sw,min,HB} = \sqrt{\frac{C_{eq}}{L_\sigma} \cdot (2 \cdot v'_{opp} V_{sw} - V_{sw}^2)} \quad \text{for} \quad v'_{opp} > 1/2 \cdot V_{sw} \tag{4.32}$$

$$v_{T,on}(T_{dt,iZVS}) \leq 0 \tag{4.33}$$

Simplifying (4.33) leads to:

$$i_{sw,min,FB} = \frac{2 \cdot \sqrt{L_\sigma \cdot C_{eq} \cdot V_{sw} \cdot v'_{opp}}}{L_\sigma} \quad \text{for} \quad v'_{opp} > 0 \tag{4.34}$$

iZVS-D occurs when the deadtime is either too short to fully discharge the output capacitance of the turned-on MOSFET or too long, causing the AC voltage v_{AC} to swing back. Both cases can be observed in Fig. 4.15. If the deadtime T_{dt} deviates from the value marked by the black dotted line, a higher voltage V_{DS} remains at the turned-on MOSFET, resulting in increased switching losses. The optimal deadtime $T_{dt,opt}$ is investigated in the following section.

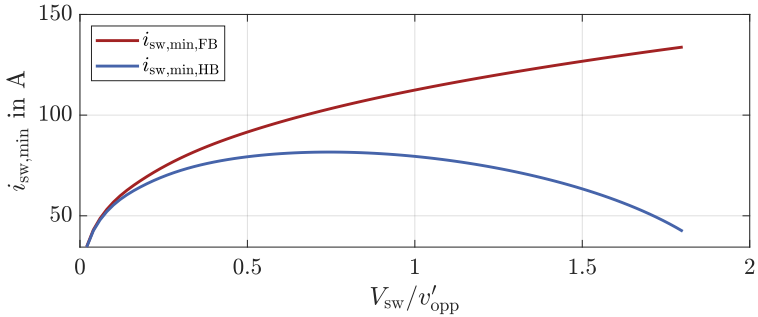


Figure 4.16: Minimal necessary current to achieve cZVS for a constant positive opposing voltage v'_{opp}

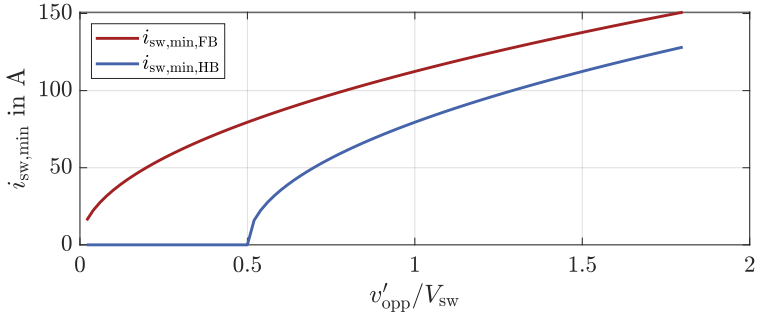


Figure 4.17: Minimal necessary current to achieve cZVS for a constant positive switching voltage V_{sw}

Impact of the opposing voltage

The resonant commutation process in (4.25) consists of two superimposed sine and cosine oscillations: one part is dependent on the initial current i_{sw}, and the other part on the voltage difference $V_{\mathrm{sw}} - v'_{\mathrm{opp}}$. The superposition of these oscillations results in a sinusoidal wave with varying phase and amplitude, depending on the ratio between the two parts. The phase shift is zero when the voltage difference is zero, i.e., $V_{\mathrm{sw}} - v'_{\mathrm{opp}} = 0$. Figure 4.18 shows the effect of varying the

opposing voltage v'_{opp}. The colored region of the plot indicates the resonant oscillations, while the grayed-out area represents the continuation of the voltage if no clamping diodes were present. It is evident that the difference between V_{sw} and v'_{opp} alters both the amplitude and phase shift of the resonant commutation process. When $V_{\mathrm{sw}} > v'_{\mathrm{opp}}$, a positive phase shift occurs, and the amplitude increases. Conversely, for a negative voltage difference, the phase shift is negative, and the amplitude is reduced. This is because a smaller opposing voltage supports the resonant commutation, whereas a negative difference has the opposite effect.

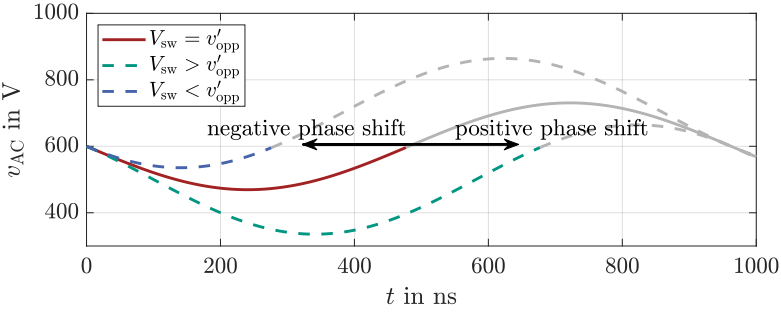


Figure 4.18: Impact of the opposing voltage v_{AC} on the resonant commutation with gray beeing the continuation if there were no clamping diodes (equal switching currents for all curves)

4.3.3 Optimal Deadtime

Looking at the resonant commutation process illustrated in Fig. 4.19 and 4.20, the significance of the optimal deadtime becomes apparent. If the energy stored in the inductor $E_{\mathrm{L}\sigma}$ is insufficient to achieve cZVS, only a small time window allows for minimal switching losses since a swing back of the voltage occurs after that time window and the residual voltage is increasing again. This window, highlighted in green in Fig. 4.19, represents the optimal deadtime $T_{\mathrm{dt,opt}}$. Although the optimal deadtime technically corresponds to a single point at the minimum of the AC voltage v_{AC}, minor deviations from this point due to resonant oscillations do not significantly increase switching losses since the steepness of the AC voltage is low at the minimum due to the sinusoidal characteristic. Based

on this insight, the optimal deadtime for achieving cZVS can be determined by identifying the minimum of v_{AC}, as expressed in (4.35). If cZVS is achievable, satisfying the conditions in (4.32) and (4.34) for HB and FB commutation, respectively, Fig. 4.20 illustrates the typical waveforms. In contrast to the iZVS-C scenario described earlier, the range for the optimal deadtime $\Delta T_{\mathrm{dt,iZVS}}$ is considerably broader and expands with increasing switching current i_{sw}. This window, in which cZVS and thus minimum switching losses are achieved, is marked by the red highlighted area in Fig. 4.20. To identify the lower limit of this range, the point at which the diodes start to clamp the AC voltage must be determined, as represented by (4.36) and (4.37) for FB and HB, respectively. The upper limit can be attained by employing (4.30) to calculate the time of zero crossing. However, due to the nonlinear behavior of the diodes, an analytical expression for this upper limit is not feasible and requires a numerical solution.

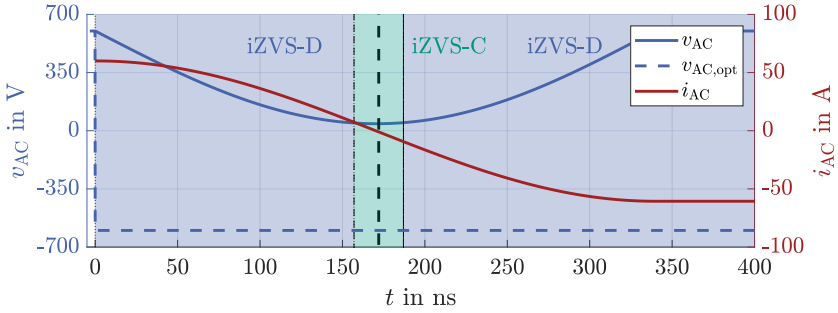


Figure 4.19: iZVS-C with optimal deadtime for FB commutation

$$T_{\mathrm{dt,iZVS}} = \sqrt{b} \begin{cases} \left(\pi - \arctan\left(\dfrac{i_{\mathrm{sw}}\sqrt{a}}{V_{\mathrm{sw}} - v'_{\mathrm{opp}}} \right) \right) & \text{for } V_{\mathrm{sw}} \geq v'_{\mathrm{opp}} \\ \left(-\arctan\left(\dfrac{i_{\mathrm{sw}}\sqrt{a}}{V_{\mathrm{sw}} - v'_{\mathrm{opp}}} \right) \right) & \text{for } V_{\mathrm{sw}} < v'_{\mathrm{opp}} \end{cases} \tag{4.35}$$

with $a = \dfrac{L_\sigma}{C_{\mathrm{eq}}}$ and $b = L_\sigma C_{\mathrm{eq}}$

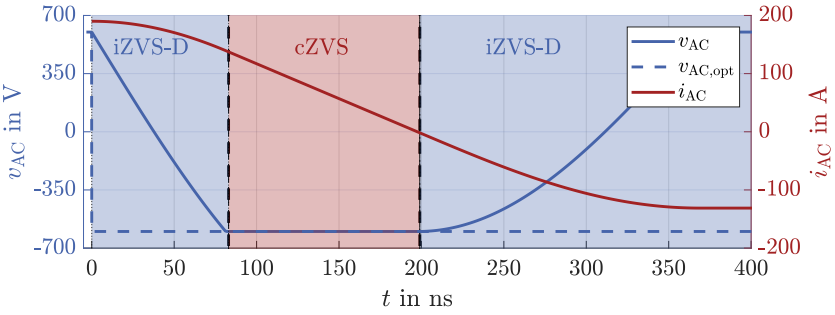


Figure 4.20: iZVS-D with optimal deadtime for FB commutation

$$T_{\mathrm{dt,FB,cZVS}} = \pm\sqrt{b}\arccos\left(\frac{\pm\sqrt{a^2 i_{\mathrm{sw}}^4 - 4ai_{\mathrm{sw}}^2 V_{\mathrm{sw}} v'_{\mathrm{opp}}} - V_{\mathrm{sw}}^2 + {v'_{\mathrm{opp}}}^2}{ai_{\mathrm{sw}}^2 - 2V_{\mathrm{sw}} v'_{\mathrm{opp}} + V_{\mathrm{sw}}^2 + {v'_{\mathrm{opp}}}^2}\right) \tag{4.36}$$

$$T_{\mathrm{dt,HB,cZVS}} = \pm\sqrt{b}\arccos\left(\frac{\pm\sqrt{a^2 i_{\mathrm{sw}}^4 - 2ai_{\mathrm{sw}}^2 V_{\mathrm{sw}} v'_{\mathrm{opp}}} - V_{\mathrm{sw}} v'_{\mathrm{opp}} + {v'_{\mathrm{opp}}}^2}{ai_{\mathrm{sw}}^2 - 2V_{\mathrm{sw}} v'_{\mathrm{opp}} + V_{\mathrm{sw}}^2 + {v'_{\mathrm{opp}}}^2}\right) \tag{4.37}$$

Analyzing the obtained deadtime for iZVS-C, iZVS-D and cZVS, it can be observed that the superposition of the two sinusoidal oscillations will result in a oscillation with different amplitude and phase depending on the difference between switching voltage V_{sw} and opposing voltage v'_{opp}. Four different cases can be observed:

1. $V_{\mathrm{sw}} = v'_{\mathrm{opp}}$
2. $V_{\mathrm{sw}} > v'_{\mathrm{opp}}$
3. $V_{\mathrm{sw}} < v'_{\mathrm{opp}}$
4. $v'_{\mathrm{opp}} < 0$ for FB or $v'_{\mathrm{opp}} < 0.5V_{\mathrm{sw}}$ for HB

Case 1. $V_{sw} = v'_{opp}$**:** If both DC sides of the DAB have the same DC link voltage V_{DC} and both AC voltages v_{AC} have the same polarity at the start of the commutation process, the deadtime characteristic is shown in Fig. 4.21 (a). In this case, only iZVS-C can be achieved up to the cZVS boundary, as indicated by the dashed line (– –). The optimal deadtime for this region remains constant with increased switching current. Once the cZVS boundary is crossed, complete Zero Voltage Switching (cZVS) can be achieved, as depicted in the red area. If the deadtime T_{dt} is too long or too short, switching losses may still occur, as indicated in the blue area. To minimize switching losses, the deadtime must lie within the red region.

Case 2. $V_{sw} > v'_{opp}$**:** For a switching voltage V_{sw} greater than the opposing voltage v'_{opp}, the AC current i_{AC} continues to increase after the start of the commutation process until the AC voltage on the switching side $v_{AC,sw}$ drops below the voltage on the opposing side $v_{AC,sw} < v'_{opp}$. This corresponds to a negative phase shift of the resonant commutation waveform, leading to a reduced minimum current required for cZVS and a longer deadtime needed to achieve the minimum of the resonant commutation for small switching currents i_{sw} (cf. Fig. 4.18). The resulting deadtime characteristic is shown in Fig. 4.21 (b).

Case 3. $V_{sw} < v'_{opp}$**:** If the opposing voltage v'_{opp} is higher than the switching voltage V_{sw}, a higher switching current i_{sw} is necessary for cZVS, as the opposing voltage further reduces the current during the commutation process. This is similar to a positive phase shift of the resonant commutation, resulting in a shorter optimal deadtime but a higher residual AC voltage for the same switching current i_{sw} (cf. Fig. 4.18). The corresponding deadtime characteristic is shown in Fig. 4.21 (c).

Case 4. Negative opposing voltage: If the opposing voltage v'_{opp} is negative for FB or lower than $v'_{opp} < 0.5V_{sw}$ for HB commutation, cZVS can always be achieved by appropriately selecting the deadtime, as the negative opposing voltage supports the commutation process. The deadtime characteristic is shown in Fig. 4.21 (d).

4.3.4 Loss characteristic for the resonant commutation

Given an optimal deadtime $T_{dt,opt}$, two primary scenarios can be distinguished: iZVS-C and cZVS. These two cases exhibit distinctly different loss characteris-

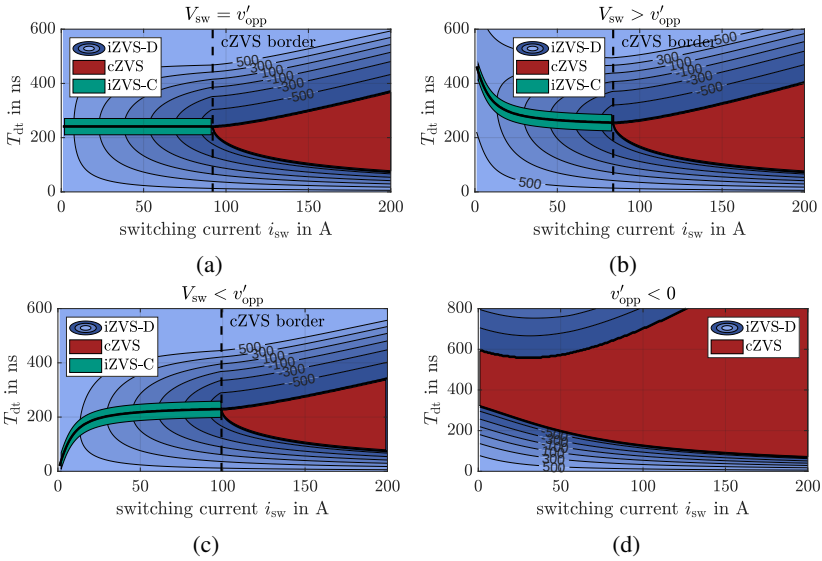


Figure 4.21: Deadtime T_{dt}, ZVS regions and residual voltage in case of iZVS for FB commutation with $V_{DC1} = 500$ V (a) $V_{sw} = v'_{opp}$ (b) $V_{sw} > v'_{opp}$ (c) $V_{sw} < v'_{opp}$ (d) $v'_{opp} < 0$

tics. In ZVS operation, the turn-off losses E_{off} are not directly influenced by the deadtime, causing them to increase monotonically with the switching current i_{sw}. This behavior contrasts with the turn-on losses E_{on}, which vary significantly depending on the specific ZVS condition. In the iZVS-C region, the turn-on losses decrease with increasing switching current i_{sw}, primarily due to the lower turn-on voltage at the end of the deadtime. As the ZVS boundary is reached, the turn-on losses approach zero and may even become slightly negative. This negative turn-on energy results from the circulating energy between the turn-on and turn-off switching events caused by the parasitic MOSFET output capacitance C_{OSS} and represents the surge current within a single FB. This behavior is illustrated in Fig. 4.22, where the half-bridge energy E_{HB} is defined as the sum of turn-on and turn-off energy (4.38). Within the iZVS-C region, the half-bridge energy for a single switching event decreases until the ZVS boundary is reached. Beyond this boundary, the losses are predominantly determined by the turn-off energy E_{off}. In the iZVS-D region, however, the minimum turn-on energy E_{on} shifts towards

higher switching currents i_{sw}, causing the point of minimum losses to also shift to higher switching current levels. This is also depicted in Fig. 4.22 with the blue lines which are representing a higher deviation of the optimal deadtime ΔT_{dt}. It should be noted that for significantly higher switching currents than required to achieve cZVS, the half-bridge energy E_{HB} becomes almost independent of the deadtime T_{dt}. This is because the turn-off losses dominate, and the impact of the deadtime on the overall loss characteristic diminishes.

$$E_{HB} = E_{on} + E_{off} \tag{4.38}$$

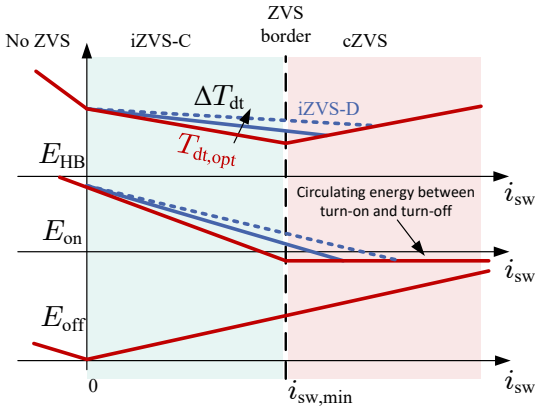


Figure 4.22: Loss Characteristic for a half bridge resonant commutation event

4.3.5 Voltage Time Area Error

Analyzing the resonant commutation waveform of the AC current i_{AC} and the AC voltage v_{AC} in Fig. 4.23, it is evident that the observed waveforms deviate significantly from the ideal resonant behavior. To quantify this deviation, the Voltage Time Area Error (VTAE) $\Phi_{error,AC}$ can be defined as the difference between the ideal AC voltage v_{AC} of the commutation process and the actual resonant AC voltage (cf. (4.39)). This VTAE leads to substantial deviations in

the AC current i_{AC}, which can cause the DAB converter to exhibit behaviors that differ from those predicted by the ideal model. To incorporate this effect into the DAB modeling process, it can be assumed that the AC voltage v_{AC} remains constant over the entire deadtime T_{dt} and has the same VTAE compared to the previously calculated waveform. Based on this assumption, a rectangular VTAE signal can be introduced into the Fourier series of the FDM to account for the nonlinearities observed during commutation (cf. Fig. 4.24). The resulting Fourier coefficient, shown in (4.40), consists of the ideal AC voltage coefficient $\underline{V}_{AC,k}$ and an additional term that accounts for the VTAE, represented as N rectangular components with an amplitude of $\Phi_{error,AC,n}/T_{dt}$. Here, N refers to the number of switching events per period T for one side of the AC voltage. Since the steady-state behavior of the DAB affects the resonant commutation, and the resonant commutation impacts the steady-state behavior of the converter, an iterative solver is required to accurately capture these interdependencies and to determine the non-ideal behavior of the DAB.

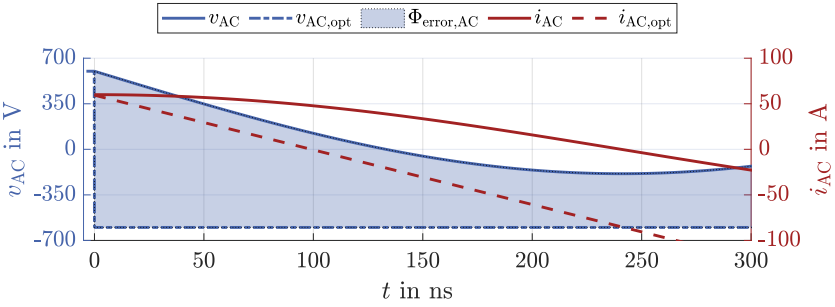


Figure 4.23: Voltage Time Area Error (VTAE) and resulting AC current i_{AC} due to the voltage error

$$\Phi_{error,AC} = \int_0^{T_{dt}} v_{AC,opt}(t) - v_{AC}(t)\mathrm{d}t \tag{4.39}$$

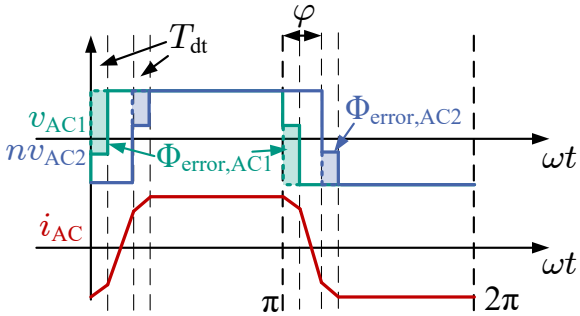


Figure 4.24: Waveform for SPS with consideration of the VTAE as a rectangular error

$$\underline{V}_{AC,VTAE,k} = \underline{V}_{AC,k} + \sum_{n=1}^{N} \frac{2\sqrt{2}\Phi_{error,AC,n}}{k\pi T_{dt}} \sin\left(k\pi \frac{T_{dt}}{T}\right) e^{-jk\frac{2\pi t_{sw,n}}{T}} \tag{4.40}$$

4.3.6 Including the commutation process in the DAB model

The calculation of the VTAE requires the exact switching current i_{sw} for each switching event. However, incorporating the VTAE in the commutation process leads to a change in the switching current i_{sw} at each switching instance. Therefore, deriving a closed-form analytical expression becomes infeasible when considering the VTAE in the operation of the DAB. The most common solution to this problem is an iterative approach, as illustrated in Fig. 4.25. The iterative process starts with the ideal DAB model, as presented in chapter 2.1. Using this ideal model as the baseline, the VTAE is computed for each switching event and incorporated into the Fourier series representation of the frequency domain model, as shown in (4.40). The resulting AC current i_{AC} is then compared to the AC current obtained from the previous step, before the inclusion of the VTAE. If the relative error, defined by (4.41), is below 1%, the calculated waveforms are considered sufficiently accurate, and the iteration process is terminated. Oth-

erwise, a new iteration step is initiated using the updated waveforms from the previous iteration. To further evaluate the accuracy of the iterative approach, alternative error metrics can be applied. However, using the switching currents i_{sw} as the error criterion provides the advantage of enabling fast error computation, thereby reducing the overall computational time required for the model convergence.

$$\varepsilon_{\mathrm{FDM}} = \frac{\sum_{n=1}^{4} i_{\mathrm{sw,new}}(n)^2}{\sum_{n=1}^{4} i_{\mathrm{sw,old}}(n)^2} \tag{4.41}$$

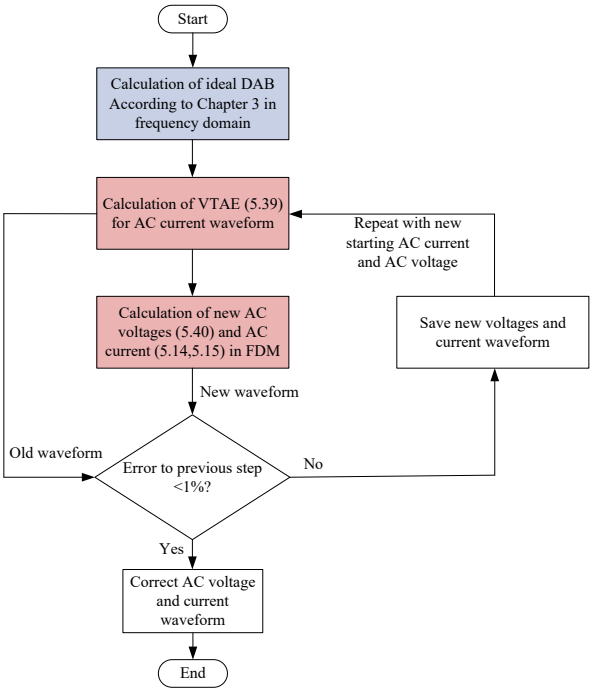


Figure 4.25: Flow chart of the modeling approach considering the VTAE of a DAB

4.3.7 Implications for the Operation of the Dual Active Bridge

In the previous sections, the impact of the deadtime, parasitic components, and the VTAE on a single switching event was thoroughly analyzed. These phenomena significantly influence the operational behavior and efficiency characteristics of the DAB when using the modulation schemes introduced earlier. The extent of this impact varies greatly, which is discussed in [E5, E6] and shown for SPS modulation in [60, 61, E7, E8] and for TCM in [62].

Single Phase Shift

For SPS operation of the DAB, the VTAE results in a varying error between the DC1 and DC2 sides, leading to a deviation in the applied phase shift φ. This error φ_{error} can be calculated using (4.42) and results in an actual active phase shift φ_{actual} as expressed in (4.43). Due to this deviation, the transferred power P of the DAB no longer aligns with the ideal model, leading to a power transfer characteristic that deviates from the expected behavior. The resulting error is dependent on the transfer ratio M_{DAB} of the DAB and can be categorized into two distinct cases:

For $M_{\text{DAB}} \approx 1$**:** The power transfer characteristic resembles a small S-shaped curve, which has point symmetrical behavior to the coordinate origin.

For $M_{\text{DAB}} \neq 1$**:** The power transfer characteristic forms a larger S-shaped curve, which does not have a symmetry.
The waveforms for both cases are shown in Fig. 4.26. The main difference of both cases are the switching currents $i_{\text{sw,DC1/DC2}}$ on both sides of the DAB. For unity operation both currents are similar whereas for buck and boost operation they are different which will lead to differing commutation speeds.

$$\varphi_{\text{error}} = \frac{\Phi_{\text{error,AC2}} - \Phi_{\text{error,AC1}}}{(V_{\text{DC1}} + V_{\text{DC2}})} \cdot (2\pi \cdot f_{\text{sw}}) \tag{4.42}$$

$$\varphi_{\text{actual}} = \varphi + \varphi_{\text{error}} \tag{4.43}$$

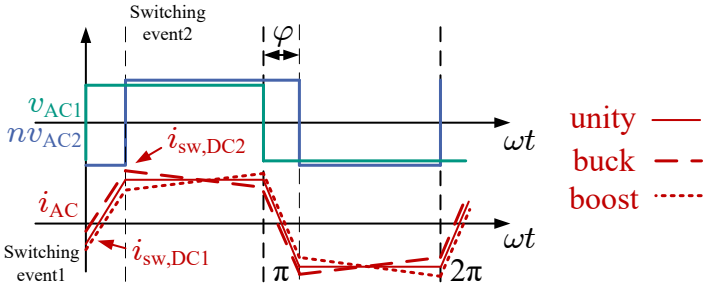


Figure 4.26: Waveforms for SPS in unity, boost and buck operation for positive power transfer

Figure 4.27 (a) illustrates the impact of the VTAE shown in Fig. 4.27 (b) on the transfer characteristic of the DAB under unity operation conditions. For low power P, the deviation between the VTAE model and the ideal model becomes significant, resulting in a highly nonlinear transfer characteristic. As the ZVS border for the DC1 side is approached (cf. Fig. 4.27), the VTAE remains nearly constant, whereas the VTAE for the DC2 side exhibits a steep curvature. This difference arises because no distinct ZVS border can be defined for the lagging switching event at the DC2 side full-bridge (FB) commutation, which is characterized by a negative counter-voltage (cf. Fig. 4.21 and 4.26). Consequently, near these operating points, the transfer characteristic of the DAB remains nearly constant, meaning that a change in the setpoint power P_{set} will result in no observable change in the output power. For negative power flow, the DAB exhibits a symmetric behavior, with DC1 and DC2 sides effectively swapping roles. At the ZVS border for the DC2 side, the resulting transfer characteristic is similarly constant, leading to a small "S"-shaped power transfer curve. This characteristic behavior reduces the stability of the control loop and impacts the dynamic response of the controller, as discussed in Chapter 3, for operating points near the ZVS border. In these regions, the controller may struggle to adjust the power transfer effectively, which could lead to oscillations or slow response times in the power regulation.
The behavior of the VTAE on the AC1 and AC2 sides differs significantly for buck and boost operation compared to unity operation. During boost operation (cf. Fig. 4.28), the current at switching event 1, $i_{\text{sw,DC1}}$, is reduced relative to

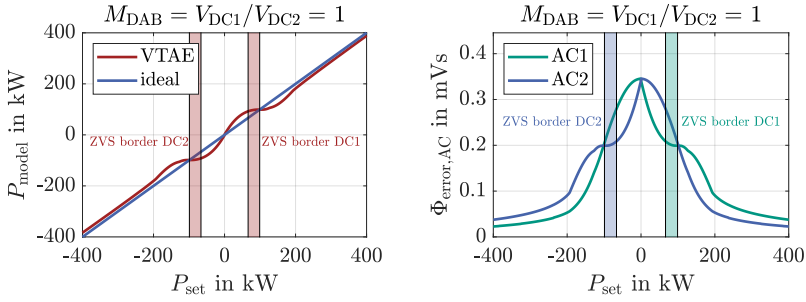


Figure 4.27: SPS modulation (a) transfer characteristic (b) VTAE for AC1 and AC2 side for unity operation $M_{DAB} = V_{DC1}/V_{DC2} = 1$

$i_{sw,DC2}$ due to the voltage difference (cf. Fig. 4.26). This results in a maximum VTAE on the AC1 side across a wide operating range where ZVS is not achieved at all. In contrast, the AC2 side achieves ZVS almost throughout the entire operating range, leading to a comparatively small VTAE. The resulting transfer characteristic, shown in Fig. 4.28 (a), forms a ”big S” shape, with a maximum deviation much larger than that observed in unity operation. For buck operation, a similar behavior can be observed, with the main difference being that the switching current $i_{sw,DC1}$ on the DC1 side increases due to the voltage difference (cf. Fig. 4.26). Consequently, the corresponding VTAE on the AC1 and AC2 sides swaps positions (cf. Fig. 4.29 (b)). The resulting transfer characteristic is again ”big S” shaped, as depicted in Fig. 4.29 (a). The ”big S” shape of the transfer characteristic during both buck and boost operation indicates that the VTAE has a more significant impact under non-unity operating conditions. This nonlinearity can pose a challenge for controller design and stability, as the power transfer response may become highly sensitive to even small changes in operating points, particularly in regions with large VTAE deviations. It is crucial to account for this behavior in both steady-state modeling and dynamic control strategies to ensure optimal DAB performance and avoid potential instabilities near the ZVS borders.
Additionally to the transfer characteristic which is highly influenced by the resonant commutation process, considering the resonant circuit will result in a deviation of the ZVS border of the DAB and therefore the efficiency charac-

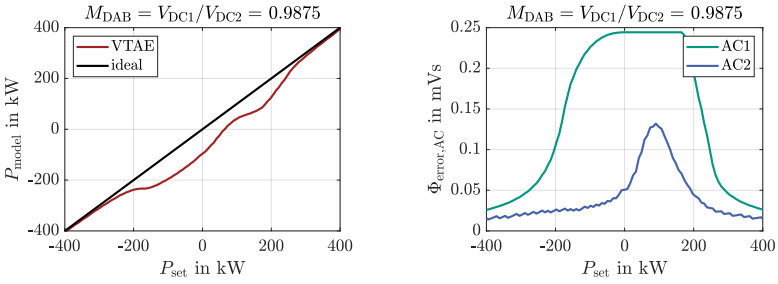


Figure 4.28: SPS modulation (a) transfer characteristic (b) VTAE for AC1 and AC2 side for boost operation $M_{DAB} = V_{DC1}/V_{DC2} < 1$

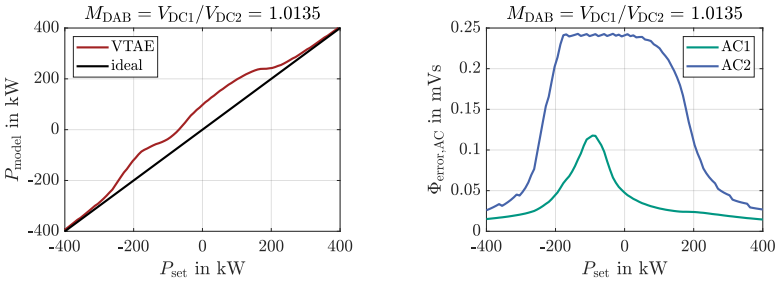


Figure 4.29: SPS modulation (a) transfer characteristic (b) VTAE for AC1 and AC2 side for buck operation $M_{DAB} = V_{DC1}/V_{DC2} > 1$

teristics compared to the previously presented models. According to (4.34), the assumption that the current through the turned on transistor has to be smaller then 0 does not hold for real life applications since a minimum amount of energy in the inductor is necessary to fully charge/discharge the MOSFET output capacitances. Additionally, the waveform is slightly changed due to the VTAE, both effects will result in a reduced ZVS region for SPS operation as shown in Fig. 4.30. However, it is noted that violating the ZVS region does not necessary results in massively increased switching losses since a gradually increase in turn

on losses occur until full turn on losses are reached and hence the FB operates under full hard switching conditions (cf. section 4.3.4).

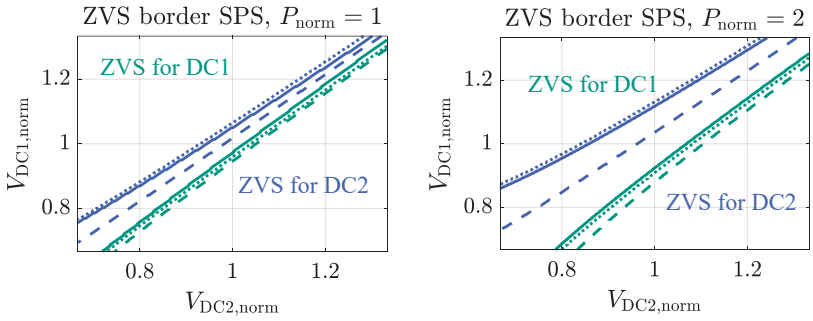


Figure 4.30: ZVS border for SPS with different normalized power P_{norm} and a small magnitizing inductance ($m = {}^{L_{\text{m}}}/_{L_\sigma} = 10$): (——)lossy model with magnetizing inductance and considering the resonant commutation process (– –)ideal model (·····)lossy model

Triangular Current Modulation

Comparable to the operation with SPS modulation, the VTAE significantly influences the operation in TCM. Figure 4.31 illustrates the waveforms using both the ideal model and the VTAE model. While the influence varies between boost and buck operation, it is important to note that for negative power transfer, the waveforms for boost and buck operation are swapped compared to those shown in Fig. 4.31. In both cases, the currents in the freewheeling state are not zero as typically assumed under ideal conditions. This is due to the fact that in TCM, there is always a switching event where it is assumed that both the DC1 and DC2 sides switch simultaneously. However, this assumption is invalidated by the resonant commutation process, which only allows the transition of one of the AC voltages, either v_{AC1} or v_{AC2}, during the deadtime, depending on the sign of the AC current i_{AC}. The other AC voltage will remain at the initial value and will have a commutation at the turn-on instant which will lead to full turn-on and turn-off losses of the switches. In addition to the increased circulating currents

within the freewheeling states, this behavior results in hard switching events with full switching losses, as depicted in Fig. 4.31. These findings highlight the need to consider the VTAE in both design and operational analysis of DAB systems, as the non-idealities investigated can lead to increased losses and reduced efficiency.

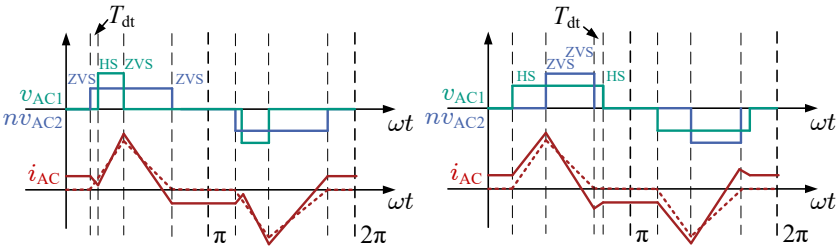


Figure 4.31: Waveform for TCM with consideration of the VTAE compared to the lossless model (a) buck operation (b) boost operation (——) VTAE model (·····) lossless model

Due to the asymmetrical behavior of the DAB under TCM operation, the transfer characteristic also exhibits asymmetry relative to the origin. In the case of buck operation with positive power P, illustrated in Fig. 4.31 (a), the transferred power remains relatively stable, with the efficiency being the primary parameter influenced by the resonant commutation process. Conversely, in boost operation, as depicted in Fig. 4.31 (b), there is a notable reduction in the transferred power compared to the ideal model due to the reduced voltage time area for nv_{AC2}. This decrease results in a lower steepness of the transfer characteristic during boost operation with positive power and during buck operation with negative power. The resulting transfer characteristic is presented in Fig. 4.32. This deviation of the transfer characteristic does not influence the stability of the controller, but will result in reduced dynamic of the system depending on the direction of the power flow and the operation mode (boost or buck). However, switching between SPS and TCM can result in unstable operation since the controller has to adjust to different controlled systems due to the vastly different transfer characteristics.

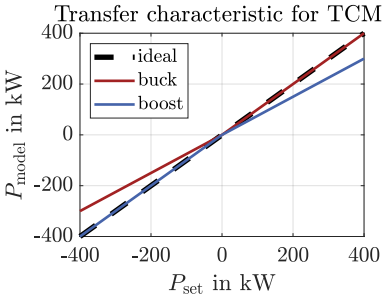


Figure 4.32: Transfer characteristic for TCM in boost and buck operation

4.4 Linearization of the Transfer Characteristic

To compensate for the non-linear Transfer Characteristic (TC) of SPS discussed in Section 4.3.7, a Function-Based Linearization (FBL) approach is employed, as first introduced in [E8]. For TCM, no compensation is necessary since the TC remains linear, and the deviations do not have a negative impact in cases of highly dynamic operation. However, as discussed in the previous section, a linearization of TCM might be beneficial in case of a operation point change between SPS and TCM. This can be done by using the same methods as for SPS but with a different function. A different compensation method is presented in [E7], where each individual operating point is compensated separately and stored in an error storage Look-up Table (LuT). In contrast, the FBL approach requires only fitted functions for each voltage set, resulting in significantly lower control effort and a reduced LuT size compared to compensating each operating point individually. This advantage is achieved by using measurement or model data to obtain an invertible function $F_{\text{fit}}(I_{\text{set}})$ that reflects the original non-linear TC as accurately as possible. The inverted function $F_{\text{fit}}^{-1}(I_{\text{set}})$ is then used in a feedforward compensation scheme to achieve a linear TC, as expressed in (4.44), where G_{DAB} is the DAB transfer function and I_{act} represents the resulting DC current. The block diagram of the DAB control system utilizing the FBL method is shown in Fig. 4.33, with the additional feedforward path highlighted in red. It is evident that the feedforward structure can be easily retrofitted into existing control schemes without adversely affecting the control behavior, as only the setpoint current is modified. To derive the invertible fitted function F_{fit}, there are three steps necessary:

1. Data acquisition
2. Curve fitting
3. Evaluation and selection of the best fitted function F_{fit}

The resulting flow chart to determine the required function and the corresponding parameters is shown in Fig. 4.34 and is further described in the following section. Each step of this method has a modular structure and can be replaced by a more suitable method for the current case, depending on the transfer function and available data.

$$I_{\text{act}} = G_{\text{DAB}}(F_{\text{fit}}^{-1}(I_{\text{set}})) \approx I_{\text{set}} \tag{4.44}$$

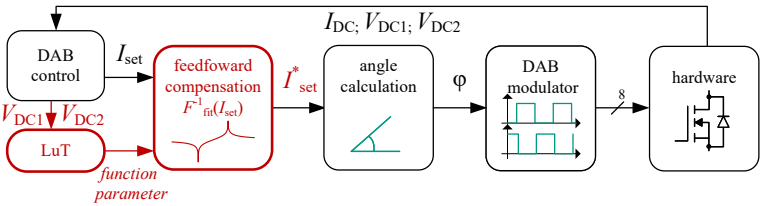


Figure 4.33: Block diagram of the DAB control system with feedforward linearization using FBL in red

Data acquisition

At the start of the data acquisition step, the voltage sets $S_{\text{VDC}} = [V_{\text{DC1}}\ V_{\text{DC2}}]$ are defined. These voltage sets must cover the entire desired operating range for SPS operation of the DAB. However, interpolation between voltage sets may be necessary to reduce the storage space required for the LuT. The distribution of the voltage sets can be uniform or clustered at specific points. In the transition from small S to large S functions, a high density of voltage sets may be required to accurately model the non linear behavior (cf. Section 4.3.7). For each voltage set, the corresponding transfer characteristic is needed. This can be obtained either

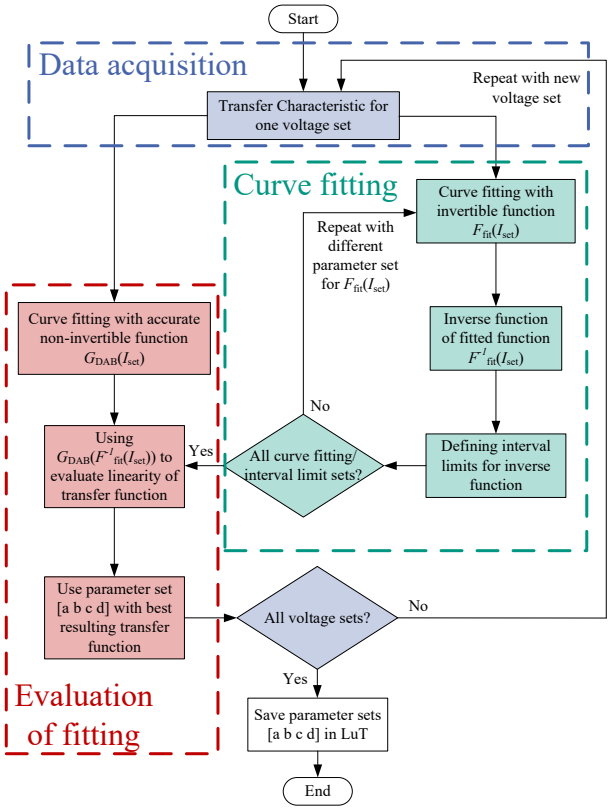


Figure 4.34: Flow chart of the fitting process for the FBL method

through the previously presented model or by using measurement data. Measurement data provides the most accurate fitted function F_{fit} without requiring extensive system knowledge or modeling effort. However, using the model-based approach reduces the initial effort, as no measurements are necessary.

Curve fitting

In the curve fitting stage, an invertible function is sought and parameterized to map the non-linear TC of the DAB as accurately as possible. This function must meet the following properties to be applicable in the FBL:

1. F_{fit} must be partially bijective to ensure invertibility
2. F_{fit} must be sufficiently accurate to handle both small and large S-shaped functions (using different functions for each shape is possible but increases the control effort)
3. F_{fit} should have as few parameters as possible to minimize the size of the LuT

One promising candidate for F_{fit} is the modified Sigmoid function in (4.45). This function has multiple advantages: it can be adjusted reasonably well to accurately represent both small and large S shapes, while requiring only four parameters $S_{\text{Sigmoid}} = [a,b,c,d]$. However, the Sigmoid function is only partially invertible, which necessitates a limitation of the fitting interval. The inverse function F_{fit}^{-1} and the corresponding fitting interval are shown in (4.46). In Fig. 4.35, the resulting functions F_{fit} and F_{fit}^{-1} as well as the fitting interval are depicted. It is not necessary to compensate the TC over the entire fitting interval; hence, a second interval is introduced, called the compensation interval, which denotes the range in which the TC is compensated. The only restriction for the compensation interval is that it must be smaller than or equal to the fitting interval. The compensation interval can also be asymmetrical which is especially beneficial for the compensation in case of buck and boost operation with SPS. Consequently, five parameters are varied in the curve fitting stage: the four Sigmoid parameters $S_{\text{Sigmoid}} = [a,b,c,d]$ and the compensation interval. Since this fitting process is conducted offline, a brute-force approach is used, where all possible combinations are calculated and evaluated in the next stage. However, a more sophisticated approach using optimization methods can be employed to reduce computational effort.

$$F_{\text{fit}}(I_{\text{set}}) = \frac{1}{a + e^{-bI_{\text{set}}+c}} + d \approx I_{\text{act}} \tag{4.45}$$

$$F_{\text{fit}}^{-1}(I_{\text{set}}) = \frac{c - \ln\left(\frac{1}{I_{\text{set}} - d} - a\right)}{b} = I_{\text{set}}^{*} \text{ with } d < I_{\text{set}} < d + \frac{1}{a} \tag{4.46}$$

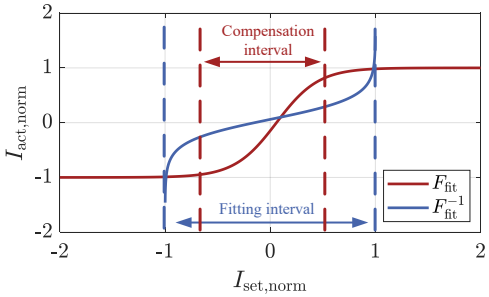


Figure 4.35: Fitting and arbitrary compensation interval using the Sigmoid function

Evaluation and selection of the best fitted function

In the curve fitting stage, all possible combinations of compensation intervals and parameters are calculated, and the best combination must be determined. To achieve this, a non-invertible function G_{DAB}^{*} is designed, which accurately fits the DAB TC for each voltage set S_{VDC}. In this case, a superposition of six to eight sinusoidal terms is used, as shown in (4.47), with the parameters $p(i)$, $k(i)$, and $l(i)$. This will result in a accurate representation of the actual transfer characteristic for small and big S shape. The parameter set that best satisfies the condition in (4.48) and resulting in a linear TC will be chosen for each voltage set S_{VDC}. The optimization criterion is shown in (4.49), where n is the the number of support points. Additionally, a secondary condition is defined as a performance metric: the gradient of the resulting transfer function $G_{\text{DAB}}(I_{\text{set}})$ must always be greater than zero to avoid controller instabilities which avoids plateaus as well as discontinuities of the resulting compensated transfer characteristic. The resulting set S_{Sigmoid} with the best properties, along with the respective compensation interval, will be stored in a LuT and used by the DAB controller.

$$G^*_{\mathrm{DAB}}(I_{\mathrm{set}}) = \sum_{i=1}^{N} p(i) \cdot \sin\left(k(i) \cdot I_{\mathrm{set}} + l(i)\right) = I_{\mathrm{act}} \text{ with } 6 \leq N \leq 8 \tag{4.47}$$

$$G^*_{\mathrm{DAB}}(F^{-1}_{\mathrm{fit}}(I_{\mathrm{set}})) = I_{\mathrm{act}} \approx I_{\mathrm{set}} \tag{4.48}$$

$$\min\ (\varepsilon_{\mathrm{FBL}}) = \min\left(\frac{\sum_{i=1}^{n} \left(I_{\mathrm{act}}(i) - I_{\mathrm{set}}(i)\right)^2}{n}\right) \tag{4.49}$$

4.5 Circular Current Injection

As discussed in the modeling section, considering the parasitic effects of the DAB during TCM operation, achieving ideal ZVS and ZCS switching is not straightforward due to the presence of the VTAE (cf. Fig. 4.31). Instead of zero current i_{AC} during the freewheeling states, the current i_{AC} is non-negligible, and switching events do not occur at ZVS or ZCS operation points. In particular, achieving ZCS operation with high-power DAB converters is challenging because the switching current changes significantly during the deadtime and switching transitions. This is mainly due to the low AC inductance L_σ and high output capacitances C_{OSS} of the switches. Consequently, switching losses increase substantially compared to ideal ZCS and ideal ZVS operation. This results in significantly higher losses than the ideal TCM considerations. To address this issue, adjustments are necessary during buck and boost operation with TCM to ensure soft switching and improve the system's efficiency. These adjustments involve modifying the circulating current in the AC circuit by adjusting the control angles φ, δ_1, and δ_2 such that each switching event of the DAB under TCM achieves full ZVS operation. This strategy is presented in [E9], [63] (considering the non-linear output capacitance), and [64] (considering a simplified model of the commutation process within the deadtime) for various applications and implementation methods. For this work, the Circular Current Injection (CCI) (Circular Current Injection) method from [E9] is analyzed. In contrast to previously presented optimizations, this method does include the non linear capacitance to calculate the minimal necessary current for ZVS as well as the time course of the commutation process and it's influence on the AC current and

ZVS behavior using the previously established modeling approach. The desired waveforms for buck and boost operation are depicted in Fig. 4.36, with subfigure (a) showing buck and (b) showing boost operation. Here, the switching currents i_{SW1}, i_{SW2}, and i_{SW3} can be independently controlled to achieve complete ZVS while maintaining a low RMS current. However, it is noted that the circulating current will slightly increase the RMS current compared to the ideal TCM current waveform. Nevertheless, for most DAB setups, the reduction of switching losses are much higher than the increased conduction losses (for a detailed analysis the ZVS behavior and conduction characteristic of the DAB is necessary). Assuming $i_{SW2} = i_{SW3}$ for a lossless DAB, only two switching currents need to be adjusted. To achieve ZVS for all switching events, the minimum required currents for i_{SW1} and $i_{SW2} = i_{SW3}$ must be determined. The modulation angles φ, δ_1, and δ_2 then need to be adapted accordingly. These adjustments must account for the actual non-ideal ZVS transition and cannot neglect the deadtime effects of the DAB. Therefore, the previously presented ZVS model (cf. section 4.3) is essential to ensure the optimal efficiency of this modulation scheme. In the following, the critical steps for this process are outlined, along with the impact of CCI on the operation of the DAB.

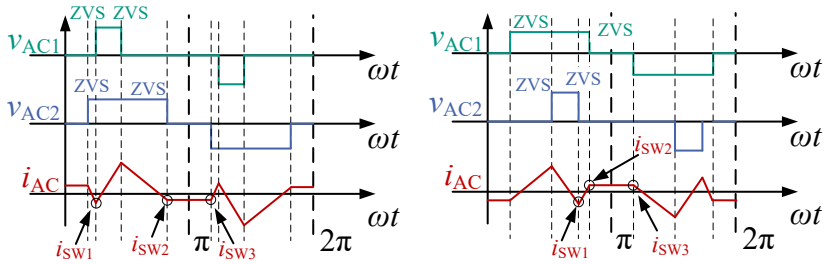


Figure 4.36: Waveform for CCI for (a) buck operation $V_{DC1} > V_{DC2}$ (b) boost operation $V_{DC1} < V_{DC2}$

Optimal Switching Current

There are two main criteria for determining the optimal switching current i_{SW} to achieve maximum efficiency. First, the current must be large enough to ensure ZVS for all switching events within the defined deadtime T_{dt}. Secondly, since the switching current is proportional to the additional circulating current, it directly impacts the overall RMS current in the AC circuit, leading only to small increased conduction losses. Theoretically, a complex optimization process would be necessary to balance these two factors. In practice, however, the reduction in switching losses due to ZVS is generally much greater than the increase in RMS losses, especially in high-power DAB systems. Therefore, only the exact ZVS boundary must be determined for all switching events. This is achieved by using the CTD model described in Section 4.3. The cZVS condition defined in (4.32) needs to be adapted to the respective switching events under CCI. The resulting minimum currents $i_{SW,min}$ for buck and boost operation are summarized in Table 4.2. Depending on the deadtime T_{dt}, the transfer ratio of the DAB, and the specific switching event (primarily influenced by the opposing voltage), the minimal switching current may be constrained either by the deadtime or by the current itself (cf. Section 4.3.3). If the minimum current is determined by the deadtime T_{dt}, it means that the energy stored in the inductance is sufficient for cZVS operation, but a further reduction of the current would lead to a non-optimal deadtime (either too high or too low) and therefore no cZVS operation is possible anymore (cf. Section 4.3.3). Conversely, if the minimal current is constrained by the current itself, then the energy stored in the inductor would not be sufficient to fully charge or discharge the output capacitances if it is further reduced. Consequently, a higher switching current is required, if a deadtime limitation is present, for cZVS compared to the case with an optimal deadtime. For the currents i_{SW2} and i_{SW3}, the higher value between the two must be applied since both are equal for the operation of a lossless DAB. Even in the presence of losses, both currents can generally be assumed to be nearly equal. Furthermore, the current-limited (energy-based) constraints apply only when the deadtime is optimal (cf. Section 4.3.3). If the deadtime deviates significantly from its ideal value, then the deadtime-limited equations for the minimal currents, as presented in Table 4.2, should always be applied.

Modulation Angle Adaption

In order to achieve the current and voltage waveform depicted in Fig. 4.36, the control angles φ, δ_1 and δ_2 must be adjusted to inject the desired circulating

current. This is accomplished by starting with the conventional TCM control angles and subtracting a constant angle φ_{ad} and δ_{ad} as shown in (4.50) and (4.51), respectively. Depending on whether the operation mode is buck or boost, only δ_2 (buck) or δ_1 (boost) is adjusted.

$$\varphi_{\mathrm{CCI}} = \varphi_{\mathrm{TCM}} - \varphi_{\mathrm{ad}} \tag{4.50}$$

$$\delta_{\mathrm{CCI}} = \delta_{\mathrm{TCM}} - \delta_{\mathrm{ad}} \tag{4.51}$$

The adjusting angle can be calculated according to (4.52)-(4.55) for buck and boost operation. It is noted that the VTAE Φ_{sw} does have a significant impact on the angles and cannot be neglected. It can be observed that the adjusted angle solely depends on the voltage transfer ratio as a operation point dependent parameter. Therefore, no power dependency is present and for a fixed voltage transfer ratio a constant φ_{ad} and δ_{ad} can be utilized. This enables an easy to implement offline optimization of the angles for each voltage transfer ratio with a interpolation between each supporting point. Additionally, these adjustments can simply be implemented in an existing TCM modulation scheme.

$$\varphi_{\mathrm{ad,buck}} = \left(i_{\mathrm{sw1}} L_{\sigma} + \frac{\Phi_{\mathrm{sw1}} + \Phi_{\mathrm{sw2}} + \Phi_{\mathrm{sw3}}}{2} \right) \frac{2\pi f_{\mathrm{sw}}}{V_{\mathrm{DC2}}} \tag{4.52}$$

$$\delta_{\mathrm{ad,buck}} = \left(2 \cdot i_{\mathrm{sw2}} L_{\sigma} - \Phi_{\mathrm{sw1}} - \Phi_{\mathrm{sw2}} + \Phi_{\mathrm{sw3}}\right) \frac{2\pi f_{\mathrm{sw}}}{V_{\mathrm{DC2}}} \tag{4.53}$$

$$\varphi_{\mathrm{ad,boost}} = \left(i_{\mathrm{sw1}} L_{\sigma} + \frac{\Phi_{\mathrm{sw1}} - \Phi_{\mathrm{sw2}} - \Phi_{\mathrm{sw3}}}{2} \right) \frac{2\pi f_{\mathrm{sw}}}{V_{\mathrm{DC1}}} \tag{4.54}$$

$$\delta_{\mathrm{ad,boost}} = \left(2 \cdot i_{\mathrm{sw2}} L_{\sigma} + \Phi_{\mathrm{sw1}} - \Phi_{\mathrm{sw2}} + \Phi_{\mathrm{sw3}}\right) \frac{2\pi f_{\mathrm{sw}}}{V_{\mathrm{DC1}}} \tag{4.55}$$

Adjusted Operation Point

Using CCI will result in a different power transfer characteristic compared to TCM due to the additional circular current. However, only a change in i_{sw1} does change the transferred power. For i_{sw2} and i_{sw3} the transferred power P does not change. The resulting power using CCI is given in (4.56) and (4.57) for boost and buck operation. The comparison of both transferred power for TCM and CCI is shown in Fig. 4.37 (a). It is evident, that for CCI the power for the same control angle φ is always reduced compared to ideal TCM. This is expected since more circular current is injected which does require a part of the voltage time area of v_{AC1} and v_{AC2} at which no power is transferred.

$$P_{CCI,boost} = P_{TCM}(\varphi) - \frac{\pi - \delta_2(\varphi)}{\pi} V_{DC2} \cdot i_{sw1} \tag{4.56}$$

$$P_{CCI,buck} = P_{TCM}(\varphi) - \frac{\pi - \delta_1(\varphi)}{\pi} V_{DC1} \cdot i_{sw1} \tag{4.57}$$

The maximum transferable power using TCM and CCI is limited by the maximum outer phase shift angle φ. For TCM this limit is given in chapter 2. However, for CCI this upper limit is lower and can be calculated according to (4.58). Since the maximum power P_{max} only directly depends on φ the maximum power can be calculated with (4.56) and (4.57) as well as the standard TCM equations. The resulting comparison of the maximum power P_{max} for different voltage transfer ratios is shown in Fig. 4.37 (b). As expected the maximum power for CCI is always slightly decreased compared to TCM.

$$\varphi_{max,CCI,boost/buck} = \frac{\pi - \delta_{add}}{2} \left(1 - \frac{V_{DC1/2}}{V_{DC2/1}}\right) \tag{4.58}$$

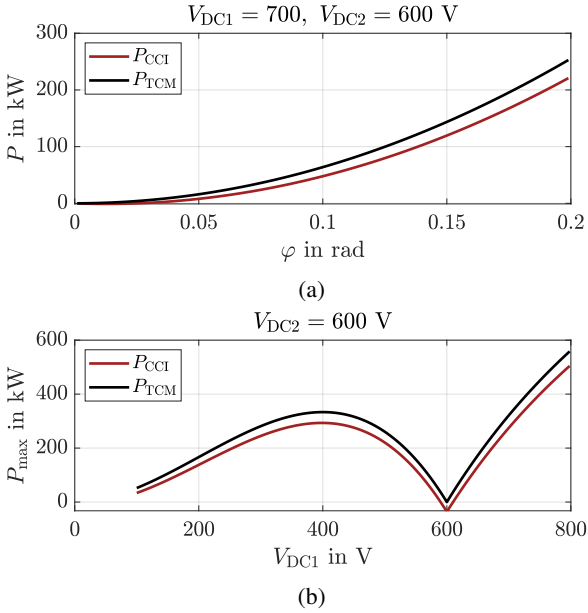


Figure 4.37: Comparison of transferred power for TCM and CCI (a) transferred power P for different φ for buck operation (b) maximum transferable power P_{max} for different voltage transfer ratio

Table 4.2: Minimal Current for each switching event for CCI to achieve ZVS operation

Switching Event	Boost	Buck
i_{sw1}	for $V_{\mathrm{DC2}} \leq 2 \cdot V_{\mathrm{DC1}}$	for $V_{\mathrm{DC1}} \geq 2 \cdot V_{\mathrm{DC2}}$
limited by current	$\sqrt{\frac{C_{\mathrm{eq}}}{L_\sigma}} \cdot (2 \cdot V_{\mathrm{DC1}} V_{\mathrm{DC2}} - V_{\mathrm{DC2}}^2)$	$\sqrt{\frac{C_{\mathrm{eq}}}{L_\sigma}} \cdot (-2 \cdot V_{\mathrm{DC2}} V_{\mathrm{DC1}} + V_{\mathrm{DC1}}^2)$
	for $V_{\mathrm{DC2}} > 2 \cdot V_{\mathrm{DC1}}$	for $V_{\mathrm{DC1}} < 2 \cdot V_{\mathrm{DC2}}$
limited by deadtime	$\frac{(V_{\mathrm{DC2}} - V_{\mathrm{DC1}}) \left(\cos\left(\frac{T_{\mathrm{dt}}}{\sqrt{L_\sigma C_{\mathrm{eq}}}} \right) - 1 \right)}{\sqrt{\frac{L_\sigma}{C_{\mathrm{eq}}}} \sin\left(\frac{T_{\mathrm{dt}}}{\sqrt{L_\sigma C_{\mathrm{eq}}}} \right)} + V_{\mathrm{DC2}}$	$\frac{(V_{\mathrm{DC2}}) \left(\cos\left(\frac{T_{\mathrm{dt}}}{\sqrt{L_\sigma C_{\mathrm{eq}}}} \right) - 1 \right)}{\sqrt{\frac{L_\sigma}{C_{\mathrm{eq}}}} \sin\left(\frac{T_{\mathrm{dt}}}{\sqrt{L_\sigma C_{\mathrm{eq}}}} \right)} + V_{\mathrm{DC1}}$
i_{sw2}		
limited by deadtime	$\sqrt{\frac{C_{\mathrm{eq}}}{L_\sigma}} \cdot V_{\mathrm{DC1}} \cdot \cot\left(\frac{T_{\mathrm{dt}}}{\sqrt{L_\sigma C_{\mathrm{eq}}}} \right)$	$\sqrt{\frac{C_{\mathrm{eq}}}{L_\sigma}} \cdot V_{\mathrm{DC2}} \cdot \cot\left(\frac{T_{\mathrm{dt}}}{\sqrt{L_\sigma C_{\mathrm{eq}}}} \right)$
i_{sw3}		
limited by current	$\sqrt{\frac{C_{\mathrm{eq}}}{L_\sigma}} \cdot V_{\mathrm{DC1}}^2$	$\sqrt{\frac{C_{\mathrm{eq}}}{L_\sigma}} \cdot V_{\mathrm{DC2}}^2$
limited by deadtime	$\frac{V_{\mathrm{DC1}}}{\sqrt{\frac{L_\sigma}{C_{\mathrm{eq}}}} \sin\left(\frac{T_{\mathrm{dt}}}{\sqrt{L_\sigma C_{\mathrm{eq}}}} \right)}$	$\frac{V_{\mathrm{DC2}}}{\sqrt{\frac{L_\sigma}{C_{\mathrm{eq}}}} \sin\left(\frac{T_{\mathrm{dt}}}{\sqrt{L_\sigma C_{\mathrm{eq}}}} \right)}$

4.6 Non-Ideal Transformer Characteristics

One important component for the behavior of the DAB is the MFT. In the frequency range of the switching frequency and its relevant multiples, hereinafter referred to as Medium Frequency (MF), the transformer can be modeled as an ideal transformer with its stray inductances L_σ. However, due to the switching of the semiconductors and the associated high-frequency components, the High Frequency (HF) behavior of the AC circuit, and in particular the MFT, must be analyzed to avoid unfavorable operating conditions such as excessive core losses, increased electromagnetic interference (EMI), or thermal stress on the winding insulation. Additionally, undesired oscillations, such as resonances between the parasitic capacitances of the transformer and the stray inductances, could lead to voltage spikes or current overshoot, which may damage the components or degrade the system's performance.

High Frequency Modeling of the AC Circuit

In order to analyze the transformer in the HF domain, an equivalent circuit diagram, as shown in Fig. 4.38, is applied [65–67]. The AC inductances are separated depending on whether they are located inside the transformer (L_σ) or at the DC1 or DC2 side connections (L_{AC1} and L_{AC2}). Additionally, the transformer winding capacitances $C_{\mathrm{w1/2}}$, between the turns of a winding, and the coupling capacitance C_{c} are added to the previously established transformer model, as these capacitances can have a significant impact, especially for foil windings [48] used in this work. The winding configuration, along with a representation of the individual capacitances, is shown in Fig. 4.39 for the transformer utilized in this dissertation and the "layered foil winding" configuration. Analyzing this network, a frequency-dependent impedance Z_{AC} of the AC circuit, as seen from the DC1 and DC2 sides, can be defined in (4.59) and (4.60), respectively [68]. Depending on the symmetry of the transformer and its connections ($L_{\mathrm{AC1}} = L_{\mathrm{AC2}}$ and $C_{\mathrm{w1}} = C_{\mathrm{w2}}$), the impedance can vary depending on the side of the AC circuit. However, the series resonance points always occur at the same resonance frequencies. The resulting impedances are shown in Fig. 4.40. Two main resonances are observed at the lowest magnitude of the impedance. The first resonance is usually more pronounced since the damping caused by the AC resistances $R_{\mathrm{AC1}}(f)$ and $R_{\mathrm{AC2}}(f)$ is frequency-dependent, and both increase with frequency due to the skin and proximity effects in litz wires [69, 70].

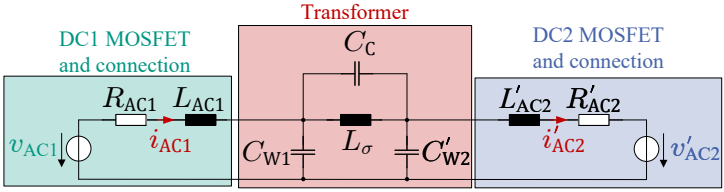


Figure 4.38: HF equivalent circuit diagram of the AC circuit of a DAB with MFT

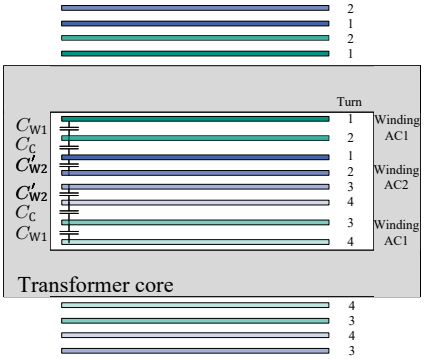


Figure 4.39: Winding configuration "layered foil winding" of the MFT with parasitic capacitances

$$Z_{AC1}(\omega) = \frac{V_{AC1}(\omega)}{i_{AC1,HF}(\omega)} = \frac{(y_{AC2} + y_T + y_{w2})}{(-y_T^2 + (y_T + y_{w1})y_{AC2} + (y_T + y_{w1})(y_T + y_{w2}))} + \frac{1}{y_{AC1}} \tag{4.59}$$

$$Z'_{AC2}(\omega) = \frac{V'_{AC2}(\omega)}{i'_{AC2,HF}(\omega)} = \frac{(y_{AC1} + y_T + y_{w1})}{(-y_T^2 + (y_T + y_{w2})y_{AC1} + (y_T + y_{w2})(y_T + y_{w1}))} + \frac{1}{y_{AC2}} \tag{4.60}$$

with

$$
\begin{aligned}
y_{\mathrm{AC1}} &= \frac{1}{R_{\mathrm{AC1}} + j\omega L_{\mathrm{AC1}}} & y_{\mathrm{AC2}} &= \frac{1}{R'_{\mathrm{AC2}} + j\omega L'_{\mathrm{AC2}}} \\
y_{\mathrm{w1}} &= j\omega C_{\mathrm{w1}} & y_{\mathrm{w2}} &= j\omega C'_{\mathrm{w2}} \\
y_{\mathrm{T}} &= \frac{1}{j\omega L_{\sigma}} + j\omega C_{\mathrm{C}}
\end{aligned}
\tag{4.61}
$$

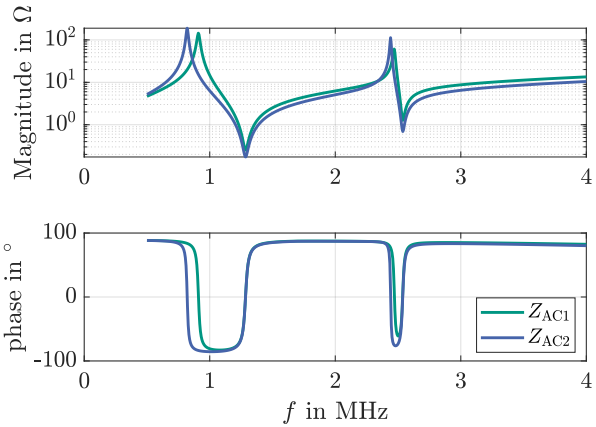


Figure 4.40: Impedance Z_{AC} of the HF equivalent circuit seen from DC1 and DC2 side

Using the impedance Z_{AC} of the AC circuit, the resonance frequencies can be calculated by finding the local minima of the impedance. To reduce the complexity of the resulting term, it is assumed that both winding capacitances are equal ($C_{\mathrm{w1}} = C_{\mathrm{w2}} = C_{\mathrm{w}}$), which holds true for symmetrical transformer configurations as used in this DAB. However, the same procedure can also be applied to asymmetric transformer configurations with increased complexity of the equations.

$$
f_{\mathrm{res1}} \approx \sqrt{\frac{L_{\sigma}\left(C_{\mathrm{c}}\left(L_{\mathrm{AC1}} + L_{\mathrm{AC2}}\right) + C_{\mathrm{w}} L_{\mathrm{AC2}}\right) + C_{\mathrm{w}} L_{\mathrm{AC1}}\left(2L_{\mathrm{AC2}} + L_{\sigma}\right) - \sqrt{\mathscr{R}}}{4\pi^2\left[2C_{\mathrm{w}}(2C_{\mathrm{c}} + C_{\mathrm{w}}) L_{\mathrm{AC1}} L_{\mathrm{AC2}} L_{\sigma}\right]}}
\tag{4.62}
$$

with

$$\begin{aligned}\mathscr{R} = C_{\mathrm{c}}^2(L_{\mathrm{AC1}}+L_{\mathrm{AC2}})^2L_{\sigma}^2 + 2C_{\mathrm{c}}C_{\mathrm{w}}L_{\sigma}(L_{\mathrm{AC2}}^2L_{\sigma} \\ +L_{\mathrm{AC1}}^2(-2L_{\mathrm{AC2}}+L_{\sigma}) - 2L_{\mathrm{AC1}}L_{\mathrm{AC2}}(L_{\mathrm{AC2}}+L_{\sigma})) \\ +C_{\mathrm{w1}}^2(-2L_{\mathrm{AC1}}L_{\mathrm{AC2}}L_{\sigma}^2 + L_{\mathrm{AC2}}^2L_{\sigma}^2 + L_{\mathrm{AC1}}^2(4L_{\mathrm{AC2}}^2+L_{\sigma}^2))\end{aligned} \tag{4.63}$$

for

$$C_{\mathrm{w1}} = C_{\mathrm{w2}} = C_{\mathrm{w}} \tag{4.64}$$

If the AC inductance is symmetrical on the DC1 and DC2 side $L_{\mathrm{AC1}} = L_{\mathrm{AC2}} = L_{\mathrm{AC}}/2$ the expression in (4.62) is reduced to (4.65). In this special case, the coupling capacitance C_{c} does not influence the current ringing at the first resonance frequency f_{res1} anymore.

$$f_{\mathrm{res1}} \approx \frac{1}{2\pi\sqrt{C_{\mathrm{w}}L_{\mathrm{AC1}}}} \tag{4.65}$$

Excitation

The excitation of the AC circuit and MFT can be calculated using the simplified AC voltage waveform shown in Fig. 4.41. To reduce complexity, it is assumed that the switching events have a constant $\mathrm{d}v_{\mathrm{AC}}/\mathrm{d}t$, and both the rise and fall times are equal ($t_{\mathrm{r}} = t_{\mathrm{f}}$). The resulting spectrum of this excitation can be calculated according to (4.66) [71]. The spectrum of v_{AC} depends on two main parameters: the pulse width t_{pulse} of each half cycle and the rise/fall time t_{r}. The pulse width t_{pulse} depends on the modulation scheme, for SPS, it is half the period of the switching frequency $T/2$, and for TCM, it varies between 0 and $T/2$ (assuming $T \gg t_{\mathrm{r}}$). Therefore, t_{pulse} is defining for the MF spectrum while t_{r} is defining for the HF part of the spectrum. Every peak of the MF and HF component of the excitation does have an envelope which can be deduced using (4.67). Two characteristic points are evident: at $\tau_1 = 1/\pi t_{\mathrm{pulse}}$, where the envelope of the spectrum starts to fall with a slope of 20dB/decade, and at $\tau_2 = 1/\pi t_{\mathrm{r}}$, where the upper spectral bound falls with 40dB/decade. Both the envelope of the spectrum and the spectrum itself are shown in Fig. 4.42 for two different values of $\mathrm{d}v_{\mathrm{AC}}/\mathrm{d}t$. It can be observed that changing the voltage steepness of the excitation results in a shifted spectrum because τ_2 changes, thereby shifting the second characteristic

point. However, for frequencies lower than τ_2, the spectrum is not influenced by the voltage steepness.

$$V_{\mathrm{AC,n}} = 2\hat{v}_{\mathrm{AC}} \frac{t_{\mathrm{pulse}}}{T} \mathrm{sinc}\left(n\omega_0 \frac{t_{\mathrm{pulse}}}{2}\right) \mathrm{sinc}\left(n\omega_0 \frac{t_{\mathrm{r}}}{2}\right) e^{-jn\omega_0 \frac{t_{\mathrm{pulse}}+t_{\mathrm{r}}}{2}} \tag{4.66}$$

$$20\log_{10}\left(V_{\mathrm{AC,envelope}}\right) = 20\log_{10}\left(2\hat{v}_{\mathrm{AC}} \frac{t_{\mathrm{pulse}}}{T}\right) + 20\log_{10}\left|\mathrm{sinc}(\pi t_{\mathrm{pulse}} f)\right| + 20\log_{10}\left|\mathrm{sinc}(\pi t_{\mathrm{r}} f)\right| \tag{4.67}$$

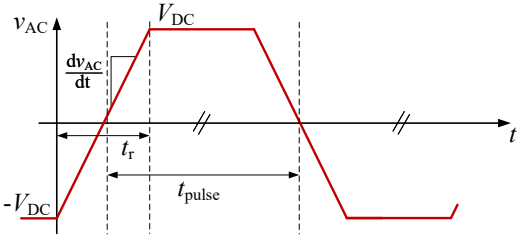


Figure 4.41: Simplified AC voltage for the DAB AC voltage v_{AC} which excites the HF circuit

Transformer Current Ringing

Using (4.68), the resulting AC current spectrum can be calculated. The resulting spectrum is shown in Fig. 4.43 for different values of $\mathrm{d}v_{\mathrm{AC}}/\mathrm{d}t$. There is a clear resonance point at the first root of the impedance Z_{AC} which is f_{res1}, and can result in noticeable current ringing depending on the voltage steepness and the AC circuit parameters. As expected from the excitation spectrum, a higher $\mathrm{d}v_{\mathrm{AC}}/\mathrm{d}t$ will result in increased current ringing. However, depending on the root of Z_{AC}, the value of $\mathrm{d}v_{\mathrm{AC}}/\mathrm{d}t$ must be set very low to reduce the spectrum at the resonance point, which may not be feasible for reasonable operation. Since this

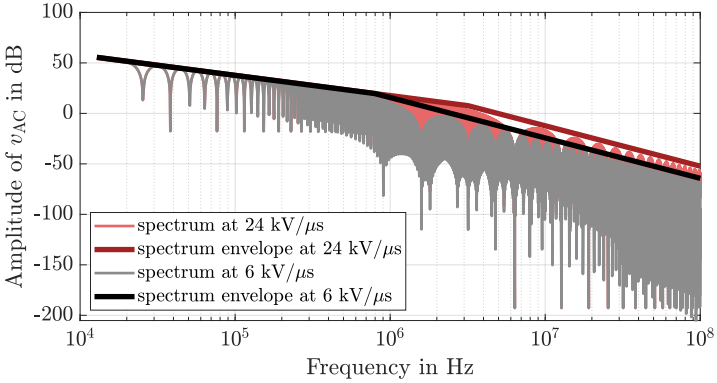


Figure 4.42: Spectrum of the AC voltage v_{AC} for different $\frac{dv_{AC}}{dt}$

current ringing occurs at high frequencies, the frequency-dependent AC resistance $R_{AC}(f)$ is significantly higher, leading to increased conduction losses in the connections and the transformer due to skin and proximity effect.

$$i_{AC,HF}(\omega) = \frac{|V_{AC}(\omega)|}{Z_{AC}(\omega)} \tag{4.68}$$

Superposition of Current Ringing

So far for all investigations on the current ringing of the DAB AC circuit, an excitation of only one AC side was considered. However, this assumption does not hold for DAB operation with SPS or TCM, since the phase shift can occur in the same range as the oscillation period length $T_{osci} = 1/f_{osci}$. This can lead to an overlap of both oscillations depending on the three phase shifts. To reduce complexity, only SPS operation is considered in this analysis since only one phase shift angle φ and two excitations have to be considered. Nevertheless, the presented methods can be easily applied to all modulation schemes if necessary. Using the HF equivalent circuit diagram in Fig. 4.38, it becomes evident that a superposition of both currents, $i_{AC1,QAC1}(f)$ and $i_{AC1,QAC2}(f)$, caused by their respective AC voltage sides, is necessary to obtain the resulting spectrum. Both

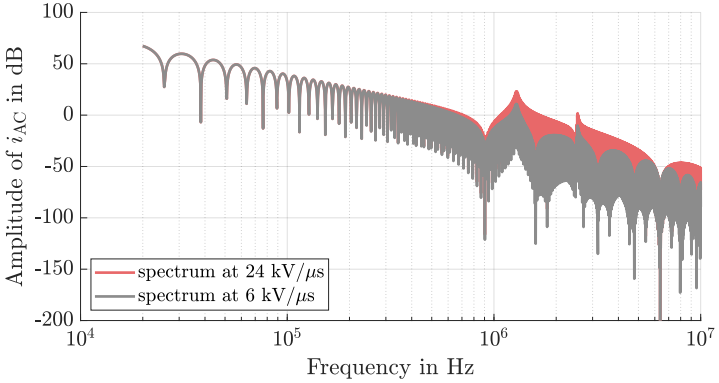


Figure 4.43: Spectrum of the AC current i_{AC} for different $\frac{dv_{AC}}{dt}$

currents can be calculated according to (4.69), (4.70), and (4.71). The resulting superposition of both currents depends on the phase shift φ of the DAB and is given in (4.72).

$$i_{AC1,QAC1,HF}(\omega) = \frac{|V_{AC1}(\omega)|}{Z_{AC1}(\omega)} \tag{4.69}$$

$$i'_{AC2,QAC2,HF}(\omega) = \frac{|V'_{AC2}(\omega)|}{Z'_{AC2}(\omega)} \tag{4.70}$$

$$i_{AC1,QAC2,HF}(\omega) = \frac{y_T \cdot y_{AC1}}{y_T \cdot (y_{AC1} + y_{w1}) + y_{w1}} i'_{AC2,QAC2,HF}(\omega) \tag{4.71}$$

$$i_{AC1,HF}(\omega) = i_{AC1,QAC1,HF}(\omega) + i_{AC1,QAC2,HF}(\omega) e^{-j\omega \frac{\varphi}{2\pi f_{sw}}} \tag{4.72}$$

Figure 4.44 shows the resulting amplitude $\hat{i}_{\mathrm{AC1}}(f = f_{\mathrm{osci}})$ for different phase shifts φ during SPS operation. The operating point can significantly influence the resulting current ringing depending on the inductance ratio $L_{\mathrm{AC1}}/L_{\mathrm{AC2}}$. In a symmetrical AC circuit, the amplitude of the oscillations is dependent on the phase shift. Since the impedances Z_{AC1} and Z_{AC2} are nearly equal, the resulting spectra of $i_{\mathrm{AC1,QAC1,HF}}(\omega)$ and $i_{\mathrm{AC1,QAC2,HF}}(\omega)$ are also almost identical. As a result, the phase shift leads to constructive or destructive superposition of both currents, depending on the ratio of the resonance frequency f_{res1} and the phase shift φ. If the inductance ratio is large, the impact of the phase shift becomes negligible. This is because one side of the DAB causes minimal oscillation, and the superposition of the current is dominated by the side with the higher inductance, which can exhibit significant oscillations.

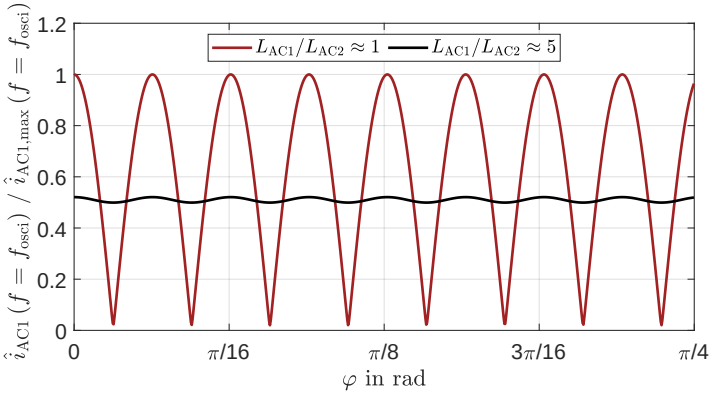


Figure 4.44: Amplitude of $i_{\mathrm{AC}}(f = f_{\mathrm{osci}})$ with superposition of switching events on both AC sides with an phase shift of φ between v_{AC1} and v_{AC2} and different ratio of $L_{\mathrm{AC1}}/L_{\mathrm{AC2}}$ normalized to the highest oscillation amplitude possible

Reducing the Current Ringing

In order to reduce current ringing, two main approaches are possible. First, the excitation can be reduced so that the spectrum at the resonance frequency of the AC circuit is significantly attenuated [68]. This can be achieved by lowering the $\mathrm{d}v_{\mathrm{AC}}/\mathrm{d}t$, which will also reduce the excitation amplitude in the HF range (cf. Fig. 4.42). However, the potential for reduction is limited since a significantly

lower $\mathrm{d}v_{\mathrm{AC}}/\mathrm{d}t$ is required to achieve substantial attenuation of the excitation. Additionally, $\mathrm{d}v_{\mathrm{AC}}/\mathrm{d}t$ is directly linked to the ZVS behavior of the DAB. A reduced steepness can only be achieved by adding or increasing a snubber capacitance in parallel to the switches, which in turn necessitates higher switching currents for ZVS and increases the non-linearity of the DAB. Especially at partial load operation, this will impair both dynamic performance and efficiency. The second method to avoid current ringing in the AC circuit is to modify the AC circuit impedance such that the resonance frequency is increased or the impedance at the resonance point remains high. This can be achieved in three different ways:

1. Reducing the inductances: By lowering the AC inductances L_σ and $L_{\mathrm{AC1/2}}$, the resonance frequency shifts to higher frequencies, resulting in lower excitation at those frequencies. However, this approach has significant drawbacks. First, the AC inductance directly affects the transferred power and the dynamic behavior of the DAB. Second, the soft-switching capability depends on the inductance, and higher inductances result in more efficient operation at reduced load.

2. Changing the distribution of the inductances: The inductances can be redistributed between the DC1 and DC2 sides of the DAB, thereby altering the resonance points of the impedance Z_{AC}. However, this approach is only feasible for lower transferred power levels and when using external additional inductances. For high-power DAB, the inductance is usually determined solely by the transformer's stray inductance and the connections to the transformer. Moreover, this method is most effective for asymmetrical DAB configurations, where the transformer turns ratio n is significantly different from one [67].

3. Optimizing the transformer: Current ringing can be mitigated by modifying the transformer's parasitic elements. Specifically, reducing the parasitic capacitances within and between the windings (intra, and inter winding capacitance) can increase the impedance at high frequencies and shift the resonance frequency to points with lower excitation.

For high-power DABs, improving the transformer stray parameters is the most promising approach, as it does not negatively affect MF operation. The analysis of the HF behavior revealed that the winding capacitances C_{w1} and C_{w2} are the primary contributors to current ringing. This is why an improved winding arrangement for the transformer, as shown in Fig. 4.45, was developed in collaboration with *Schmidbauer transformers and Equipment GmbH*. This winding

configuration, referred to as a "parallel foil winding" reduces the winding capacitance by a factor of approximately 30. As a trade-off, the AC inductance L_{AC} increases to a minimum value of 2 μH due to the different connection style. The resulting impedance Z_{AC} for the layered and parallel foil winding configurations is shown in Fig. 4.46 (a). As expected, the resonance frequency increases by a factor of approximately 3, and the magnitude of the impedance at the resonant point also increases significantly. Both factors lead to a considerable reduction in current ringing in the AC circuit, as evidenced by the AC current spectrum i_{AC} shown in Fig. 4.46 (b). Therefore, the parallel foil winding provides an effective method for reducing current ringing in the AC circuit of the DAB.

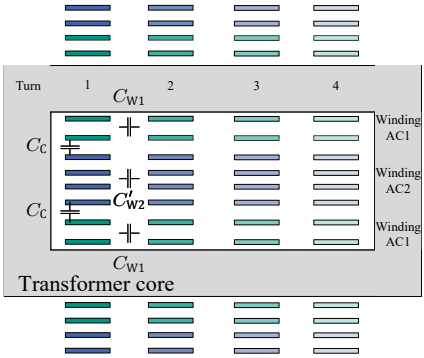
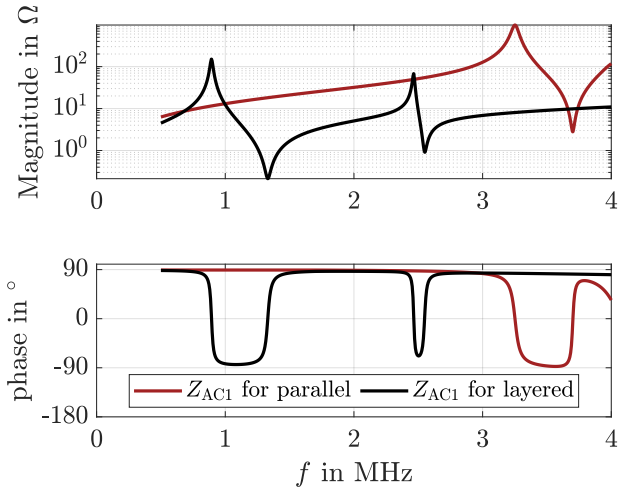
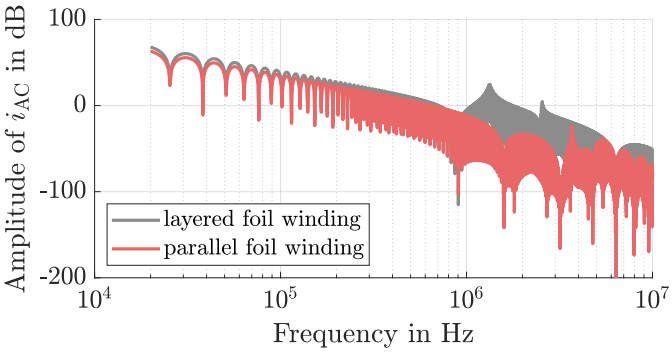


Figure 4.45: Winding configuration of the MFT with optimization of the parasitic capacitances "parallel foil winding"



(a)



(b)

Figure 4.46: Comparison of (a) Z_{AC1} for layered and parallel foil winding transformer (b) the spectrum of i_{AC} for layered and parallel foil winding transformer for a $\mathrm{d}v/\mathrm{d}t = 6\ \mathrm{kV}/\mu\mathrm{s}$

4.7 Conclusion

This chapter introduces an extended DAB model for steady state operation. Step by step, the ideal model presented in chapter 2 is expanded to include relevant non-ideal conditions. First, the AC resistance and magnetizing inductance are introduced, and their impact on ZVS behavior and the operation range is discussed. A novel and comprehensive resonant commutation model is introduced, which is utilized to determine the exact ZVS conditions necessary for highest efficiency. This includes the minimal required switching current, the optimal deadtime, and the voltage time area error (VTAE) caused by the resonant commutation process. Using this VTAE, the nonlinear transfer characteristic of the converter is derived, and appropriate countermeasures are presented. The core difference compared to the existing modelling approaches lies in the detailed treatment of the resonant commutation process. Unlike the the existing models, which do not calculate the VTAE, the ideal deadtime, minimal necessary switching current or the resulting transfer function all at once, the proposed ZVS model explicitly calculates all of these quantities based on just one mathematical framework. Furthermore, the efficiency in TCM operation is increased using the Circular Current Injection (CCI) method by ensuring ZVS operation. In the final section, the impact of parasitic AC parameters on the AC circuit is analyzed, and an improved transformer design is proposed to reduce their effect.

Chapter 5

Design of the Dual Active Bridge Converter and the Test Bench

This chapter gives an overview of the test bench and the different configurations used to validate the modelling in the previous chapters. The applied measurement methods and the measurement equipment is presented as well as the configuration of each 500 kW DAB converter and the signal processing system. The hardware of the DAB is explained and a protection method is shown. In the last section, a calorimetric measurement setup is shown to determine the distribution of power losses among the individual components of the DAB converter.

5.1 Test Bench architecture

The modelling approach of the DAB is tested on a test bench. The topology is shown in Fig. 5.1. The test bench consists of two independently controlled DABs with one controlling the V_{DC2} voltage and the other one controlling the power flow. To reduce grid requirements, a circular power flow is applied where one DC link of the the two DABs are connected to each other. A galvanic isolated DC power supply, which compensates for occurring losses, is used to reduce Electromagnetic Interference (EMI) due to jumping potentials caused by the switching of the rectifier. No communication between both DABs is implemented and the only interaction is at the Human-Machine Interface (HMI) level of the system.

However, to improve the dynamic behavior of this system, a communication between both DABs might be beneficial for improved feedforward control of load steps and voltage deviations. The resulting test bench is shown in Fig. 5.2 (a) while Fig. 5.2 (b) shows one of the two identical DAB converter cabinets.

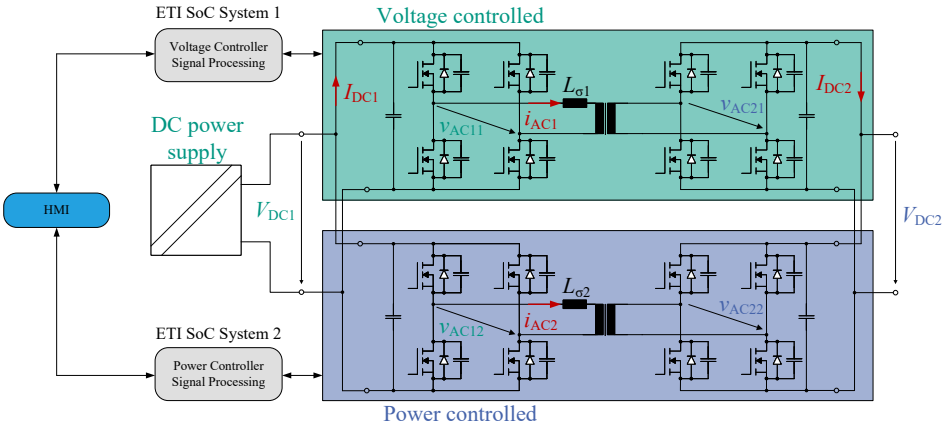
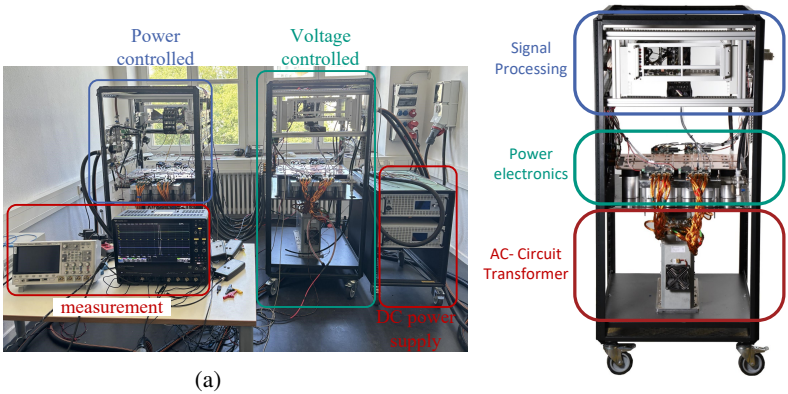


Figure 5.1: Electrical test bench setup

DAB Parameter Configuration

To ensure a robust validation of the model presented in chapter 4, the test bench is designed such that a parameter variation is possible. The two different transformer designs presented in chapter 4.6 are applied. Additionally, the stray inductance L_σ is varied. To validate the commutation model, the MOSFET output capacitance C_{OSS} is artificially adjusted by using a non-damped capacitive snubber circuit. Since the different transformer designs does have a significant impact on the behavior of the DAB, these two are differentiated as the "layered foil winding" and "parallel foil winding" setup (cf. chapter 4.6 with Fig. 4.39 and Fig. 4.45). The resulting system parameters for each setup are shown in table 5.1. The two transformer concepts do have significant different winding arrangements however, most of the parasitic components are equal except the winding capacitances C_w. The transformer stray inductance $L_{\sigma,\text{Transformer}}$ and coupling capacitances C_c are not changed significantly due to the same overlapping area



(a) (b)

Figure 5.2: (a) Test bench setup (b) DAB converter cabinet

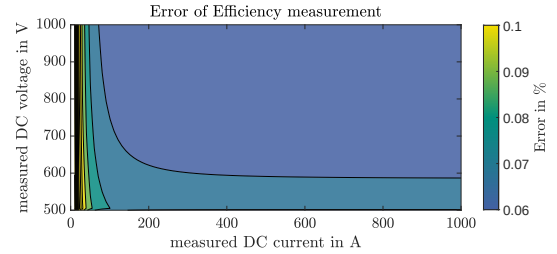
and general arrangement of both windings. The minimum possible stray inductance $L_{\sigma,\min}$ of the whole AC circuit however does change significantly due to the different connection style necessary with the improved winding arrangement (cf. section 5.2.5).

Table 5.1: System parameter for the different setups

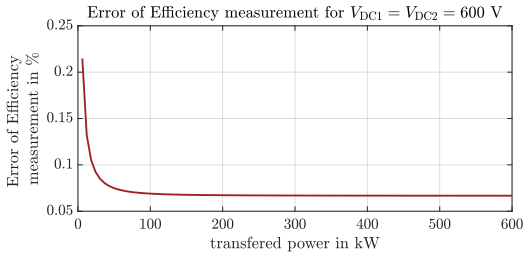
Parameter	layered foil winding	parallel foil winding
P_{max}	500 kW	
$V_{\text{DC,min}}$	500 V	
$V_{\text{DC,max}}$	800 V	
f_{sw}	20 kHz	
$L_{\sigma,\text{min}}$	0.6 μH	2 μH
	Semiconductor	
Generation	Gen 1	Gen 1 [D1] / Gen 2 [D2]
$V_{\text{DS,max}}$	1200 V	
$I_{\text{D,max}}$	1200 A	
$I_{\text{sw,max}}$	1500 A	
C_{eq}	$\approx$ 11 nF @ 700 V	$\approx$ 15 nF @ 700 V
$C_{\text{Snubber,max}}$	not investigated	24 nF
	Transformer Parameter	
$L_{\sigma,\text{Transformer}}$	0.6 μH	
C_{w}	26 nF	< 1.6 nF
C_{c}	6 nF	1 nF
n	1:1	

Efficiency Measurement

For efficiency and power measurement, the power analyzer card GN310B by *HBM* [D3] is used. The transferred power P, the losses P_{v} and the efficiency η is measured independently for each DAB. For current measurement, an additional current transducer CT1000 by *Signaltec* is [D4] necessary. This provides an accurate and highly dynamic measurement. However, for this setup the focus is set on a more accurate measurement instead of a measurement with wide frequency range since only DC values are measured to determine the efficiency of the DAB. The relevant parameter are shown in table 5.2. The resulting error of the efficiency measurement is shown in Fig. 5.3 and the error amounts to 0.06 % for the relevant measurement range.



(a)



(b)

Figure 5.3: Error of the efficiency measurement using a CT1000 current transducer and the GN310B power analyzer card for equal measured voltages $V_{DC1} = V_{DC2}$

Table 5.2: Accuracy of the efficiency measurement

	GN310B	CT1000
error measuring range (@DC)	0.015 %	0.0012 %
error measured value (@DC)	0.02 %	0.015 %
maximum bandwidth	500 kHz	300 kHz

Dynamic Measurement

Table 5.3: Parameter of Dynamic Measurement

WaveRunner 8058HD	
Channel	8
Bandwidth	500 MHz
Vertical Resolution	12 bit (up to 15 bit with enhanced resolution)
Rise Time	700 ps
Sample Rate	10 $^{GS}/_{s}$
Differential Probe	
Bandwidth	100 MHz
Rise Time	3.5 ns
Accuracy	± 2 %
Noise	< 230 mVrms
Rogowski Coil	
Typical Accuracy	± 1 %
Bandwidth	16 MHz
Peak Current	6 kA
Peak $^{di}/_{dt}$	40 $^{kA}/_{\mu s}$

For dynamic measurements and waveforms, the WaveRunner 8058HD 8 channel oscilloscope by *Teledyne Lecroy* [D5] is used. For voltage measurement the DP10013 differential probe by *Micsig* [D6] is utilized, whereas for current measurement the CWT30 rogowski coil by *PEM* [D7] is applied.

5.2 Dual Active Bridge Converter

In the previous chapter the full test bench was presented. It consists of two nearly identical DAB converters which are presented in this section. All relevant components are discussed including the signal processing system, protection circuits, measurements and gate driver.

5.2.1 Signal Processing System

The central signal processing system is based on the SoM PicoZed 7030 board with at the Institute of Electrical Engineering (ETI) in-house designed mainboard

which in combination forms the ETI System on Chip (SoC) System [72]. The key characteristics are shown in table 5.4. The PicoZed 7030 provides a dual-core ARM Cortex-A9 and a Kintex-7 FPGA [D8]. In Fig. 5.4, the division of tasks between ARM core and FPGA is shown. All critical functions such as the controller and measurements are implemented on the FPGA for real time capabilities. Only non-critical features are implemented on the ARM core as well as the HMI is located on the ARM core. The HMI is realized using a Ethernet-Interface and a communication with the processing unit is possible from a standard PC. Additionally, a CAN-Interface is provided which enables communication with auxiliary systems, such as cooling units. Due to varying applications for different test benches the system has to be highly modular and versatile. This is achieved by using different Extension Card (EC) on the mainboard which are exchangeable with each other. For the DAB three different ECs are necessary, the Analog-Digital Conversion (ADC) EC which provides a high performance analog digital conversion (shown in Fig. 5.5 (b)), an optical fiber EC for EMI resistant communication (shown in Fig. 5.5 (c)) and the optical fiber card with FPGA extension for faster response times and multiplexing of signals (shown in Fig. 5.5 (d)).

ADC Card

The ADC EC utilizes the LTC2325-16 ADC-chip with four analog inputs which have simultaneous sampling at 5 $\mathrm{Ms/s}$ and a resolution of 16 bits. The analog front-end allows inputs in the range of ± 10.24 V. For current measurement and current signals an adapter board is necessary. However, this adapter board is fully supplied by the ADC EC and no additional auxiliary system is necessary. In total, the ADC EC consists of three ADC-chips and therefore a maximum of 12 analog channels are possible. The PCB is shown in Fig. 5.5 (b)). In Fig. 5.4 the various task are depicted. ADC EC does provide measurement signals for the calorimetric measurement as well as the DC current measurements. All of these signals are current signals. Hence, for each ADC the adapter board is necessary.

Optical Fiber Card

The DAB communication is solely achieved by optical fibers for a higher resilience to EMI. Therefore, an important EC is the optical fiber card which has two different versions. One is the normal optical fiber card with a total of eight transmitter and eight receiver using the AFBR-1624Z and AFBR-2624Z, respectively. Each one has a data throughput of 50 MBd. The second optical fiber card

Table 5.4: Characteristic of the ETI SoC System

	PicoZed 7030
Processor Core	ARM Cortex A9 Dual Core
On-Chip Memory	256 kB
Clock Rate	667 MHz
Programmable Logic	Kintex-7 FPGA
Logic Cells	125000
PL IOs	250

has an extension using a MAX10 FPGA for multiplexing and low level logic operation. Using this extension a maximum of twelve transmitter and twelve receiver are possible. Additionally, using the MAX10 low level protection such as overvoltage and overcurrent protection can be achieved much faster compared to the central FPGA unit. That is the reason why the MAX10 optical fiber card is used for the gate driver signals and error feedback of the gate driver. Whereas the reduced version does control the voltage measurement.

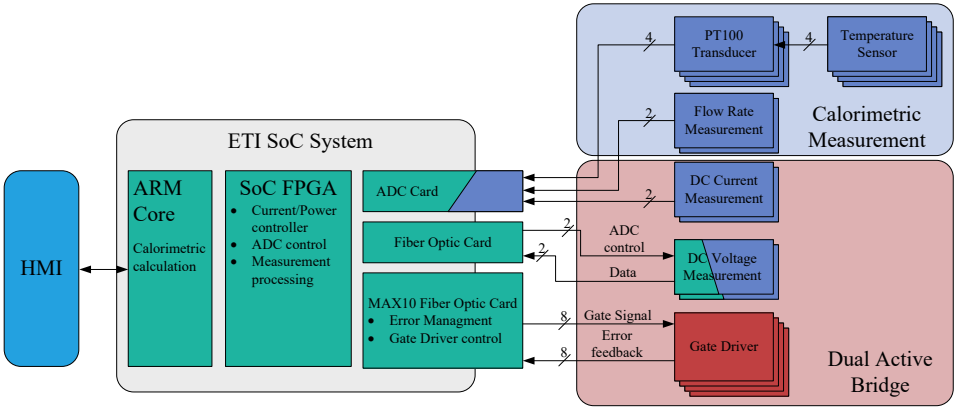
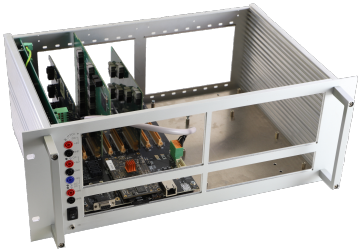


Figure 5.4: Design of the Signal Processing



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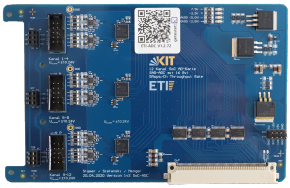

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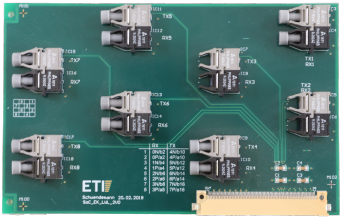

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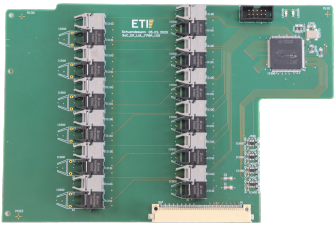


(d)

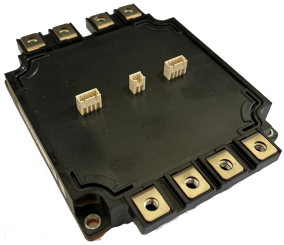
Figure 5.5: (a) SoC as central processing unit (b) ADC card (c) fiber optic card (d) MAX10 fiber optic card

5.2.2 Power MOSFET Module

The power SiC MOSFET module used for this DAB is the FMF1200DX1-24A (Gen1) [D1] and FMF1200DXZ-24B (Gen2) [D2] by *Mitsubishi Electric*. The characteristics and differences of both SiC MOSFET modules are shown in table 5.5. The module itself is shown in Fig. 5.6(a). In comparison, the Gen2 module does provide lower overall losses (conduction and switching) while having $\approx 40\%$ more output capacitance. This does increase the minimal necessary switching current for ZVS. In case of the gate characteristics, both modules behave similar with the second generation having a reduced total gate charge compared to the first generation. This enables both modules to be controlled with the same gate driver hardware.

Snubber Capacitance

In [22], a snubber capacitance in parallel to the MOSFETs is employed to reduce switching losses and improve the efficiency of a DAB. The main idea behind a lossless snubber capacitance is to reduce the MOSFET current at the turn-off instant by dividing it between the MOSFET channel and the snubber capacitance, which also needs to be charged. In theory, the larger the capacitance, the smaller the MOSFET turn-off current, resulting in reduced losses. However, practical applications impose limitations on the size of a snubber capacitance. The first limiting factor is the high-frequency oscillations that can occur between the MOSFET output capacitance, the DC link, and the snubber capacitor. Increased snubber capacitance intensifies these oscillations, necessitating a trade-off between oscillation and loss reduction. Secondly, a low-inductive connection is essential to reduce oscillations and lower the impedance of the snubber, facilitating an efficient current share between the snubber capacitor and the MOSFET output capacitance. The third limiting factor is the reduction of the ZVS operation range for the DAB. The snubber capacitance C_{Snubber} acts as a voltage-independent enlargement of the equivalent capacitance C_{eq} introduced in chapter 4.3. This leads to a higher necessary minimum switching current i_{sw} and increased deadtime to achieve cZVS and minimal turn-on losses. The deadtime diagram for SPS and 1:1 operation, with and without a snubber capacitance of $C_{\mathrm{Snubber}} = 24$ nF, is shown in Fig. 5.7. The optimal deadtime $T_{\mathrm{dt,opt}}$ and the minimal necessary switching current $i_{\mathrm{sw,min}}$, to achieve full ZVS, increases with approximately $\sqrt{(C_{\mathrm{eq,MOSFET}}+C_{\mathrm{Snubber}})/C_{\mathrm{eq,MOSFET}}}$ (cf. (4.32,4.34)). Depending on the optimized operation points the snubber capacitance can therefore be limited due to the ZVS behavior of the DAB.



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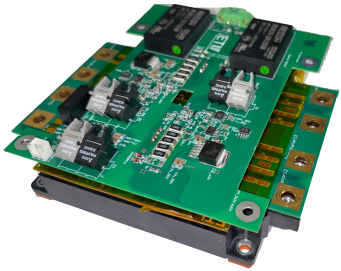

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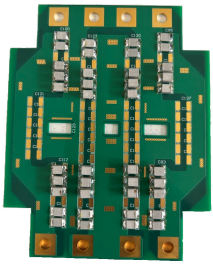


(c)

Figure 5.6: (a) SiC MOSFET module (b) Snubber PCB with gate driver PCB on the MOSFET module (c) Snubber PCB with a capacitance of $C_{\text{snubber}} = 24$ nF per MOSFET switch

Table 5.5: Characteristics of the SiC MOSFET modules

Symbol	Parameter	Gen1	Gen2
	Maximum Values		
V_{DS}	Drain-Source Voltage	1200 V	
I_D	Continuous Drain Current	1200 A	
$I_{D,turnoff}$	Turn-off Drain Current	1500 A	
	Electrical Characteristic		
$C_{Q,eq}$	Charge based Capacitance @ 700 V	11 nF	15 nF
E_{on}	Turn On Energy ($V_{DS} = 600$ V, $I_{sw} = 1200$ A)	90 mJ	66 mJ
E_{off}	Turn Off Energy ($V_{DS} = 600$ V, $I_{sw} = 1200$ A)	82 mJ	54 mJ
$R_{DS,on}$	Drain-Source On State Resistance @ $T_j = 150$ °C	1.8 mΩ	1.5 mΩ
Q_G	Total Gate Charge	5.2 μC	2.6 μC

As a compromise between reduced turn-off losses, limited oscillations, and a sufficiently large ZVS range, the snubber capacitance was set to $C_{Snubber} = 24$ nF for each MOSFET switch. To minimize the inductance of the connection, a PCB with 8 interlocking layers was designed. To achieve the desired capacitance and high surge current capabilities, 20 C0G ceramic capacitors in parallel were used. The mechanical design is shown in Fig. 5.6 (b) and (c). The direct connection of the PCB to the MOSFET terminals helps to minimize inductance as much as possible. Using this setup, a maximum snubber capacitance temperature of 60°C was achieved.

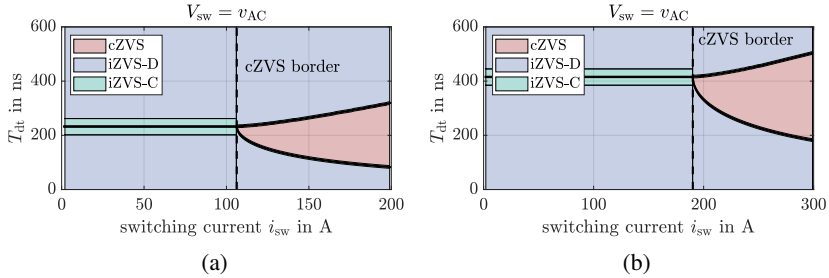


Figure 5.7: Deadtime diagram for $V_{DC1} = V_{DC2} = 600$ V (a) without snubber (b) with snubber capacitance $C_{Snubber} = 24$ nF per MOSFET

5.2.3 Gate Driver

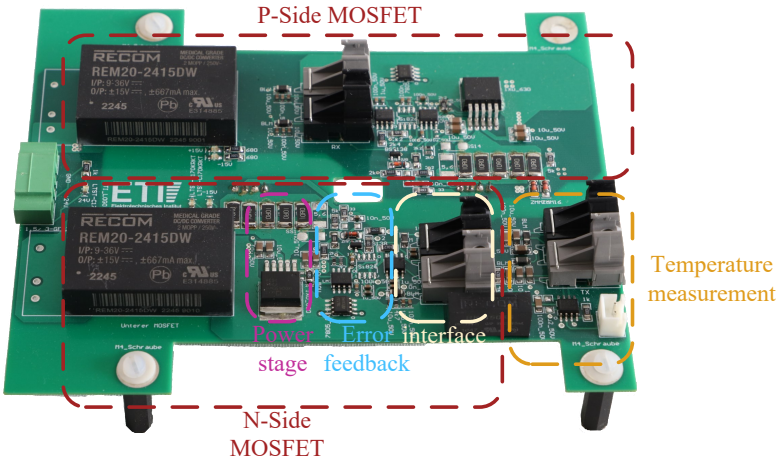


Figure 5.8: PCB of the resulting gate driver

The Gate Driver (GD), shown in Fig. 5.8, fulfills two important roles for a DC/DC converter. Firstly, safe turn on and turn off has to be ensured. For that an IXD630 MOSFET driver power stage is used. This power stage does provide a sufficient peak gate current of up to 30 A with a maximum possible switching voltage of ± 20 V. This results in a minimal gate resistor of 1 Ω which is lower then recommended for the SiC MOSFET power module. The maximum switching frequency using this GD is $f_{\mathrm{sw,max}} = 30$ kHz due to thermal limitations. The second task of the GD is the module protection in case of overcurrent caused by a Short Circuit (SC) or controller malfunction. This is especially important using SiC power devices. Due to the reduced chip thickness and the reduced desaturation effect, the SC withstand time is drastically reduced for SiC MOSFETs ($< 1 - 10\ \mu$s) compared to traditional Si IGBTs ($> 10\ \mu$s) [73]. But the fast turn off transient for SiC can also increase the difficulty in handling a SC for SiC MOSFETs since higher currents will result in increased overvoltage stress for a fast turn off. That is why a slow turn off or multi stage turn off might be necessary to handle the SC. However, this will further increase the SC response time and increase the thermal stress due to higher losses. Especially for IGBTs the state

of the art method for SC is a desaturation method [74, 75]. Nevertheless, this method is often not fast enough and does not provide soft turn off or overcurrent protection in a switching event. That is why a mirror source detection method is used in this DAB [76, 77, E10]. In combination with the Real Time Current Control (RTC) provided by Mitsubishi Electric, a fast and low stress overcurrent and SC turn off can be implemented. The resulting simplified circuit diagram of the gate driver is shown in Fig. 5.9 and the simplified waveforms in case of a SC in Fig. 5.10.

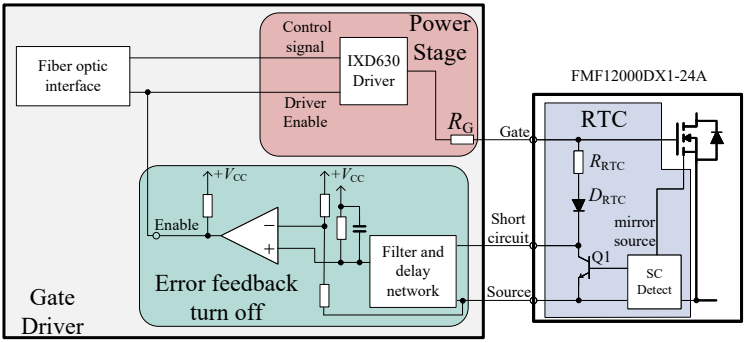


Figure 5.9: Gate Driver Circuit with mirror source overcurrent protection

t_0 to t_1: At $t = t_0$ the short circuit occurs and the current is increasing fast until the overcurrent detection threshold of $i_D = i_{D,th}$ at $t = t_1$ is reached.

t_1 to t_4: Upon reaching the current threshold, the SC is detected. However, there is a delay up to t_2 at which the transistor Q1 is turned on and the short circuit output pin of the module is reduced to source potential. Additionally, the gate voltage V_{GS} is reduced due to the voltage divider of R_G and the RTC resistor R_{RTC} (cf. (5.1)). A typical value for this voltage should be between 3 V and 6 V. This reduction of the gate voltage of the MOSFET will result in an operation in the active region and will limit or even reduce the SC current. Nevertheless, in this operation mode very high losses occur due to the high voltage between drain and source V_{DS}. Between t_3 and t_4 the GD itself does detect the short circuit

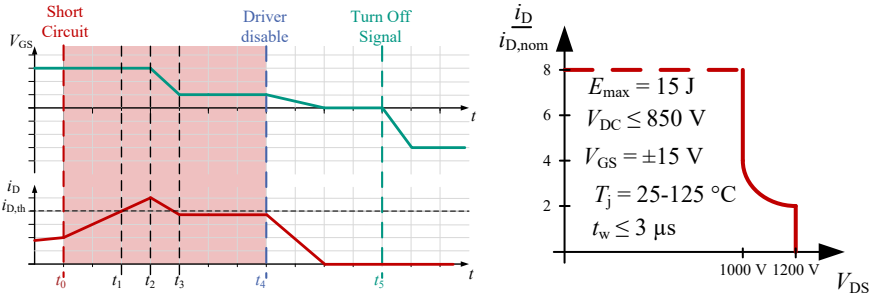


Figure 5.10: (a) Gate voltage V_{GS} and drain current i_D using the mirror source overcurrent protection (b) Short Circuit Safe Operating Area (SCSOA)

output of the module. To ensure a slow turn off a small delay network is applied which will add a delay of around 200 ns.

$$V_{GS} = \frac{R_{RTC}}{R_{RTC} + R_G} \cdot \left(V_{turn,on} - V_{f,Drtc-V_{Q1}}\right) + V_{f,Drtc} + V_{Q1} \tag{5.1}$$

t_4 to t_5: When the GD does detect the overcurrent event it will turn off the power stage of the gate driver. This is done by disabling the IXD630 which will lead to an open circuit at the gate. Due to the passive discharge, the gate will be discharged to 0 V slowly which ensures a low voltage stress turn off. At the same time a feedback signal is send to the superordinate control system of the converter which will turn off the converter to achieve a full turn off at t_5.
In total, the time between the SC and the turn off at t_4 should not be more than $t_{max} = 3\ \mu$s to avoid damaging the MOSFETs.
To check whether the Short Circuit Safe Operating Area (SCSOA) in Fig. 5.10 (b) is complied and to test the performance of the overcurrent and SC protection, measurements are carried out. Two different scenarios are tested. The first scenario is turning on to an existing SC with low inductance. This is shown in Fig. 5.11 (a) and the operating area compared to the SCSOA in Fig. 5.11 (b). The second scenario is a high inductive load which models a SC within the transformer

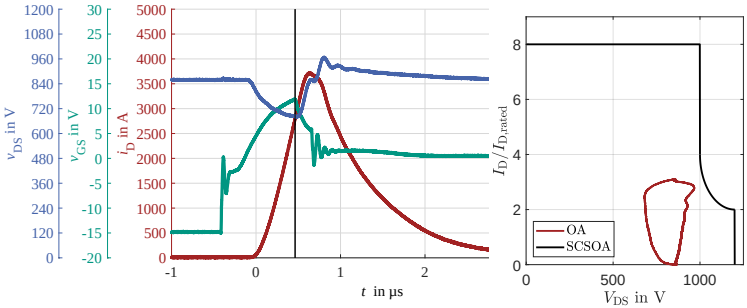


Figure 5.11: Measurement for $V_{DC} = 850$ V (a) waveforms for a turn on to an existing SC with a low inductive (b) Operating Area (OA) compared with the SCSOA

of the DAB. The resulting waveform is shown in Fig. 5.12 with an inductance of $L_\sigma = 2\ \mu$H. The key performance indicators for different junction temperatures T_J are shown in Fig. 5.13. The SCSOA is not violated at any operation point. Therefore, an efficient overcurrent and SC protection is implemented.

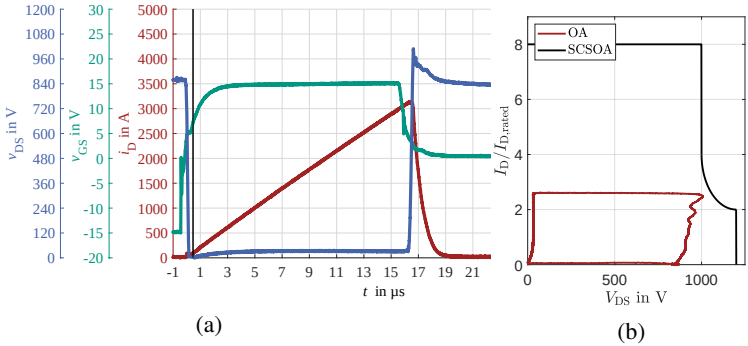


Figure 5.12: Measurement for $V_{DC} = 850$ V (a) waveforms for a high inductive SC (b) OA compared with the SCSOA

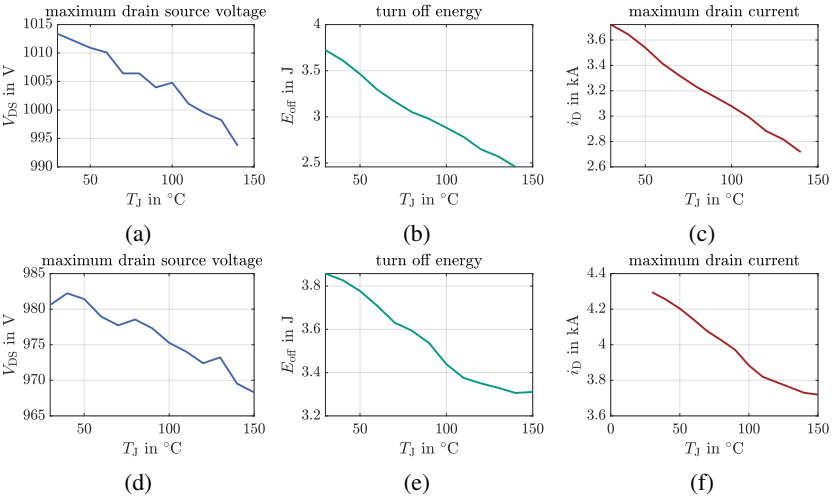


Figure 5.13: Measurements for $V_{DC} = 850$ Vand maximum drain source voltage V_{DS}, turn off energy E_{off} and maximum drain current i_D (a)-(c) for a high inductive SC (d)-(f) and for a low inductive SC

5.2.4 DC circuit

The DC circuit of the DAB comprises the DC-Link itself, the DC connections, and the necessary measurements of the DC current I_{DC} and DC voltages V_{DC}. The key requirements of the DC-Link include having sufficient capacitance to minimize the voltage ripple caused by the switching of the FB, a low inductive design to reduce overvoltage stress on the semiconductors, and an increased switching speed capability for hard-switching operation points. Additionally, the RMS current capabilities of the capacitors and bus bars are crucial design factors. For MF applications, the voltage ripple is typically not a concern since the oscillating energy due to the MF waveforms is much smaller compared to the stored energy. However, the RMS current capability is particularly important for DAB applications due to the presence of high AC components in the DC-Link current during buck and boost operation, especially when using TCM [52]. As a result, foil capacitors are preferred over electrolytic capacitors due to their superior current handling capabilities. In this design, the E50.N14-384NT0 foil capacitor by *Electronicon* is used [D9]. To minimize the inductance, a layered structure using 3 mm thick copper bars was selected. This design allows for a large cross-sectional area, ensuring low resistance at high frequencies, despite skin and proximity effects typically encountered in the DC-Link during buck and boost operation. The resulting DC-Link parameters are shown in table 5.6. Figure 5.14 illustrates the resulting design of the DC circuit, while Fig. 5.15 depicts the corresponding DC connections of the DAB, along with the DC voltage and DC current measurement points.
During the DC-Link design, it is crucial to connect the semiconductor module terminals as symmetrically as possible to ensure an even current distribution at the connection points. This is especially important since the FMF1200 modules lack internally connected DC terminals. The design of the DC circuit was evaluated through double-pulse testing. Figure 5.16 (a) shows the turn-off overvoltage ΔV_{DS} for different switching currents i_{sw}. Figure 5.16 (b) illustrates the corresponding turn-off current slope $\mathrm{d}i/\mathrm{d}t$. From these measurements, the commutation inductance L_{DC} of the DC-Link, including the parasitic inductance of the semiconductor, can be determined as shown in (5.2).

$$L_{DC} = \frac{\Delta V_{DS}}{\mathrm{d}i/\mathrm{d}t} \approx 25\ \mathrm{nH} \tag{5.2}$$

Figure 5.17 presents the resulting voltage slope $\mathrm{d}v/\mathrm{d}t$ for this setup. The maximum value is below $7\,\mathrm{kV}/\mu\mathrm{s}$, which does not pose any extra problems for the AC circuit

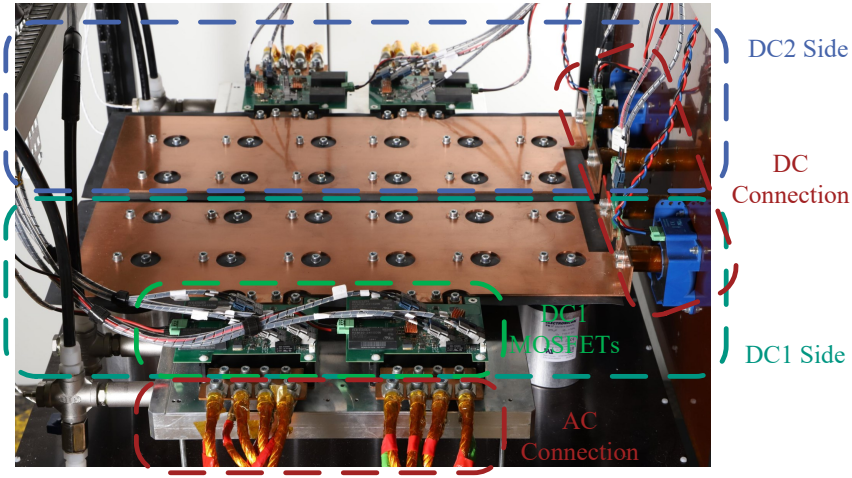


Figure 5.14: DC-Link

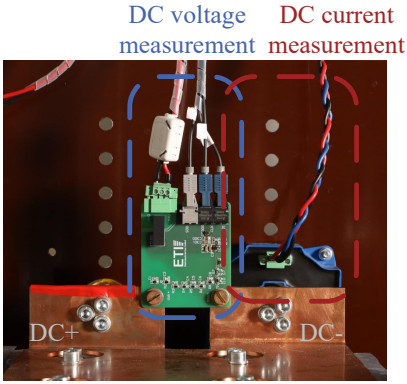


Figure 5.15: Connections of the DC side

Table 5.6: Parameter for DC Link and DC Capacitor

Symbol	Parameter	Gen1
	Parameter of Capacitor	
$V_{\mathrm{DC,max}}$	Maximum DC Link voltage	1100 V
$C_{\mathrm{DC,Cap}}$	Capacitance of Capacitor	375 μF
$I_{\mathrm{C,max}}$	Maximum RMS current per capacitor	90 A
$L_{\sigma,\mathrm{Cap}}$	Capacitor stray inductance	40 nH
	Parameter of DC Link	
n_{C}	Amount of parallel capacitor	12
C_{DC}	total DC link capacitance	4.5 mF
$I_{\mathrm{DC,max}}$	Maximum DC link AC current	1080 A
$L_{\sigma,\mathrm{DC}}$	DC Link stray inductance	10 nH

and the transformer insulation. The resulting hard-switching energies are shown in Fig. 5.18 at $T_{\mathrm{j}} = 30°\mathrm{C}$.

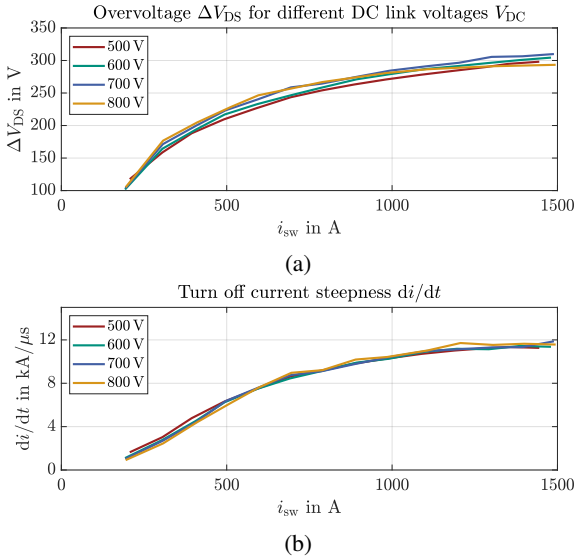


Figure 5.16: (a) Overvoltage ΔV_{DS} and (b) current steepness $\mathrm{d}i_D/\mathrm{d}t$

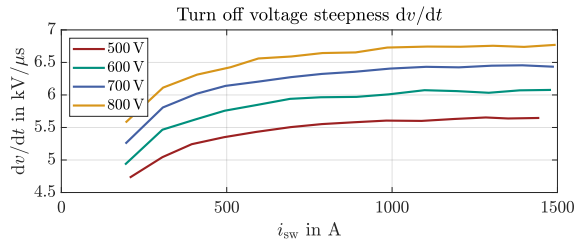


Figure 5.17: Voltage steepness $\mathrm{d}v/\mathrm{d}t$ for a turn off

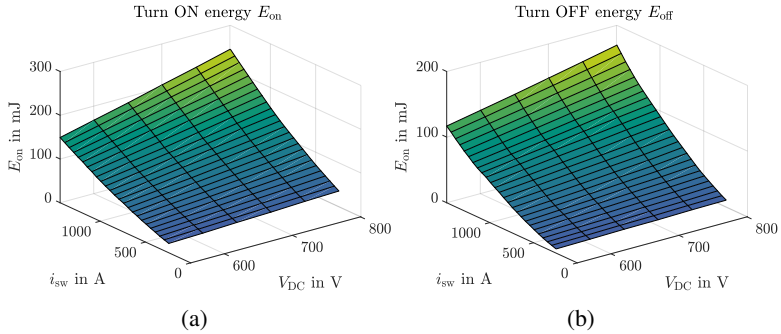


Figure 5.18: (a) Turn ON energy (b) Turn OFF energy for a double pulse

5.2.5 AC circuit

The AC circuit consists of two main components, the MFT as well as the connection between the semiconductors and the MFT. The design of both is essential for the behavior of the DAB.

Medium Frequency Transformer

The MFT used is designed by *Schmidbauer transformers and Equipment GmbH* and depicted in Fig. 5.19. One of the biggest challenges in designing a MFT for high power applications is the winding configurations. Due to the high AC frequency of the DAB, the skin and proximity effects does have a significant impact on the AC resistance of the transformer [47]. The two main winding methods to reduce the AC resistance are a litz wire winding and a foil winding (cf. section 4.6). Using litz wire does have an advantage of an easy and flexible construction which is why it is preferred in low cost, low power applications. However, using litz wire at high power, high frequency operation does have significant disadvantages. Litz wires have a low fill factor due to the insulation layer at each individual strand. Therefore, a higher cross section is necessary. Additionally, the connection of the litz wire is difficult at higher cross sections. The cable lug has to be pressed and soldered for a low impedance connection but this will result in uneven distribution of the current between each strand of the litz wire [78]. That is the reason why foil windings are proposed for higher power applications [48]. The advantage is a high fill factor and the connection is easy to

Table 5.7: Transformer parameter for the different winding configuration

Parameter	layered foil winding	parallel foil winding
Transformer Parameter		
$L_{\sigma,\text{Transformer}}$	0.6 μH	
C_{w1}	$\approx$ 26 nF	$\approx$ 0.25 nF
C_{w2}	$\approx$ 26 nF	$\approx$ 1.6 nF
C_{c}	$\approx$ 6 nF	$\approx$ 1 nF
V_{max}	850 V	
I_{max}	1140 A	
P_{max}	640 kW	
$\mathrm{d}v/\mathrm{d}t$	12 kV/μs	
n	1:1	
cooling	air	
weight	$\approx$ 100 kg	
power density volumetric	$\approx$ 11 kW/l	
power density gravimetric	$\approx$ 6.4 kW/kg	

accomplish. The disadvantage is a more complex construction of the system and increased parasitic capacitances C_{w} and C_{c}. For this system, two foil winding configurations are utilized. A parallel foil winding and a layered foil winding presented in section 4.6. The parameter of each transformer configuration is shown in table 5.7

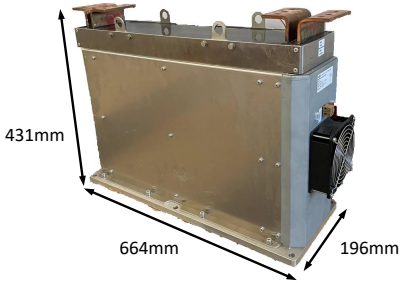
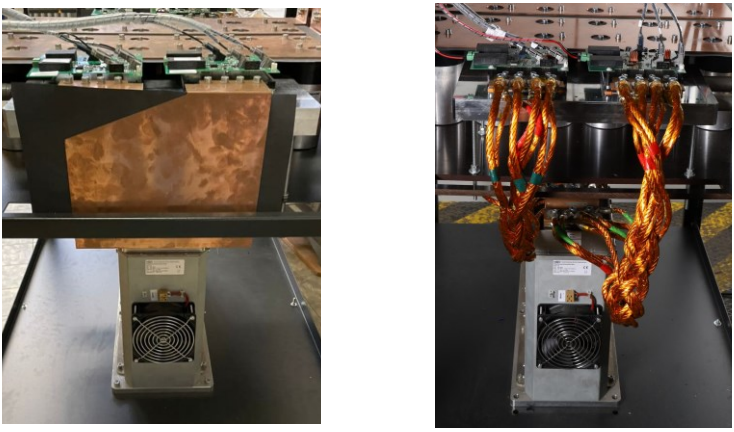


Figure 5.19: Picture of the MFT



(a) (b)

Figure 5.20: (a) Transformer connection using copper bars (b) Transformer connection using multiple litz wire in parallel

Transformer Connection

The connection of the transformer to the power electronics can be made similarly to the MFT using either a foil or copper bar or litz wires. Both setups are shown in Fig. 5.20. In addition to the previously mentioned advantages and disadvantages of both conductor styles, the litz wire does provide a flexibility in the litz wire routing which makes it easy to tune the AC inductances of the DAB. This outweighs the disadvantages of the increased AC resistance due to the wire connectors in a prototype setup (especially since outside of the transformer a higher copper cross section can be achieved by paralleling multiple litz wire). However, for a series product the copper bar would be the preferred connection style. For this setup, the resulting additional inductance due to the connection can vary between 0.2 μH and a maximum of 2.5 μH depending on the length of the litz wire and copper bar.

5.2.6 Calorimetric Measurement

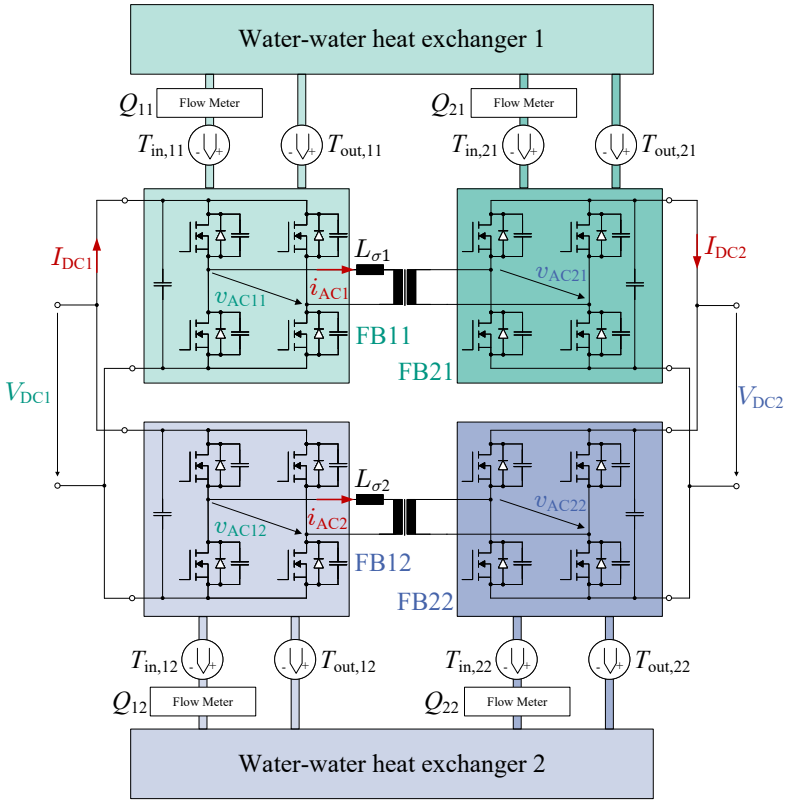


Figure 5.21: Calorimetric measurement setup

To acquire a loss distribution of the DAB, a calorimetric measurement setup was constructed to accurately determine the semiconductor losses. This setup is shown in Fig. 5.21. Each DAB has its own cooling circuit to avoid mutual influence of the two DABs. For each FB, the input and output water temperature $T_{\text{in/out}}$ is measured using a screw-in PT100 temperature sensor [D10]. To improve accuracy of the measured values, the PT100 sensor has to be in the wa-

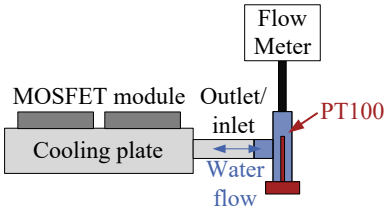


Figure 5.22: Positioning of the temperature sensors for the calorimetric measurement

ter flow that is why the setup in Fig. 5.22 is applied. That way, the PT100 is completely immersed in the water flow. For an accurate measurement value acquisition, the appropriate PT100 transducer is used [D11]. Additionally, for each full bridge the water flow rate Q is measured using the flow meter *DFM-Ms-AN* [D12] and *DFM-POM-AN* [D13] by *Bio-Tech e.K.*. Both flow meter have similar performance. Using (5.3), the resulting calorimetric losses due to the semiconductor switches for each FB can be determined using the heat capacity of water c_p and the density of water ρ. To eliminate temperature dependencies of the temperature measurement and flow rate measurement, a constant inlet temperature is necessary. In this case the temperature was chosen to be 20 °C which represents the room temperature. Additionally, a constant water temperature of 20 °C will result in minimal heat dissipation of the cooling plate, the water and the power module to the surrounding air since this is equal to the room temperature of the laboratory. A full thermal insulation of the system is not feasible due to the size of the components and the test bench overall. The resulting system parameters of this setup are shown in table 5.8. The flow rate Q is in theory a freely selectable parameter, in this application however there are several limiting factors to the flow rate. On the one hand, the flow rate has to be high enough to cool down the semiconductors and should enable the highest possible power loss. On the other hand, the flow rate should be as low as possible to increase the accuracy of the calorimetric measurement. This is due to the limited accuracy of the PT100 temperature sensor. With a lower flow rate Q the temperature difference between in and outlet will increase for the same semiconductor losses which will in result in increased accuracy. A good compromise between these two contradictory goals is between 7 $^{\mathrm{l}}/_{\mathrm{min}}$ and 8 $^{\mathrm{l}}/_{\mathrm{min}}$. Small deviations between the FB flow rates is due to asymmetrical structure of the water supply tubes. In addition the measurement

Table 5.8: System parameters of the calorimetric measurement system

Parameter	FB11	FB21	FB12	FB22
Q	7.21 $^{l}/_{min}$	8.2 $^{l}/_{min}$	6.75 $^{l}/_{min}$	7.3 $^{l}/_{min}$
T_{in}		20 °C		
T_{out}		35 °C		
$P_{meas,max}$		≈ 7 kW		

range of the PT100 measurement transducer is designed for maximum accuracy which results in a reduced measurement range between 15 °C and 35 °C and the corresponding maximum measurable losses of ≈ 7 kW.

$$P_{v,calo} = (T_{out} - T_{in}) \cdot Q \cdot c_p \cdot \rho \tag{5.3}$$

To ensure accuracy of the calorimetric measurement setup, reference measurements are performed. A constant DC current is injected in the anti parallel diodes of the MOSFETs to generate a constant and easy to measure electrical power loss P_v in the power modules. The resulting electrical power P_v is measured using a power analyzer and compared to the measured calorimetric power losses $P_{v,calo}$. The resulting error ε can be calculated according to (5.4). That way each FB can be measured and verified independently. The resulting error ε of the calorimetric measurement are shown in Fig. 5.23 and Fig. 5.24 for each FB. For a power loss above 500 W, the error is between $\pm 2\%$. This is regarded as sufficiently accurate for the purpose of a loss decomposition. Therefore, the calorimetric measurement principle is validated. The transformer losses are estimated by measuring the overall DAB losses and subtracting the power module losses determined by the calorimetric measurement. However, this only holds for the assumption that all additional losses (eg. capacitor losses, bus bar losses etc.) are negligible compared to the transformer. Further breakdown of the losses is not possible with this setup.

$$\varepsilon_{calo} = \left(\frac{P_{v,el}}{P_{v,calo}} - 1 \right) \cdot 100\% \tag{5.4}$$

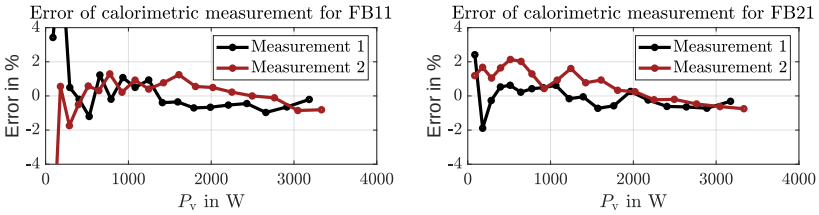


Figure 5.23: Error for calorimetric loss measurement for the voltage controlled DAB

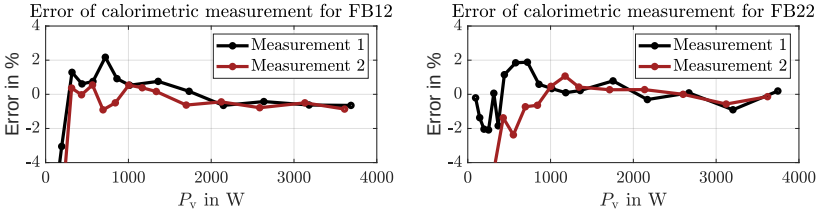


Figure 5.24: Error for calorimetric loss measurement for the power controlled DAB

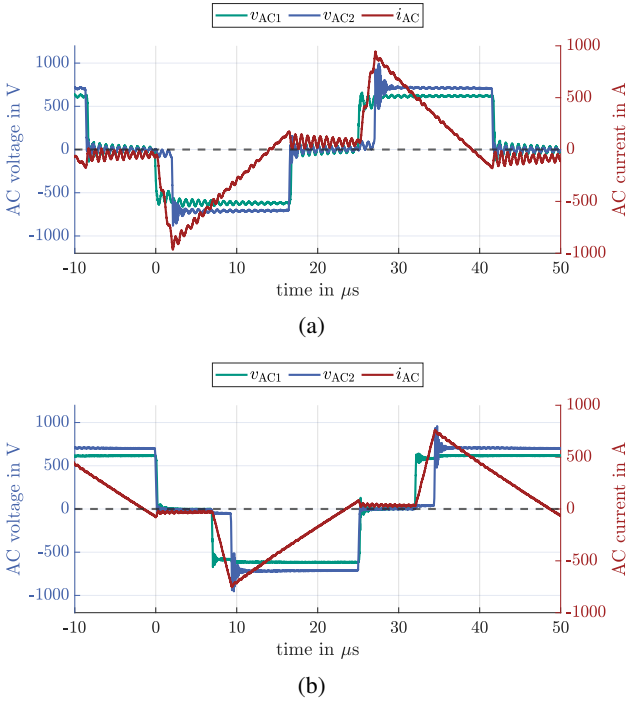
Chapter 6

Measurement results

This chapter provides experimental verification of the presented models and theoretical findings on the full-scale DAB prototype introduced in chapter 5. First, the time domain behavior of the DAB with different stray inductances L_σ and transformer designs is presented for different operating points. Since the impact of the transformer on the efficiency is essential, this is followed by an analysis of the transformer model and the improvement through an optimized winding design. The efficiency and loss distribution of the DAB are then analysed. To assess the accuracy of the resonant commutation model, its impact on both SPS and TCM operation is validated. On this basis, the performance of the FBL linearisation method and the efficiency improvements achieved by CCI are demonstrated. Unless otherwise stated, all measurements are made using the Gen 1 MOSFET chipset. For both inductance configurations, $L_\sigma = 0.6\ \mu$H and $L_\sigma = 1.2\ \mu$H, the layered foil winding transformer is used, resulting in HF oscillations in both cases. All measurements with $L_\sigma = 2\ \mu$H are made using the parallel foil winding configuration, which does not exhibit HF oscillations.

6.1 Time Domain Behavior

To get a comprehensive overview of the DAB behavior, the first step is to analyse the time domain waveforms for both SPS and TCM over the three main configurations with $L_\sigma = 0.6\ \mu$H, $L_\sigma = 1.2\ \mu$H, and $L_\sigma = 2\ \mu$H. Figure 6.2 shows the operation at $P \approx 300$ kW with SPS operation for all three configurations.
It can be seen that a decrease in AC inductance results in a more dominant voltage drop across the MOSFETs on state resistances, which is reflected in a steeper

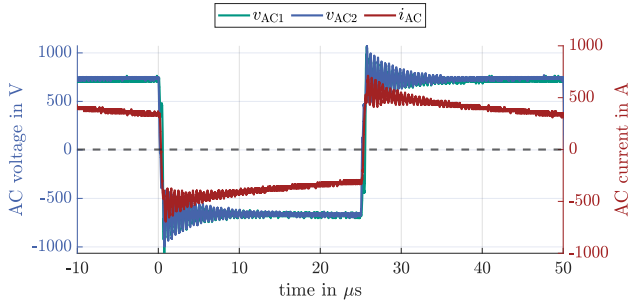


(a)

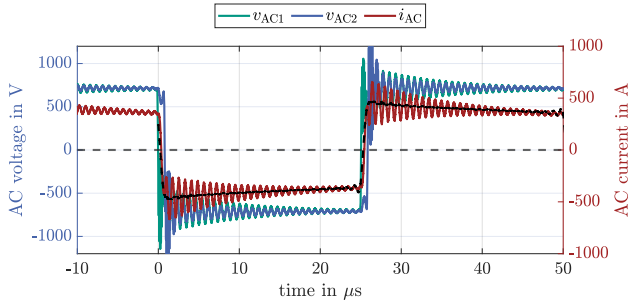
(b)

Figure 6.1: Waveform with TCM for $V_{DC1} = 600$ V, $V_{DC2} = 700$ V and $P \approx 160$kW: (a) $L_\sigma = 1.2\ \mu$H, (b) $L_\sigma = 2\ \mu$H

current drop as described in section 4.1. In addition, the lower inductance configurations and the layered foil transformer exhibit significant HF oscillations for both AC current i_{AC} and AC voltages v_{AC1} and v_{AC2}. Looking at the TCM operation in boost and buck mode, shown in Fig. 6.1 and Fig. 6.3 respectively, the influence of non-linear commutation becomes apparent, as described in the commutation model. This can be seen in the AC current i_{AC} during the free wheeling states. The current is expected to be zero there but due to the commutation it has a remaining deviation. Again a strong oscillations can be observed for the setups with the layered foil transformer. For both SPS and TCM the AC waveforms corresponds to the expected behavior explained in the previous chapters. In the following the individual parasitic effects are discussed and analyzed separately.



(a)



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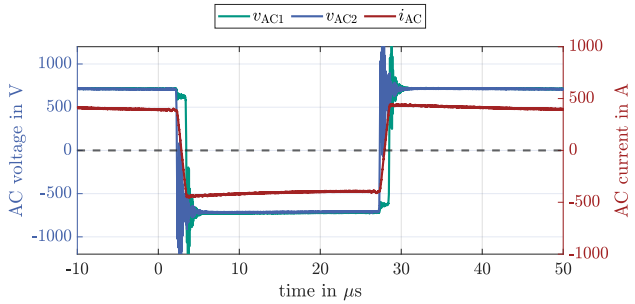
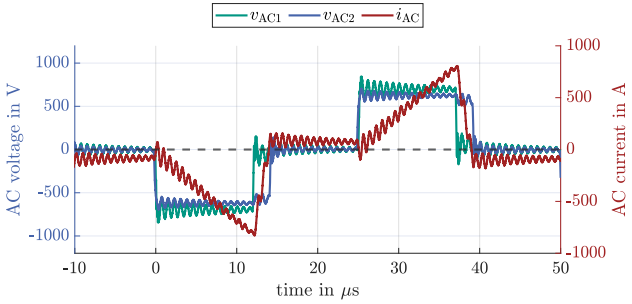
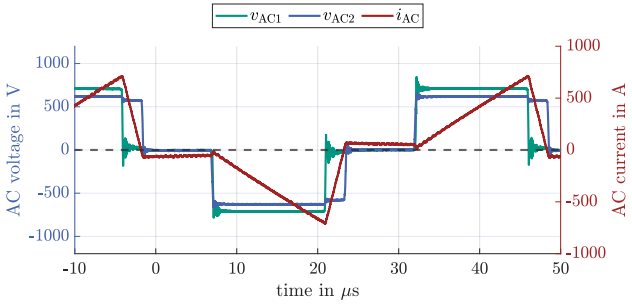


(c)

Figure 6.2: Waveforms with SPS for $V_{DC1} = V_{DC2} = 700$ V and $P \approx 300$kW: (a) $L_\sigma = 0.6\ \mu$H, (b) $L_\sigma = 1.2\ \mu$H, (c) $L_\sigma = 2\ \mu$H



(a)



(b)

Figure 6.3: Waveform with TCM for $V_{DC1} = 700$ V, $V_{DC2} = 600$ V and $P \approx 160$kW: (a) $L_\sigma = 1.2\ \mu$H, (b) $L_\sigma = 2\ \mu$H

6.2 Transformer Characteristics

In section 4.6, the HF model of the MFT was presented. To validate the presented model, the calculated frequency dependent impedance Z_{AC} is compared with measurements. The results for the layered foil winding are shown in Fig. 6.4 and the parallel foil winding in Fig. 6.5. Both transformers can be modelled using the presented approach. In addition, it can be observed that the parallel foil winding provides a higher impedance at HF and therefore a reduced susceptibility to oscillations can be observed. This can also be seen in the AC waveforms of both setups shown in Fig. 6.6. Here, no oscillations are observed for the parallel foil winding, whereas the layered foil winding shows significant oscillations in the AC voltages $v_{AC1/2}$ and the AC current i_{AC}.

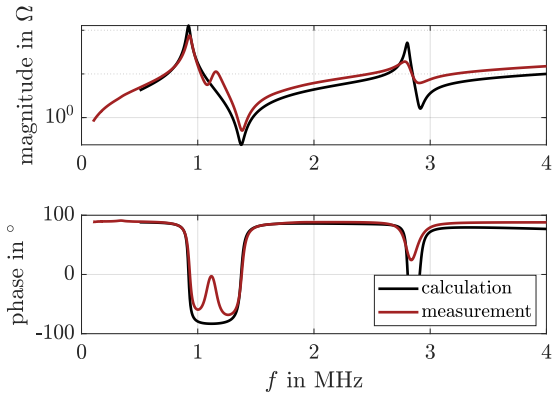


Figure 6.4: Measured and calculated transformer impedance Z_{AC1} of the layered foil winding

As discussed in chapter 4.6, the amplitude of the current ringing is highly dependent on the phase shifts of the DAB due to the superposition of the two FB operations. Considering only the SPS operation, the dependence of the current ringing on the DAB operating point can be reduced to the phase shift φ. Due to the dependence of the transmitted power P on the phase shift φ, the amplitude changes with the transmitted power of the DAB. The comparison between measurement and model of the initial amplitude of the current i_{osci} is shown in Figs. 6.7 (a) and 6.8 (a). Assuming that this oscillation is fully damped within half

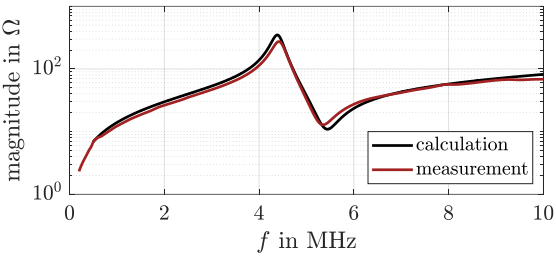


Figure 6.5: Measured and calculated transformer impedance Z_{AC1} of the parallel foil winding

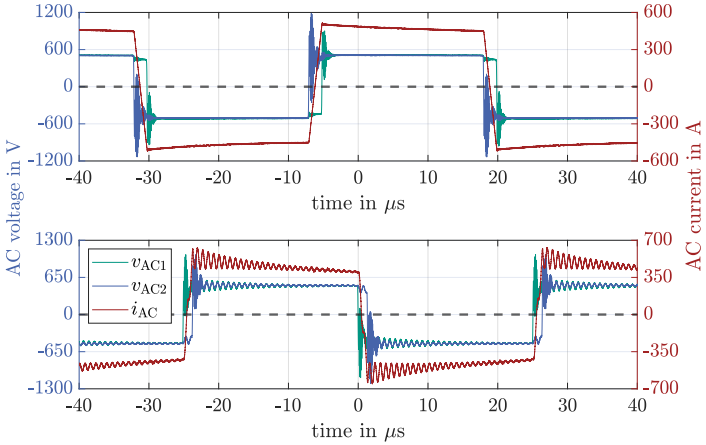


Figure 6.6: Measured AC waveforms for (top) parallel foil winding (bottom) and layered foil winding at $V_{\mathrm{DC1}} = V_{\mathrm{DC1}} = 500$ V and $P \approx 220$ kW

a switching cycle (which is true for the presented system), the losses caused by the oscillation $P_{\mathrm{v,osci}}(\varphi)$ can be calculated for each operating point of the DAB according to (6.1). This is shown in figures 6.7 (b) and 6.8 (b). The resulting efficiency, assuming no oscillations, is shown in Fig. 6.7 (c) and Fig. 6.8 (c). It

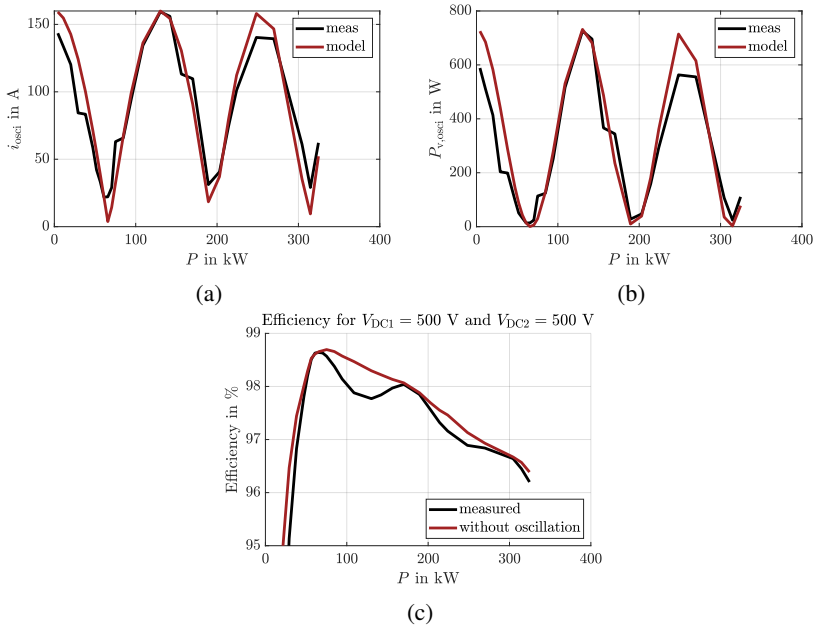


Figure 6.7: (a) Peak current of the oscillation $\hat{i}_{\text{AC,osci}}$ (b) estimated losses due to oscillations (c) estimated efficiency excluding oscillation losses

can be seen that the ripple of the efficiency curves is caused by the superposition of the HF excitation of both FB on the transformer.

$$P_{\text{v,osci}}(\varphi) = \frac{1}{f_{\text{sw}}} L_{\sigma} \hat{i}^2_{\text{AC,HF}}(\varphi) \tag{6.1}$$

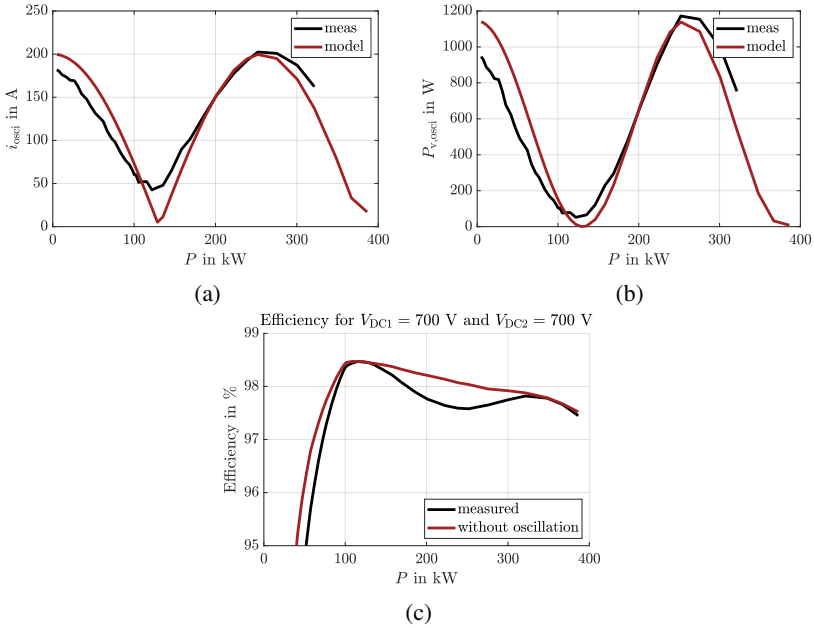


Figure 6.8: (a) Peak current of the oscillation $\hat{i}_{\mathrm{AC,osci}}$ (b) estimated losses due to oscillations (c) estimated efficiency excluding oscillation losses

6.3 Efficiency measurements

One of the defining parameters for a DC/DC converter in almost any application is the efficiency at different operating points. For the DAB, unity operation with SPS and buck/boost operation with TCM need to be investigated. To evaluate where the losses originate from, for both SPS and TCM, the calorimetric measurement setup presented in 5.2.6 is used. In addition to the analysis of different operating points, the effect of a snubber capacitance on both unity and buck/boost operation is investigated. The influence of the dead time T_{dt} and the AC inductance L_σ is also analyzed and an outlook is given on the efficiency improvement from a newer generation of MOSFET chipset.

6.3.1 Single Phase Shift

To evaluate the efficiency under SPS operation, the different DAB setups are compared at unity operation $M = 1$ with varying DC link voltages. The resulting efficiency curves are presented in Fig. 6.9. It is evident in Fig. 6.9 (d) that a higher inductance leads to an increase in both the efficiency at lower power levels and the peak efficiency itself compared to configurations with a lower inductance. However, a significant impact of the HF oscillation on the efficiency of the layered foil winding (measurements for $L_\sigma = 0.6\ \mu$H and $L_\sigma = 1.2\ \mu$H) compared to the parallel foil winding configuration (measurements for $L_\sigma = 2\ \mu$H) can be observed. Consequently, no general conclusion can be drawn regarding the influence of the inductance (or other DAB parameters) on the efficiency without separating the HF losses (cf. Section 6.3.5 and Section 6.2).
The calorimetric measurements under SPS operation shown in Fig. 6.10 are utilized to analyze the loss distribution between the FB of the DAB side and the passive components. The additional losses are comparable for both the high-inductive and low-inductive setups. However, the semiconductor losses differ in distribution between the DC1 and DC2 sides. This discrepancy is attributed to the increasing influence of the AC resistance R_{AC} on the current waveform, as introduced in Section 4.1. The DC1 side exhibits an increased switching current, resulting in the ZVS boundary being reached at lower power levels, which leads to reduced switching and overall losses at low power. However, at high power operation, the increased switching current causes elevated switching losses. In contrast, the DC2 side demonstrates inverse behavior due to the reduced switching current. At $L_\sigma = 2\ \mu$H, the influence of the AC resistance on the loss distribution is negligible.

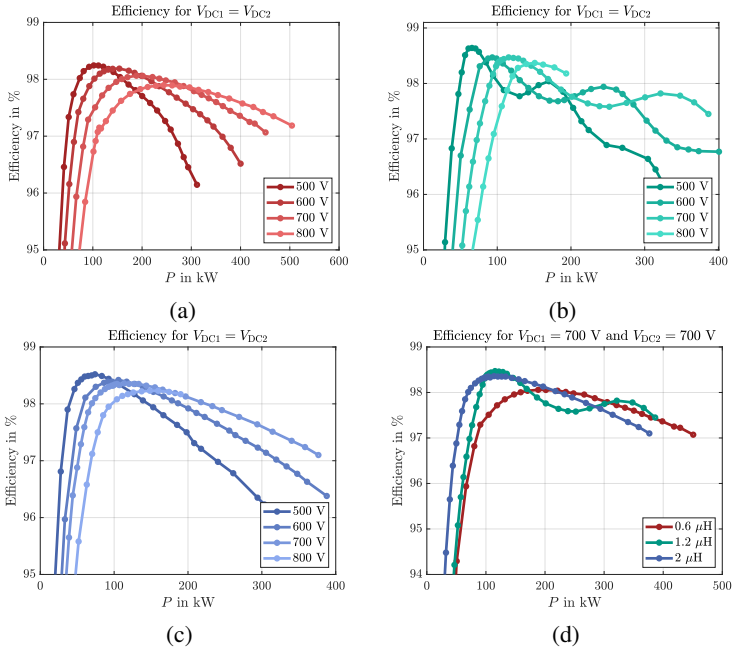


Figure 6.9: Efficiency for $M = 1$ with different voltages $V_{DC1} = V_{DC2}$ (a) layered foil winding with $L_\sigma = 0.6\,\mu$H (b) layered foil winding with $L_\sigma = 1.2\,\mu$H (c) parallel foil winding with $L_\sigma = 2\,\mu$H (d) comparison of each setup with $V_{DC1} = V_{DC2} = 700$ V

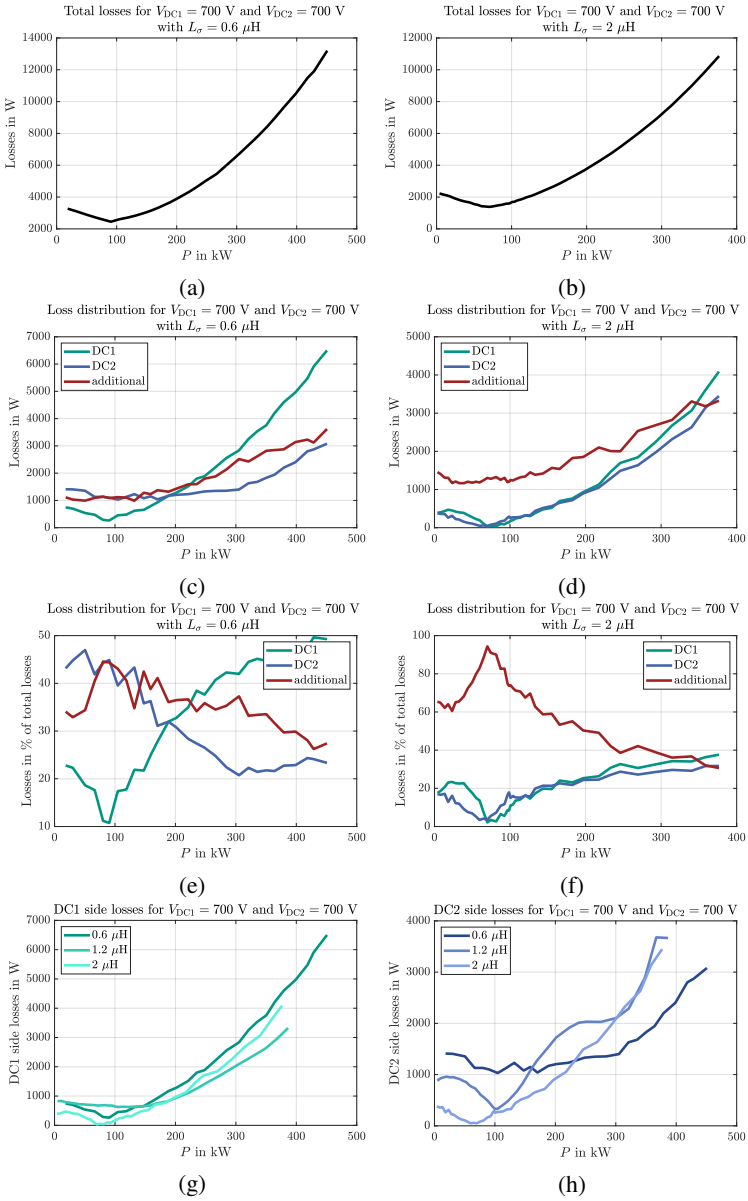


Figure 6.10: Calorimetric loss measurements for SPS with different inductances

6.3.2 Triangular Current Modulation

For buck and boost operation, the commonly applied modulation scheme is TCM, which provides improved efficiency compared to SPS. The resulting efficiencies for different transfer ratios M and inductances L_σ are shown in Fig. 6.11 and Fig. 6.12 for $L_\sigma = 1.2\ \mu$H and $L_\sigma = 2\ \mu$H, respectively. Additionally, they are compared to unity operation ($M = 1$). The higher the buck/boost ratio, the lower the efficiency, as the peak of the triangular-shaped current i_{AC} increases, leading to higher switching losses. The calorimetric loss distribution for boost operation with $V_{\mathrm{DC1}} = 600$ V and $V_{\mathrm{DC2}} = 700$ V is shown in Fig. 6.13. In contrast to SPS operation, the losses are primarily concentrated on the higher voltage side (DC2) due to the high current peak of the triangular-shaped waveform, which increases linearly with the transferred power P. This results in linearly increasing total losses with higher currents and leads to nearly constant efficiency curves (cf. Fig. 6.11 and Fig. 6.12). This behavior causes asymmetrical thermal stress on the semiconductors, which must be considered for buck and boost operation. In this case about $50-60$ % of the total losses occur on the side with the higher voltage.

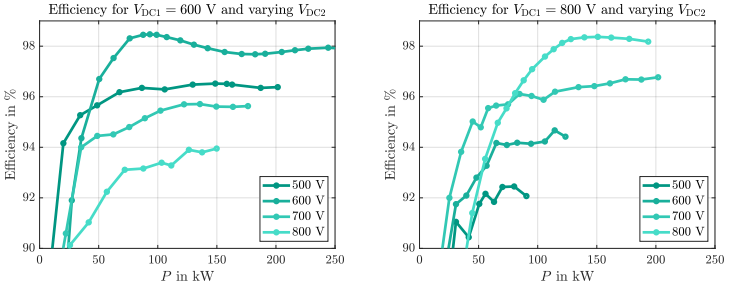


Figure 6.11: Efficiency for different transfer ratios of the DAB with SPS for unity operation and TCM with buck and boost operation for $L_\sigma = 1.2\ \mu$H

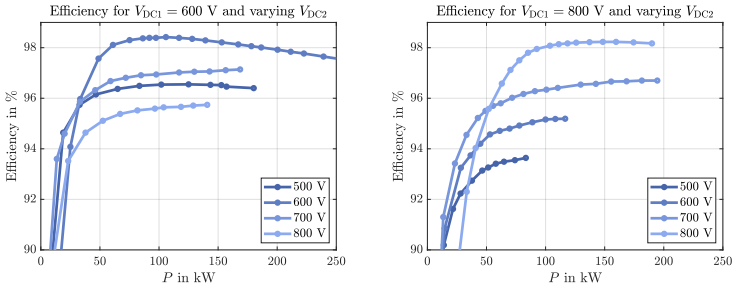


Figure 6.12: Efficiency for different transfer ratios of the DAB with SPS for unity operation and TCM with buck and boost operation for $L_\sigma = 2\ \mu$H

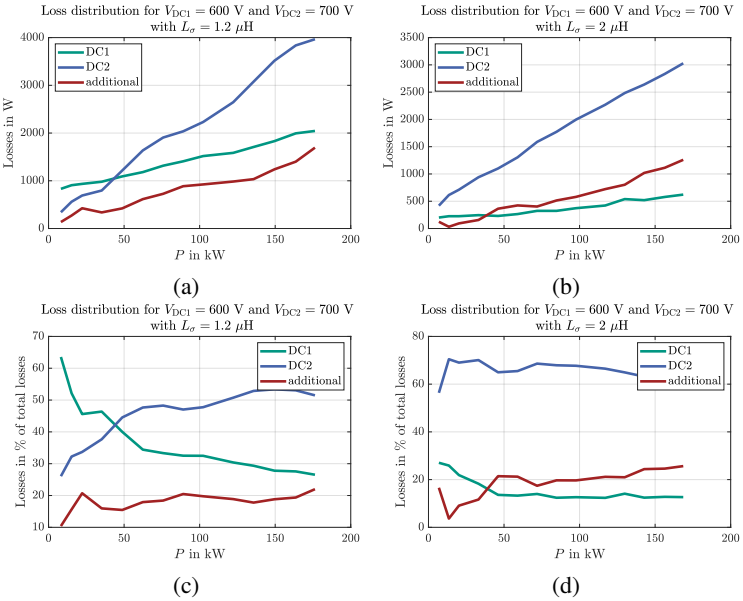


Figure 6.13: Calorimetric loss measurements for TCM with different inductances for boost operation

6.3.3 Snubber capacitance

In section 5.2.2, a snubber capacitance is proposed to increase the efficiency of the DAB by reducing the turn-off losses. However, it was demonstrated that the ZVS range is limited due to an increase in capacitance. Additionally, for buck and boost operation, the MOSFET output capacitance C_{OSS} has a non-negligible influence on efficiency due to its non-linearity and the presence of a non-zero freewheeling current. These effects are further amplified by the snubber capacitance. This can be observed in the measurements for boost operation (TCM) and unity operation (SPS) in Fig. 6.14. For SPS operation, the efficiency increases by up to approximately 0.5 % at higher power levels. However, at low power levels, ZVS is not achieved when using a snubber capacitance, leading to increased losses. Analyzing the loss distribution reveals that the increased MOSFET capacitance causes a minimum in losses at higher power levels on both the DC1 and DC2 sides. This confirms that a careful trade-off in the snubber capacitor size is crucial for optimizing efficiency. For TCM operation, losses increase across the entire operating range due to the higher freewheeling current, which results in greater switching and conduction losses. Both the DC1 and DC2 sides exhibit increased losses. In summary, the snubber significantly improves efficiency during unity operation but reduces efficiency under TCM operation. However, applying CCI may improve efficiency even when using a snubber capacitance. Hence, the decision to use a snubber depends on the specific application.

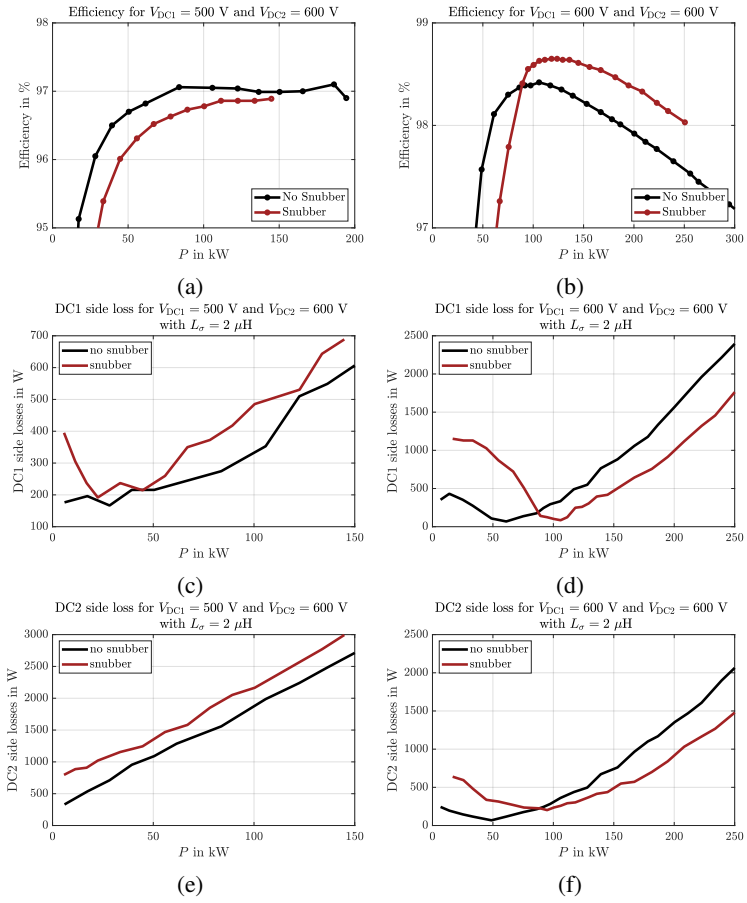


Figure 6.14: Comparison with and without a snubber capacitance: (a,b) efficiency for boost and unity operation, (c,e) losses for $V_{DC1} = 500$ V and $V_{DC2} = 600$ V, (d,f) losses for $V_{DC1} = V_{DC2} = 600$ V

6.3.4 Impact of the deadtime on the efficiency

The deadtime T_{dt} of the semiconductor switches has a direct influence on ZVS behavior of the DAB and therefore on the switching losses of the MOSFETs. However, as discussed in section 4.3.3, a sufficiently high switching current will always result in cZVS independently of the deadtime. For SPS, a significant impact of the deadtime T_{dt} at partial load is observable. However, with an increase in power P, the impact of the deadtime is diminishing and at higher loads, there is no impact anymore. This is due to the linear dependency of the switching currents on the power level. In Fig. 6.15, this impact can be observed by comparing two different deadtimes $T_{dt} = 200$ ns and $T_{dt} = 300$ ns. In case of TCM operation, however, the connection between deadtime and efficiency is not so straight forward as compared to SPS. This is due to the increasing impact of the non-linear current described in section 4.3.7. Depending on the direction of the power, the ratio of inductance L_σ and capacitance C_{OSS}, and voltage ratio of V_{DC1} and V_{DC2}, the efficiency can be increased or decreased with a change in deadtime T_{dt}. For this case, a generally valid statement is not possible within the same system, and even less so in comparison to different systems, as the influence depends on many parameters.

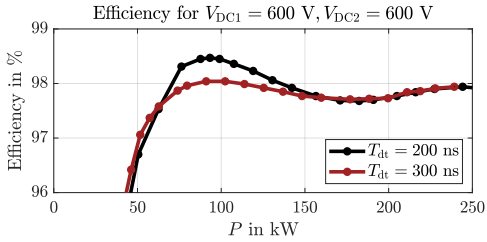


Figure 6.15: Efficiency for $T_{dt} = 200$ ns and $T_{dt} = 300$ ns with SPS and $V_{DC1} = V_{DC2} = 600$ V and $L_\sigma = 1.2\ \mu$H

6.3.5 Impact of the AC inductance

An important parameter for the efficiency of the DAB is the AC inductance L_σ, which requires a comparison of different inductances. However, two different transformer concepts are used, with the layered foil transformer exhibiting significant oscillations. The parallel foil transformer, on the other hand, does not

have these oscillations. As discussed earlier, the effect of these HF oscillations cannot be neglected in terms of efficiency. As the parallel foil transformer has a lower inductance of about $L_\sigma = 2\ \mu$H, a reduction is not possible. Therefore measurements with and without HF oscillations have to be compared. In order to isolate the losses due to HF oscillations and to compensate for the reduction in efficiency caused by them, the mathematical approach in section 6.2 is applied. After compensation of the HF oscillations, the dashed efficiency curves in Fig. 6.16 are obtained. The solid lines represent the raw measurement data. In the case of SPS, it can be seen that a lower inductance results in higher efficiency at all operating points except very low power, due to the reduced ZVS region with lower inductances. This is to be expected, as a lower L_σ results in a smaller control angle φ and therefore less circular currents. For TCM however, a lower inductance results in a lower efficiency. This is due to a higher turn-off current at the top of the triangle and therefore higher total losses when the inductance is reduced.

6.3.6 Comparison of Gen 1 and Gen 2 MOSFET Chipset

To highlight the potential for further efficiency improvements beyond the scope of the measurements carried out in this dissertation, a comparative evaluation is shown using the new generation of SiC MOSFET chipset FMF1200DXZ-24B (Gen2) [D2]. While all other measurements were performed with an older chipset FMF1200DX1-24A (Gen1) [D1], this comparison demonstrates the performance gains achievable through recent advancements in semiconductor technology. The results shown in Fig. 6.17 indicates a significant efficiency improvement across all operating points, underlining the impact of device selection on overall converter performance, as well as the potential efficiency gains with future developments in semiconductor devices.

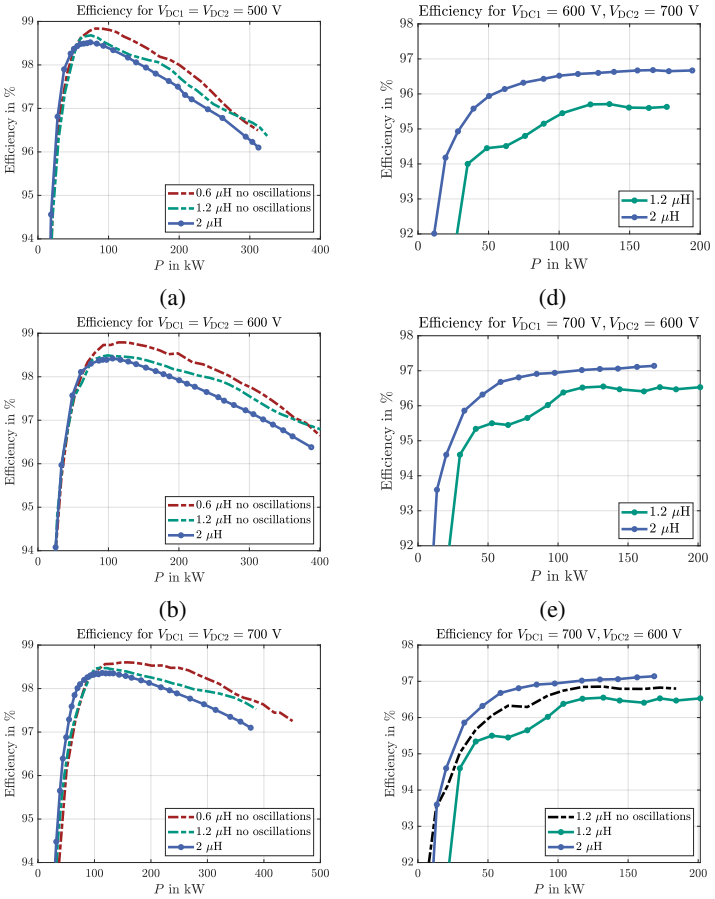


Figure 6.16: Comparison of efficiency for SPS (a-c) and TCM (d-f) for different AC inductances L with mathematical compensation of the losses caused by the AC oscillations according to section 6.2

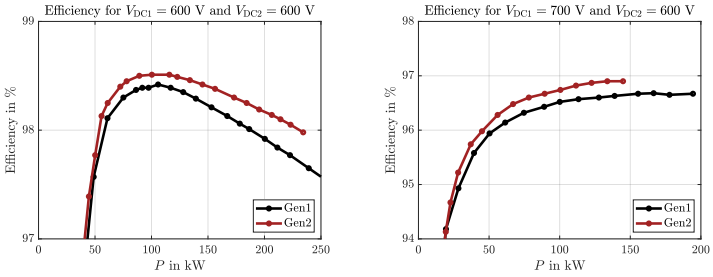


Figure 6.17: Comparison of the efficiency for Gen1 and Gen2 SiC MOSFET chipset in (a) unity operation (b) buck operation

6.3.7 Key Parameters Influencing Converter Efficiency

In this section, the key parameters influencing the converter efficiency were presented. Firstly, the AC inductance has a decisive impact on the efficiency, for SPS with unity operation a small inductance is preferred, however using TCM for buck and boost operation necessitates a larger inductance for high efficiency operation. Similar behavior can observed using a snubber capacitance. For SPS operation an increase in efficiency is achieved whereas for TCM the efficiency is reduced using a snubber. The impact of the deadtime can be significant for partial load if chosen incorrectly. This shows that the optimal design of the DAB depends on the application and the relevant operation points. Therefore, no general rule can be applied. For each application an individual optimization is required to achieve highest efficiency.

6.4 Resonant Commutation Process

Since the resonant commutation process significantly affects the behaviour and efficiency of the DAB, the model presented in section 4.3 is validated by measurements. First, the time domain waveforms of the AC current i_{AC} and the AC voltage v_{AC} are compared with the proposed model. This is followed by an analysis of the switching energies and the effect of various parameters such as the deadtime T_{dt}, which can be used to confirm the time domain modelling approach.

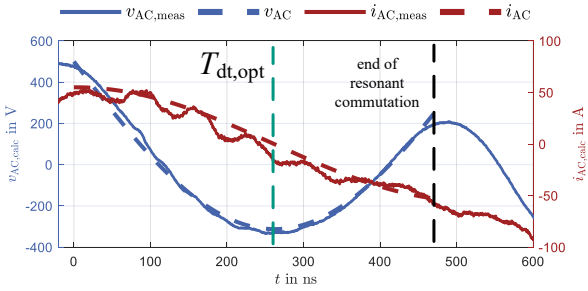
Waveform Analysis

Analyzing the time course of the current i_{AC} and the voltage v_{AC}, a distinction can be made between two main cases, namely one in which the freewheeling diodes are not clamped and one in which the diodes are clamping. The first case corresponds to iZVS-C and the second includes both cZVS and iZVS-D. The results are shown in Fig. 6.18 (a) and (b) respectively. Both the calculated and measured waveforms show a very good fit until the end of the resonant commutation process is reached and a hard switching event occurs at the end of the resonant commutation, with reduced voltage across the transistors. As this hard switching event is mainly defined by the switching characteristics of the MOSFET, it is not included in the modeling approach. Hence, the model derived in section 4.3 is validated with the help of the measurements.

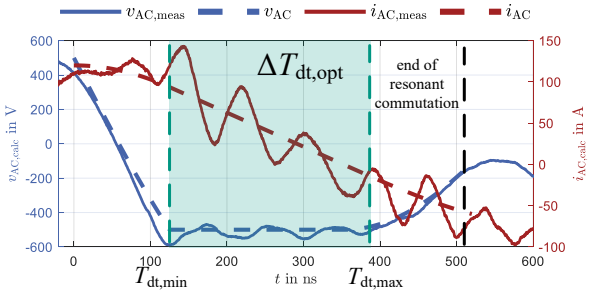
Switching Energy

To measure the ZVS energy, both the switch-on energy E_{on} and the switch-off energy E_{off} must be measured for the same switching event. This is due to the energy circulating between the output capacitors C_{OSS} of both HB switches. The resulting HB switching energy E_{HB} is given in (6.2). The measurement setup for the ZVS switching energy measurement is shown in Fig. 6.19. It is important to measure the switching behaviour in a setup as close to the converter as possible, as small deviations will result in very different switching energies. For this section, all measurements are performed with the converter introduced in chapter 5.2 with different inductances L_σ and the first generation chipset of MOSFETs. By measuring both E_{on} and E_{off} for the same switching event, double pulse testing is not required. Instead, a single pulse is used as shown in Fig. 6.20 where a FB commutation is shown. However, a HB commutation can be measured by the same procedure. First, the current i_{AC} is increased by the voltage difference of $v_{AC1} - v'_{opp}$. This is necessary to do since the very low inductance will result in high currents due to the comparatively long turn-on time t_{on} of the MOSFETs. This makes it very difficult to achieve low switching currents if the voltage difference $v_{AC1} - v'_{opp}$ is not used to increase the current but only one of these two voltages. Three different scenarios can be tested with this setup, a positive or negative opposing voltage v'_{opp} as well as an opposing voltage of zero.

$$E_{HB} = E_{on} + E_{off} = \int v_{DS,H} \cdot i_{D,H} \mathrm{d}t + \int v_{DS,L} \cdot i_{D,L} \mathrm{d}t \tag{6.2}$$



(a)



(b)

Figure 6.18: Comparison of calculated and measured waveforms for the current i_{AC} and the voltage v_{AC} for a resonant commutation process with positive opposing voltage v'_{opp}: (a) No clamping of the free wheeling diodes (iZVS-C), (b) clamping of the free wheeling diodes (iZVS-D)

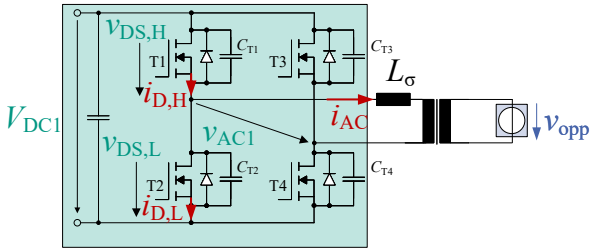


Figure 6.19: Measurement setup for ZVS switching behavior

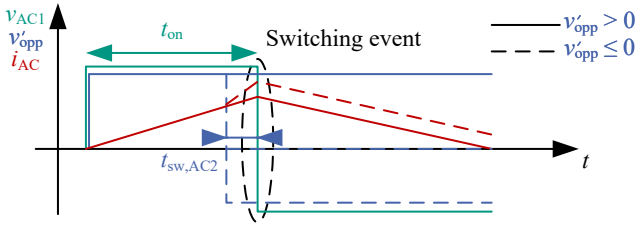


Figure 6.20: Single pulse waveform for measurement of the ZVS switching behavior for FB switching (——) switching event with positive opposing voltage v'_{opp} (– –) switching event with negative opposing voltage v'_{opp}

Figure 6.21 shows the switching energy E_{HB} for a HB as a function of the deadtime T_{dt} for $V_{DC1} = V_{DC2} = 500$ V and 700 V. As discussed in section 4.3.4, E_{HB} initially decreases as i_{sw} increases up to the ZVS limit at which the switching energy starts to increase again. Depending on the deadtime T_{dt}, the ZVS limit is reached at different currents. At the optimum deadtime (cf. section 4.3.3), the ZVS limit and thus the minimum switching energy is reached at the lowest current i_{sw}, while with increasing deviation from the optimum deadtime,

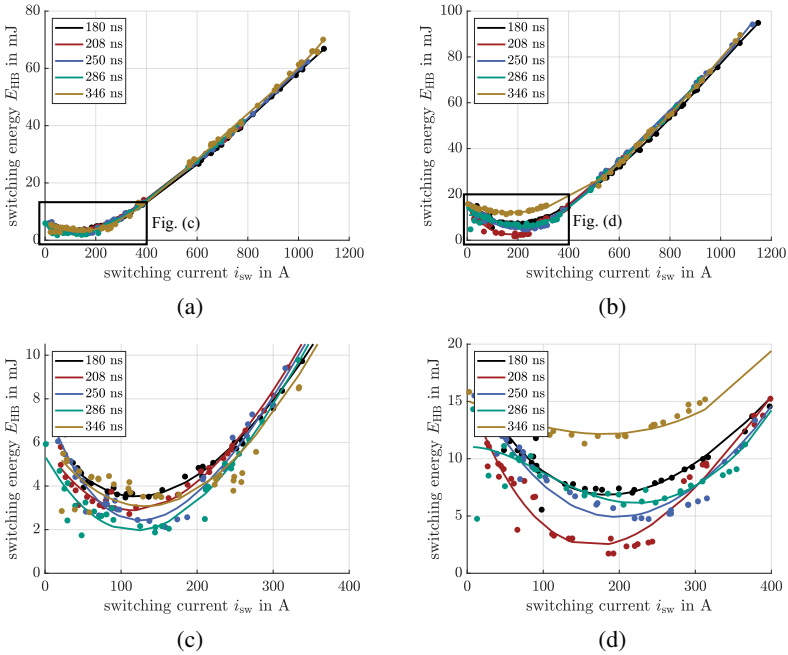


Figure 6.21: HB switching losses E_{HB} for $L_\sigma = 0.6\,\mu$H, positive opposing voltage and various deadtime T_{dt} (a,c) $V_{DC1} = V_{DC2} = 500$ V (b,d) $V_{DC1} = V_{DC2} = 700$ V

the minimum shifts to higher currents. In addition, the switching energies are higher for suboptimal deadtimes up to a factor of 2. For high switching currents $i_{sw} > 3 \cdot i_{sw,min}$, the switching energy E_{HB} is no longer dependent on T_{dt} (provided that the deviation is not off by an order of magnitude).
If a negative opposing voltage v'_{opp} is considered, the ZVS range is significantly increased. A comparison of the HB switching energy E_{HB} and the turn-on energy E_{on} for both positive and negative opposing voltages is shown in Fig. 6.22. The HB energies do not decrease as the switching current increases for a negative opposing voltage because ZVS is achieved for all measured currents. However, the HB switching energy is higher compared to a positive opposing voltage due to the increase in the AC current during the turn-off at the switching event for a negative opposing voltage. It is important to note, that for this investigations,

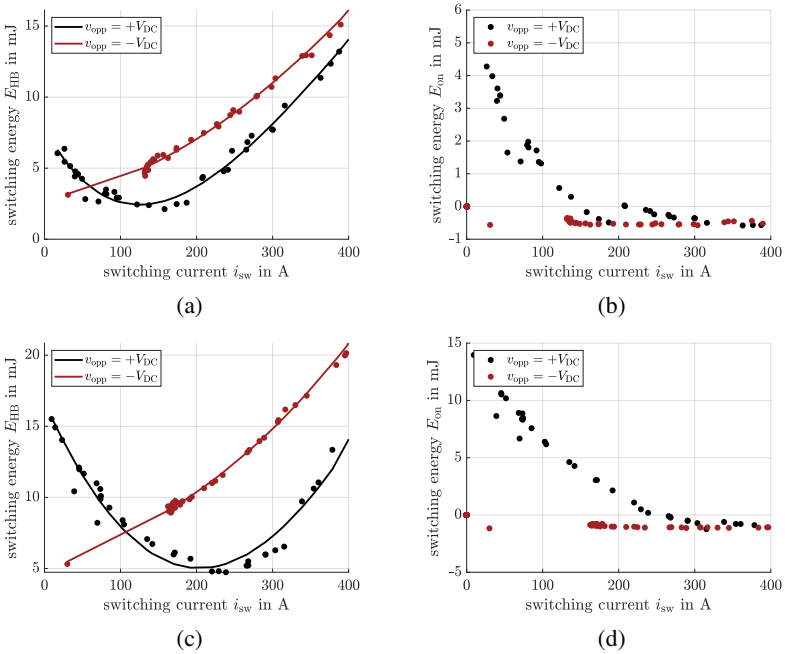


Figure 6.22: Switching energies E_{HB} and E_{on} for $L_\sigma = 0.6\,\mu$H with positive and negative opposing voltage v_{opp} (a,b) $V_{DC1} = V_{DC2} = 500$ V (c,d) $V_{DC1} = V_{DC2} = 700$ V

the switching current i_{sw} is always defined at the start of the swtiching event, i.e. at the start of the turn off, not the turn on. Looking at the turn-on losses, it can be seen that ZVS is always achieved with a negative opposing voltage, which is reflected in the permanently negative switch-on energy.

6.5 Impact of the resonant commutation

In the following section, the impact of the resonant commutation on the operation of the DAB is validated. As shown before, the impact varies depending on the modulation scheme applied to the DAB. That is why the impact on SPS is shown first followed by TCM.

The non-linear transfer characteristic of SPS and the compensation

This section focuses on validating the proposed approach for modelling non-linearity in the transfer function. The theoretical assumptions are supported by empirical data, and the transfer function is compensated using the FBL method. First, the modelling of the transfer characteristic is validated. Figure 6.23 shows the comparison of the modelled and measured transfer characteristics for unity, buck and boost operation. Here the small S and big S characteristics for unity, buck and boost operation are shown. All three cases are accurately modelled. Additionally, in Fig. 6.23 (d) the influence of different AC inductances on the measured transfer characteristic is shown. It is evident that as the inductance is reduced, the non-linearity becomes more critical and the errors increase. This results in higher non-linearity with higher rated power of the DAB and therefore cannot be neglected for high power operation. Two criteria are introduced to evaluate the improvements made by the FBL method to increase the linearity of the transfer function. The maximum error $\varepsilon_{\max}$ between the measured power P_{meas} and the set power P_{set} in (6.3) and the Root Mean Square Deviation (RMSD) value $\varepsilon_{\text{RMSD}}$ of both the measured power and the set power in (6.4) with i being the respective measurement point and n being the total amount of measurement points.

$$\varepsilon_{\max} = \max_i \left| P_{\text{meas}}(i) - P_{\text{set}}(i) \right| \tag{6.3}$$

$$\varepsilon_{\text{RMSD}} = \sqrt{\frac{\sum_{i=1}^{n} \left(P_{\text{meas}}(i) - P_{\text{set}}(i) \right)^2}{n}} \tag{6.4}$$

The resulting transfer characteristics of the DAB using SPS with and without compensation are compared in Fig. 6.24 (a), (c) and (e) for unity, buck and boost operation respectively. Linearisation is achieved in all three cases. The deviation from the ideal linear transfer characteristic is shown in Fig. 6.24(b), (d) and (f). In all three cases, the error is significantly reduced at all operating points and the steepness of the slope is also reduced, resulting in improved controller performance. The two error criteria for the performance of the FBL are shown in Fig. 6.25 (a) and (b) for different voltage transmission ratios. It can be seen that both criteria show a significant improvement using the FBL compensation method.

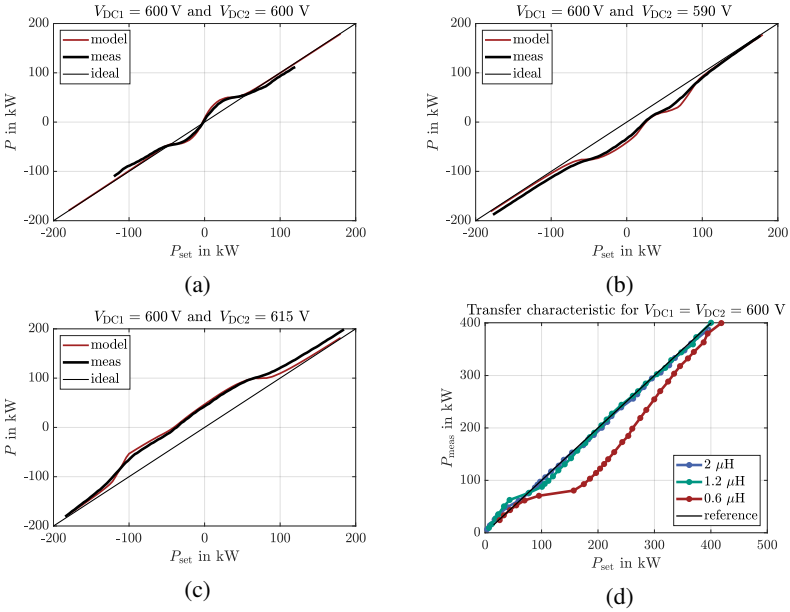


Figure 6.23: Comparison of the mathematical model and measurements of the transfer characteristic of the DAB (a) $V_{DC1} = V_{DC2} = 600$ V (b) $V_{DC1} = 600$ V and $V_{DC1} = 590$ V (c)$V_{DC1} = 600$ V and $V_{DC2} = 615$ V (d) Comparison for different AC inductances

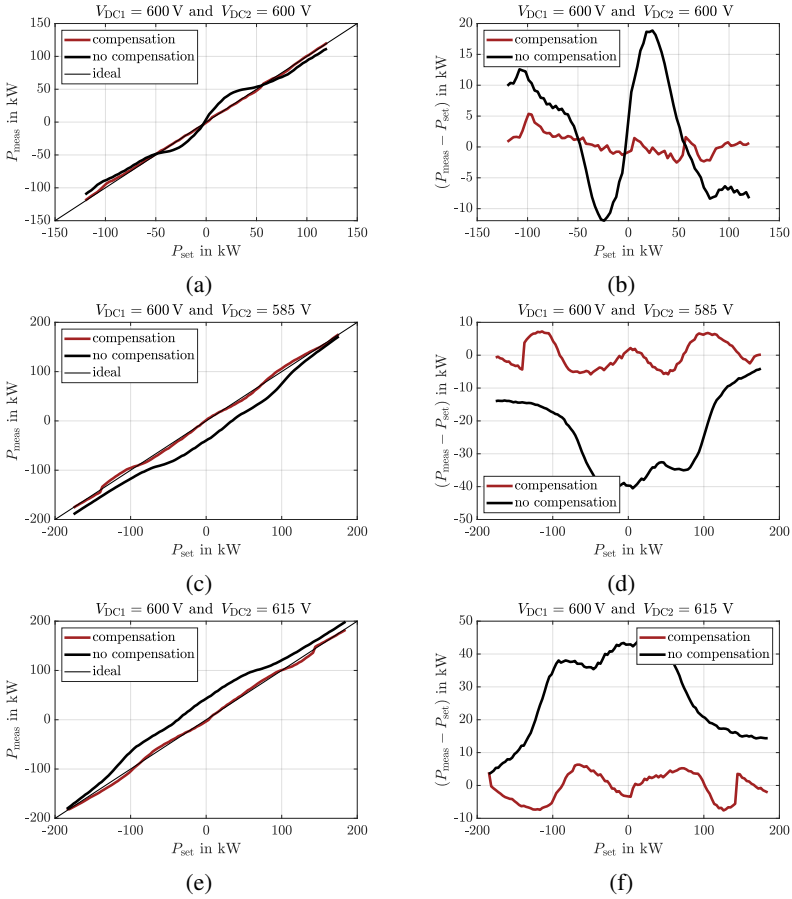
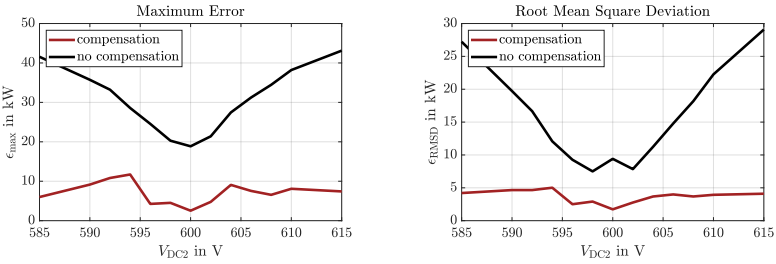


Figure 6.24: Measurement of the non-compensated and compensated transfer characteristic of the DAB and the deviation of the ideal transfer characteristic $P_{meas} - P_{set}$ (a,b) $V_{DC1} = V_{DC2} = 600$ V (c,d) $V_{DC1} = 600$ V and $V_{DC1} = 585$ V (e,f) $V_{DC1} = 600$ V and $V_{DC2} = 615$ V

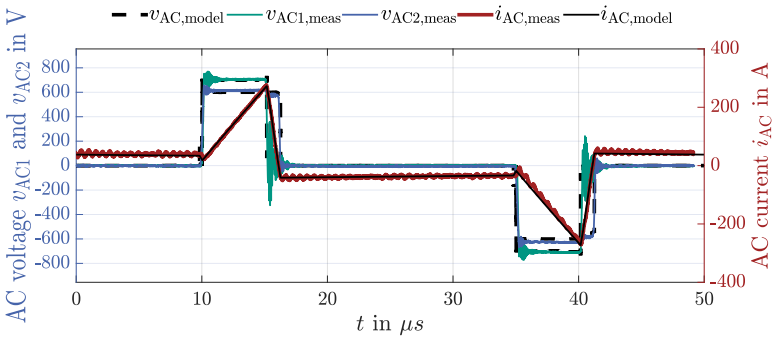


(e) (f)

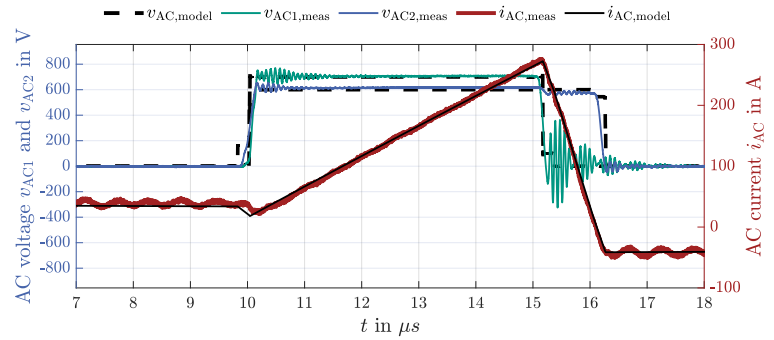
Figure 6.25: Measurement of the non-compensated and compensated transfer characteristic of the DAB (a) Maximum error using the FBL compensation method with $V_{DC1} = 600$ V (b) RMSD using the FBL compensation method with $V_{DC1} = 600$ V

Current waveform for TCM

As discussed in section 4.3.7, the transfer characteristic for TCM operation is linear and therefore does not pose a problem for controlling the DAB. However, the current waveform deviates from the expected triangular current i_{AC} due to the commutation process. The model and measurement are compared in Fig. 6.26 and Fig. 6.27 for buck and boost operation. The measurements are performed at low power rating since the impact of the commutation process is the highest at lower power. Both show a good match between measurement and model. The resulting current at the free-wheeling states as well as the triangular current shape can be predicted accurately. Hence, the model could be validated.



(a)



(b)

Figure 6.26: Comparison of calculated and measured waveform for TCM with $P \approx 20$kW

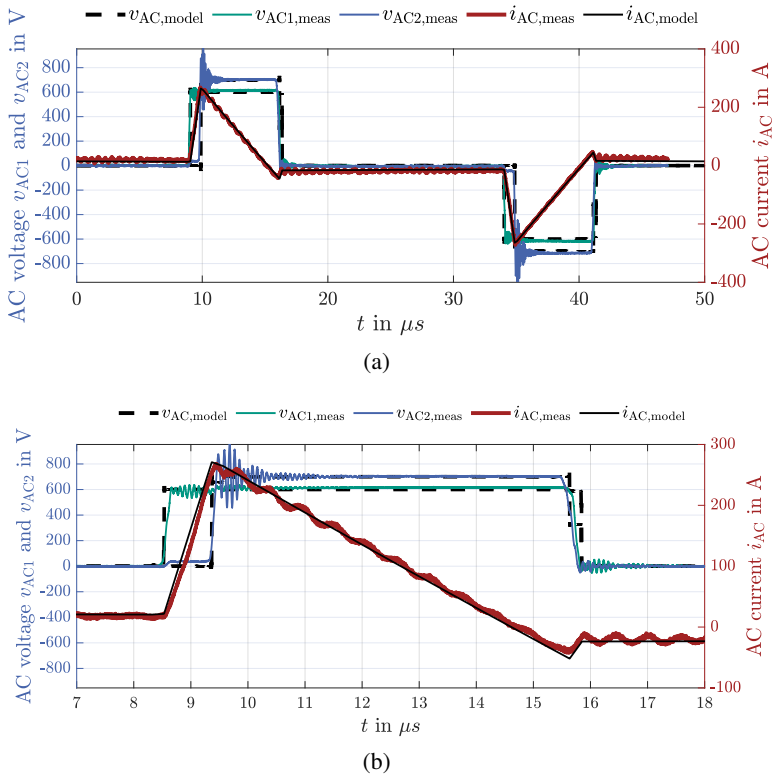
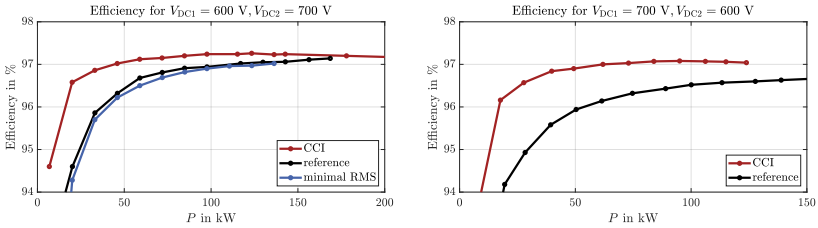


Figure 6.27: Comparison of calculated and measured waveform for TCM with $P \approx 20$kW

6.6 Circular Current Injection

In order to quantify the improvements in soft switching operation made possible by the CCI method, experimental measurements have been carried out under different operating conditions. First, the optimal switching current of i_{sw1}, i_{sw2} and i_{sw3} are measured. To do this, the switching energy for each event is measured for different switching currents. The resulting HB energy is shown in Fig. 6.29. Here the minimum of E_{on} denotes the minimum switching current to achieve cZVS. For all switching events, cZVS can be achieved if the current is sufficient, as indicated by the negative switch-on energy E_{on}. The minimum currents required to achieve cZVS are compared with the calculated values in the table 6.1. The resulting waveform using CCI with the optimum currents is shown in Fig. 6.30.



(a) (b)

Figure 6.28: Comparison of the efficiency for TCM and CCI for (a) boost and (b) buck operation

Table 6.1: Comparison of measured and calculated minimal necessary switching currents $i_{sw,min}$ for ZVS using CCI

Switching Event	Boost		Buck	
	measured	calculated	measured	calculated
$i_{sw1,min}$	80 A	88 A	83 A	91 A
$i_{sw2,min}$	48 A	50 A	51 A	50 A
$i_{sw3,min}$	61 A	66 A	63 A	66 A

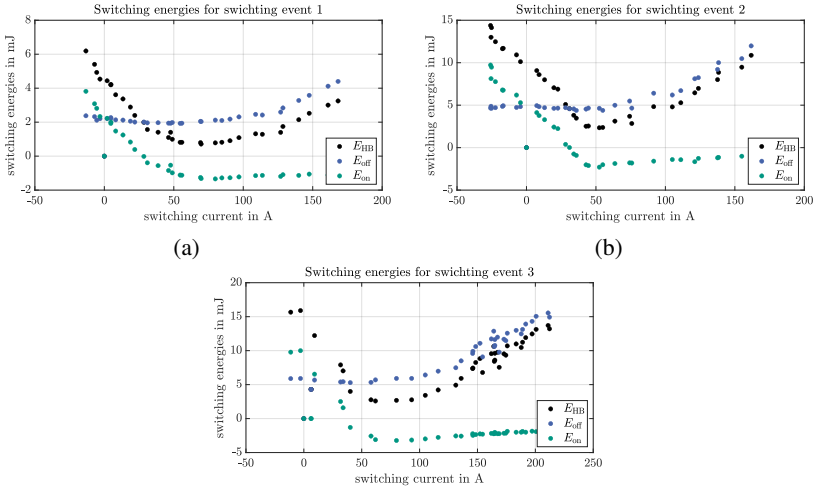


Figure 6.29: Measured HB switching energy E_{HB} for (a) switching event 1 (b) switching event 2 (c) switching event 3

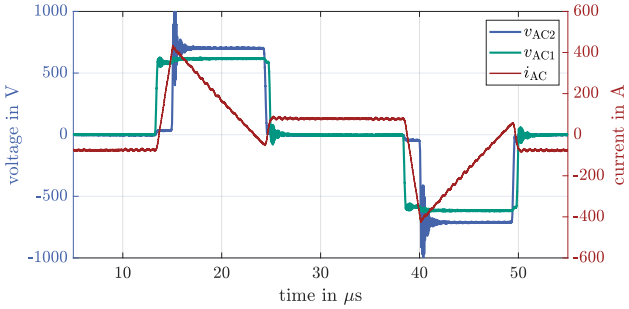
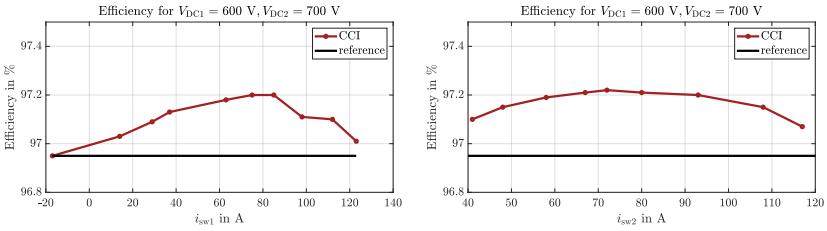


Figure 6.30: Measured waveform for 46 kW boost operation $V_{DC1} = 600\,V$ and $V_{DC2} = 700\,V$

The resulting efficiency curves for boost and buck operation using the values from table 6.1 and the setup in table 5.1 are shown in Fig. 6.28 (a) and (b) for boost and buck operation, respectively. The efficiency with CCI is increased over the whole operating range compared to the reference. Besides using CCI in order to ensure cZVS operation, it could also be applied to reduce the RMS current to a minimum by setting all switching currents to zero. This results in the lowest possible RMS current, but ZVS is no longer achieved. When using the minimum RMS waveforms, the efficiency is significantly increased compared to the ZVS optimized CCI. In the case of boost operation, the efficiency using the minimum RMS current is even slightly reduced compared to the non-ideal waveforms due to the high switching energies when switching at zero current i_{sw} (cf. Fig. 6.29). As the power level increases, the efficiency improvements are reduced due to the constant reduction in losses with CCI, which is independent of the power level. Therefore, CCI will have the highest efficiency gain at partial load with a decrease in improvements as the power level increases. However, the efficiency is improved at all operating points. To evaluate the parameter sensitivity of the CCI, the switching currents i_{sw1} and $i_{sw2} \approx i_{sw3}$ are varied independently and the efficiency is compared. Figure 6.31 shows the results. Even with a large variation in the switching currents, a significant improvement in efficiency can be achieved. This shows a high resilience to parameter variations and model inaccuracies of the CCI method.



(a) (b)

Figure 6.31: Efficiency for different switching currents for boost operation with variation of (a) i_{sw1} (b) $i_{sw2} \approx i_{sw3}$ for $P \approx 84$ kW

6.6.1 Conclusion

In summary, various measurements on a full-scale prototype with a power rating of up to 500 kW confirm the theoretical observations and models. Time domain analyses demonstrated, on the one hand, that the behavior of the DAB over the course of a switching period can be accurately reproduced. On the other hand, it was shown that the resonant commutation process can be reliably modeled using the proposed commutation model. Efficiency and calorimetric loss measurements further supported the validity of the theoretical models and predictions. An increase in efficiency was achieved through the application of CCI in both buck and boost mode. Notably, at partial load, an improvement of several percentage points was observed. Furthermore, a linearization of the DAB transfer characteristic was achieved using the proposed FBL method, significantly reducing the deviation from ideal linear behavior. In addition, the transformer model was validated, and measurements confirmed that a ”parallel foil winding” provides substantial improvements compared to a ”layered foil winding”. The previously observed oscillations were almost completely eliminated.

Chapter 7

Conclusion

In the presented work, a high-power Dual Active Bridge (DAB) converter with an input/output voltage rating between 500 V and 800 V and a power rating of 500 kW is designed, analyzed, and modeled. The results related to the DAB converter are summarized as follows:

- In chapter 2, the operating principle of the DAB was introduced, and the advantages and disadvantages of different modulation strategies were discussed. In particular, Single Phase Shift (SPS) modulation and Triangular Current Modulation (TCM) were presented and compared. It was shown that a combination of SPS and TCM can cover a wide operating range. SPS is well suited for unity transfer operating points, whereas TCM offers significant benefits in both buck and boost operation modes.
- In chapter 3, a novel DAB control scheme was introduced. The dynamic setpoint limiter enables maximum dynamic response without violating system constraints. Both voltage and power control loops were designed and implemented. It was shown that an accurate DAB model significantly improves the dynamic behavior and stability of the controller design.
- In chapter 4, a steady-state model of the DAB under non-ideal conditions was presented. It was shown that the resonant Zero Voltage Switching (ZVS) transition has a particularly strong influence on the DAB-operation. A capacitance-based time-domain (CTD) model was derived to capture the switching behavior of the DAB. Based on this model, the optimal deadtime for minimal losses, the voltage-time-area error (VTAE), and the minimum required current to achieve ZVS were calculated. It was shown that a high output

capacitance of the switches, in combination with the low AC inductance required for high power transfer, has a defining impact on the DAB. Due to the VTAE, the transfer characteristic of the DAB is highly nonlinear, which is why a compensation method based on Function-Based Linearization (FBL) was introduced. Additionally, it was shown that Zero Current Switching (ZCS) is not feasible for high-power DABs. This is caused by the low AC inductance necessary for high power, which leads to a strong current variation during the resonant commutation. As a result, an improved modulation strategy based on TCM was proposed. The resulting Circular Current Injection (CCI) method achieves ZVS for all switching events, thereby reducing losses and improving efficiency.

- The Medium Frequency Transformer (MFT) is a critical component of the DAB. Therefore, a high-frequency model of the transformer was developed and is presented in chapter 4.6. It was shown that a disadvantageous winding design can cause high-frequency oscillations. Based on these findings and the developed model, an improved winding configuration was proposed which greatly reduces the HF oscillations. The impact of these HF oscillations on the efficiency was derived and improvements due to the optimized transformer design are shown.

- In chapter 5, a full-scale DAB prototype was designed and presented. Additionally, the test bench used to validate the findings of the previous chapters was described. For accurate loss distribution analysis across DAB components, a calorimetric measurement system was implemented. This system allows for semiconductor loss measurements with an accuracy of $\pm 2\%$.

- In chapter 6, the measurement results obtained on the test bench are presented. The impact of inductance, output capacitance, and transformer characteristics on efficiency, semiconductor losses, and transfer behavior is analyzed for unity, buck and boost operation. The accuracy of both the CTD and transformer models was validated. Furthermore, the performance improvements achieved using the CCI and FBL methods were demonstrated. Using CCI can improve the efficiency for multiple percentage points at light load and is resilient to parameter deviations. An improvement for the whole operation range is possible. Additionally, it was shown that a high efficiency with unity operation and buck and boost operation is achieved with opposite optimizations. For unity operation a big snubber capacitance with a low stray inductance is necessary whereas for buck and boost operation a high stray inductance and a small snubber capacitance is preferable. This demonstrates that the optimization of

a DAB converter strongly depends on the application profile. For the prototypes a peak efficiency of $\eta \approx 98.5$ % was achieved, along with a maximum transferred power of $P \approx 500$ kW.

In summary, a full-scale prototype of a DAB was successfully implemented, meeting the requirements of the presented application scenarios. Furthermore, the challenges associated with the design and operation of a high-power DAB were identified and addressed. This enables an accurate prediction of the efficiency as well as operation of a high power DAB in an early development stage without the necessity of a hardware prototype.

Future Work

Medium Voltage A potential continuation of this work could involve adapting the results to a medium voltage prototype in order to better explore potential grid related applications. Typically, grid applications require medium voltage on one of the connection points and low voltage on the other connection point. Particular attention should be given to achieving a very high insulation voltage of the transformer for medium-voltage applications with system volages up to 36 kV. This will inherently result in a increased stray inductance which should be reduced as far as possible to achieve maximum power rating. In addition, medium-voltage semiconductors with voltage ratings from 1.7 kV up to 6.5 kV must be evaluated with respect to their suitability and the resulting switching behavior under ZVS conditions. Due to the asymmetric switching speed of MV and LV semiconductor switches, the impact of the non linearity of the DAB is further increased. Therefore the impact of such a unsymmetrical DAB should be investigated.

Extension to three phase and multiport DAB Moreover, the proposed methods should be extended, particularly in terms of modeling, to a three-phase DAB and a multi-port DAB. This enables a better comparison of the advantages and disadvantages of the respective topologies and allows for a well founded decision depending on the specific application.

Optimized Modulation Additionally, an optimization of the modulation scheme based on the developed models is possible and can improve efficiency beyond the use of SPS, TCM and CCI. In order to do so, a global converter optimization is necessary which can include all the modeling approaches while still maintain reasonable computational effort.

Online calculation It is also imaginable to change the presented linearization and modulation methods (FBL and CCI) from an offline calculated approach to an online approach which is able to adjust the operation of the DAB online in order to improve performance in terms of efficiency and control.

Glossary

Commonly Used Abbreviations

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List of Figures

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Bibliography

List of Publications

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Datasheets and Application Notes

[D1] M. Electric, *FMF1200DX1-24A*.

[D2] M. Electric, *FMF1200DXZ-24B*.

[D3] HBM, *GEN-Serie GN310B (GN311B)*.

[D4] S. GmbH, *CT High Precision Current Transducers*.

[D5] T. LeCroy, *WaveRunner 8000HD*.

[D6] Micsig, *Micsig High Voltage Differential Probes DP Series*.

[D7] PEM, *CWT Specification*.

[D8] X. Inc., *Zynq-7000 SoC Data Sheet: Overview (DS190)*.

[D9] Electronicon, *E50.N14-384NT0*.

[D10] Sensorshop24, *Einschraubtemperaturfühler mit G1/2" Gewinde*.

[D11] Sensorshop24, *Norm- bzw. Hutschienen-Messumformer für PT1000 und PT100 (0-10V/4-20mA)*.

[D12] Bio-Tech, *DFM-Ms-AN*.

[D13] Bio-Tech, *DFM-POM-AN*.