A Coordinated DC Protection Strategy Based on Prioritized DC-link Capacitor Fault Interruption

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***Abstract*— Protection in DC networks has long been a complex challenge, often cited as a major barrier to their widespread adoption. The presence of large DC-link capacitors and the replacement of traditional transformers with power electronic converters result in fault current rise rates that are tens to hundreds of thousands of times higher than those in AC grids. Despite this, conventional DC protection strategies are largely borrowed from the traditional AC protection mindset. In DC networks, the inclusion of large link capacitors renders the series insertion of circuit breakers, similar to AC network practices, suboptimal, as breakers must interrupt fault currents injected from multiple sources with varying escalation time constants. Existing DC circuit breaker technologies also inherently struggle to simultaneously achieve high interruption speed, minimal size, and low cost. Consequently, relying on a single circuit breaker does not necessarily offer an optimal solution in terms of speed, cost, or compactness. This paper investigates fault propagation mechanisms in common power electronic converter topologies and proposes a novel protection strategy based on the coordinated use of multiple circuit breakers with varying interruption speeds. The proposed approaches are also validated through comprehensive simulations.**

Keywords—circuit breaker, coordination, DC protection, fault current, hybrid, solid-state

I. Introduction

When the "War of Currents" concluded in favor of AC networks at the end of the 19th century, leading to the global dominance of AC electricity distribution, few could have predicted that, about a century and a half later, the idea of replacing AC networks with DC networks would resurface [1]. During the War of Currents, Edison designed his energy distribution system around the development of multiple small DC grids in each city, with a central generator connected radially to consumers. However, due to the voltage limitations of DC networks, transmitting large amounts of power resulted in significant voltage drops along the line, leading to lower voltage levels for consumers located farther from the generator.

Today, clean DC energy sources, such as photovoltaic units, have become widespread in urban areas and are now much closer to end users. By the end of 2024, over 37% of Germany's total installed electricity generation capacity came from solar power, with slightly more than 67% of that capacity installed on rooftops [2]. A significant portion of renewable energy sources, storage systems, and electrical loads are also inherently DC, and connecting them to the AC grid requires an additional, inefficient energy conversion step. These factors have led many researchers to reconsider the suitability of Edison's early DC microgrid model for meeting the growing energy demand with renewable sources.

However, the widespread adoption of DC microgrids is currently hindered by several critical challenges, including their technological immaturity, and the inherent complexity of DC protection systems [3]. Unlike traditional AC networks, which have undergone extensive development over more than a century and are governed by well-established standards, DC networks remain in an early stage of evolution. A particularly significant obstacle lies in the protection mechanisms of DC microgrids. The presence of large DC-link capacitors and the absence of natural current zero-crossing points result in fault currents that escalate extremely rapidly, reaching several tens of per unit within microseconds, which can be up to five orders of magnitude faster than in AC systems. Consequently, fault detection and isolation speed become critically important; delays in detection necessitate the interruption of substantially higher fault currents, thereby increasing the complexity and cost of fault isolation strategies [4].

To address fault isolation challenges in DC power systems, various technologies have been developed, each offering distinct advantages and limitations. While fuses are applicable in certain niche scenarios, the energy stored in DC-link capacitors is typically insufficient to melt the fuse element effectively. Consequently, electrothermal and electromagnetic mechanisms often fail to deliver the required response speed and reliability for high di/dt fault conditions.

Mechanical Circuit Breakers (MCBs), despite their low on-state voltage drop and minimal conduction losses, are generally unsuitable for fast fault interruption. Although they are often equipped with arc chambers and benefit from the absence of cooling systems, resulting in a more compact design, their fault clearing time typically spans several tens of milliseconds. This delay renders them impractical for high di/dt fault scenarios.

An alternative approach involves solid-state circuit breakers (SSCBs), which leverage semiconductor technologies and can be implemented in various topologies [5]-[6]. These breakers offer reaction times as low as one microsecond, making them the fastest among available options. However, their significant on-state voltage drops and high conduction losses necessitate extensive cooling systems, substantially increasing the overall system size. Moreover, the limited surge current handling capability of semiconductors requires either oversizing the semiconductor's conduction capability or integrating bulky fault current limiters to manage di/dt rates, both of which adversely affect the final product's weight and volume.

A third category comprises Hybrid Circuit Breakers (HCBs), which mostly combine a semiconductor-based commutation branch with a mechanical main breaker [7]. This configuration enables artificial current zeroing in the main

branch, allowing sufficient time for fault clearance. From a performance standpoint, hybrid breakers offer a balanced compromise: they exhibit low conduction losses and on-state voltage drops, while achieving fault interruption times in the range of several hundred microseconds. This makes them significantly faster, at least by an order of magnitude, than purely mechanical breakers.

As is evident, various technologies have been developed for DC circuit breakers, each offering a distinct range of performance characteristics. A fundamental challenge in this domain is the trade-off between key parameters: no single technology currently achieves optimal performance in both on-state voltage and conduction losses, as well as in interruption speed. Enhancing one of these attributes often comes at the expense of another. Consequently, the prevailing approach is to select the circuit breaker type based on the specific application requirements. In scenarios where the rate of current change (di/dt) and the source current supply capacity are limited, mechanical circuit breakers and fuses remain viable options. However, in high di/dt applications, solid-state circuit breakers are increasingly favored despite their relatively higher conduction losses, due to their superior response speed.

This paper investigates the feasibility of using a dual-breaker configuration, comprising two circuit breakers with different reaction times, instead of a single breaker. The goal is to achieve improved performance in both fault interruption time and conduction losses. Unlike AC faults, DC faults exhibit multiple stages of evolution, each characterized by distinct time constants and originating from at least two sources: the DC power supply and the DC link capacitors, which differ in their time constants and fault current contribution capacities.

The proposed concept involves deploying a fast-acting circuit breaker to interrupt the initial stage of fault evolution, while a slower breaker with lower conduction losses is placed in the main power path to disconnect the primary source during the final fault stage. This staged interruption strategy aims to optimize overall system performance by leveraging the strengths of each breaker type.

The remainder of this paper is structured as follows. First, an in-depth analysis is presented of pole-to-pole short-circuit faults occurring at the output of a diode-based three-phase rectifier and DC-DC converters, highlighting their fault characteristics and implications for protection strategies. Next, a novel fault interruption approach is proposed, specifically targeting the DC-link capacitors in DC systems, which leverages a staged response mechanism to optimize fault isolation. This is followed by a comprehensive evaluation of the proposed configuration through simulation studies, demonstrating its effectiveness under fault occasions. Finally, the paper concludes by summarizing the key findings and suggesting avenues for future research aimed at enhancing fault management in DC power systems.

II. Pole-to-Pole Short-Circuit Fault Analysis

The maximum allowable reaction time of protective devices in power systems is governed by the safety limits of both equipment and personnel. Specifically, fault isolation time must not exceed the duration that system components can tolerate fault conditions. Modern energy networks are increasingly integrating power electronic converters, which, unlike traditional grid elements, have inherently lower fault current

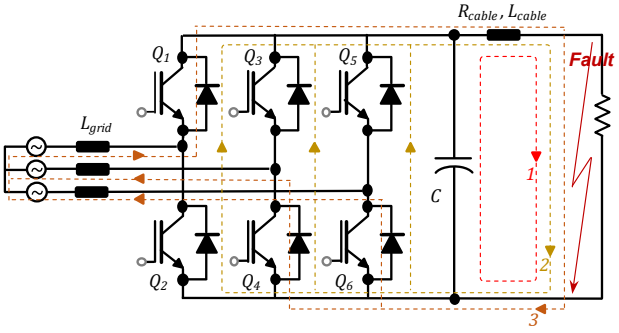

Fig. 1. Short-circuit fault path through 3-phase front-end AC-DC converter.

withstand capabilities. This combination of widespread adoption and limited fault tolerance makes these converters a critical bottleneck in future protection schemes, where the speed of protective response must align with their vulnerability. This section investigates the impact of severe fault scenarios, particularly pole-to-pole short-circuit faults, on three converter topologies: three-phase rectifiers (used at AC-DC interfaces), DC-DC converters in boost mode (for connecting batteries and PV cells to the grid), and DC-DC buck converters (commonly used in charging systems). DC-DC converters are also expected to assume transformer-like roles in future DC microgrids, further emphasizing the importance of their fault response characteristics.

A. Three-phase AC-DC Front-End Converter

Fig. 1 illustrates the short-circuit current path in an AC-DC Front-End Converter. For proper operation of this active bidirectional converter, the DC-link voltage (V_{DC}) must exceed the peak value of the line-to-line AC voltage (V_{LL}). If this voltage condition is violated, as occurs during a pole-to-pole fault, the converter transitions into an uncontrollable three-phase diode rectifier mode. In this figure, R_{grid} and L_{grid} represent the equivalent resistance and inductance of the AC grid, while R_{cable} and L_{cable} denote the resistance and inductance of the cable connecting the converter terminals to the fault location. The fault current evolves through three distinct stages [8]:

1) DC-link capacitor discharge stage

The initial stage following a pole-to-pole fault is dominated by the discharge of the DC-link filter capacitor. This stage is characterized by a rapid rise in fault current and a simultaneous decline in the DC-bus voltage. As the capacitor discharges, the energy released is partially absorbed by the cable inductance.

At this stage, the DC-link capacitor, cable inductance, and fault resistance form an RLC circuit, as illustrated in Fig. 1 (Path 1). Consequently, the fault current during this phase can be described by the characteristic response of an RLC circuit.

$$i_f(t) = \frac{V_c(0)}{L_{cable}(s_2 - s_1)}[e^{-s_1 t} - e^{-s_1 t}] + \frac{I_f(0)}{(s_2 - s_1)}[-s_1 e^{-s_1 t} + s_2 e^{-s_1 t}] \quad (1)$$

Here, $V_c(0)$ and $I_f(0)$ denote the initial voltage across the DC-link capacitor and the initial current through the cable inductance at the moment the fault occurs, respectively.

The roots of the characteristic equation are given by:

$$\alpha = \sqrt{\alpha^2 - {\omega_0}^2} \tag{2}$$

where the damping factor and resonance frequency are:

$$\alpha = \frac{R_{f,1}}{2L_{cable}} \tag{3}$$

$$\omega_0 = \frac{1}{\sqrt{L_{cable}C}} \tag{4}$$

where $R_{f,1}$ represents the total equivalent resistance of the circuit, comprising the cable resistance (R_{cable}), the equivalent series resistance (ESR) of the DC-link capacitor, and the fault resistance. An increase in cable inductance leads to a reduction in the peak value of the fault current. However, this also results in diminished damping and a slower transient response. Consequently, faults occurring in close proximity to the converter terminals exhibit higher current peaks and a significantly faster rate of rise.

Depending on the relative magnitudes of α^2 and ${\omega_0}^2$, the fault current response can be classified as overdamped ($\alpha^2 > {\omega_0}^2$), critically damped ($\alpha^2 = {\omega_0}^2$), or underdamped ($\alpha^2 < {\omega_0}^2$). Oscillatory behavior in both the DC-link voltage and current waveforms is observed exclusively under underdamped fault responses. In such cases, the freewheeling diodes feeding stage is activated accordingly. In contrast, for overdamped responses, the third stage is triggered directly following the initial capacitor discharge event.

2) freewheeling diodes conduction stage

During the initial stage, the DC-link capacitor fully discharges through the cable, transferring its stored energy into the cable inductance. This inductive energy is subsequently released in the following time intervals. Given the potentially high inductive energy and minimal dissipative losses in the system, the cable current commutates to the converter's freewheeling diodes, as illustrated in Fig. 1 (Path 2). If this stage persists for an extended duration, the diodes may be subjected to excessive stress, increasing the risk of damage. Therefore, it is often necessary to detect and isolate the fault during the first stage to prevent the onset of this potentially harmful condition. The fault current at this stage can be calculated as:

$$i_f(t) = I_0^{'} e^{-\left(\frac{R_{f,2}}{L_{cable}}\right)t} \tag{5}$$

Here, $I_0^{'}$ is the value of the fault current at the end of stage one. $R_{f,2}$ also represents the total equivalent resistance of the circuit, comprising R_{cable}, fault resistance, and the equivalent on-state resistance of three diode branches.

3) source current feeding stage

The final stage of fault progression, commonly referred to as grid-side or source current feeding, occurs when the fault remains undetected and uncleared during the preceding two stages. At this point, the fault current is directly influenced by the converter topology. Certain converter topologies possess fault current limiting capabilities and can isolate the output from the input. Conversely, topologies such as the six-switch AC-DC converter lack this functionality. In such cases, the converter behaves as an uncontrolled diode-bridge rectifier, with fault current supplied by the AC grid via the freewheeling diodes, as illustrated in Fig. 1 (Path 3).

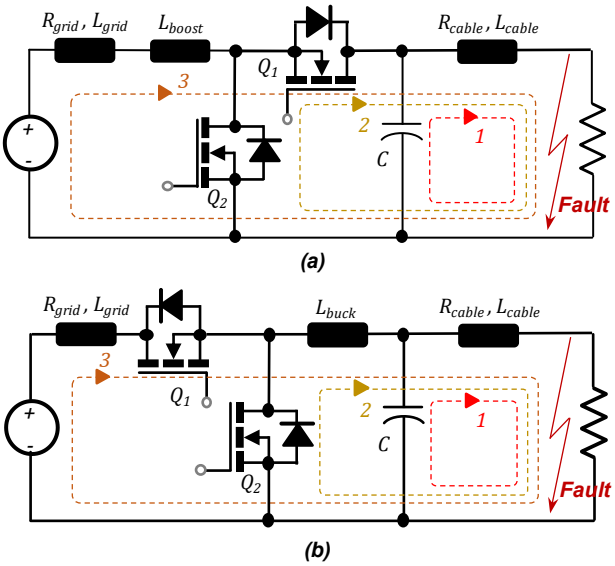

Fig. 2. Short-circuit fault path through DC-DC converter in a) boost, and b) buck operating modes.

During this stage, the fault reaches a steady-state condition, where the DC-bus voltage is determined by the product of the fault current and the fault resistance, which is typically low. The resulting fault circuit can be modeled as a first-order RL transient. A key distinction between this stage and the preceding ones lies in the significantly longer time constant, primarily due to the inclusion of the AC grid inductance (L_{grid}) in the fault current path. This inductance can be substantial, which can considerably limit the rate of rise of the fault current during this stage.

B. DC-DC Converter in Boost Mode

DC-DC converters operating in boost or buck mode exhibit a fault evolution process that closely resembles the three-stage behavior observed in front-end AC-DC converters. The first stage, involving the discharge of the DC-link capacitor, follows the same dynamics previously analyzed in Equations (1) through (4). In boost mode, the second stage of fault evolution also mirrors that of the front-end AC-DC converter, where the fault current path is established through the forward-biased anti-parallel diodes of switches Q_1 and Q_2 (Fig. 2 (a) Path 2), and can be calculated using Equation (5).

However, the third stage, where the fault current is supplied directly from the DC source (Fig. 2 (a) Path 3), presents distinct characteristics. Specifically, the presence of a large boost inductor (L_{boost}) in the fault path significantly increases the time constant of this stage. Additionally, typical DC sources such as photovoltaic cells have a limited short-circuit current feeding capability, which prevents the fault current from rising dramatically. Similarly, batteries exhibit comparable behavior due to their internal resistance, which causes a substantial voltage drop under high current conditions, thereby limiting further current increase. Consequently, the fault current growth in this stage is expected to be considerably slower.

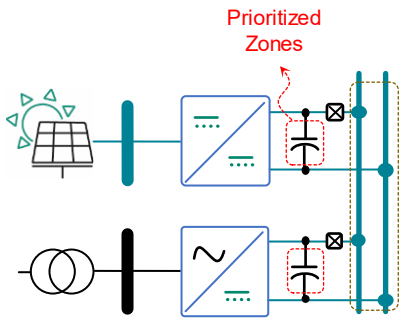

Fig. 3. Definition of prioritized protection zones for DC-link capacitors.

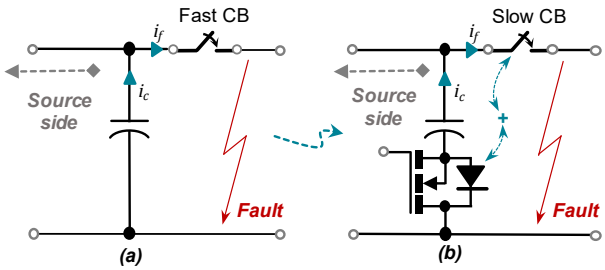

Fig. 4. Double circuit breakers methodology: a) Conventional single breaker protection b) Dual-breaker setup featuring a fast capacitor breaker.

C. DC-DC Converter in Buck Mode

In DC-DC converters operating in buck mode, the second stage of fault evolution, where the fault current flows through the buck inductor and the anti-parallel diode of switch Q_2 (Fig. 2 (b) Path 2), differs from the behavior observed in the previously discussed converters. Due to the presence of a large buck inductor in the fault path, this stage begins only after the current in the line inductor and the buck inductor equalizes. The inductor also increases the time constant of fault current growth, resulting in a slower response during this stage.

A more significant distinction arises in the third stage of fault evolution. Unlike front-end AC-DC converters and boost-mode DC-DC converters, the presence of switch Q_1 in buck-mode converters enables the system to independently interrupt the fault current during this final stage [9].

III. Prioritized DC-link Capacitor Protection

Currently, several collaborative groups such as the Open DC Alliance (ODCA) and Current/OS, comprising major companies and academic institutions, are actively working to define the development roadmap and establish standards for DC power networks. One of the key contributions from Current/OS is the proposal of a zonal protection plan tailored for DC networks.

As the number of distributed energy resources and bidirectional systems increases, the complexity of protection planning also escalates. To address this challenge, Current/OS has introduced a zone-based classification approach, grouping circuits according to fault impact severity and assigning specific protection requirements to each group. Five primary zones, numbered 0 through 4, have been defined. For instance, Zone 0 includes the outputs of voltage sources without any protective devices, where faults can lead to severe and irreversible damage. Zone 1 employs basic protection using fuses or slow breakers, while Zones 3 and 4 utilize high-speed solid-state circuit breakers to minimize fault impact [10].

A critical issue in this zonal protection strategy is the trade-off between protection level and system cost and efficiency. Higher protection levels require more expensive fault interruption devices and introduce additional power losses. Therefore, developing methods that enhance protection levels with minimal cost and loss penalties is essential.

The core idea of this paper is the introduction of DC link capacitor branches as a new protection zone within DC networks (Fig. 3). As discussed earlier, the initial stage of a fault in DC systems typically involves the rapid discharge of link capacitors, characterized by an extremely short time constant. Currently, two main approaches are used to interrupt faults at this stage. The first method involves slowing the fault current rise by adding reactors in the power path. However, since these reactors must handle the full nominal current of the network, their physical size becomes significantly large. The second method employs solid-state circuit breakers in the power path to reduce fault reaction time. Yet, placing semiconductor devices directly in the power path introduces substantial power losses and necessitates large cooling systems.

Nevertheless, replacing each circuit breaker with two others having distinct reaction times may offer a solution to the problem. Although the discharge rate of capacitors is very high, their current typically represents only a small fraction of the main power path current. Therefore, a fast circuit breaker with relatively high losses can be employed to interrupt the capacitor current in the initial stage. This breaker, which should ideally be a solid-state type with the shortest possible reaction time, is placed in series with the capacitor branch. Meanwhile, the fault current in the second and third stages evolves with longer time constants, allowing the use of a slower circuit breaker with significantly lower losses to clear the fault current in these stages along the main power path. Thus, although two circuit breakers are used instead of one, the specifications of each breaker are closely matched to its specific function, resulting in reduced losses and a smaller overall system size.

The general schematic of the proposed method is presented in Fig. 4. The semiconductor device used to interrupt the capacitor fault current may consist of a single MOSFET with an anti-parallel diode, as the switch is required to block current flow in only one direction during capacitor discharge. The advantages and potential drawbacks of separating the main circuit breaker from the capacitor circuit breaker can be summarized as follows.

- By adding a dedicated capacitor circuit breaker, the capacitor current can be directly measured and used as a fault detection indicator. Under normal conditions, the capacitor conducts AC ripple current, whereas during a fault, the current increases sharply in a single direction. This behavior suggests that fault-induced variations in capacitor current may be more accurately distinguishable than those in the main line current.
- The DESAT protection of the semiconductor device in series with the capacitor can be directly utilized to interrupt the capacitor discharge current. This enables interruption times of even less than one microsecond.
- On the other hand, care must be taken to ensure that the addition of a series switch does not impair the capacitor's performance during transients that require the injection of large currents.

IV. Simulation Results

In this section, the performance of the proposed fault interruption model is evaluated through simulation, focusing on clearing faults that occur on the output side of front-end AC-DC converters and DC-DC converters. To this end, three converter topologies, as specified in Table I, are simulated using MATLAB. In all three scenarios, a solid pole-to-pole short-circuit fault is intentionally triggered on the output side of the converters to assess the effectiveness of the proposed protection topology.

Fault detection in each case is achieved by monitoring the capacitor current and applying a threshold-based detection mechanism. The threshold is deliberately set high enough to account for typical fault detection delays. Additionally, the delay in the capacitor breaker's operation is modeled using a realistic driver profile. The main power path switch is configured to open with a delay of 1 millisecond, up to 1000 times slower than the capacitor breaker. The following simulation results assess the feasibility of employing two switches with significantly different response times and evaluate their combined effectiveness in fault clearing.

A. Three-phase Diode-bridge Rectifier

The simulations presented in this section are conducted on a three-phase diode bridge rectifier connected to a low-voltage residential grid. In such grids, the short-circuit power is limited, and the impedance-to-resistance ratio is relatively low. Instead of employing a front-end AC-DC converter, a three-phase diode bridge rectifier is modeled. This choice is justified by the behavior observed during fault conditions: when the DC-link voltage drops below the peak line voltage of the AC side, only the anti-parallel diodes remain capable of conducting current, as previously discussed. Fig. 5 illustrates the performance of the proposed model in interrupting a short-circuit fault. Two scenarios are considered:

TABLE I. SPECIFICATIONS OF THE SIMULATED TOPOLOGIES AND FAULT

Specification	Value
Three-phase Diode-bridge Rectifier	
Input line voltage	380 V
Output power	10 kW
Output capacitors capacitance	2000 µF
Snubber (clamping voltage, voltage @ 1mA)	Varistor -775 V, 450 V
Grid short-circuit power (SCP)	100 kVA
Grid X/R ratio	3
Fault specification	500 µH -0.01 Ω
Boost Topology	
Input voltage	220 V
Output voltage -power	380 V -2 kW
Switching Frequency	20 kHz
Boost inductor inductance -resistance	1.9 mH -10 mΩ
Output capacitors capacitance	66 µF
Snubber (clamping voltage, voltage @ 1mA)	Varistor -775 V, 450 V
Reaction delay of converter switches	10 µs
Fault inductance -resistance	100 µH -0.01 Ω
Buck Topology	
Input voltage	380 V
Output voltage -power	220 V -1 kW
Switching Frequency	100 kHz
Buck inductor inductance -resistance	1.02 mH -7 mΩ
Output capacitors capacitance	47 µF
Snubber (clamping voltage, voltage @ 1mA)	Varistor -775 V, 450 V
Reaction delay of converter switches	10 µs
Fault inductance -resistance	100 µH -0.1 Ω

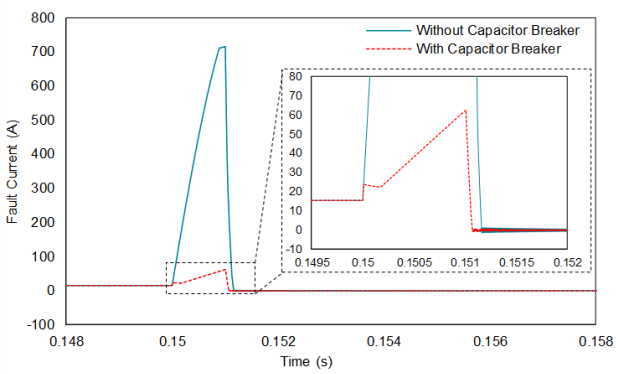

Fig. 5. Fault clearing performance of the proposed methodology for 3-phase diode-bridge rectifiers.

- **Scenario 1**: No series MOSFET is present with the capacitor. Protection is provided solely by a single switch in series with the main power path, which operates with a delay of 1 ms.
- **Scenario 2**: A series breaker is added alongside the capacitor. This switch, in conjunction with the slower main breaker, jointly handles fault protection.

The fault is initiated at t = 0.15 s. As shown, in Scenario 1, without the capacitor breaker, the fault current surges to approximately 50 per unit, which would likely destroy all anti-parallel diodes in a real system. However, in Scenario 2, the addition of the capacitor breaker enables rapid interruption of the capacitor discharge current, effectively preventing the extreme rise in fault current (represented by the red dashed line). The figure also highlights the distinct time constants associated with different fault stages, confirming the effectiveness of using two circuit breakers with varying response times for enhanced protection.

B. DC-DC Converter in Boost Mode

Fig. 6 illustrates the fault current at the output of a boost converter under scenarios similar to those previously discussed. The basic boost topology lacks a controllable semiconductor device in the main path. Consequently, in the absence of an output-side breaker, the fault current originating from the source continues to rise steadily. However, the presence of a large boost inductor in the power path can limit the rate of current increase, as is evident in Fig. 6.

It is assumed that the main semiconductor switch of the converter opens 10 microseconds after fault detection. As shown in the figure, without a capacitor-side breaker, the fault

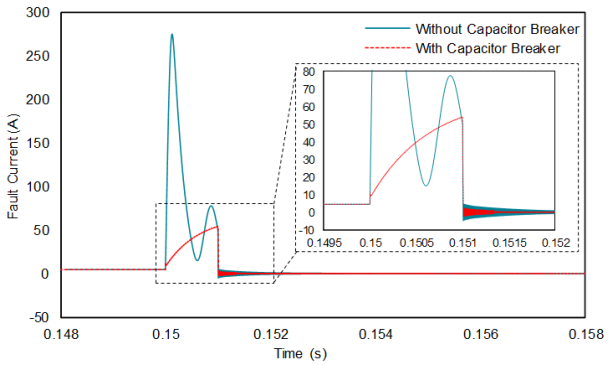

Fig. 6. Fault clearing performance of the proposed methodology for DC-DC converters in boost mode.

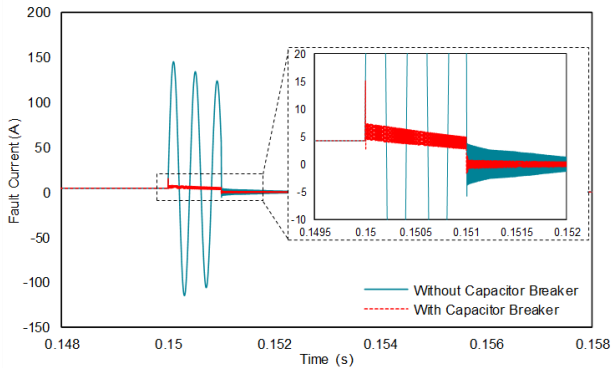

Fig. 7. Fault clearing performance of the proposed methodology for DC-DC converters in buck mode.

current can again exceed 50 per unit. Even with the addition of a capacitor breaker, the fault current may still reach up to 10 times the nominal current. This indicates that, despite the presence of the boost inductor, the grid-side inductor may not be sufficiently large to effectively limit the fault current time constant in the third fault stage.

It is important to note that the simulations assume an ideal DC source. In practical applications, boost converters are typically connected to photovoltaic modules or batteries. Particularly in the case of PV modules, the power source is inherently incapable of supplying such high fault currents. The short-circuit current of a PV module is generally no more than 15% higher than its nominal current, making a tenfold increase in fault current highly unlikely in real-world conditions.

C. DC-DC Converter in Buck Mode

Unlike the boost topology, the buck converter includes a controllable semiconductor device in the main power path, which allows it to actively interrupt the source-side contribution to fault current. Fig. 7 presents the fault current at the output of the buck converter for two defined scenarios. In both cases, the converter main semiconductor device is assumed to open with a delay of 10 microseconds following fault detection.

In the absence of a capacitor-side breaker, opening the main switch causes the output capacitor and the fault inductor to oscillate, potentially resulting in a fault current peak exceeding 30 per unit. However, when a capacitor breaker is added, the fault current is effectively limited to approximately twice the nominal current, demonstrating the strong fault-clearing capability of this topology.

More notably, in this topology, if the capacitor breaker can interrupt the capacitor discharge current before it reaches a critical level for the freewheeling diode, the main power breaker may not even be required for fault isolation. This implies that the converter can independently clear output-side faults, simplifying protection strategies.

CONCLUSION

This paper has proposed an innovative approach to fault isolation in DC systems. It is known that two key specifications of DC circuit breakers, reaction time and power loss, vary in different directions depending on the breaker technology. By strategically deploying two circuit breakers with distinct performance characteristics along different fault supply paths, the system can achieve simultaneous minimization of conduction losses and switching reaction time. Simulation results presented in this study indicate that introducing a separate fast switch in the capacitor discharge path allows the main power path breaker to be selected with up to 1000 times slower response, while keeping the fault current within acceptable limits prior to clearance. This strategy opens the possibility of using mechanical or hybrid breakers in the main power path, potentially reducing both the total losses and the physical size of the breaker assembly.

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