Stacked Josephson junctions for quantum circuit applications

Alex Kreuzer,[1] Thilo Krumrey,[1] Hossam Tohamy,[1] Alexandru Ionita,[1] Hannes Rotzinger,[1,2,*] and Alexey V. Ustinov[1,2]

[1] *Physikalisches Institut, Karlsruhe Institute of Technology, 76131 Karlsruhe, Germany*

[2] *Institute for Quantum Materials and Technologies, Karlsruhe Institute of Technology, 76131 Karlsruhe, Germany*

(Received 3 June 2025; revised 30 September 2025; accepted 14 April 2026; published 5 June 2026)

Low-loss inductors are essential components in various superconducting circuits, such as qubits or digital electronics. In this study, we investigate highly compact inductors formed by vertically stacking Josephson junctions. Our implementation employs several layers of aluminum separated by tunnel barriers. Individual stacks are connected by suspended superconducting bridges, which are free of additional dielectric materials and, therefore, should not contribute significantly to losses. We present implementation details, fabrication results, and device characterization measurements.

DOI: 10.1103/klgx-jff9

I. INTRODUCTION

The distribution of electrical currents in superconducting circuits often requires the use of inductors. This is particularly the case in quantum circuits, where dissipative circuit elements, such as resistors, are typically avoided, owing to their Nyquist contribution to the overall noise. Inductive elements are realized either by creating a magnetic field, for instance by using a sufficiently long wire, or by exploiting the kinetic energy of the charge carriers. Wires made of a material with low charge carrier density (see, e.g., [1–7]) or Josephson tunnel contacts are particularly suitable as kinetic inductors because of their small size and very low stray magnetic field. Notable applications include a variety of qubit types [8–11], compact microwave resonators [12–15], traveling-wave parametric amplifiers [16–19], tunable superconducting filters [20], or superconducting digital electronic circuits [21–26].

Arrays of Josephson junctions are advantageous when a linear current-phase relation with a high inductance is required (up to microhenrys, see, e.g., [27–29]). The junctions are typically arranged side-by-side on a dielectric substrate with dimensions ranging from micrometers to nanometers. The advantages of using junction arrays as inductors lie in their well-predictable properties and ease of fabrication.

The study of stacked junction arrays has a long history in the field of superconducting electronics. For example, stacks have been used to model the electrodynamics of layered high-temperature superconductors [30–33], to improve the properties of Josephson oscillators [34], and as lumped inductors for superconducting digital circuits [24,25].

When developing a large inductive impedance $Z = \omega L > Z_0 \approx 377\ \Omega$, it is crucial to consider the stray capacitance of the individual inductive elements. The combination of self- and stray capacitances and junction inductances gives rise to plasmonlike oscillatory modes, which can pollute the frequency spectrum and degrade device performance [35–40]. For applications requiring an extremely high impedance, an elegant approach has recently been developed, in which the planar junction array is under-etched and separated from the dielectric substrate [28,41]. Here, reducing the dimensions of the array achieves a reduction in parasitic capacitance. For very small Josephson junctions on the nanometer scale, where the Josephson energy E_J is comparable to the charging energy E_c, quantum phase fluctuations must be taken into account [9,35–38,42].

In this paper, we seek to reduce the on-chip footprint of Josephson junction arrays by employing a stacked configuration, with the ultimate objective of developing inductors for highly integrated superconducting circuits. While we adhere to the design of quantum circuits, such as the fluxonium qubit [9], possible applications are not confined to this field. We believe that the technique could be used for most of the aforementioned array applications. The proposed approach is independent of the number of junctions per stack and allows the total inductance to be tailored by varying the number of Josephson junctions

*Contact author: rotzinger@kit.edu

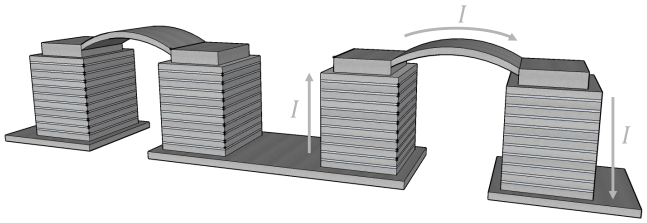

FIG. 1. Array of stacked junctions, each with a bridge arch connecting the top of two stacks. The stacks and the arches are not to scale.

and their individual kinetic inductances. Given that the footprint area of the stack A is constant, the kinetic inductance is solely dependent on the critical current density of each junction. We connect two neighboring stacks by a suspended superconducting bridge, thus adding no additional dielectric material in the vicinity of the inductor (see Fig. 1). Fabrication-imposed junction area inhomogeneities are compensated by an individual adjustment of the tunnel barrier thickness. This results in a narrower critical current distribution, as observed in the current-voltage characteristics.

The paper is organized as follows. First, we evaluate the expected stray capacitance of Josephson junction stacks. After that, we describe the fabrication process and present the measurement results for two types of Josephson junction stack.

II. STRAY CAPACITANCE ESTIMATES

We consider a pair of N-junction stacks, each with a square footprint and $N+1$ superconducting electrodes placed on a dielectric substrate. The two stacks are connected by a superconducting bridge, as sketched in Fig. 2(a). The bottom layer has a thickness h_0, an area A, and a width l; the stacks are separated by a distance d. The bridge has height h_N and width w_N (perpendicular to the arch). The thickness of the ith stacked electrode is h_i.

The two stacks connected by the bridge form an array of $2N+1$ superconducting islands, where each island i has a mutual capacitance $C_{i,j}$ with another island $j \neq i$. For neighboring islands, this is the capacitance of the junction C_J. In addition, depending on the dimensions of the stacks and the arch, the superconducting island i exhibits a stray capacitance $C_{\mathrm{stray},i}$, coupling it to more distant islands and the ground $C_{\mathrm{g},i}$ (e.g., owing to wiring or ground planes). Individual contributions of stray capacitance are estimated using a numerical finite-element solver [43]. We assume that $h_i \ll l$ and consider only the stray capacitance contribution $C_{i,i+2}$ with the next-but-one neighboring electrode (with an effective capacitor area proportional to $l \cdot h_i$). Since the bottom electrode ($i=0$) is placed directly on the substrate, we consider its stray capacitance $C_{0,i}$ with each stacked electrode within the stack. The coupling between

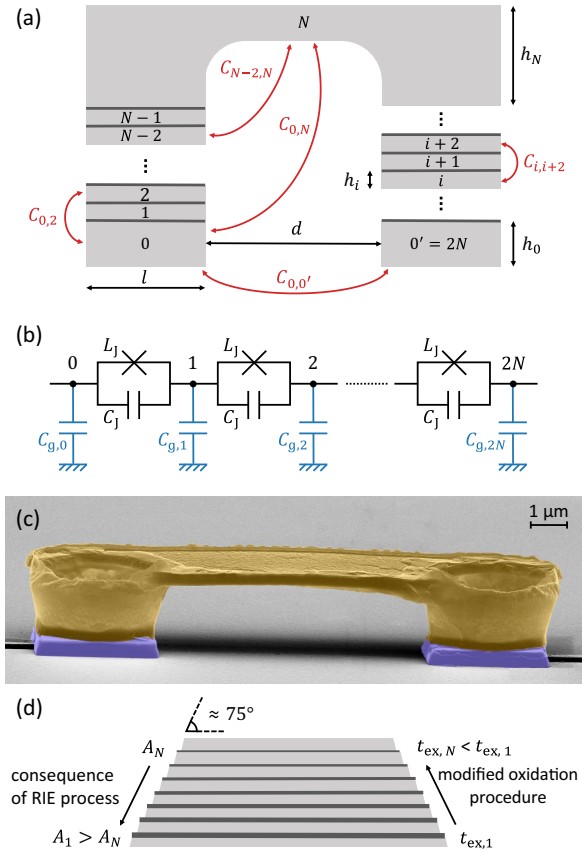

FIG. 2. (a) Two stacks connected by a bridge in side view, used to estimate the stray capacitance of superconducting islands. The width w_N of the bridge is perpendicular to the sketch plane. (b) Array of $2N$ Josephson junctions. C_J and L_J denote, respectively, the capacitance and inductance of one junction, $C_{\mathrm{g},i}$ marks the island's capacitance to ground. (c) False-color scanning electron micrograph of two stacks and an aluminum bridge (gold). Each stack consists of eight $\mathrm{Al/AlO}_x\mathrm{/Al}$ junctions (purple). (d) Stack cross section (not to scale). Reactive ion etching (RIE) of the conductor (Al) and tunnel barrier (AlO_x) results in the formation of a slanted sidewall. To compensate for the differing junction areas, the oxygen exposure is decreased from the bottom to the top.

the bottom electrodes $C_{0,0'}$ of the two connected stacks is dominated by the electric field inside the substrate (e.g., silicon, sapphire), which typically has a dielectric constant significantly higher than that of vacuum. Assuming that $h_i \approx 10$ nm and $d > 1$ µm, we neglect the contribution of the capacitance between the inner electrodes of the adjacent stacks. The stray capacitance between the bottom electrode and the arch is denoted $C_{0,N}$. We consider a narrow bridge arch with $w_N < d$ and assume a linear scaling of the stray capacitance with w_N. Since the height of the fabricated bridges h_N is comparable to their width, we take into account the stray capacitance between each stacked electrode and the arch $C_{i,N}$.

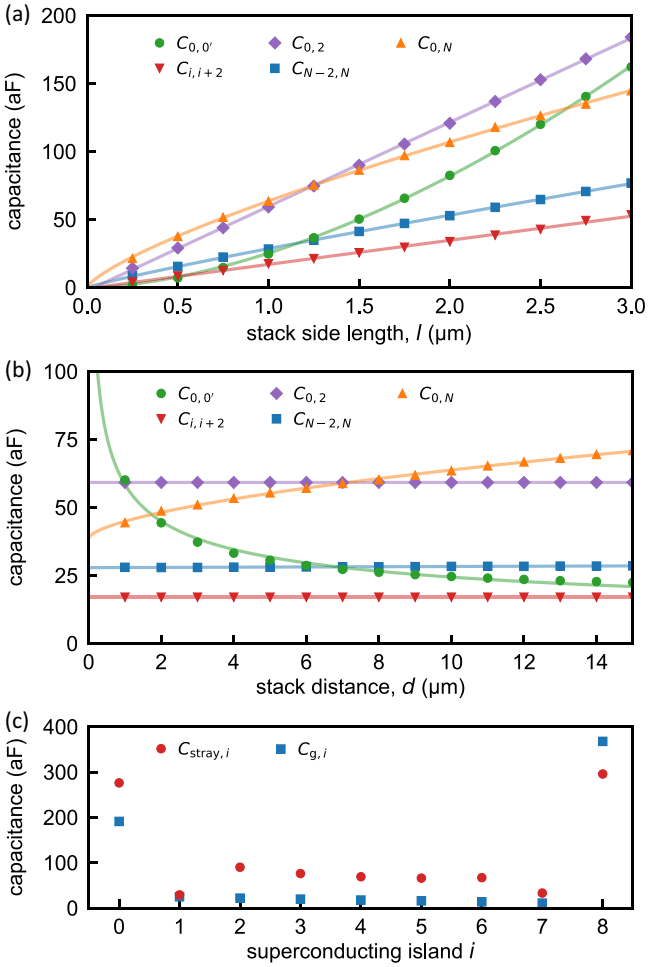

FIG. 3. Stray capacitance $C_{i,j}$ between pairs of superconducting islands of the junction stack. (a) Dependence on l (d fixed to 10 μm). (b) Dependence on d (l fixed to 1 μm). (c) Total stray capacitance $C_{\mathrm{stray},i}$ and capacitance to ground $C_{\mathrm{g},i}$ for each superconducting island in a stack. The islands $i = 0$ and $i = 8$ correspond to the bottom electrode and the bridge arch. In the three plots, the double stack arrays are modeled with the parameters $N = 8$, $h_0 = 100$ nm, $h_i = 35$ nm, $h_N = 3$ μm, and $w_N = 1$ μm.

The numerically estimated stray capacitance components are plotted in Fig. 3(a) as a function of the width of the stack l and in Fig. 3(b) as a function of the distance between the two stacks d. For all stacks with l below 3 μm, the stray capacitance is dominated by the coupling to the bottom electrode within a stack ($C_{0,2}$ and $C_{0,N}$). For footprints larger than 1 μm, the substrate contribution $C_{0,0'}$ cannot be neglected. The situation is different when considering the distance between the stacks. Here, $C_{0,0'}$ dominates for $d \leq l = 1$ μm; for large d, the capacitance $C_{0,N}$ between the bottom electrode and the arch dominates. The numerical data are fitted to polynomial functions, with parameters given in Table I.

TABLE I. Numerical results of the stray capacitance between parts of the junction array as a function of stack side length l and stack distance d (fits to the data shown in Fig. 3).

Capacitance (aF)	l (μm)	d (μm)
$C_{0,0'}$	$25 \cdot l^{1.7}$	$58 \cdot d^{-0.4}$
$C_{0,2}$	$62 \cdot l - 2$	59
$C_{0,N}$	$64 \cdot l^{0.8}$	$6 \cdot d^{0.6} + 39$
$C_{i,i+2}$	$18 \cdot l - 1$	17
$C_{N-2,N}$	$29 \cdot l^{0.9}$	28

Summation of all contributions gives the total stray capacitance of island i:

$$C_{\mathrm{stray},i} = \sum_{j \neq i} C_{i,j}\,. \tag{1}$$

The estimated $C_{\mathrm{stray},i}$ for the stacks fabricated and measured in this study (designed with $N = 8$, $l = 1$ μm, $d = 10$ μm, $h_0 = 100$ nm, $h_i = 35$ nm, $h_N = 3$ μm, and $w_N = 1$ μm) is shown in Fig. 3(c). For stacked $\mathrm{Al/AlO}_x\mathrm{/Al}$ junctions with a specific capacitance $C_{\mathrm{J}} \approx 50$ fF/μm^2 [44], the estimated stray capacitance is negligible, yielding $C_{\mathrm{stray},i}/C_{\mathrm{J}} \approx 10^{-3}$. Consequently, long-range mutual capacitance coupling [38,45] can be neglected, allowing the junction stack to be modeled as a nearest-neighbor coupled junction array, as depicted in Fig. 2(b).

The dispersion relation of the collective mode in a uniform junction array is given by

$$\omega_k = \omega_0 \sqrt{\frac{1 - \cos\left(\frac{\pi k}{N_{\mathrm{J}}}\right)}{\frac{C_{\mathrm{g}}}{2C_{\mathrm{J}}} + 1 - \cos\left(\frac{\pi k}{N_{\mathrm{J}}}\right)}} \tag{2}$$

for $k = 1, 2, \ldots, N_{\mathrm{J}} - 1$, where ω_0 is the plasma frequency of a single junction and N_{J} is the total number of junctions in the array [39]. The collective mode frequency is suppressed by the island's capacitance to ground C_{g}, in particular through the Coulomb screening of the Cooper pairs across the array, where $\lambda = \sqrt{C_{\mathrm{J}}/C_{\mathrm{g}}}$ determines the screening length [38,46,47].

The elementary block of our example array, which could be used in an element superconducting fluxonium qubit, contains eight stacked junctions with a typical $C_{\mathrm{J}} \approx 50$ fF for a size of 1 μm^2 and $L_{\mathrm{J}} \approx 1$ nH. This corresponds to a plasma frequency $\omega_0/2\pi = 1/\sqrt{L_{\mathrm{J}}C_{\mathrm{J}}} \approx 22.5$ GHz. We use the numerically estimated C_{g} for each superconducting island [Fig. 3(c)], including the capacitance to the ground plane, mutual capacitance to the surroundings of the islands, and the average ground capacitance, $\Sigma_i C_{\mathrm{g},i}/N \approx 59$ aF, to estimate the frequency of the first collective mode in the array. This corresponds to the junction capacitance-to-stray-capacitance size ratio of 50 fF/59 aF, $C_{\mathrm{J}}/C_{\mathrm{g}} \approx 850$. Using Eq. (2), we expect

$\omega_1/2\pi \approx 0.98 \cdot \omega_0/2\pi \approx 22.2$ GHz. Because of the nonmonotonic variation of the stray capacitance [see Fig. 3(c)], this only provides an estimate of the fundamental mode.

This frequency is well above the operation frequencies of typical quantum circuit applications, e.g., superconducting qubits [8–10]. For comparison, in a previously studied planar array of 200 junctions [48], the estimated ratio was $C_J/C_g \approx 35$. Masluk *et al.* [39] investigated a planar junction array specially designed to reduce stray capacitance to the ground, achieving a ratio of $C_J/C_g \approx 1000$. They reported $\omega_1/2\pi = 0.78 \cdot \omega_0/2\pi = 14.2$ GHz for an array with 80 junctions placed directly on the substrate.

As the number of junctions in a stack increases, additional islands are positioned farther away from the substrate, resulting in a decrease in C_g. In the case of a large array (where $N \gg 1$), the stray capacitance contributions of the bottom electrode and the arch become negligible. For example, with 40 stacked junctions, we estimate the capacitance to the ground $C_g \approx 15$ aF. Consequently, for a double stack array with 80 junctions, we expect the lowest mode frequency to be approximately $0.91 \cdot \omega_0/2\pi \approx 20.6$ GHz.

III. FABRICATION

The fabrication process begins with the deposition of an $Al/(AlO_x/Al)_N$ multilayer on a sapphire substrate. Each aluminum layer has a thickness of 35 nm. This is followed by an oxygen exposure to form the tunnel barrier. In the next step, the stacked junctions are defined by a square resist mask and etched in a dry $ArCl_2/ArCl_2O_2$ reactive ion etching (RIE) process using an inductively coupled plasma (ICP) tool. The etching is calibrated to stop within the bottom layer, which has a thickness of 100 nm. This layer is used for wiring and additional structures and will be defined in a later step. Finally, a bridge arch is deposited on the junction stacks using optical lithography, aluminum deposition, and $ArCl_2$ dry etching.

The fabrication result of an example array with 2×8 junctions is shown in Fig. 2(c). Here, the two square junction stacks have a footprint of approximately 3×3 μm^2, while the bridge arch has a typical height of approximately 3 μm and a length of 10 μm.

To study the dependence of the tunnel barrier on oxygen exposure, we fabricated four wafers at different base pressures and systematically varied the junction size between 1 μm^2 and 30 μm^2. Figure 4 shows the median values of 20 individual test structures for each base pressure. The data are consistent with the expected behavior of $A_{design} \propto 1/R_N^{JA}$ (solid lines). The extracted specific junction resistances are listed in Table II.

In a separate experiment, we fabricated arrays of eight junctions per stack. Here, the footprint (2×2 μm^2) and an oxygen barrier pressure (6 mbar) is kept fixed but the total number of stacks is varied. Figure 5 gives the median values of R_N^{JA} of 20 samples for each array. The data were compared with $R_N^{JA} = \rho n^b$, where n is the number of stacks and agrees well with $b = 0.96$ and $\rho = 4.8$ kΩ. From the Ambegaokar-Baratoff [49] relation, we can estimate the critical current, and thus the expected specific inductance with $L_J = \Phi_0/2\pi I_C$ as approximately 5.4 nH per stack.

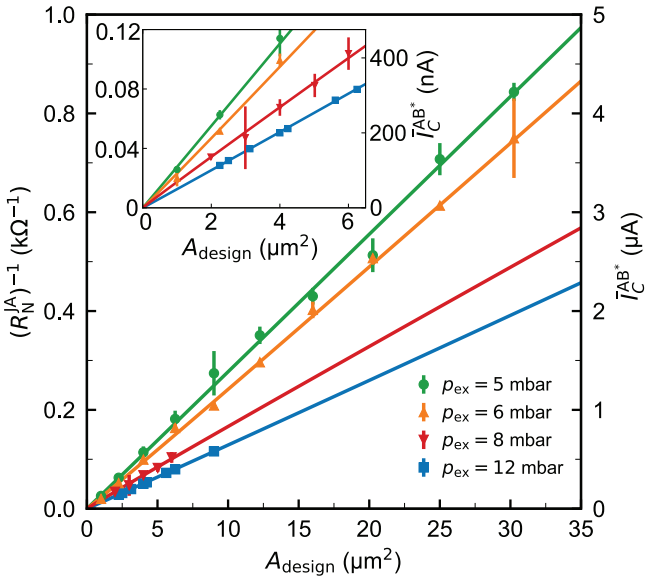

FIG. 4. Dependence of inverse normal resistance $(R_N^{JA})^{-1}$ of arrays comprising $2 \times 8 = 16$ junctions on designed junction area A_{design} for four different wafers and varied oxygen exposure pressure. Error bars indicate the standard deviation over 20 measured arrays. The y-axis on the right side gives the estimate of the derived average critical current $\bar{I}_C^{AB*}$ per junction within the array.

IV. UNCOMPENSATED JOSEPHSON JUNCTION ARRAYS

A typical current-voltage characteristic (IVC) of a sample comprising eight junctions, with a footprint of 4×4 μm^2, is shown in Fig. 6. The IVC exhibits hysteresis typical of underdamped Josephson junctions with a McCumber parameter of $\beta_C = (4I_C/\pi I_r)^2 \approx 10^3$. We measure a ratio of subgap resistance to normal resistance, R_{sg}/R_N^{JA} of about 40. From the total gap voltage of 2.84 mV, we estimate an average single junction gap voltage of $\bar{V}_{gap} \approx 355$ μV. This is close to the expected BCS value, $2\Delta/e = 360$ μV, of Al at low temperatures, see, e.g.,

TABLE II. Specific junction resistance at a given tunnel barrier oxidation pressure (same data as Fig. 4).

p_{ex} (mbar)	5	6	8	12
ρ (kΩ/μm^2)	36.3	43.2	57.5	79.6

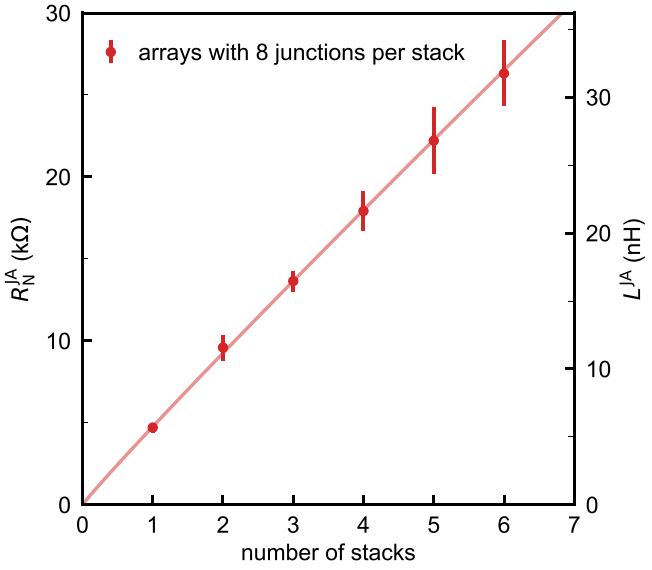

FIG. 5. Dependence of normal resistance R_N^{JA} on number of stacks (n) in arrays. Each stack consists of eight junctions with a footprint of $2 \times 2\ \mu m^2$. Error bars indicate the standard deviation over 20 measured arrays. The solid line is a fit to $R_N^{JA} = \rho n^b$ and is in good agreement with $b = 1$. The second y-axis shows an estimate for the expected inductance.

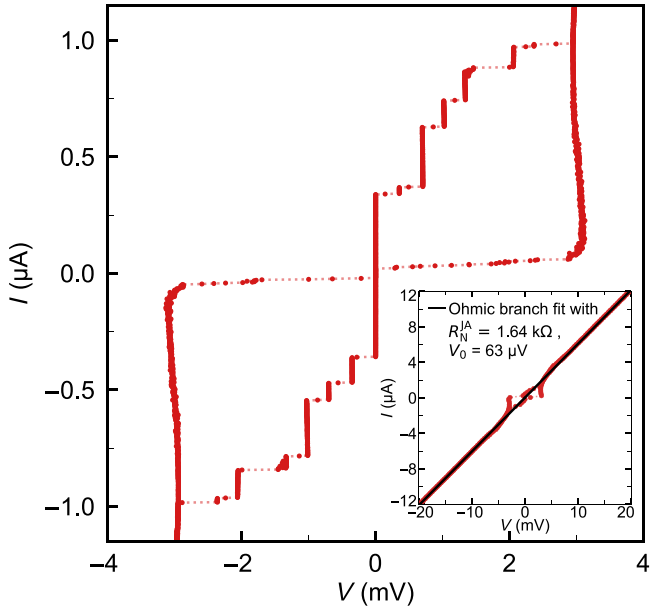

FIG. 6. Current-voltage characteristic of uncompensated array consisting of $2 \times 4 = 8$ stacked junctions with a footprint of $4 \times 4\ \mu m^2$. The individual junctions in the array switch to the normal state at bias currents between 350 nA and 1 μA. See text for details.

Lotkhov *et al.* [44]. A comparison of $V = R_N^{JA} I + V_0$, with the Ohmic branch, yields a normal resistance R_N^{JA} of 1.64 kΩ.

An interesting feature is shown on the critical current branch. Here, the IVC shows six voltage discontinuities that are multiples of $\bar{V}_{gap}$. We interpret these as reduced I_C of individual junctions in the array that switch to the normal conducting state at different bias current values. Since all junctions in the fabrication should nominally have the same current density, we attribute the distribution of I_C to a varying area of the individual junctions. This assumption is supported by scanning electron micrographs (not shown).

For most applications, it is desirable to have junctions in the array with a uniform I_C distribution, ideally with a constant I_C. Then, owing to the constant inductance fraction, the phase φ would drop equally across each junction. For small phase drops with a sufficiently large number of junctions ($\Delta\varphi < \pi/4$), the inductance contribution of each individual junction is approximately linear and the total array inductance scales with the number of junctions [50,51]. This is not the case if the critical current spread is large, since the individual contribution of junctions with a smaller I_C can then lead to significant nonlinearity.

V. COMPENSATED JOSEPHSON JUNCTION ARRAYS

We identify the RIE step as the origin of the slanted etch profile, mainly because, in the chemistry used, the aluminum is etched much more efficiently than AlO_2. This effectively leads to a staircaselike structure, visualized in Fig. 2(d). A consequence of the side wall profile is an increase of the junction area from top to bottom.

We tested two strategies to mitigate the effect of the I_C distribution in the stacks. First, we optimize the etch recipe to increase the side slope from 50° to 75°. This increases the uniformity of the individual junctions, but also allows for stacks with a much smaller footprint.

The second strategy relies on a fundamental difference between planar and stacked arrays. In most planar configurations, each Josephson junction is defined with the same tunnel barrier parameters, i.e., dielectric material and thickness. Because the tunnel barriers are subsequently fabricated in a stacked geometry, the individual barrier parameters or even the material in each layer can be tweaked. In particular, we have modified the oxidation procedure in the fabrication process to account for the different junction sizes by gradually reducing the oxidation times from the bottom to the top of the stack. The exposure of the ith stacked junction was adjusted using the well-known empirical trend for the tunnel barrier resistance as a function of oxygen exposure pressure multiplied by time, as outlined by Kleinsasser *et al.* [52]. We aim for an approximately equal R for all junctions $(E_i/E_1)^\alpha \approx A_i/A_1$, where $i = 1$ refers to the bottom junction and area A_1 of the stack. We use an empirically determined exponent $\alpha \approx 0.4$ for the exposure range of 10^2 to 10^4 mbar s.

In the deposition process, we keep the oxygen exposure pressure constant and vary the individual junction

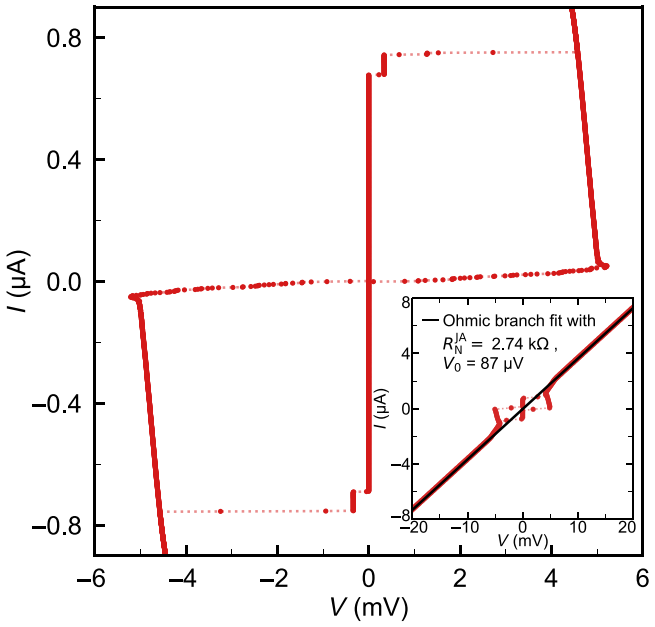

FIG. 7. *IV* curve of compensated array comprising $2 \times 8 = 16$ stacked junctions, with footprint of $3 \times 3\ \mu m^2$. Stacked junctions were oxidized with increasing exposure times to take care of the systematic change in junction area (compare with Fig. 6). Typical junction I_C are close to 750 nA. The McCumber parameter $\beta_C \approx 10^5$ and the subgap resistance to the normal resistance ratio, $R_{sg}/R_N^{JA} \approx 10^2$, with $R_{sg} \approx 100\ k\Omega$, were obtained from the measured data.

oxidation times. They are set based on the ratio of the individual area to the stack footprint, $t_{ex,i} = t_{ex,1}(A_i/A_1)^{1/\alpha}$.

Figure 7 shows the current-voltage characteristics of an array consisting of 16 junctions with a footprint of $3 \times 3\ \mu m^2$, fabricated using the compensation technique. The junctions were oxidized with decreasing exposure times from 12 to 6 min at a pressure of 5 mbar.

While most of the IVCs are very similar, the steplike structure of uncompensated arrays is no longer visible. We also note a $\beta_C \approx 10^5$ and a subgap resistance of the order of 100 kΩ ($R_{sg}/R_N^{JA} \approx 10^2$). From the Ambegaokar-Baratoff relation, we expect a critical current of 1.6 μA, which is about a factor of 2 larger than the switching current observed in the IVC. We attribute this difference to a noise or phase diffusion induced suppression. Assuming a uniform I_C distribution, we expect an inductance of 3.3 nH for the junction array. This corresponds to an impedance of approximately 124 Ω at 6 GHz, which is well below the resistance quantum $R_Q = h/(2e)^2 \approx 6.45\ k\Omega$. As this fabrication method is scalable, higher impedances can be achieved by either increasing the number of junctions or reducing their critical current.

VI. CONCLUSION

We have demonstrated that stacks of Josephson junctions can be fabricated to form compact and high-quality inductors with low stray capacitance and McCumber parameters of the order of 10^5. Area variations in the stack are compensated by fine tuning the tunnel barrier thickness, resulting in increased uniformity of the critical current. According to our estimates, stacked junction arrays have significantly lower stray capacitance than their conventional planar counterparts. The arrays can contain an almost arbitrary number of junctions and do not require additional dielectric layers, making them attractive for superconducting quantum circuit applications.

ACKNOWLEDGMENT

We acknowledge the support of Silvia Diewald and Aina Quintilla from the KIT Nanostructure Service Laboratory. This research was supported by the German Federal Ministry of Education and Research under the Research Program Quantum Systems, through the projects GeQCoS (FZK13N15691) and qBriqs (FZK13N15950).

DATA AVAILABILITY

The data that support the findings of this article are not publicly available. The data are available from the authors on reasonable request.

[1] A. Dacca, G. Gemme, R. Musenich, R. Parodi, S. Pittaluga, S. Rizzini, and V. Buscaglia, in *8th Workshop on RF Superconductivity* (Istituto Nazionale di Fisica Nucleare, Rome, Italy, 1997), p. 1103.

[2] S. Mitra, G. C. Tewari, D. Mahalu, and D. Shahar, Negative magnetoresistance in amorphous indium oxide wires, Sci. Rep. **6**, 37687 (2016).

[3] H. Rotzinger, S. T. Skacel, M. Pfirrmann, J. N. Voss, J. Münzberg, S. Probst, P. Bushev, M. P. Weides, A. V. Ustinov, and J. E. Mooij, Aluminium-oxide wires for superconducting high kinetic inductance circuits, Supercond. Sci. Technol. **30**, 025002 (2017).

[4] D. Niepce, J. Burnett, and J. Bylander, High kinetic inductance NbN nanowire superinductors, Phys. Rev. Appl. **11**, 044014 (2019).

[5] N. Kirsh, E. Svetitsky, S. Goldstein, G. Pardo, O. Hachmo, and N. Katz, Linear and nonlinear properties of a compact high-kinetic-inductance WSi multimode resonator, Phys. Rev. Appl. **16**, 044017 (2021).

[6] M. Kristen, J. N. Voss, M. Wildermuth, H. Rotzinger, and A. V. Ustinov, Random telegraph fluctuations in granular microwave resonators, Appl. Phys. Lett. **122**, 202602 (2023).

[7] M. Kristen, J. N. Voss, M. Wildermuth, A. Bilmes, J. Lisenfeld, H. Rotzinger, and A. V. Ustinov, Giant two-level systems in a granular superconductor, Phys. Rev. Lett. **132**, 217002 (2024).

[8] J. E. Mooij, T. P. Orlando, L. Levitov, L. Tian, C. H. van der Wal, and S. Lloyd, Josephson persistent-current qubit, Science **285**, 1036 (1999).

[9] V. E. Manucharyan, J. Koch, L. I. Glazman, and M. H. Devoret, Fluxonium: Single Cooper-pair circuit free of charge offsets, Science **326**, 113 (2009).
[10] F. Yan, Y. Sung, P. Krantz, A. Kamal, D. K. Kim, J. L. Yoder, T. P. Orlando, S. Gustavsson, and W. D. Oliver, Engineering framework for optimizing superconducting qubit designs, ArXiv:2006.04130.
[11] R. Kuzmin, N. Mehta, N. Grabon, and V. E. Manucharyan, Tuning the inductance of Josephson junction arrays without SQUIDs, Appl. Phys. Lett. **123**, 182602 (2023).
[12] W. Zhang, K. Kalashnikov, W.-S. Lu, P. Kamenov, T. DiNapoli, and M. E. Gershenson, Microresonators fabricated from high-kinetic-inductance aluminum films, Phys. Rev. Appl. **11**, 011003(R) (2019).
[13] J. Basset, D. Watfa, G. Aiello, M. Féchant, A. Morvan, J. Estève, J. Gabelli, M. Aprili, R. Weil, A. Kasumov, H. Bouchiat, and R. Deblock, High kinetic inductance microwave resonators made by He-beam assisted deposition of tungsten nanowires, Appl. Phys. Lett. **114**, 102601 (2019).
[14] S. Frasca, I. N. Arabadzhiev, S. Y. B. de Puechredon, F. Oppliger, V. Jouanny, R. Musio, M. Scigliuzzo, F. Minganti, P. Scarlino, and E. Charbon, NbN films with high kinetic inductance for high-quality compact superconducting resonators, Phys. Rev. Appl. **20**, 044021 (2023).
[15] M. Yang, X. He, W. Gao, J. Chen, Y. Wu, X. Wang, G. Mu, W. Peng, and Z. Lin, Kinetic inductance compact resonator with NbTiN micronwires, AIP Adv. **14**, 085027 (2024).
[16] T. C. White *et al.*, Traveling wave parametric amplifier with Josephson junctions using minimal resonator phase matching, Appl. Phys. Lett. **106**, 242601 (2015).
[17] C. Macklin, K. O'Brien, D. Hover, M. E. Schwartz, V. Bolkhovsky, X. Zhang, W. D. Oliver, and I. Siddiqi, A near–quantum-limited Josephson traveling-wave parametric amplifier, Science **350**, 307 (2015).
[18] F. Faramarzi, R. Stephenson, S. Sypkens, B. H. Eom, H. LeDuc, and P. Day, A 4–8 GHz kinetic inductance traveling-wave parametric amplifier using four-wave mixing with near quantum-limited noise performance, APL Quantum **1**, 036107 (2024).
[19] A. Giachero, M. Vissers, J. Wheeler, L. Howe, J. Gao, J. Austermann, J. Hubmayr, A. Nucciotti, and J. Ullom, Kinetic inductance traveling wave amplifier designs for practical microwave readout applications, J. Low Temp. Phys. **215**, 152 (2024).
[20] V. Kaplunenko and G. M. Fischer, Josephson junction arrays as a variable inductor in RF circuits and tunable filters, Supercond. Sci. Technol. **17**, S145 (2004).
[21] C. Altimiras, O. Parlavecchio, P. Joyez, D. Vion, P. Roche, D. Esteve, and F. Portier, Tunable microwave impedance matching to a high impedance source using a Josephson metamaterial, Appl. Phys. Lett. **103**, 212601 (2013).
[22] S. K. Tolpygo, Superconductor digital electronics: Scalability and energy efficiency issues (Review article), Low Temp. Phys. **42**, 361 (2016).
[23] S. K. Tolpygo, V. Bolkhovsky, D. E. Oates, R. Rastogi, S. Zarr, A. L. Day, T. J. Weir, A. Wynn, and L. M. Johnson, Superconductor electronics fabrication process with MoN_x kinetic inductors and self-shunted Josephson junctions, IEEE Trans. Appl. Supercond. **28**, 1100212 (2018).
[24] A. E. Fox, G. Butler, M. Thompson, P. D. Dresselhaus, and S. P. Benz, Induced current effects in Josephson voltage standard circuits, IEEE Trans. Appl. Supercond. **29**, 1101808 (2019).
[25] M. A. Castellanos-Beltran, D. I. Olaya, A. J. Sirois, P. D. Dresselhaus, S. P. Benz, and P. F. Hopkins, Stacked Josephson junctions as inductors for single flux quantum circuits, IEEE Trans. Appl. Supercond. **29**, 1300705 (2019).
[26] S. K. Tolpygo, J. L. Mallek, V. Bolkhovsky, R. Rastogi, E. B. Golden, T. J. Weir, L. M. Johnson, and M. A. Gouker, Progress toward superconductor electronics fabrication process with planarized NbN and NbN/Nb layers, IEEE Trans. Appl. Supercond. **33**, 1101512 (2023).
[27] K. Likharev, *Dynamics of Josephson Junctions and Circuits* (Gordon and Breach Science Publishers, Amsterdam, the Netherlands, 1986).
[28] I. V. Pechenezhskiy, R. A. Mencia, L. B. Nguyen, Y.-H. Lin, and V. E. Manucharyan, The superconducting quasicharge qubit, Nature **585**, 368 (2020).
[29] M. T. Bell, I. A. Sadovskyy, L. B. Ioffe, A. Y. Kitaev, and M. E. Gershenson, Quantum superinductor with tunable nonlinearity, Phys. Rev. Lett. **109**, 137003 (2012).
[30] A. V. Ustinov, H. Kohlstedt, M. Cirillo, N. F. Pedersen, G. Hallmanns, and C. Heiden, Coupled fluxon modes in stacked $Nb/AlO_x/Nb$ long Josephson junctions, Phys. Rev. B **48**, 10614 (1993).
[31] S. Sakai, A. V. Ustinov, H. Kohlstedt, A. Petraglia, and N. F. Pedersen, Theory and experiment on electromagnetic-wave-propagation velocities in stacked superconducting tunnel structures, Phys. Rev. B **50**, 12905 (1994).
[32] N. F. Pedersen and A. V. Ustinov, Fluxons in Josephson transmission lines: New developments, Supercond. Sci. Technol. **8**, 389 (1995).
[33] A. V. Ustinov and H. Kohlstedt, Interlayer fluxon interaction in Josephson stacks, Phys. Rev. B **54**, 6111 (1996).
[34] S. V. Shitov, A. V. Ustinov, N. Iosad, and H. Kohlstedt, On-chip radiation detection from stacked Josephson flux-flow oscillators, J. Appl. Phys. **80**, 7134 (1996).
[35] R. M. Bradley and S. Doniach, Quantum fluctuations in chains of Josephson junctions, Phys. Rev. B **30**, 1138 (1984).
[36] L. I. Glazman and A. I. Larkin, New quantum phase in a one-dimensional Josephson array, Phys. Rev. Lett. **79**, 3736 (1997).
[37] K. A. Matveev, M. Gisselfält, L. I. Glazman, M. Jonson, and R. I. Shekhter, Parity-induced suppression of the Coulomb blockade of Josephson tunneling, Phys. Rev. Lett. **70**, 2940 (1993).
[38] D. B. Haviland, K. Andersson, and P. Ågren, Superconducting and insulating behavior in one-dimensional Josephson junction arrays, J. Low Temp. Phys. **118**, 733 (2000).
[39] N. A. Masluk, I. M. Pop, A. Kamal, Z. K. Minev, and M. H. Devoret, Microwave characterization of Josephson junction arrays: Implementing a low loss superinductance, Phys. Rev. Lett. **109**, 137002 (2012).
[40] N. Maleeva, L. Grünhaupt, T. Klein, F. Levy-Bertrand, O. Dupre, M. Calvo, F. Valenti, P. Winkel, F. Friedrich,

W. Wernsdorfer, A. V. Ustinov, H. Rotzinger, A. Monfardini, M. V. Fistul, and I. M. Pop, Circuit quantum electrodynamics of granular aluminum resonators, Nat. Commun. **9**, 3889 (2018).

[41] C. Jünger, T. Chistolini, L. B. Nguyen, H. Kim, L. Chen, T. Ersevim, W. Livingston, G. Koolstra, D. I. Santiago, and I. Siddiqi, Implementation of scalable suspended superinductors, Appl. Phys. Lett. **126**, 044003 (2025).

[42] I. M. Pop, I. Protopopov, F. Lecocq, Z. Peng, B. Pannetier, O. Buisson, and W. Guichard, Measurement of the effect of quantum phase slips in a Josephson junction chain, Nat. Phys. **6**, 589 (2010).

[43] Ansys, Inc., ANSYS MAXWELL: Low Frequency EM Field Simulation, https://www.ansys.com/products/electronics/ansys-maxwell (2023), accessed: 2025-11-25.

[44] S. V. Lotkhov, E. M. Tolkacheva, D. V. Balashov, M. I. Khabipov, F.-I. Buchholz, and A. B. Zorin, Low hysteretic behavior of Al/AlO_xAl Josephson junctions, Appl. Phys. Lett. **89**, 132115 (2006).

[45] S. Ó Peatáin, T. Dixon, P. J. Meeson, J. M. Williams, S. Kafanov, and Y. A. Pashkin, Simulating the effects of fabrication tolerance on the performance of Josephson travelling wave parametric amplifiers, Supercond. Sci. Technol. **36**, 045017 (2023).

[46] M. V. Fistul, V. M. Vinokur, and T. I. Baturina, Macroscopic Coulomb blockade in large Josephson junction arrays, ArXiv:0806.4311.

[47] S. Feldman and A. Rogachev, Quantum phase transition in small-size 1D and 2D Josephson junction arrays: Analysis of the experiments within the interacting plasmons picture, ArXiv:2411.06492.

[48] T. Weißl, B. Küng, E. Dumur, A. K. Feofanov, I. Matei, C. Naud, O. Buisson, F. W. J. Hekking, and W. Guichard, Kerr coefficients of plasma resonances in Josephson junction chains, Phys. Rev. B **92**, 104508 (2015).

[49] V. Ambegaokar and A. Baratoff, Tunneling between superconductors, Phys. Rev. Lett. **10**, 486 (1963).

[50] D. M. Basko and F. W. J. Hekking, Disordered Josephson junction chains: Anderson localization of normal modes and impedance fluctuations, Phys. Rev. B **88**, 094507 (2013).

[51] D. V. Nguyen and D. M. Basko, Inhomogeneous Josephson junction chains: A superconducting meta-material for superinductance optimization, Eur. Phys. J. Spec. Top. **226**, 1499 (2017).

[52] A. Kleinsasser, R. Miller, and W. Mallison, Dependence of critical current density on oxygen exposure in Nb-AlO_x-Nb tunnel junctions, IEEE Trans. Appl. Supercond. **5**, 26 (1995).